MAINTENANCE MANUAL
FOR
MTD™ SERIES AND DATA RADIO
LOGIC BOARD 19D902151G3

TABLE OF CONTENTS

DESCRIPTION

Logic Board 19D902151G3 controls the operation of the MTD SERIES mobile radio. The Logic Board contains a microcontroller and associated memory circuits which include an EPROM for controller software, a programmable EEPROM to store customer System/Group Sets, frequencies and options, and RAM for controller working memory. MTX and MRX modem data from the Audio Board are controlled by a Modem IC on the Logic Board.

The Logic Board also contains latch circuitry for tone generation, data I/O and volume control. An electrically erasable potentiometer (EEPOT) is used for the volume control. In addition, the board provides the audio paths between RF Board A3, Audio Board A2 and the Control Board (Front Cap).

The logic board mounts on the bottom of the frame assembly underneath the Audio Board. A Block Diagram of the Logic Board is shown in Figure 1.

The logic board generates and receives the control signals described in Table 1

CIRCUIT ANALYSIS

A description of the symbol numbers used in the following text is contained in the Block Diagram, Outline and Schematic Diagrams, and Parts List as listed in the Table of Contents above. Also, refer to the IC/Module Data Sheets for pin out information (see Table of Contents).

MICROCONTROLLER, DECODER AND LATCH

Microcontroller U701 is an 8-bit, control-oriented microcomputer with internal input/output interface (I/O), and 256x8 random access memory (RAM). The microcontroller provides all of the radio timing and control signals. An 11.0592 MHz external crystal (Y701) is used for clocking.

Microcontroller U701 controls the following circuits:

- Synthesizer
- Transmit circuit
- Decoding of RX Data
- Generation of TX Data
- Microphone, Speaker and Data mute gates
- Generation of Signalling Tones

Ericsson GE Mobile Communications Inc.
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LBI-38616

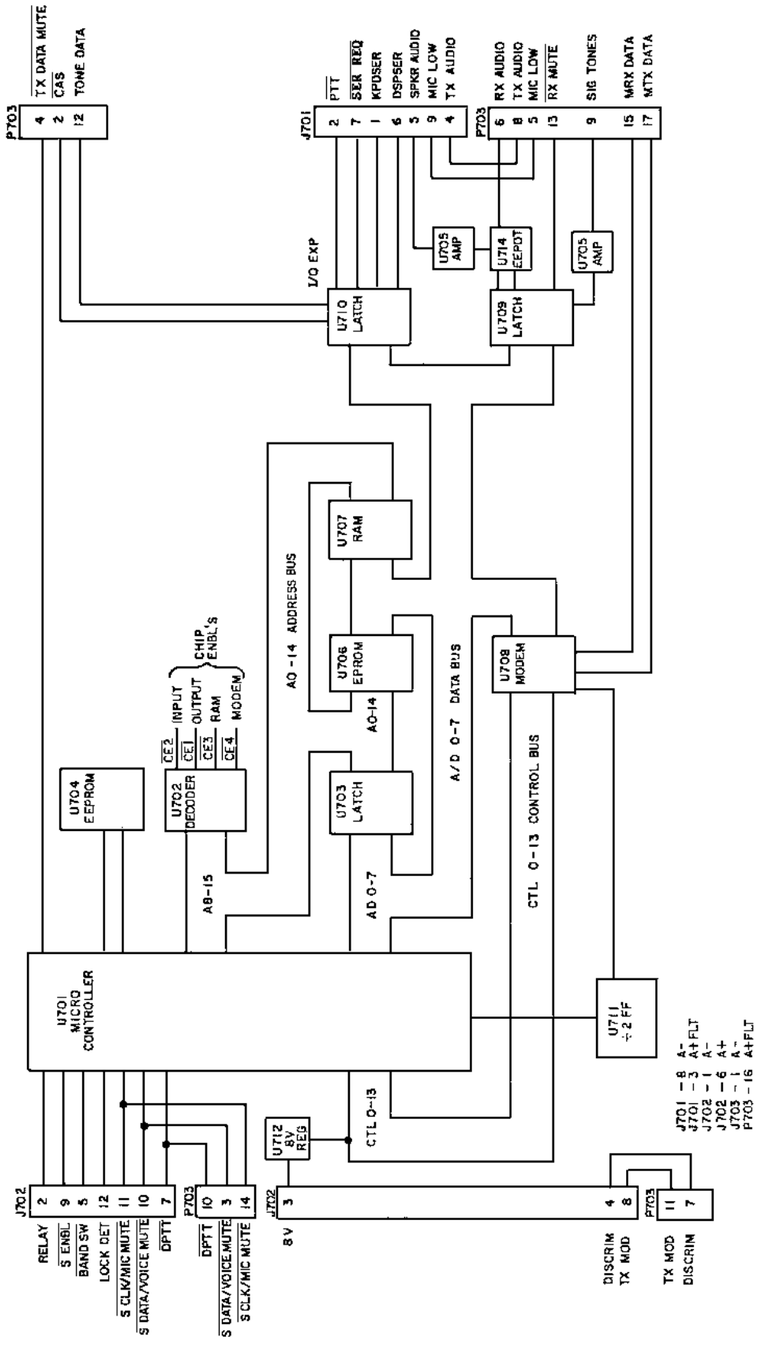


Figure 1 - Logic Board Block Diagram

Table 1 - Control Signals

RECEIVES FROM	GENERATES TO	RECEIVES FROM	GENERATES TO
AUDIO BOARD RX TONE DATA MRX DATA CAS (SQUELCH) CONTROL BOARD: (MTD) KEYPAD SERIAL PTT SER REQ	AUDIO BOARD SIGNAL TONES MTX DATA DPTT TX DATA MUTE RX MUTE MIC MUTE S DATA/VOICE MUTE CONTROL BOARD: (MTD) DISPLAY SERIAL	RF BD SYNTH: LOCK DETECT	RF BD SYNTH: S CLK/MIC MUTE S ENABLE S DATA/VOICE MUTE BAND SWITCH DPTT

Communications between the microcontroller and control board (on MTD) is by 9600 Baud serial data.

Keypad and Display Serial lines are RXD and TXD respectively are for PC Programmer operation. A 9600 Baud, RS-232 ASCII link interfaces the radio to the PC Programmer. These lines are also used in serial communications with other devices (Control Board, RDI, and external logic boards).

Two additional ICs directly support the controller. U703 is an Octal 3-state, non-inverting transparent Latch used with ALE (Address Latch Enable). U703 is used to demultiplex the controller Address/Data Bus. U702 is a three bit address to one-of-eight active low decoder outputs. It uses address lines A13, A14 and A15 as inputs, and provides Chip Enables for INPRT (U710 I/O EXP), OUTPRT (U709 D Latch), RAM (U707) and Modem (U708). NOR gate (U713) combines Read and Write to the enable signal for INPRT and OUTPRT.

ERASABLE PROM (EPROM)

EPROM U706 is a 64 K x 8 bit, ultraviolet Erasable and Electrically Programmable Read Only Memory. U706 stores all the software routines required by the controller for radio operation. The EPROM does not contain any customer specific information.

ELECTRICALLY ERASABLE PROM (EEPROM)

EEPROM U704 is a 2048 x 8 bit memory device designated the personality PROM. This personality PROM stores all required Customer information, which includes:

- Group Sets and System Sets
- Frequencies
- Options

The EEPROM can be conveniently programmed through J701 on the Logic Board without opening up the radio.

RAM

The (U707) IC is a 8 K x 8 bit, High Speed Static CMOS RAM. This IC is used by the controller for additional temporary data storage during radio operation.

MODEM AND JK FLIP FLOP

Modem chip U708 provides for transmitting and receiving 9600 or 4800 baud, high speed data. This is performed by serial/parallel and parallel/serial conversions for MTX and MRX data respectively. The controller passes and receives modem data on the parallel Data bus. Another Modem chip function is to provide for a "watchdog timer" in controller operation. Whenever the timer is not routinely set, as with a software failure, the modem IC re-initiates the system startup (powers up the radio).

LBI-38616

A 11.0592 MHz clock signal is provided for microcontroller operation by crystal Y701. A JK Flip Flop (U711) performs a divide by two function to provide the 5.5296 MHz used by the modem in the 4800 baud mode of operation.

BUS TRANSCEIVER

U710 is an Octal, 3-state, non-inverting Bus Transceiver. Grounding pin 1 of I/O expansion IC U710 permits data to pass in only one direction. CAS (Squelch) and RX Tone Data are applied to the Logic Board from the Audio Board. PTT, Serial Request, Keypad and Display Serial data are applied from the Control Unit (MTD) or external units. The output of U710 is applied to the Data Bus.

D-TYPE FLIP-FLOP AND EEPOT

U709 is an octal D-type flip- flop that is used to latch the RX MUTE, UP/DN, INC and Signal Tones from the microcontroller. Signal Tones generated by the microcontroller are latched and transformed into sine waves (digital to analog conversion) by resistor network R723. The network output is applied to Op Amp U705B for the required gain.

The UP/$\overline{DN}$ and INC signals are used to control the direction and value of EEPOT U714. The digitally controlled potentiometer has a minimum resistance of 40 ohms, and a maximum resistance of 10 K ohms. The EEPOT is adjusted in 101-ohm increments. Incrementing UP increases the speaker audio volume.

Filtering and gain is provided by Op Amp U705A.

RELAY AND VOLTAGE REGULATOR

In addition to the control and latching circuits, the Logic Board contains a horn relay circuit, a + 5 volt voltage regulator and battery voltage filter.

Horn Relay

The horn relay circuit consists of NPN buffer transistor Q702 and NPN relay driver transistor Q703. The circuit is activated by the controller for a received call, when enabled by the EEPROM. The circuit is capable of handling up to 150 milliamperes to drive an external relay coil.

VoItage Regulator

Voltage regulator U712 supplies a regulated + 5 volts DC to all of the Logic Board ICs except for Op Amp U705. U705 is supplied by the filtered A +. A reset circuit is combined with the regulator to provide the controller (via the modem chip) with a power-up signal for startup or restarts. The + 8 volts DC is supplied to U712 from 8-volt regulator U102 located on the RF Board.

Battery Voltage Filter

Transistor circuit Q704 operates as a filter circuit for the A + battery voltage. This circuit is used to reduce "alternator whine" interference. The filtered A + (13 Volts DC) is used on the Audio Board. Transistors Q708 and Q707 provide surge protection for Q704 by automatically shutting down if an over current condition is sensed at J701. Reset occurs when power is re-applied to the unit.

9600 AND 4800 BAUD OPERATION

For 4800 Baud operation, the jumper, P706, is installed on J706 pins 1 and 2. This enables the • 2 clock to the modem U708.

For 9600 Baud operation, the jumper, P706, is installed on J706 pins 2 and 3. This enables the crystal clock to modem U708.

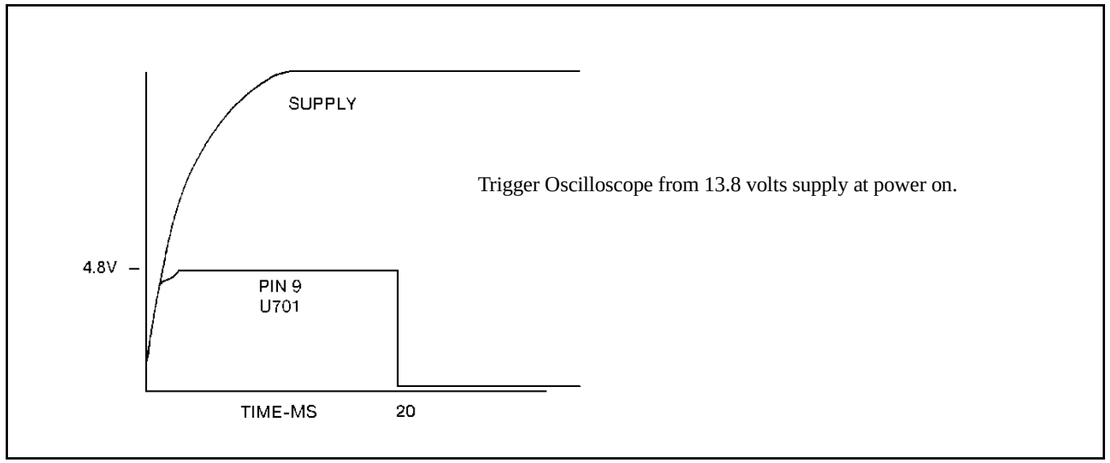
LOGIC BOARD QUICK CHECKS

If a faulty Logic Board is suspected, it can be confirmed by substitution of a known good board.

DC CHECKS

Power for the Logic Board is supplied by the 8 volts on J702, Pin 3. This conies the + 8-Volt Regulator (U102) located on the RF Board.

1. Check for +5 ±0.25 volts on U712, Pin 5.
2. Check the Microcontroller Reset line (U701, Pin 10). If Reset is occurring, check the Regulator U705, Pin 2 and Q701. See Figure 2 for Reset Waveform.
3. Check for oscillator activity by examining the ALE clock on U701, Pin 33 (see Figure 3). If not present, examine the system clock on U701, Pin 20. The presence of a system clock but no ALE may indicate that U701 is defective. If the system clock is not present, check Y701 and related components.
4. All output lines from the Microcontroller are pulled to + 5 Volts through 50 K-Ohm resistors inside the Microcontroller. If a line is high, you may ground that pin and monitor the results. Service Note: If a line is low, the line may not be forced to + 5 Volts.



Trigger Oscilloscope from 13.8 volts supply at power on.

Figure 2 - Reset Waveform

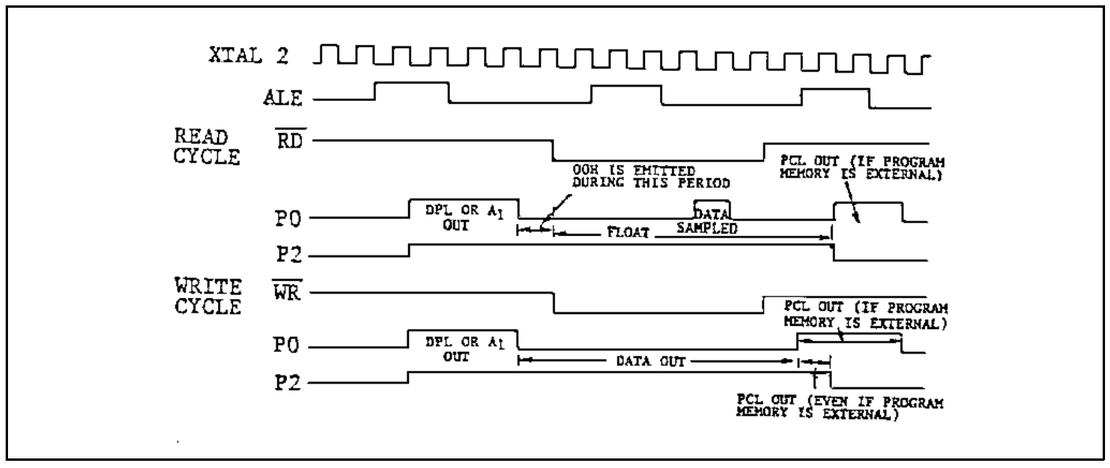
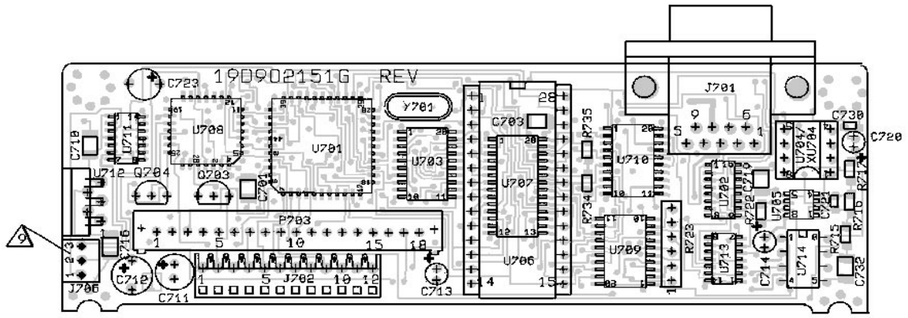


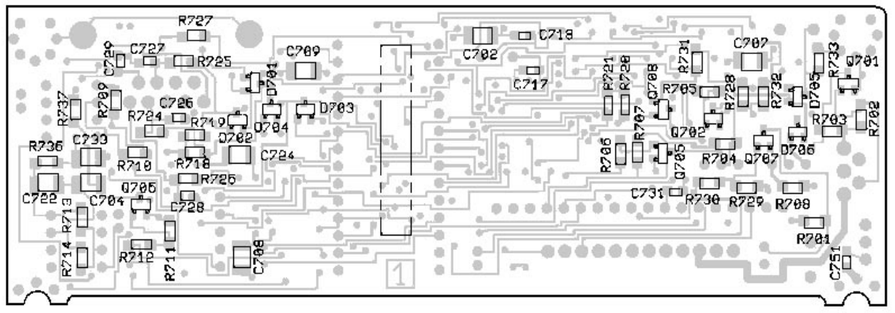
Figure 3 - Timing Waveforms

COMPONENT SIDE



(19D902151, Sh. 3, Rev. 1)
(19D902860, Component side Rev. 1)

SOLDER SIDE



(19D902151, Sh. 3, Rev. 1)
(19D902860, Solder side Rev. 1)

LEAD IDENTIFICATION
FOR Q703 & Q704

IN-LINE
TOP VIEW
NOTE; CASE SHAPE IS DETERMINING
FACTOR FOR LEAD IDENTIFICATION

LEAD IDENTIFICATION
FOR Q701, Q702, Q705-Q708
(TOP VIEW)

LEAD IDENTIFICATION
FOR D701-D706
(TOP VIEW)

CAUTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

LOGIC BOARD
19D902151G3

PARTS LIST

LOGIC BOARD
19D902151G3
ISSUE 2

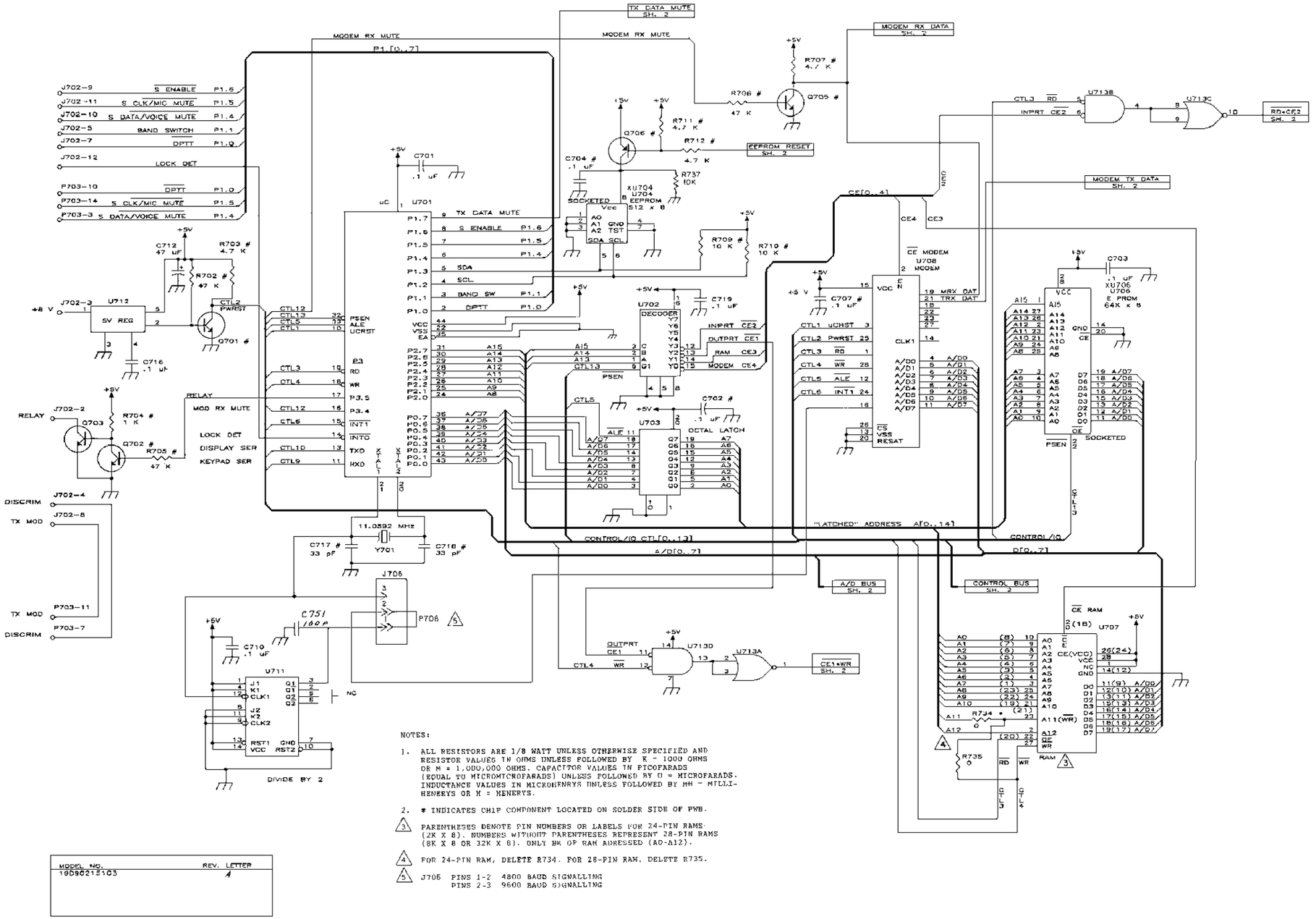
SYMBOL	GE PART NO.	DESCRIPTION
		- - - - - - - - - - CAPACITORS - - - - - - - - - -
C701 thru C704	19A702052P26	Ceramic: 0.1 uF ±10%, 50 VDCW.
C707 thru C710	19A702052P26	Ceramic: 0.1 uF ±10%, 50 VDCW.
C711	19A704879P15	Electrolytic: 47 uF ±20%, 35 VDCW.
C712	19A701534P9	Tantalum: 47 uF ±20%, 6.3 VDCW.
C713	19A704879P8	Capacitor, Electrolytic: 2.2uF ±20%, 50 VDCW.
C714	19A704879P5	Electrolytic: 10 uF ±20%, 16 VDCW.
C716	19A702052P26	Ceramic: 0.1 uF ±10%, 50 VDCW.
C717 and C718	19A702061P37	Ceramic: 33 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C719	19A702052P26	Ceramic: 0.1 uF ±10%, 50 VDCW.
C720	19A704879P5	Electrolytic: 10 uF ±20%, 16 VDCW.
C721	19A702061P77	Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C722	19A702052P26	Ceramic: 0.1 uF ±10%, 50 VDCW.
C723	19A703314P9	Electrolytic: 4.7 uF -10+50% tol, 50 VDCW; sim to Panasonic LS Series.
C724	19A702052P26	Ceramic: 0.1 uF ±10%, 50 VDCW.
C726 thru C731	19A702061P77	Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C732 and C733	19A702052P26	Ceramic: 0.1 uF ±10%, 50 VDCW.
C751	19A702061P61	Ceramic: 100 pF ±5%, 50 VDCW.
		- - - - - - - - - - DIODES - - - - - - - - - -
D701 thru D706	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99.
		- - - - - - - - - - JACKS - - - - - - - - - -
J701	19B209727P40	Connector.
J702	19A704779P11	Connector; sim to Molex 22-17-2122.
J706	19A703248P11	Post: Gold Plated, 10 mm length.
		- - - - - - - - - - PLUGS - - - - - - - - - -
P703	19A704874P1	Connector: sim to: Elco 00-9021-18-12-00-339.
P706	19A702104P2	Connector, jumper.
		- - - - - - - - - - TRANSISTORS - - - - - - - - - -
Q701 and Q702	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q703 and Q704	19A702503P2	Silicon, NPN: sim to 2N4401.
Q705	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q706 and Q707	19A700059P2	Silicon, PNP: sim to MMBT3906.
Q708	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R701	19B800607P560	Metal film: 56 ohms ±5%, 1/8 w.
R702	19B800607P473	Metal film: 47K ohms ±5%, 1/8 w.
R703	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R704	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R705 and R706	19B800607P473	Metal film: 47K ohms ±5%, 1/8 w.
R707	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R708	19B800607P2R2	Metal film: 2.2 ohms ±5%, 1/8 w.
R709 and R710	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R711 thru R713	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R714	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R715	19B800607P473	Metal film: 47K ohms ±5%, 1/8 w.
R716	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R717	19B800607P560	Metal film: 56 ohms ±5%, 1/8 w.
R718 thru R721	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R722	19B800607P332	Metal film: 3.3K ohms ±5%, 1/8 w.
R723	19A704885P5	Resistive Network: ±2%, 1/8 w.
R724 thru R727	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R728	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R729	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R730	19B800607P332	Metal film: 3.3K ohms ±5%, 1/8 w.
R731 and R732	19B800607P272	Metal film: 2.7K ohms ±5%, 1/8 w.
R733	19B800607P473	Metal film: 47K ohms ±5%, 1/8 w.
R734	19B800607P1	Metal film: Jumper.
R736	19B800607P473	Metal film: 47K ohms ±5%, 1/8 w.
R737	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
		- - - - - - - - - - INTEGRATED CIRCUITS - - - - - - - - - -
U701	19A705557P2	Digital: 8-Bit Microcomputer; sim to C80C32.
U702	19A704445P101	Digital: CMOS 1-of-8 Decoder/Demulti- plexer; sim to 74HC138.
U703	19A703471P302	Digital: Octal Data Latch; sim to 74HC373.
U704	19A705553P1	EEPROM: sim to 24C16
U705	19A116297P7	Linear: Dual Op Amp; sim to MC4558CD.
U706	19A705551P1	EPROM: 64K x 8; sim to TI 27C512.
U707	19A705603P2	Digital: 8K x 8-Bit Static CMOS RAM; sim to uPD4464G-200.
U708	19A704727P15	Digital: Modem.
U709	19A704380P311	Digital: CMOS Octal Data Flip-Flop; sim to 74HC273.
U710	19A703471P308	Digital: Octal Tri-State Transceiver; sim to 74HC245.
U711	19A704380P301	Digital: CMOS Dual J-K Flip-Flop; sim to 74HCT107.
U712	19A704970P1	Linear: 5 Volt Regulator with Reset Output; sim to SGS L387.
U713	19A703483P301	Digital: CMOS Quad 2-Input NOR Gate; sim to 74HC02.
U714	19A705180P2	Digitally Controlled Potentiometer: 40 - 10K ohms; sim to X9103P.
		- - - - - - - - - - SOCKETS - - - - - - - - - -
XU704	19A700156P15	Socket, IC: 8 Pins, Tin Plated.
XU706	19B801736P3	Socket, Strip: 14 pins on .1" centers, tin plated.
		- - - - - - - - - - CRYSTALS - - - - - - - - - -
Y701	19A702511G15	Quartz: 11.059200 MHz.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

PRODUCTION CHANGES

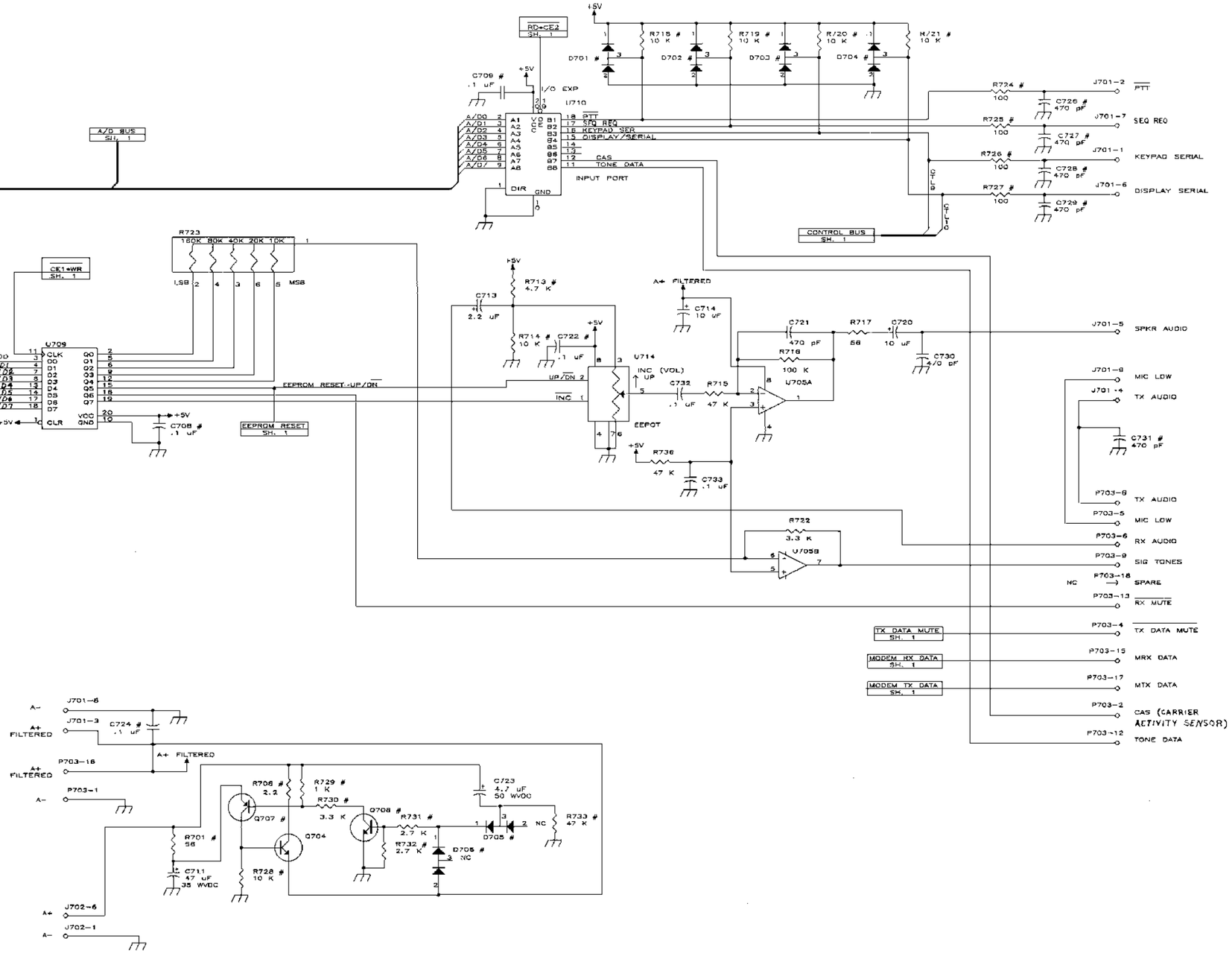
Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter" which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

REV. A LOGIC BOARD 19D902151G3
To eliminate RF spare, capacitor C751 added. PWB revised to eliminate manual mode to board.



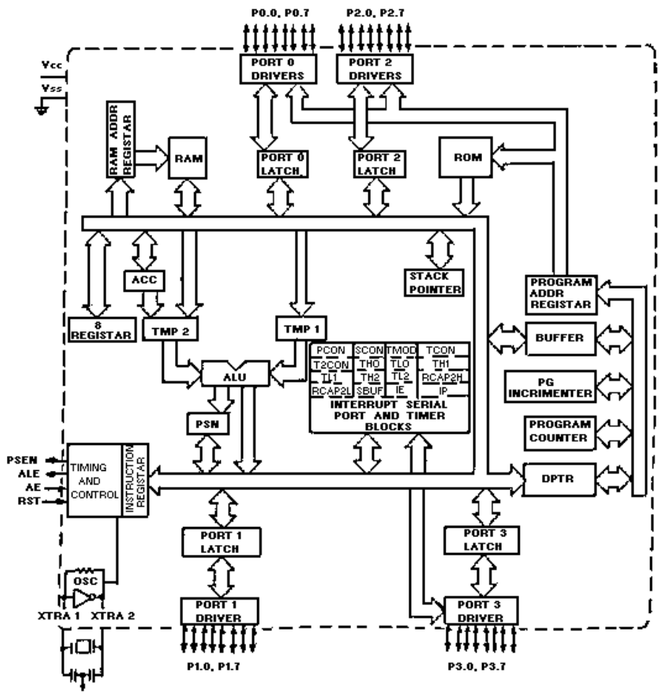
LOGIC BOARD 19D902151G3

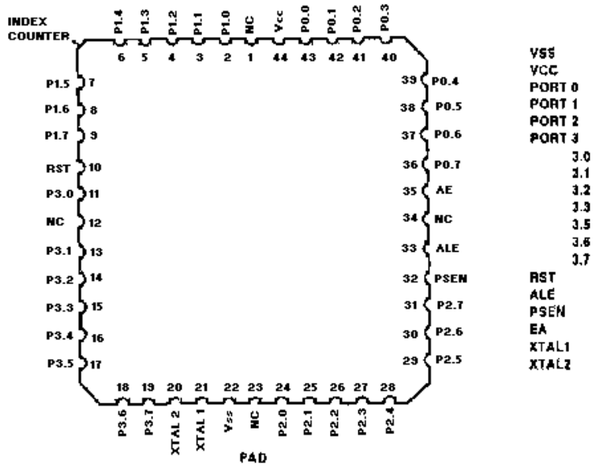
(19D902861, Sh. 1, Rev. 1)



LOGIC BOARD
19D902151G3
(19D902861, Sh. 2, Rev. 1)

FUNCTION DIAGRAM

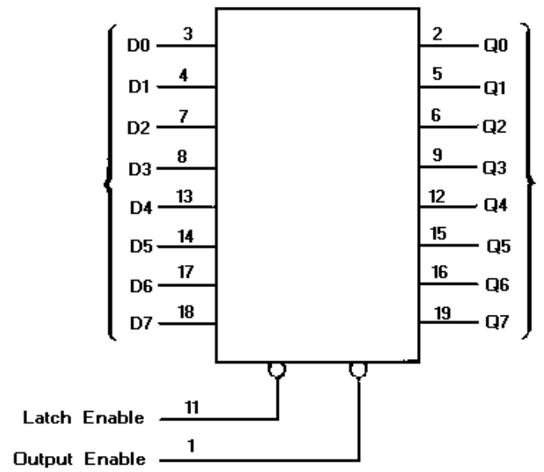




VSS	CIRCUIT GROUND POTENTIAL.
VCC	+5V POWER SUPPLY
PORT 0	8—BIT OC BI-DIRECTIONAL I/O PORT.
PORT 1	8—BIT QUASI-BIDIRECTIONAL I/O PORT.
PORT 2	8—BIT QUASI-BIDIRECTIONAL I/O PORT.
PORT 3	8—BIT QUASI-BIDIRECTIONAL I/O PORT.
3.0	RXD — SERIAL PORT RECEIVER DATA.
3.1	TXD — SERIAL PORT TRANSMITTER DATA.
3.2	INT0 — INTERRUPT 0 INPUT.
3.3	INT1 — INTERRUPT 1 INPUT.
3.5	T1 — COUNTER 1 INPUT.
3.6	WR — WRITE CONTROL.
3.7	RD — READ CONTROL.
RST	RESET.
ALE	ADDRESS LATCH ENABLE.
PSEN	PROGRAM STORE ENABLE OUTPUT.
EA	INTERNAL/EXTERNAL INSTRUCTION FETCH.
XTAL1	INPUT TO OSCILLATOR AMPLIFIER.
XTAL2	OUTPUT FROM OSCILLATOR AMPLIFIER.

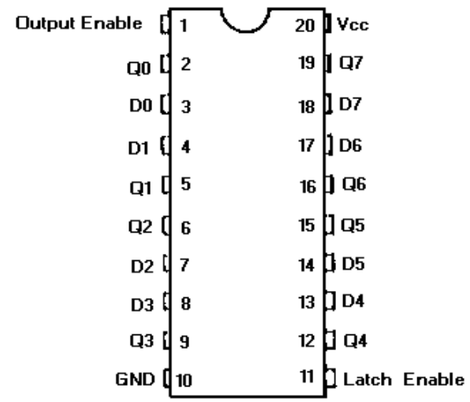
MICROCONTROLLER U701
19A705557P2

BLOCK DIAGRAM



Pin 20 = Vcc
Pin 10 = GND

PIN ASSIGNMENT



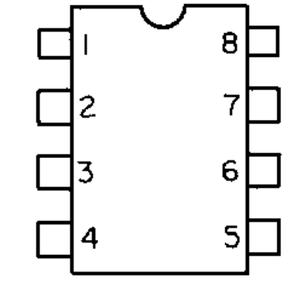
FUNCTION TABLE

Output Enable	Latch Enable	D	Output
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

OCTAL DATA LATCH U703
19A703471P302

PIN CONFIGURATION

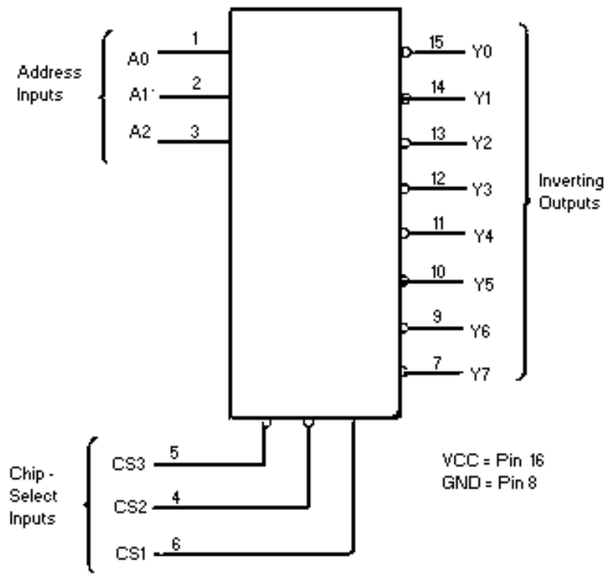


FUNCTIONS

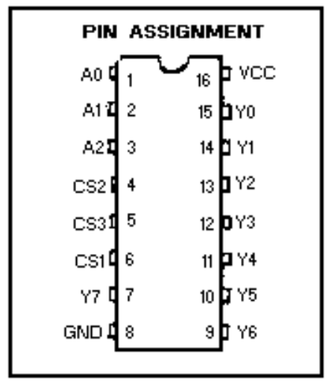
1 TO 3	A0 TO A2 ADDRESS INPUTS
4	Vss
5	SDA SERIAL DATA
6	SCL SERIAL CLOCK
7	TEST INPUT→ TO Vss
8	Vcc

EEPROM U704
19A705553P1

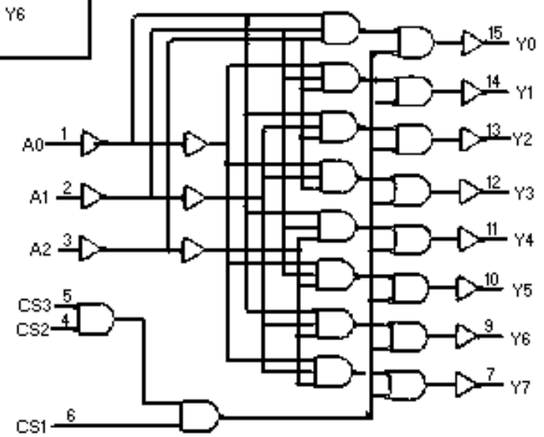
BLOCK DIAGRAM



PIN ASSIGNMENT



LOGIC DIAGRAM



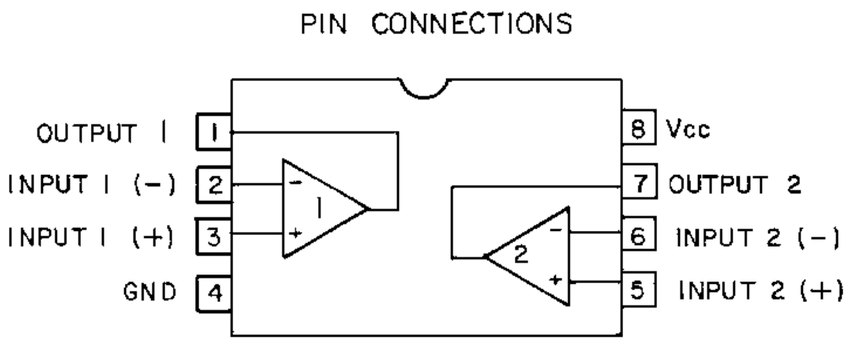
FUNCTION TABLE

Inputs						Outputs							
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

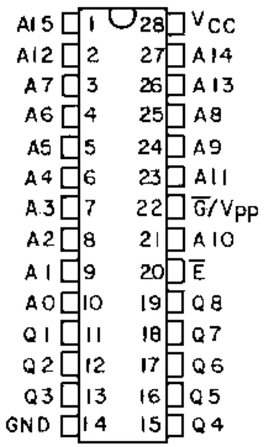
H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care

DECODER U702
19A704445P101

PIN CONNECTIONS



DUAL OP AMP U705
19A116297P7



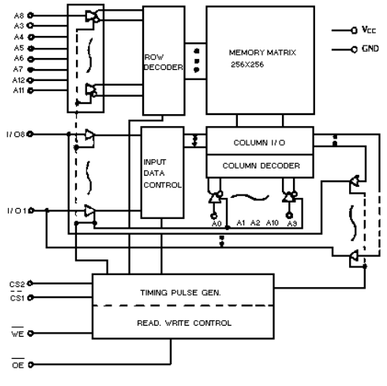
PIN NOMENCLATURE	
A0 - A15	Address Inputs
$\overline{E}$	Chip Enable/Power On
GND	Ground
Q1 - Q8	Outputs
Vcc	5-V Power Supply
$\overline{G}$/Vpp	12.5-V Power Supply/ Output Enable

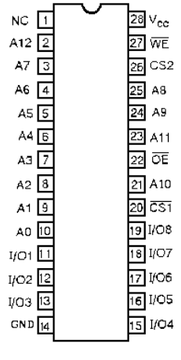
EPROM U706
19A705551P1

TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O	Icc
X	H	X	X	Not Selected	High Z	Standby
X	X	L	X	Not Selected	High Z	Standby
H	L	H	H	Output Disabled	High Z	Active
H	L	H	L	Read	Dout	Active
L	L	H	H	Write	Din	Active
L	L	H	L	Write	Din	Active

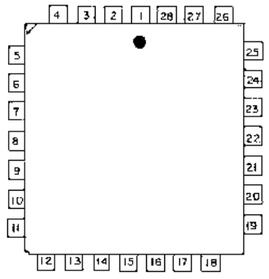
X= H or L

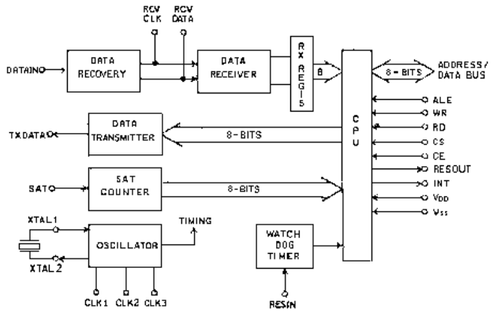




STATIC RAM 8K x 8 U707
19A705603P2

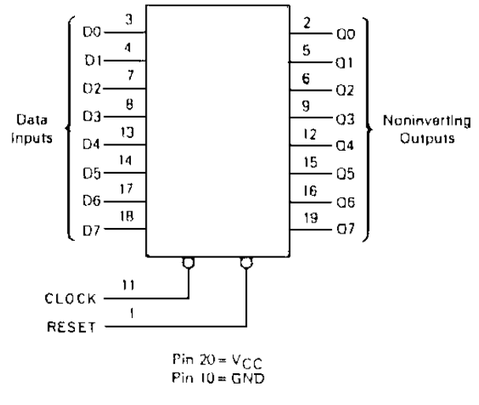
PIN	NAME	FUNCTION
1	RD	READ ENABLE (ACTIVE LOW)
2	CE	CHIP ENABLE (ACTIVE LOW)
3	RESOUT	RESET OUTPUT (ACTIVE HIGH)
4	AD0	BI-DIRECTIONAL A/D BUS
5	AD1	BI-DIRECTIONAL A/D BUS
6	AD2	BI-DIRECTIONAL A/D BUS
7	AD3	BI-DIRECTIONAL A/D BUS
8	AD4	BI-DIRECTIONAL A/D BUS
9	AD5	BI-DIRECTIONAL A/D BUS
10	AD6	BI-DIRECTIONAL A/D BUS
11	AD7	BI-DIRECTIONAL A/D BUS
12	ALE	ADDRESS LATCH ENABLE (ACTIVE HIGH)
13	V_{SS}	GROUND
14	CLK1	BUFFERED OSCILLATOR OUTPUT
15	V_{DD}	+5 VOLT SUPPLY
16	XTAL1	OSCILLATOR INPUT
17	XTAL2	OSCILLATOR OUTPUT
18	CLK2	CLOCK OUTPUT
19	RXDATA	RECEIVED DATA INPUT
20	SAT	RECEIVED SAT INPUT
21	TXDATA	TRANSMIT DATA OUTPUT
22	RCVCLK	RECOVERED CLOCK OUTPUT
23	RCVDAT	RECOVERED DATA OUTPUT
24	INT	INTERRUPT REQUEST (ACTIVE LOW)
25	RESIN	RESET INPUT (ACTIVE HIGH)
26	CS	CHIP SELECT (ACTIVE LOW)
27	CLK3	TRANSMIT CLOCK OUTPUT
28	WR	WRITE ENABLE (ACTIVE LOW)



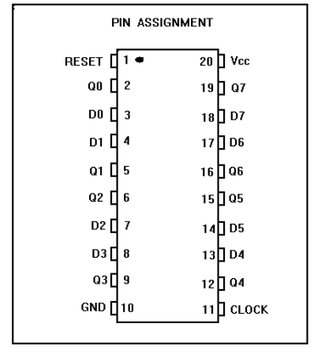


MODEM U708
19A704727P5

LOGIC DIAGRAM



PIN ASSIGNMENT

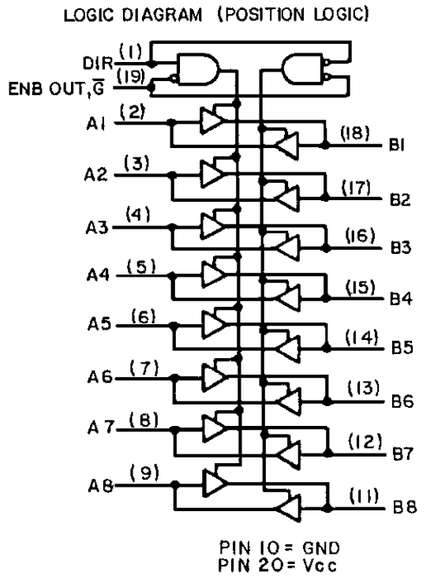


FUNCTION TABLE

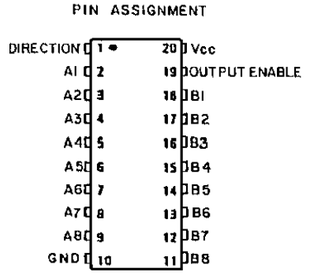
INPUT			OUTPUT
RESET	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	NO CHANGE
H	↓	X	NO CHANGE

OCTAL DATA FLIP-FLOP U709
19A704380P311

LOGIC DIAGRAM (POSITION LOGIC)



PIN ASSIGNMENT

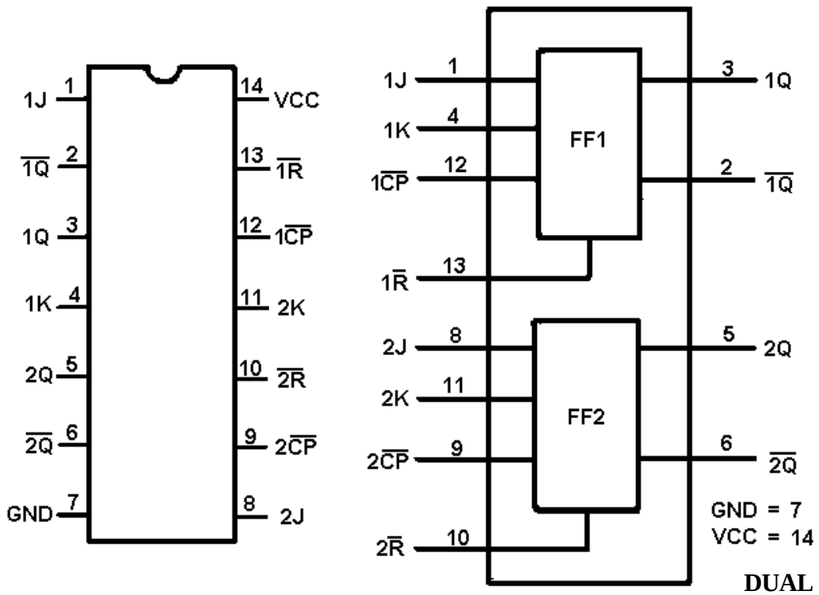


FUNCTION TABLE

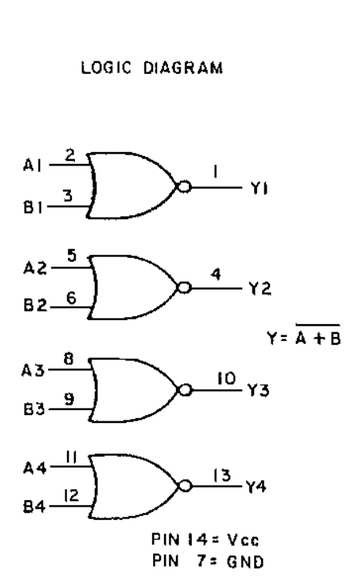
CONTROL INPUTS		OPERATION
OUTPUT ENABLE	DIRECTION	
L	L	DATA TRANSMITTED FROM BUS B TO BUS A
L	H	DATA TRANSMITTED FROM BUS A TO BUS B
H	X	BUSES ISOLATOR (HIGH IMPEDANCE STATE)

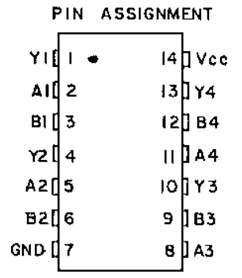
X=DON'T CARE

OCTAL TRI-STATE TRANSCEIVER U710
19A703471P308



DUAL J-K FLIP-FLOP U711
19A704380P301

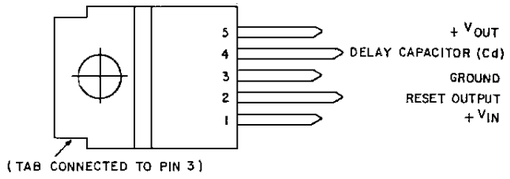


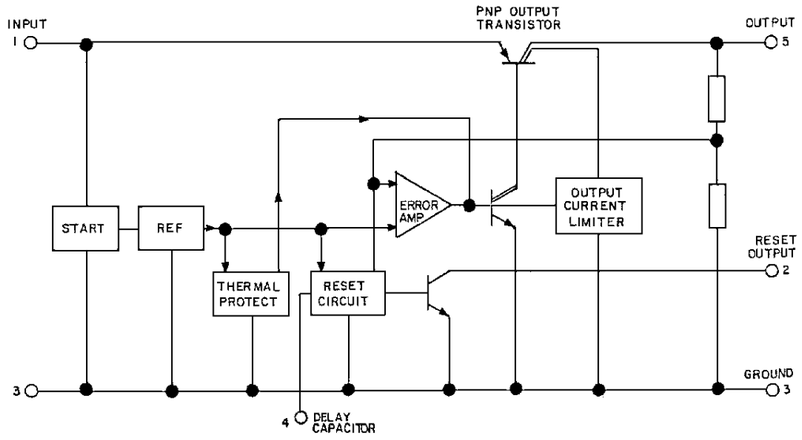


FUNCTION DIAGRAM

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

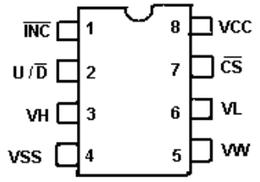
QUAD 2-INPUT NOR GATE U713
19A703483P301





5 VOLT REGULATOR U712
19A704970P1

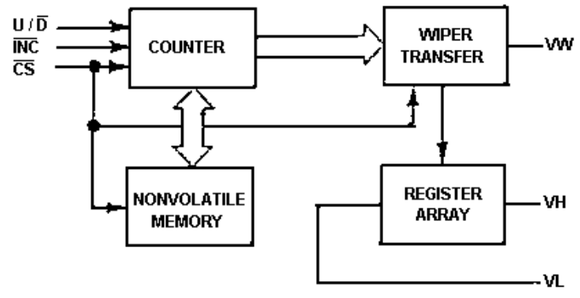
PIN CONFIGURATION



PIN NAME

VH	HIGH TERMINAL OF POT
VW	WIPER TERMINAL OF POT
VL	LOW TERMINAL OF POT
VSS	GROUND
VCC	SYSTEM POWER
U/D	UP/DOWN CONTROL
INC	WIPER MOVEMENT CONTROL
CS	CHIP SELECT

FUNCTIONAL DIAGRAM



DIGITALLY CONTROLLED POTENTIOMETER U714
19A705180P2