ADDENDUM NUMBER 1 TO MAINTENANCE MANUAL
LBI-38641F
Refer to ECO#20026373
ADDENDUM NUMBER 1 TO MAINTENANCE MANUAL
LBI-38641F
Refer to ECM#200/26373

VHF RECEIVER SYNTHESIZER MODULE 19D902781G1
(19D903621, Sh. 2, Rev. 5)
ADDENDUM NUMBER 1 TO MAINTENANCE MANUAL
LBI-38641F
Refer to ECOM#20026373

VHF RECEIVER SYNTHESIZER MODULE 19D902781G2
(19D903769, Sh. 1, Rev. 4)
ADDENDUM NUMBER 1 TO MAINTENANCE MANUAL
LBI-38641F
Refer to ECO#20026373

VHF RECEIVER SYNTHESIZER MODULE 19D902781G2
(19D902781G2, Sh. 2, Rev. 4)
GENERAL

The addendum identifies production changes to the MASTR® III VHF Receiver Synthesizer Module 19D902781G1 & G2. New diagrams are also included.

PRODUCTION CHANGE

Rev. 2A Receiver Synthesizer Module 19D902780G1 & G2
To reduce RF emissions, the conductive connector grommet was replaced with a thicker part to ensure contact with the front panel at RF connectors. RF Shielding Grommet was changed from 19B802690P1 to 19D802690P2.
VHF RECEIVER SYNTHESIZER MODULE
19D902781G1 & G2

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DESCRIPTION

The Receiver Synthesizer Module provides the local oscillator signal (LO) to the Receiver Front End Module of the MASTR III base station. The module also provides the reference oscillator signal to the transmitter synthesizer. Receiver Synthesizer Module 19D902781G1 (Group 1) generates an output injection signal in the 157 to 172 MHz range, and 19D902781G2 (Group 2) generates a signal in the 129 to 152 MHz range.

The Receiver Synthesizer Module is a phase-locked loop (PLL) design, as shown in the block diagram (Figure 1). Its output is generated directly by the VCO Q1 and buffered by Monolithic Microwave Integrated Circuits (MMIC) U1 and U3.

The logic signals from controller (U10, 12, and 13) determine the synthesizer frequency. Frequency stability is maintained by either using the internal reference oscillator Y1 or by applying a high precision reference signal to the EXT Reference Oscillator Port J4. The internal reference oscillator is a temperature controlled crystal oscillator (TCXO) operating at 12.8 MHz. The oscillator has a stability of ± 1.5 ppm over the temperature range of -30°C to +75°C. See the table containing General Specifications for the minimum external oscillator specifications.

The buffered VCO output is sampled by the resistive splitter and conditioned by buffer amplifier U2. It is then fed to the divide by 64/65 dual modulus prescaler U5. The divided output from the prescaler is connected to the F_in input of the PLL U6. Within the PLL, the divided VCO input signal F_in is divided again. The PLL also divides down the 12.8 MHz reference signal. Three inputs from the controller: ENABLE, CLOK, and serial DATA program the PLL divider circuits.
The divided reference signal and the divided VCO signal are compared in the PLL phase detector. When the reference and VCO signals are identical, the PLL phase detector generates a constant DC output voltage. This voltage is buffered by U8 and filtered by the loop filter circuit. It is then applied to Q1 setting the VCO on frequency.

If the compared frequencies (phases) differ, an error voltage is generated which adjusts the VCO frequency. During this out-of-lock condition, the PLL also sends a Lock Detect signal (LD) to the controller and lights the FAULT LED on the front panel of the module.

### CIRCUIT ANALYSIS

The Receiver Synthesizer Module consists of the following circuits:

- Voltage Controlled Oscillator
- Buffer Amplifiers
- Reference Oscillator and Buffer
- Prescaler and Synthesizer
- Loop Filter
- Digital Control
- Voltage Regulators

### VOLTAGE CONTROLLED OSCILLATOR

The free running Voltage Controlled Oscillator (VCO) is composed of a grounded-gate JFET (Q1) and associated circuitry. Inductor L10 and associated capacitors form the resonant tank circuit. The circuit’s use of high Q components minimizes phase noise.

Frequency tuning of the VCO is done by changing the DC output voltage level from the loop filter U14. The Loop Filter Out signal from U14 is routed through L4 and R3 and applied to the two varicap diodes D4 and D5. The voltage level applied determines the diodes’ capacitance and sets the resonant frequency of the oscillator. If the VCO drifts or the frequency is changed, the DC voltage level changes causing the VCO’s resonant frequency to change. The output of the oscillator is then applied to a buffer amplifier: Course adjustment of frequency is done by adjusting trimmer capacitor C52 while applying a calibration voltage to the V_TUNE line connected to U14.4-11.

### BUFFER AMPLIFIERS

The MMIC Buffer Amplifier stage is composed of three MMICs (U1, U2, and U3) and a resistive splitter. The amplifiers serve two purposes: amplifying the local oscillator signal (LO OUTPUT) for injection into the Receiver Front End assembly and providing a feedback signal to the synthesizer Phase-Locked Loop (PLL).
Integrated circuits U1 and U3 provide amplification of the local oscillator signal. The output of U1 is fed to a resistive signal splitter composed of R13 through R18. One of the resistive signal splitter outputs drives amplifier U3. The U3 output signal is coupled by C17 to a low-pass filter network (C24 and C25, L6, L8, and L9) and a resistive pad (R25, R26 and R30) for isolation. The local oscillator signal is finally routed to J2, LO OUT, for connection to the Receiver Front End Assembly. The LO output level at BNC connector J3 is nominally 0 dBm.

The other output of the resistive signal splitter drives U2. The amplified output from U2, PRESCALER BUFFER OUT, is coupled to the 50 ohm input of the prescaler U5 via capacitors C16 and C45.

REFERENCE OSCILLATOR AND BUFFER

The reference oscillator section provides a reference signal to the PLL section. The circuit design allows using either an external or internal oscillator.

When using an external oscillator, the internal oscillator is disabled by setting a logic low on the INT OSC line from the TR Shelf Interface Board. A high precision external oscillator may then be connected to the module through the external reference oscillator connector J4. EXT REF IN J4 has a 50 ohm input impedance and is coupled to the base of Q12. Buffer Q12 conditions the signal and applies it to the synthesizer U6 via coupling capacitor C10.

The internal reference oscillator, Y1, provides a 12.8 MHz signal with a stability of ±1 ppm. It is enabled by applying a logic high signal on the INT OSC line. This signal turns on Q2, allowing it to conduct and apply +5 volts to pin 1 of the oscillator Y1. The 12.8 MHz output signal (Y1 pin 2) is then sent to the synthesizer U6 via coupling capacitor C9.

The reference oscillator signal, either external or internal, is also routed to Q13 via coupling capacitor C54. The output taken from the emitter of Q13 is applied through C11 to the input of Buffer Amplifier U4. The buffered signal is coupled through C12 to a low pass filter network (C32, C33, C34, and C35) and a resistive pad (R27, R28, and R31) for isolation. The output from the resistive pad is then connected to J3, REF OUT, making the reference oscillator signal available for external use.

PRESCALER AND SYNTHESIZER IC

The integrated circuit U6 is the heart of the synthesizer. It contains the necessary frequency dividers and control circuitry to synthesize output frequencies by the technique of dual modulus prescaling. U6 also contains an analog sample and hold phase detector and a lock detector circuit.

Within the U6 are three programmable dividers which are serially loaded using the CLOCK, DATA, and ENABLE inputs (pins 11, 12, and 13 respectively). A serial data stream (DATA) on pin 12 is shifted into the internal shift registers by low to high transitions of the clock input (CLOCK) at pin 11. A logic high (ENABLE) on pin 13 then transfers the program information from the shift registers to the divider latches. The serial data determines the VCO frequency by setting the internal A, R, and N dividers.

The 12.8 MHz reference oscillator signal OSCIN is internally routed to the “R” divider. The “R” divider divides down the 12.8 MHz reference signal to a lower frequency, FR, as directed by the input data and divides the signal to the internal analog phase and lock detectors.

The “A” and “N” dividers process the loop feedback signal from the VCO (by way of the dual modulus prescaler U5). The output of the “N” divider, FN, is a divided down version of the VCO output frequency. This signal is also applied to the internal phase detector. The ramp and hold constants are determined by C26, R37, C31, and R36.

The analog phase detector output voltage (PD OUT) is proportional to the phase difference between FR and FN. This output serves as the loop error signal. When operating on the correct frequency, the inputs to the phase detector are identical and the output voltage of the analog phase detector is constant. If the compared frequencies (phases) differ, the analog phase detector increases or decreases the DC output voltage (PD_OUT). This error signal voltage tunes the VCO to whatever frequency is required to keep FR and FN locked (in phase).

The lock detector furnishes the Fault circuit in U13 with the lock detect (LD) signal. When FR and FN are in phase, the lock detector output sends a logic high on the LD line to the fault circuit U13. If the VCO is not locked onto the correct frequency, the resulting out-of-phase condition causes the output from the lock detector to be a logic low.

LOOP FILTER

The error signal, ANOUT, is applied to the loop filter at U8.2-5 and U8.1-3. U8.2 acts as a buffer amplifier with gain. The output signal from the amplifier is applied to a low pass filter consisting of R42, R43, C35 and C36 via the bivalent switch U14. The filter removes noise and sampling frequencies from the error voltage. The switch, U14, selects the proper filter configuration for operation in the narrow band, wide band or tuning mode. The control signals (OPEN_LOOP, ENABLE_NOT, and TUNE_CTRL) for U14 are derived from the digital control circuits U10, U12, and U13. U8.1 provides a buffered output for testing at the DIN connector on the rear of the module.

DIGITAL CONTROL

Logic control circuits (other than those inside the synthesizer IC - U6) consist of the following:

- Digital Control Circuit (U10, U12, & U13)
- Level Shifters
- Fault Circuit

The Digital Control Circuits U10, U12, & U13 serve as an interface between the controller and the synthesizer IC.

As an address decoder, U10 enables the input gates when the A0, A1, and A2 input lines (pins 4, 3, and 2) receive the correct address code from the controller. For the Receiver synthesizer enable the address is 010 on A0, A1, and A2 respectively. After receiving the proper logic code, the input gate U12 is enabled. This allows the ENABLE, CLOCK, and serial DATA information to pass on to the synthesizer via the level shifters.

The Level Shifters Q3, Q4, and Q5 convert the five (5) volt logic level to the eight (8) volt logic level required by the synthesizer.

The Fault circuit, U13, monitors the lock detect signal from the PLL synthesizer. Under normal (locked) condition, the PLL sends a logic high signal to U13. U13 processes the signal and providing a logic high output which saturates Q6. With Q6 saturated, the FAULT LED (CR1) turns off. U13 also sends a logic high signal, FLAG 2, (U13.3-8) to the controller indicating the VCO’s frequency is correct.

When the VCO is not on the correct frequency, the synthesizer sends a logic low signal to U13. This causes U13 to cutoff Q6 which turns on the FAULT LED. U13 also sends a logic low signal to the controller indicating the VCO’s frequency is incorrect.

VOLTAGE REGULATORS

Voltage regulators U15 and U16 reduce the +13.8 VF current and +8 Vdc current to +5 Vdc and +8 Vdc respectively. The output from U15 (CVSY) is used by both the synthesizer IC and logic circuitry while the 8 Vdc output from U16 is used for the op-amps, level shifters, and the discrete +8 VOSC regulator circuit.

The discrete +8 V OSC regulator circuit is a linear regulator consisting of U9A, Q7, Q8, and associated circuitry. The error amplifier U9A controls Q7 and pass element Q8. The +8 V OSC is used as the power source for the VCO circuit, where additional filtering is provided to keep noise to a minimum.

MAINTENANCE

RECOMMENDED TEST EQUIPMENT

The following test equipment is required to test the Synthesizer Module:

1. Modulation Analyzer; HP 8901A, or equivalent
2. Power Supply; 12.0 Vdc @ 500 mA
3. Frequency Counter; 10 MHz - 250 MHz
4. Power Meter; -20 dBm to +10 dBm
5. Spectrum Analyzer; 0 - 1 GHz

TEST AND ALIGNMENT

Initialization

Apply +12 Vdc to the test fixture.

Current consumption

Measure the current through pins 15A, 15B, 15C, 16A, 16B, and 16C.

Verify the current is less than 250 mA. Total current is the +13.8 VF current and +12 Vdc current combined.

Reference Oscillator

Adjust Y1 for an output frequency of 12.8 MHz ±5 Hz. Measure the output power of the reference oscillator output (J3).

Oscillator Alignment

Ground the ENABLE TEST line (pin 22A). Apply +5 Vdc to the W, TUNE line (pin 26A). Measure the frequency of the free running oscillator at the LO OUT port (J2).
Adjust the trimmer capacitor C52 to the correct frequency:

- Group 1 - 170 MHz ± 100 kHz.
- Group 2 - 150 MHz ± 100 kHz.

**Synthesizer Loading**

Unground the ENABLE TEST line (pin 22A). Load the synthesizer IC Group 1 - 170 MHz.

Group 2 - 150 MHz.

Verify the lock indicator (CR1) is off or the FLAG 2 line is high.

**Hum and Noise**

Initialize the HP 8901A for 300 Hz - 3 kHz, 750 us deemphasis, average FM deviation, and 0.44 dB reference for the deviation.

Verify the hum and noise (J2) is less than -55 dB.

**Output Power and Harmonic Content**

Verify the output power (J2) at the fundamental frequency is:

0 dBm ± 0.0 dB

Verify the harmonic content is less than -30 dBc.

---

**SERVICE NOTES**

The following service information applies when aligning, testing, or troubleshooting the RX Synthesizer:

- Logic Levels:
  - Logic 1 = high = 4.5 to 5.5 Vdc
  - Logic 0 = Low = 0 to 0.5 Vdc
- Receiver Synthesizer Address = A0 A1 A2 = 010
- Synthesizer data input stream is as follows:
  - 14-bit "R" divider most significant bit (MSB) = R13 through "R" divider least significant bit (LSB) = R0
  - 10-bit "N" divider MSB = N9 through "N" divider LSB = N0
  - 7-bit "A" divider MSB = A6 through "A" divider LSB = A0
- Single high Control bit (last bit) Latched When Control Bit = 1

**DATA ENTRY FORMAT**

- Synthesizer lock is indicated by the extinguishing of the front panel LED indicator and a logic high on the fault FLAG 2 line (J1 pin 12C).
- Always verify synthesizer lock after each new data loading.

---

**TROUBLESHOOTING CHART**

<table>
<thead>
<tr>
<th>SYMPTOM</th>
<th>AREAS TO CHECK</th>
<th>INDICATIONS</th>
</tr>
</thead>
</table>
| I. Loop Fails To Lock | 1. Check for:
+8 Vdc at U16-3,
+5 Vdc at U15-3,
+8 Vdc at Q6-C. |
|                     | 2. Check for 12.8 MHz reference at U6-2, and U6-3.
Typical Levels:
500 mVpp @ U6-2
2.5 Vpp @ U6-3 |
|                     | 3. Check for LO output @ J2.
FLO ≥ 5 MHz, 0dBm nominal. |
|                     | 4. Check Prescaler output @ U5-4. Typically: 2.4 MHz square wave @ 1.25 Vpp. |
|                     | If LO power is good, Check for 3.2 Vdc @ U2-3. Replace U2, then U5 if necessary. |
| II. Reference OSC. not present or low power. | 5. Check for CLOCK, DATA, and ENABLE signals are reaching U6 pins 11,12, and 13 respectively. (0, 8V logic levels) |
|                     | 6. Check Ramp Signal @ U6-15. It should be 5 kHz nominal. |
|                     | Bad digital control circuitry. Troubleshoot using standard procedures. Ensure all programming signals are present at J1. (CLOCK,DATA,ENABLE,A0,A1 and A2) |
|                     | If reference oscillator and programming signals are present for proper programming information. Last resort - replace Synthesizer IC U6. |
|                     | Bad supply switch Q2 or wrong Control Signal Internal Osc. Troubleshoot using standard procedures. Replace Y1 as last resort |
|                     | Bad buffer amplifier Q13. Troubleshoot using standard procedures. |

Continued
### Troubleshooting Chart (Continued)

<table>
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<th>SYMPTOM</th>
<th>AREAS TO CHECK</th>
<th>INDICATIONS</th>
</tr>
</thead>
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<tr>
<td>III. LO power low or tuned out of band.</td>
<td>1. Check tuning with 6 Vdc applied using test procedure. (f_2 \pm 5) MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2. Check DC bias at Buffer Amplifiers U1, U2, &amp; U3 pin 3 Typ. 3.2 Vdc.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>LO tuning incorrect. Retune following test procedure.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2. Check DC bias at Buffer Amplifiers U1, U2, &amp; U3 pin 3 Typ. 3.2 Vdc.</td>
<td></td>
</tr>
<tr>
<td>IV. LO signal not present. (i.e. Q1 does not oscillate)</td>
<td>1. Check DC bias at Q1 drain. (Typ. +8 Vdc)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2. Check DC bias at Q1 source. (Typ. +0.9 Vdc)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Replace Q1.</td>
<td></td>
</tr>
</tbody>
</table>

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**Receiver Synthesizer Module**  
19D902781G1 & G2  
(Checklist 06, Rev. 1)
<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PART NO.</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>C24</td>
<td>1A70225P32</td>
<td>Ceramic: 16 pf ±5%, 50 VDCW, temp coef ±30 ppm/°C</td>
</tr>
<tr>
<td>C25</td>
<td>1A70225P33</td>
<td>Ceramic: 10 pf ±5%, 50 VDCW, temp coef ±30 ppm/°C</td>
</tr>
<tr>
<td>C26</td>
<td>1A70225P34</td>
<td>Ceramic: 1 ti ±1%, 50 VDCW, temp coef ±30 ppm/°C</td>
</tr>
<tr>
<td>C27</td>
<td>1A70225P35</td>
<td>Ceramic: 100 pf ±5%, 50 VDCW, temp coef ±30 ppm/°C</td>
</tr>
<tr>
<td>C28</td>
<td>1A70225P36</td>
<td>Ceramic: 10 fF ±5%, 50 VDCW, temp coef ±0 ppm/°C</td>
</tr>
</tbody>
</table>

**INDUCTORS**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PART NO.</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>19A703P01</td>
<td>Coil, 1 mH ±20%, (Used in G2).</td>
</tr>
<tr>
<td>L2</td>
<td>19A704P02</td>
<td>Coil, 0.1 mH ±30%. (Used in G1).</td>
</tr>
<tr>
<td>L3</td>
<td>19A705P03</td>
<td>Coil, 10 mH ±30%. (Used in G1).</td>
</tr>
<tr>
<td>L4</td>
<td>19A706P04</td>
<td>Coil, 100 mH ±30%. (Used in G1).</td>
</tr>
</tbody>
</table>

**DIODES**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PART NO.</th>
<th>DESCRIPTION</th>
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<tbody>
<tr>
<td>Q1</td>
<td>19A707P01</td>
<td>Silicon, NPN: sim to 2N3904, low profile.</td>
</tr>
<tr>
<td>Q2</td>
<td>19A708P02</td>
<td>Silicon, NPN: sim to 2N3904, low profile.</td>
</tr>
<tr>
<td>Q3</td>
<td>19A709P03</td>
<td>Silicon, NPN: sim to 2N3904, low profile.</td>
</tr>
</tbody>
</table>

**RESISTORS**

<table>
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<tr>
<th>SYMBOL</th>
<th>PART NO.</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>19B800P01</td>
<td>Metal film: 0.05 ohm ±5%, 1/8 w.</td>
</tr>
<tr>
<td>R2</td>
<td>19B800P02</td>
<td>Metal film: 0.05 ohm ±5%, 1/8 w.</td>
</tr>
<tr>
<td>R3</td>
<td>19B800P03</td>
<td>Metal film: 0.05 ohm ±5%, 1/8 w.</td>
</tr>
<tr>
<td>R4</td>
<td>19B800P04</td>
<td>Metal film: 0.05 ohm ±5%, 1/8 w.</td>
</tr>
</tbody>
</table>

**CAPACITORS**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PART NO.</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>1A70225P08</td>
<td>Ceramic: 12 pf ±5%, 50 VDCW, temp coef ±30 ppm/°C (Used in G2).</td>
</tr>
<tr>
<td>C2</td>
<td>1A70225P09</td>
<td>Ceramic: 22 pf ±5%, 50 VDCW, temp coef ±30 ppm/°C (Used in G1).</td>
</tr>
<tr>
<td>C3</td>
<td>1A70225P10</td>
<td>Ceramic: 22 pf ±5%, 50 VDCW, temp coef ±30 ppm/°C. (Used in G1).</td>
</tr>
<tr>
<td>C4</td>
<td>1A70225P11</td>
<td>Ceramic: 10 pf ±5%, 50 VDCW, temp coef ±30 ppm/°C. (Used in G1).</td>
</tr>
<tr>
<td>C5</td>
<td>1A70225P12</td>
<td>Ceramic: 10 pf ±5%, 50 VDCW, temp coef ±30 ppm/°C. (Used in G1).</td>
</tr>
<tr>
<td>C6</td>
<td>1A70225P13</td>
<td>Ceramic: 10 pf ±5%, 50 VDCW, temp coef ±30 ppm/°C. (Used in G1).</td>
</tr>
<tr>
<td>C7</td>
<td>1A70225P14</td>
<td>Ceramic: 10 pf ±5%, 50 VDCW, temp coef ±30 ppm/°C. (Used in G1).</td>
</tr>
<tr>
<td>C8</td>
<td>1A70225P15</td>
<td>Ceramic: 10 pf ±5%, 50 VDCW, temp coef ±30 ppm/°C. (Used in G1).</td>
</tr>
</tbody>
</table>

**MISCELLANEOUS**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PART NO.</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>19B801P01</td>
<td>Connector, DVI: 26 pin contacts, right angle mounting: sim to AMP 585088-1.</td>
</tr>
<tr>
<td>J2</td>
<td>1A1150P02</td>
<td>Connector, receptacle.</td>
</tr>
</tbody>
</table>

*COMPONENTS, ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES*
### IC Data

#### Symbol | Part No. | Description
--- | --- | ---
R70 thru R72 | 19B80007P102 | Metal film: 1K ohms ±5%, 1/8 w. through R76
R73 thru R76 | 19B80007P103 | Metal film: 10K ohms ±5%, 1/8 w.
R77 and R78 | 19B80007P101 | Metal film: 100 ohms ±5%, 1/8 w.
R79 thru R88 | 19B80007P102 | Metal film: 1K ohms ±5%, 1/8 w. through R88

---

### Production Changes

Changes in the equipment to improve or simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by these revisions.

**REV. A - RECEIVER SYNTHESIZER BOARD 19D902664G1 & G2**

- To improve regulator operation at low supply voltage. Changed resistor R10. Resistor R10 was 10 ohms (19B80007P100).

**REV. B - RECEIVER SYNTHESIZER BOARD 19D902664G1 & G2**

- To accommodate SOG synthesizer IC package U6 (PLCC package discontinued) and make provision for RC compensation network (R89, C82) in 10-Volt regulator circuit. Resistor R89 and capacitor C82 are not installed. Modified printed circuit board layout. Pinout wire board changed from 19D800007P100 to 19D902665P100 (74HC04). Changed U6. Synthesizer U6 was 19B80007P102.

**REV. A - RECEIVER SYNTHESIZER MODULE 19D902781G1 & G2**

- To install RF shielding grommets. Installed 9 RF shielding grommets (19B805470P1) on three BNC connectors of input/output RF ports.

**REV. C - RECEIVER SYNTHESIZER BOARD 19D902664G1 & G2**

- To add filtering in the output circuit of the pre-scaler buffer amplifier. Changed resistor C16. Capacitor C16 was 19A802052P3 (470 pF). Added capacitor C102 and inductor L18. Changed resistor R24. Resistor R24 was 19B800007P100 (10 Ohms).

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#### Circuit Diagrams

![Circuit Diagram](image_url)

**U5**

19B10944P201

Modulator Preselector

- **FUNCTION TABLE**
- **PIN ASSIGNMENT**
- **TOP VIEW**

**U6**

19B800902P7

Synthesizer

- **INPUT**
- **OUTPUT**
- **CONTROL**

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**U1 thru U4**

19A706592P7

Silicon Bipolar IC

**PIN 1. RF INPUT**

**2. GROUND**

**3. RF OUTPUT AND BIAS**

**4. GROUND**

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**U1 thru U4**

19A706592P7

Silicon Bipolar IC
U8 & U9
19A702293P2
Dual Operational Amplifier

U10
19A703471P120
Decoder/Demux

U12 & U13
19A70483P302
Logic Gate/Inverter

U14
19A702765P4
Quad Analog Switch

U15
19A704971P8
+5 Regulator

U16
19A70497P10
+8V Regulator

Y1
19B801351P12
Crystal Oscillator