MAINTENANCE MANUAL MULTISITE COORDINATOR II CONTROLLER BOARD 19D903299P1

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SPECIFICATIONS

TEMPERATURE	- 30°C to + 60°C
DIMENSIONS (Height X Width)	200 mm X 330 mm (typical)
WEIGHT	1.0 kG (typical)
POWER	+ 5.0 Volts ± 10% 1.75 Amperes (maximum) 3.0 Amperes Fuse + 15 Volts ± 10% 0.3 Amperes (maximum) 0.5 Amperes Fuse - 15 Volts ± 10% 0.3 Amperes (maximum) 0.5 Amperes Fuse
DIGITAL LEVELS:	TTL/CMOS/HCMOS RS-232C RS-422 FUTUREBUS OPTOCOUPLER
DIGITAL DATA RATE	9600/19200 BAUD 720 kBAUD 1.8 MEGA BAUD

DESCRIPTION

Ericsson GE's Controller Board 19D903299P1 is the basic processing unit used in the Multisite Coordinator II trunking system. The Controller Board is a dual processing unit which provides interfacing and control functions for the various modules in the system. This is accomplished by sending command signals directly to the audio board(s) over two interfaces. The first interface is a HSCX-based HDLC port and the second is a PPI-based audio control port. Both of these ports are coupled directly to the interface microprocessor on each Controller Board.

A single Controller Board supports eight (8) audio boards. Each audio board carries four audio/data channels. This gives the Controller Board control of thirty two (32) audio /data channels.

The Controller Board has two principal processing units (refer to Figure 1). The first is an interface microprocessor that is responsible for most of the logical processing functions of the node. The other microprocessor is a communications controller that routes command messages between the interface microprocessor, the internal message bus and the external serial link to the RF site, dispatcher, console or other RF unit. The Controller Board also has a dual-port RAM memory which conveys messages and other communications between the interface microprocessor and the communications controller.

The communications controller is principally a message router. Once a valid message is received, the communications controller loads the message into the dual-port RAM and signals the interface microprocessor that a message is waiting. The interface microprocessor then retrieves the message and processes it accordingly. Similarly, the interface microprocessor generates messages for transmission to the site or dispatcher, or for broadcast on the internal message bus. The interface microprocessor loads the message in the dual-port RAM and notifies the communications controller that a message is waiting. The communications controller retrieves the message and routes it to the internal message bus or external serial port. This depends on the address of the message within the dual-port RAM. The dual-port RAM is segregated into memory

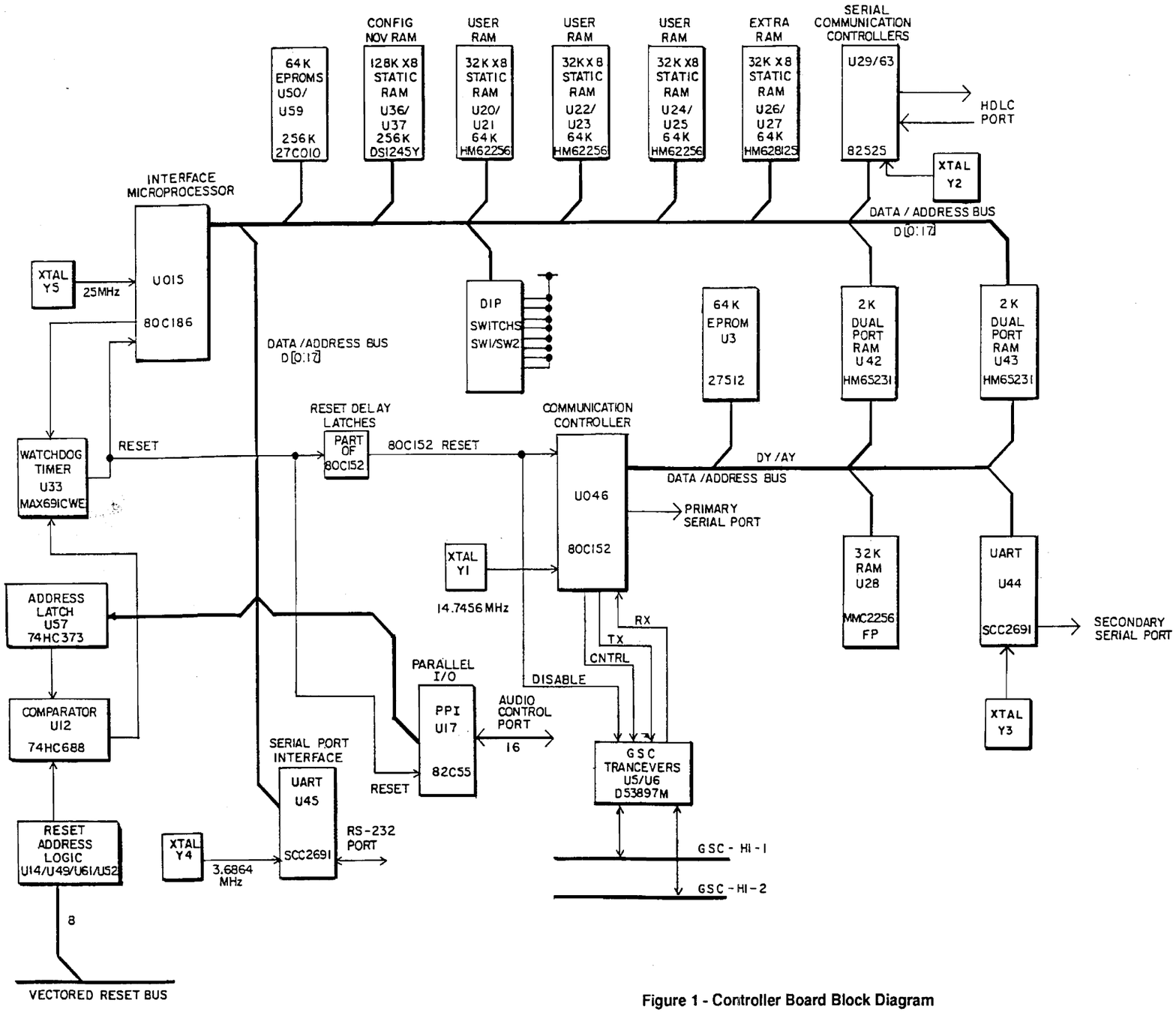


Figure 1 - Controller Board Block Diagram

buffer packets. Each packet is allocated for messages either to or from the internal message bus, the external serial port and the interface microprocessor.

The Controller Board enables a single interface microprocessor to handle the processing requirements for a given node in the distributed multisite coordinator. The architecture of the Controller Board insulates the interface microprocessor so that it is reserved for message processing and is not required to perform message routing functions. Message routing functions are performed by the communications controller.

CIRCUIT ANALYSIS

VOLTAGE REGULATION

External voltage input levels to the Controller Board are +5 Vdc, +15 Vdc and -15 Vdc. These levels are regulated to produce +5 Vdc, +12 Vdc and -12 Vdc respectively. Refer to the Schematic Diagram, Sheet 2.

+5 Vdc (Vcc) Filtering

The external +5 Vdc connects to the Vcc filtering circuit from **+5EXT** through 3 amp fuse F1. Filtering is provided 100 µF capacitor C75. LED9 illuminates when Vcc is present.

The filtered Vcc output is taken from the point labeled Vcc on the Schematic Diagram. The Vcc can be read, using a voltmeter, between **TP3** (Vcc) and **TP4** (GND).

+12 Vdc Regulation

The external +15 Vdc connects to the +12 Vdc regulation circuits from **+15EXT** through 0.5 amp fuse F3. Filtering, ahead of linear voltage regulator U2 (78M12), is provided by 0.1 µF capacitor C4 and 100 µF capacitor C76. Additional filtering, after U2, is provided by 0.1 µF capacitor C3 and 100 µF capacitor C74. Leaded diode D1 removes any negative transients. LED6 illuminates when +12 Vdc is present.

The regulated +12 Vdc is taken at the point labeled **+12V** on the Schematic Diagram. The +12 Vdc can be read, using a voltmeter between **TP2** (+12 Vdc) and **TP4** (GND).

-12 Vdc Regulation

The external -15 Vdc connects to the -12 Vdc regulation circuits from **-15EXT** through 0.5 amp fuse F2. Filtering, ahead of linear voltage regulator U1 (79M12), is provided by 0.1 µF capacitor C5 and 100 µF capacitor C77. Additional filtering, after U1, is provided by 0.1 µF capacitor C6 and 100 µF capacitor C73. Leaded Diode D2 provides protection from positive transients. LED5 illuminates when -12 Vdc is present.

The regulated -12 Vdc is taken at the point labeled **-12V** on the Schematic Diagram. The -12 Vdc can be read, using a voltmeter between **TP1** (-12 Vdc) and **TP4** (GND).

DECOUPLING

Decoupling on the Controller Board is provided by 0.01 µF capacitors (C13 through C96) connected between all voltage inputs of integrated circuits (U3 through U63) and ground (GND). Refer to the Schematic Diagram, Sheet 2.

PROCESSING DEVICES

Interface microprocessor U15 (80C186) and a communications controller U46 (80C152) are the main processing devices on the Controller Board. There are two dual-port RAM's U42 and U43 (HM65231) through which the microprocessor and controller communicate with each other. The dual-port RAM's each have 2k bytes of memory and each RAM performs different functions. One of the dual-port RAM's holds the bus/slot bit map that indicates the status of each audio slot in every audio bus in the coordinator. In addition, this RAM is also used as a scratch pad memory by the interface processor and/or communications controller. The other dual-port RAM is used to transfer messages between the interface processor and communications controller. This RAM is described in more detail later in the text.

Communications Controller (80C152)

The communications controller (U46) is coupled to the dual-port RAM's by a data and address bus (DY[0:7] and AY[1:15]) This bus also connects the controller to non-volatile EPROM U3 (27C512), volatile USER RAM U28 (HM62256FP) and UART standard serial port interface U45 (SCC2691AC1A28). The EPROM contains 64k bytes of memory and holds the programs executed by the communications controller.

The UART is a full-duplex asynchronous receiver/transmitter. The transmitter accepts parallel data from the microprocessor and converts it to a serial bit stream on the (TxD) output pin, Pin 4. The receiver accepts serial data on the (RxD) pin (Pin 3), converts the serial data input to a parallel format to send to the microprocessor.

The primary serial port is embedded within the communications controller and is a standard RS-232 port as is the UART. These serial ports couple the communications controller to the RF site controller, dispatcher console or other unit to which a particular node is assigned. Land lines connect these units to the multisite coordinator. RF, Microwave, optical or other means may also be used to transmit signals to the coordinator.

The Controller Board makes use of the U46 GSC port. This is a high speed serial input. It is connected in a half duplex two line setup and can be attached to one of two physical sets of lines. BTL drivers plus AND gates select between the two lines.

Communications controller U46 connects to multisite message bus **GSC_HI_1** and backup message bus **GSC_HI_2** through GSC transceiver U5 (DS3897M). There are separate receive, transmit and control lines between the communications controller and the GSC transceiver. Both GSC bus drivers are enabled all the time. Data is transmitted on both busses simultaneously. The communications controller selects from which bus it will receive. Upon receiving a transmit control signal, the transceiver accepts the message from the communications controller and places the message on the message bus.

U46 is also in charge of eight input and eight output optocoupler lines. The optocouplers U38, U39, U40 and U41 are IL066-004 quad devices. The inputs are fed into Port 6. The outputs are brought into Port 5. Optocoupler U038B input is capable of interrupting U15.

The controller (U46) can read the state of the PRIMARY line. It also directly controls two LED's, LED2 **ERROR** and LED3 **RUN.**

Interface Microprocessor (80C186)

Interface microprocessor U15 processes messages for the node. Messages are received from communications controller U46 through a dual-port RAM. The interface microprocessor is continuously polling for a pending message in the dual-port RAM sent by U46. The operation of the interface microprocessor acts almost exclusively in response to messages.

The interface microprocessor is supported by several other components on the Controller Board. Address/data bus D[0:17] allows the microprocessor to communicate with these other components to perform logical tasks. The interface microprocessor has available two battery-backed up 128k X 8 static RAM's U36/U37 (DS1245Y), **CONFIG NOVRAM**, providing 256k of non-volatile storage. This storage is controlled by the LCS chip select enable lines. **MEMORY DECODER** U19 (AMPAL22V10AJC) is used to control allocation of microprocessor memory space required by other components.

A 192k block of volatile static **USER RAM** is provided by three segments of two 32k X 8 static RAM's U20 through U25 (HM62256FP). Each segment is 16 bits wide (8 bits/RAM) giving 64k per segment. This block of memory is enabled by the MCS select lines.

A segment of **EXTRA RAM** is provided by two 128k X 8 RAM's U31/U32 (HM62812S). This memory is enabled by the **CS_XRAM** line. This provides a total of 256k of volatile static RAM.

The microprocessor UCS select line enables the program memory. The program memory is stored in two 128 X 8 EPROM's U58/U59 (27C010) These EPROM's provide 256k of PROM space. This space is arranged as a 16 bit wide area. The EPROM's are not selected directly by the UCS select line. The microprocessor decode goes through U19 before going to the EPROM's.

The interface microprocessor also couples through the Address/Data bus to DIP switches SW1 and SW2. These switches determine the personality of the board, e.g., MIM or CIM and are set manually with installation of the board.

The interface microprocessor is responsible for maintaining the audio processing database for the audio boards in the specified node. There are eight (8) audio boards in a node and each board carries four audio channels. The interface microprocessor communicates directly to the audio boards through the HSCX-based HDLC port and PPI-based audio control port U17 (82C55). The parallel port (U17) sends nearly all of the signal commands between the interface microprocessor

and the audio boards. The audio control bus is a sixteen (16) bit bus (AC[0:15]) originating at ports A and B of U17.

The HDLC port is used primarily for fault detection and for sending messages from the audio boards microprocessors to the interface microprocessor.

Peripheral Circuitry

The Controller Board has peripheral circuitry to maintain the interface microprocessor and the communications controller. The peripheral circuits are enabled from the microprocessor's seven peripheral select lines (PCS0 through PCS6).

Clocks:

There is a 25 MHz clock (Y5) for the interface microprocessor and a 14.7456 MHz clock (Y1) for the communications controller provide timing for the two microprocessors.

Watch-Dog Timer:

The operation of the interface microprocessor is monitored by watch-dog timer U33 (MAX691CWE). This timer must be regularly reset by the microprocessor or the timer will reset the microprocessor and communications controller. The microprocessor U15 is reset directly by the watch dog. Reset Out of U15 is buffered by U62B and supplied to a reset extend/delay circuit (U53A, U4A) which resets the communications controller (U46). In addition, the watch-dog timer indirectly disables the GSC transceivers U5/U6 when it resets the controller. This is to prevent transmission or reception of messages during the reset operation. The reset must hit within one and a half second intervals to keep the watch-dog from timing out. The select line PCS0 is used to trigger a one-shot. The one shot is set long enough that one pulse resets the watch-dog. The WDOG_TRIG output of U15, Pin 25 connects to the input of OR gate U62D (74HC32D). The output of U62D triggers multivibrator U4B (74HC123A). The output of U4B (!PWDOG_TRIG) connects to the input of AND gate U14A (74HC08D). The output of U14A drives transistor Q3 to reset the watch-dog. Transistor Q2, also driven by U14A, illuminates LED4 each time the watch-dog reset occurs.

UART:

The interface microprocessor has a serial RS-232 serial port through UART U45 (SCC2691). The UART is enabled by the second select line, PCS1. This device has an on board baud rate generator and an eight bit register I/O space. The UART appears as an eight bit device. The serial lines are tied to RS-423 drivers. These lines are available on the back connectors of the board and on the front connector P1A. Each port also has as RS-232 drive going to P2A. This connector makes the board easy to hook up to a protocol analyzer and is used for diagnostic purposes. The interface processor is accessed directly by using this serial port to bypass the communications controller. This serial link allows an operator using a supervisory or diagnostic unit to interact directly with the interface microprocessor.

Parallel I/O:

Select line PCS2 enables parallel I/O U17 (82C55A). The parallel I/O has three eight bit bi-directional ports (A,B and C). **NOTE:** the ports are on even addresses. The 82C55A is an eight bit device. Ports A (PA[0:7]) and B (PB[0:7]) provide 16 bits of I/O for control of audio boards. These lines are buffered by drivers U7/U8/U9 (74HC245ADW). Port A is also used to send eight bit device addresses. The buffered output of U9 is converted to BTL levels by interface U18 (DS3896). Port C (PC[0:7]) provides several bit controls. These include the direction controls for the buffer circuit of ports A and B. Four bits, sent to BTL driver U6, provide external control lines. They are the **A/B MOM, A_LATCH,** External Reset and External Primary/Secondary select lines. One line (PC6) is not used. The final line (PC7) gives U15 control of LED8.

Disable Circuitry:

The Controller Board provides complex disable circuitry. A large part of this circuitry includes 8-bit logical device address compare circuit U12 (74HC688). One side of U12 is fed by the device address coming through the BTL driver from the backplane connectors. The other side is fed from latch U57 (74HC373). This latch is set by select line PCS3. The disable circuitry is enabled when the device address in U57 and the device address coming from the connector agree. This brings the equal output of comparator U12 low which is then

inverted through inverter U49F (74HC04) so it can be ANDed through AND gate U14B (74HC08D). The gates U51 and U61 provide an exclusive OR function between the card A/B switch and the external A/B signal coming from the connector. If they are the same, U61C will be high which enables the matching address line to get through gate U14B. This signal then gets ANDed again with the externally supplied Add Latch signal. It can then be used to clock flip-flop U52B to provide primary or secondary service selection. When not primary, the controller can listen but cannot talk. The primary line is used to disable buffers U7 and U8. It also disables transmit RS-423 line driver U68 (DS3487) through AND gate U14C (74HC08D).

Microprocessor U15 latches the known address at U57. When the device address coming in PROM U18 equals the address at U57, then: the card can be put in secondary by **PRI_EXT,** put in permanent reset by **RES_EXT.** The device address and control lines originate from the controller w/ MOM Bit Set.

There is another, stronger form of disable. This is a latched reset mode caused by the device address matching and the external **RES EXR** signal being clocked on the inputs to AND gate U13B (74HC08D). This toggles flip-flop U52B to latch transistor Q1 to hold reset. All I/O is basically disabled in this mode.

Configuration Switches:

Microprocessor U15 also reads configuration switches SW1 and SW2. They are arranged as a sixteen bit word on the microprocessor PCS4 select line. **NOTE:** Three of the switches, the Watchdog Disable, MOM and A/B switches directly affect hardware.

HDLC Serial Communication Controllers:

There are two serial communication controllers (U29/U63 (82525)) controlled by U15. These controllers can operate in one of many complex HDLC modes. They have on board baud rate generators, or they can be clocked externally. They can handle a network of HSCX components with a minimum of microprocessor intervention. One controller is on the lower data bus, the other is on the upper data bus. Each controller has two channels. One channel is selected by the microprocessor PCS5 line. The other is selected by the PCS6 select line. The two microprocessor select lines are ORed in U19 as a single select to the HSCX controllers. Two select lines are needed because forcing the registers to even addresses causes each channel to occupy the 128 byte limit of a select.

The controller on the lower bus handles HDLC communications. One side has a full duplex four wire RS-423 interface. The other side is arranged in a single wire half duplex configuration. The controller on the upper bus is arranged with both channels on a Time Division Multiplexed **(TDM)** line. This line gets the master clock and frame synchronization clocks from the clock board through the board connector. This allows the audio bus to be **"piped"** to the outside world.

LAYOUT OF DUAL-PORT RAM

Figure 2 shows the layout of the dual-port RAM used for transferring messages between the interface microprocessor and communications controller. The dual-port RAM acts as a message box for the interface microprocessor and communications controller. Messages flowing between the microprocessor and controller are posted in the dual-port RAM until the recipient has an opportunity to receive the message.

The message memory location in this dual-port RAM are arranged into buffer segments to identify the source of the message. The dual-port RAM memory consists of six buffer segments of which three segments are allocated to the communications controller and the other three segments are allocated to the interface microprocessor. Each buffer packet is capable of holding eight (8) 32-byte messages.

With respect to the memory buffer segments allocated to the communications microprocessor, one packet holds messages from the external serial port, a second packet holds messages from the GSC message bus and a third packet holds messages generated by the communications controller for the interface microprocessor. The communications controller loads messages into the appropriate buffer packet in the dual-port memory depending on the source of the message.

Similarly, when the interface microprocessor generates a message, it places the message in one of the three buffer segments in the dual-port RAM. The segment allocated to the pending message depends on the destination of the message (GSC, serial port or communication controller). The interface microprocessor places messages to be sent to the serial port in the "for **serial port**" segment, messages to be broadcast on the message bus in the **"for GSC message bus"** segment and messages for the communications controller in the **"for communications controller"** segment. The communications controller knows where to route the message by its location in the dual-port RAM.

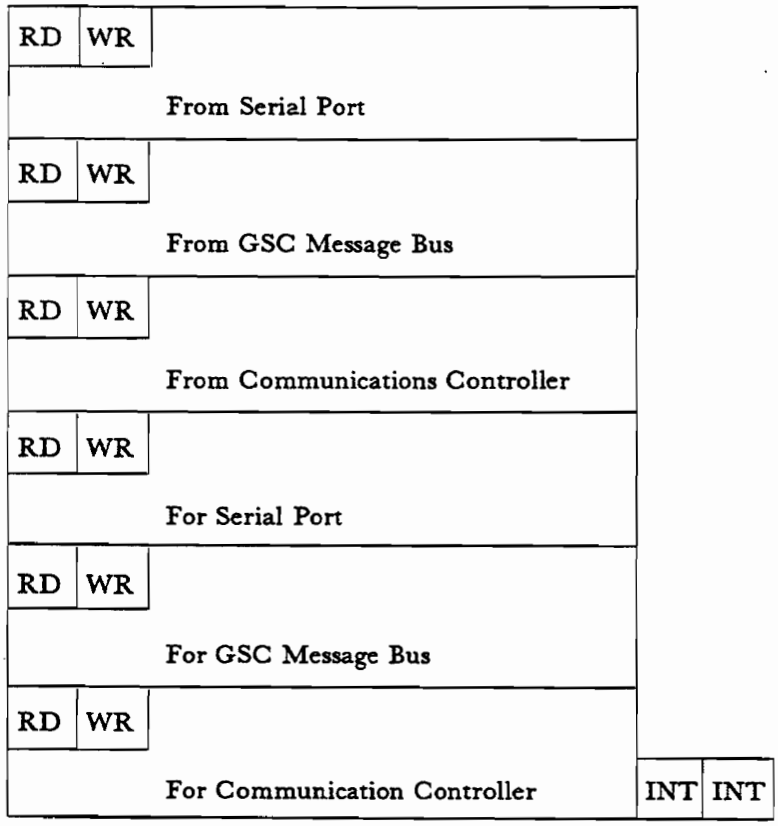
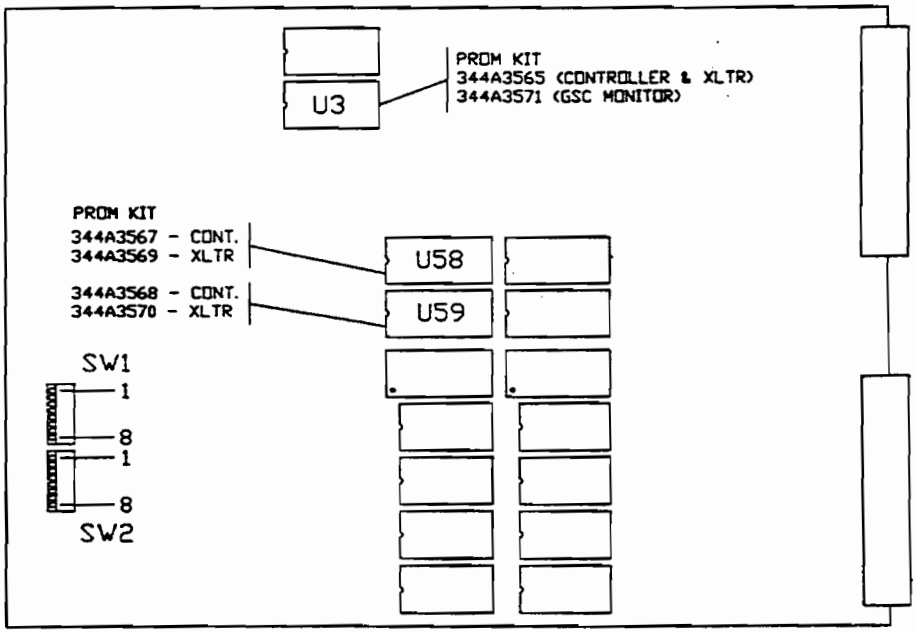


Figure 2 - Dual-Port Message Locations

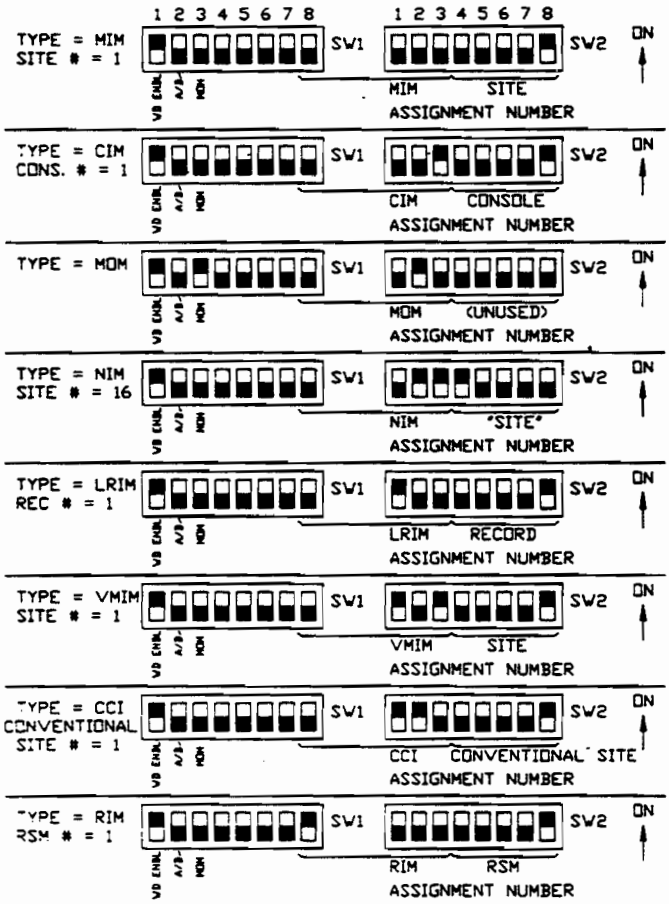
LED IDENTIFICATION

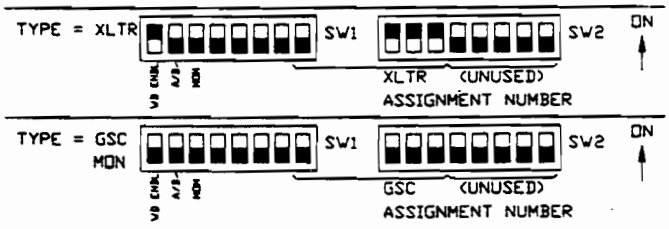
LED1	RESET
LED2	ERROR
LED3	RUN
LED4	Watchdog
LED5	- 12 V
LED6	+ 12 V
LED7	Y_Rxd0_232 Mon
LED8	Y_Txd0_232_Mon
LED9	+ 5 V
LED10	Y_Txd1_232_Mon
LED11	Y_Rxd1_232_Mon
LED12	X_Txd0_232
LED14	X_Rxd0_232

CONTROLLER BOARD



MSC II CONTROLLER BOARD SWITCH SETTINGS





SWITCH SETTINGS

(19D903515, Sh. 3, Rev. 2)

QUICK REFERENCE TO TROUBLESHOOTING

SYMPTOMS	ACTION
One or more power LED's not lit	Check fuses F1 through F3
Watch Dog Timer resetting (LED4 flashing every 1-1/2 second)	Check for bent pin(s) on EPROM's U58 and U59
Sanity LED (LED3) not flashing	U46 (80C152) microprocessor is not running; check for bent pin(s) on EPROM U3
Secondary LED (LED12) lit	Check device number and personality dip switch settings. Another control card with the same settings is likely.
Node ID does not show on Monitor Module (MOM) configuration screen	1. Check for conditions described above 2. Check for correct dip switch settings 3. Check GSC RX and TX data. If no RX or TX data consult Engineering
No data to console or site	1. Check all conditions described above 2. Check data cable connection to MSC II I/O panel
Will not initialize an audio card	1. Check first five conditions above 2. Check correct placement of PI/O jumper cables on backplane 3. Check PI/O headers on backplane for bent pins
	CONTROLLER BOARD TEST POINTS Vcc TP3 + 12V TP2 - 12V TP1 **GSC DATA** TRANSMIT (TX) TP12 RECEIVE (RX) TP11 **RESET** /REST P10

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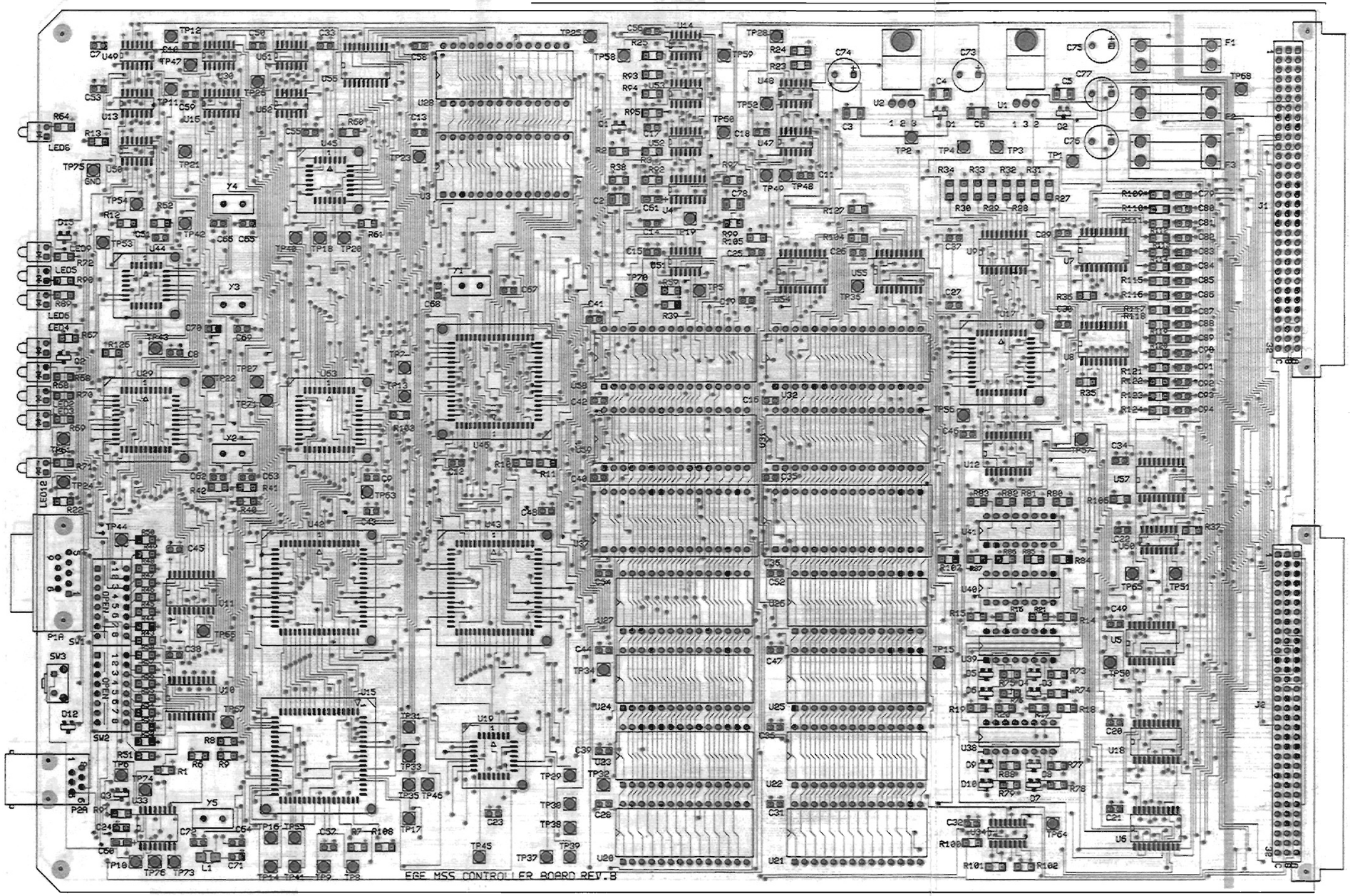
CAUTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES

COMPONENT SIDE

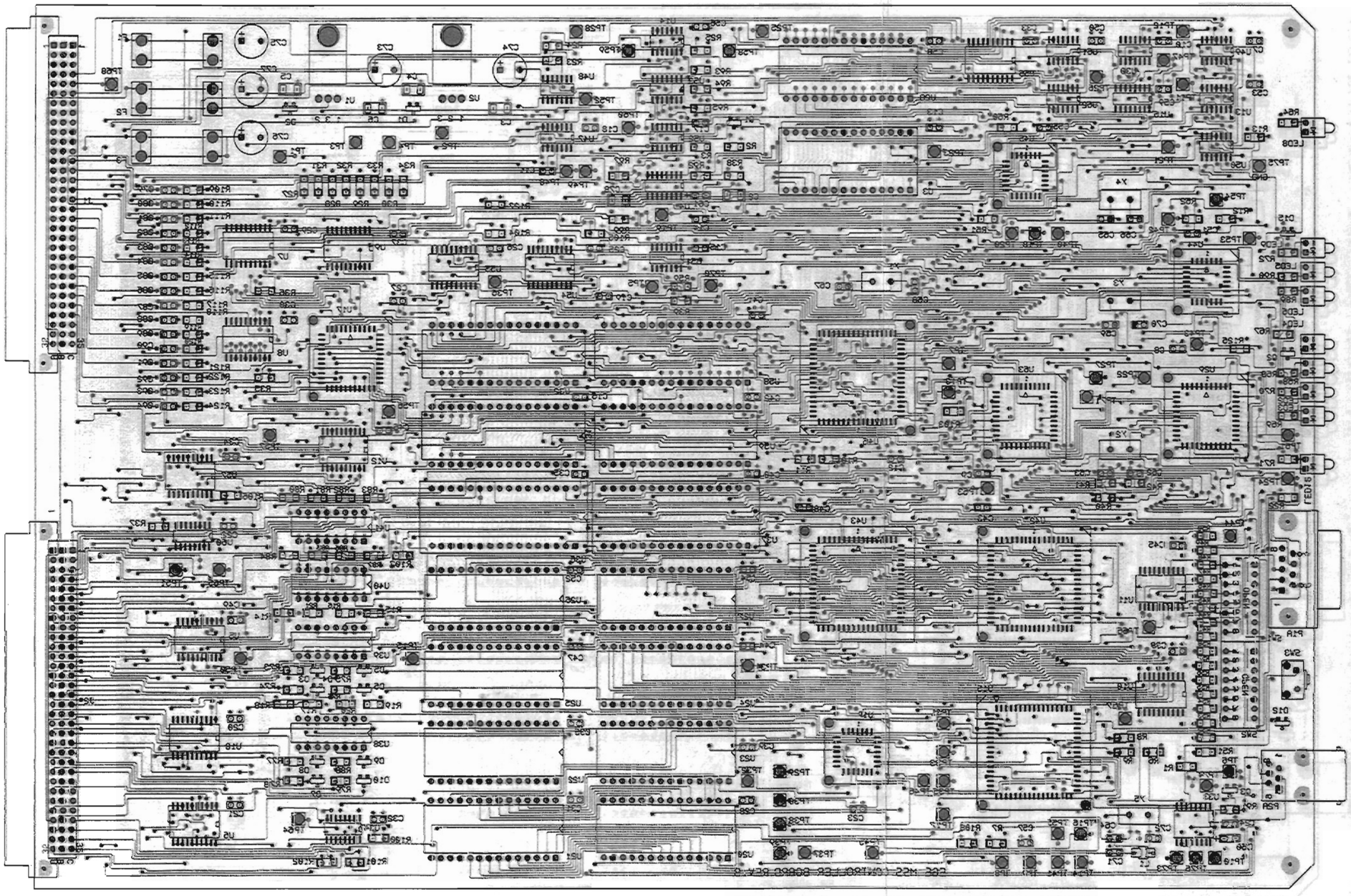


RUNS ON INTERNAL PATTERN
RUNS ON BOTH SIDES
RUNS ON EXTERNAL PATTERN

(19D903229, Rev. B)
(TDI-T91084, Component Side, Layer 1, Rev. 0)
(TDI-T91084, Component Side, Layer 2, Rev. 0)

CONTROLLER BOARD
19D903299P1

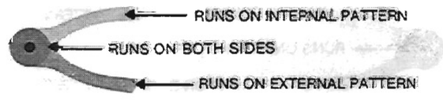
SOLDER SIDE

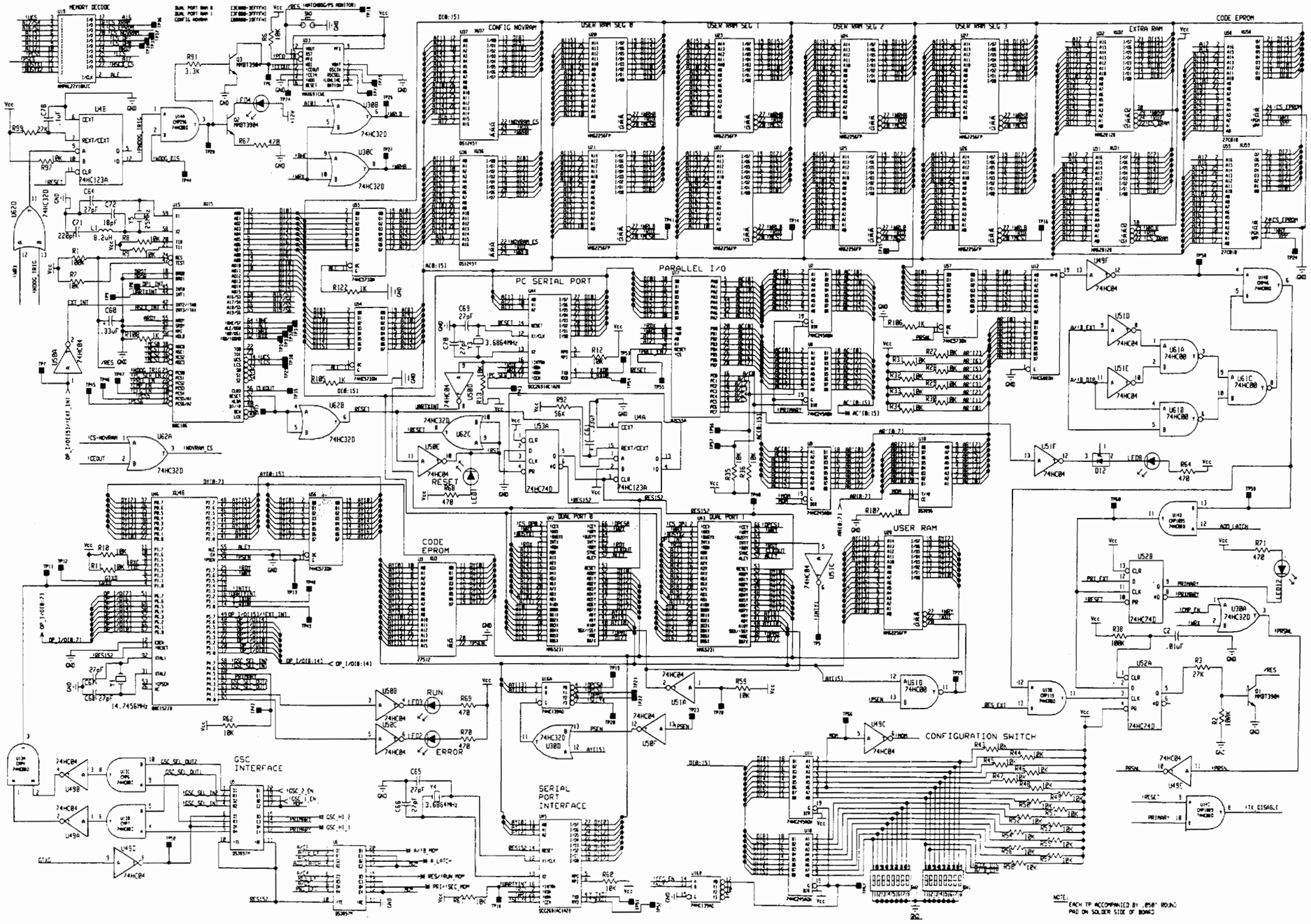


CAUTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES

CONTROLLER BOARD
19D903299P1

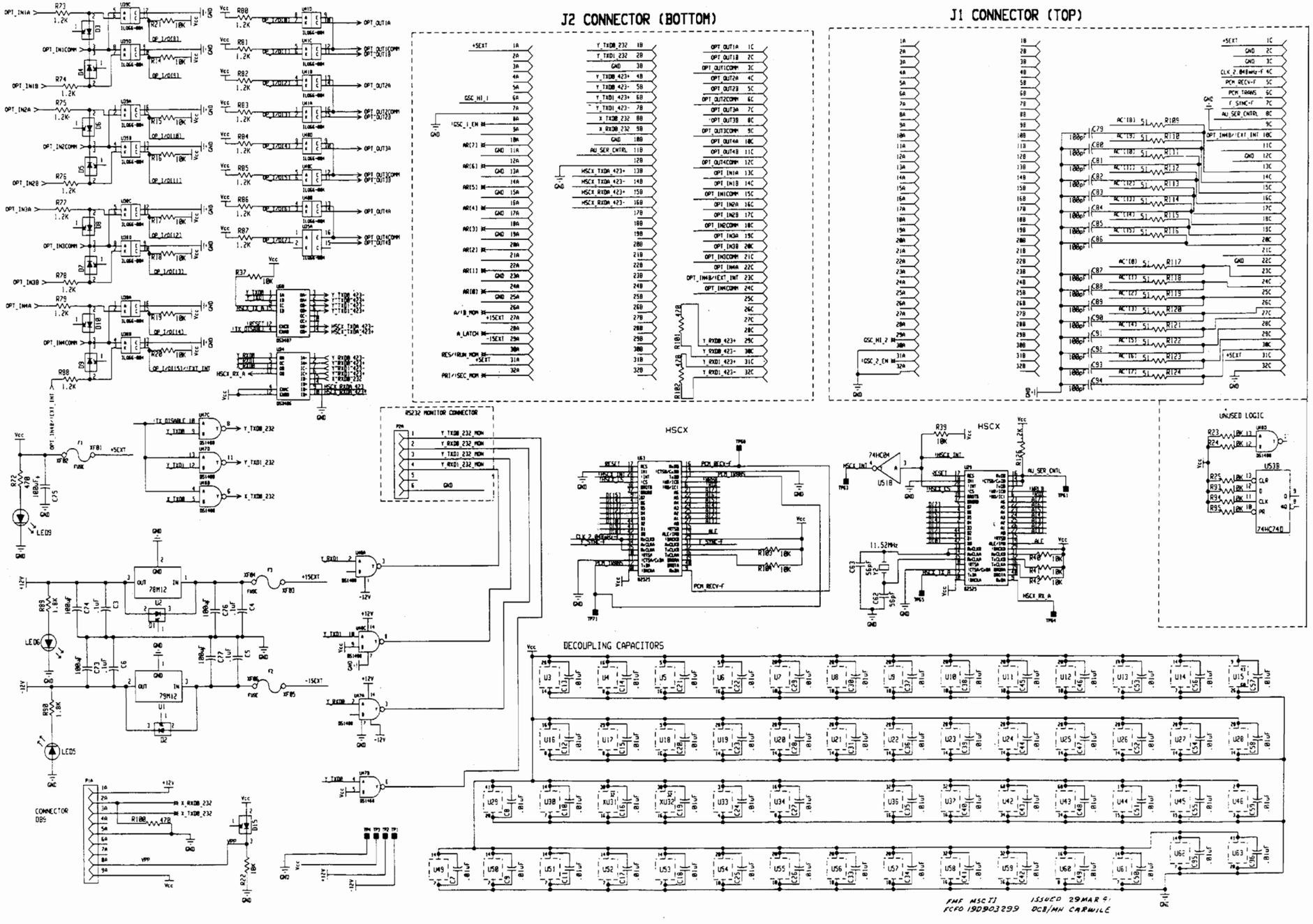
(19D903229, Rev. B (Flipped))
(TDI-T91084, Solder Side, Layer 4, Rev. 0)
(TDI-T91084, Solder Side, Layer 3, Rev. 0)





(19D903301, Sheet 1, Rev. E/M)

CONTROLLER BOARD
19D903299P1



CONTROLLER BOARD
19D903299P1

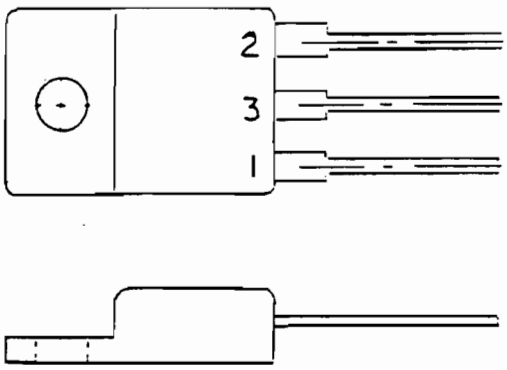
(19D903301, Sheet 2, Rev. E/M)

CONTROLLER BOARD
19D903299P1, REV. E/M

SYMBOL	GE PART NO.	DESCRIPTION
		- - - - - - - - - - -CAPACITORS- - - - - - - - - - -
C002	19A702052P14	CHIP: .01uF
C003 thru C006	19A702052P26	CHIP: .1uF
C007 thru C059	19A702052P14	CHIP: .01uF
C060 and C061	19A705205P12	CHIP: .33uF
C062 and C063	19A702061P49	CHIP: 56pF
C064 thru C070	19A702061P33	CHIP: 27pF
C071	19A702052P1	CHIP: 220pF
C072	19A702061P25	CHIP: 18pF
C073 thru C077	19A703314P4	LEADED: 47uF
C078	19A702052P26	CHIP: .1uF
C079 thru C094	19A702061P61	CHIP: 100pF
		- - - - - - - - - - -DIODES- - - - - - - - - - -
D001 thru D015	19A700053P2	CHIP
		- - - - - - - - - - -FUSE- - - - - - - - - - -
F001	19A134961P20	FUSE: 2.0
F002	19A134961P10	FUSE: .5
F003	19A134961P10	FUSE: .5
		- - - - - - - - - - CONNECTORS- - - - - - - - - -
J001 and J002	19B801587P4	CONNECTOR: 96 PIN
		- - - - - - - - - - INDUCTOR - - - - - - - - - -
L001	19A700021P28	CHIP: 8.2uH
		- - - - - - - - - - - LED's- - - - - - - - - -
LED01 thru LED12	19A703595P10	HLMP-1301-010
		- - - - - - - - - - -PLUGS- - - - - - - - - -
P001	19B209727P37	AMP: DB-9
P002	19J706197PXX	TELEPHONE TYPE: 6 PIN
		- - - - - - - - - - TRANSISTORS - - - - - - - - -
Q001 thru Q003	19A700076P2	CHIP
		- - - - - - - - - - -RESISTORS- - - - - - - - - -
R001 and R002	19A702931P401	CHIP: 100.0K 1%
R003	19B800607P273	CHIP: 27K 5%
R005 thru R036	19B800607P103	CHIP: 10K 5%
R038	19B800607P104	CHIP: 100K 5%
R039 thru R062	19B800607P103	CHIP: 10K 5%
R064	19B800607P561	CHIP: 560 5%
R067 thru R072	19B800607P471	CHIP: 470 5%
R073 thru R088	19B800607P122	CHIP: 1.2K 5%
R089 and R090	19B800607P182	CHIP: 1.8K 5%
R091	19B800607P332	CHIP: 3.3K 5%
R092	19B800607P563	CHIP: 56K 5%
R093 thru R095	19B800607P103	CHIP: 10K 5%
R097 and R099	19B800607P273	CHIP: 27K 5%
R100 thru R102	19B800607P471	CHIP: 470 5%
R103	19B800607P103	CHIP: 10K 5%
R104 thru R108	19B800607P102	CHIP: 1000 5%
R109 thru R124	19B800607P510	CHIP: 51 5%
R126	19B800607P122	CHIP: 1.2K 5%
R127	19B800607P102	CHIP: 1000 5%
		- - - - - - - - - - SWITCHES- - - - - - - - - -
SW01 and SW02	19A149955P1	SW3
SW03	19A149923P2	SW1
		- - - - - - - - TEST POINT CONNECTORS - - - - - - - -
TP01 thru TP76	344A3367P1	TP1622P1
		- - - - - - - -INTEGRATED CIRCUITS - - - - - - - -
U001	19A134718P2	MC7912CT: T-220: MOT
U002	19A134717P2	MC7812CT: T-220: MOT
U003SP	344A3373G1	27C512 (A705551P3): DIP-28: INTEL,TI (150 ns)
U004	19A704380P321	74HC123A: SO-16 N: MOT,TI,RCA
U005 and U006	19A149953P202	DS3897M: SO-20 W: NATIONAL
U007 thru U011	19A703471P108	74HC245ADW: SO-20 W: MOT,TI,RCA
U012	19A703483P318	74HC688DW: SO-20 W: MOT,TI,RCA
U013 and U014	19A703483P305	74HC08D: SO-14 N: MOT,TI,RCA
U015S	19A149880P1	80C186-16: PLCC-68: INTEL
U016	19A703471P321	74HC139AD: SO-16 N: MOT,TI,RCA
U017	19A705991P101	82C55A: PLCC-44: INTEL
U018	19A149953P201	DS3896: SO-20 W: NATIONAL
U019P	344A3173G2/3137P1	PAL22V10AJC: PLCC-28: AMD,CYPRESS,TI
U020 thru U028S	19A705981P2	62256-12: DIP-28: HITACHI
U029	19A149956P1	SAB82525N: PLCC-44: SIEMENS
U030	19A703483P311	74HC32AD: SO-14 N: MOT,TI,RCA
U033	19A149895P1	MAX691CWE: SO-16 W: MAXIM
U034	19A149929P201	DS3486: SO-16 N: NATIONAL
U036S and U037S	344A3067P1	DS1245Y-120: DIP-32: NATIONAL
U038 thru U041	344A3071P1	ILQ66-4-004: DIP-16 SMT: HP,TI
U042 and U043	344A3054P301	HM65231-5: PLCC-68: HITACHI
U044 and U045	344A3059P201	SCC2691AC1A28: PLCC-28: SIEMENS
U046S	19A705982P101	80C152JB-1: PLCC-68: INTEL
U047 and U048	19A116704P101	DS1488: SO-14 N: NATIONAL,MOT
U049 thru U051	19A703483P104	74HC04: SO-14 N: MOT,TI,RCA
U052 and U053	19A704380P302	74HC74D: SO-14 N: MOT,TI,RCA
U054 thru U057	19A7034471P318	74HC573DW: SO-20 W: MOT,TI,RCA
U058SP	344A3137G3	27C010 (A149954P1): DIP-32: INTEL,TI
U059SP	344A3137G4	27C010 (A149954P1): DIP-32: INTEL,TI
U060	19A149930P201	DS3487: SO-16 N: NATIONAL
U061	19A703483P302	74HC00: SO-14 N: MOT,TI,RCA
U062	19A703483P311	74HC32AD: SO-14 N: MOT,TI,RCA
U063	19A149956P1	SAB82525N: PLCC-44: SIEMENS
		- - - - - - - - - - -FUSE CLIPS- - - - - - - - - -
XF01 thru XF30	19A116688P2	FUSE CLIPS
		- - - - - - - - - - IC SOCKETS - - - - - - - - - -
XU03	19A700156P3	SOCKET: DIP-28
XU15	344A3339P5	SOCKET: PLCC-68
XU28 thru XU37	19A700156P3	SOCKET: DIP-28
XU46	344A3339P5	SOCKET: PLCC-68
XU58 and XU59	19A700156P17	SOCKET: DIP-32
		- - - - - - - - - - -CRYSTALS- - - - - - - - - -
Y001	19A702511G37	XTL14P7456MHZ: 14.7456MHz: DALE,CTS
Y002	19A702511G5	XTL11P52MHZ: 11.52MHz: DALE,CTS
Y003	19A702511G9	XTL3P6864MHZ: 3.6864MHz: DALE,CTS
Y004	19A702511G9	XTL3P6864MHZ: 3.6864MHz: DALE,CTS
Y005	19A702511G45	XTL25MHZ: 25.0 MHZ: DALE,CTS

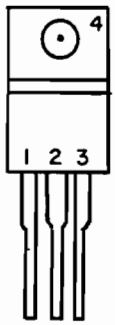
*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

VOLTAGE REGULATOR U001
19A134718P2 (MC7912CT)



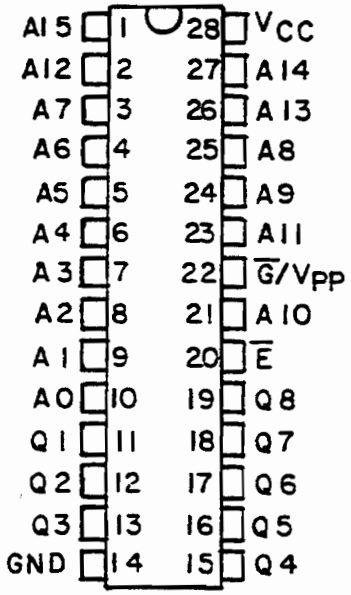
1. COMMON
2. OUTPUT
3. INPUT

VOLTAGE REGULATOR U002
19A134717P2 (MC7812CT)

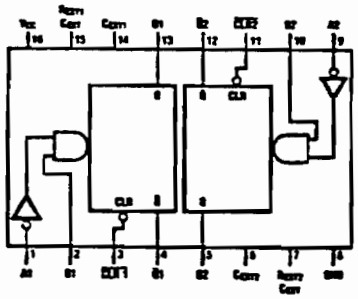


1. INPUT
2. COMMON
3. OUTPUT
4. TAB COMMON

EPROM U003
344A3373G12 (27C512 (A705551P3)



DUAL MULTIVIBRATOR U004
19A704380P321 (74HC123A)

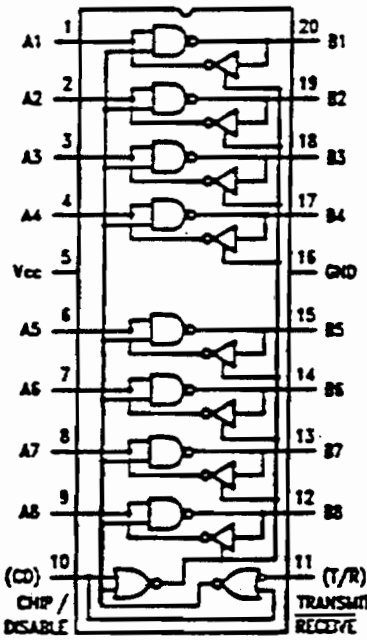


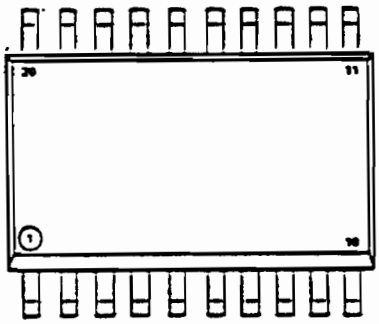
Truth Table

Inputs			Outputs	
$\overline{Clear}$	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ One High Level Pulse
⎎ One Low Level Pulse
X = Irrelevant

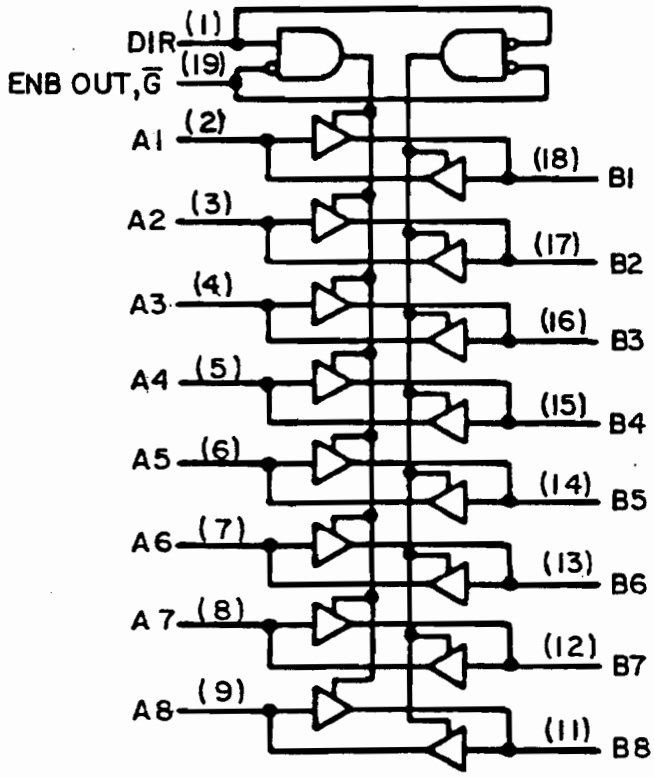
TRANSCEIVERS U005/U006
19A149953P202 (DS3897M)





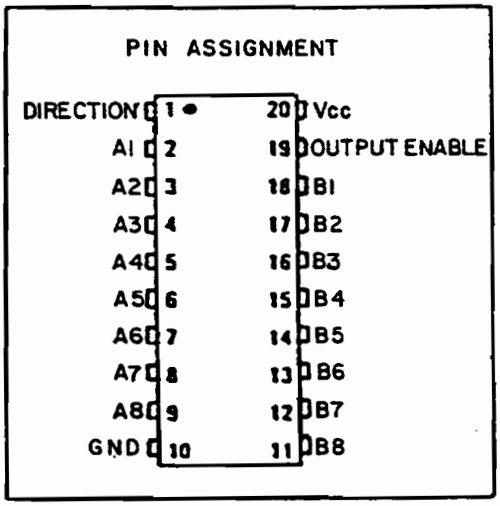
OCTAL BUS TRANSCEIVERS
U007/U008/U009/U010/U011
19A703471P108 (74HC245ADW)

LOGIC DIAGRAM (POSITION LOGIC)



PIN 10 = GND
PIN 20 = Vcc

PIN ASSIGNMENT



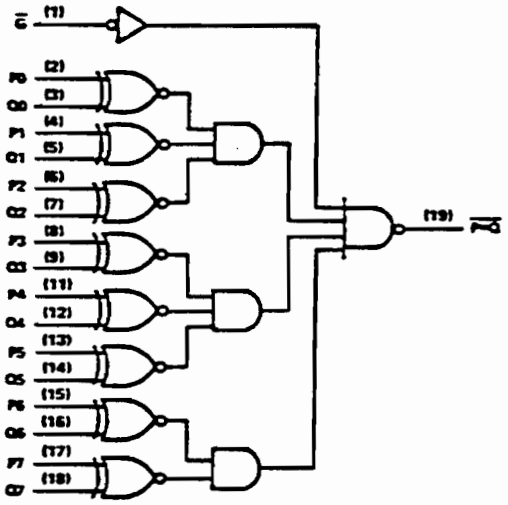
FUNCTION TABLE

CONTROL INPUTS		OPERATION
OUTPUT ENABLE	DIRECTION	
L	L	DATA TRANSMITTED FROM BUS B TO BUS A
L	H	DATA TRANSMITTED FROM BUS A TO BUS B
H	X	BUSES ISOLATOR (HIGH IMPEDANCE STATE)

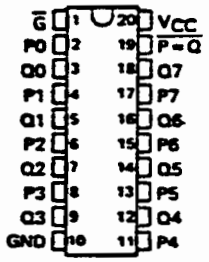
X=DON'T CARE

8-BIT WORD COMPARATOR U012
19A703483P318 (74HC688DW)

logic diagrams (positive logic)



SN74HC688 . . . DW OR N PACKAGE
(TOP VIEW)

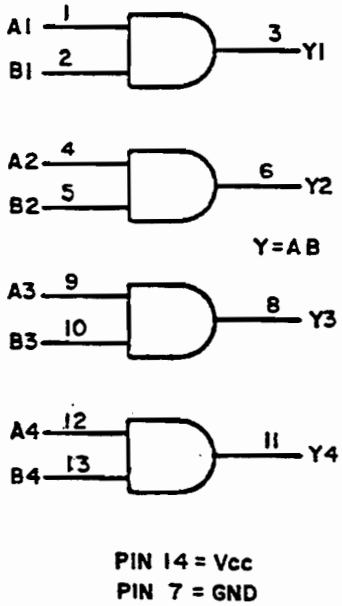


FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{G}$	$\overline{P=Q}$
P=Q	L	L
P>Q	X	H
P<Q	X	H
X	H	H

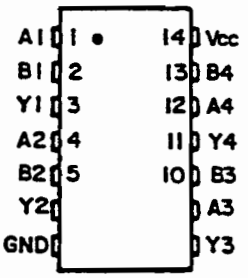
QUAD 2-INPUT AND GATES U013/U014
19A703483P305 (74HC08D)

LOGIC DIAGRAM



PIN 14 = Vcc
PIN 7 = GND

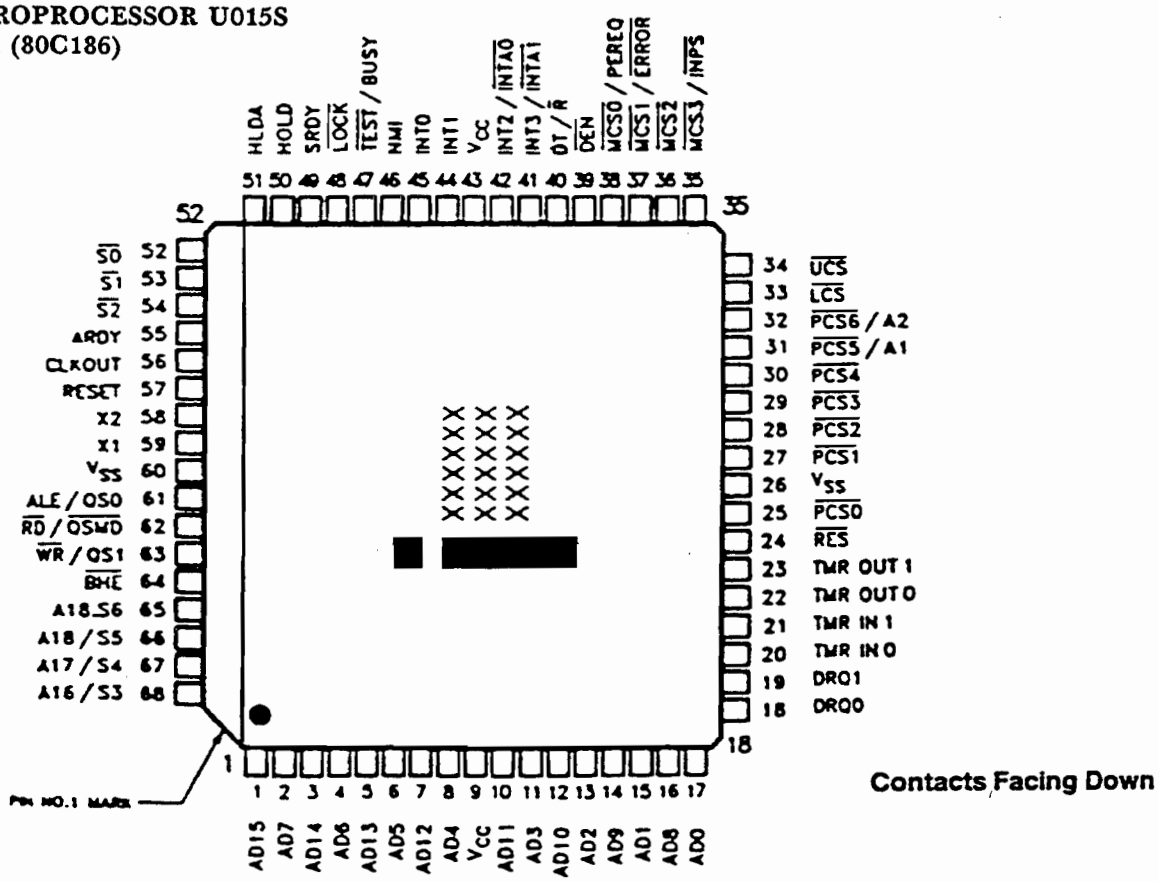
PIN ASSIGNMENT



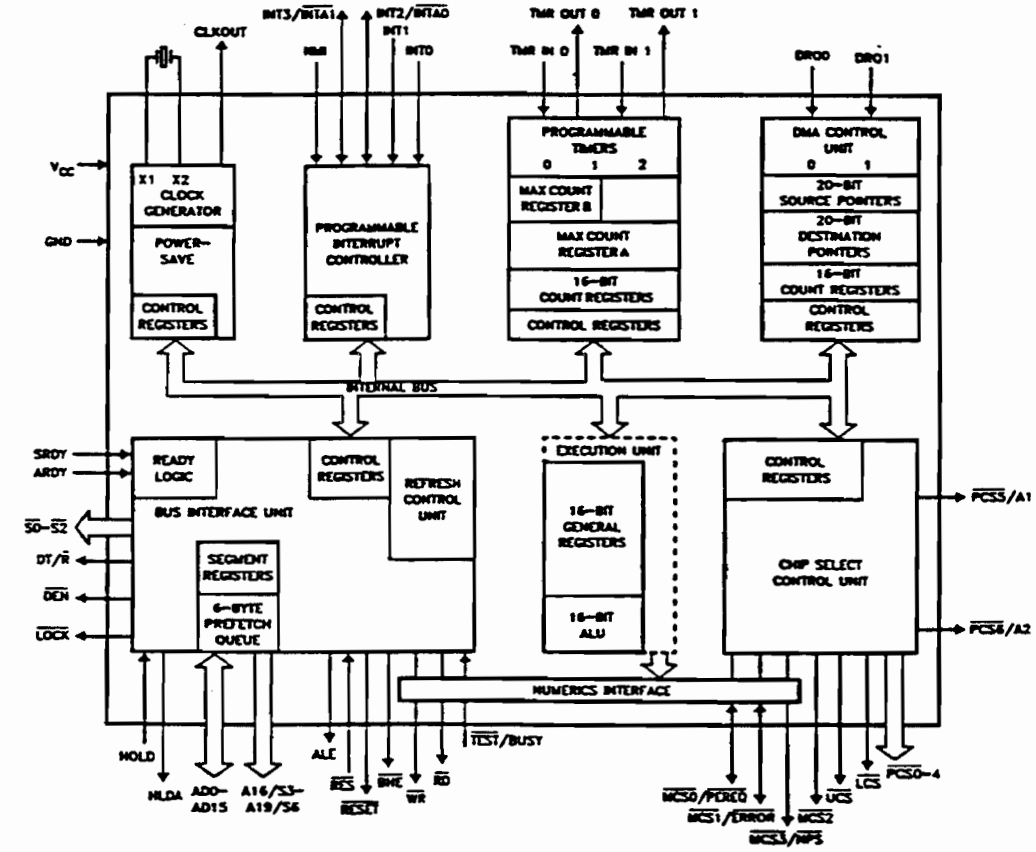
FUNCTION CHART

INPUT		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

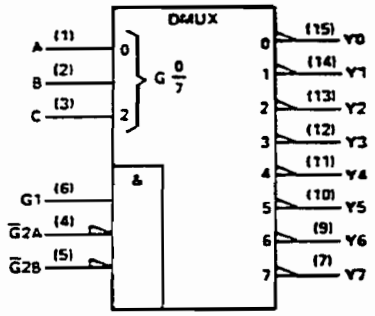
16-BIT MICROPROCESSOR U015S
19A149880P1 (80C186)



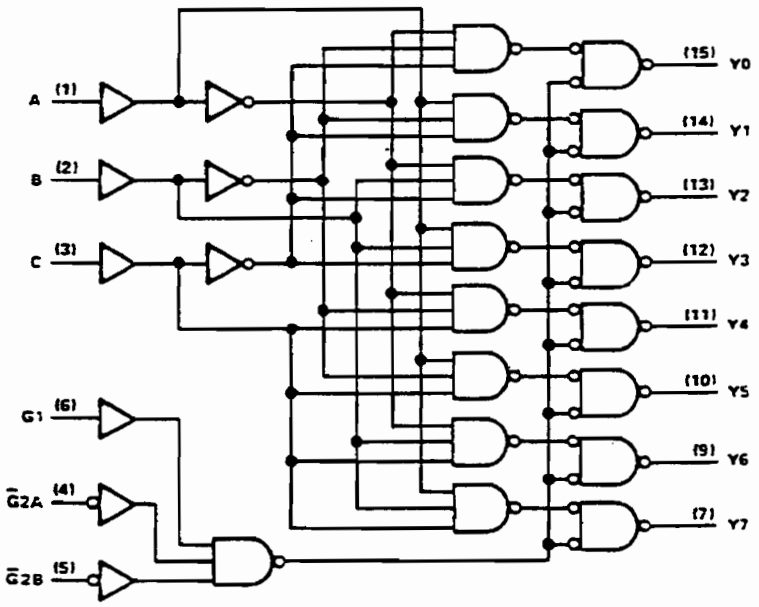
Contacts Facing Down



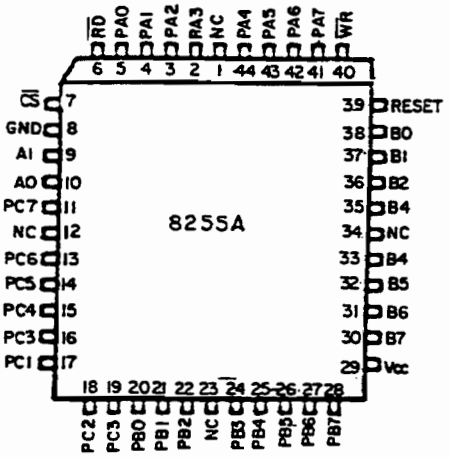
DUAL 1-OF-4 DECODE/DEMUX U016
19A703471P321 (74HC139AD)



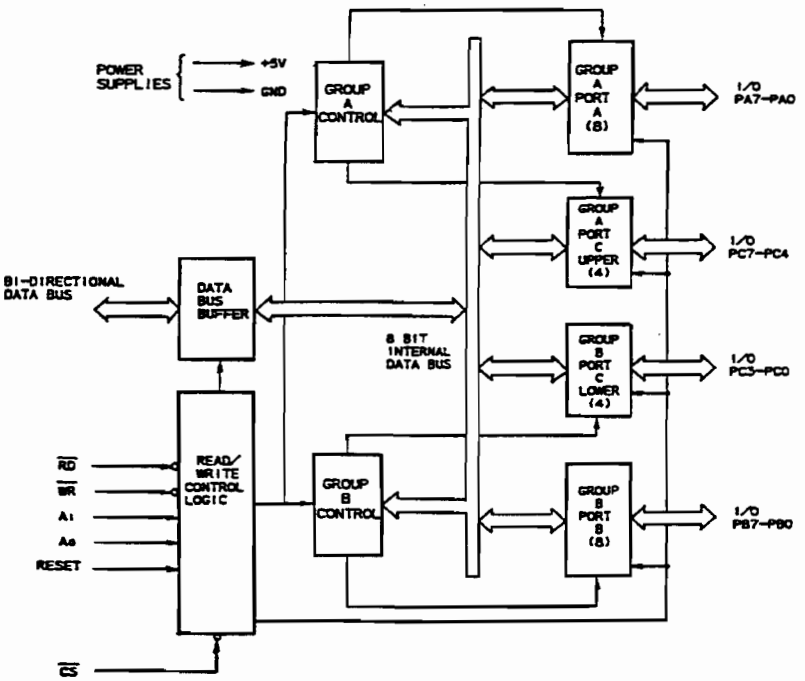
LOGIC DIAGRAM (POSITIVE LOGIC)



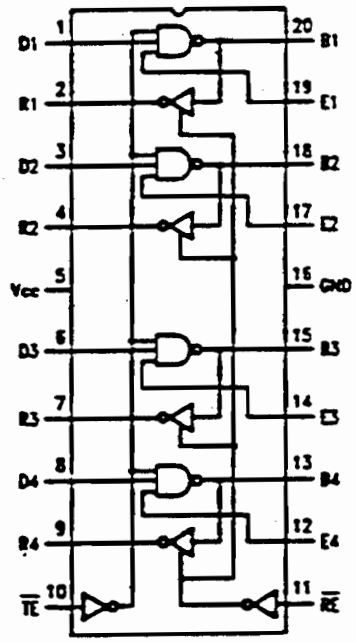
CMOS PROGRAMMABLE PERIPHERAL INTERFACE U017
19A705991P101 (82C55A)

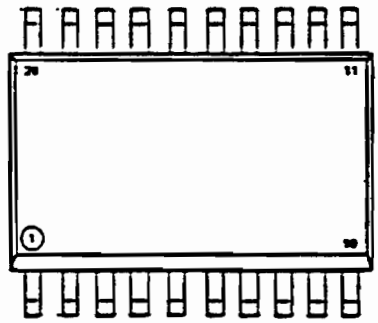


BLOCK DIAGRAM

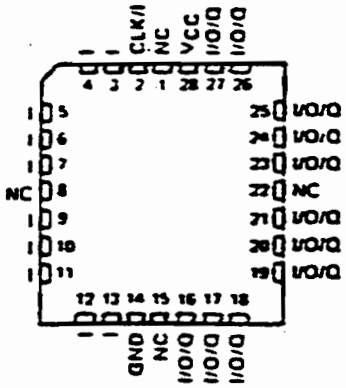


TRANSCEIVER U018
19A149953P201 (DS3896)





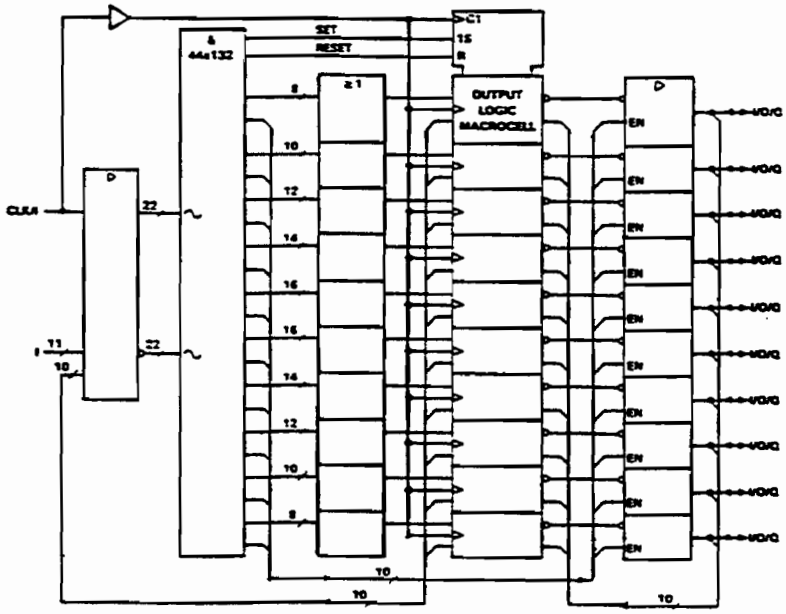
PROGRAMMABLE LOGIC ARRAY U019P
344A3173G2/3137P1 (PAL22V10AJC)



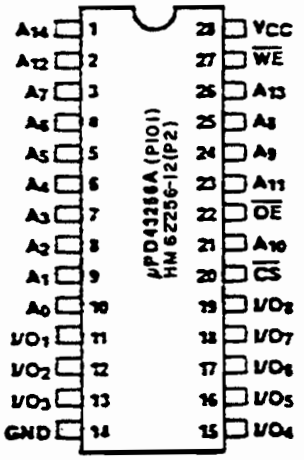
NC—No internal connection

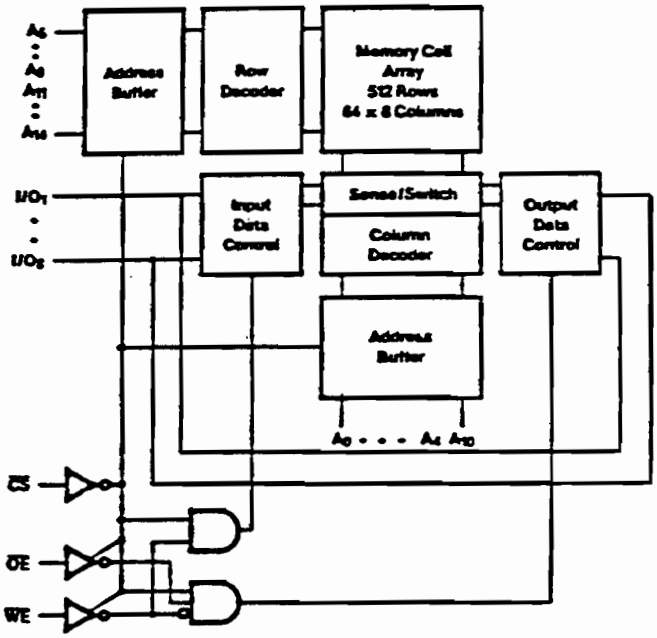
Pin assignments in operating mode

functional block diagram (positive logic)

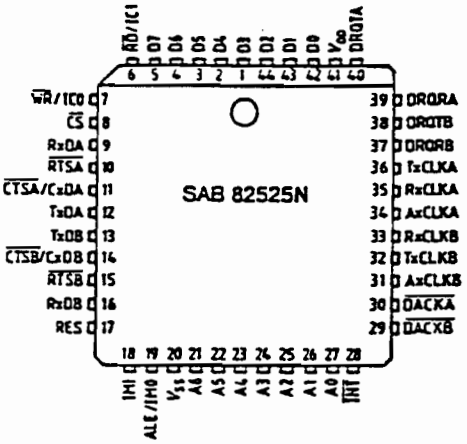


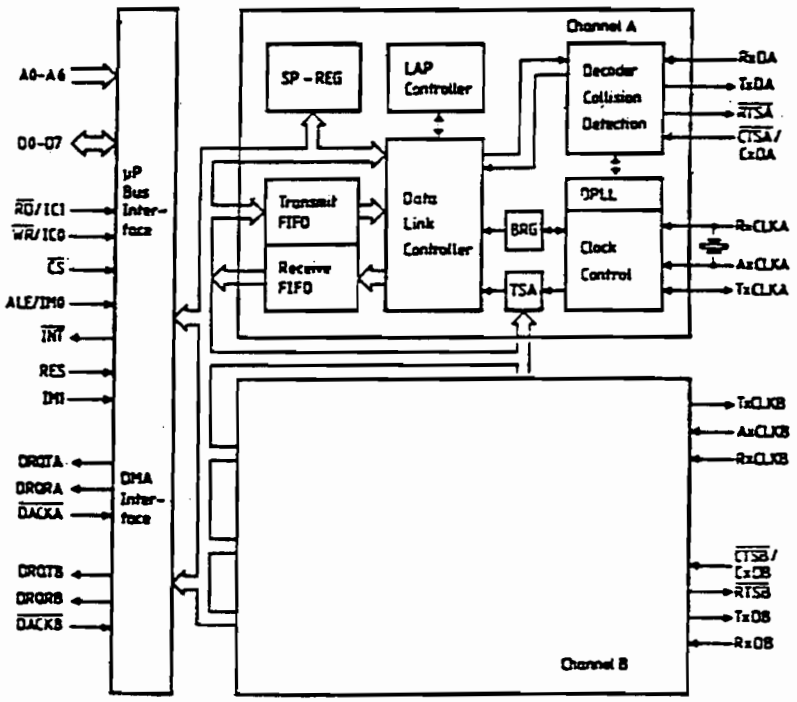
32K x 8 CMOS STATIC RAM
U020/U021/U022/U023/U024
U025/U026/U027/U028S
19A705981P2 (HM62256-12)



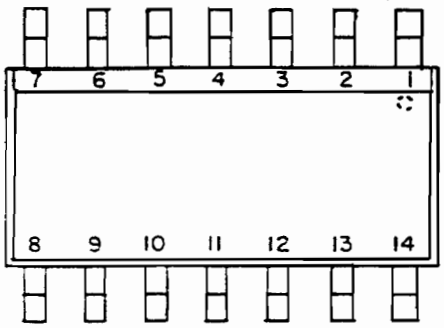


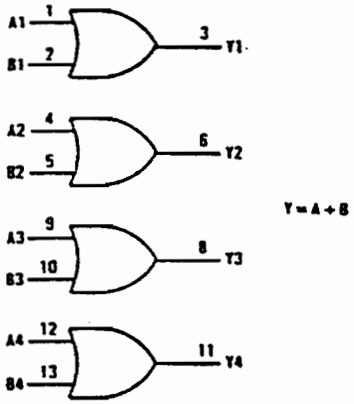
SERIAL COMMUNICATIONS CONTROLLER U029/U63
19A149956P1 (SAB82525N)





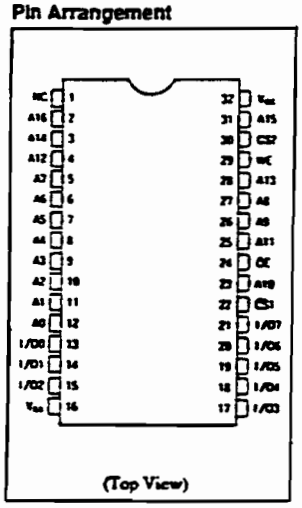
QUAD 2-INPUT OR GATES U030
19A703483P311 (74HC32AD)



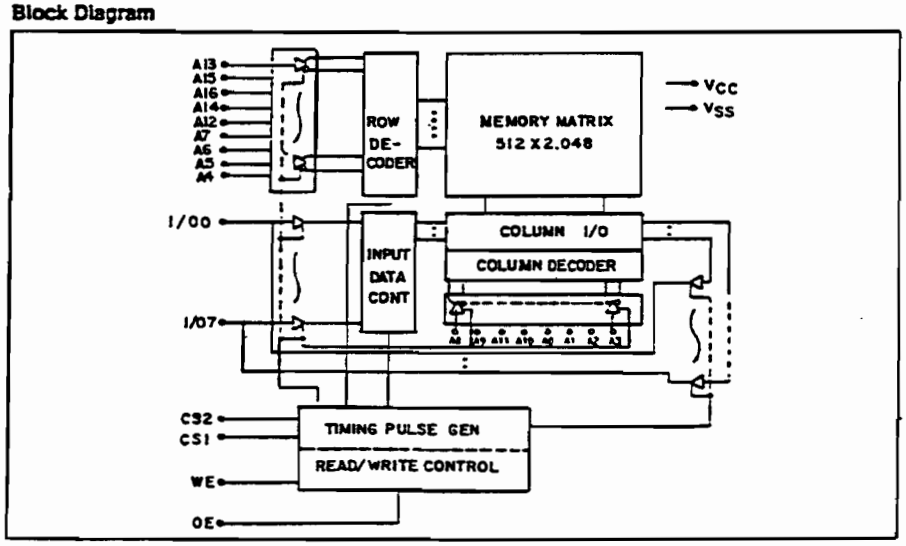


EXTRA RAM U031/U032
(HM628125)

Pin Arrangement

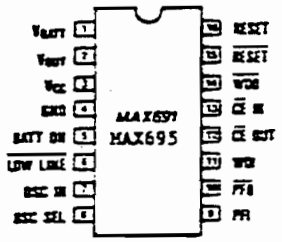


Block Diagram

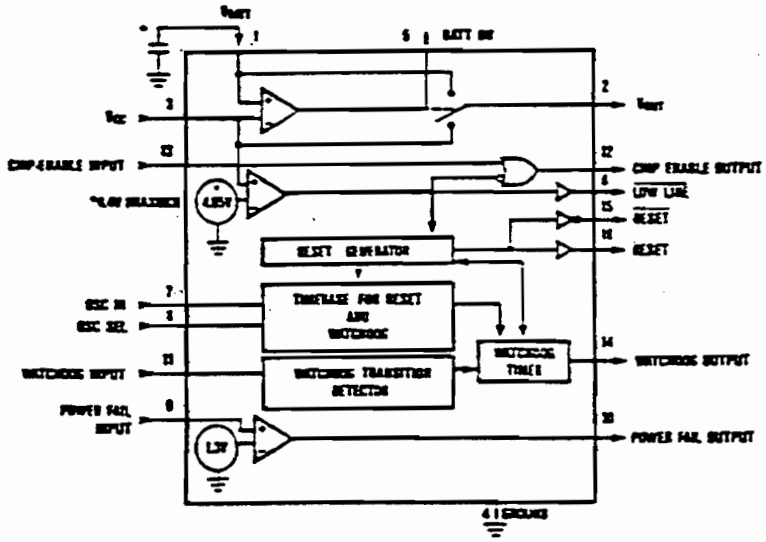


WATCH-DOG TIMER U033
19A149895P1 (MAX691CWE)

BLOCK DIAG.

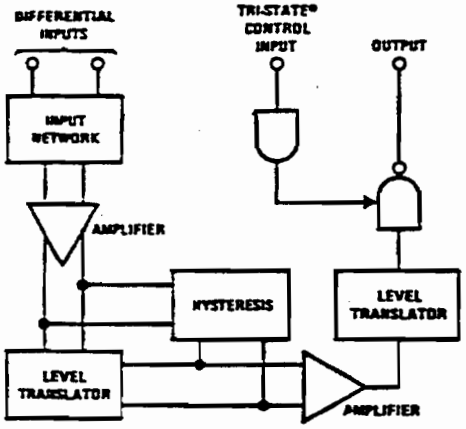


TOP VIEW

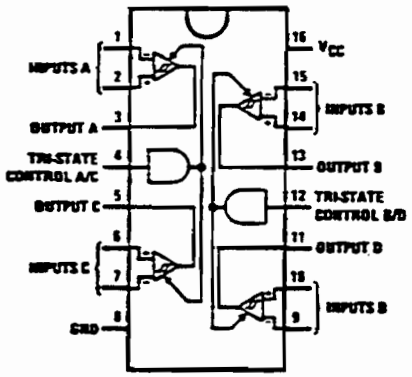


QUAD LINE RECEIVER RS-423 U034
19A149929P201 (DS3486)

Block and Connection Diagrams



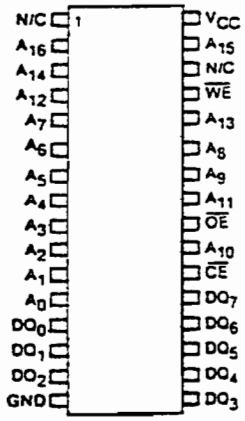
Dual-In-Line Package



Top View

128k X 8 NON-VOLATILE SRAM U036S/U037S
344A3067P1 (DS1245Y-120)

PIN CONNECTIONS

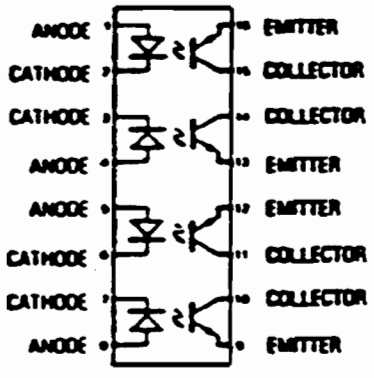


PIN NAMES

A_0-A_{16}	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ_0DQ_7	- Data In/Data Out
V_{CC}	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
N/C	- No Connect

OPTO COUPLER
U038/U039/U040/U041
344A3071P1 (ILQ66-4-004)

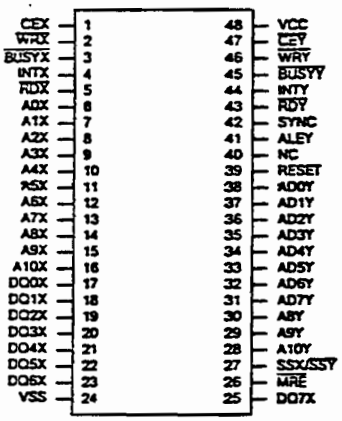
TOP VIEW

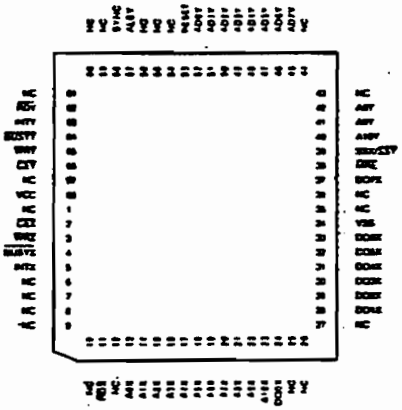


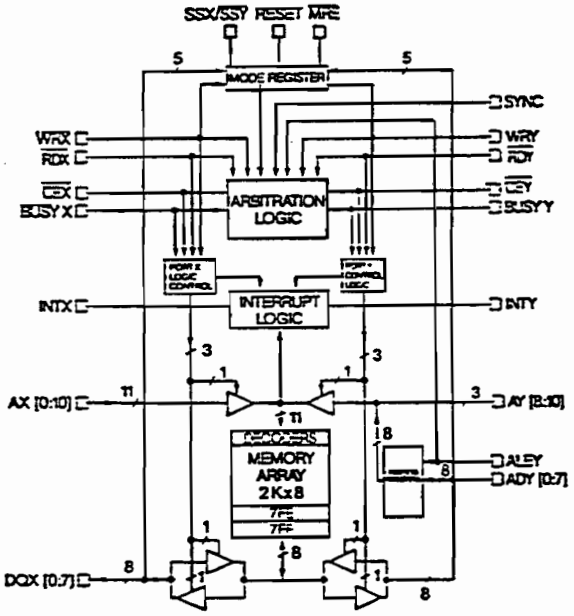
LED CHIPS ON PINS 2, 3, 6, 7
PT CHIPS ON PINS 10, 11, 14, 15

2k X 8 DUAL PORT RAM U042/U043
344A3054P301 (HM65231-5)

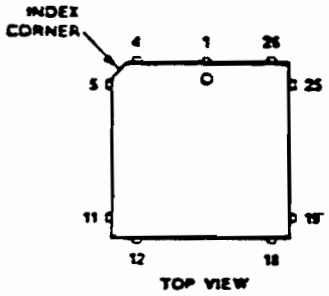
PIN IDENTIFICATION



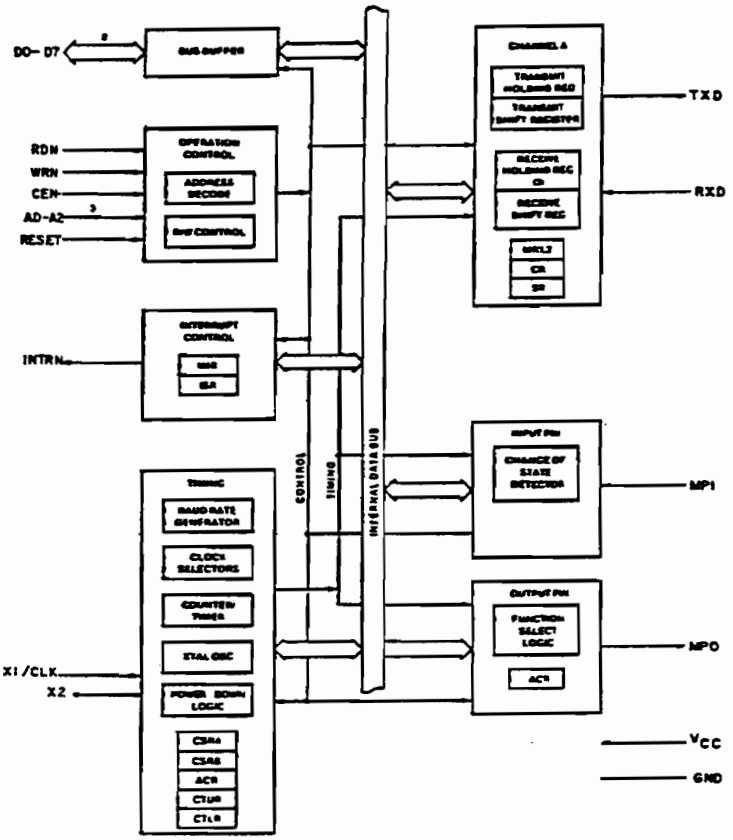




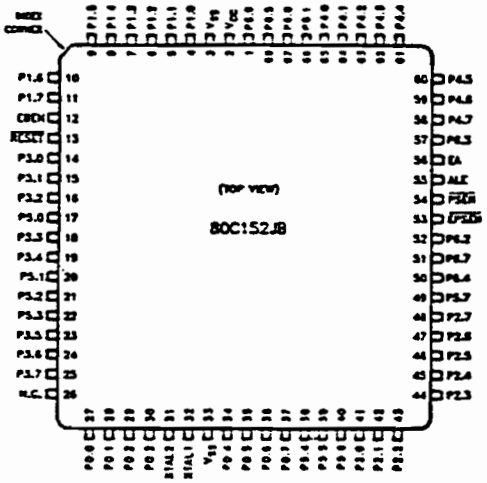
UART COMMUNICATIONS DEVICE U044/U045
344A3059P201 (SCC2691AC1A28)

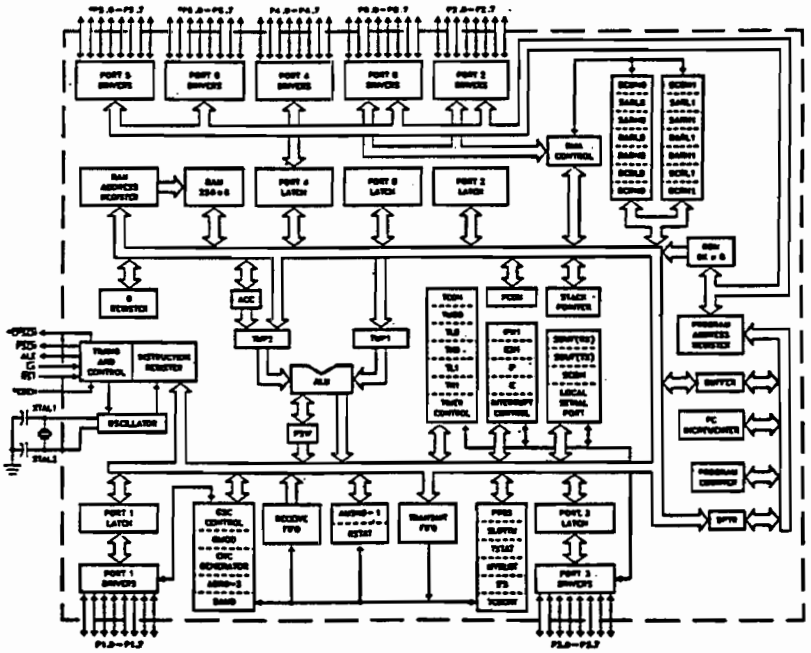


Pin	Symbol	Pin	Symbol
1	V_{CC}	15	GND
2	RDN	16	INTRN
3	R$\overline{x}$D	17	CEN
4	T$\overline{x}$D	18	D7
5	MPO	19	D6
6	MPI	20	D5
7	NC	21	D4
8	NC	22	D3
9	A2	23	NC
10	A1	24	D2
11	A0	25	D1
12	X1/CLK	26	NC
13	X2	27	D0
14	RESET	28	WRN

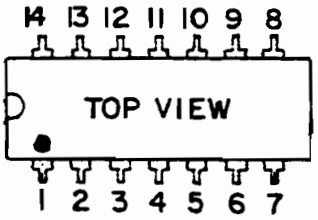


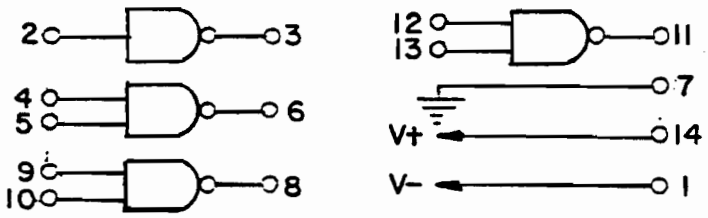
MICROCOMPUTER U046S
19A705982P101 (80C152JB-1)



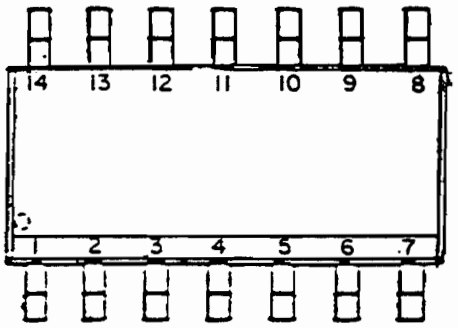


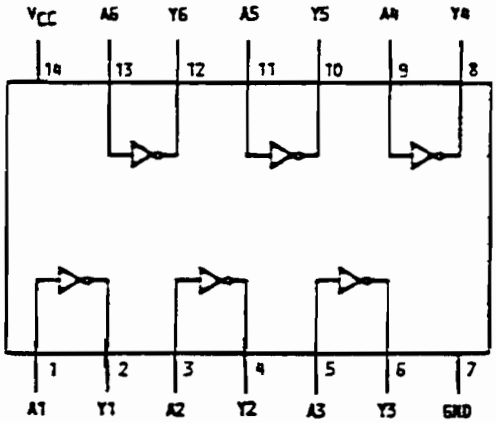
QUAD DTL RS-232C LINE DRIVER U047/U048
19A116704P101 (DS1488)



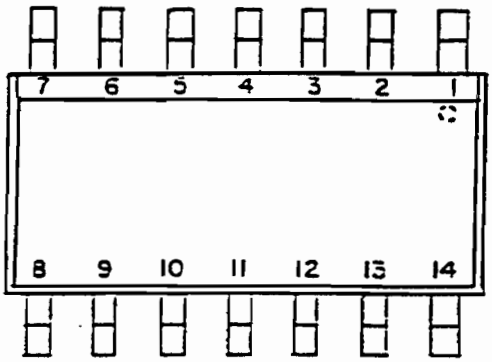


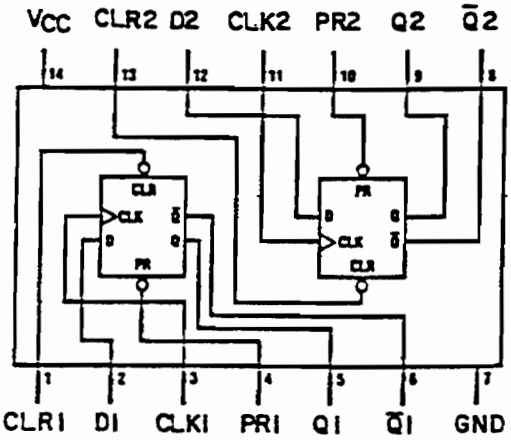
HEX INVERTERS
U049/U050/U051
19A703483P104 (74HC04)





CMOS DUAL D FLIP-FLOP W/SET-RESET
U052/U053
19A704380P302 (74HC74D)





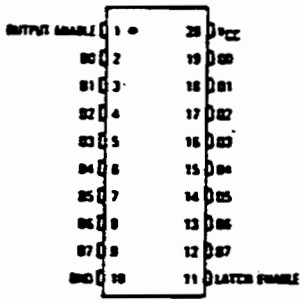
Inputs				Outputs	
PR	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	Q̄0

Note: Q0 = the level of Q before the indicated input conditions were established.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

OCTAL 3-STATE NON INVERTING LATCH
UO54/U055/U056/U057
19A703471P318 (74HC573DW)

PIN ASSIGNMENT

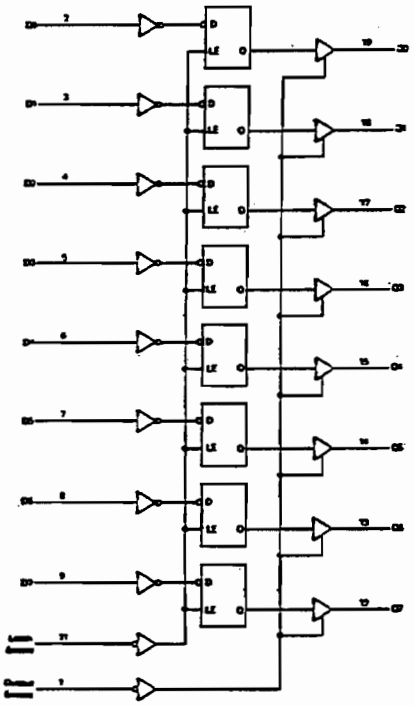


FUNCTION TABLE

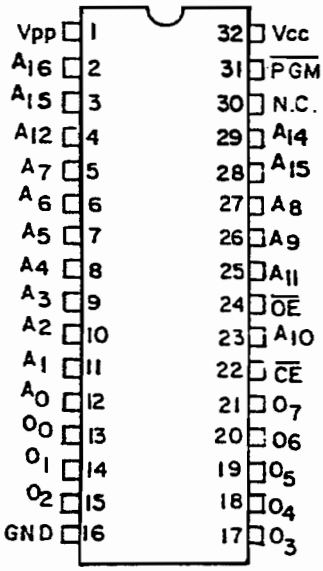
Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

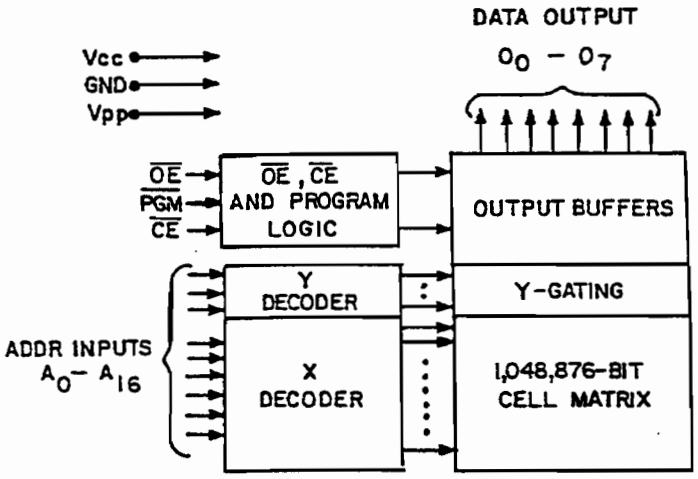
X = don't care
Z = high impedance

EXPANDED LOGIC DIAGRAM



128k X 8 EPROM U058SP/U059SP
344A3137G3/G4 (27C010 (A149954P1))

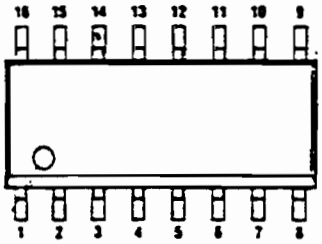




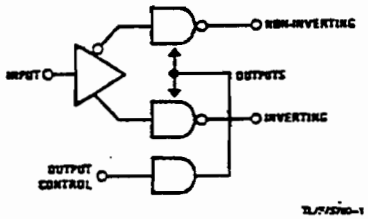
PIN NAME

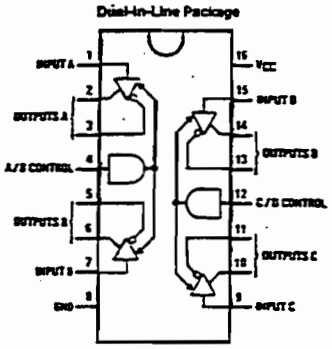
$A_0 - A_{14}$	ADDRESSES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
$O_0 - O_7$	OUTPUTS
$\overline{PGM}$	PROGRAM
NC	NO CONNECT

QUAD RS-422 LINE DRIVER U060
19A149930P201 (DS3487)



Block and Connection Diagrams





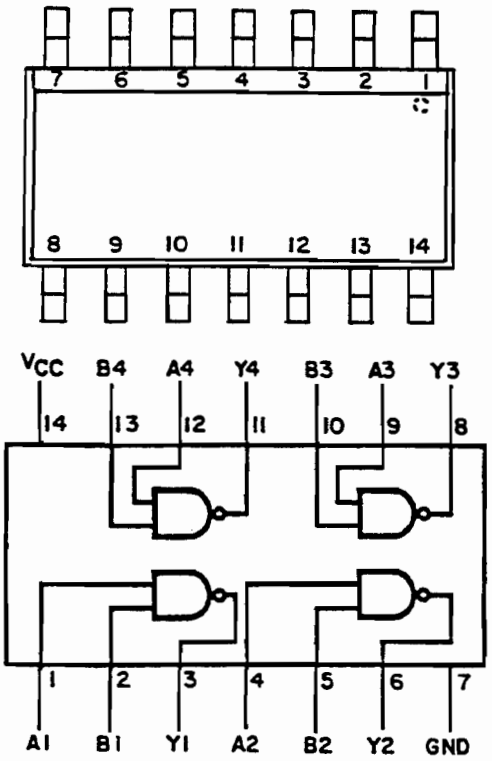
Top View

Truth Table

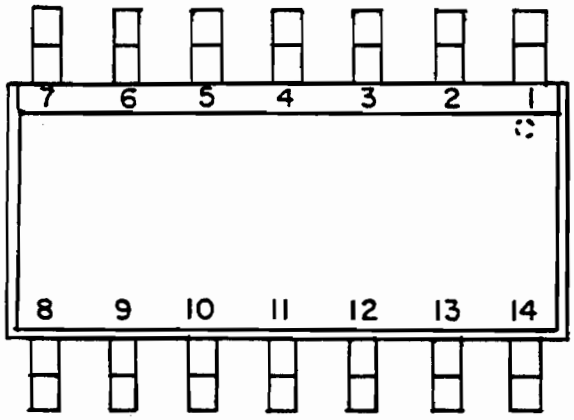
Input	Control Input	Non-Inverter Output	Inverter Output
H	H	H	L
L	H	L	H
X	L	Z	Z

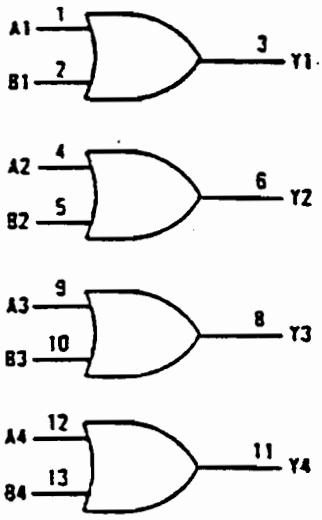
L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

QUAD 2-INPUT NAND GATE U061
19A703483P302 (74HC00)



QUAD 2-INPUT OR GATES U062
19A703483P311 (74HC32AD)





$Y = A + B$

PIN 14 = V_{CC}
PIN 7 = GND

ADDENDUM NO. 1 TO LBI-38667A (PCMS)

This addendum adds information on Controller Board 19D903299P3. This Controller Board replaces Controller Board 19D903299P1 in all CEC/IMC Digital Audio Switch applications. Backwards compatibility with the P1 Controller Board is retained. A revised maintenance manual completely documenting P3 Controller Board will be issued at a later date. Contact your service representative for additional information.

Controller Board 19D903299P3 information added by this addendum includes the board's:

- Assembly/Outline Diagram (pages 2 and 3)
- Schematic Diagram (pages 4 thru 9)
- Parts List (pages 10 thru 12)
- Production Changes (page 12)

5 JUMPER Q2 PIN 2 TO ONE SIDE OF R139.

6 JUMPER THE OTHER SIDE OF R139 TO R91.

7 CONNECT R138 BETWEEN U42 PIN 49 AND R132.

8 JUMPER U47 PIN 12 TO U48 PIN 9.

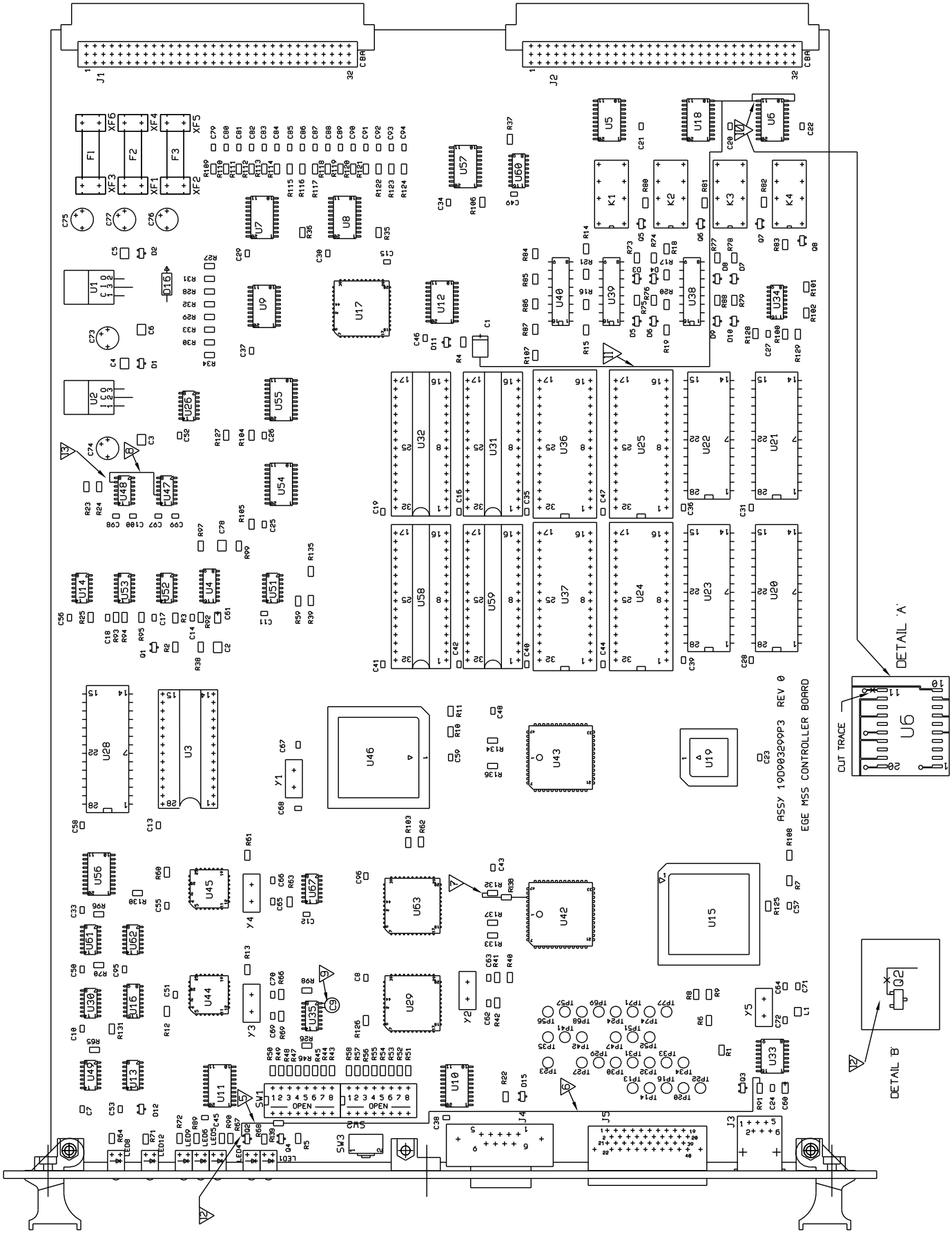
9 CONNECT C9 BETWEEN U35 PIN 6 AND U35 PIN 7.

10 SEE DETAIL 'A' TO CUT TRACE TO U6 PIN 11 ON COMPONENT SIDE OF PWB.

11 JUMPER U6 PIN 10 TO U6 PIN 11 TO U18 PIN 10 TO C1.

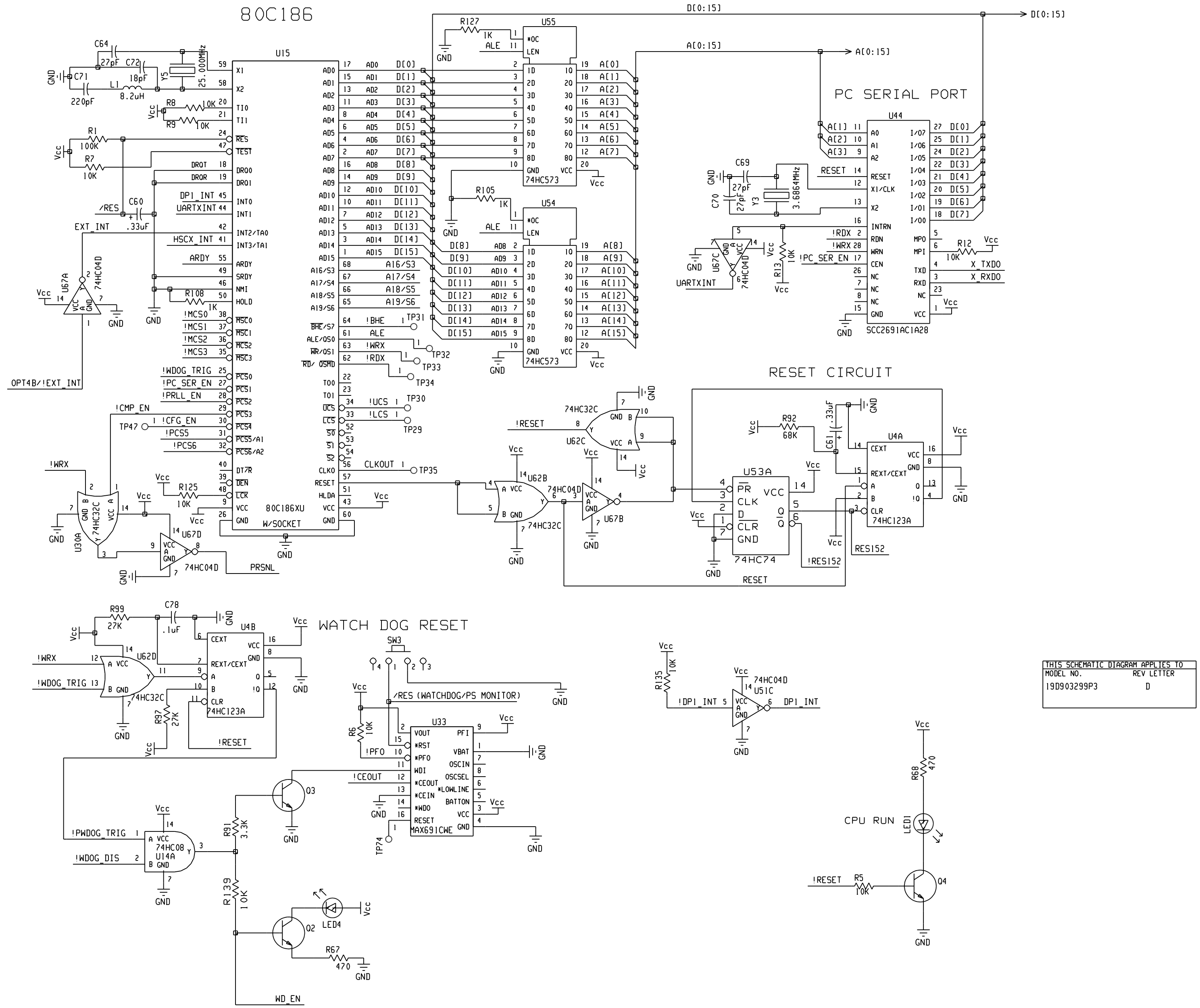
12 CUT TRACE TO Q2 PIN 2 ON COMPONENT SIDE OF PWB. SEE DETAIL 'B'.

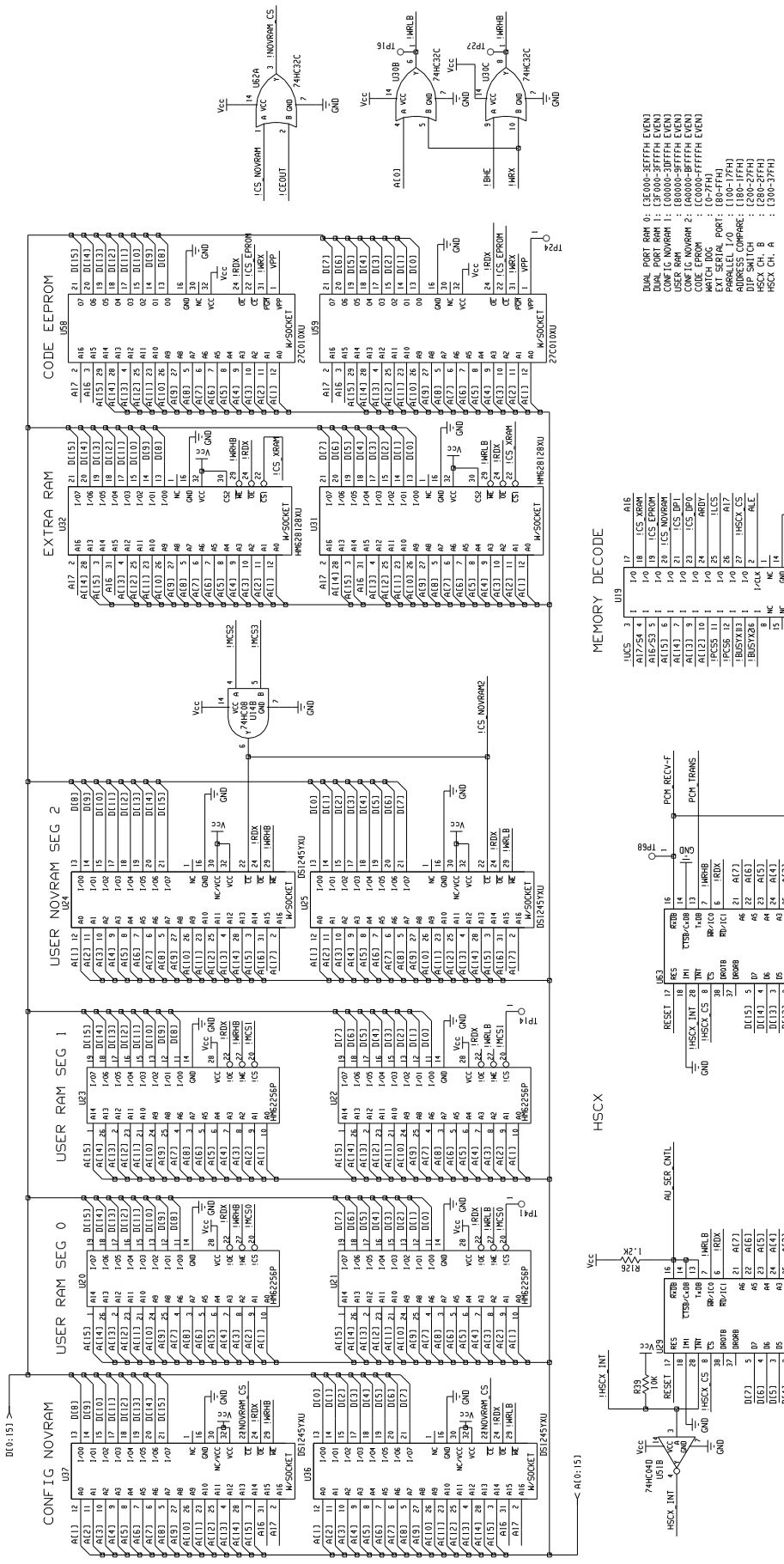
13 CUT TRACE TO U48 PIN 9 ON COMPONENT SIDE OF PWB. BETWEEN R24 AND U48 PIN 9.

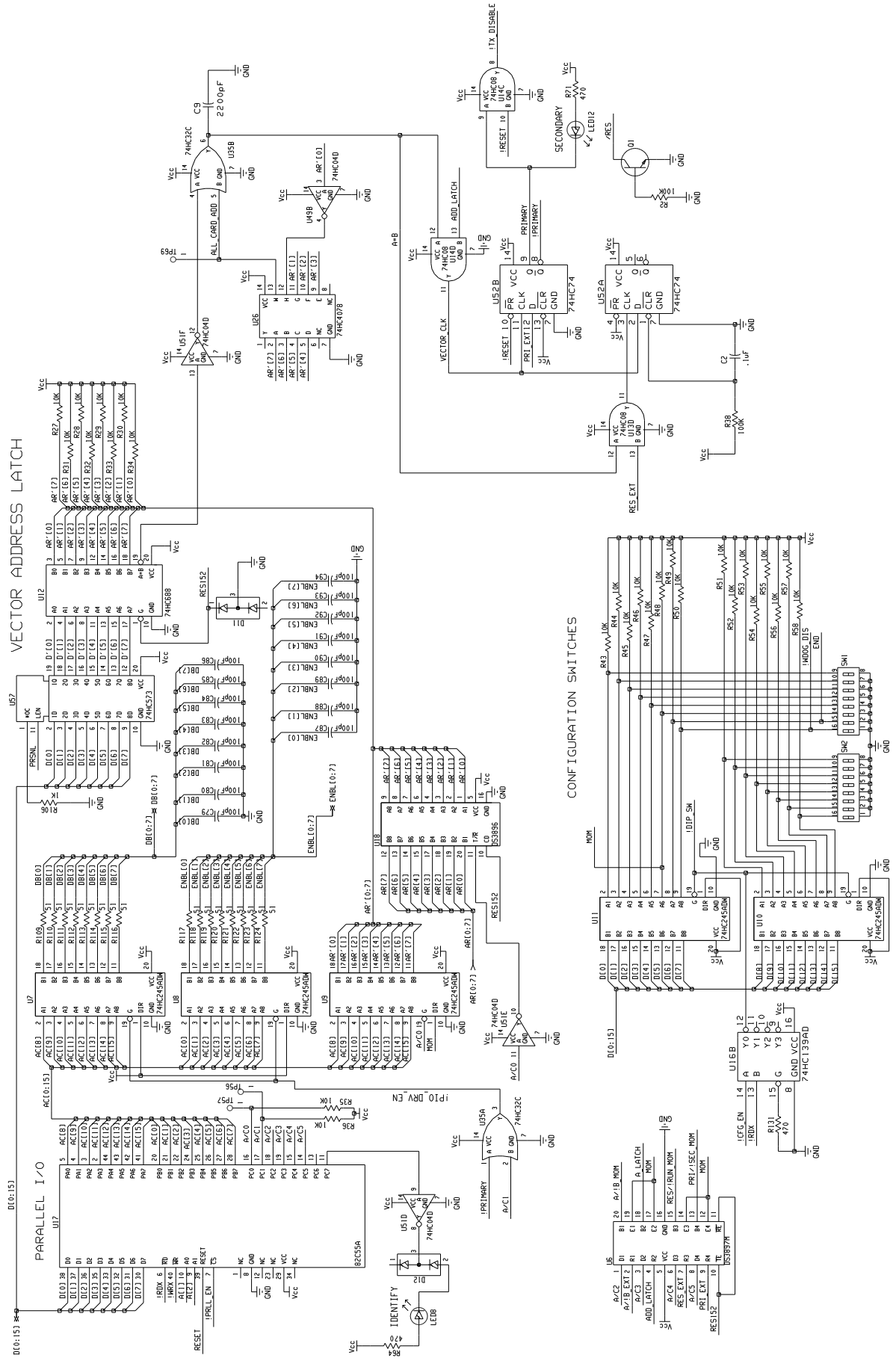


(19D903299, Sh. 2, Rev. 5)

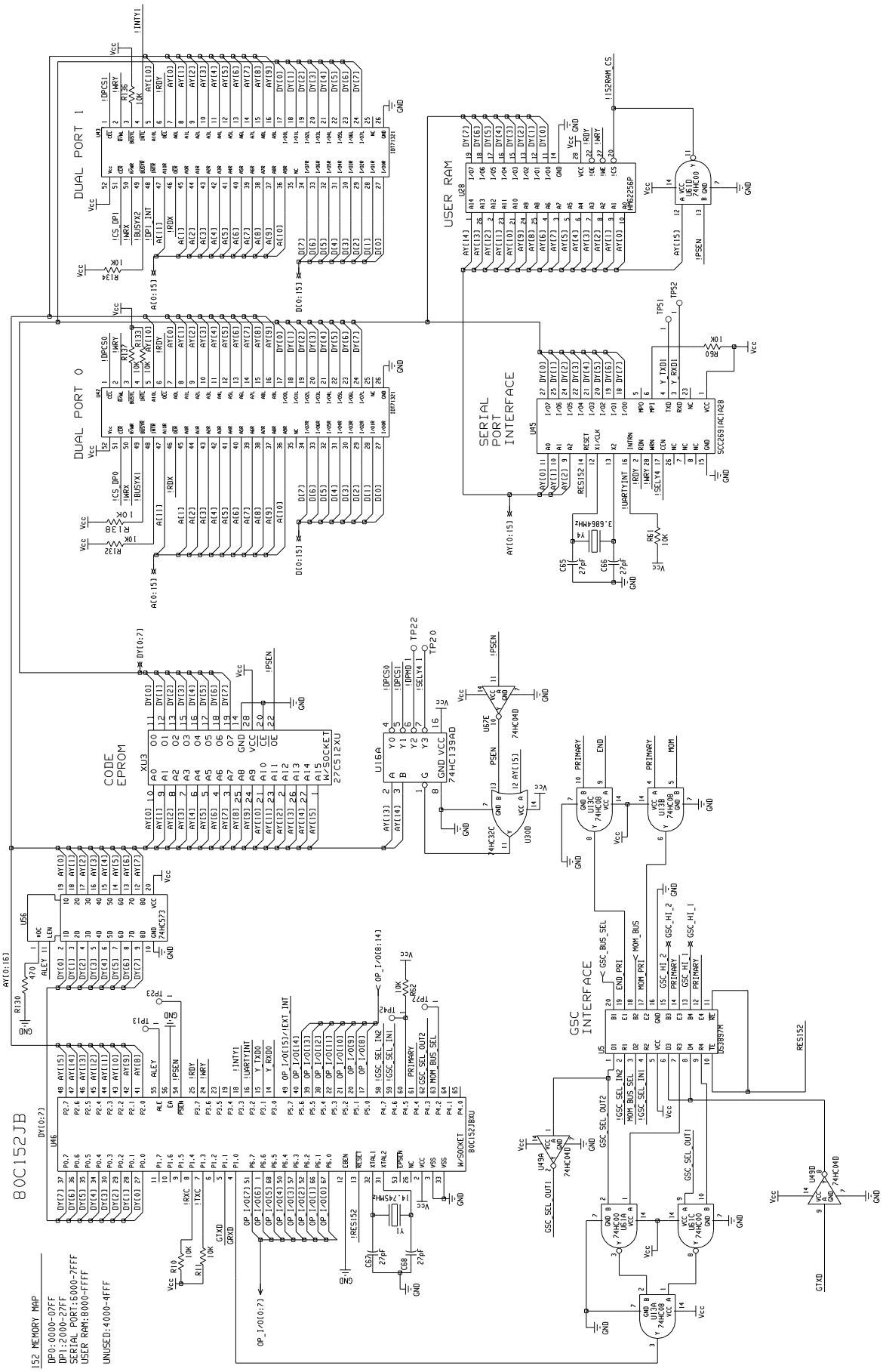
(19D903980, Sh. 1, Rev. 2)




CODE EEPROM
EXTRA RAM
USER NOVRAM SEG 2
USER RAM SEG 1
USER RAM SEG 0
CONFIG NOVRAM
MEMORY DECODE
HSCX
DUAL PORT RAM 0: (3E000-3EFFFH EVEN)
DUAL PORT RAM 1: (3C000-3CFFFH EVEN)
CONFIG NOVRAM : (00000-03DFFH EVEN)
USER RAM : (80000-9FFFFH EVEN)
CONFIG NOVRAM 2: (A0000-BFFFFH EVEN)
CODE EPROM : (C0000-FFFFFH EVEN)
WATCH DOG : (0-7FH)
EXT SERIAL PORT: (80-FFH)
PARALLEL I/O : (100-17FH)
ADDRESS COMPARE: (180-1FFH)
DIP SWITCH : (200-27FH)
HSCX CH. B : (280-2FH)
HSCX CH. A : (300-37FH)

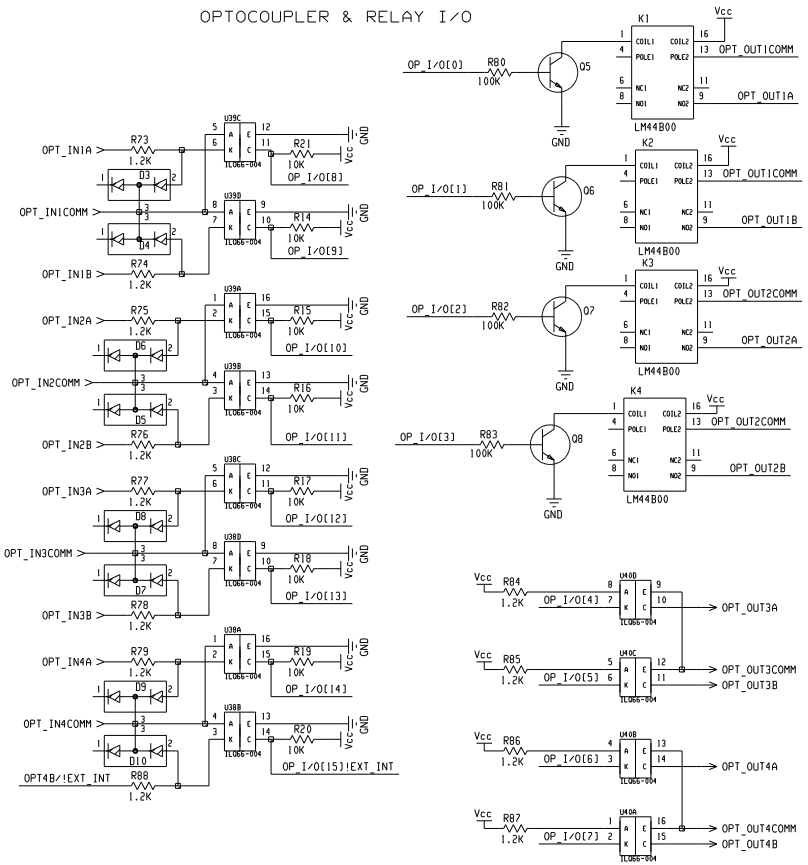


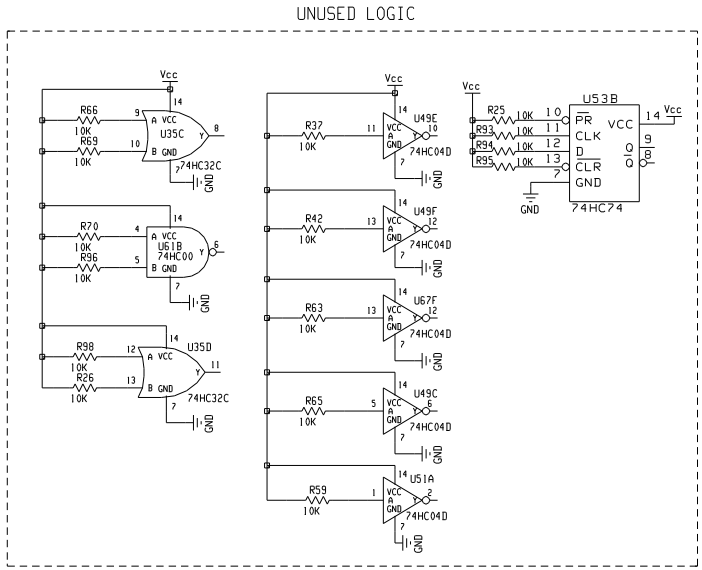
(19D903980, Sh. 3, Rev. 3)

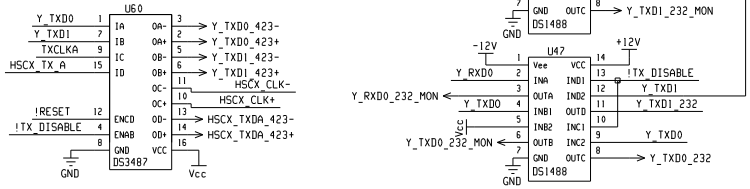


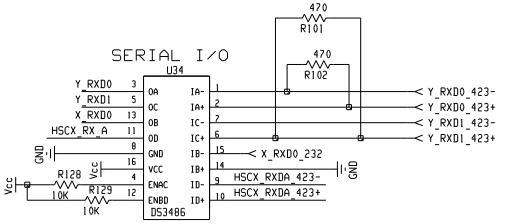
(19D903980, Sh. 4, Rev. 0)

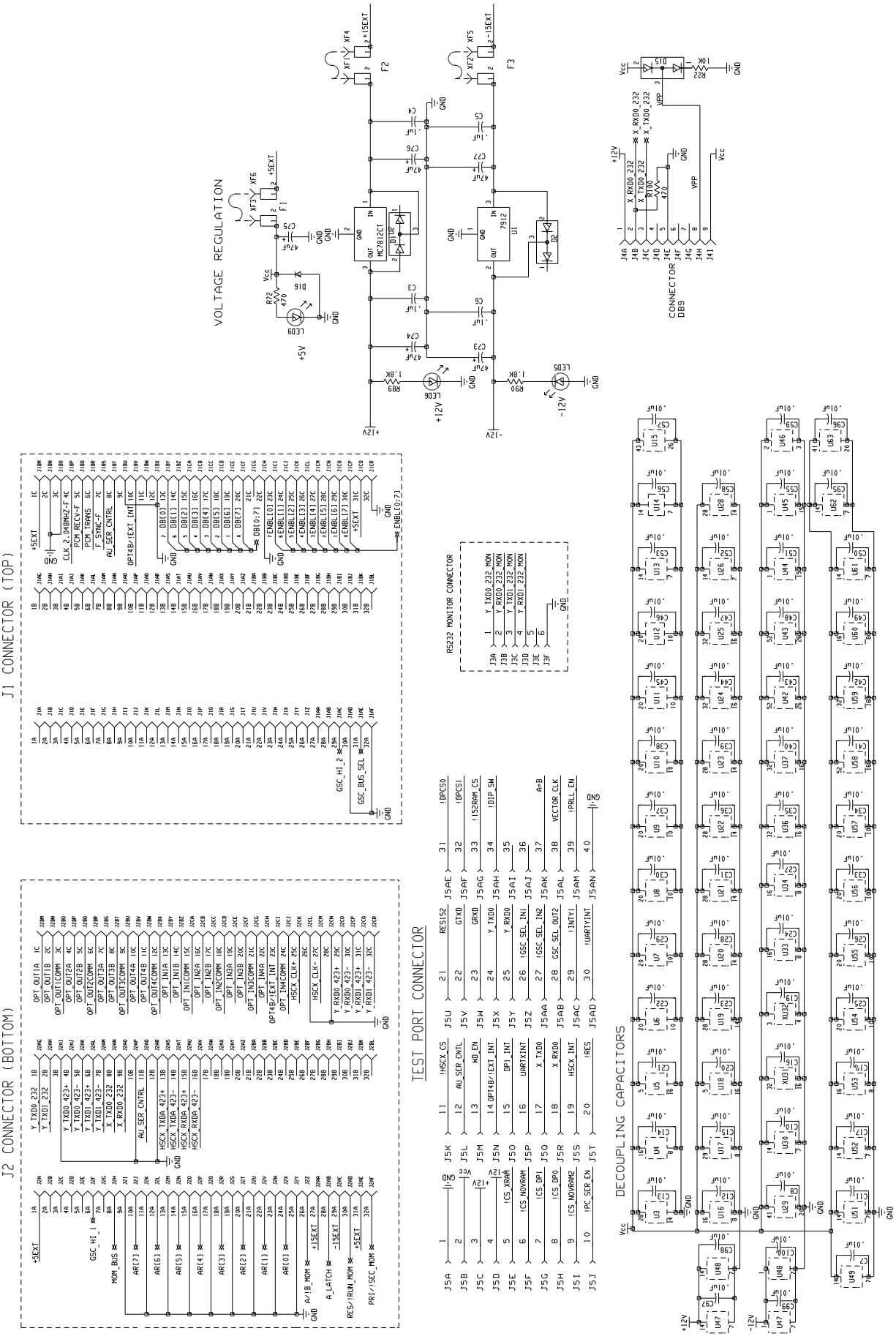
ADDENDUM NO. 1 TO LBI-38667A










J2 CONNECTOR (BOTTOM)
J1 CONNECTOR (TOP)
TEST PORT CONNECTOR
RS232 MONITOR CONNECTOR
VOLTAGE REGULATION
DECOUPLING CAPACITORS
CONNECTOR DB9
MOM_BUS
AR[7]
AR[6]
AR[5]
AR[4]
AR[3]
AR[2]
AR[1]
AR[0]
A_LATCH
RES/!RUN_MOM
PRI/!SEC_MOM
A/!B_MOM
+5EXT
-15EXT
+15EXT
GSC_H1_2
GSC_BUS_SEL
Y_TXD0_232
Y_TXD1_232
Y_TXD0_423+
Y_TXD0_423-
Y_TXD1_423+
Y_TXD1_423-
X_TXD0_232
X_RXD0_232
AU_SER_CNTRL
HSCX_TXD0_423+
HSCX_TXD0_423-
HSCX_RXD0_423+
HSCX_RXD0_423-
HSCX_CLK+
HSCX_CLK-
Y_RXD0_423+
Y_RXD0_423-
Y_RXD1_423+
Y_RXD1_423-
OPT_OUT1A
OPT_OUT1B
OPT_OUT1COMM
OPT_OUT2A
OPT_OUT2B
OPT_OUT2COMM
OPT_OUT3A
OPT_OUT3B
OPT_OUT3COMM
OPT_OUT4A
OPT_OUT4B
OPT_OUT4COMM
OPT_IN1A
OPT_IN1B
OPT_IN1COMM
OPT_IN2A
OPT_IN2B
OPT_IN2COMM
OPT_IN3A
OPT_IN3B
OPT_IN3COMM
OPT_IN4A
OPT_IN4B
OPT_IN4COMM
CLK 2.048MHZ-F
PCM RECV-F
PCM TRANS
F SYNC-F
AU_SER_CNTRL
OPT4B/!EXT_INT
DB[0:7]
ENBL[0:7]
!HSCX_CS
AU_SER_CNTL
WD_EN
OPT4B/!EXT_INT
DPI_INT
UARTXINT
X_TXD0
X_RXD0
HSCX_INT
!RES
!HSCX_CS
!DPCS0
!DPCS1
!1528RAM_CS
!DIP_SW
Y_TXD0
Y_RXD0
!GSC_SEL_IN1
!GSC_SEL_IN2
GSC_SEL_OUT2
!INTY1
!UARTYINT
A+B
VECTOR_CLK
!PRLL_EN
!CS_XRAM
!CS_NOVRAM
!CS_DPI
!CS_DPO
!CS_NOVRAM2
!PC_SER_EN
RS232 MONITOR CONNECTOR
Y_TXD0 232 MON
Y_RXD0 232 MON
Y_TXD1 232 MON
Y_RXD1 232 MON
+12V
-12V
+5V
Vcc
GND
VPP
X_RXD0 232
X_TXD0 232

CONTROLLER BOARD
19D903299P3 Rev. D
(344A4087G1 - G3)

SYMBOL	PART NUMBER	DESCRIPTION
		---------- CAPACITORS----------
C2 thru C6	19A702052P26	Ceramic: 0.1uF ±10%, 50 VDCW.
C7 and C8	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C9 *	19A700233P9	Ceramic: 2200 pF ±20%, 50 VDCW.
C10 thru C31	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C33 thru C53	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C55 thru C59	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C60 and C61	19A705205P12	Tantalum: .33 uF, 16 VDCW; sim to Sprague 293D.
C62 and C63	19A702061P49	Ceramic: 56 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C64 thru C70	19A702061P33	Ceramic: 27 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C71	19A702052P1	Ceramic: 220 pF ±10%, 50 VDCW.
C72	19A702061P25	Ceramic: 18 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C73 thru C77	19A703314P4	Electrolytic: 47 uF -10+50%, 16 VDCW; sim to Panasonic LS Series.
C78	19A702052P26	Ceramic: 0.1uF ±10%, 50 VDCW.
C79 thru C94	19A702061P61	Ceramic: 100 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C95 thru C100	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
		---------- DIODES ----------
D1 thru D12	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99.
D15	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99.
D16	T324ADP1041	Silicon: Rectifier; sim to 1N4004.
		---------- FUSES ----------
F1	19A134961P20	Cartridge: 2.0 Amps Slow-Action; sim to Littelfuse 218 002.
F2 and F3	19A134961P10	Cartridge: 0.5 Amp Slow-Action; sim to Littelfuse 218.500.
		---------- JACKS ----------
J1 * and J2 *	19B801587P13	DIN plug: 96-Position; sim to AMP 2-534068-8.
J3	19J706197P3	Connector: 8 contacts; sim to AMP 520251-4.
J4	19B209727P37	Connector, plug: 9 contacts, sim to AMP 745781-4.
J5	19B802174P2	DIN receptacle: 40-Position; sim to AMP 5-175474-5.

SYMBOL	PART NUMBER	DESCRIPTION
		---------- RELAYS ----------
K1 thru K4	19B235621P1	Reed: 2 Form C contacts; sim to GI Clare HGZM2-C05.
		---------- INDUCTORS ----------
L1	19A700021P28	Coil, Fixed: 8.2 uH.
		---------- INDICATORS ----------
LED1	19A703595P9	Optoelectric: Green LED; sim to HLMP-1540-010
LED4 thru LED6	19A703595P9	Optoelectric: Green LED; sim to HLMP-1540-010
LED8 and LED9	19A703595P9	Optoelectric: Green LED; sim to HLMP-1540-010
LED12	19A703595P9	Optoelectric: Green LED; sim to HLMP-1540-010
		---------- TRANSISTORS----------
Q1 thru Q4	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q5 thru Q8	344A3104P2	Silicon, NPN: Darlington; sim to MMBTA13LT1.
		---------- RESISTORS----------
R1 and R2	19A702931P401	Metal film: 100K ohms ±1%, 1/8 w.
R5 thru R37	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R38 *	19A702931P401	Metal film: 100K ohms ±1%, 1/8 w.
R39 thru R63	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R64	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R65 and R66	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R67 and R68	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R69 and R70	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R71 and R72	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R73 thru R79	19B800607P122	Metal film: 1.2K ohms ±5%, 1/8 w.
R80 thru R83	19A702931P401	Metal film: 100K ohms ±1%, 1/8 w.
R84 thru R88	19B800607P122	Metal film: 1.2K ohms ±5%, 1/8 w.
R89 and R90	19B800607P182	Metal film: 1.8K ohms ±5%, 1/8 w.
R91	19B800607P332	Metal film: 3.3K ohms ±5%, 1/8 w.
R92	19B800607P683	Metal film: 68K ohms ±5%, 1/8 w.
R93 thru R96	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R97	19B800607P273	Metal film: 27K ohms ±5%, 1/8 w.

SYMBOL	PART NUMBER	DESCRIPTION
R98	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R99	19B800607P273	Metal film: 27K ohms ±5%, 1/8 w.
R100 thru R102	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R103 and R104	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R105 and R106	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R108	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R109 thru R124	19B800607P510	Metal film: 51 ohms ±5%, 1/8 w.
R125	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R126	19B800607P122	Metal film: 1.2K ohms ±5%, 1/8 w.
R127	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R128 and R129	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R130 and R131	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R132 thru R137	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R138 and R139	3R151P103J	Composition: 10K ohms ±5%, 1/8 w.
		----------SWITCHES----------
SW1 and SW2	19A149955P1	DIP, Rocker: 8-Position; sim to Grayhill 76PSB08S.
SW3	19A149923P2	Pushbutton: Single-Pole Normally-Open; sim to ITT Schadow KSLOV311.
		---------- TEST POINTS----------
TP13 and TP14	344A3367P1	Metal loop w/orange insulator.
TP16	344A3367P1	Metal loop w/orange insulator.
TP20	344A3367P1	Metal loop w/orange insulator.
TP22 thru TP24	344A3367P1	Metal loop w/orange insulator.
TP27	344A3367P1	Metal loop w/orange insulator.
TP29 thru TP35	344A3367P1	Metal loop w/orange insulator.
TP41 and TP42	344A3367P1	Metal loop w/orange insulator.
TP47	344A3367P1	Metal loop w/orange insulator.
TP51 and TP52	344A3367P1	Metal loop w/orange insulator.
TP56 and TP57	344A3367P1	Metal loop w/orange insulator.
TP68 and TP69	344A3367P1	Metal loop w/orange insulator.
TP71	344A3367P1	Metal loop w/orange insulator.
TP74	344A3367P1	Metal loop w/orange insulator.
TP77	344A3367P1	Metal loop w/orange insulator.

SYMBOL	PART NUMBER	DESCRIPTION
		----------INTEGRATED CIRCUITS----------
U1	19A134718P2	Linear: -12 Volt Regulator; sim to uA7912U.
U2	19A134717P2	Linear: 12 Volt Regulator; sim to MC7812CT.
U4	19A704380P321	Digital: Monostable Multivibrator; sim to 74HC123.
U5 and U6	19A149953P202	Digital: 4-Channel Bus Transceiver; sim to DS3897.
U7 thru U11	19A703471P108	Digital: Octal Tri-State Transceiver; sim to 74HC245.
U12	19A703483P318	Digital: 8-Bit Comparator; sim to 74HC688.
U13 and U14	344A3064P208	Digital: Quad 2-Input AND Gate; sim to 74HCT08.
U15	19A149880P1	Digital: 16-Bit Microprocessor; sim to 80C186.
U16	19A703471P321	Digital: Dual 1-of-4 Decoder; sim to 74HC139A.
U17	19A705991P101	Digital: Programmable interface; sim to Harris C82C55A.
U18	19A149953P201	Digital: 8-Channel Bus Transceiver; sim to DS3896.
U19	344A3172G4	PAL (Programmed).
U20 thru U23	19A705981P2	Digital: 32K x 8-Bit Static RAM; sim to HM62256-12.
U24 and U25	344A3067P1	Digital: 128K x 8-Bit Nonvolatile RAM; sim to DS1245Y-120.
U26	19A703483P303	Digital: 8-Input OR/NOR Gate; sim to 74HC4078A.
U28	19A705981P2	Digital: 32K x 8-Bit Static RAM; sim to HM62256-12.
U29	19A149956P1	Digital: Serial Communication Controller; sim to 82525N.
U30	19A703483P311	Digital: Quad 2-Input OR Gate; sim to 74HC32.
U33	19A149895P1	Digital: Supervisory Circuit; sim to MAXIM MAX691C.
U34	19A149929P201	Digital: Quad RS-422/423 Line Receiver; sim to DS3486.
U35	19A703483P311	Digital: Quad 2-Input OR Gate; sim to 74HC32.
U36 and U37	344A3067P1	Digital: 128K x 8-Bit Nonvolatile RAM; sim to DS1245Y-120.
U38 thru U40	344A3071P1	Linear: Quad Optocoupler; sim to Siemens ILQ66-004T.
U42 and U43	344A3766P201	Digital: 2K x 8-Bit Static DPRAM; sim to IDT71321LA70JI.
U44 and U45	344A3059P201	Digital: UART; sim to Signetics SCC2691A.
U46	19A705982P101	Microcomputer: 8-bit extended I/O; sim to INTEL 80C152JB-1.
U47 and U48	19A116704P101	Digital: Quad RS-232C Line Driver; sim to MC1488D.
U49	344A3064P207	Digital: Hex Inverter; sim to 74HCT04.
U51	344A3064P207	Digital: Hex Inverter; sim to 74HCT04.

SYMBOL	PART NUMBER	DESCRIPTION
U52 and U53	344A3064P209	Digital: Dual Data Flip-Flop; sim to 74HCT74.
U54 thru U57	19A703471P318	Digital: Octal Tri-State Transceiver/Latch; sim to 74HC573.
U60	19A149930P201	Digital: Quad RS-422 Line Driver; sim to DS3487
U61	344A3064P206	Digital: Quad 2-Input NAND Gate; sim to 74HCT00
U62	19A703483P311	Digital: Quad 2-Input OR Gate; sim to 74HC32.
U63	19A149956P1	Digital: Serial Communication Controller; sim to 82525N.
U67	19A703483P104	Digital: CMOS Hex Inverter; sim to 74HC04.
		----------FUSE SOCKETS----------
XF1 thru XF6	19A116688P2	Clip, Fuse: sim to Littelfuse 111501.
		---------- SOCKETS ----------
XU3	19A700156P3	Socket, IC: 28 Pins, Tin Plated.
XU15	344A3339P5	Socket, IC: PLCC surface mount: 68-Pin; sim to AMP 822070-4.
XU19	344A3339P2	Socket, IC: PLCC surface mount: 28-Pin; sim to AMP 822066-4.
XU24 and XU25	19A700156P17	Socket, IC: 32-Pin Low-Profile; sim to AMP 2-644018-3.
XU31 and XU32	19A700156P17	Socket, IC: 32-Pin Low-Profile; sim to AMP 2-644018-3.
XU36 and XU37	19A700156P17	Socket, IC: 32-Pin Low-Profile; sim to AMP 2-644018-3.
XU46	344A3339P5	Socket, IC: PLCC surface mount: 68-Pin; sim to AMP 822070-4.
XU58 and XU59	19A700156P17	Socket, IC: 32-Pin Low-Profile; sim to AMP 2-644018-3.
		---------- CRYSTALS ----------
Y1	19A702511G37	14.7456 MHz.
Y2	19A702511G5	11.520000 MHz.
Y3 and Y4	19A702511G9	3.6864 MHz.
Y5	19A702511G45	25 MHz.
		----------MISCELLANEOUS----------
7	19C852128P2	Panel, Front.
8	344A4192	Hardware, Front Panel Mounting Kit.

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter" which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

Rev. A **Controller Board 19D903299P3**
To improve operation, changed resistor R38 from 10K ohms (19B800607P103) to 100K ohms (19B702931P401).

Rev. B **Controller Board 19D903299P3**
To improve operation, added 2200 pF capacitor C9 (19A700233P9) between U35 pin 6 and ground.

Rev. C **Controller Board 19D903299P3**
To improve operation during Controller Board live insertion procedures, changed 96-pin DIN connectors J1 and J2 from standard-type connectors (19B801587P4) to connectors with extended power pins (19B801587P13).

Rev. D **Controller Board 19D903299P3**
To improve redundant MIM operation, removed capacitor C1 and resistors R3, R4 & R107. Also disconnected U6 pin 11 from ground and connected it to U6 pin 10. In addition, connected U18 pin 10 and U12 pin 1 to RES152. (All changes on schematic diagram sheet 3.)