MAINTENANCE MANUAL
MULTISITE COORDINATOR II
CLOCK BOARD
19D903305P1

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SPECIFICATIONS

Input Voltage	+ 5 Vdc
Clock Frequencies:	
BCLK	2048 KHz
SSYNC	512 KHz
FSYNC	8 KHz
2175 Hz	2175 Hz

DESCRIPTION

Multisite Coordinator II Clock Board 19D903305P1 provides two sets of clocking signals for the **T**imed-**D**ivision-**M**ultiplexed **(TDM)** circuits. Each set of clocking signals consist of a 2.048 MHz master bit clock **(BCLK)**, a sample sync pulse for every eight bit clocks **(SSYNC)**, a frame sync pulse for every 256 bit clocks **(FSYNC)** and a 2175 Hz clock remote keying applications. The BCLK and the 2175 Hz signals have fifty percent (50%) duty cycles. The SSYNC is high for one BCLK pulse and the FSYNC is high between two BCLK leading edges.

The clocks are output to the backplane through Futurebus transmitters. The transmitters are controlled by front panel switch SW100/SW200.

CIRCUIT ANALYSIS

The Clock Board consists of two identical clocking circuits. On the Outline and Schematic Diagrams, one circuit is designated by the 100 series of numbers (U100). The other clocking circuit is designated by the 200 series of numbers (U200). The Block Diagram of Figure 1 shows both circuits as one and components are designated U100/U200, LED100/LED200, F100/F200, etc. The same component designation is used in the following text. Components which do not follow this designation are LED301, LED400, TP300, TP301, TP400 and TP401.

ERICSSON

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Private Radio Systems
Mountain View Road
Lynchburg, Virginia 24502
1-800-528-7711 (Outside USA, 804-528-7711)

Printed in U.S.A.

POWER CIRCUITS

Power to the Clock Board is provided by the **+5EXT** input. This + 5 Vdc input is fused by 0.5 Amp fuse F100/F200. When the +5 Vdc is present on the Clock Board LED400 (labeled **PWR A**) is illuminated for the clocking circuit with the 100 series number designations. LED301 (labeled **PWR B**) is illuminated for the clocking circuit with the 200 series number designations.

The input voltage (Vcc2) for the **PWR A** circuit is measured between TP400 (ground) and TP401 (+ 5 Vdc). The input voltage (Vcc1) for the **PWR B** is measured between TP300 (ground) and TP301 (+5 Vdc).

DECOUPLING

Decoupling for the **PWR A** circuit is provided by 0.1 µF capacitors C200 through C205. Additional filtering is provided by 100 µF capacitor C207. Decoupling for the **PWR B** circuit is provided by 0.1 µF capacitors C100 through C105. Additional filtering for this circuit is provided by 100 µF capacitor C107.

CLOCKING CIRCUIT

Crystal Oscillator circuit U102/U202 (14LS321N) along with 8.192 MHz crystal Y100/Y200 provides the initial clock frequency (refer to Figure 1 Block Diagram). This clock is applied to the inputs of 4-bit ripple counter U103B/U203B (74HC393-2) and 12-stage binary counter U104/U204 (74HC4040). The outputs from U103B/U203B and U104/U204 are applied to inputs of programmable logic array U105/U205 (AMPAL22V10AJC).

Another clock generated by U103B/U203B is applied to the clock input of 4-bit ripple counter U103A/U203A (74HC393-2) and U105/U205. The outputs of U103A/203A are also applied to inputs of U105/U205.

The outputs of U105/U205 are as follows:

Pin	Clock	Test Point	Frequency
18	BCLK	TP101/TP201	2048 kHz
19	SSYNC	TP102/TP202	256 kHz
20	FSYNC	TP103/TP203	8 kHz

These outputs are connected to the inputs of futurebus transceivers U100/U200 (SN75ALS056), Pins 2, 3 and 4 respectively. An additional output T1/T2 (4.350 KHz) is connected from U105/U205, Pin 21 to the input of flip-flop U101A/U201A, Pin 3 (74HC74). The output of U101A/U201A **(TONE 2175)** also connects to an input of U100/U200, Pin 1. The output of U101/U201 is read at TP100/TP200 (2175 Hz).

The outputs from futurebus transceivers U100 connect to top connector J1, terminals 1B, 3B, 5B and 7B (Output B). The outputs from futurebus transceivers U200 connect to the bottom connector J2, terminals 25B, 27B, 29B and 31B (Output A).

Futurebus transceivers U100 can be turned on or off with switch SW100. Futurebus transceivers U200 can be turned on or off with switch SW200.

QUICK REFERENCE TO TROUBLESHOOTING

Test Point	Frequency
TP101/TP201	2048 kHz
TP102/TP202	256 kHz
TP103/TP203	8 kHz

Check the above Test Points for the right frequency, otherwise, replace the board.

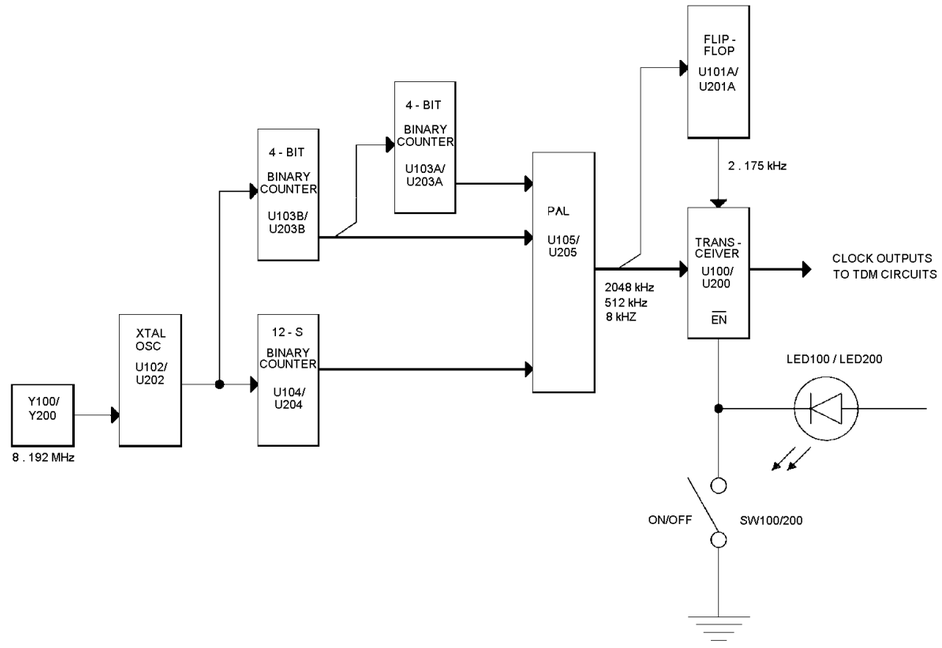
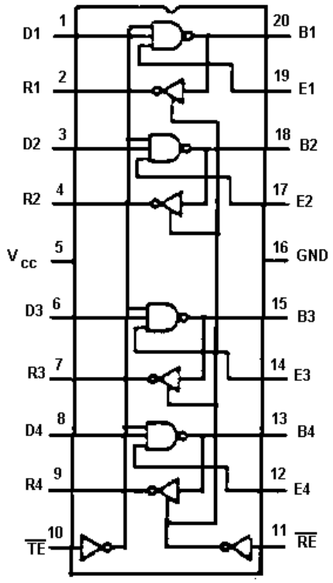
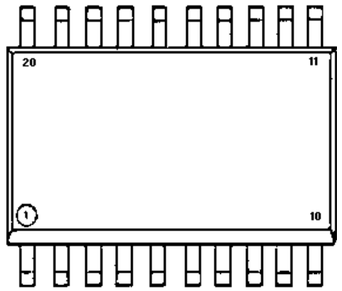


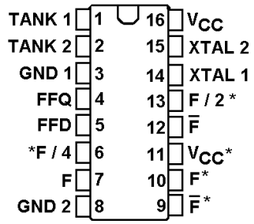
Figure 1 - Clock Board Block Diagram

TRANSCEIVER (8-CHANNEL) U100/U200
19A149953P201 (DS3896M)

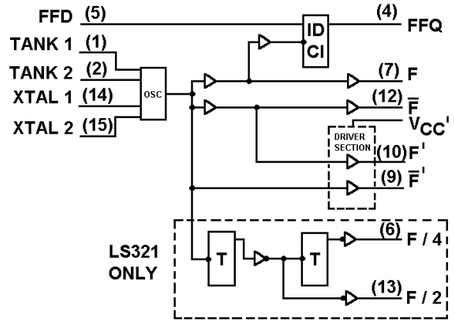




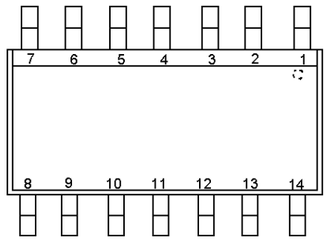
CRYSTAL OSCILLATOR U102/U202
19A700037P425 (74LS321N)

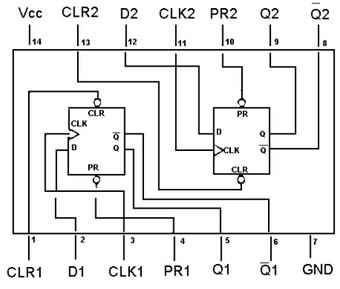


NC – No internal connection
* LS321 ONLY



DUAL D TYPE FLIP-FLOP W/SET & RESET U101/U201
19A704380P302 (74HC74D)



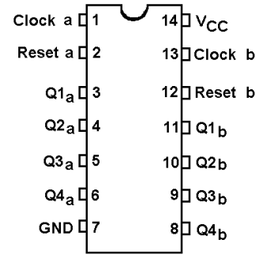


INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
K	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

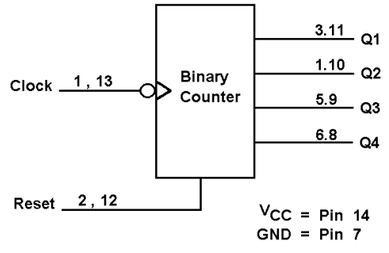
NOTE: Q0 = the level of Q before the indicated inout conditions were established.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

DUAL 4-BIT BINARY RIPPLE COUNTER U102/203
19A703987P114 (74HC939N)

PIN ASSIGNMENT



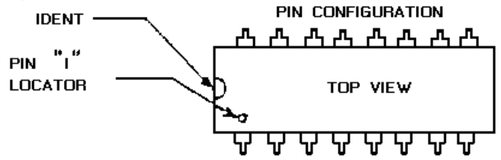
BLOCK DIAGRAM

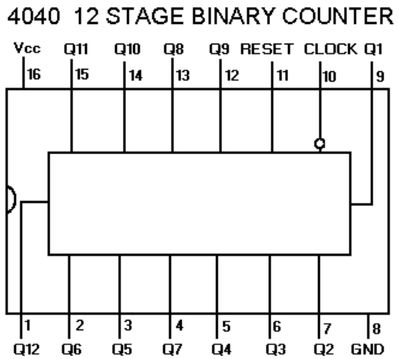


FUNCTION TABLE

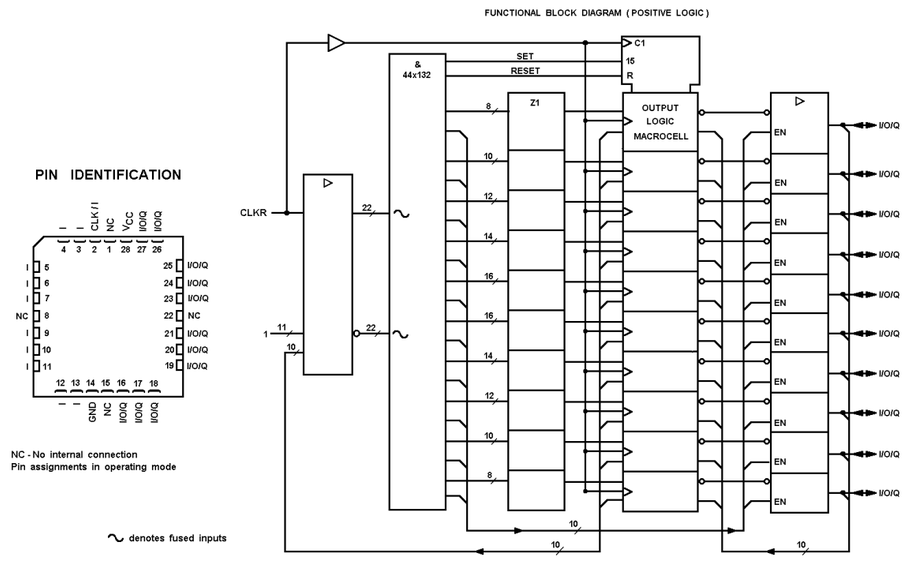
Clock	Reset	Outputs
X	H	L
H	L	No Change
L	L	No Change
↑	L	No Change
↓	L	Advance to Next State

12-STAGE BINARY COUNTER U104/U204
19A703987P301 (74C4040N)





PROGRAMMABLE ARRAY LOGIC U105/U205
344A3693G1/344A3137P1 (PALC22V10AJC)



CLOCK BOARD
19D903305P1
(344A3517, Rev. 1)

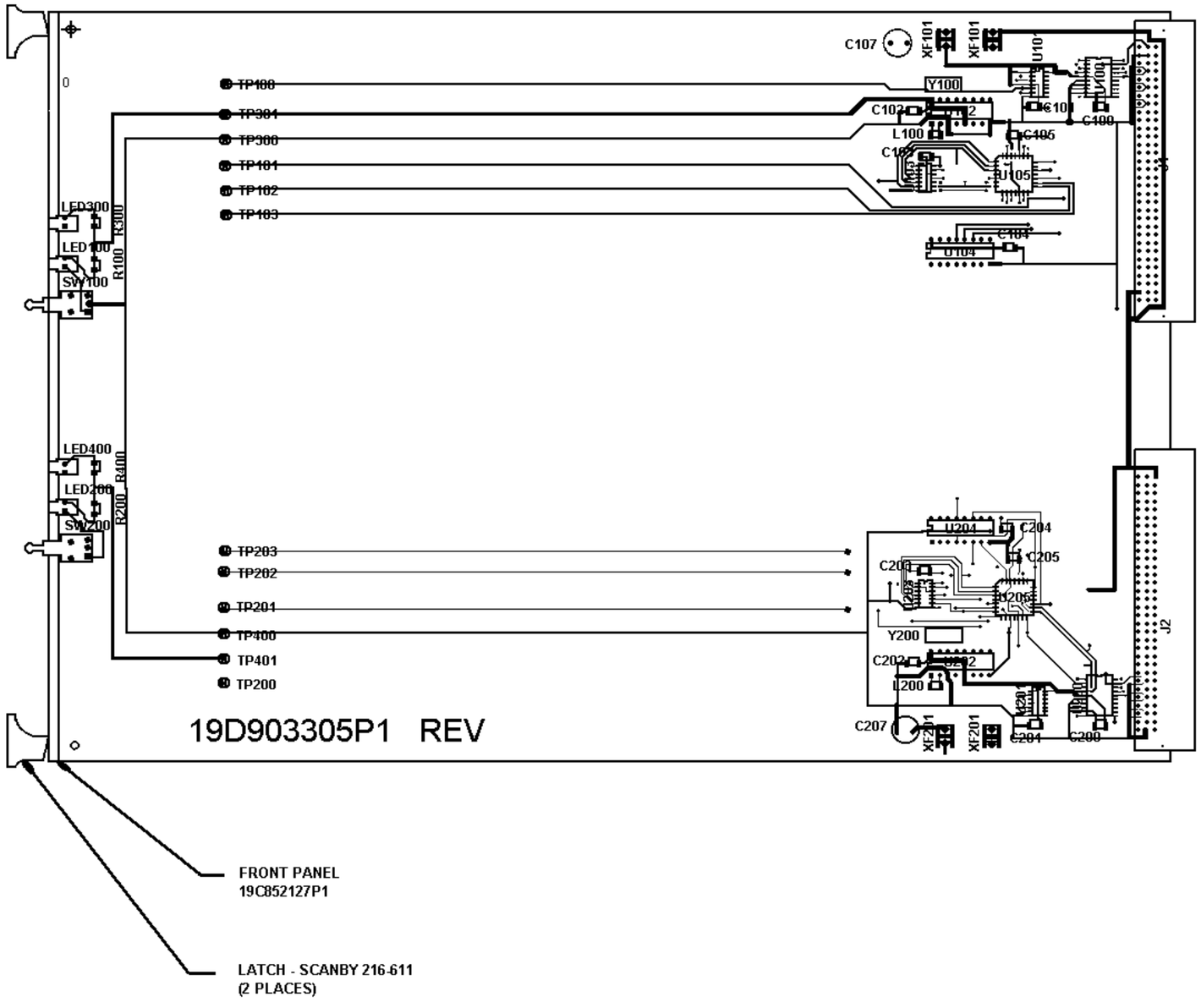
SYMBOL	PART NO.	DESCRIPTION	
		-------CAPACITORS-------	
C100 thru C106	19A702052P26	Chip: .1µF	
C107	19A703314P12	Leaded: µ100 F	
C200 thru C205	19A702052P26	Chip: .1µF	
C207	19A703314P12	Leaded: 100 µF	
		---------- FUSE ----------	
F100 and F200	19A134961P10	Fuse: 0.5 Amp	
		----------CONNECTORS----------	
J1 and J2	19B801587P4	Connector: 96 Pin	
		---------- INDUCTORS ----------	
L100 and L200	19A705470P52	Chip: 180 µH	
		---------- LED's----------	
LED100 LED200 LED300 LED400	19A703595P10	LED	
		---------- RESISTORS ----------	
R100 R200 R300 and R400	19A702931P230	Chip: Resistor 2000 Ohms 5%	
		----------SWITCHES----------	
S100 and S200	19A705959P3	Switch	
		---------- TEST POINTS ----------	
TP100 thru TP103 TP200 thru TP203 TP300 TP301 TP400 and TP401	344A3367P1	Test Point	
		------INTEGRATED CIRCUITS------	
U100	19A149953P210	Transceiver	DS3896M
U101	19A704380P302	Flip-Flop	74LS321N
U102	19A700037P425	Crystal Oscillator	74LS321
U103	19A703987P114	Binary Counter	74HC393N
U104	19A703987P301	High Speed Counter	74HC4040N
U105	344A3693G1	Programmable Array Logic	PALC22V10AJC
U200	19A149953P210	Transceiver	DS3896M
U201	19A704380P302	Flip-Flop	74LS321N
U202	19A700037P425	Crystal Oscillator	74LS321
U203	19A703987P114	Binary Counter	74HC393N
U204	19A703987P1	High Speed Counter	74HC4040N
U205	344A3693G1	Programmable Array Logic	PALC22V10AJC
		----------FUSE CLIPS----------	
XF101 XF102 XF201 and XF202	19A116688P2	Fuse Clip	
		----------CRYSTALS----------	
Y100 and Y200	19A702511G11	Crystal 8.192 MHz	

*COMPONENTS, ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

PRODUCTION CHANGES

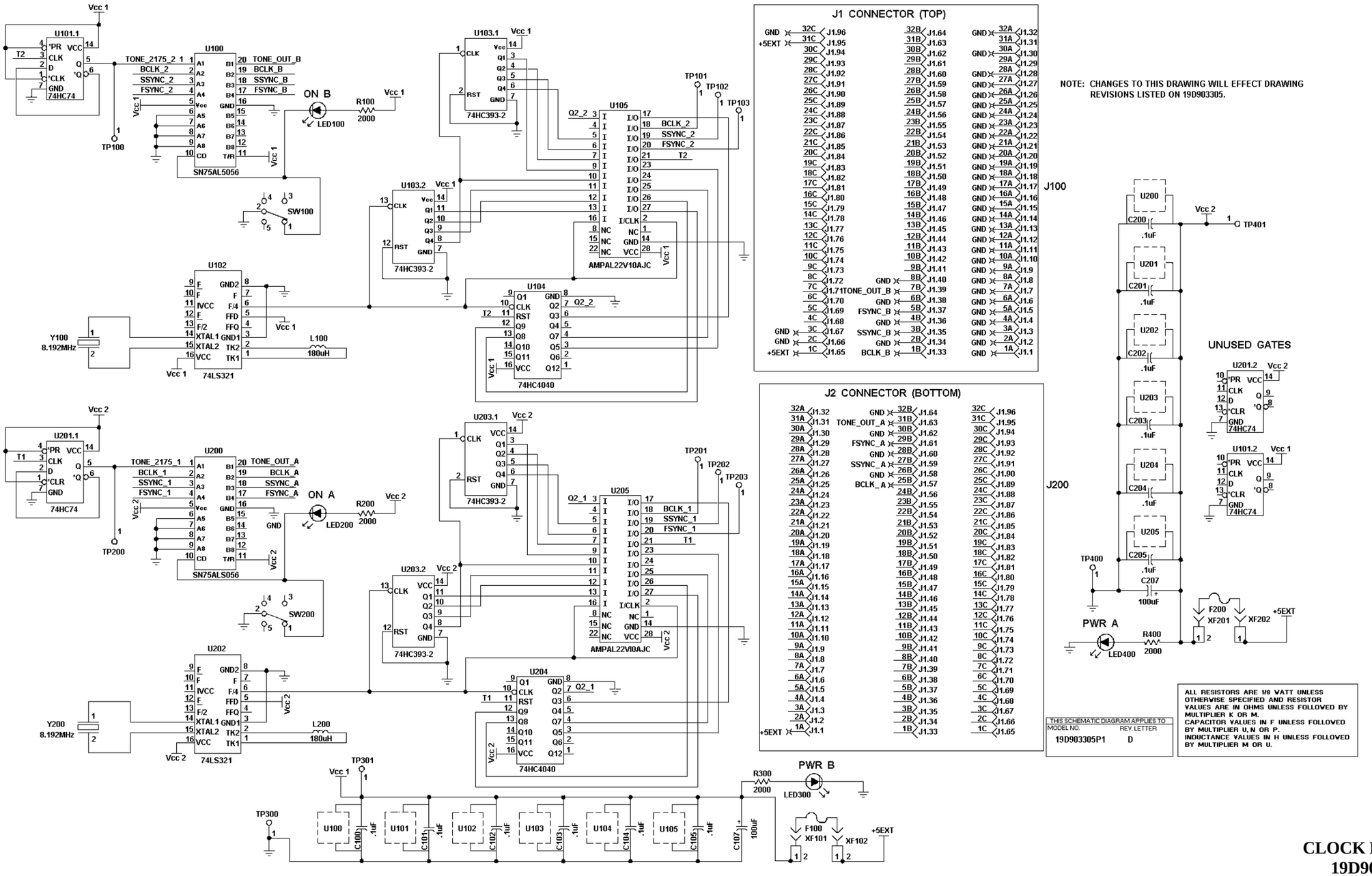
Changes in the equipment to improve or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by these revisions.

Rev. D <u>Clock Board 19D903305P1</u>
To reduce audio distortion caused by a noisy Bit Clock signal, tied the following pins on connector J1 together: J1A-01 thru J1A-28, J1A-30, J1A-32, J1B-02, J1B-04, J1B-06, J1C-02 and J1C-03. This change coincides with Terminator Board 19D903308P1 Rev. A Change.



CLOCK BOARD
19D903305P1

(19D903305, Sh. 1, Rev. 2)



CLOCK BOARD
19D903305P1

(19D903307, Rev. 2)