MAINTENANCE MANUAL
FOR
UHF RECEIVER SYNTHESIZER MODULE
19D902781G3, G7, G8, G10

TABLE OF CONTENTS

	Page
DESCRIPTION	Front Cover
GENERAL SPECIFICATIONS	1
CIRCUIT ANALYSIS	2
VOLTAGE CONTROLLED OSCILLATOR	2
FREQUENCY DOUBLER	2
RF AMPLIFIERS	2
REFERENCE OSCILLATOR AND BUFFER	2
PRESCALER AND SYNTHESIZER	2
LOOP FILTER	2
DIGITAL CONTROL	2
VOLTAGE REGULATORS	3
MAINTENANCE	3
TEST AND ALIGNMENT PROCEDURE	3
TROUBLESHOOTING	4
OUTLINE DIAGRAM	5
PARTS LIST	6
PRODUCTION CHANGES	7
IC DATA	8
ASSEMBLY DIAGRAM	10
SCHEMATIC DIAGRAM	11

DESCRIPTION

The Receiver Synthesizer Module, 19D902781G3, G7, G8 or G10 provides the local oscillator signal (LO) to the Receiver Front End Module of the MASTR III base station. The module also provides the reference oscillator signal to the transmitter synthesizer.

Figure 1 is a block diagram of the Receiver Synthesizer Module. The synthesizer is connected in a phase-locked loop (PLL) configuration. The synthesizer°s output is generated by the VCO, Q1, and multiplier Q16. It°s then buffered by the Monolithic Microwave Integrated Circuit (MMIC) U2.

The logic signals from the controller (U10, U12, and U13) control the synthesizer frequency. Frequency stability is maintained by using either the internal reference oscillator Y1 or applying an external high precision reference signal to the EXT Reference Oscillator Port J4. The internal reference oscillator, Y1, is a temperature controlled crystal oscillator (TCXO) operating at 12.8 MHz. The oscillator has a stability of ±1.0 ppm over the temperature range of -30°C to +75°C.

The multiplier output is sampled by the resistive splitter and conditioned by buffer amplifier U3. It is then fed to the divide by 128/129 dual modulus prescaler U5. The divided output from the prescaler is connected to the F_{in} input of the PLL U6. Within the PLL the divided multiplier input signal F_{in} is divided again. The PLL also divides down the 12.8 MHz reference signal. Three inputs from the controller; ENABLE, CLOCK, and serial DATA program the PLL divider circuits.

ERICSSON

Ericsson Inc.
Private Radio Systems
Mountain View Road
Lynchburg,Virginia 24502
1-800-528-7711
(Outside USA, 804-528-7711)

Printed in U.S.A.

The divided reference signal and the divided multiplier signal are compared in the PLL phase detector. When the reference and multiplier signals are identical the PLL phase detector generates a constant DC output voltage. This voltage is buffered by U8 and filtered by the loop filter circuit. It is then applied to Q1 setting the VCO on frequency.

If the compared frequencies (phases) differ, an error voltage is generated which adjusts the VCO frequency. During this out-of-lock condition, the PLL also sends a Lock Detect (LD) signal to the controller and lights the FAULT LED on the front panel of the module.

Table 1 - General Specifications

ITEM	SPECIFICATION
FREQUENCY TUNING Mechanical	 424.4 MHz-451.4 MHz (G3) 446.4 MHz-472.6 MHz (G7) 401.4 MHz-421.4 MHz (G8) 470.6 MHz-490.6 MHz (G10)
Electrical Full Specifications Degraded Specifications	 2 MHz 3 MHz
Channel Spacing	6.25 kHz
FREQUENCY STABILITY	±1.5 ppm
LO POWER OUTPUT	2.0 dBm ±2 dBm
LO NOMINAL IMPEDANCE	50 ohms
PHASE NOISE @ 25 kHz Offset	 >-137 dBc/Hz
HUM AND NOISE Companion Receiver	 -55 dB
HARMONICS @ LO PORT	<-30 dBc
SWITCHING SPEED	<50 ms
CURRENT DRAIN +13.8V +12V	 <200 mA <50 mA
REFERENCE OSCILLATOR Frequency Output Power Output Impedance	 12.8 MHz ±1.5 dBm 1 dBm ±2 dBm 50 ohms
EXT. REFERENCE OSCILLATOR Frequency Power Impedance	 5.00 MHz to 17.925 MHz (must be integer divisible by the channel spacing) +10 dBm ±3 dBm into 50 ohms 50 0hms

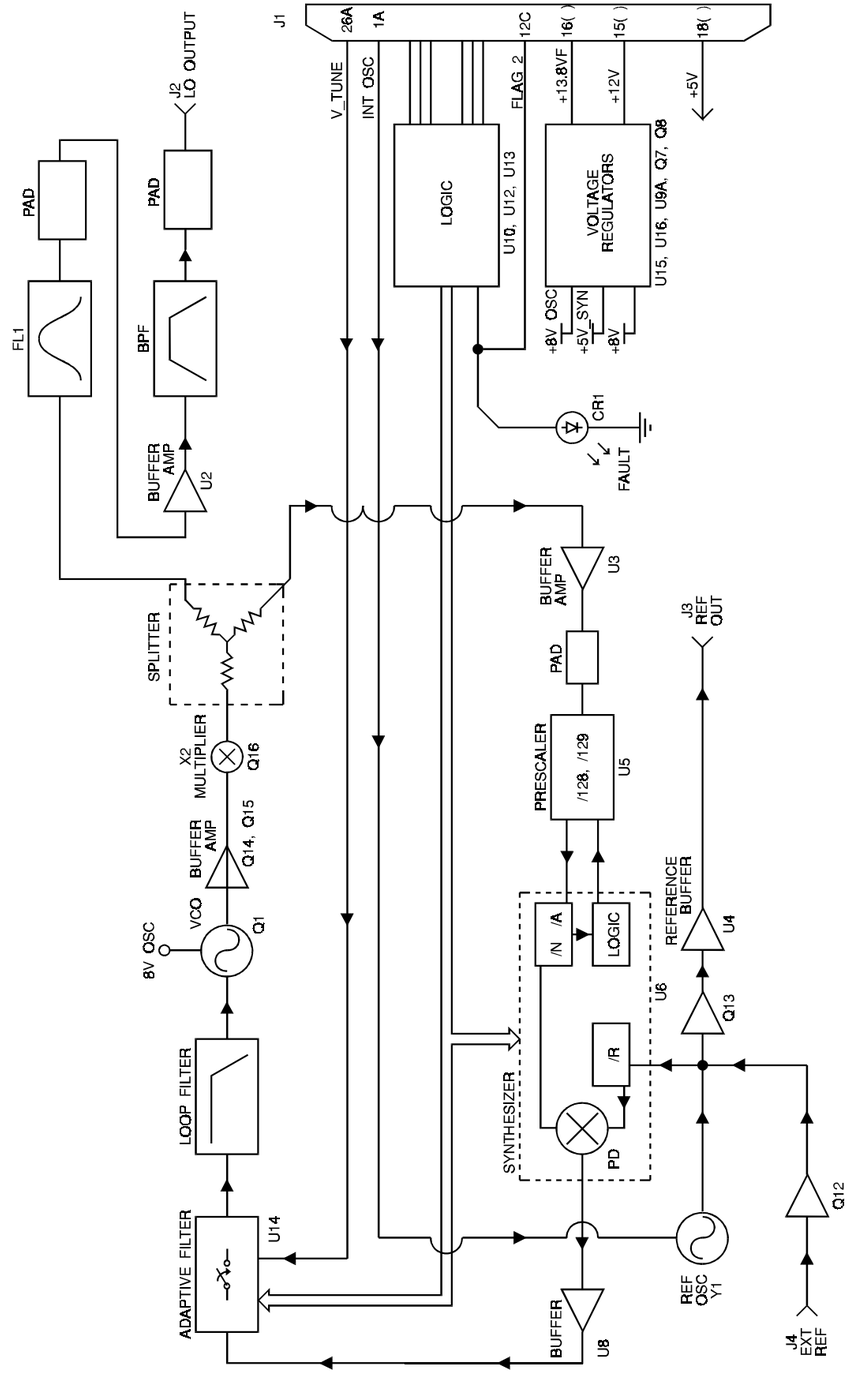


Figure 1 - Receiver Synthesizer Block Diagram

CIRCUIT ANALYSIS

The Receiver Synthesizer Module consists of the following circuits:

- Voltage Controlled Oscillator
- Multiplier (Frequency Doubler)
- Buffer Amplifiers
- Reference Oscillator and Buffer
- Prescaler and Synthesizer
- Loop Filter
- Digital Control
- Voltage Regulators

VOLTAGE CONTROLLED OSCILLATOR

The free running Voltage Controlled Oscillator (VCO) is composed of a grounded-gate JFET (Q1) and associated circuitry. Inductor L10 and associated capacitors form the resonant tank circuit. The circuit's use of high-Q components minimizes phase noise.

Frequency tuning of the VCO is done by changing the DC output voltage level from the loop filter U14. The Loop Filter Out signal from U14 is routed through L4 and R3 and applied to the two varicap diodes D4 and D5. The voltage level applied determines the diodes' capacitance and sets the resonant frequency of the oscillator. If the VCO drifts or the frequency is changed, the DC voltage level changes causing the VCO's resonant frequency to change. The output of the oscillator is then applied to a buffer amplifier. Course adjustment of frequency is done by adjusting trimmer capacitor C52 while applying a calibration voltage to the V_TUNE line connected to U14.4 pin 11.

FREQUENCY DOUBLER

Transistors Q14 and Q15 form a buffer stage to drive transistor multiplier Q16. They isolate VCO Q1 from loading effects which would degrade oscillator loaded Q and hence noise performance. Transistor multiplier Q16 is tuned to pass the second harmonic of the VCO output and hence serves as a frequency doubler. Tank elements L1, C97-C99 and L12 form a resonant circuit and matching network to drive the resistive splitter (R13, R17, R18, R96, R97, R99, R100).

RF AMPLIFIERS

The RF chain begins with a resistive splitter (R13, R17, R18, R96, R97, R99 and R100). The output of the splitter at R99 is attenuated by 7.5 dB and provides impedance matching to Helical Filter FL1 which is tuned to pass the LO Frequency while rejecting harmonics by about 40 dB. The output of FL1 is fed thru resistive pad R12, R14 and R15 to MMIC Amp U2 which operates in compression. Output Amp U2 is followed by a bandpass filter (L13-L15, C86, C87 and C101) and resistive attenuator (R30, R101 and R102). The final output at the front panel BNC connector J2 is nominally 1.5 dBm and drives the Receiver Front End LO input.

The other output at the resistive splitter at R100 is attenuated by 20 dB and drives buffer amp U3 into compression. U3 drives the synthesizer prescaler, providing a feedback signal for the synthesizer phase locked loop.

REFERENCE OSCILLATOR AND BUFFER

The reference oscillator section provides a reference signal to the PLL section. The circuit design allows using either an external or internal oscillator.

When using an external oscillator, the internal oscillator is disabled by placing a logic low on the INT OSC line from the T/R Shelf Interface Board. A high precision external oscillator may then be connected to the module through the external reference oscillator connector J4, EXT REF IN. J4 has a 50 ohm input impedance and is coupled to the base of Q12. Buffer Q12 conditions the signal and applies it to the synthesizer U6 via coupling capacitor C10.

The internal reference oscillator, Y1, provides a 12.8 MHz signal with a stability of ±1.0 ppm. It is enabled by applying a logic high signal on the INT OSC line. This signal turns on Q2, allowing it to conduct and apply +5 volts to pin 1 of the oscillator Y1. The 12.8 MHz output signal (Y1 pin 2) is then sent to the synthesizer via coupling capacitor C9.

The reference oscillator signal, either external or internal, is also routed to Q13 via coupling capacitor C54. The output taken from the emitter of Q13 is applied through C11 to the input of Buffer Amplifier U4. The buffered signal is coupled through C12 to a low pass filter network (C32,C33,C34, and L7) and a resistive pad (R27, R28, and R31) for isolation. The output from the resistive pad is then connected to J3, REF OUT, making the reference oscillator signal available for external use.

PRESCALER AND SYNTHESIZER IC

The integrated circuit U6 is the heart of the synthesizer. It contains the necessary frequency dividers and control circuitry to synthesize output frequencies by the technique of dual modulus prescaling. U6 also contains an analog sample and hold phase detector and a lock detector circuit.

Within U6 are three programmable dividers which are serially loaded using the CLOCK, DATA, and ENABLE inputs (pins 11, 12, and 13 respectively). A serial data stream (DATA) on pin 12 is shifted into the internal shift registers by low to high transitions on the clock input (CLOCK) at pin 11. A logic high (ENABLE) on pin 13 then transfers the program information from the shift registers to the divider latches. The serial data determines the VCO frequency by setting the internal R, A, and N dividers.

The 12.8 MHz reference oscillator signal OSCIN is internally routed to the "R" divider. The "R" divider divides down the 12.8 MHz reference signal to a lower frequency, F_r, as directed by the input data and applies the signal to the internal analog phase and lock detectors.

The "A" and "N" dividers process the loop feedback signal from the multiplier (by way of the dual modulus prescaler U5). The output of the "N" divider, F_v, is a divided down version of the multiplier output frequency. This signal is also applied to the internal phase detector. The ramp and hold constants are determined by C26, R37, C31, and R36.

The analog phase detector output voltage (PD OUT) is proportional to the phase difference between F_v and F_r. This output serves as the loop error signal. When operating on the correct frequency, the inputs to the phase detector are identical and the output voltage of the analog phase detector is constant. If the compared frequencies (phases) differ, the analog phase detector increases or decreases the DC output voltage (PD OUT). This error signal voltage tunes the VCO to whatever frequency is required to keep F_v and F_r locked (in phase).

The lock detector furnishes the Fault circuit in U13 with the lock detect (LD) signal. When F_v and F_r are in phase, the lock detector output sends a logic high on the LD line to the fault circuit U13. If the VCO is not locked onto the correct frequency, the resulting out-of-phase condition causes the output from the lock detector to be a logic low.

LOOP FILTER

The error signal, ANOUT, is applied to the loop filter at U8.2 pin 5 and U8.1 pin 3. U8.2 acts as a buffer amplifier with gain. The output signal from the amplifier is applied to a loop filter consisting of R42, R43, R44, C35 and C36 via the bilateral switch U14. The filter removes noise and sampling frequencies from the error voltage. The switch, U14, selects the proper filter configuration for operation in the narrow band, wide band or tuning mode. The control signals (OPEN_LOOP, ENABLE_NOT, and TUNE_CTRL) for U14 are derived from the digital control circuits U10, U12, and U13. U8.1 provides a buffered output for testing at the DIN connector on the rear of the module.

DIGITAL CONTROL

Logic control circuits (other than those inside the synthesizer IC - U6) consist of the following:

- Digital Control Circuit (U10, U12, & U13)
- Level Shifters
- Fault Circuit

The Digital Control Circuits U10, U12, & U13 serve as an interface between the controller and the synthesizer IC.

As an address decoder, U10 enables the input gates when the A0, A1, and A2 input lines (pins 4, 3, and 2) receive the correct address code from the controller. For the Receiver synthesizer the enable address is 010 on A0, A1, and A2 respectively. After receiving the proper logic code, the input gate U12 is enabled. This allows the ENABLE, CLOCK, and serial DATA information to pass on to the synthesizer via the level shifters.

The Level Shifters Q3, Q4, and Q5 convert the five (5) volt logic level to the eight (8) volt logic level required by the synthesizer.

The Fault circuit, U13, monitors the lock detect signal from the PLL synthesizer. Under normal (locked) condition, the PLL sends a logic high signal to U13. U13 processes the signal and provides a logic high output which saturates Q6. Saturating Q6 turns off the FAULT LED (CR1). U13 also sends a logic high signal, FLAG 2, (U13.3 pin 8) to the controller indicating the VCO's frequency is correct.

When the VCO is not on the correct frequency, the synthesizer sends a logic low signal to U13. This causes U13 to cutoff Q6 which turns on the FAULT LED (CR1). U13 also sends a logic low signal to the controller, on the FLAG 2 line, indicating the VCO's frequency is incorrect.

VOLTAGE REGULATORS

Voltage regulators U15 and U16 reduce the +13.8 VF line to +5 Vdc and +8 Vdc respectively. The output from U15 (+5V_SYN) is used by both the synthesizer and logic circuitry while the 8 Vdc output from U16 is used for the op-amps, level shifters, and the discrete +8V OSC regulator circuit.

The discrete +8V OSC regulator circuit is a linear regulator consisting of U9A, Q7, Q8, and associated circuitry. The error amplifier U9A controls Q7 and pass element Q8. The +8V OSC is used as the power source for the VCO circuit, where additional filtering is provided to keep noise to a minimum

MAINTENANCE

RECOMMENDED TEST EQUIPMENT

The following test equipment is required to test the Synthesizer Module:

1. Modulation Analyzer; HP 8901A, or equivalent
2. Power Supply; 12.0 Vdc @ 500 mA
3. Frequency Counter; 10 MHz - 250 MHz
4. Power Meter; -20 dBm to +10 dBm
5. Spectrum Analyzer, 0 - 1 GHz

SERVICE NOTES

The following service information applies when aligning, testing, or troubleshooting the RX Synthesizer:

- Logic Levels:
  Logic 1 = high = 4.5 to 5.5 Vdc
  Logic 0 = Low = 0 to 0.5 Vdc

- Receiver Synthesizer Address = A0 A1 A2 = 010

- Synthesizer data input stream is as follows:
  14-bit "R" divider most significant bit (MSB) = R13 through "R" divider least significant (LSB) = R0

  10-bit "N" divider MSB = N9 through "N" divider LSB = N0

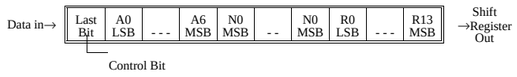
  7-bit "A" divider MSB = A6 through "A" divider LSB = A0

  Single high Control bit (last bit)

  Latched When Control Bit = 1

DATA ENTRY FORMAT

Latched When
Control Bit = 1



- Synthesizer lock is indicted by the extinguishing of the front panel LED indicator and a logic high on the fault FLAG 2 line (J1 pin 12C).
- Always verify synthesizer lock after each new data loading.

TEST AND ALIGNMENT

INITIALIZATION

Apply +12 Vdc to the test fixture.

Current Consumption

Measure the current through pins 15A, 15B, 15C, 16A, 16B, AND 16C.

Verify the current is less than 250 mA. Total current is the +13.8 VF current and +12 Vdc current combined.

Reference Oscillator

Adjust Y1 for an output frequency of 12.8 MHz ±2 Hz. Measure the output power of the reference oscillator output (J3).

Verify the output power is 1 dBm ±2 dBm.

Oscillator Alignment

Ground the ENABLE TEST line (pin 22A). Apply +4 Vdc to the V_TUNE line (pin 26A). Measure the frequency of the free running multiplied oscillator at the LO OUT port (J2).

Adjust the trimmer capacitor C52 for 445 MHz (G3), 470 MHz (G7), 420 MHz (G8) or 490 MHz (G10) ±100 kHz.

Synthesizer Loading

Unground the ENABLE TEST line (pin 22A). Load the synthesizer IC for 445 MHz (G3) or 470 MHz (G7) or 420 MHz (G8) or 490 MHz (G10).

Verify the lock indicator (CR1) is off or the FLAG 2 line is high.

Hum and Noise

Initialize the HP 8901A for 300 Hz - 3 kHz, 750 µsec de-emphasis, average FM deviation, and 0.44 dB reference for the deviation.

Verify the hum and noise (J2) is less than -55 dB.

Output Power and Harmonic Content

Adjust both slugs on FL1 for maximum output level measured at J2.

Verify the output power (J2) at the fundamental frequency is:

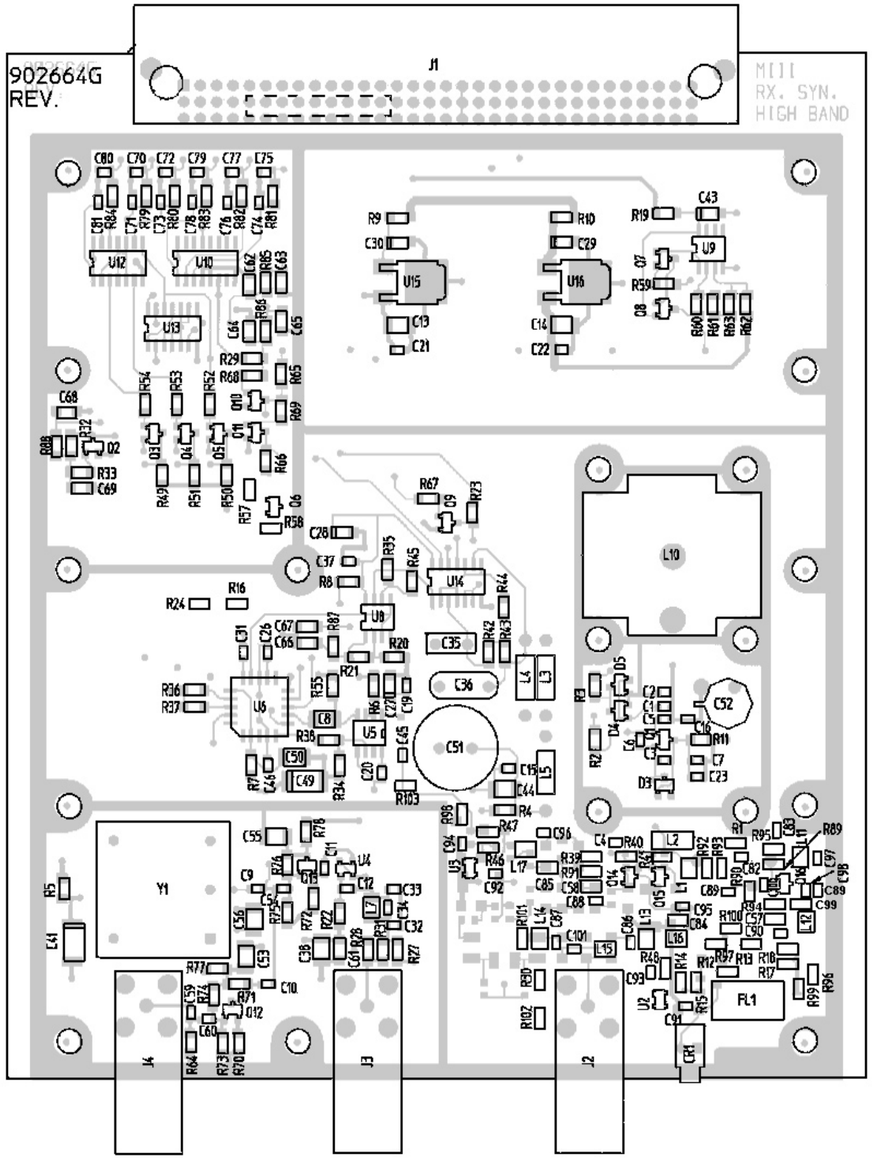
2 dBm ±2 dB

Verify the harmonic content is less than -30 dBc.

TROUBLESHOOTING CHART

SYMPTOM	AREAS TO CHECK	INDICATIONS
I. Loop Fails To Lock	1. Check for: +8 Vdc at U16-3, +5 Vdc at U15-3 +8 Vdc at Q8-C.	Bad Regulation circuitry. Troubleshooting using standard procedures.
	2. Check for 12.8 MHz reference at U6-2 and U6-3. Typical Levels: 500 mVpp @U6-2 2.5 Vpp @U6-3.	Reference Osc. Module defective or supply not present or low. Proceed to reference oscillator section II.
	3. Check for LO output @J2. F_{LO} ±5 MHz, 0 dBm nominal	LO tuning incorrect, or buffer amplifier bad. Proceed to LO tuning and power section III.
	4. Check Prescaler output @U5-4. Typically: 2-4 MHz square wave @1.25 Vpp.	If LO power is good, check for 3.2 Vdc @U2-3. Replace U2, then U5 if necessary.
	5. Check for CLOCK, DATA, and ENABLE signals at U6 pins 11, 12 and 13 respectively. (0, 8V logic levels)	Bad digital control circuitry. Troubleshoot using standard procedures. Ensure all programming signals are present at J1. (CLOCK, DATA, ENABLE, A0, A1 and A2).
	6. Check Ramp Signal @U6-15. It should be 6.25 kHz nominal.	If reference oscillator and programming signals are present for proper programming information. Last resort - replace Synthesizer IC U6.
II. Reference OSC. not present or low power.	1. Check for 4.3 Vdc supply at junction of R5 and C41.	Bad supply switch Q2 or wrong Control Signal Internal Osc. Troubleshooting using standard procedures. Replace Y1 as last resort.
	2. Check 12.8 MHz signal @Q13-E. Should be approx. 350 mVpp.	Bad buffer amplifier Q13. Troubleshoot using standard procedures.
III. LO power low or tuned out of band.	1. Check tuning with 6 Vdc applied using test procedure. F_{LO} ±5 MHz.	LO tuning incorrect. Retune following test procedure.
	2. Check DC bias at Buffer Amplifiers U1, U2, & U3 pin 3 Typ. 3.2 Vdc.	Bad Buffer Amplifier. Replace bad part.
IV. LO signal not present. (i.e. Q1 does not oscillate)	1. Check DC bias at Q1 drain. (Typ. +8Vdc).	Replace Q1.
	2. Check DC bias at Q1 source. (Typ. +0.9 Vdc).	

COMPONENT SIDE



LEAD IDENTIFICATION FOR Q1 (SOT) TRANSISTORS

TOP VIEW

(D) 2 — 3 (G)

(S) 1

LEAD IDENTIFICATION FOR D3 - D5 (SOT) DIODES

TOP VIEW

2 — 3

1

LEAD IDENTIFICATION FOR Q2 - Q16 (SOT) TRANSISTORS

TOP VIEW

(B) 2 — 3 (C)

(E) 1

LEAD IDENTIFICATION U2 - U4 (SOT) INT CKT

TOP VIEW

OUTPUT — GND

GND — INPUT

(19D902664, Sh. 2, Rev. 4)
(19D902665, Layer 1, Rev. 1)

UHF RECEIVER SYNTHESIZER BOARD
19D902664G3 ,G7, G8, G10

UHF RECEIVER SYNTHESIZER MODULE 19D902781G3, G7, G8, G10 ISSUE 5

SYMBOL	PART NO.	DESCRIPTION
		- - - - - - - - - MISCELLANEOUS - - - - - - - - -
3	19D902509P4	COVER.
4	19D902555P1	Handle.
6	19A702381P506	Screw, thread forming: TORX, No. M3.5-.6 x 6.
7	19A702381P513	Screw, thread forming: TORX, No. M3.5 - 0.6 X 13.
10	19D902824P1	Casting.
11	19A702381P508	Screw, thd. form: No. 3.5-0.6 x 8.
23	19B802690P1	Grommet.
		UHF RECEIVER SYNTHESIZER BOARD 19D902664G3, G7, G8, G10
		- - - - - - - - - CAPACITORS - - - - - - - - -
C1	19A702236P15	Ceramic: 3.9 pF + or -0.25 pF, 50 VDCW, temp or -30 PPM/°C. (Used in G7, G3, G10).
C1	19A702236P17	Ceramic: 4.7 pF + or -0.5 pF, 50 VDCW, temp or -60 PPM/°C. (Used in G8).
C2	19A702236P15	Ceramic: 3.9 pF + or -0.25 pF, temp coef -30 PPM/°C. (Used in G8).
C3	19A702236P38	Ceramic: 33 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C. (Used in G3).
*C3	19A702236P36	Ceramic: 27 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C. (Used in G7 and G8).
C3	19A702236P34	Ceramic: 22 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM. (Used in G10).
C4	19A702236P9	Ceramic: 1.8 pF + or -0.25 pF, 50 VDCW, temp or -30 PPM.
C5	19A702236P30	Ceramic: 15 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C. (Used in G3).
*C5	19A702236P28	Ceramic: 12 pF + or - 5%, 50 VDCW, temp coef 0 + or -30 PPM. (Used in G7, G8, G10).
C6	19A702236P36	Ceramic: 27 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C. (Used in G3).
*C6	19A702236P34	Ceramic: 22 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM. (Used in G7 and G8).
C6	19A702236P32	Ceramic: 18 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM. (Used in G10).
C7	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C8	19A702052P26	Ceramic: 0.1uF + or - 10%, 50 VDCW.
C9	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C10	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C11	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C12	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C13 and C14	19A702052P26	Ceramic: 0.1uF + or - 10%, 50 VDCW
C15	19A702052P5	Ceramic: 1000 pF + or -10%, 50 VDCW.
C16	19A702236P23	Ceramic: 8.2 pF + or -.25 pF, 50 VDCW, temp or -30 PPM. (Used in G3).
*C16	19A702236P25	Ceramic: 10 pF + or -.5 pF, 50 VDCW, temp coef -30 PPM/°C. (Used in G7 & G10).
C16	19A702236P28	Ceramic: 12 pF + or -.5 pF, 50 VDCW, temp coef -30 PPM/°C. (Used in G8).
C19	19A702052P3	Ceramic: 470 pF + or - 10%, 50 VDCW.
C20	19A702052P3	Ceramic: 470 pF + or - 10%, 50 VDCW.
C21	19A702052P3	Ceramic: 470 pF + or - 10%, 50 VDCW.
C22	19A702052P3	Ceramic: 470 pF + or - 10%, 50 VDCW.
C23	19A702052P5	Ceramic: 1000 pF + or -10%, 50 VDCW.
C26	19A702052P8	Ceramic: 3300 pF + or - 10%, 50 VDCW.
C27	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C28	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C29	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C30	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C31	19A702052P1	Ceramic: 220 pF + or - 10%, 50 VDCW.
C32	19A702052P1	Ceramic: 220 pF + or - 10%, 50 VDCW.
C33	19A702052P1	Ceramic: 220 pF + or - 10%, 50 VDCW.
C34	19A702236P43	Ceramic: 51 pF + or - 5%, 50 VDCW, temp coef - 30 PPM/°C.
C35	19A703684P1	Metallized Polyester: 0.47 uF + or -10%, 63 v.
C36	19A703902P3	Metal: 0.047 uF + or -10%, 50 VDCW.
C37	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C38	19A702052P26	Ceramic: 0.1uF + or - 10%, 50 VDCW
C43	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C44	19A702052P26	Ceramic: 0.1uF + or - 10%, 50 VDCW.
C45	19A702052P3	Ceramic: 470 pF + or - 10%, 50 VDCW.
C46	19A702052P3	Ceramic: 470 pF + or - 10%, 50 VDCW.
C49	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C50	19A702052P26	Ceramic: 0.1uF + or - 10%, 50 VDCW.
C51	19A701225P3	Electrolytic: 220 uF, -10+50%, 25 VDCW.
C52	19A134227P5	Variable: 1.5 to 14 pF, 100 VDCW. (Used in G40, G3 and G8).
C53	19A702052P26	Ceramic: 0.1uF + or - 10%, 50 VDCW.
C54	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C55	19A702052P26	Ceramic: 0.1uF + or - 10%, 50 VDCW.
C56	19A702052P26	Ceramic: 0.1uF + or - 10%, 50 VDCW
C57	19A702061P99	Ceramic: 1000 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C.
C58	19A702061P99	Ceramic: 1000 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C.
C59	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C60	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C61 and C62	19A702061P99	Ceramic: 1000 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C.
C63	19A702061P99	Ceramic: 1000 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C.
C64	19A702061P99	Ceramic: 1000 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C.
C65	19A702061P99	Ceramic: 1000 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C.
C66	19A702061P99	Ceramic: 1000 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C.
C67	19A702061P99	Ceramic: 1000 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C.
C68	19A702061P99	Ceramic: 1000 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C.
C69	19A702061P99	Ceramic: 1000 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C.
C70	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C71	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C72	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C73	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C74	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C75	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C76	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C77	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C78	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C79	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C80	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C81	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM. (Used in G40, G3, G7 and G8).
C82 and C83	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW. (Used in G80, G5, G40,
C84	19A702061P99	Ceramic: 1000 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C.
C85	19A702061P99	Ceramic: 1000 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C.
C86 and C87	19A702236P28	Ceramic: 12 pF + or - 5%, 50 VDCW, temp coef 0 + or -30 PPM. (Used in G80, G5, G40, G3, G7 and G8).
C88	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C89	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C90	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW. (Used in G40, G3, G7
C91	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM. (Used in G80, G5, G40, G3, G7 and G8).
C92 thru C96	19A702061P61	Ceramic: 100 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM. (Used in G40, G3, G7 and G8).
C97	19A702236P1	Ceramic: 0.5 pF + or -.l pF, 50 VDCW, temp coef -30 PPM. (Used in G3, and G7).
C97	19A702236P11	Ceramic: 2.7 pF + or -.25 (Used in G8).
C98 and C99	19A702236P30	Ceramic: 15 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C. (Used in G3, and G7).
C98 and C99	19A702236P31	Ceramic: 16 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C. (Used in G8).
C98 and C99	19A702236P28	Ceramic: 12 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C. (Used in G10).
C100	19A702236P25	Ceramic: 10 pF + or -.5 pF, 50 VDCW, temp coef -30 PPM/°C.
C101	19A702236P10	Ceramic: 2.2 pF + or -2.5 pF, 50 VDCW, temp or -30 PPM/°C.
		- - - - - - - - - - DIODES - - - - - - - - - -
CR1	19A703595P10	Optoelectic: Red LED; sim to HP HLMP-1301-010.
		- - - - - - - - - - FILTERS - - - - - - - - - -
FL1	344A3802P4	FILTER ,HEL RF (Used in G8).
FL1	344A3802P2	FILTER ,HEL RF (Used in G3).
FL1	344A3802P3	FILTER, RF: 475 MHz SIM TO TOKO SHW-44545A-475 (Used in G7, G10)
		- - - - - - - - - - JACKS - - - - - - - - - -
J1	19B801587P7	Connector, DIN: 96 male contacts, right angle to AMP 650887-1.
J2 thru J4	19A115938P24	Connector, receptacle.
		- - - - - - - - - - INDUCTORS - - - - - - - - - -
*L2	19A705470P25	Coil, fixed: .1uH; sim to Toko 380LB-1R0M.
L3 and L4	19A700024P13	Coil, RF: 1.0 uH + or -10%.
L5	19A700024P15	Coil, RF: 1.5 uH + or - 10%.
L10	19C851001P4	Coil, RF: sim to Paul Smith SK901-1.
		- - - - - - - - - - CRYSTALS - - - - - - - - -
Y1	19B801351P14	Module: Crystal Oscillator, 12.8 MHz + or -1.0 PPM.
		- - - - - - - - - - DIODES - - - - - - - - - -
D3	19A705377P1	Silicon, Hot Carrier: sim to MMB0201.
D4 and D5	19A149674P1	DIODE ,SILICON.
		- - - - - - - - - - INDUCTORS - - - - - - - - - -
L1	19A705470P2	Coil, Fixed: 12 nH; sim to Toko 380NB-12nM.
L7	19A705470P24	Coil, Fixed: 0.82 uH; sim to Toko 380NB-R82M.
L11 and L12	19A705470P2	Coil, Fixed: 12 nH; sim to Toko 380NB-12nM.
L13 and L14	19A705470P1	Coil, Fixed: 10 nH; sim to Toko 380NB-10nM.
L15	19A705470P10	Coil, fixed: 56 nH; sim to Toko 380NB-56nM.
L16 and L17	19A705470P15	Coil, fixed: .15uH; sim to Toko 380NB-R15M.
		- - - - - - - - - - TRANSISTORS - - - - - - - - -
Q1	19A702524P2	N-Type, field effect; sim to MMBFU310.
Q2	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q3 thru Q5	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q6	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q7	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q8	19A700059P2	Silicon, PNP: sim to MMBT3906, low profile.
Q9 thru Q11	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q12 and Q13	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q14 thru Q16	19A704708P2	Silicon, NPN: sim to NEC 2SC3356.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1	19B800607P680	Metal film: 68 ohms + or -5%, 1/8 w.
R2	19B800607P100	Metal film: 10 ohms + or -5%, 1/8 w. (Used in G40, G3, G7
R3	19B800607P100	Metal film: 10 ohms + or -5%, 1/8 w.
*R4	19B800607P100	Metal film: 10 ohms + or -5%, 1/8 w.
R5 thru R10	19B800607P100	Metal film: 10 ohms + or -5%, 1/8 w.
R11	19B800607P183	Metal film: 18K ohms + or -5%, 1/8 w.
R12	19B800607P271	Metal film: 270 ohms + or -5%, 1/8 w.
R13	19B800607P510	Metal film: 51 ohms + or -5%, 1/8 w.
R14	19B800607P271	Metal film: 270 ohms + or -5%, 1/8 w.
R15	19B800607P180	Metal film: 18 ohms + or -5%, 1/8 w.
R16	19B800607P392	Metal film: 3.9K ohms + or -5%, 1/8 w.

* COMPONENTS, ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

SYMBOL	PART NO.	DESCRIPTION
R17	19B800607P120	Metal film: 12 ohms + or -5%, 1/8 w.
R18	19B800607P180	Metal film: 18 ohms + or -5%, 1/8 w.
R19	19B800607P100	Metal film: 10 ohms + or -5%, 1/8 w.
R20	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R21	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.
R22	19B800607P271	Metal film: 270 ohms + or -5%, 1/8 w.
R23	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R24	19B800607P562	Metal film: 5.6K ohms + or -5%, 1/8 w.
R27	19B800607P181	Metal film: 180 ohms + or -5%, 1/8 w.
R28	19B800607P181	Metal film: 180 ohms + or -5%, 1/8 w.
R29	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R30	19B800607P560	Metal film: 56 ohms + or -5%, 1/8 w. (Used in G3, G7, G8).
R30	19B800607P680	Metal film: 68 ohms + or -5%, 1/8 w. (Used in G10).
R31	19B800607P270	Metal film: 27 ohms + or -5%, 1/8 w.
R32	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.
R33	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.
R34	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R35	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R36	19B800607P393	Metal film: 39K ohms + or -5%, 1/8 w.
R37	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R38	19B800607P682	Metal film: 6.8K ohms + or -5%, 1/8 w.
R39	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R40	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R41	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R42	19B800607P823	Metal film: 82K ohms + or -5%, 1/8 w.
R43	19B800607P333	Metal film: 33K ohms + or -5%, 1/8 w.
R44	19B800607P274	Metal film: 270K ohms + or -5%, 1/8 w.
R45	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.
R46	19B800607P181	Metal film: 180 ohms + or -5%, 1/8 w.
R47	19B800607P271	Metal film: 270 ohms + or -5%, 1/8 w.
R48	19B800607P181	Metal film: 180 ohms + or -5%, 1/8 w.
R49	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R50	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R51	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R52	19B800607P473	Metal film: 47K ohms + or -5%, 1/8 w.
R53	19B800607P473	Metal film: 47K ohms + or -5%, 1/8 w.
R54	19B800607P473	Metal film: 47K ohms + or -5%, 1/8 w.
R55	19B800607P222	Metal film: 2.2K ohms + or -5%, 1/8 w.
R57	19B800607P473	Metal film: 47K ohms + or -5%, 1/8 w.
R58	19B800607P681	Metal film: 680 ohms + or -5%, 1/8 w.
R59	19B800607P222	Metal film: 2.2K ohms + or -5%, 1/8 w.
R60	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R61	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R62	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R63	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R64	19B800607P510	Metal film: 51 ohms + or -5%, 1/8 w.
R65	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R66	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R67	19B800607P473	Metal film: 47K ohms + or -5%, 1/8 w.
R68	19B800607P473	Metal film: 47K ohms + or -5%, 1/8 w.
R69	19B800607P333	Metal film: 33K ohms + or -5%, 1/8 w.
R70	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R71	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R72	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R73	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R74	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R75	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R76	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R77	19B800607P101	Metal film: 100 ohms + or -5%, 1/8 w.
R78	19B800607P101	Metal film: 100 ohms + or -5%, 1/8 w.
R79	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R80	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R81	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R82	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R83	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R84	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R85	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R86	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R87	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R88	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R89	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R90	19B800607P222	Metal film: 2.2K ohms + or -5%, 1/8 w.
R91	19B800607P101	Metal film: 100 ohms + or -5%, 1/8 w.
R92 thru R94	19B800607P101	Metal film: 100 ohms + or -5%, 1/8 w.
R95	19B800607P101	Metal film: 100 ohms + or -5%, 1/8 w.
R96	19B800607P221	Metal film: 220 ohms + or -5%, 1/8 w.
R97	19B800607P220	Metal film: 22 ohms + or -5%, 1/8 w.
R98	19B800607P180	Metal film: 18 ohms + or -5%, 1/8 w.
R99	19B800607P120	Metal film: 12 ohms + or -5%, 1/8 w.
R100	19B800607P330	Metal film: 33 ohms + or -5%, 1/8 w.
R101 and R102	19B800607P121	Metal film: 120 ohms + or -5%, 1/8 w. (Used in G3, G7, G8).
R101 and R102	19B800607P101	Metal film: 100 ohms + or -5%, 1/8 w. (Used in G10).
R103	19B800607P390	Metal film: 39 ohms + or -5%, 1/8 w.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - -
U2	19A705927P1	Silicon, bipolar: sim to Avantek MSA-0611.
U3	19A705927P1	Silicon, bipolar: sim to Avantek MSA-0611.
U4	19A705927P1	Silicon, bipolar: sim to Avantek MSA-0611.
U5	19A149944P201	Dual Modulus Prescaler: sim to Motorola MC12022A.
U6	19B800902P5	Synthesizer, custom: CMOS, serial input.
U8	19A702293P3	Linear: Dual Op Amp; sim to LM358D.
U9	19A702293P3	Linear: Dual Op Amp; sim to LM358D.
U10	19A703471P320	Digital: 3-Line To 8-Line Decoder; sim to 74HC138.
U12 and U13	19A703483P302	Digital: Quad 2-Input NAND Gate; sim to 74HC00.
U14	19A702705P4	Digital: Quad Analog Switch/Multiplexer; sim to 4066BM.
U15	19A704971P8	Voltage Regulator, Positive: sim to Motorola MC78M05CDT.
U16	19A704971P10	Voltage Regulator, 8V: sim to MC78M08CDT

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter" which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

REV. A - UHF RECEIVER SYNTHESIZER BOARD 19D902664G3

The UHF Receiver Synthesizer module was modified to meet ETSI requirements.

Items 3 and 7 were changed and item 23 was added.

Item 3 was: 19D902509P3.
Item 7 was: 19A702381P513.
C16 was 6.8 pF (19A702236P21).
C2 was deleted (19A702236P10).

REV. A - UHF RECEIVER SYNTHESIZER BOARD 19D902664G7
REV. B - UHF RECEIVER SYNTHESIZER BOARD 19D902664G3

To improve operation.
C3 was 22 pF (19A702236P34).
C5 was 10 pF (19A702236P25).
C6 was 18 pF (19A702236P32).
C16 was 8.2 pF (19A702236P23).
R4 was 47 ohms (19B800607P470).

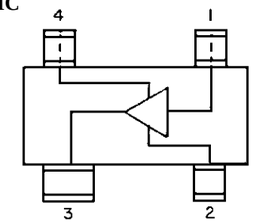
REV. B - UHF RECEIVER SYNTHESIZER BOARD 19D902664G7
REV. C - UHF RECEIVER SYNTHESIZER BOARD 19D902664G3

To support 12.5kHz operation, changed Y1.
Was 1.5PPM crystal (19B801351P12).

REV. C - UHF RECEIVER SYNTHESIZER BOARD 19D902664G7

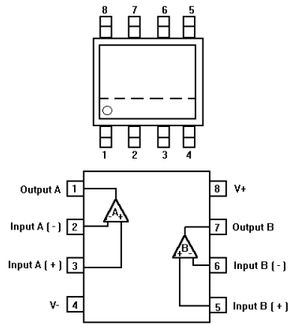
To reduce spurious radiation to meet ETSI specs.
L12 and R18 interchanged. L2 was 1uH (19A700024P13).

U2 thru U4
19A705927P1
Silicon Bipolar IC

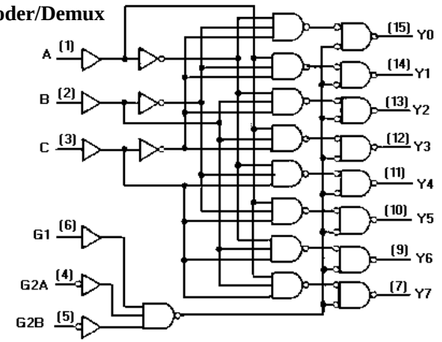


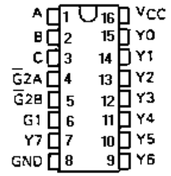
PIN 1. RF INPUT
2. GROUND
3. RF OUTPUT AND BIA
4. GROUND

U8 & U9
19A702293P3
Dual Operational Amplifier

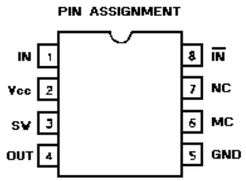


U10
19A703471P120
Decoder/Demux



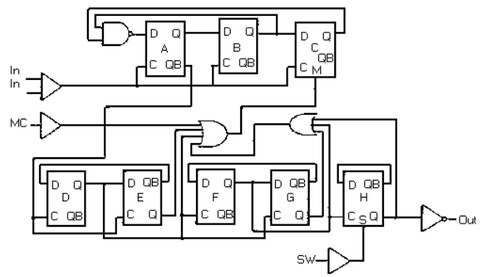


U5
19A149944P201
Modulus Prescaler

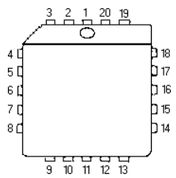


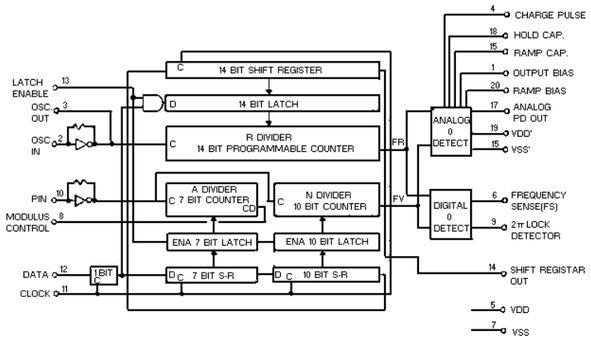
FUNCTION TABLE		
SW	MC	DIVIDE RATIO
H	H	64
H	L	65
L	H	128
L	L	129

SW: H = Vcc L = OPEN
MC: H = 2.0V TO Vcc
L = GND TO 0.8V

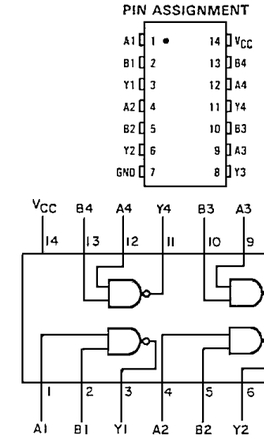


U6
19B80090P5
Synthesizer

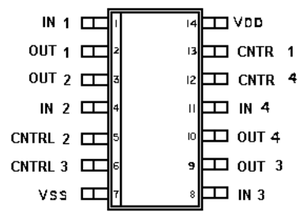


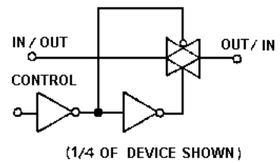


U12 & U13
19A703483P302
Logic Gate/Inverter



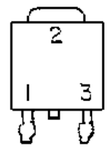
U14
19A702705P4
Quad Analog Switch





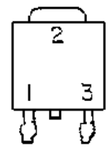
CONTROL	SWITCH
0	OFF
1	ON

U15
19A704971P8
+5V Regulator



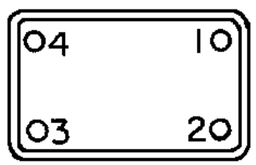
PIN	FUNCTION
1	INPUT
2	GROUND
3	OUTPUT

U16
19A704971P10
+8V Regulator



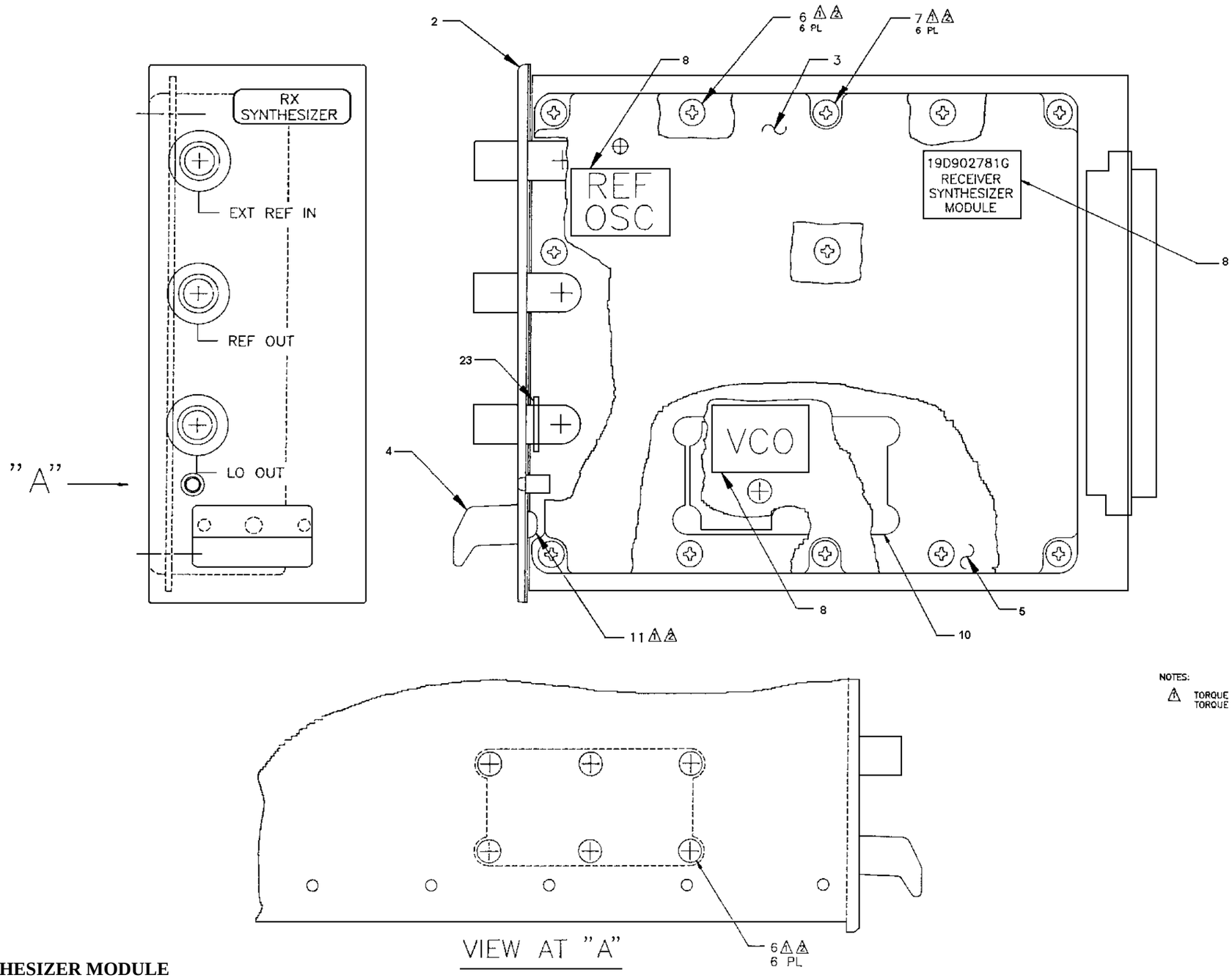
PIN	FUNCTION
1	INPUT
2	GROUND
3	OUTPUT

Y1
19B801351P12
Crystal Oscillator



PIN CONNECTIONS

1. COMMON & CASE
2. OUTPUT
3. + Vcc
4. MODULATION



NOTES:

⚠ TORQUE SCREWS, ITEMS 6 AND 7, TO 15.5 ±1.3 INCH POUND TORQUE SCREW , ITEM 11 , TO 20 ± 1.3 INCH POUNDS.

RECEIVER SYNTHESIZER MODULE
19D902781G3, G7, G8, G10

(19D902781, Sh. 2, Rev. 2)

REFERENCE OSCILLATOR & BUFFER

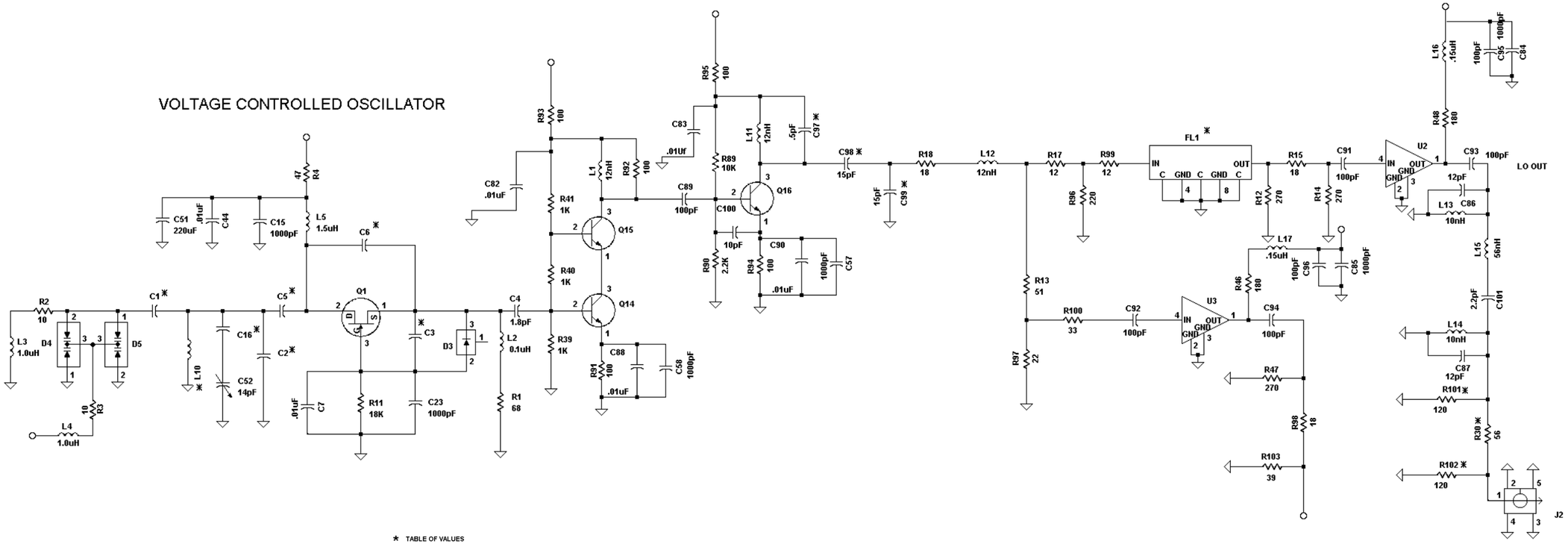
LOOP FILTER

SYNTHESIZER IC'S

THIS SCHEMATIC DIAGRAM APPLIES TO	
MODEL NO.	REV LETTER
19D902664G3	C
19D902664G7	C

RECEIVER SYNTHESIZER MODULE
19D902664G3, G7, G8, G10

(19D904091, Sh. 1, Rev. 4)

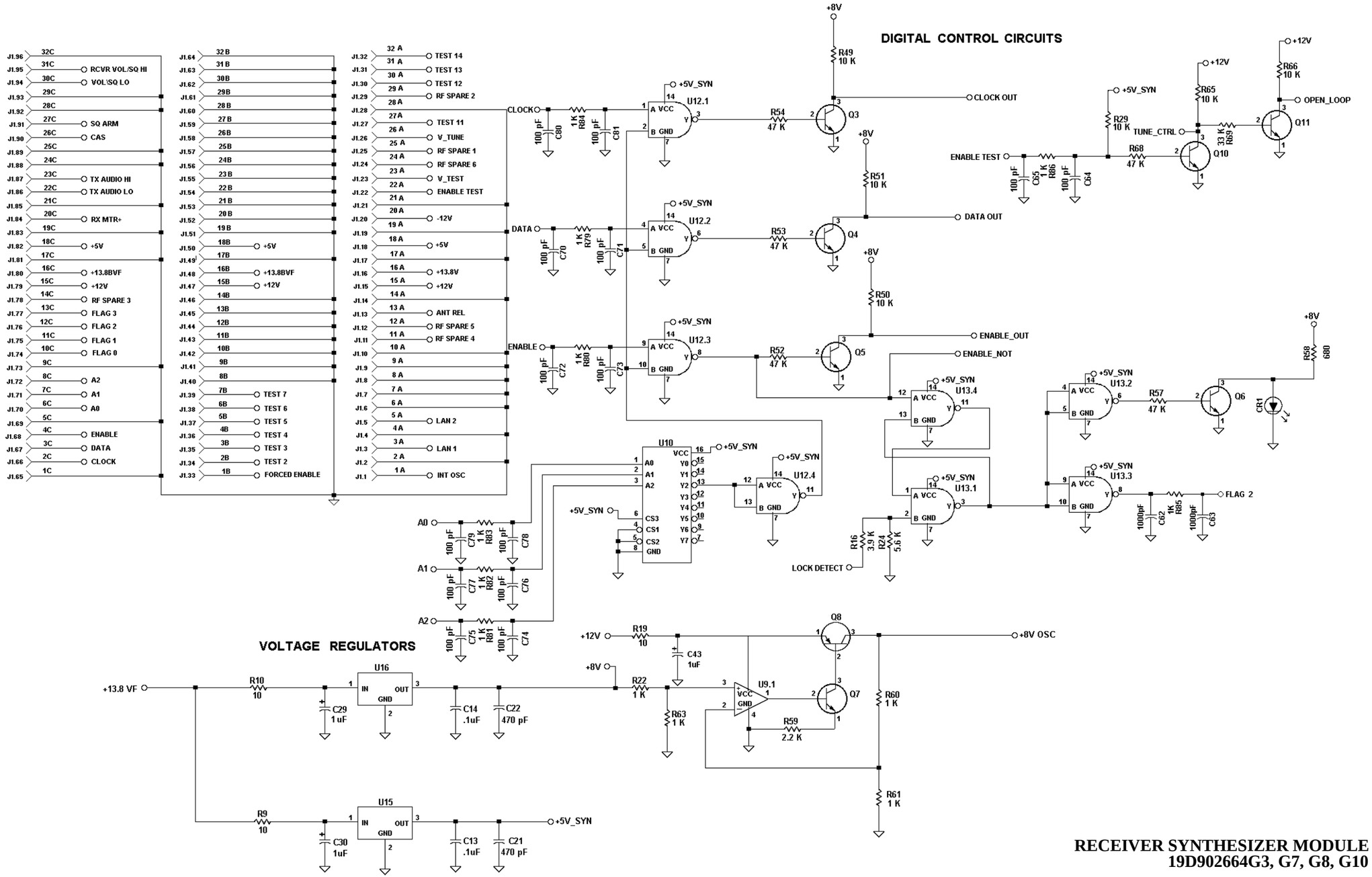


★ TABLE OF VALUES

DESIGNATOR	PART VALUE			
	902781G3	902781G7	902781G8	902781G10
C1	3.9pF	3.9pF	4.7pF	3.9pF
C2	NOT USED	NOT USED	3.9pF	NOT USED
C3	33pF	27pF	27pF	22pF
C5	15pF	12pF	12pF	12pF
C6	27pF	22pF	22pF	18pF
C16	8.2pF	10pF	12pF	10pF
C97	.5pF	.5pF	2.7pF	NOT USED
C98	15pF	15pF	16pF	12pF
C99	15pF	15pF	16pF	12pF
R30	56	56	56	68
R101	120	120	120	100
R102	120	120	120	100

RECEIVER SYNTHESIZER MODULE
19D902664G3 , G7, G8, G10

(19D904091, Sh. 2, Rev. 7)


DIGITAL CONTROL CIRCUITS
RCVR VOL/SQ HI
VOL\SQ LO
SQ ARM
CAS
TX AUDIO HI
TX AUDIO LO
RX MTR+
+5V
+13.8BVF
+12V
RF SPARE 3
FLAG 3
FLAG 2
FLAG 1
FLAG 0
A2
A1
A0
ENABLE
DATA
CLOCK
TEST 7
TEST 6
TEST 5
TEST 4
TEST 3
TEST 2
FORCED ENABLE
TEST 14
TEST 13
TEST 12
RF SPARE 2
TEST 11
V_TUNE
RF SPARE 1
RF SPARE 6
V_TEST
ENABLE TEST
-12V
+5V
+13.8V
+12V
ANT REL
RF SPARE 5
RF SPARE 4
LAN 2
LAN 1
INT OSC
CLOCK
DATA
ENABLE
+5V_SYN
+8V
+12V
CLOCK OUT
DATA OUT
ENABLE_OUT
ENABLE_NOT
ENABLE TEST
TUNE_CTRL
OPEN_LOOP
FLAG 2
LOCK DETECT
+8V OSC
VOLTAGE REGULATORS
+13.8 VF
+5V_SYN
RECEIVER SYNTHESIZER MODULE
19D902664G3, G7, G8, G10
(19D904091, Sh. 3, Rev. 2)