MAINTENANCE MANUAL
LOGIC BOARD
P29\5000006000

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DESCRIPTION

The Logic Board resides in the PC and serves as the controlling circuitry to drive the Audio Tower circuitry. The Logic Board is the only board in the CCS which has clock or oscillator signals on it.

The Logic Board controls all of the matrix switches and volume levels on the Matrix Board's digital pot circuits. The dispatcher communicates with the Logic Board through the dispatcher keyboard and the input lines from the Audio Tower. The Logic Board is connected to the Audio Tower through a DB37 cable and is connected to the dispatcher keyboard through a locking connector on the Logic Board's outside edge. The Logic Board conducts most of its activity without PC intervention.

CIRCUIT ANALYSIS

The Logic Board can be placed in any of the expansion slots for the AT-type PC. A DIP Switch located on the board selects the board's memory address and should have all of its switches set on (D000:0000). U10 handles address decoding.

U1, an 80C152 microprocessor, drives the Logic Board. U4, a 27C512 Eprom, is the firmware for the microprocessor. U5, a 62256, is an associated RAM. Y1, an 11.0592 MHz crystal, is the clock for the microprocessor. The dual port ram, (DPRAM; U3, a 65231) handles the communication between the microprocessor and the PC via the PC expansion bus.

The microprocessor is almost constantly looking at the contents of certain set locations in the dual port memory. When it sees a command flag, it retrieves the command, executes it. When it is finished loading any return data for the PC, an interrupt is generated in the PC. The PC then retrieves its data from the dual port memory. In this way, the memory, which is bidirectional, serves as the gateway through which the PC and the microprocessor communicate.

Gates located on U46 and U13 arbitrate memory access. Because some PC systems leave the address latched on the expansion bus, special chip select and control logic is required. The following steps show the logic involved:

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Step 1 The gates look at the read and write lines on the expansion bus. If neither is active, then the address decoder for the board is not activated. This arrangement prevents the decoder from thinking that it is selected when it is not, which eliminates the generation of extraneous select signals.

Step 2 A busy condition on the expansion bus is generated if two conditions are present: **1)** the address decoder must be active (its address is selected), and **2)** an access must be active from the microprocessor side of the DPRAM. Only when both of these conditions are met is the busy line on the expansion bus active. This arrangement eliminates unneeded busy signals on the expansion bus lines.

Together these two systems serve as the arbitration system for memory access of the DPRAM.

The Logic Board needs only an 8-bit slot in the expansion chassis.

Individual ports on the microprocessor are used to turn on or off the control lines for the Audio Tower. These lines are connected to an inverter with a pullup and a diode protection circuit. Each line then connects to the DB37 to interface with the Audio Tower. The firmware within the Eprom U4 controls the microprocessor and gives it the intelligence to correctly set these lines. To set a matrix switch the microprocessor sets on and off a group of lines. The group contains the lines for the X and Y coordinate of the switch, the address of the switch chip and the state (on or off) desired. The microprocessor then toggles the strobe port and the Matrix Board sets the desired switch. This sequence occurs only when some event, such as PTT, requires it. Normally there is no signal activity on the lines.

Inputs from the Audio Tower (PTT circuits, jack sense lines, and digital inputs) are handled by a design similar to the one that handles the control lines. Signals from the DB37 go through diode protection and then are inverted before being presented to U20, U21, or U22. These chips serve as parallel buffers between the outside lines and keyboard scanner chip U36. When U36 sees that a line has changed states, it generates an interrupt in the microprocessor. The microprocessor then polls the scanner chip U36 to determine the current states of U20, U21 and U22. The microprocessor knows the last state of each chip and deduces what has changed.

Power is supplied through the expansion slot connector by the PC. An on-board voltage regulator, VR1, supplies a regulated 5 volts DC to the dispatcher keyboard. In addition, a PTC supplies a limited 12 volts DC to the DB37 cable to power the PTT circuits in the Audio Tower. This design prevents the Logic Board from seeing all of the PTT circuits become active if the Audio Tower loses power.

The dispatcher keyboard communicates serially with the microprocessor at 9600 baud. The keyboard's signal is sent through diode protection and inverted before being delivered to a microprocessor port. Firmware within U4 supplies the intelligence for this process.

An on-board A-to-D converter ,U35, receives the DC voltage from the Audio Tower for the VU meter signal. The voltage goes through diode protection, an op amp (U29A) to buffer and adjust the level, and then more diode protection before being input to the A-to-D converter chip. The resulting number is given to the microprocessor which delivers it to the DPRAM. The PC regularly checks the DPRAM and updates the graphic display to correspond to the current VU level.

An on-board tone generator chip, U38, provides alert tones for the "Tone" line in the DB37 cable. The chip is a programmable generator which divides one of the already-divided clock frequencies and outputs the desired tone. The tone is sent to the Audio Tower via the DB37 cable and then is routed to the appropriate speaker or audio line.

Dividers U31A and U31B generate the clock signals for the scanner, tone generator, and any future additions. A divided-by-8 signal is delivered to the scanner chip as its clock. A divided-by-4 signal is delivered to the programmable tone generator chip U38.

The timers in U12A and U12B generates the power-on reset. After the delay programmed by the RC network, a reset is generated to start U1.

As part of start up, U1 does the following initialization tasks:

- It reads the scanner chip several times to determine current states and to clear any pending or unprocessed interrupts.
- It clears the DPRAM and writes a signature in a set location. This signature is later accessed by the PC to verify Logic Board activity.
- It checks the state of the "Power Ind" line. If the line is active, U1 then outputs "turn off" commands to all matrix switches in the Audio Tower. This is done to ensure that the initial matrix is completely off.
- It begins polling the DPRAM for commands from the PC.
- It processes any interrupts received from the scanner chip or any data received from the keyboard.
- It begins monitoring the digital voltage received from the A-to-D converter for the VU display.

In short, U1 "wakes up, cleans up, and listens up.

For future expansion, there are on-board locations for a DSP, with its associated Eprom and Rams, and a Codec. These locations are not currently occupied and may be used in future versions. An EEPROM for information storage/retrieval and a twinaxial interface are provided, but these items are not currently supported.

The "Power Ind" line is handled like the other inputs that are scanned by the scanner chip U36. If the input changes state, the microprocessor knows that the Audio Tower has lost power. The microprocessor waits until the Audio Tower is active again and then clears all of the matrix switches before restoring the ones that were active when power was lost. The "Power Ind" line gives the microprocessor the powered status of the Audio Tower. This line is not simply a power line tied to the DB37, but is active only after the Matrix Board has performed its own reset. Therefore, all of the matrix switches are cleared in two ways: the on-board reset and the clearing by the Logic Board. This arrangement ensures that the matrix is cleared before use.

TESTING THE LOGIC BOARD

Listed below are test procedures for the CCS Logic Board. In case of problems, refer to the "**PROBLEM RESOLUTION**" section.

Required tools: Oscilloscope, DVM, AT-compatible PC, CTEST test program on PC, Logic Board Tester (Part Number V9030).

Setup procedure:

- Carefully remove the Logic Board from the PC.
- Verify that all of the switches on the DIP-Switch are on.
- Place the board back in the PC in any available slot.
- If you are using a working CRT Console System, follow the cabling instructions to connect the DB37 cable from the Audio Tower to the Logic Board.

Test Procedures:

Use the following procedure for the Logic Board Tester:

1. Connect the DB37 cable from the Logic Board Tester to the Logic Board. Power up the PC using standard procedures.

2. At the DOS prompt, insert the diskette containing the CTEST program in the A: drive and close the door. Type the command "**A:CTEST**" and press the **<Enter>** key. The PC loads the test program into memory and executes it.

Upon initialization, the CTEST program looks at memory location D000:0000 for the Rev. "signature" number of the Logic Board prom. If the contents are correct, the program prints:

"**Console Logic Board detected. Version x.xx**"

at the top of the video monitor screen. If the contents are incorrect or missing, the program reports

"**CLB not detected**"

and then exits.

3. If the "CLB board not detected" message appears, the cause may be any of the following:

- a faulty DIP-switch setting for the address of the board
- software or other options installed which conflict with the DPRAM address
- a faulty Logic Board.

4. Experienced PC users can use the DEBUG program to view the contents of DPRAM to verify the contents. Please refer to the problem resolution section for details on that and other possible procedures.

5. The Logic Board Tester emulates a complete Matrix Board. The tester has all of the chip select and decoder logic present on the Matrix Board. The tester also has one of the same cross-point switch chips as found on the Matrix Board.

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6. Instead of being wired to switch audio signals from point to point, Logic Board Tester cross-point switch chip is wired to a bank of 8 LED's. To perform a complete test on the address, data, and strobe lines, simply type a "**P**". The LED's should successively light, one at a time, until all are lit. They will then turn off one at a time until all are off. The on/off sequence will repeat 19 more times.

Should certain LED's fail to turn on, fail to turn off, or fail to follow the prescribed sequence in any other way, a problem exists. Refer to the **PROBLEM RESOLUTION** section below and to the schematics on the Logic Board and the Matrix Board.

7. When the LED test is successful, you have completely tested the majority of the functions of the Logic Board. Press the PTT test on the Logic Board Tester. PTT2 should change color as the key is pressed and should return to original color as the key is released. This procedure tests one of the PTT circuits. Next, press "**1**," on the PC keyboard. You should be able to hear the first relay click on. Press "**Q**" and the relay should turn off. The second relay can be tested by pressing "**2**," on the PC keyboard to turn it on and "**W**" to turn it off.

3. With the DISPATCHER keyboard connected to the Logic Board, press a key on the keyboard. One or more 3-digit numbers should appear on the PC monitor as a key is pressed. If no 3-digit numbers appear, check for + 5 volts DC (0.1) output from VR1 to Pin 1 of the keyboard connector J1).

At this point you have tested enough of the functions of the Logic Board to determine whether it can switch audio signals, receive PTT, and activate relays. The testing to this point does not include all PTT signals, nor does it include the tone generation circuit or the VU meter circuit.

PROBLEM RESOLUTION

If the CTEST program does not recognize the Logic Board as being active and present in the PC, power the PC off and back on within 3 seconds. Repeat the execution procedure for the CTEST program. If the board is now shown as present and active, return to the normal test procedures for the rest of the tests. If the board is still not detected by CTEST, press the esc key to exit from CTEST. Type "debug" and press the Enter key. When - prompt appears, type "DD000:0" and press the Enter key. You should see a line that reports the letters "CLB" and the Rev. number for the Logic Board prom followed by a large number of 0's. If the Rev. number and the 0's are not on the screen, either the Logic Board itself is malfunctioning or another memory conflict of some kind is occurring.

To correct the Logic Board malfunction, use the following procedure:

Step 1 Verify that the board has power.

Step 2 If power is present, the problem may be a faulty U1, U3, U4, or U12. Check the oscillator circuit for the microprocessor (U1) to see if it is active. U12 is the turn-on reset circuit. If U12 never resets, the microprocessor may be inactive.

Step 3 Check U36, which is the scanner for external inputs from the PTT, Sense, Digital inputs, and other inputs. If U36 is hung in an active state, it could cause the microprocessor to hang up.

Step 4 Check the DIP Switch. If the DIP Switch is defective, the microprocessor and board could be working perfectly, but merely programmed for the wrong address. Verify logic level 0 on U10, pins 14, 9, 7, 5, and 3. Verify that there is 5 volts DC (0.1) on U10, pins 18,16, and 12 (for the "D000" address).

A test that shows that the board is working properly but not ADDRESSED by the PC is that the first two LED's will be on, the rest off, when the board is first powered up. If CTEST cannot change these LED's with the "P" function, the address may be wrong.

Step 5 If no problem is found in the address, check to see if any recent software or hardware changes to the PC could be causing the problem.

If the Logic Board is active but is not activating and deactivating the LEDs correctly, the problem may be in the lines between the microprocessor and the DB37. Use the following procedure:

Step 1 Run the CTEST test program as instructed in the test procedures.

A test that shows that the board is working properly but not ADDRESSED by the PC is that the first two LED's will be on, the rest off, when the board is first powered up. If CTEST cannot change these LED's with the "P" function, the address may be wrong.

Step 2 If certain LEDs do not turn on or turn off, consult the schematics and determine which address lines are involved.

Step 3 Connect probes at the inputs (U28, U27, or U19) to the inverters driving the address lines involved.

Step 4 Verify that a signal is present.

Step 5 Trace the signal until the faulty component is located. In some cases, shorts between lines may be the problem.

If a pattern can be found, the CTEST program can help verify the problem.

CTEST can be used to set or reset single switches. In this manner you activate or deactivate certain address lines and trace the signals. To use CTEST in this way, simply type the letter "X" followed by 4 digits. In sequence, these 4 digits are:

- The chip desired for the switching operation (1-8).
- The next 2 digits are the X and Y coordinates of the switch on the chip. Each digit can be from 0 thru 7.
- The last digit will either be a 0 or a 1. A 0 turns off that particular switch, and a 1 turns it on.

For example, if you type

X 1111

address lines 0,1,2 (x),3,4,5 (y) are set for 0,0,1,0,0,1 respectively. Select lines 0,1,2 are set to 0,0,1 respectively. Data then is a 1 and Strobe is toggled for the switching operation.

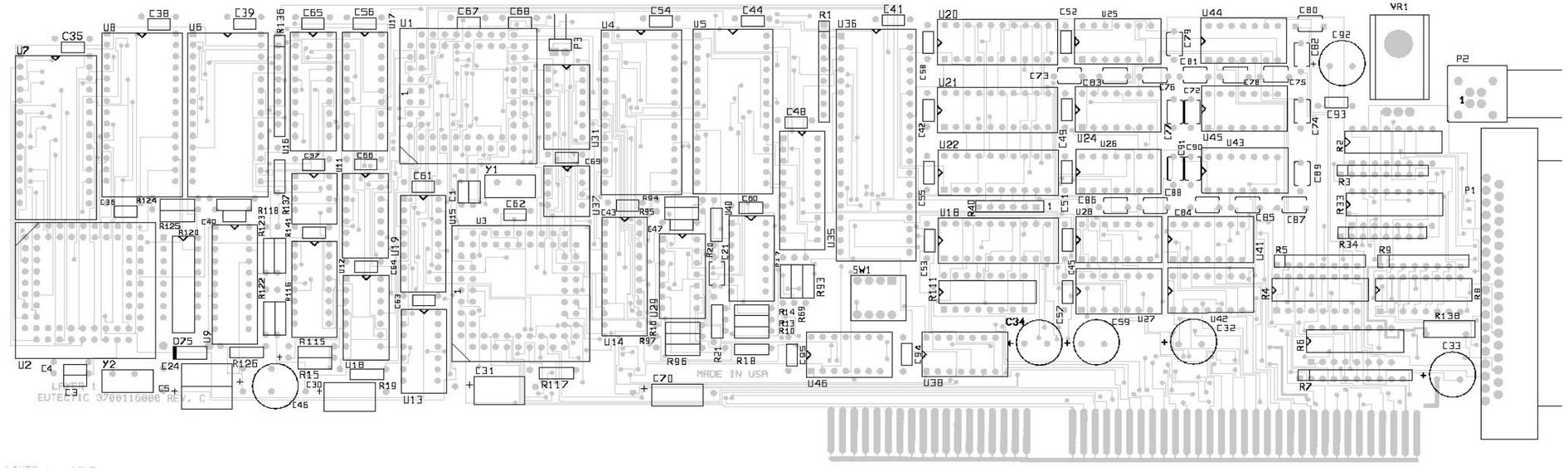
By studying the failure pattern and the schematic you can use CTEST for problem resolution.

If the PC does not boot at all, check U19, pin 12. The pin should be 5 Vdc (±0.1). This is the IOCHRDY line used by the Logic Board to indicate that it is ready to be accessed by the PC. If this line is low, the entire expansion bus is locked up and the PC is dead. U46 provides the input for U19's output and might be the problem.

Since the Logic Board is a complex component, the potential exists for many different kinds of problems. The board is a complete microprocessor with memory and prom. The Logic Board has a DPRAM to serve as a memory addressable by the board or by the host PC. The DPRAM is therefore the communications system between the microprocessor and the PC. Failure to set or unset certain switches can occur. These failures can be due to faulty components, shorts between lines, or failed connections. Poor audio is usually due to some sort of switches being set incorrectly. If too many audio circuits are switched together in the Matrix Board, distortion can result.

There are no adjustments on the Logic Board. If a fault can be located, it probably can be corrected. If a fault cannot be located, the board should be returned for repair.

COMPONENT SIDE



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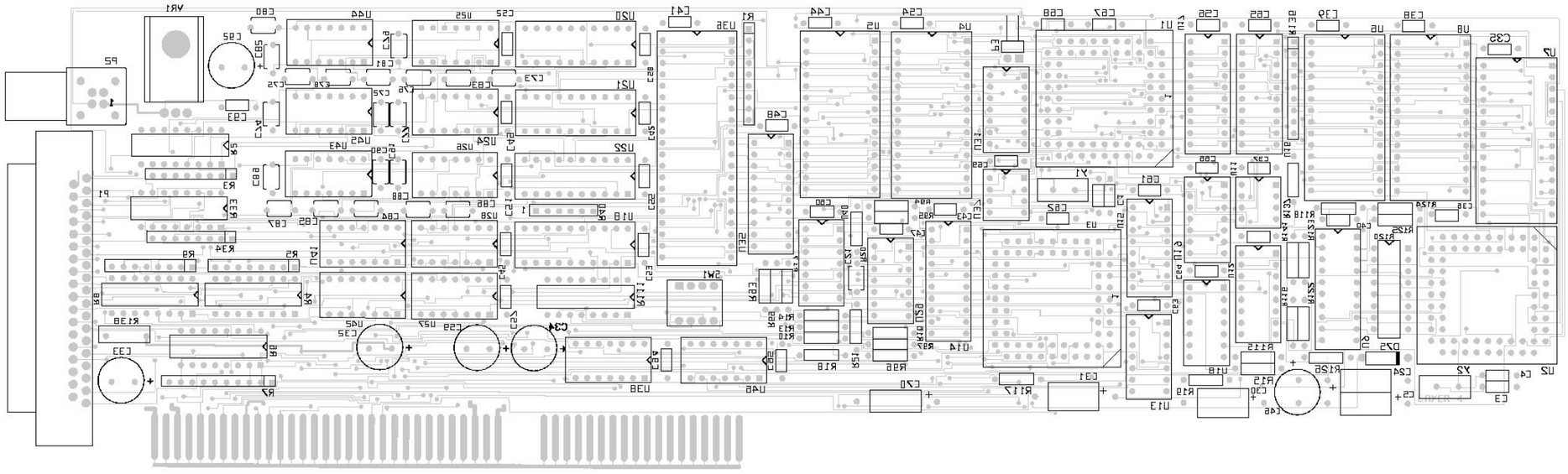
(P29/3700116000, Component Side, Rev. C)

SOLDER SIDE



(P29/3700116000)
(P29/3700116000, Solder Side)

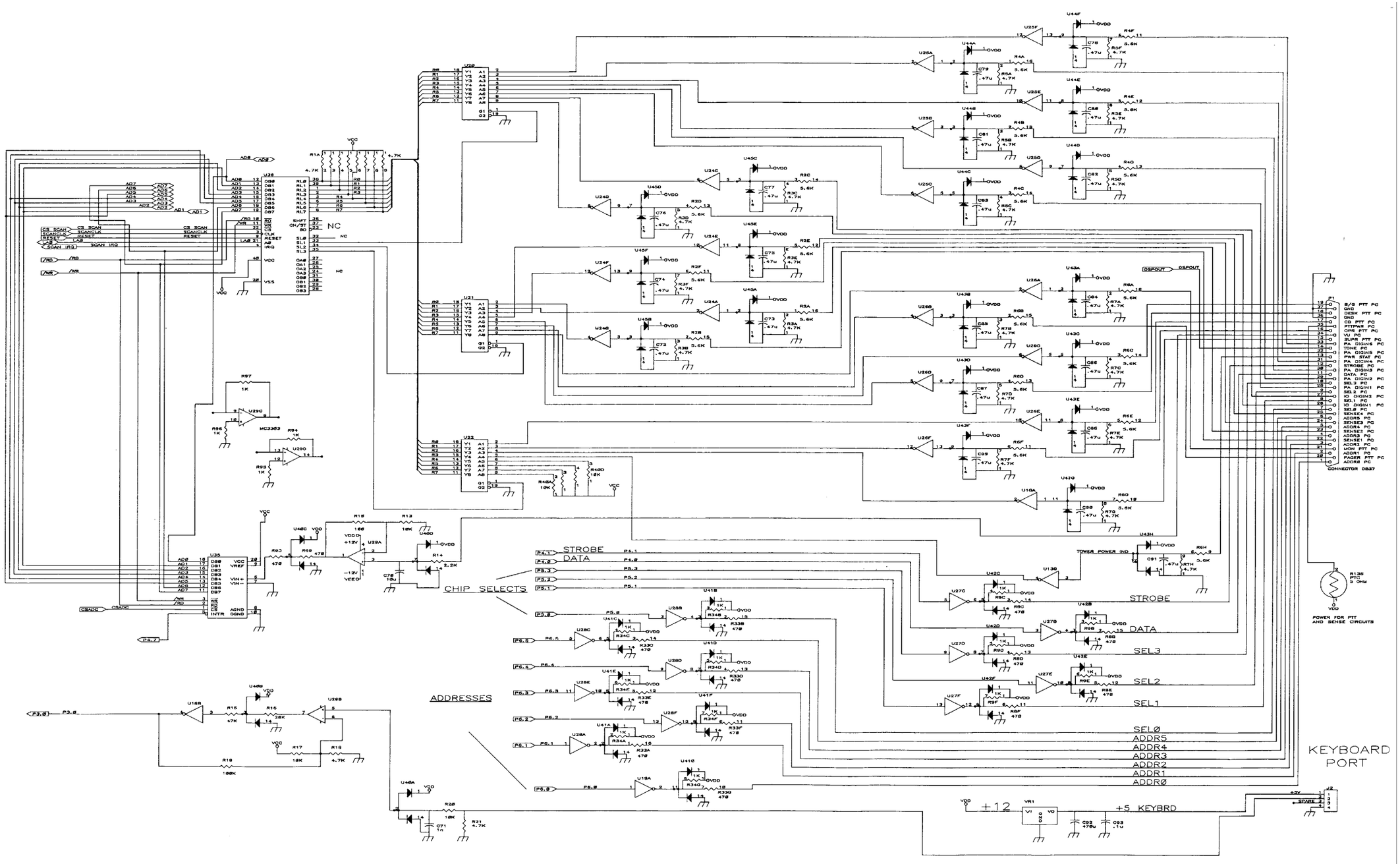
LOGIC BOARD

CONSOLE LOGIC
P29\5000006000

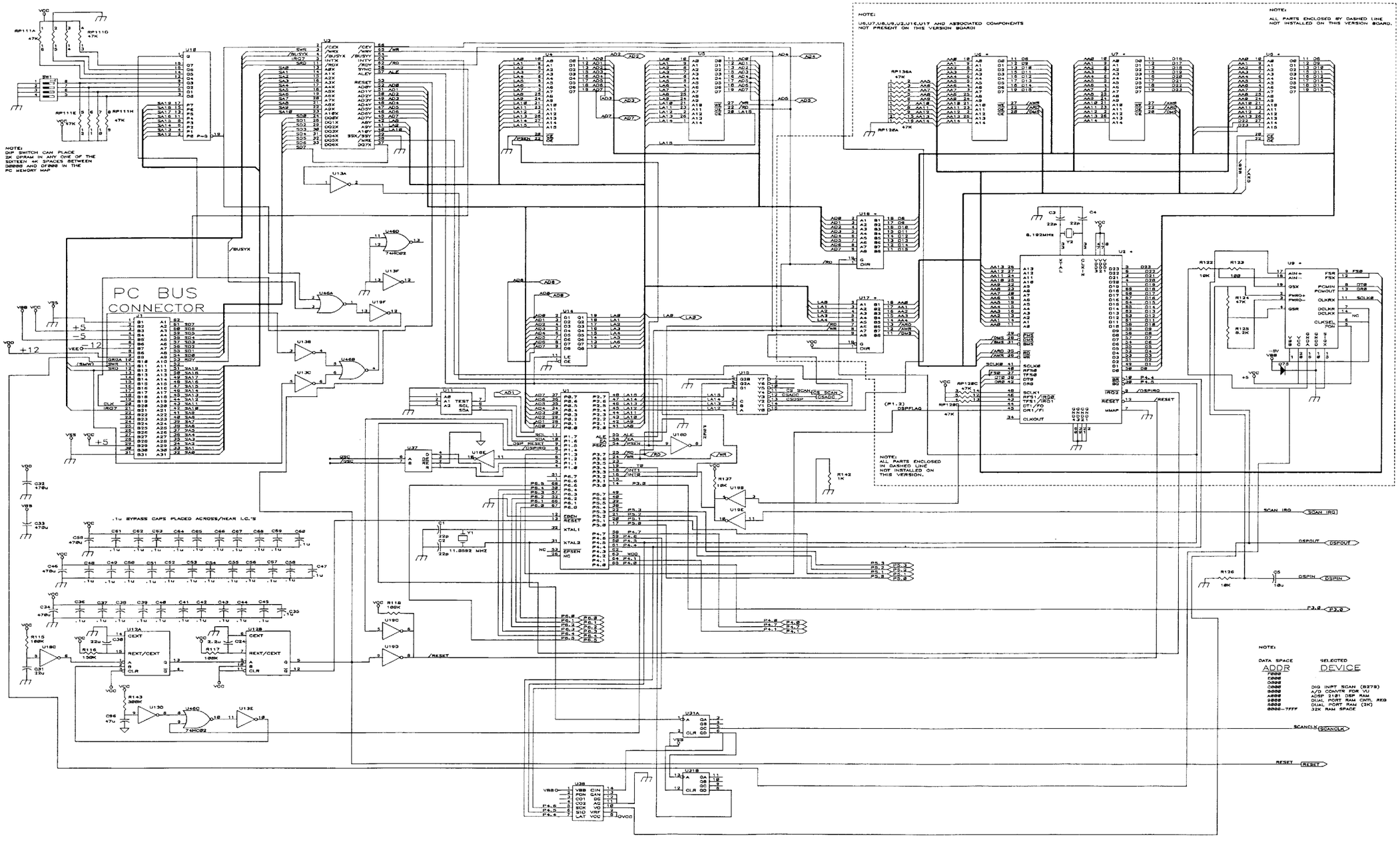
Revised: March 28, 1991
Revision: 1.0

ITEM	QUANTITY	REFERENCE	PART
1	1	Y2 *	8.192MHz
2	6	R122*,R13,R17,R20,R126,R137	10K
3	2	R123*,R1	0100
4	4	R124*,R15,RP120*,RP136*	47K
5	1	R125	8.2K
6	4	C3*,C1,C2,C4*	22p
7	2	C5,C70	10u
8	2	C31,C3	022u
9	6	C33,C32,C34,C46,C59,C92	470u
10	34	C35,C36,C37,C38,C39,C40,C41,C42, C43,C44,C45,C47,C48,C49,C50,C51, C52,C53,C54,C55,C56,C57,C58,C60, C61,C62,C63,C64,C65,C66,C67,C68,C69,C93	.1u
11	5	R142,R94,R95,R96,R97	1K
12	1	C24	2.2u
13	4	R118,R19,R115,R117	100K
14	5	U18,U13,U24,U25,U26	74HC14 HEX INVERTING SCHMITT TRIGGER
15	1	U46	74HC02 QUAD 2-INPUT NOR GATE
16	3	U19,U27,U28	7406 HEX INVERTER
17	3	U5,U6 *,U7 *	62256 RAM
18	2	U4,U8 *	27C512 PROM
19	1	U3	HM65231PLC DPRAM
20	1	U10	74HC688 8-BIT COMPARATOR
21	1	U14	74HC573 TRI-STATE OCTAL D-TYPE LATCH
22	1	U11	X2404 EEPROM
23	1	U37	SN75176B RS422 BUS TRANSCEIVER
24	1	U1	80C152JBMPU
25	1	U15	74HC138 3-TO-8 LINE DECODER
26	1	U12	74HC123 DUAL RETRIG MONOSTABLE MULTIVIB
27	1	U31	74HC393 TRI-STATE OCTAL D-TYPE FLIP FLOP
28	1	U38	ML2036 TONE GENERATOR
29	1	Y1	11.0592 MHz
30	1	SW1	SW DIP-4
31	1	D75	1N4001 DIODE
32	1	S1	28 PIN DIP SOCKET
33	1	R116	150K
34	2	U16 *,U17 *	74HC245 OCTAL TRI-STATE RECEIVER
35	1	U2 *	ADSP-2101-PGA DSP
36	1	U9 *	TCM29C13 CODEC
37	1	R14	2.2K
38	2	R18,R21	4.7K
39	1	P1	CONNECTOR DB37
40	1	U29	MC3303 QUAD OP AMP
41	1	R16	20K
42	2	R93,R69	470
43	1	R138	PTC KEYSTONE KC005R-ND
44	20	C76,C72,C73,C74,C75,C77,C78,C79,C80,C81,C82,C83, C84,C85,C86,C87,C88,C89,C90,C91	.47u
45	6	U45,U43,U44,U41,U40,U42	DIODE ARRAY FSA2501P
46	1	PCB	
47	1	VR1	LM7805 VOLTAGE REG
48	1	J2	LEMO EPG.1B.304.HLN
49	1	U36	8279 KEYBOARD SCAN
50	3	U20,U21,U22	74HC541 INVERTING OCTAL TRI-STATE BUFFER
51	1	U35	ADC0841 A-TO-D CONVERTER
52	3	RP2,RP4,RP6	8x5.6 K DIP 16 PACK
53	1	RP40	5x10 K SIP PACK
54	1	RP111	8x47 K DIP 16 PACK
55	2	RP9,RP34	7x1K SIP PACK
56	1	RP1	8x4.7K SIP PACK
57	2	RP3,RP5	7x4.7K SIP PACK
58	1	RP7	9x4.7K SIP PACK
59	2	RP8,RP33	8x470KDIP 16 PACK
60	2	S2,S3	68 PIN PLCC SOCKET
61	1	DB37	(MALE) TO DB37 (MALE) 10 FT SHIELDED CABLE

ALL PARTS FOLLOWED BY * ARE NOT INSTALLED IN THIS VERSION AND SHOULD NOT BE INCLUDED IN ANY PARTS COUNT.
ALL RESISTORS ARE 1/4 W CARBON UNLESS OTHERWISE NOTED.

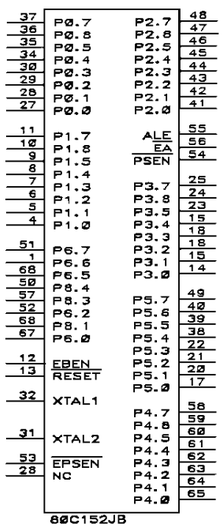


LOGIC BOARD
(Sheet 1 of 2)

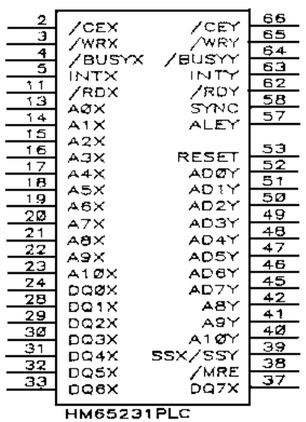


LOGIC BOARD
(Sheet 1 of 2)

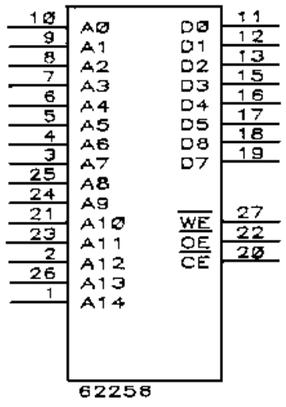
MICROPROCESSOR U1
(80C152JB)



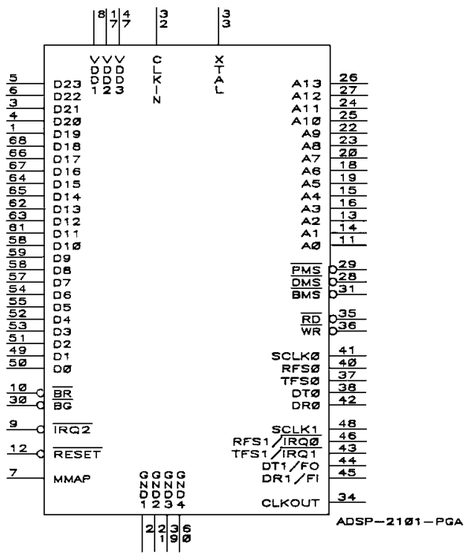
DUAL PORT RAM U3
HM65231PLC



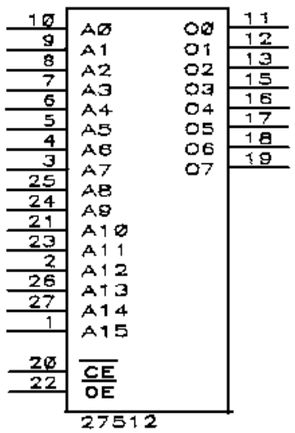
RAM U5, U6, U7
62256



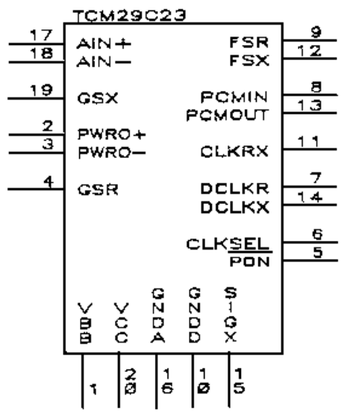
U2
ADSP-2101-PGA



EPROM U4, U8
27C512

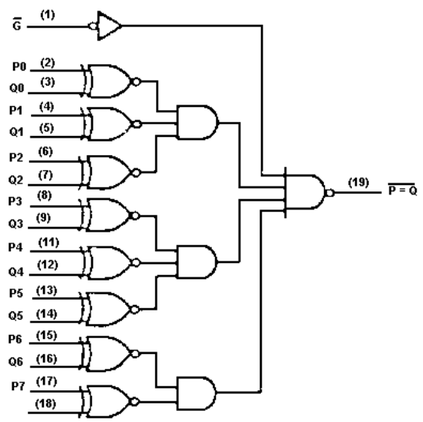


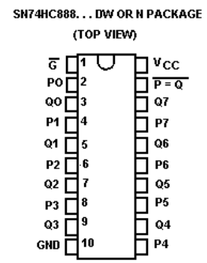
CODEC U9
TCM29C13



U10
74HC688

logic diagrams (positive logic)

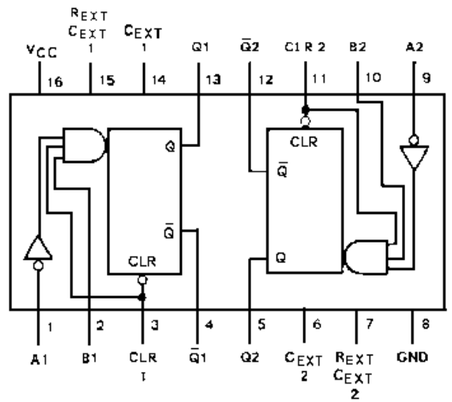




FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE $\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P > Q	X	H
P < Q	X	H
X	H	H

DUAL RETRIGGERABLE MONSTABLE TIMER U12
(74HC123)

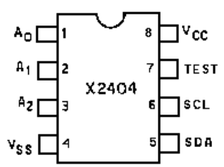


Truth Table

Inputs			Outputs	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊓
H	↓	H	⊓	⊓
↑	L	H	⊓	⊓

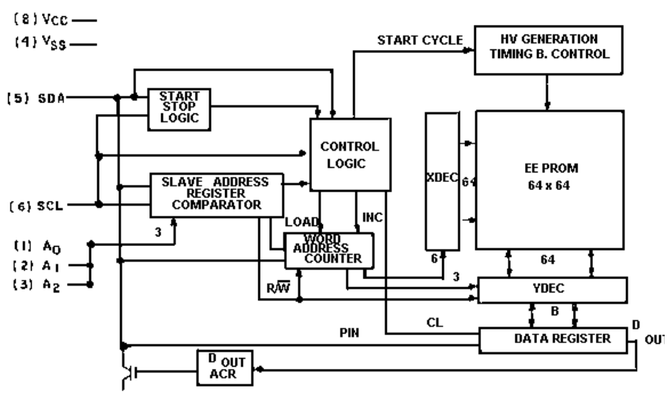
512 X 8 EEPROM U11
(X2404)

PIN CONFIGURATION

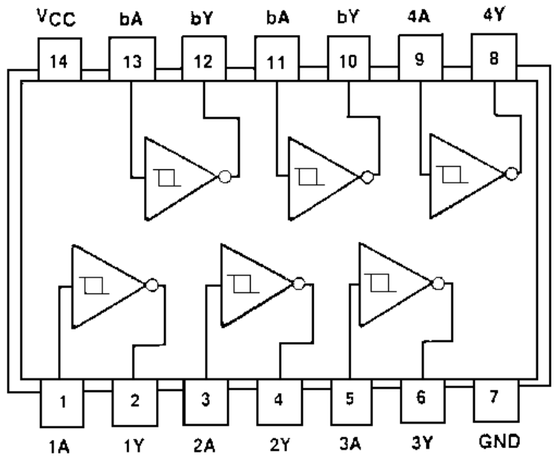


1 A_0 → TO V_{SS}
2 AND 3 A AND A ADDRESS INPUTS
4 V_{SS}
5 SDA SERIAL DATA — I^2C BUS
6 SCL SERIAL CLOCK — I^2C BUS
7 TEST INPUT — TO V_{SS}
8 V_{CC}

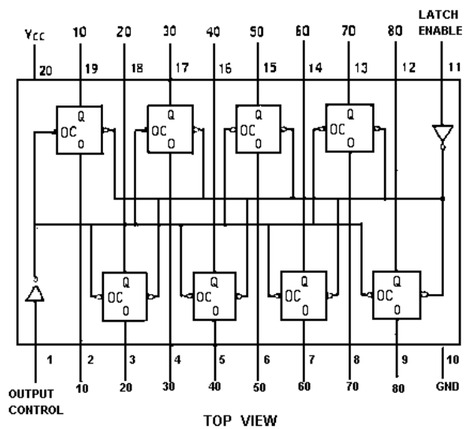
FUNCTION DIAGRAM



HEX INVERTING SCHMITT TRIGGERS U13,U18,U24,U25,U26
74HC14



TRI-STATE OCTAL D-TYPE LATCH U14
74HC753

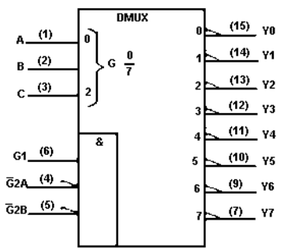


TRUTH TABLE

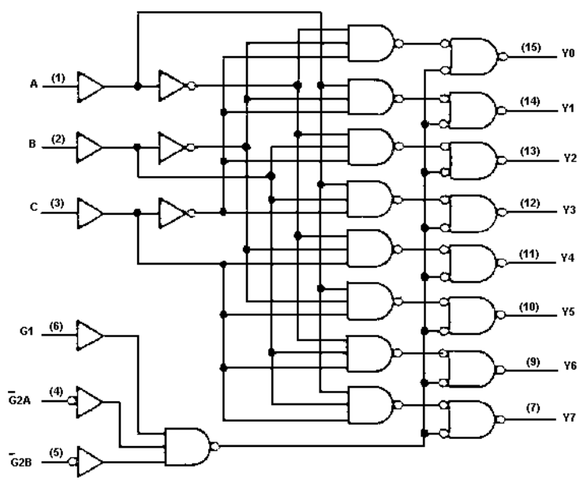
Ouput Control	Latch Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level
Q_0 = level of output before steady-state input conditions were established.
Z = high impedance
X = Don't care

3-TO-8 LINE DECODER U15
74HC138

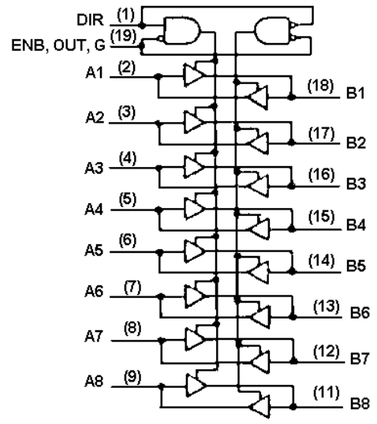


LOGIC DIAGRAM (POSITIVE LOGIC)

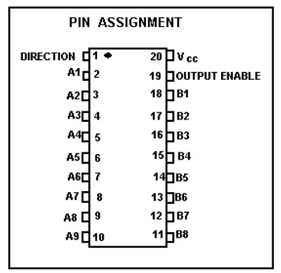


OCTAL TRI-STATE TRANSCEIVERS U16,U17
74HC245

LOGIC DIAGRAM (POSITION LOGIC)



PIN ASSIGNMENT

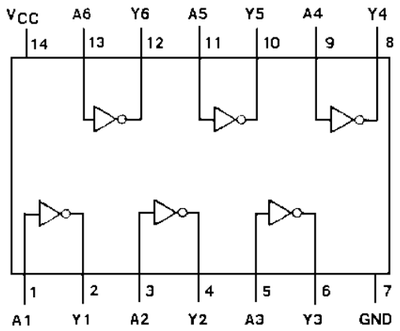


FUNCTION TABLE

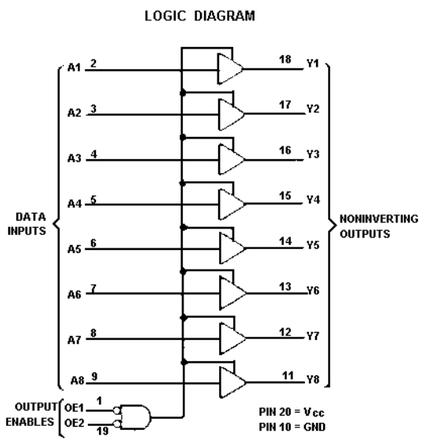
CONTROL INPUTS		OPERATION
OUTPUT ENABLE	DIRECTION	
L	L	DATA TRANSMITTED FROM BUS B TO BUS A
L	H	DATA TRANSMITTED FROM BUS A TO BUS B
H	X	BUSES ISOLATOR (HIGH IMPEDANCE STATE)

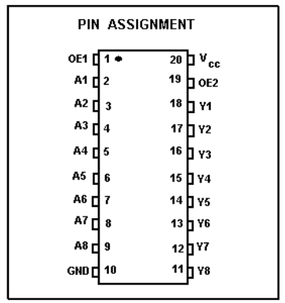
HEX INVERTERS U19,U27,U28
7406

LOGIC DIAGRAM



ANALOG TO DIGITAL CONVERTER U35
ADC0841



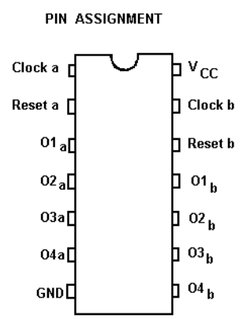


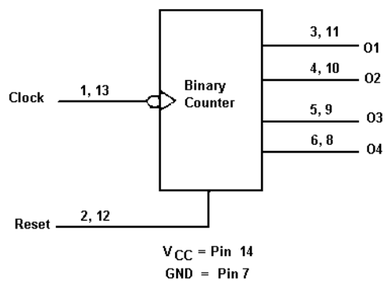
FUNCTION TABLE

Inputs			Ouput
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Z = high impedance
X = don't care

OCTAL TRI-STATE BUFFERS U20,U21,U22
(74HC541)

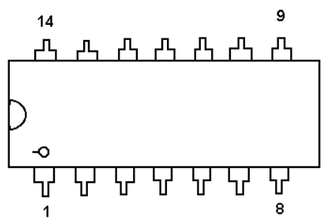


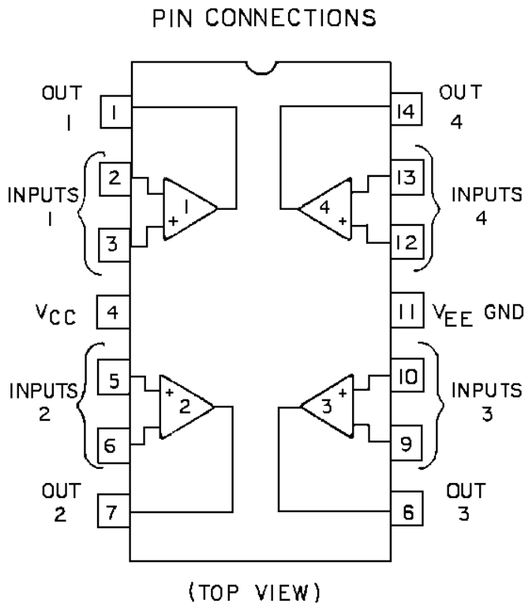


FUNCTION TABLE

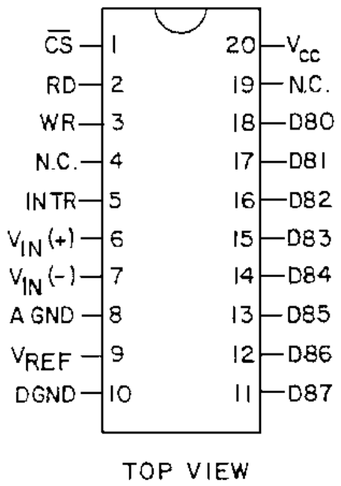
Clock	Reset	Outputs
X	H	L
H	L	No Change
L	L	No Change
⌐	L	No Change
⌐	L	Advance to Next State

KEYBOARD SCAN U36
8279

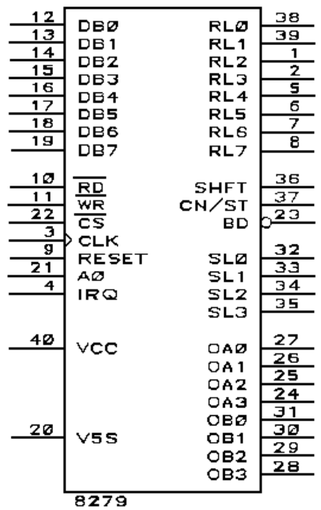




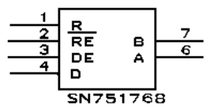
QUAD OPERATIONAL AMPLIFIER U29
(MC3303)



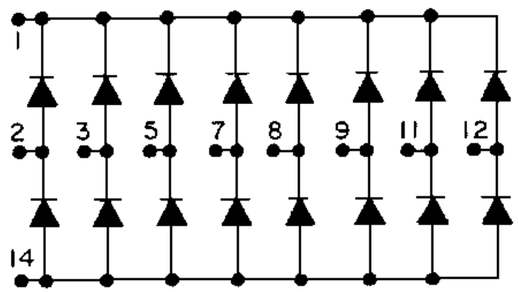
DUAL 4-BIT DECADE COUNTER U31
74HC393



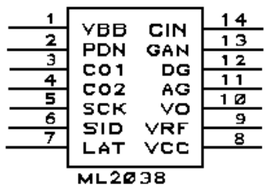
RS-422 BUS TRANSCEIVER U37
SN75176B



DIODE ARRAY U40,U41,U42,U43,U44,U45
FSA2501PDA

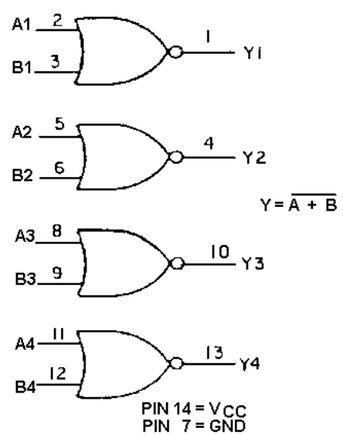


PROGRAMMABLE TONE GENERATOR U38
ML2036

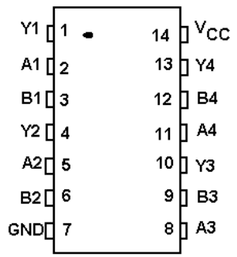


QUAD 2-INPUT NOR GATE U46
(74HC02)

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION DIAGRAM

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

ADDENDUM NO. 1 TO LBI-38720 (PCCR)

This addendum incorporates "Revision Letter" production change information on the Logic Board. Note that Revision B changes the board's part number from P29/5000060000 to P29/5000060001.

Rev. A **Logic Board P29/5000060000 (344A3927P24)**

To activate Audio Tower power status sensing (correct board layout error), disconnected U27 pin 1, disconnected U13 pin 13 and installed a jumper from U13 pin 12 to U22 pin 5. Also installed jumper from U13 pin 13 to the positive (+) terminal of C5.

Rev. B **Logic Board P29/5000060001 (344A3927P24)**

To prevent printed-wire board shorts caused by mechanical stress of P1 connector and other components, replaced P29/5000060000 board with P29/5000060001 board. Revision B is the initial production release of P29/5000060001.