MAINTENANCE MANUAL
MICROCOMPUTER BOARD
19D902865G1, G3, G4

TABLE OF CONTENTS

Ericsson GE Mobile Communications Inc.
Mountain View Road • Lynchburg, Virginia 24502

Printed in U.S.A.

LBI-38726

SPECIFICATIONS*

Input Power		
A+	(J6-23)	13.8 VDC ±20%
SW A+	(J6-24)	13.8 VDC ±20%
+5V	(J6-25)	5.0 VDC ±5%
Maximum Current Drain		
A+		
	RELAY-CTRL HIGH	5 Milliamperes
	RELAY-CTRL LOW	2 Milliamperes
SW A+		300 Milliamperes
+5V		250 Milliamperes
Temperature Range:		-30°C to +70°C (-22°F to +158°F)
Logic Levels		
High (1)		4.0 ±1.0 VDC
Low (0)		0.5 ±0.5 VDC
Rise Time		100 Nanoseconds
Fall Time		100 Nanoseconds
EL Driver Output (13.8 VDC SW A+)		
Voltage		125 Volts RMS
Frequency		400 Hz
Current		15 Milliamperes
Power Relay Control (2.7 K load on Relay Control)		
High Level		2.5 Volts Minimum
Low Level		0.5 Volts Maximum
Light Level Detect		
Upper Hysteresis (Maximum)		2.6 VDC
Lower Hysteresis (Minimum)		2.4 VDC
Watchdog Timer Reset		
Pulse Width		200 Milliseconds (Nominal)
Timeout Period		1.6 Seconds (Nominal)

* These specifications are intended primarily for the use of the service technician. Refer to the appropriate Specification Sheet in the applicable maintenance manual for the complete specifications.

DESCRIPTION

Microcomputer Board 19D902865 provides the intelligent interface to the Keypad/Display Board and the Input/Output Board. The Microcomputer Board also provides the intelligence necessary to interface with the radio, siren/light/PA unit, the vehicular repeater unit, dual control head and Voice Guard unit.

The Microcomputer Board contains an 80C52 microcontroller with external program memory in a FLASH-EPROM. The Microcomputer also contains an EEPROM containing the control unit (radio system) personality along with the user control settings.

Power up/down control of the control unit and the rest of the radio system is performed by a flip-flop. This flip-flop switches the A+ power to the rest of the radio system through a relay.

AC power for the electroluminescent panel is generated by the EL driver device. This power is duty-cycle modulated to provide the intensity control of the EL backlighting.

The fast squelch detector is comprised of an analog filter/limiter circuit. The fast squelch detector provides a quick indication of carrier activity on the receive radio channel.

Ambient light level from the phototransistor on the Keypad/Display Panel is limited by a voltage comparator. This is used to automatically turn on the EL backlighting and reduce the LED brightness.

An optional limited channel guard signal from the radio is re-limited by a comparator. The Microcomputer Board performs the channel guard (tone or digital) decoding in the radio system.

A holding register is used to buffer data to the Keypad/Display Board. This provides isolation and drive of the signals to the Keypad/Display Board.

A second holding register is used to buffer data to the Input/Output (I/O) Board. This provides isolation and drive of the signals to the I/O Board.

A decoder is used to generate a gated write pulse to the holding registers on the Microcomputer Board and other registers on the I/O Board.

The watchdog timer is used to provide a control unit reset pulse. The watchdog timer is used to monitor the microcomputer software execution.

CIRCUIT ANALYSIS

The Microcomputer Board represents the heart of the control unit. It contains the microcomputer, firmware and personality data required to operate the unit. Display data is output to the display board and keypad inputs are received through J1. Interface to the Input/Output Board is through a 26-pin ribbon cable (connector J6).

Figure 1 shows a block diagram of the digital input/output devices. The data bus (U1-36 through U1-43) acts as a parallel port when writing to U5 and U6. U7 is a decoder that is used to provide the memory mapping of U5, U6 and addition I/O on the I/O Board.

POWER RELAY CONTROL CIRCUIT

The power control for the control unit is performed by flip-flop U8.1 and associated circuitry. The power control flip-flop turns on and off the power relay on the Input/Output Board which supplies the switched battery power (SW A+) from the raw continuous battery power (A+).

The output control signal to route A+ to SW A+ on the I/O board is RELAY-CTRL (J6-12). When RELAY-CTRL is high, the relay on the I/O board is turned on (closed) and supplies power to SW A+. When RELAY-CTRL is low, the relay on the I/O board is turned off (opened) and no power is supplied on SW A+.

The relay control flip-flop is powered from the continuous battery power (A+). This ensures that starting from a powered down condition, the control unit can be powered up from the front panel (keypad board).

When the control unit is initially powered down (SW A+, +5V, and RELAY-CTRL are at zero volts but continuous battery power is running on A+), the board is turned on by grounding the PWRSW (J1-3). This turns on transistor Q2. The collector of Q2 is pulled up to A+ causing a rising edge to the clock input of flip-flop U8.

The rising edge causes the flip-flop U8-1 to change state from Q = 0 to Q = 1. The $\overline{Q}$ output becomes $\overline{Q}$ = 0, thereby turning on pass transistor Q3 and allowing continuous A+ to be sent to RELAY-CTRL and onto the I/O Board to activate the power control relay. A subsequent press of the power switch will generate another rising edge to the clock input of the flip-flop, thereby toggling its state from Q = 1 to Q = 0 (Q becomes Q = 1). With Q = 1, pass transistor Q3 turns off which removes continuous A+ from RELAY-CTRL turning off the power control relay on the I/O Board.

Resistor R35 and capacitor C33 provide a hysteresis feedback to the input of the flip-flop. This hysteresis provides debounce on the PWR button (PWSW) in order to prevent chatter on the power up and power down due to mechanical switch bounce.

Resistor R31, diode D1 and capacitor C31 provide filtering on the A+ power to the relay control flip-flop. This filtering prevents the ignition noise and spurious battery voltage drops from changing the state of the relay control flip-flop.

Resistor R32, diode D2 and capacitor C32 provide filtering on the A+ power used in the generation of the clock pulse to the flip-flop.

Zener diode VR5 and diode D4 insure the pass transistor Q3 turns on only when Q = 0 irrespective of spikes on A+.

MICROCOMPUTER, LATCH, EPROM AND EEPROM CIRCUITS

The intelligence of the control unit is contained in the microcomputer U1. The microcomputer is an 80C52 - 8 bit controller. U1 is a high performance CMOS processed part, utilizing internal timers and a serial interface on a priority interrupt structure. The internal CPU handles the Boolean processing, internal bit and byte RAM addressing, instruction fetching and execution and interface to the external world by means of 16 dedicated I/O lines along with an 8 bit bussed memory-mapped I/O.

Microcomputer U1 operates at an internal clock instruction cycle time of 11.0592 MHz (nominal). The clock frequency is determined by quartz crystal Y1, which provides a fundamental mode of operation, and capacitors C51 and C52, which provide start up time and frequency stability over the specified temperature range.

The microcomputer accesses program memory information from the FLASH-EPROM U3. The FLASH-EPROM (EPROM) is a 64K by 8 bit programmable read-only-memory device. This device contains both the operational instruction code for the CONTROL UNIT normal mode of operation as

LBI-38726

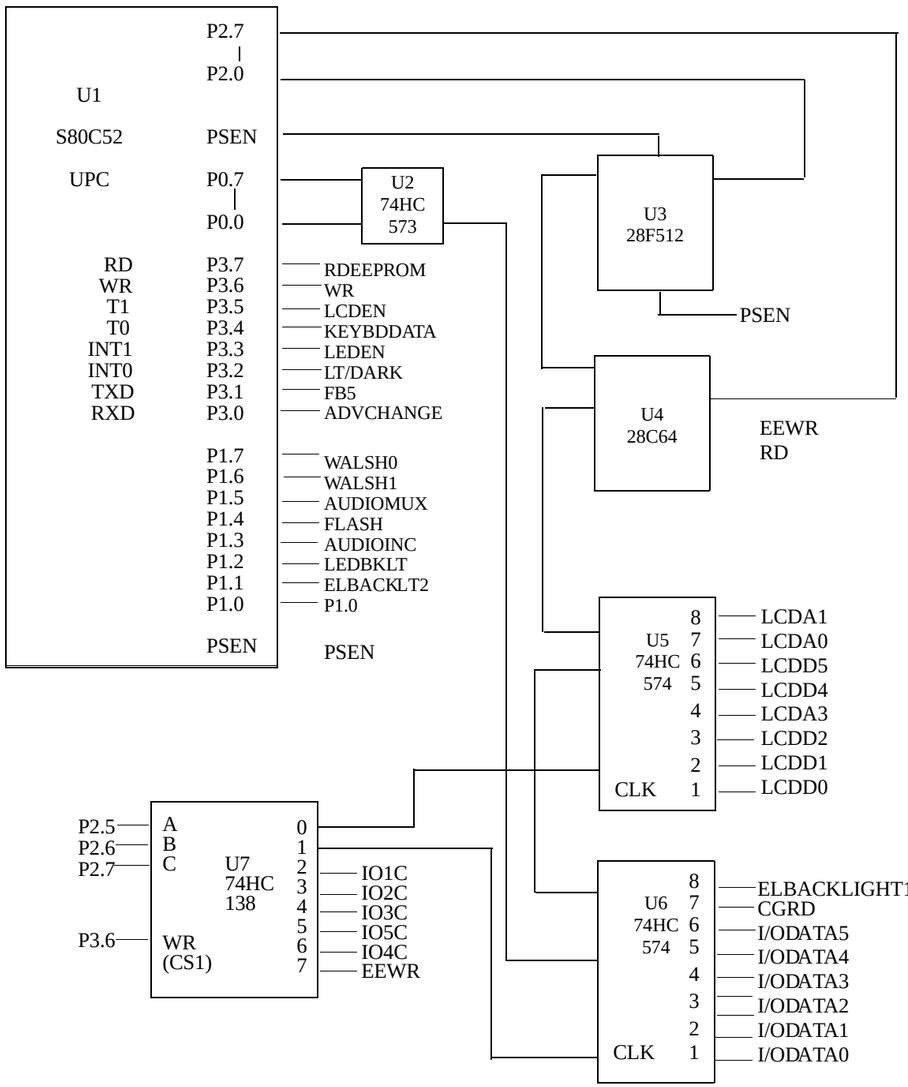


Figure 1 - Digital Block Diagram

well as the test code necessary to implement the test and control functions.

Each access to the EPROM for program memory information is proceeded by an address setup to the EPROM. The high order 8 bits of the address are held stable on lines A8 through A15. Lines A8 through A14 are routed to the EPROM high order address inputs. Address line A15 (P2.7) is routed to the EPROM through U14 which is also used in the flash programming of the EPROM. The low order 8 bits of the address are latched and held stable by the address holding latch U2. The low order address lines are latched on a high to low going pulse on the ALE line. After the address is held stable, the microcomputer issues a low going pulse on PSEN to read the 8 bit program memory information contained in the EPROM at the specified address.

Settings for the radio personality and control unit are contained in the EEPROM U4. The EEPROM is an 8K by 8 bit electrically erasable programmable read-only-memory. This device provides nonvolatile storage of radio personality and user controlled settings. Each access to the EEPROM for personality information is preceded by an address setup to the EEPROM.

The high order 8 bits of the address are held stable on lines A8 through A15. Lines A8 through A12 are routed to the EEPROM high order address inputs. The low order 8 bits of the address are latched and held stable by the address holding latch U2. The low order address lines are latched on a high to low going pulse on the ALE line. After the address is held stable, the microcomputer issues a low going pulse on RD (to read) or WR (to write) the 8 bit personality information from or to EPROM at the specified address.

Device U13 and associated circuitry provide the gated write pulse to EEPROM (U4-27). The gated write pulse is generated from the microcomputer on the signal line WR (U1-18).

Address lines A9 through A12 are gated into U13 to provide an enable to the address decoder U7. The lower order 512 bytes are writable by the microcomputer

In order to write the remaining locations, a PC programmer cable must be installed whereby the control line EEWREN (J6-14) is grounded, thereby allowing writing to all EEPROM locations. When EEWREN is low, diode D3 is low, pulling the inhibit control to U7 low.

Holding register U5 interfaces with the keypad boards to read keypad closure information, activate LEDs and update the LCD display. U5 is accessed via a memory-mapped write to address location 0000 hex.

Holding register U6 interfaces with the I/O board to read radio status and input information, to write radio control information and to route audio paths between the radio and the control unit. U6 is accessed via memory-mapped write address location 2000 hex.

KEYBOARD INTERFACE CIRCUITS

In addition to U5, there are five lines on the microcomputer that interface with the keypad boards. They are LEDBKLT, FLASH, LEDEN, LCDEN and KEYBDDATA.

The holding register U5 latches the data lines to the keypad board. This 8 bit data is used to turn on and off LEDs, setup characters to be written to the LCD display and clock out the sampled keypad closure information to the microcomputer.

WATCHDOG TIMER CIRCUIT

The watchdog timer U11 is used to monitor the operation of the microcomputer software. It generates a reset pulse in the unlikely condition that the microcomputer goes awry and does not execute the program memory software properly.

The watchdog timer consists of a MAX695 integrated circuit. The microcomputer services the watchdog timer at the WDI input (U11-11). The service line is derived at WDT. Presently resistor R79 is installed (R78 removed), allowing servicing to occur through U6-19 (I/ODATA0). The microcomputer toggles WDT at least every 1.6 seconds to prevent the watchdog timer from timing out and generating a board reset. If a hardware or software failure occurs such that U11 is not serviced, a 200 millisecond reset pulse is generated at U11-16. This reset pulse is or'ed with the power on reset from the I/O board (J6-26 and inverted through Q5) by U13.4 and sent to the microcomputer at U1-10.

LIGHT/DARK SENSOR CIRCUIT

The outside ambient light level is detected by the microcomputer via the LT/DARK (U1-14) signal derived from the light level detect circuitry consisting of comparator U10 and associated circuitry.

LT/SENSOR is an analog signal (0 to 5 Volts) inputted to the negative input of U10. As the ambient light level increases in intensity, the LT/SENSOR signal increases in level. Resistor R61 provides a load for the analog level derived from the emitter of the phototransistor on the keypad board. Capacitor C21 provides light level filtering. The load value of R61 was chosen to obtain a nominal ambient light threshold detect at approximately 4 to 5 milliwatts/(cm*cm).

The positive input of U10 is set up with a nominal DC bias level of 2.5 Volts. This bias level fixes the nominal threshold point.

Resistor R62 provides a small level of hysteresis for the detection of the ambient light level. This is used to prevent the comparator from oscillating at light levels near the nominal threshold detect setting.

As the light level increases from a dark condition to a strong light level (0 towards 5 Volts), LT/DARK will start at +5 Volts (due to the internal pull up on the microcomputer) and will flip to

LBI-38726

0 Volts as the LT/SENSOR signal passes the 2.5-Volt reference. As the light level decreases from a strong light to a dark condition (5 Volts toward 0 Volts), LT/DARK will start at 0 Volts and will flip to +5 Volts when the LT/SENSOR signal passes the 2.5 Volt reference.

CHANNEL GUARD LIMITER CIRCUIT

The microcomputer detects the channel guard information on the receiver radio frequency channel. The limited channel guard signal is derived from the radio and again is limited by U10 and buffered by Q9. The microcomputer samples the channel guard signal through AUDIOMUX (U1-7) and is controlled by transistor Q8.

Bias on U10 is set at a nominal 2.5 Volts for detecting the channel guard signal from the radio. U10 serves to buffer and re-threshold the signal received from the radio over the long cable

FAST SQUELCH DETECT CIRCUIT

The fast squelch detect circuit on the microcomputer board is used to provide a quick detection of carrier activity on a receiver radio frequency channel. This quick detection is used in SCAN operation to lock onto a high priority incoming call. The bias used in the detection of carrier activity is noise squelch.

The fast squelch circuit consists of a three-pole high pass filter, an averaging detector, a DC amplifier and a trigger. The fast squelch circuit is used to provide a fast indication of carrier activity on a channel by monitoring the channel received noise component in the 6000 to 8000 Hz range.

A high pass filter, consisting of C61, C62, R81, R82 and U9, removes all voice signals (0 to 3000 Hz) from the incoming received signal on FASTSQ (J6-17). The output signal of the high pass filter (which consists of noise outside of the voice audio band in the range of 6000 to 8000 Hz) is sent to the averaging detector stage.

Noise in the 6000 to 8000 Hz band is applied to the averaging detector which consists of R83, R84, R85, R86, R87, C63, C64, C71 and U9. The noise is rectified to provide an average DC output level proportional to the noise input. A large noise level provides a larger DC output level.

The average DC level is amplified by C72, R88, R89 and U9 to produce a level ranging from 0 to 5 Volts DC. This amplifier buffers the amplified DC level to the input of the trigger.

The trigger consists of R90, R91, C73 and U9. The inverting input of U9 is referenced to BIAS (2.5 Volts DC). When the DC level exceeds 2.5 Volts the U9 trigger switches and provides a positive voltage to transistor Q11 (if enabled by transistor Q10). For a large noise component in the 6000 to 8000 Hz range, U9 saturates at the high level. The output of transistor Q11 is read by the microcomputer on AUDIOMUX U1-7) when selected (during audio mux read multiplexing).

GESTAR GENERATION

On some control unit applications, P1.6 and P1.7 of the microcomputer are used to generate GESTAR signalling (TONE) for injection into the transmit path.

HORNRING CIRCUIT

Positive Or Negative Hornring Detect
(P11 on J11-2 and J11-3)

The hornring circuit allows the software to look for either a positive (A+) active or negative (A-) active signal. PC programming denotes which polarity is the active state. Note that the audio mux line at the connector (J6-16) Must be floating, I/ODATA4 = 0, I/ODATA5 = 1 and CGRD = 1 in order to read the input.

The following describes the proper setup to read the HORNRING input correctly.

Positive active (AUDIOMUX = 1 as input):

HORNRING	P1.6	P1.7	AUDIOMUX
A+	0	1	0
float	0	1	1

Negative active (P1.7 = 1 as input):

A-	1	0	NA
float	1	1	NA

Positive Hornring Detect
(P11 on J11-1 and J11-2)

The hornring circuit allows detection of positive (A+) active hornring inputs only. The positive active input hornring is read via J6-16 floating, I/ODATA4 = 0, I/ODTAT5 = 1 and CGRD = 1. (P1.6 and P1.7 are not used.)

ELECTROLUMINESCENT (EL) PANEL DRIVER CIRCUIT

The electroluminescent (EL) panel driver is a voltage converter that transforms the SW A+ input to a 125 VRMS AC signal.

CAUTION

This transformer must be terminated in an equivalent circuit in order not to cause damage. The equivalent circuit is a 33K ohm resistor in parallel with a 0.068 F capacitor.

The intensity of the EL panel backlighting is changed by varying the duty cycle of ELBACKLT (U6-19). The duty cycle varies from 100 percent (fully on) to 0 percent (fully off) with a cycle time of about 20 milliseconds.

When ELBACKLT1 is high, transistor Q12 is turned on, thereby turning on the pass transistor Q13 which supplies SW A+ power to the EL driver U12. The EL driver accepts the SW A+ input power and generates the nominal AC power required for the EL panel on the keypad board. The EL driver U12 generates the AC power at a specified frequency.

Compensation is provided in the EL driver for degradations over time in the capacitive load of the EL panel. Resistors R114, R115, R116 and capacitors C36 and C42 provide input filtering to the EL driver.

ELBACKLT2 is not presently used (resistor R117 not installed).

MEMORY-MAPPING USING MUX U7

Refer to Table 1 which shows control unit external device memory-mapping of the microcomputer.

MEMORY ADDRESS (HEX)	PSEN	RD	WR	DEVICE ACCESSED
0000 - FFFF	0	1	1	EPROM U3
E000 - FFFF	1	0	1	EEPROM U4 (RD)
E000 - E1FF	1	1	0	EEPROM U4 (RD/WR)
0000	1	1	0	REGISTER U5
2000	1	1	0	REGISTER U6
4000	1	1	0	I/O BD IO1C
6000	1	1	0	I/O BD IO2C
8000	1	1	0	I/O BD IO3C
C000	1	1	0	I/O BD IO4C
A000	1	1	0	I/O BD 1O5C

Table 1 - Microcomputer Memory-Mapping

The upper three address lines A13, A14 and A15 (U1-26 through U1-28) are used as address inputs U7-1 through U7-3) for U7. The select CS2 line (U7-5) is decoded to prevent writing to the EEPROM U4 address above E1FF Hex. The select CS1 (U7-4) signal is the microcomputer WR (U1-18) signal that is memory mapped to address the various I/O devices (U5, U6 and IO1C through IO5C).

WRITING TO PARALLEL OUTPUT REGISTER U5 AND U6

Writing to register U5 and U6 (74HC574 OCTAL D FLIP-FLOP) is accomplished by providing data on the address bus AD0 through AD7 and then activating the Y0 or Y1 signal (WR from U7). The truth table for U5 and U6 is as follows:

OPERATING MODE	INPUTS		OUTPUTS
	Y	Dn	QN
LOAD "1"	↑	1	1
LOAD "0"	↑	0	0

↑ = Low To High Clock Transition
Dn = Logic Level Prior To Clock Transition

TEST PROCEDURES

A functional System Test Procedure for the microcomputer board consists of exercising the board using a standard "dumb" terminal. This test uses the software that is part of the microprocessor on the microcomputer board to make power and continuity checks, check the keypad/display panel and provide functional checks for the microcomputer and I/O boards.

An additional test procedure is available (where applicable) that uses the S-800 Automatic Tester. For complete information on this procedure, refer to Automatic Tester maintenance manual, LBI-38166.

FLASH PROGRAMMING

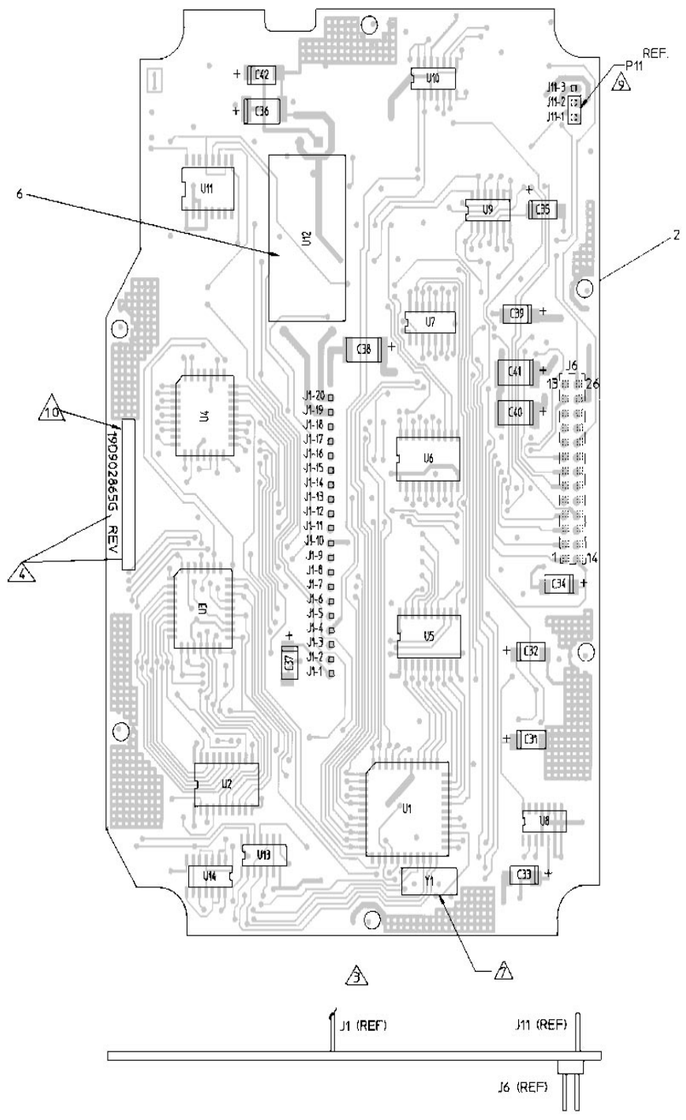
The microcomputer board is capable of receiving future software upgrades and feature enhancements via flash programming of the EPROM U3.

This is accomplished by raising the EEWREN line (6-14) to +12 Volts. The +12 Volts is routed to the flash EPROM (3-1) and to the voltage divider R65/R66. The PFI input of the watchdog timer (U11-9) compares the level of the EEWREN line to be above 8.6 Volts. When EEWREN exceeds 8.6 Volts, the PFO output (U11-10) goes high. This places the microcomputer in the bootrom mode of operation. In this mode, the microcomputer can program the flash memory U3 via a proprietary serial communications protocol. Comparators U10.3 and U10.4 generate a reset pulse whenever the PFO output of U11 goes from a high to a low or vice-versa. The comparators use the transition region at about 1.6 to 3.3 to generate a reset out. Resistor R45 and capacitor C12 slow the edge at PFO so that the comparators can generate a reset pulse of at least 5 microseconds in duration.

PC PROGRAMMING

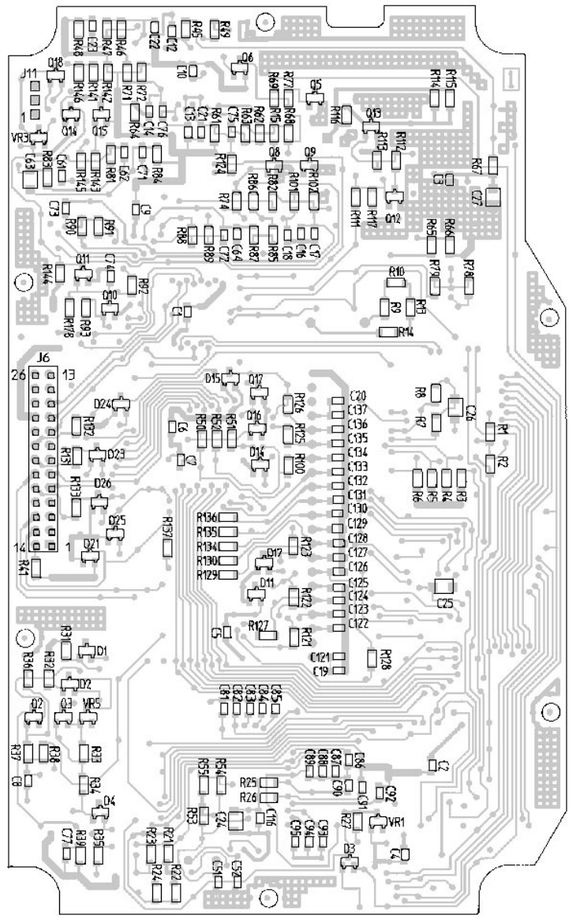
PC Programming of the U4 EEPROM is accomplished via the PC Programmer cable and TQ3310 Serial Programming Adapter. Programming of all locations of the EEPROM is executed through a proprietary serial communications protocol. The PC Programmer cable grounds the EEWREN to enable writing to any address location of the U4 EEPROM.

COMPONENT SIDE



(19D902865, Sh. 1, Rev. 4)
(19D902866, Layer 1, Rev. 1))

SOLDER SIDE



(19D902865, Sh. 1, Rev. 4)
(19D902866, Layer 4, Rev. 1))

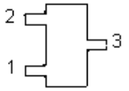
J11/P11 JUMPER CHART		
POSITION	FUNCTION	GROUPS
1 AND 2	POSITIVE HORN RING	4
2 AND 3	POSITIVE OR NEGATIVE HORN RING DETECT	1&3

R53, R54, R55, R78, R91, R117 NOT USED IN GROUPS 1 & 3.

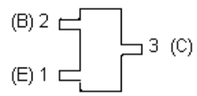
THE FOLLOWING ITEMS ARE MOS DEVICES REQUIRING SPECIAL CARE: U1-U8, U11, U13 AND U14.

CAUTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES

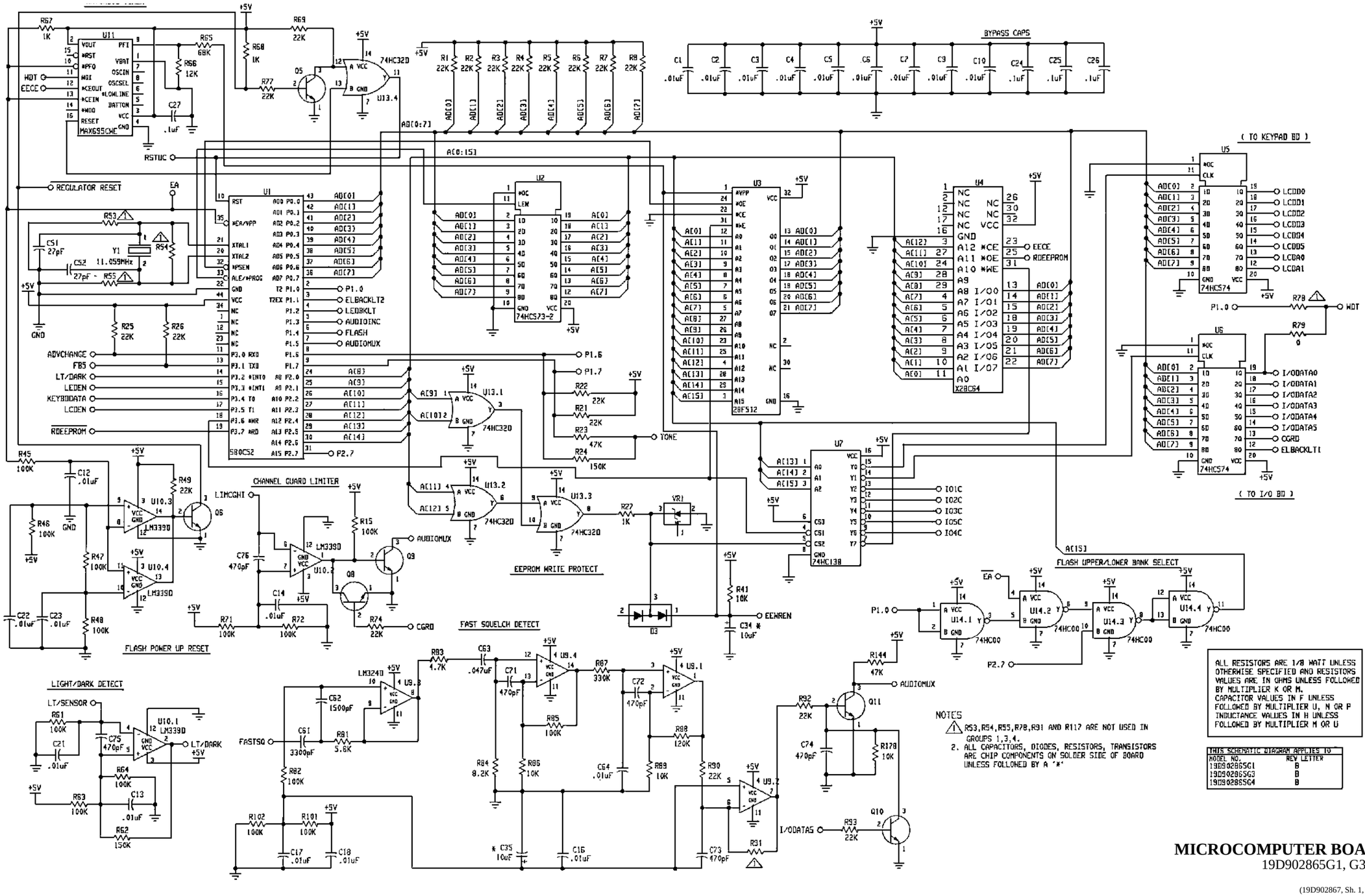
LEAD IDENTIFICATION FOR
D1, D2, D4, D11, D12, D14, D15,
D21, D23-D26, VR1, VR3, AND VR5
(SOT) DIODES
(TOP VIEW)



LEAD IDENTIFICATION FOR
Q1, Q2, Q3, Q5, Q6, AND Q8 - Q18
(SOT) TRANSISTORS
(TOP VIEW)

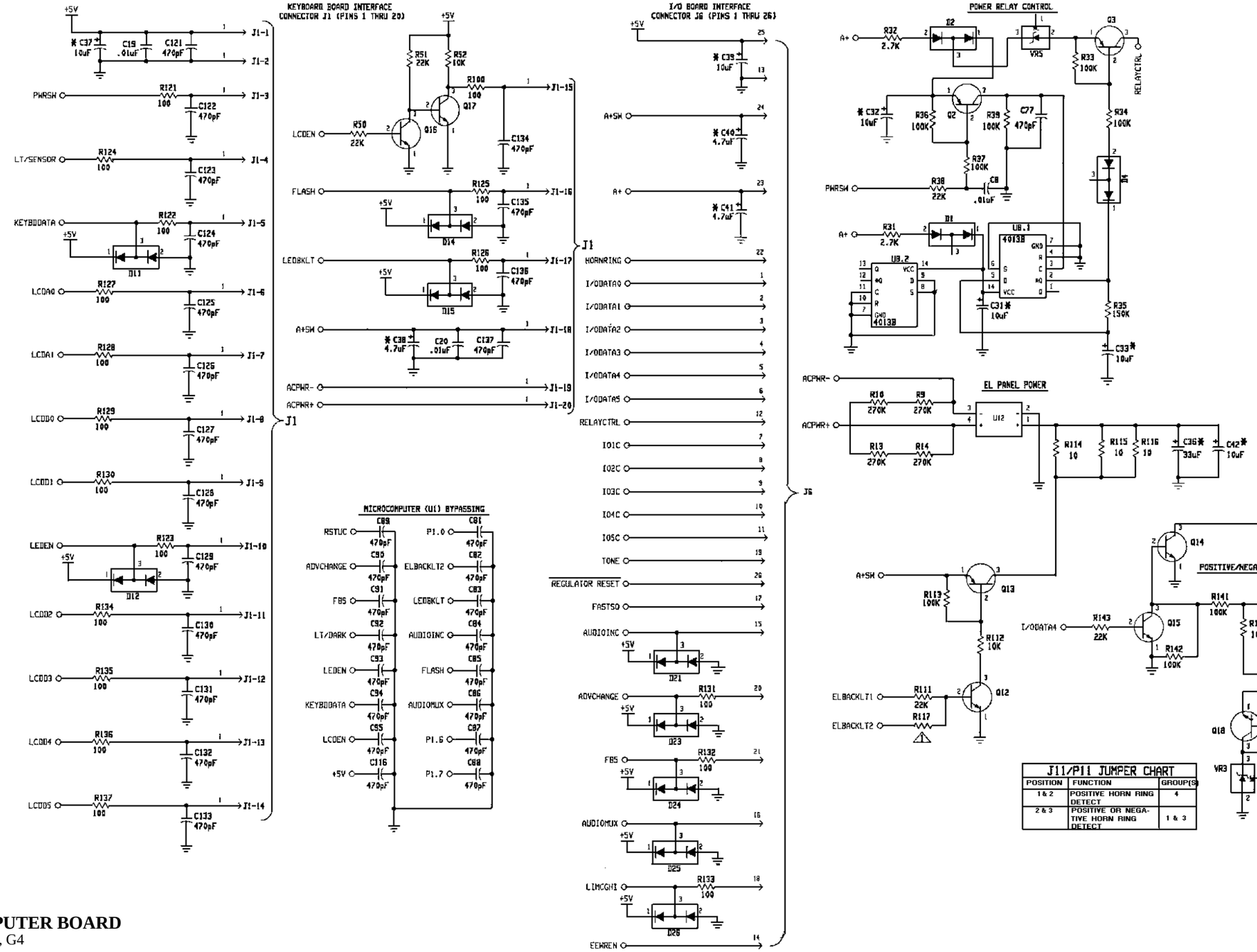


MICROCOMPUTER BOARD
19D902865G1, G3,G4



MICROCOMPUTER BOARD
19D902865G1, G3, G4

(19D902867, Sh. 1, Rev. 2)



MICROCOMPUTER BOARD
19D902865G1, G3, G4

(19D902867, Sh. 2, Rev. 1)

MICROCOMPUTER BOARD
19D902865G1, G3, G4
ISSUE 1

SYMBOL	GE PART NO.	DESCRIPTION
		- - - - - - - - - CAPACITORS - - - - - - - - -
C1 thru C10	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C12 thru C14	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C16 thru C23	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C24 thru C27	19A702052P26	Ceramic: 0.1 uF ±10%, 50 VDCW.
C31 thru C35	19A705205P6	Tantalum: 10 uF ±20%, 16 VDCW; sim to Sprague 293D.
C36	19A705205P15	Tantalum: 33 uF ±20%, 16 VDCW; sim to Sprague 293D.
C37	19A705205P6	Tantalum: 10 uF ±20%, 16 VDCW; sim to Sprague 293D.
C38	19A705205P18	Tantalum: 4.7 uF ±20%, 35 VDCW; sim to Sprague 293D.
C39	19A705205P6	Tantalum: 10 uF ±20%, 16 VDCW; sim to Sprague 293D.
C40 and C41	19A705205P18	Tantalum: 4.7 uF ±20%, 35 VDCW; sim to Sprague 293D.
C42	19A705205P6	Tantalum: 10 uF ±20%, 16 VDCW; sim to Sprague 293D.
C61	19A702052P8	Ceramic: 3300 pF ±10%, 50 VDCW.
C62	19A702052P6	Ceramic: 1500 pF ±10%, 50 VDCW.
C63	19A702052P22	Ceramic: 0.047 uF ±10%, 50 VDCW.
C64	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C71 thru C77	19A702052P3	Ceramic: 470 pF ±10%, 50 VDCW.
C81 thru C95	19A702052P3	Ceramic: 470 pF ±10%, 50 VDCW.
C116	19A702052P3	Ceramic: 470 pF ±10%, 50 VDCW.
C121 thru C137	19A702032P3	Ceramic: 470 pF ±10%, 50 VDCW.
		- - - - - - - - - - DIODES - - - - - - - - - -
D1 and D2	19A700053P2	Silicon: 2 diodes in series; Sim to BAV99.
D3	19A705377P4	Silicon: Hot Carrier, 70 PiV; sim to Siemens BAS70-04.
D4	19A700053P2	Silicon: 2 diodes in series; sim to BAV99.
D11 and D12	19A700053P2	Silicon: 2 diodes in series; sim to BAV99.
D14 and D15	19A700053P2	Silicon: 2 diodes in series; sim to BAV99.
D21	19A700053P2	Silicon: 2 diodes in series; sim to BAV99.
D23 thru D26	19A700053P2	Silicon: 2 diodes in series; sim to BAV99.
		- - - - - - - - - - JACKS - - - - - - - - - -
J1	19A703248P15	Post: Gold Plated, 21 mm length.
J6	19A702333P54	Connector, printed wiring, two part: 26 pins, rated 1 amp; sim to Dupont 78207-110.
J11	19A703248P11	Post: Gold Plated, 10 mm length.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

SYMBOL	GE PART NO.	DESCRIPTION
		- - - - - - - - - - PLUGS - - - - - - - - - -
P11	19A702104P2	Connector: 2 Position Shorting, Gold Plated; sim to Berg 65474-003.
		- - - - - - - - - TRANSISTORS - - - - - - - - -
Q2 and Q3	19A700059P2	Silicon, NPN: sim to MMBT3906.
Q5 and Q6	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q8 thru Q12	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q13	19A703197P2	Silicon, PNP: sim to MMBT4403, low profile.
Q14 thru Q18	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
		- - - - - - - - - RESISTORS - - - - - - - - -
R1 thru R8	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R9 and R10	19B800607P274	Metal film: 270K ohms ±5%, 1/8 w.
R13 and R14	19B800607P274	Metal film: 270K ohms ±5%, 1/8 w.
R15	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R21 and R22	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R23	19B800607P473	Metal film: 47K ohms ±5%, 1/8 w.
R24	19B800607P154	Metal film: 150K ohms ±5%, 1/8 w.
R25 and R26	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R27	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R31 and R32	19B800607P272	Metal film: 2.7K ohms ±5%, 1/8 w.
R33 and R34	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R35	19B800607P154	Metal film: 150K ohms ±5%, 1/8 w.
R36 and R37	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R38	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R39	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R41	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R45 thru R48	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R49 thru R51	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R52	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R61	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R62	19B800607P154	Metal film: 150K ohms ±5%, 1/8 w.
R63 and R64	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R65	19B800607P683	Metal film: 68K ohms ±5%, 1/8 w.
R66	19B800607P123	Metal film: 12K ohms ±5%, 1/8 w.
R67 and R68	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R69	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R71 and R72	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.

SYMBOL	GE PART NO.	DESCRIPTION
R74	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R77	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R79	19B800607P1	Metal film: Zero ohms ±5%, 1/8 w.
R81	19B800607P562	Metal film: 5.6K ohms ±5%, 1/8 w.
R82	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R83	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R84	19B800607P822	Metal film: 8.2K ohms ±5%, 1/8 w.
R85	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R86	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R87	19B800607P334	Metal film: 330K ohms ±5%, 1/8 w.
R88	19B800607P124	Metal film: 120K ohms ±5%, 1/8 w.
R89	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R90	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R92 and R93	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R100	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R101 and R102	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R111	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R112	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R113	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R114 thru R116	19B800607P100	Metal film: 10 ohms ±5%, 1/8 w.
R121 thru R137	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R141 and R142	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R143	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R144	19B800607P473	Metal film: 47K ohms ±5%, 1/8 w.
R145	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R146	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R178	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
		- - - - - - - INTEGRATED CIRCUITS - - - - - -
U1	19A705557P6	Digital: CMOS 8-Bit Microcomputer; sim to Harris 1880C52.
U2	19A703471P318	Digital: CMOS Octal 3-State Non-Inv Latch; sim to 74HC573-2.
U3	19A705710G15	EPROM KIT (Flash Memory). (Used in Group 1).
U3	19A149935G4	EPROM KIT (Flash Memory). (Used in Group 3).
U3	19A705963P2	EPROM: CMOS 512K(64 x 8) Flash Memory; sim to Intel N28F512-200 PIC4. (Used in Group 4).
U4	19A149755P2	EEPROM: CMOS 8K x 8; sim to Xicor X28C64.
U5 and U6	19A704380P316	Digital: CMOS Octal Data Flip-Flop; sim to 74HC574.
U7	19A703471P320	Digital: CMOS 3 to 8 Line Decode/Demux; sim to 74HC138.
U8	19A700029P509	Digital: CMOS Dual Data Flip-Flop; sim to 4013B.
U9	19A702293P1	Linear: Quad Op Amp; sim to LM324D.
U10	19A704125P1	Linear: Quad Voltage Comparator; sim to LM339D.
U11	19A149895P1	Digital: CMOS Supervisory Circuit; sim to MAX691C.
U12	19A149417P2	Driver, Electroluminescent; sim to Endicott Research E746.
U13	19A703483P311	Digital: CMOS Quad 2-Input OR Gate; sim to 74HC32D.
U14	19A703483P302	Digital: CMOS Quad 2-Input NAND Gate; sim to 74HC00.

SYMBOL	GE PART NO.	DESCRIPTION
		- - - - - - - VOLTAGE REGULATORS - - - - - - -
VR1	19A700083P101	Silicon, Zener; 4.7 Volts; sim to BZx84-C4V7.
VR3	19A700083P101	Silicon, Zener; 4.7 Volts; sim to BZx84-C4V7.
VR5	19A700083P101	Silicon, Zener; 4.7 Volts; sim to BZx84-C4V7.
		- - - - - - - - - CRYSTALS - - - - - - - - -
Y1	19A702511G15	Quartz: 11.059200 MHz.
		- - - - - - - - MISCELLANEOUS - - - - - - - -
	19A701316P1	Plate, Insulating. (For Crystal Y1.)

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

REV. A - MICROCOMPUTER BOARD 19D903865G1
REV. A - MICROCOMPUTER BOARD 19D903865G3
REV. A - MICROCOMPUTER BOARD 19D903865G4
This revision removed pull-up resistor R144 to adjust voltage drop due to analog mux on the I/O Board.

R144 was 19B800607P103 - Metal film, 10K ohms ±10, 1/8 w.

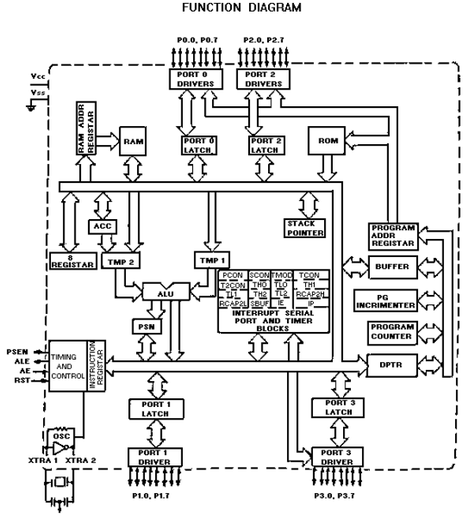
REV. B - MICROCOMPUTER BOARD 19D903865G1
REV. B - MICROCOMPUTER BOARD 19D903865G3
REV. B - MICROCOMPUTER BOARD 19D903865G4
This revision added pull-up resistor R144 (19B800607P473, 47K ohms) to insure sufficient pull-up current for U1-7 (AUDIOMUX).

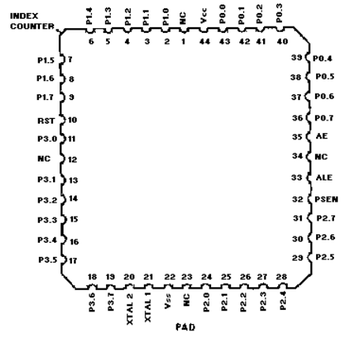
This revision also changed Flash Memory EPROM U3 software to 19A705710G15 on the 19D902865G1 board and to 19A149935G4 on the 19D902865G3 board to correct T99 tone interdigit time.

U3 was 19A705710G14 - EPROM KIT. (Group 1).

U3 was 19A149935G3 - EPROM KIT. (Group 3).

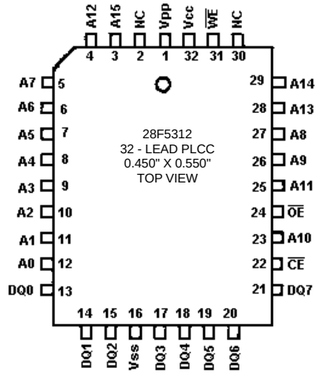
MICROCOMPUTER U1
19A705557P6

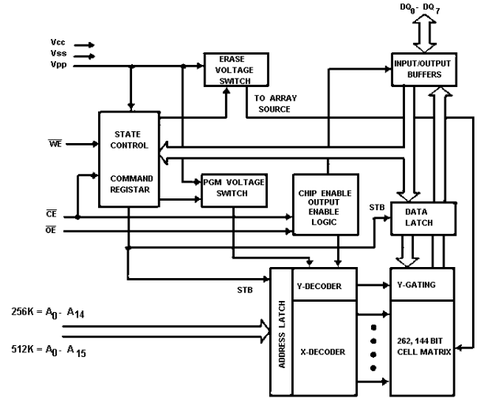




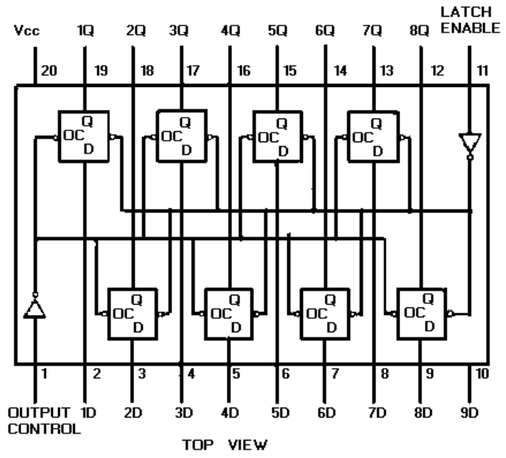
VSS	CIRCUIT GROUND POTENTIAL
VCC	+5V POWER SUPPLY
PORT 0	8—BIT OC BI-DIRECTIONAL I/O PORT.
PORT 1	8—BIT QUASI-BIDIRECTIONAL I/O PORT.
PORT 2	8—BIT QUASI-BIDIRECTIONAL I/O PORT.
PORT 3	8—BIT QUASI-BIDIRECTIONAL I/O PORT.
3.0	RXD — SERIAL PORT RECEIVER DATA.
3.1	TXD — SERIAL PORT TRANSMITTER DATA.
3.2	INT0 — INTERRUPT 0 INPUT.
3.3	INT1 — INTERRUPT 1 INPUT.
3.5	T1 — COUNTER 1 INPUT.
3.6	WR — WRITE CONTROL.
3.7	RD — READ CONTROL.
RST	RESET.
ALE	ADDRESS LATCH ENABLE.
PSEN	PROGRAM STORE ENABLE OUTPUT.
EA	INTERNAL/EXTERNAL INSTRUCTION FETCH.
XTAL1	INPUT TO OSCILLATOR AMPLIFIER.
XTAL2	OUTPUT FROM OSCILLATOR AMPLIFIER.

EPROM U3
19A705963P2





OCTAL-NONINVERT LATCH U2
19A703471P318



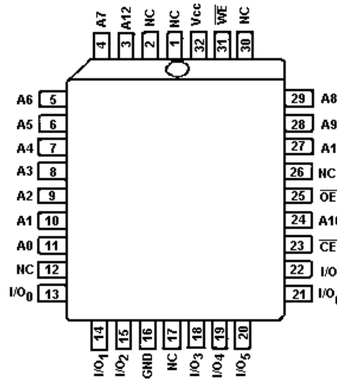
TRUTH TABLE

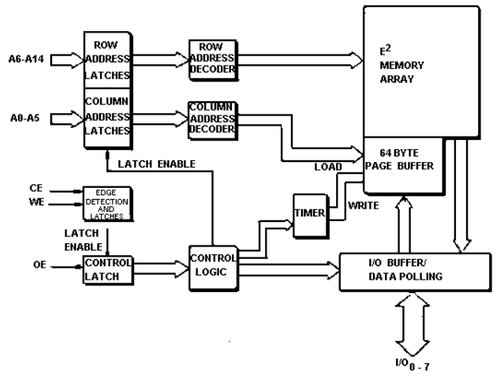
Output Control	Latch Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level
Q_0 = level of output before steady-state input conditions were established.
Z = high impedance
X = Don't care

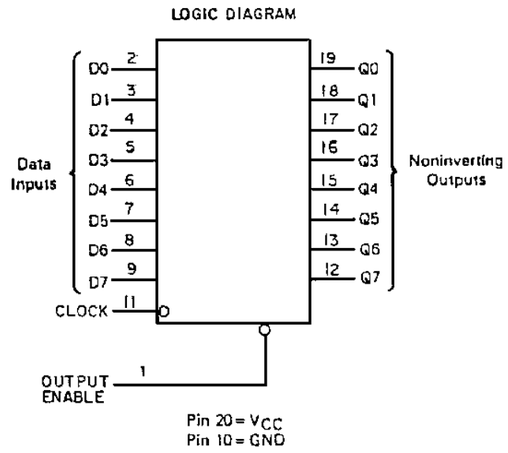
EEPROM U4
19A149755P2

PLASTIC LEADED CHIP CARRIER
TOP VIEW





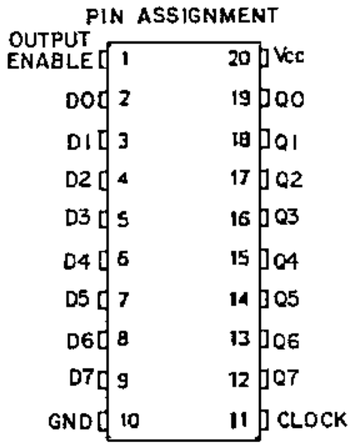
LOGIC DIAGRAM



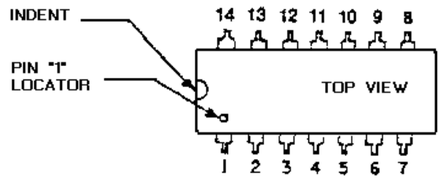
Pin 20 = V_{CC}
Pin 10 = GND

OCTAL DTA FLIP-FLOP U5 & U6
19A704380P316

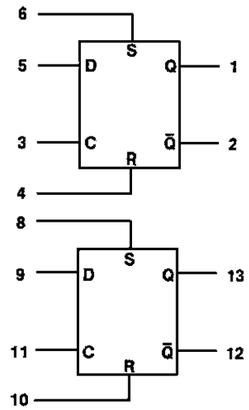
PIN ASSIGNMENT



PIN CONFIGURATION

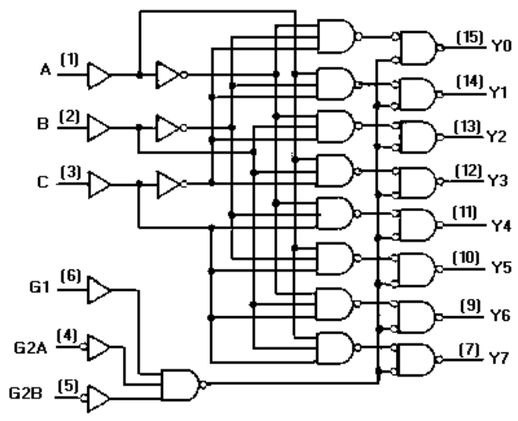


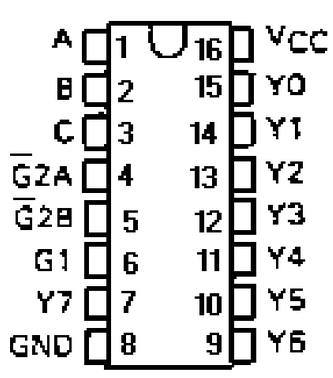
DUAL DATA FLIP-FLOP U8
19A700029P509



V_{DD} = PIN 14
V_{SS} = PIN 7

DECODE/DEMUX U7
19A703471P320

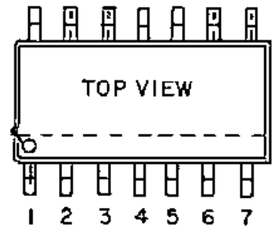


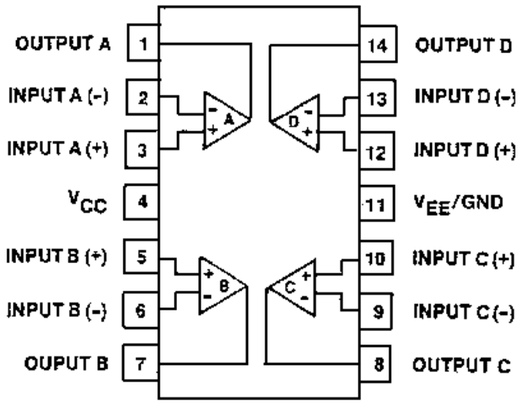


FUNCTION TABLE

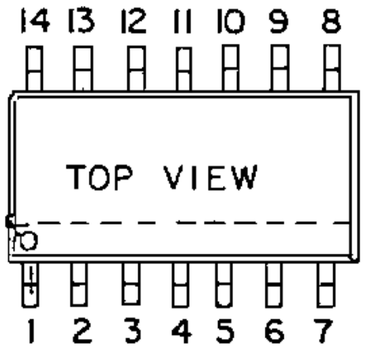
ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

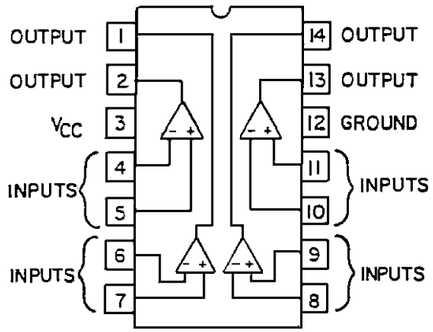
OPERATIONAL AMPLIFIER U9
19A702293P1



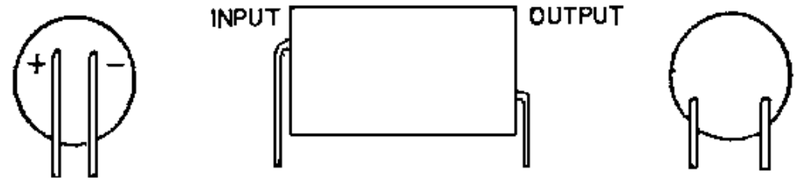


VOLTAGE COMPARATOR U10
19A704125P1

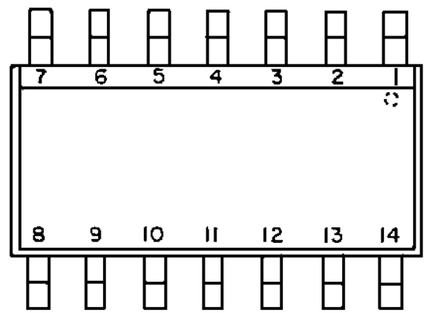


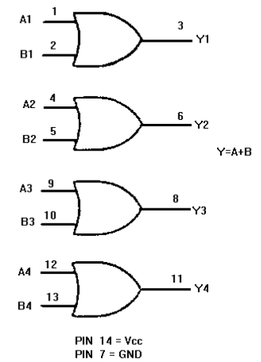


ELECTROLUMINESCENT DRIVER U12
19A149417P2

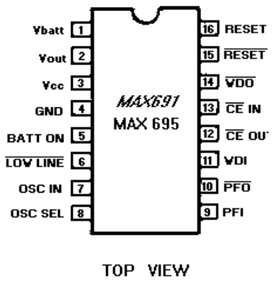


LOGIC OR GATE U13
19A703483P311

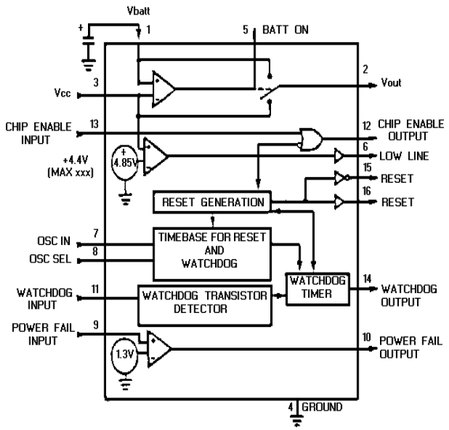




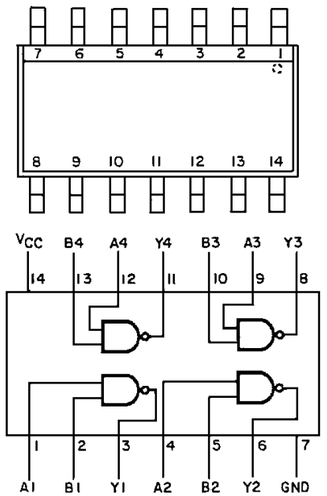
SUPERVISORY CIRCUIT U11
19A149895P1



TOP VIEW



LOGIC HAND GATE U14
19A703483P302



LBI-38726

This page intentionally left blank