

# MAINTENANCE MANUAL FOR 403-500 MHz PERSONAL TWO-WAY FM RADIO COMBINATION

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## INTRODUCTION

The recommended troubleshooting procedure, as illustrated in Figure 1, is to isolate the fault to a specific section of the M-RK Personal radio; the radio section; the logic section or the battery pack. Then further localize the fault to a specific stage of the suspected section. The last step is to isolate and identify the defective component.

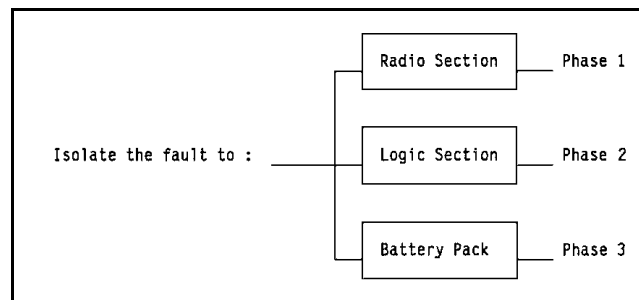


Figure 1 - Recommended Troubleshooting Procedure

The following list of test equipment is recommended when servicing or troubleshooting the M-RK Personal Radio.

Recommended Test Equipment :

- Audio Analyzer
- Digital Voltmeter
- DC Power Supply
- Multimeter
- Oscilloscope

Servicing Setup

The servicing setup is shown in Figure 1A. This illustrates the test boxes, cables, etc. required when the M-RK needs to be disassembled for troubleshooting or servicing.

Maintenance/Warranty

1. Repair and Return is available at Authorized Service Centers (ASC) or at Ericsson Inc., in Lynchburg, VA.

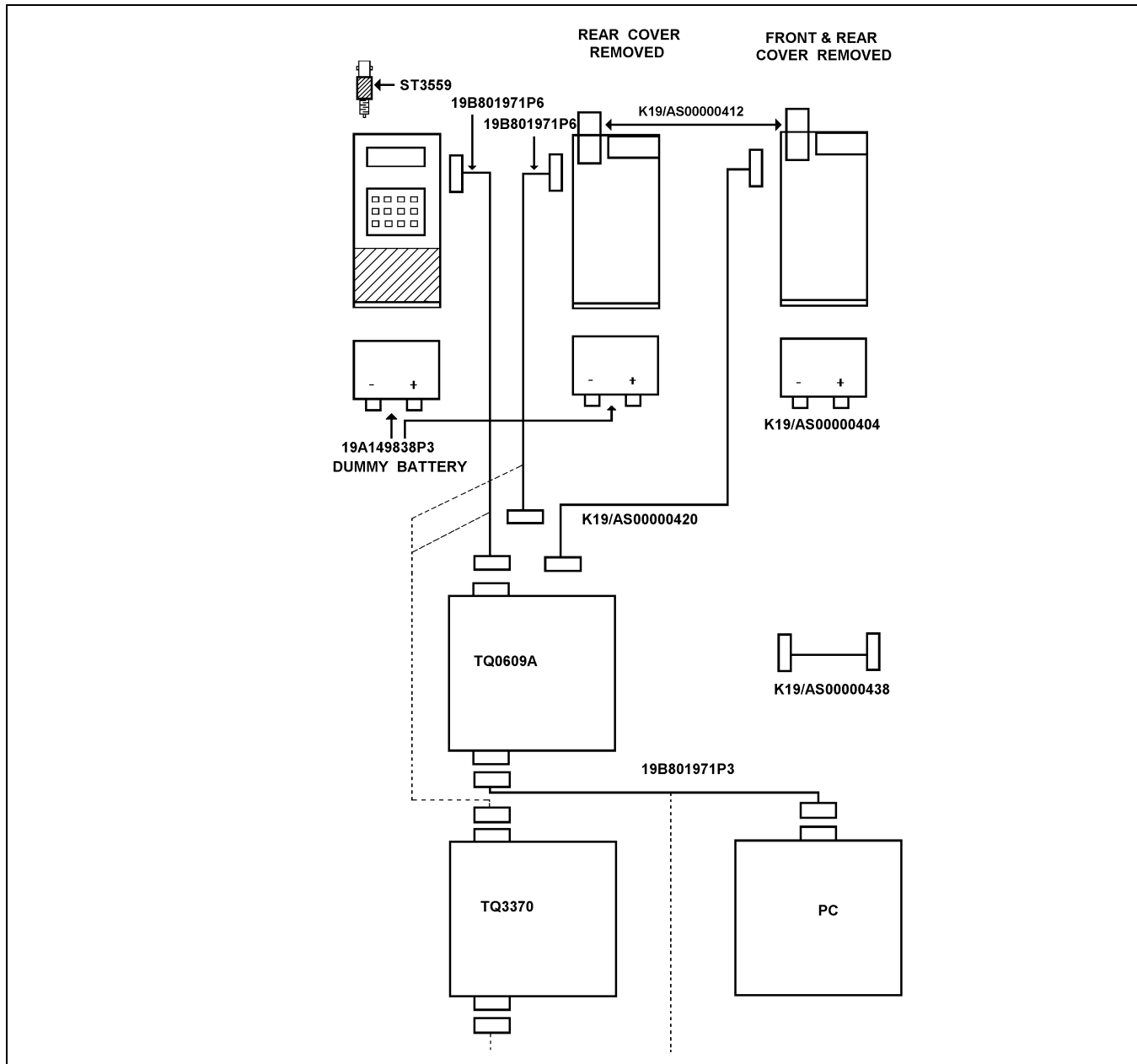


Figure 1A - Servicing Setup

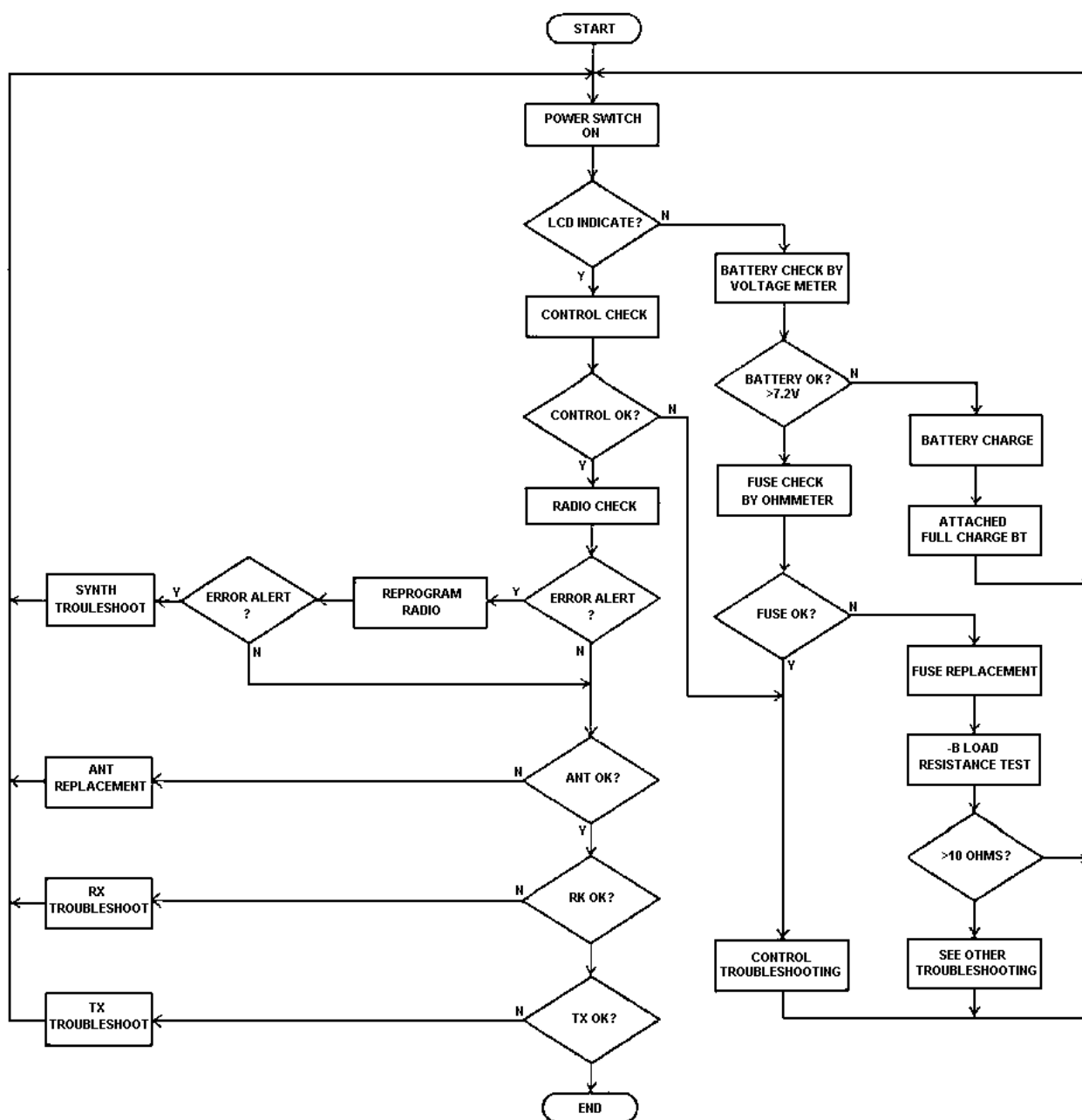
2. Board level Repair and Return is recommended. Servicing to component level is not recommended.
3. Parts and components available through Service Parts are shown and listed in LBI-38746. When ordering replacement parts, please add the prefix "K19/" to the listed part number.
4. Standard warranty (3 months labor, 12 months parts) applies. Option PKCSIP extends labor warranty to 12 months.

## PHASE 1 : RADIO SECTION TROUBLESHOOTING

### Functional Troubleshooting

Once the fault has been isolated to the radio section, the next step is to further isolate the fault to a specific stage of the radio section; Frequency Synthesizer (SYN), Receive (RX) and Transmit (TX). The flowchart (See Page 2) will assist in isolating the fault to a specific stage of the radio section.

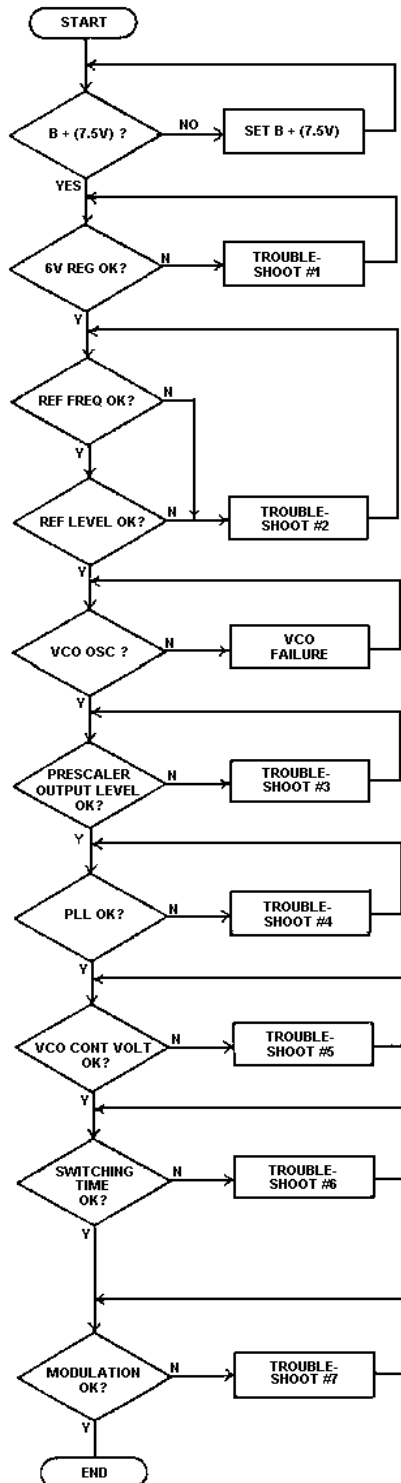
### Functional Troubleshooting Flowchart:



## SYNTHESIZER

The following flowchart can be used to isolate a defective stage in the synthesizer circuit.

Synthesizer Flowchart:



### Troubleshooting for the Synthesizer :

#### 1. 6.0 Volt Regulator

The 6.0 volt regulator consists of regulator U6 and transistor Q105. If a fault is found with the regulated 6.0 volt output line, trace the fault source along this line back to the regulator. A typical current flowing is 30 mA. Typical voltages for the synthesizer are shown in Table 1.

Any repair should be made so that the current and voltage at each assembly and component agrees with the typical value.

#### 2. Reference Oscillator VCTCXO (Z1)

The reference oscillator is contained in one assembly. Typical data, when the reference oscillator is working properly, is shown in Table 2.

Table 2 - Typical Data For The Reference Oscillator

Item	Typical Value	Remarks
Supply Voltage	5.3 Vdc	
Current Drain	1.5 to 1.8 mA	5 PPM (UHF/UHF) 1.5 PPM (800/900 MHz)
Output Frequency	13.2 MHz	
Output Level	1 to 2 Vp-p	

#### 3. Prescaler Output Level

VCO U5 has an output level of about 0 dBm. Part of the VCO output is applied to the input of buffer amplifier transistor Q101 through a capacitor. After amplification, the output is applied to the input of the Prescaler, which is operating under 128/129 modulus control. A typical prescaler output level is 1 volt p-p, which is applied to the input of the PLL.

When checking the prescaler, refer to the typical value on Table 1.

#### 4. Phase-Lock-Loop (U2)

- Check for approximately 1 to 2 volts p-p reference signal input at Pin 2 of U2.
- Check that the reference signal frequency is 13.2 MHz and that frequency stability is  $\pm 5$  PPM.(VHF/UHF)( $\pm 1.5$  PPM (800/900 MHz)).

- c. Measure the input from the prescaler at Pin 10 of U2 and verify approximately 1 volt p-p input level.
- d. Verify that approximately 5 volts p-p (Vss-Vcc) control pulse is present at Pin 8 of prescaler control U2.
- e. Cause the PLL to unlock. Then check for the presence of approximately 5 volts p-p (Vss-Vcc) PD and FD pulse outputs at Pin 6 and Pin 17 of U2 respectively. Also check for approximately 6 volts p-p (Vss+B) at Pin 1 of U4. If the pulse output is absent or shifted to either the Vss or the Vcc side, the PLL may fail to lock over a certain section of the frequency range or the entire range. If this fault occurs, the possible trouble source is ramp resistor R111, ramp capacitor C131 or hold capacitor C132.
- f. Verify that the local voltages at the test points listed on Table 1 agree with the typical values also listed on Table 1.
- g. Verify that the CLOCK, DATA, ENABLE and WIDE/NARROW signals coming from the Control Board are at the proper level and the proper duration (refer to Figure 2).

If the CLOCK and DATA are improper, the PLL operation will become erratic. If the duration of the W/N pulse is shorter than 10 milliseconds, which is the minimum value, the PLL may fail to lock.

#### NOTE

If parts other than those specified in the parts list are used in the associated circuit of the PLL, the switching time may be affected. Whenever any parts are replaced in the associated circuit, check the switching time.

Table 1 - Synthesizer Portion Typical Voltages - UHF

No.	Test Points	Voltage (V)	Remarks
1	U1 (1)	3.0	
2	U1 (2)	5.3	
3	U1 (3)	0 (GND)	
4	U1 (4)	1.2p-p	V <sub>L</sub> : 3.2, V <sub>H</sub> : 4.4
5	U1 (5)	0 (GND)	
6	U1 (6)	4.8p-p	V <sub>L</sub> : 0.6, V <sub>H</sub> : 5.4
7	U1 (7)	—	
8	U1 (8)	3.0	
9	U2 (1)	4.4	
10	U2 (2)	1.6p-p	V <sub>L</sub> : 1.6, V <sub>H</sub> : 3.2
11	U2 (5) (19)	5.6	
12	U2 (6) (17)	0.9(RX), 1.0(Tx)	at 403 MHz
13	U2 (8)	4.8p-p	V <sub>L</sub> : 0.6, V <sub>H</sub> : 5.4
14	U2 (9)	5.5	
15	U2 (10)	1.2p-p	V <sub>L</sub> : 1.8, V <sub>H</sub> : 3.0
16	U2 (11)	0	
17	U2 (12)	0	
18	U2 (13)	0	
19	U2 (15)	1.6o-p(Rx), 1.7o-p(Tx)	at 403 MHz
20	U2 (18)	0.2p-p	V <sub>L</sub> :1.6,V <sub>H</sub> :1.8(Rx), V <sub>L</sub> :1.8,V <sub>H</sub> :2.0(Tx),
21	U2 (20)	4.2	
22	Z1 (3)	5.2	
23	U4 (1)	1.1(Rx), 1.3 (Tx)	at 403 MHz
24	U4 (2)	0.9(Rx), 1.0 (Tx)	
25	U4 (3)	0.9 (Rx), 1.0(Tx)	at 403 MHz
26	U4 (4) (5)	0 (GND)	
27	U4 (6)	0 (GND)	
28	U4 (7)	—	
29	U4 (8)	7.4	

No.	Test Points	Voltage (V)	Remarks
30	U3 (9) (10)	1.1(Rx), 1.3(Tx)	at 403 MHz (Hi impedance)
31	U3 (8) (11)	1.1(Rx), 1.3(Tx)	at 403 MHz
32	U3 (6) (12)	0	
33	U3 (5) (13)	0 (GND)	
34	U3 (7)	0 (GND)	
35	U3 (2) (3)	0 (GND)	
36	U3 (1) (4)	0 (GND)	
37	U3 (14)	6.0	
38	U5 (1)	0.1 (Rx, 3.9(Tx)	
39	U5 (3)	0	
40	U5 (4)	5.2	
41	U5 (5)	0	
42	U5 (7)	5.0(Rx), 0.2(Tx)	
43	U5 (10)	5.1	
44	U5 (12)	1.1(Rx), 1.3(Tx)	at 403 MHz (Hi impedance)
45	U5 (2) (6) (8) (9) (11) (13) (14)	0 (GND)	
46	Q101 Base	1.4	
47	Q101 Emitter	0.6	
48	Q101 Collector	6.0	
49	Q102 (1)	5.0 (Rx), 0.2(Tx)	
50	Q102 (2) (3)	0.1(Rx), 3.9(Tx)	
51	Q102 (4)	5.0 (Rx), 0(Tx)	
52	Q103 (5) (6)	0 (GND)	
53	Q103 Base	1.2	
54	Q103 Emitter	0.6	
55	Q103 Collector	6.7	
56	Q105 (1)	0 (GND)	
57	Q105 (2)	7.5	
58	Q105 (3)	0	

No.	Test Points	Voltage (V)	Remarks
59	Q106 Base	5.8	
60	Q106 Emitter	5.2	
61	Q106 Collector	6.0	
62	Q107 Base	7.4	
63	Q107 Emitter	6.8	
64	Q107 Collector	7.5	

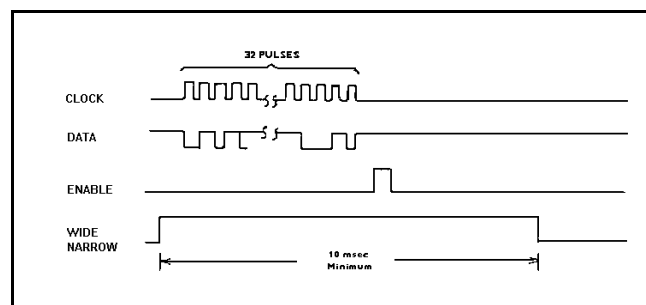


Figure 2 - Clock, Data, Enable, and Wide/Narrow Signals

## 5. VCO Control Voltage

### a. VCO Control Voltage should be

- Approximately 1 volt or more at the lowest channel of any band.
- Approximately 4.5 volts or less at the highest channel of any band.

Verify the VCO control voltage at the testpoint TPPD using a high impedance oscilloscope.

## 6. Switching Time

The channel frequency must be locked within 10 milliseconds, which is the duration of the Wide/Narrow pulse. That is, the switching time is restricted by the Wide/Narrow pulse.

- ### a. Switching time is largely influenced by the leakage current characteristics of C133 and C152. Be sure to use parts having the ratings specified on the Parts List when replacing these parts. Also, if moisture collects on the printed wire board, the insulation resistance of the board may be lowered, also affecting the switching time.

- b. The channel switching sequence and the action of the related functions are shown in figure 3.

#### 7. Modulation Degree vs Modulation flatness :

The M-RK equipment can be modulated with audio beginning with 10 Hz. For this reason, the same modulation signal is applied to both VCO and VCTCXO in phase. The modulation signal of low frequencies below 10 to 30 Hz, modulates the VCTCXO output whereas the high frequency signals modulate the VCO. Modulation characteristics can be adjusted using modulation adjust controls R120 and R121 as follows :

#### NOTES

1. Modulation flatness is to be adjusted with the radio section only. This means that the TX MOD signal which exits the control board at P1-2B must be disconnected from where it normally enters the radio board at J1-2B. Using an external audio signal generator, inject an audio signal into the radio board at J1-2B. The recommended method would be to use Extender Cable K19/AS00000438 to separate the control board from the radio board, open-circuit the wire that connects P1-2B to J1-2B, and inject the audio signal directly into J1-2B.
2. For this adjustment, select the center channel.

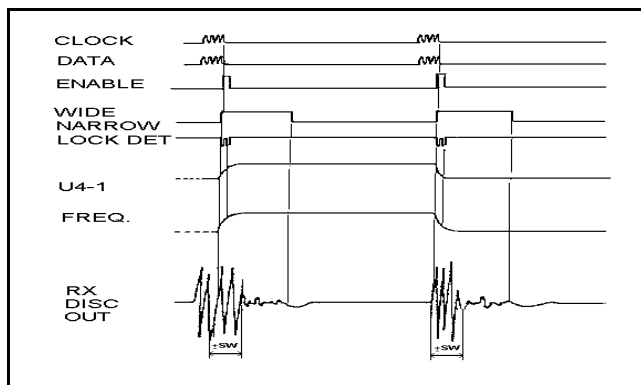


Figure 3 - Channel Switching Sequence

1. Apply a 0.45 Vrms signal at 1 kHz to the radio board TX MOD input at J1-2B and adjust R121 for  $\pm 3$  kHz deviation.
2. Change the signal frequency to 10 Hz. Adjust R120 for  $\pm 3$  kHz deviation.

3. Change the signal to a 10 Hz rectangular waveform signal. Then, the demodulated output from the modulation analyzer should look like figure 4. If the level adjustments under step 1 and 2 are out of balance, the rectangular waveform will be distorted (refer to figure 4).

#### NOTE

For this test, the modulation analyzer must have low frequency response to less than 1 Hz.

4. Change the carrier frequency to the highest channel of the band and then to the lowest channel. Check the modulation flatness each time (refer to Figure 5).

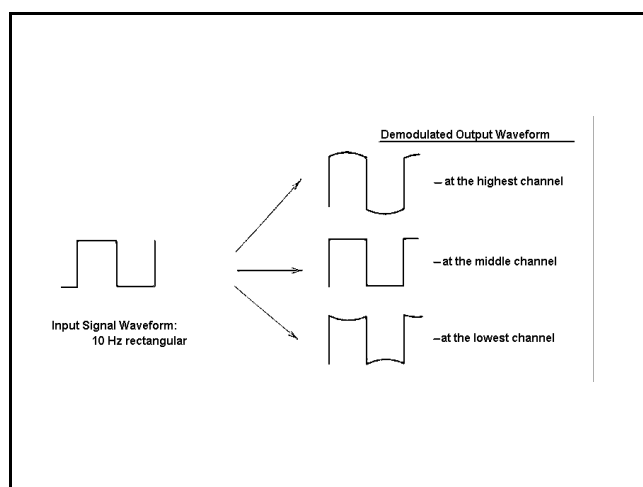


Figure 4 - Typical Rectangular Waveform of Demodulated Output

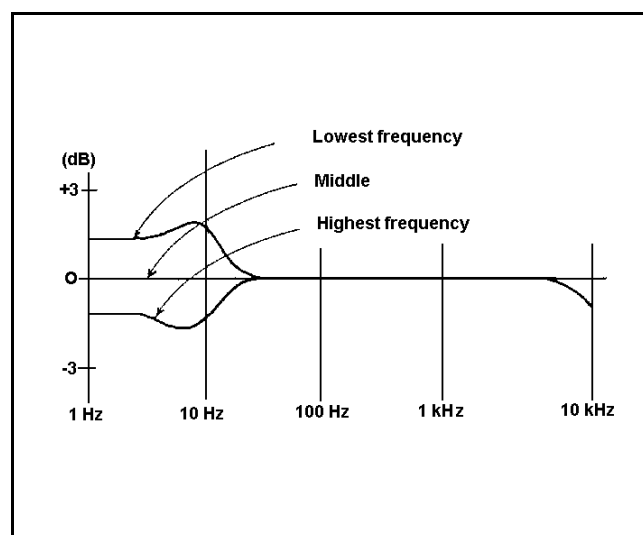


Figure 5 - Typical Modulation Frequency Characteristics

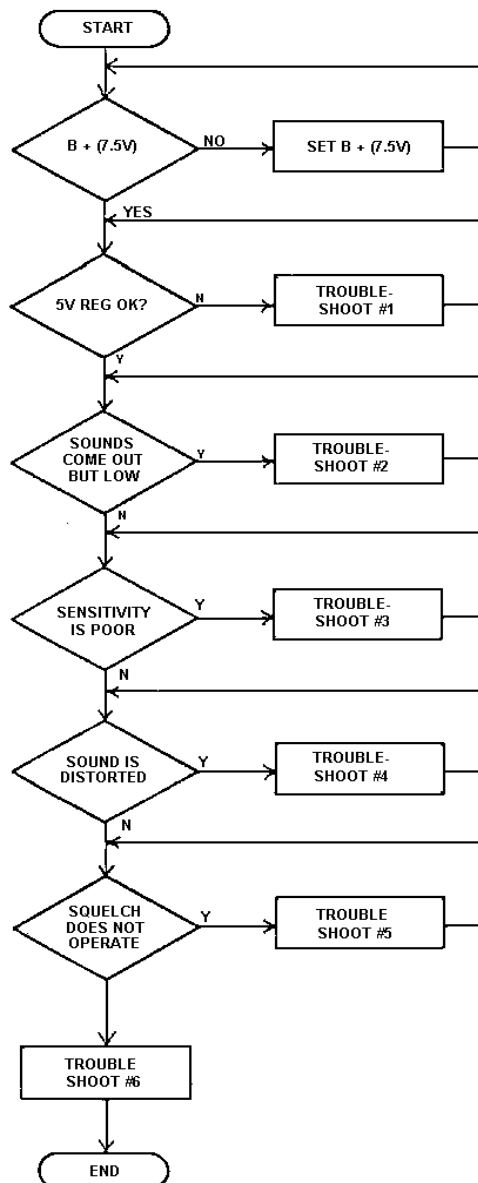
If a large level difference is found between the modulation characteristics at 10 Hz and those at 100 Hz when the carrier frequency is changed from the highest to the lowest, the problem is with the VCO modulation characteristics.

When the waveform of the demodulated output is distorted for a modulation frequency of 10 Hz or lower, the problem is with the VCTCXO. If the distortion is substantial, the carrier frequency may be affected by modulation.

### Receive

The following flowchart can be used to isolate a defective stage in the receive circuit.

Flowchart:



### Troubleshooting for the Receiver :

1. Measure the voltage of U10 input and output. If the voltage of U10 input is 7.5 V and the voltage of U10 output is not 5 +0.2V, U10 (voltage regulator) is probably no good.
2. If sound comes out of the receiver, but the volume does not increase, the problem may be due to either the Radio section or the Logic section.
  - a. Radio Section : Check the output signal for about 280 mVp-p at the audio terminal of the RX section (J1 Pin 3B) when a standard modulated signal (1 kHz at 3.0 kHz frequency deviation) of 0.5mVrms (-53 dBm) is supplied at the antenna terminal or UDC RF Connector. If the signal level at the audio terminal of the Rx is substantially low after return R312, IC U11 is suspected to be defective.
  - b. Control Board : The receive RF signal comes into P1, Pin 3B. The signal is then applied through a 14dB amplifier, 300-3000Hz BPF, de-emphasis and a 44 dB volume level control. The signal is then amplified by SPK amplifier U11 to drive the speaker. Typical levels needed to obtain a 1 kHz, 0.5 watt receive rated audio output are shown in Figure 6.
3. When receive sensitivity is poor, refer to the radio section Schematic Diagram and typical voltages shown on Table 3. The receive section consists of low noise amplifier Q301, local oscillator amplifier Q103, If amplifier Q302 and second If circuit IC U11.
  - a. Level Diagram: A frequency Relationship Diagram is shown in Figure 7 and a Typical Level Diagram is shown in Figure 8.
  - b. Adjustments :
    - (1) C318 is provided for the adjustment of the second local oscillator.
    - (2) When the desired channel frequency with standard modulation is applied to the antenna terminal, adjust C323 for maximum output at RX Audio.



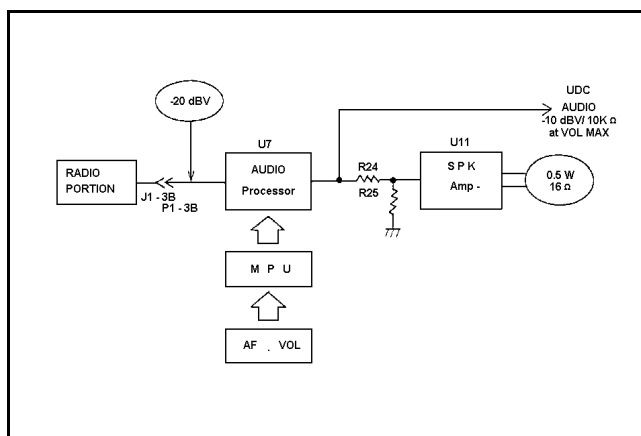


Figure 6 - Receive Audio Output

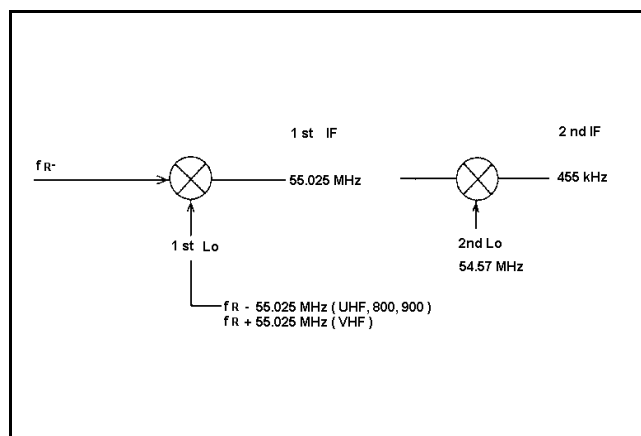


Figure 7 - Frequency Relationship Diagram

## (3) Adjustment of L304 and L306

- (a) Adjust L304 and L306 in this order to obtain the best SINAD sensitivity.
- (b) Next, adjust L304 and L306 in this order to obtain the minimum distortion of RX Audio Output : when receiving a standard modulated signal at 0.5mVrms.
- (c) If there is more than half a turn difference in the settings of L304 and L306 in the adjustments steps a. and b. above, a defective L304, L306 or the matching circuit is likely.

- c. Receiver first Local Oscillator Level : Local input level to Z2 is designed to be +7 dBm/50 ohms. Generally the input level is +6 to +8 dBm. If local input level is 3 dBm or less, sensitivity, intermodulation and If/2 spurious will be degraded.
- d. If the receive sensitivity changes by more than 5 dB across the band a circuit defect associated with FL301 and FL302 is likely.

Band	Receive Band
VHF	24 MHz
UHF	30 MHz
800 MHz	18 MHz
900 MHz	6 MHz

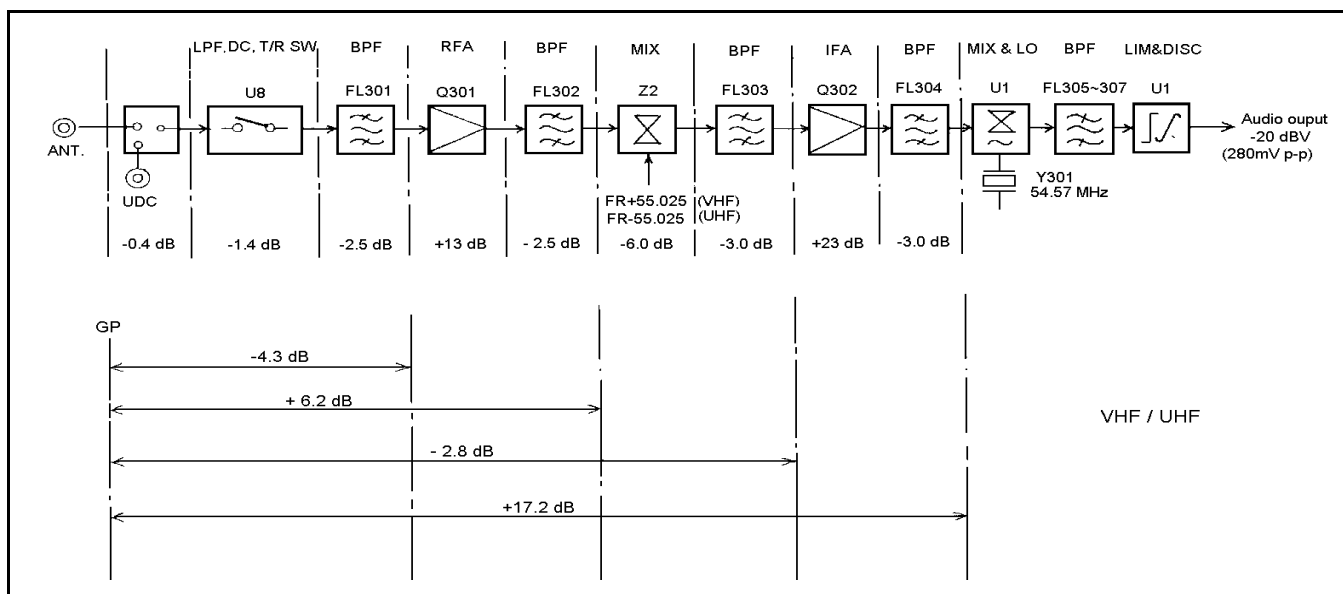


Figure 8 - Typical Level Diagram

Table 3 - Receive Section Typical Voltages

No.	Test Points	Voltage (V)	Remarks
1	Q301 Base	1.5	
2	Q301 Emitter	0.8	
3	Q301 Collector	5.8	
4	Q302 Base	1.2	
5	Q302 Emitter	0.4	
6	Q302 Collector	4.0	
7	U10 (1)	0 (GND)	
8	U10 (2)	7.4	
9	U10 (3)	5.0	
10	U11 (1) (13) (20)	0 (GND)	
11	U11 (2)	3.0	
12	U11 (3)	3.0	
13	U11 (4)	3.0	
14	U11 (5)	2.4	
15	U11 (6)	3.3	
16	U11 (7)	3.2	
17	U11 (8)	3.2	
18	U11 (9)	2.6	
19	U11 (10)	3.3	
20	U11 (11)	0.9	
21	U11 (12)	0.6	2.2 (-53dBm)
22	U11 (14)	0.7	
23	U11 (15)	0.7	
24	U11 (16)	—	
25	U11 (17)	—	
26	U11 (18)	—	
27	U11 (19)	4.1	
28	U11 (21)	1.1	
29	U11 (22)	4.1	

No.	Test Points	Voltage (V)	Remarks
30	U11 (23)	3.4	
31	U11 (24)	3.9	
32	U12 (1)	0.9	
33	U12 (2)	0.9	
34	U12 (3)	0 (GND)	
35	U12 (4)	5.0	
36	U12 (5)	5.0	

4. If distortion in the received signal is substantially high, try to perform checks with the Radio and Control Board individually.
  - a. Check the Local Oscillator frequency. Check the frequency after connecting a frequency counter through a 1 PF capacitor to the collector of Q103. The frequency relation at various stages is shown in figure 8. If a frequency error is 5 PPM (VHF/UHF)(1.5 PPM (800/900 MHz)) or more in the temperature range of 20 to 25C, adjust the frequency of VCTCXO (Z1). The frequency of VCTCXO is 13.2 MHz.
  - b. Check the Usable Band Width. Usable band width is generally  $\pm 2.5$  kHz (VHF/UHF/800 MHz)( $\pm 1.75$  kHz(900MHz)) or more of the desired receiving frequency. If the  $\pm$ balance is greatly different, the received signal may be distorted. This time, the problem is probably caused by FL303, FL304, FL305, FL306, FL307 or its associated components.
  - c. Distortion Check : When the radio receives a standard modulated signal, the audio output at the Audio terminal J1-3B (PI-3B) is about 280mVp-p. At this point, the distortion will be about 5%. This is because the receiver discriminator output is connected to the RX Audio terminal and de-emphasis and BP Filtering has not, at this point, been provided. Because considerable noise is contained from low audio frequencies to high audio frequencies, use test equipment with a high input impedance (100K ohms) for the distortion measurement.
  - d. The signal from the Radio Board is applied to the Control Board at P1-3B and then to the

speaker through U7 and U11. Check distortion at each point.

- e. Even if there are no electrical problems with the audio circuits on the Control Board, the speaker itself may cause distortion mechanically. The voice coil may rub or the diaphragm may be damaged or touching another part of the radio.

#### 5. Noise Squelch does not operate :

A part of receiver discriminator output is applied to the Control Board through J1-3B (P1-3B).

- a. The operation of squelch is controlled by Audio Processor U7 on the Control Board.
- b. The squelch operation level is set in the channel data E<sup>2</sup>PROM. Refer to E<sup>2</sup>PROM Programming.

#### 6. Other Problems and Cautions :

- a. A polyimide flex circuit is used at the LED flex Assy (M-RK I) and LCD/KB Flex Assy (M-RK II). If flex Assy is repeatedly disassembled for maintenance, the flex circuit can be damaged. Accordingly, keep disassembly of the Logic Section at a minimum.

### Transmit Circuit

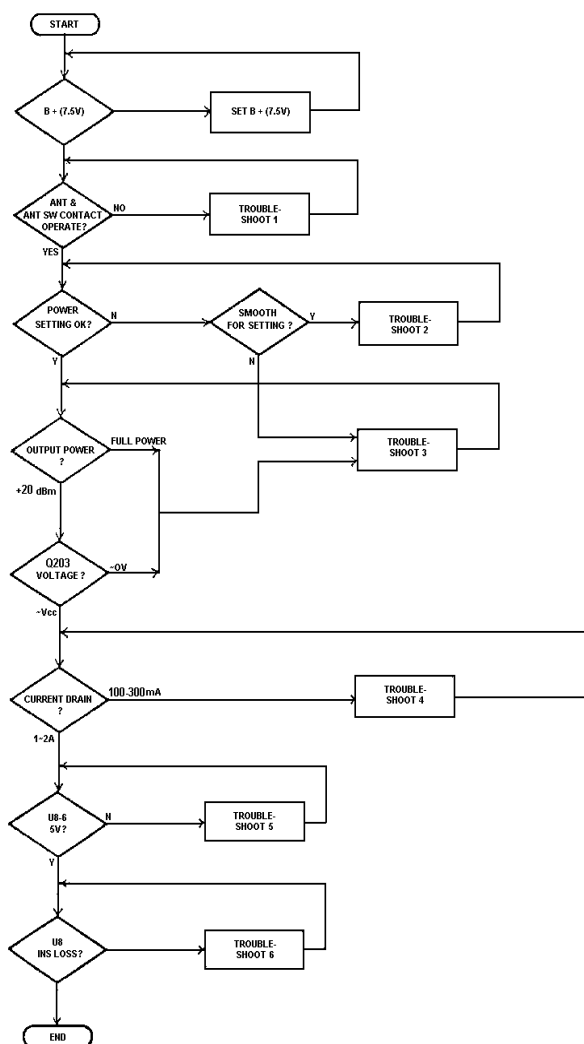
The following flowchart can be used to isolate a defective stage in the transmit circuit. Also, refer to Table 4 - Typical Transmit Circuit Voltage.

Flowchart: (Shown at right)

Troubleshooting for the Transmit Circuit :

1. Troubleshooting the Antenna Switch: Antenna Switch P1 (and J2) is a mechanical switch used to switch the RF signal between the antenna and the UDC RF connector J1. Periodically it is necessary to check that the antenna, the UDC RF Connector and RF Test Adapter (Coaxial Connector) are tightened securely. If the Antenna Switch does not contact properly even through the antenna and connectors are tightened securely, the contact of Antenna Switch may be defective.

As prescribed in the preventive maintenance section of the applicable maintenance manual, periodically clean the contact of the Antenna Switch by blowing compressed air on it. Otherwise, dust and dirt will collect on the contact and result in contact failure.



2. Check RF Output : If the transmit circuit can be set for the rated output, the transmit circuit is working properly.

### Checking

1. When the rated power output cannot be obtained smoothly, check U8.
2. If the rated power output cannot be obtained, check transistor Q203.
3. Transistor Q203 Voltage Check : When the collector voltage of transistor Q203 is about 0 volts, Q203, Q204 or U9 is probably defective.
- 4 a. If the current drain of the battery is in range of 100 to 300 milliamperes, verify that the voltage on Pin 3 of U7 is 7.3 volts. If 7.3 volts is not present at this point, the problem is with the D-PTT line

(Q201, Q202). Check to see if there is an open- or a short- circuit on other lines on the Vcc line.

b. If 7.3 volts is present at the above pins, check that voltage at collector of Q104 . If so, then check the output level of U5 (VCOT0).

c. When the output of U5 is around 0 dBm, the problem is Q104. When the output level is -5 dBm or lower, the VCO in the synthesizer circuit is probably defective. Try the troubleshooting procedure for the Synthesizer to verify the trouble with the VCO.

5. Checking Voltage at U8 : Under normal conditions, the voltage at the Pin 6 of U8 is 5 volts. If 5 volts is not present at this point, refer to troubleshoot 4.

6. Checking the U8 (LPF.DC.T/R SW) Insertion Loss : If an increase in the insertion loss of the U8 is suspected, the problem is U8.

Table 4 - Typical Transmit Voltages - UHF

No.	Test Points	Voltage (V)	Remarks
1	U7 (1)	—	
2	U7 (2)	0 (Rx), 7.3 (Tx)	Changed by power level
3	U7 (3)	0 (Rx), 5.5 (Tx)	
4	U7 (4)	0 (Rx), 7.3 (Tx)	
5	U7 (5) (6)	7.4	
6	U7 (7)	—	
7	U8 (2)	—	
8	U8 (4)	0 (Rx), 2.5 (Tx)	Changed by power level
9	U8 (6)	0 (Rx), 5.0 (Tx)	
10	U8 (8)	0 (Rx), 1.6 (Tx)	
11	U8 (13)	—	
12	U8 (1) (3) (5) (7) (9) (11) (12) (14)	0 (GND)	
13	Q104 Base	0 (Rx), 1.3 (Tx)	

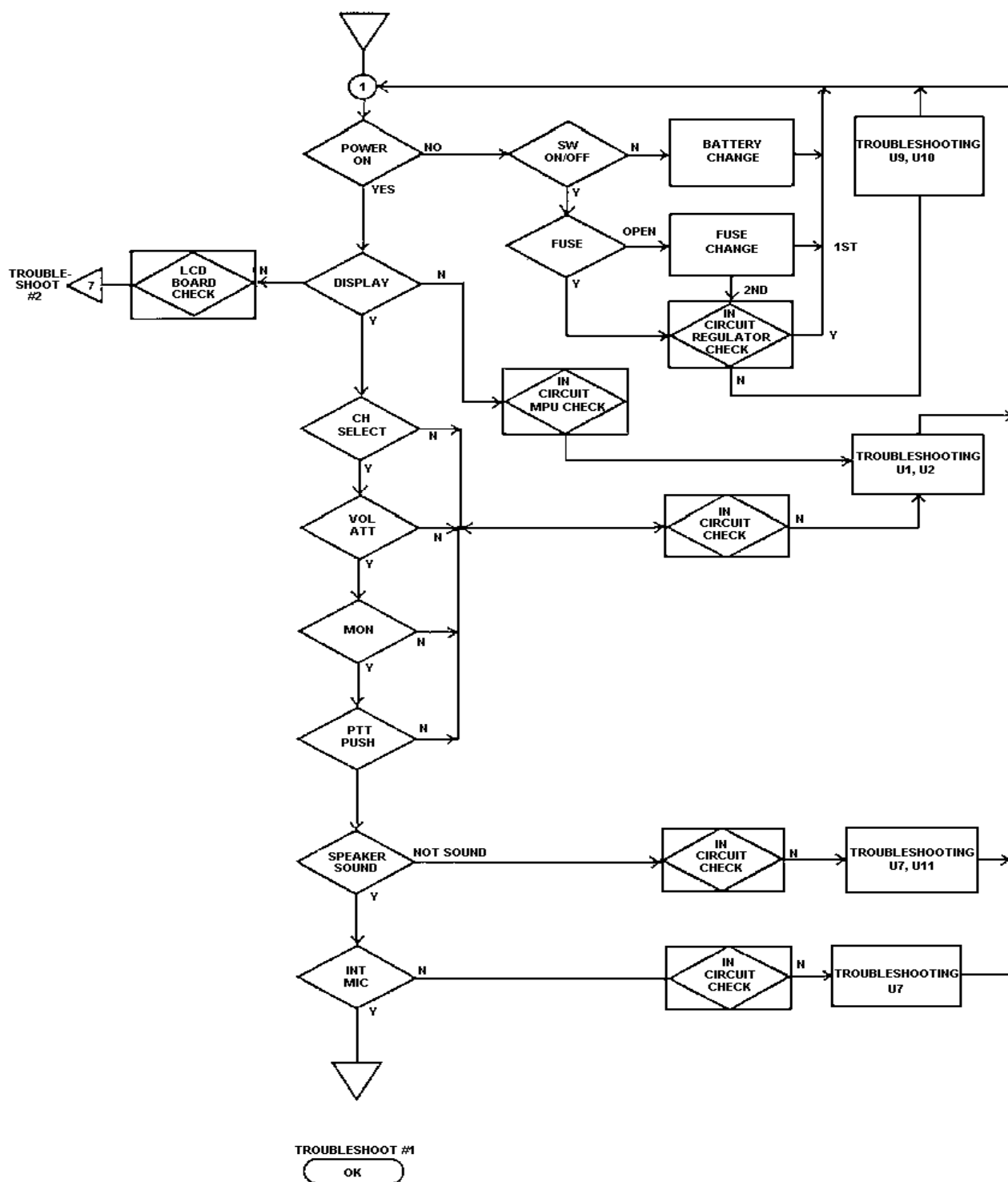
No.	Test Points	Voltage (V)	Remarks
14	Q104 Emitter	0 (Rx), 0.6 (Tx)	
15	Q104 Collector	0 (Rx), 6.7 (Tx)	
16	Q201 (1)	7.5 (Rx), 0 (Tx)	
17	Q201 (2)	0 (Rx), 5.0 (Tx)	
18	Q201 (3)	5.0 (Rx), 0 (Tx)	
19	Q201 (4)	0 (Rx), 5.0 (Tx)	
20	Q201 (5)	0 (GND)	
21	Q201 (6)	0 (GND)	
22	Q202 (1)	7.5 (Rx), 0 (Tx)	
23	Q202 (2)	0 (Rx), 7.3 (Tx)	
24	Q202 (3)	7.4	
26	Q203 Base	7.5 (Rx), 6.8 (Tx)	
27	Q203 Emitter	7.4	
28	Q203 Collector	0 (Rx), 5.5 (Tx)	Changed by power level
29	Q204 Base	0 (Rx), 2.1 (Tx)	Changed by power level
30	Q204 Emitter	0 (Rx), 1.5 (Tx)	Changed by power level
31	Q204 Collector	7.5 (Rx), 6.8 (Tx)	Changed by power level
32	Q205 (1)	5.0	
33	Q205 (2)	5.0 (Rx), 0 (Tx)	
34	Q205 (3)	0 (Rx), 5.0 (Tx)	
35	U9 (5)	3.6 (Rx), 1.9 (Tx)	Changed by power level
36	U9 (6)	0 (Rx), 1.9 (Tx)	Changed by power level
37	U9 (7)	0 (Rx), 2.1 (Tx)	Changed by power level
38	U9 (8)	0 (Rx), 4.9 (Tx)	
39	U9 (2) (3) (4)	0 (GND)	

## PHASE 2 : LOGIC SECTION TROUBLESHOOTING

Major Troubleshooting : (Display and Switch Action)

The flowchart (Display and Switch Action) can be used to isolate any defective stage located on the Control and the LCD/KB Flex Assy.(M-RK II).

## Flowchart (Internal Display and Switch Action)

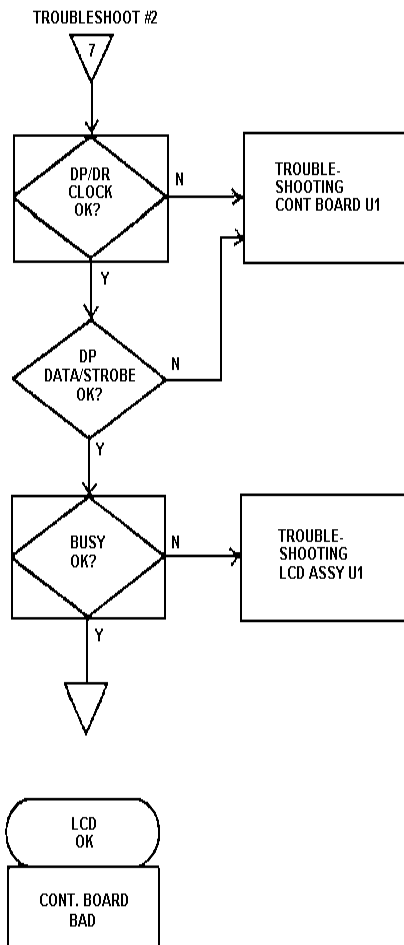


### Functional Troubleshooting: (External Input and Output Action)

The flowchart (External Input and Output Action) can be used to externally function test the Control Board through the UDC.

LCD/KB flex Assy (M-RK II) : The flowchart (LCD/KB Flex Assy) can be used to isolate any defective stage located on the LCD/KB Flex Assy.

Flowchart (LCD/KB Flex Assy)



### Troubleshooting for Logic Section

1. This troubleshooting should be made with the Control Board isolated from the Radio Board.
2. If the result is OK at Step 1, the E<sup>2</sup>PROM data (Channel No.) is displayed when power is ON. In the unlocked state of the Phase-Lock-Loop (PLL) UN-LOCK display is turned on and off at PTT.
3. If the result is OK at Step 2, the display should flicker in the unlocked state.
4. Step 3 indicated that the various switches are actuated in the sequence determined with the E<sup>2</sup>PROM data.
5. At Step 4, with 1 kHz, -20 dBV signal applied to RX, DISC terminal, check for 0.5 watt/16 ohm output to be present at the AUDIO OUT terminal.

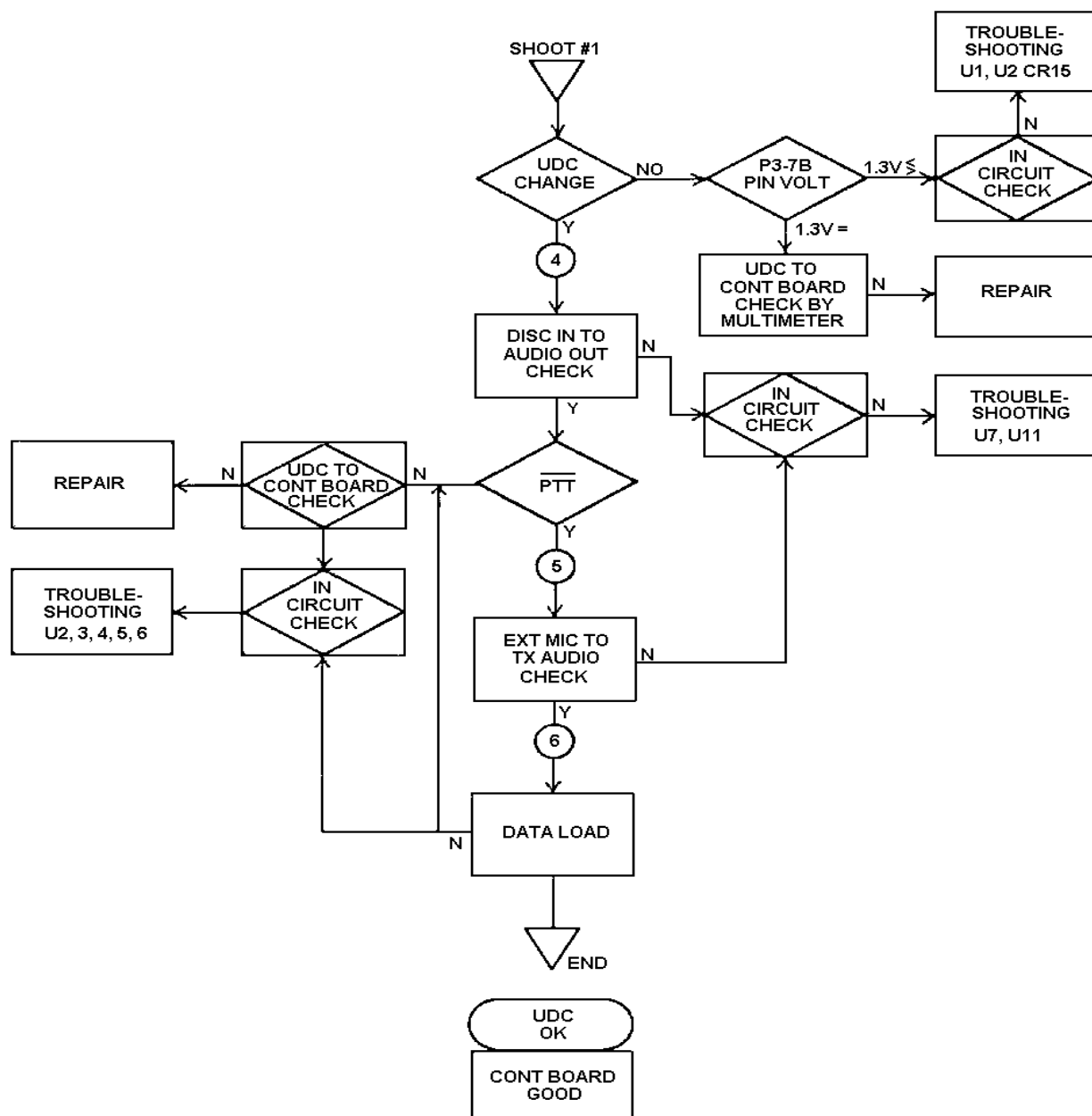
It should also be noted that when the initial VOL ATT setting is not at 0.5 watt/16 ohm, operate the AF, VOL (R8) for a volume level of 0.5 watt.

6. At Step 5, when the PTT line is grounded, the radio set is switched to the TRANSMIT mode. Then the PTT button on the side of the radio should be released.

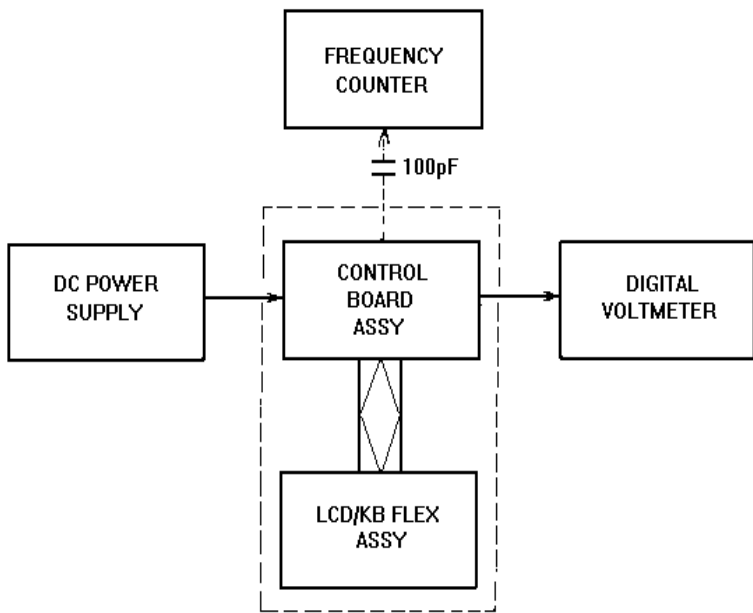
When the transmit mode is verified, apply 1 kHz, -40 dBV signal to the EXT MIC terminal from the Audio Analyzer. Check that a -7dBV +2 dB signal appears at the TX AUDIO terminal (Pin 2B of P1). Take note that the output at TX AUDIO is not subjected to limiting and without Channel Guard.

7. At Step 6, generate an arbitrary radio data with a data loader and try to load the data in the E<sup>2</sup>PROM. Check that data is loaded properly.
8. To perform an internal microphone (INT MIC) test, press and hold the PTT button and speak into the internal microphone. Check that an audio signal appears at Pin 2B of P1 (TX AUDIO terminal).

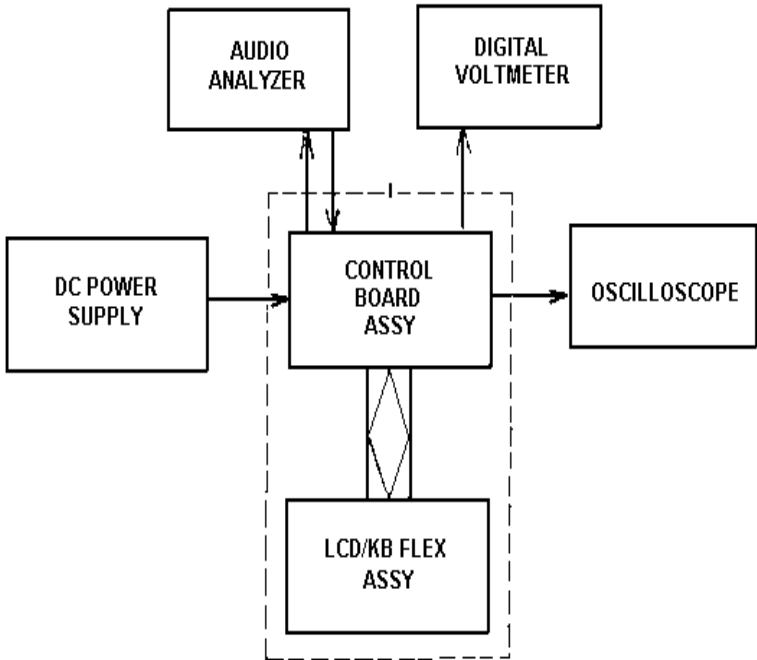
Flowchart: (External Input and Output Action)



## Logic Section Check List :

		MEASURING INSTRUMENT						
		Digital Voltmeter DC Power Supply Frequency Counter						
ITEM	TEST PROCEDURE							
1. Preliminary 1-1 Voltage Check	There are two regulated supply lines. Conduct voltage check at each check point as under. <table><tr><td><u>Check Point</u></td><td><u>Rated Voltage</u></td></tr><tr><td>U9 - Pin 1</td><td>5.0 V ±0.2 V for Control</td></tr><tr><td>U10 - Pin 3</td><td>5.0 V ±0.2 V for Audio</td></tr></table>		<u>Check Point</u>	<u>Rated Voltage</u>	U9 - Pin 1	5.0 V ±0.2 V for Control	U10 - Pin 3	5.0 V ±0.2 V for Audio
<u>Check Point</u>	<u>Rated Voltage</u>							
U9 - Pin 1	5.0 V ±0.2 V for Control							
U10 - Pin 3	5.0 V ±0.2 V for Audio							
1-2 Battery Out Check	Check that the voltage of Battery or DC Power Supply is present at P1-1B, P2-14B and P2-15b.							
1-3 Oscillator Frequency Check	Check Crystal "Y1" (IC U2-Pin 69) with frequency counter. The frequency should be within 9.8304 MHz ±300 Hz. Check Crystal.							



		MEASURING INSTRUMENT
		Audio Analyzer Oscilloscope Digital Voltmeter DC Power Supply Multimeter
ITEM	TEST PROCEDURE	
2. Preliminary 2-1 LED FLEX (M-RK I) 2-1 LCD/KB FLEX (M-RK II)	1. Check LED or LCD/KB FLEX by turning power supply on.  Insert connector (J1) on LED or LCD/KB FLEX into P2 on Control Board. Then turn power on and check that the data from Control Board is displayed in the LED or LCD/KB FLEX.	
3. SW Check and UDC Check	2-a. Operation for each switch, check whether each SW is operated or not by multimeter.  Check List	
	SW-Name	Connector Pin No. to be checked
	AF. VOL PTT MON OPT EMR	J1 — <div style="border-left: 1px solid black; border-right: 1px solid black; padding: 0 5px; display: inline-block;">           4B            1A            11A/13B            12A/13B            12B/13B         </div>  LCD/KB Flex Assy.

ITEM	TEST PROCEDURE
	<p>2-b UDC Check.</p> <p>Check List</p> <div><div><div><div>Pin No. to be checked</div><div><div>J1 —</div><div><div>1A - E3 1B - E2 2A - E1 2B - E6 3B - E4 4B - E5 5B - E7 6B - E10 7A - E12 7B - E8 8A - E11 8B - E9</div><div>- P1</div></div></div></div><div><div>UDC SIDE VIEW</div><div><div>Upper side</div><div><div><div><div>E3</div><div>E1</div><div>E2</div></div><div><div>E6</div><div>E4</div><div>E5</div></div><div><div>E8</div><div><div></div></div><div>E7</div></div><div><div>E11</div><div>E9</div><div>E10</div></div><div><div>E12</div><div></div><div></div></div></div></div><div>Lower side</div></div></div><div>UDC Flex</div></div></div>
4. RX S/N Measurement	<p>Set Audio Analyzer for 1 kHz, -20 dBv output. Apply this 1 kHz signal to RX AUDIO IN PI Pin 3B. Turn AF. VOL. to get Maximum output and check that the level at RX AUDIO OUT of P3 PIN 8B (-10 dBV or more) on Oscilloscope.</p> <p>Adjust CAL control on AUDIO Analyzer for "0". Turn 1 kHz signal off. Check that noise level is -45 dB or less.</p>
5. RX Frequency Response	<p>Set Audio Analyzer for 1 kHz, -30 dBV output. Apply this 1 kHz signal to RX AUDIO IN PI PIN 3B. Check that the level at RX AUDIO OUT of P3 PIN 8B is -20 dBV on Levelmeter and Oscilloscope. Adjust CAL control on Audio Analyzer for "0" to turn 1 kHz signal off. Change the OSC frequency from 210 Hz to 3kHz. Plot AUDIO OUT level on a graph. Check that the level from 500 Hz to 2.5 kHz is in the range of +1 dB to -3 dB from -6 dB/octave.</p>

ITEM	TEST PROCEDURE
6. RX Audio Distortion Measurement	<p>Set Audio Analyzer for 1 kHz. Apply this 1 kHz Measurement signal to RX AUDIO IN PI PIN 3B. Adjust until Levelmeter and Oscilloscope show that the P3 PIN 8B is -10 dBV.</p> <p>Check that Audio Analyzer distortion meter shows 5% or less at this time.</p> <p>Alternatively it is permitted to use SPEAKER AUDIO OUT as the check point.</p>
7. CG Opening Level Measurement	<p>Set Audio Analyzer for 67 Hz to 210.7 Hz. Apply this 67 Hz signal to RX AUDIO IN PI PIN 3B. Decrease the level of Audio Analyzer until the squelch opens. Check that the opening level is about -38dBV.</p> <p><b>NOTE :</b> Use the channel with CG tone in this test.</p>
8. SQ Operation	<p>Set Audio Analyzer for 10 kHz. Apply this 10 kHz signal to RX AUDIO IN PI PIN 3B.</p> <p>Check the output voltage for U2 Pin 59 on Control Board and plot the level on a graph. It is permitted that only the opening level and the closing level of squelch are checked.</p>
9. TX S/N Measurement	<p>On Test Set, set PTT switch to PTT and check that the Unit goes into transmit mode. Set Audio Analyzer to 1 kHz -40dBV. Apply this 1 kHz signal to EXT MIC Terminal of Test Set. There should be about -7 dBV signal at TX AUDIO OUT at PI PIN 2B. Adjust CAL control on Analyzer to null. Then turn the Analyzer output off. The S/N ratio should be 40 dB or better.</p>
10. TX Distortion Measurement	<p>Under the same test condition as with S/N measurement, measure distortion with the Audio Analyzer. The distortion should be less than 3%.</p>
11. TX Frequency Response	<p>Set Audio Analyzer for 1 kHz, -50 dBV. Apply this 1 kHz signal to EXT MIC Terminal of Test Set. Check that -17dBV signal is present at TX AUDIO OUT at PI 2B. Adjust CAL control on Audio Analyzer for null indication. Turn off the 1 kHz signal from Analyzer. Then change the output frequency of OSC 210 Hz to 3 kHz. Plot the changes in the output signal level on a graph. Check that the frequency response curve is within +1, -3 dB from 6 dB/octave over a 500 to 2.5 kHz (VHF/UHF/800 MHz), 2.3 kHz (900 MHz) range.</p>
12. Measurement of CG Encode	<p>Set PTT Switch to Off on Test Set. Select that Level and Distortion channel for which SIG appears on the LCD. Change PTT Switch to PTT side. Check that either 67 Hz to 210.7 Hz CG waveform is present at TX AUDIO OUT using an oscilloscope. Measure the CG signal level (-19 dBV is reference level). Check that the distortion in the CG waveform is less than 5%.</p>
13. Power Set Action	<p>With the PTT Switch in the PTT Position, check with digital voltmeter that 2.0 to 4.0 V is present at PIN 2A of PI.</p>
14. Syn. Clock, Syn. Data, Syn. Enable and Syn. Wide/Narrow Output	<p>Using an Oscilloscope, check that Enable signal is present at PIN 7B of PI, Data at PIN 8A, Clock at PIN 8B and Wide/Narrow at PIN 6A. In this test LOCK/UNLOCK Switch should be in the UNLOCK position.</p>

## M-RK LOGIC SECTION TEST DATA

TEST DATA  
 TEST CONDITION                      TEMP                      C  
    HUMIDITY                      %  
 TEST ASSY                      CONTROL BOARD  
    LED FLEX (MRK I)  
    LCD/KB FLEX (MRK II)

NO.	TEST ITEM	STANDARD VALUE	TEST VALUE
1-1	REGULATORS	5.0 V $\pm$ 0.2V	V
1-2	BATTERY OUT	7.5 V	V
1-3	OSCILLATORS	9.8304 MHz $\pm$ 300 kHz	MHz
2-1	LED OR LCD CHECK		GOOD/NG
3	SWITCH CHECK		GOOD/NG
3	UDC CHECK		GOOD/NG
	DATA LOAD		LOAD OK/NG
4	RX SIG/NOISE	> 45 dB	dB
5	RX FREQ RESPONSE	0.5 K - 2.5 kHz +1 dB -3dB	GOOD/NG
6	RX DISTORTION	< 5%	%
7	RX CG OPENING LEVEL	TYPICAL : -38dBv	dBV
8	SQ OPERATION		GOOD/NG
9	TX SIG/NOISE	40 dB	dB
10	TX DISTORTION	< 3%	%
11	TX FREQ RESPONSE	0.5 K - 2.5 kHz + 1 dB -3dB	GOOD/NG
12	TX CG ENCODE LEVEL	TYPICAL : -19 dBV	- dBV
12	TX CG DISTORTION	< 5%	%
13	POWER SET	2.0 V - 4.0V	V
14	SYN WIDE/NARROW CLOCK DATA ENABLE OUT		GOOD/NG

## TRACKING DATA

Tracking data is information stored in radio personality E<sup>2</sup>PROM that sets various transmit parameters to ensure proper performance over the band. If the RF Board in the radio is replaced, this tracking data may need to be changed.

If tracking data is supplied with the replacement RF Board, use the radio personality programmer to edit the personality E<sup>2</sup>PROM and enter the new tracking data. If tracking data was not supplied with the RF Board, retain the original data stored in E<sup>2</sup>PROM.

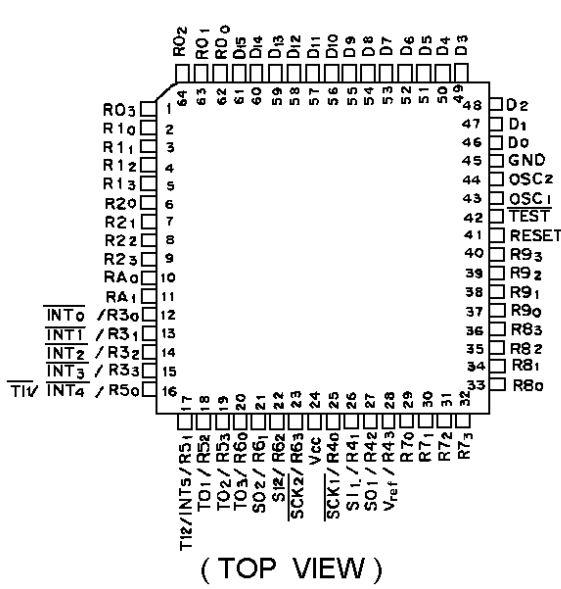
## MAINTAINING WEATHERPROOF INTEGRITY

The following maintenance procedure is required in order to assure that the radio housing will continue to meet the weatherproof features as designed.

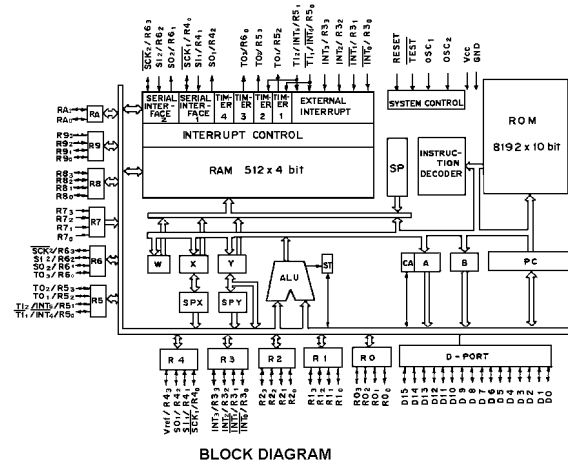
1. Replace key pads which become damaged or torn.
2. Check the "O" ring at base of the antenna when the antenna is removed. Check the housing seal around flanges of the Rear Assy. when the radio unit is opened. Avoid pinching or abrading seals when assembling. Use a light coating of Silicone Grease (GE #623 Clear Silicone Protector, or equivalent) on sealing surfaces of "O" rings to provide lubrication and to increase surface tension for waterproofing.

### NOTE

The antenna must be assembled securely to the top of the radio. Tighten to within two (2) to three (3) inch-pounds torque (40 in-ounces).

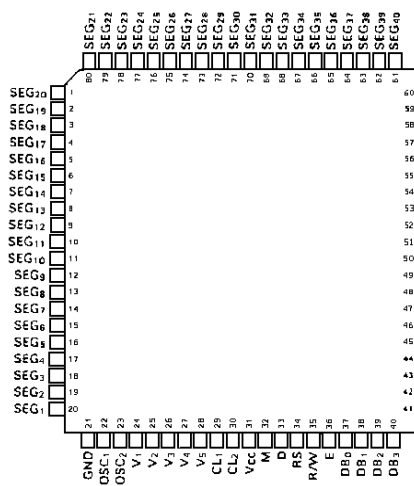


( TOP VIEW )

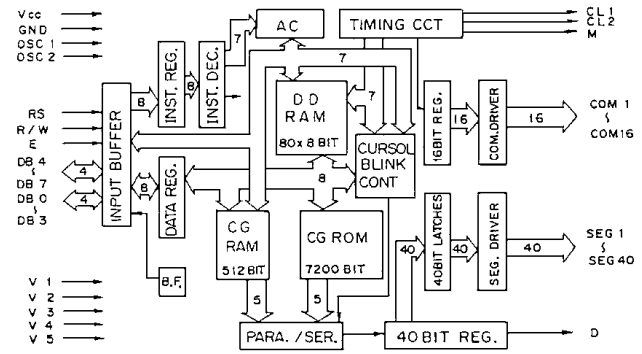


### BLOCK DIAGRAM

## LCD / KB FLEX BOARD LCD DRIVER ( U2 )



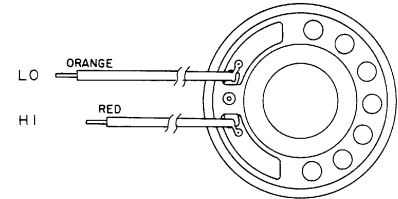
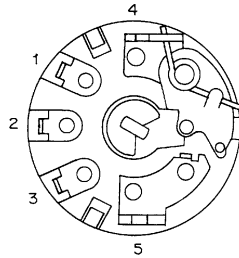
( TOP VIEW )



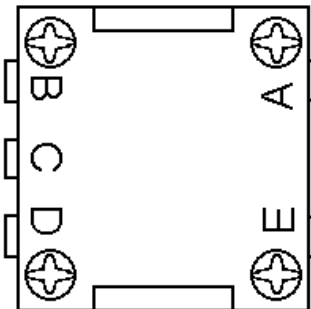
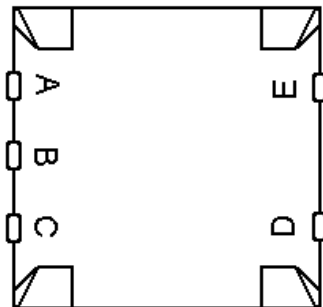
BLOCK DIAGRAM

LCD / KB FLEX  
LED FLEX  
AF VOLUME W/SWITCH ( R8 )

SPEAKER  
( LS1 )

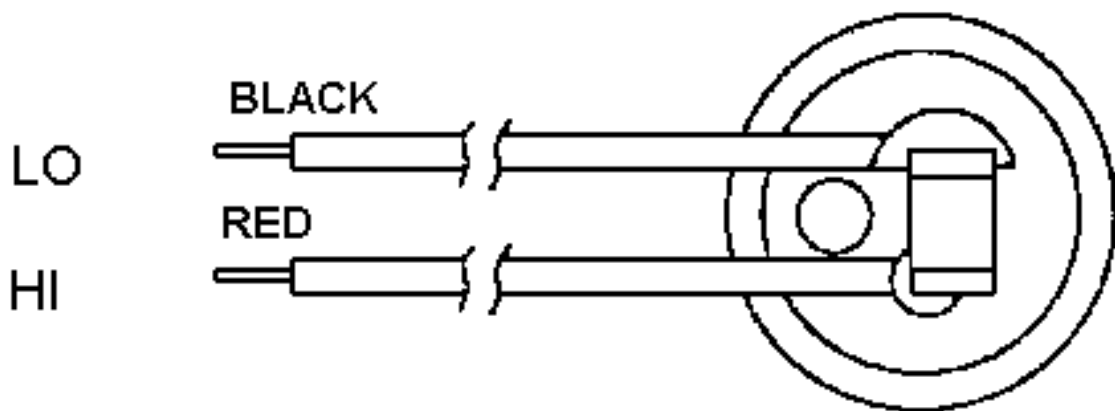


ROTARY SWITCH  
( S1 )

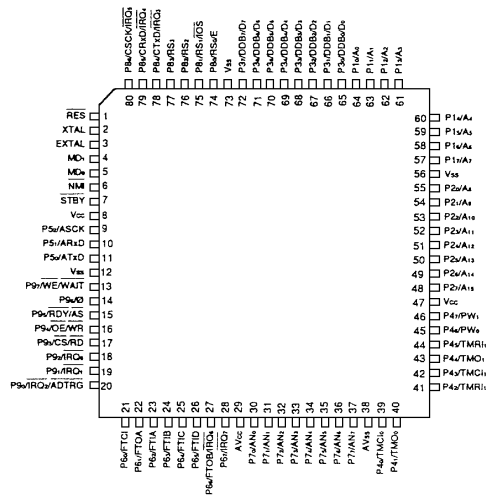


LED FLEX FROM ASSY REV. A  
LCD/KB FLEX FROM ASSY REV. C

MICROPHONE W/ CAPACITOR  
( MK1 ) ( C9 )

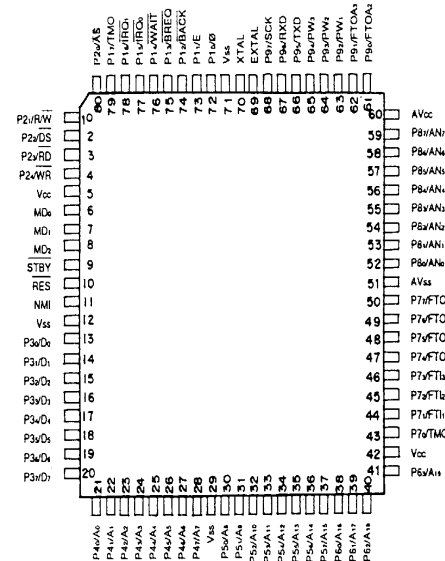


## CONTROL BOARD MICRO PROCESSOR ( U1 )

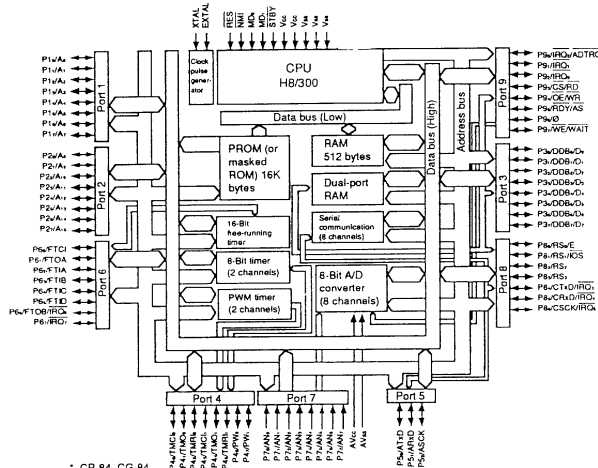


( TOP VIEW )

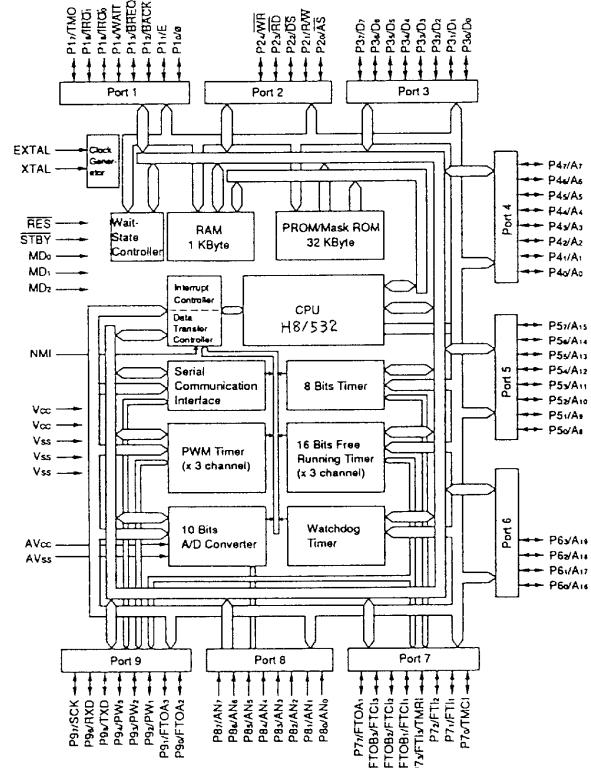
**CONTROL BOARD  
MICRO PROCESSOR ( U2 )**



( TOP VIEW )

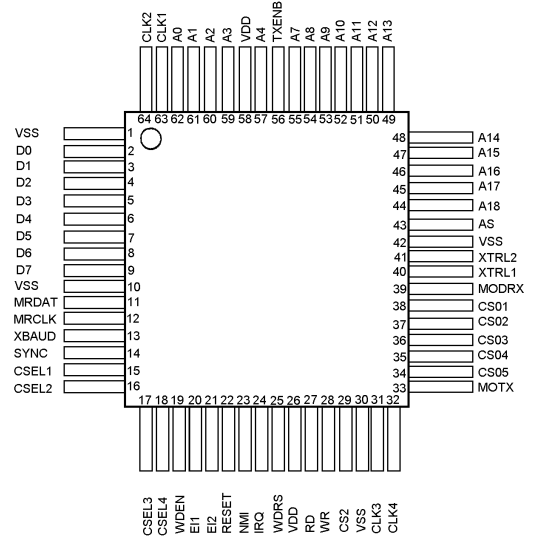
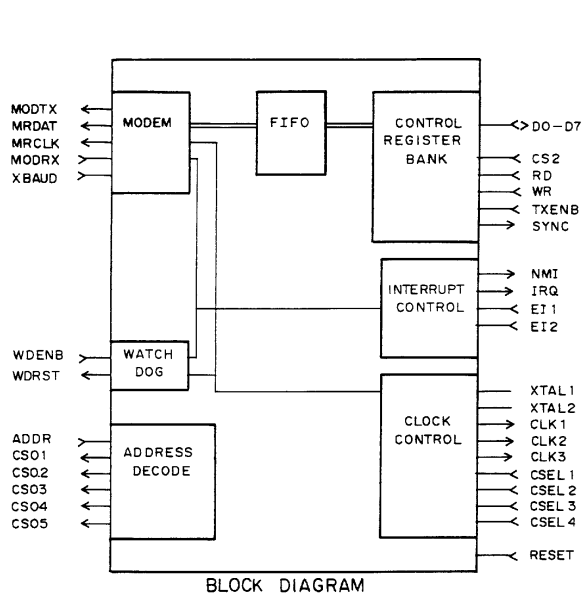


### BLOCK DIAGRAM



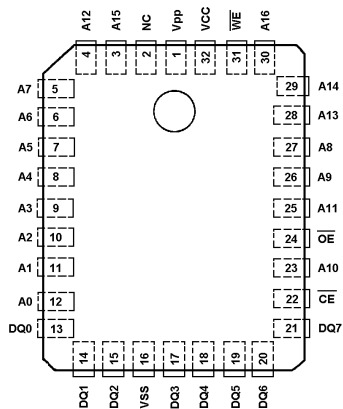


CONTROL BOARD  
DIGITAL SIGNAL PROCESSOR (U3)

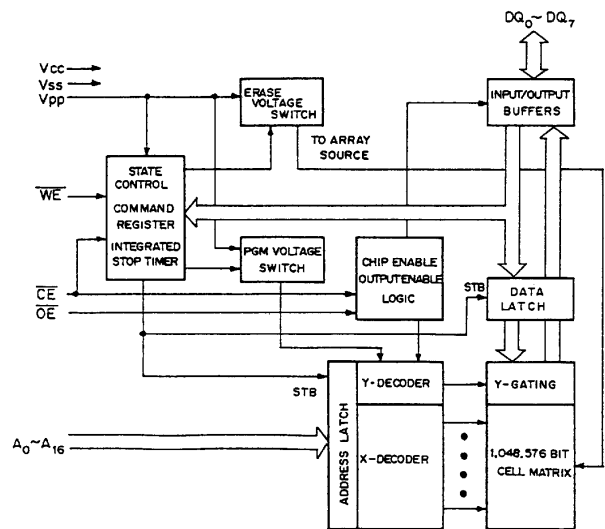


(TOP VIEW)

CONTROL BOARD  
FLASH E<sup>2</sup>PROM (U4)

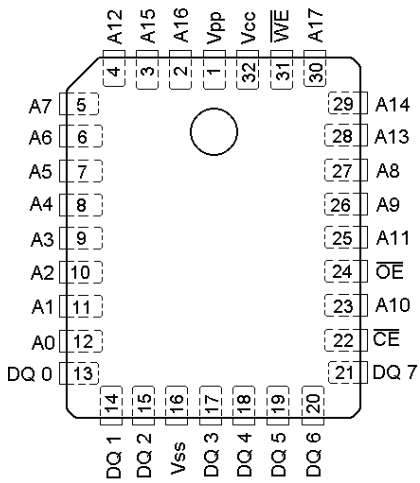


(TOP VIEW)



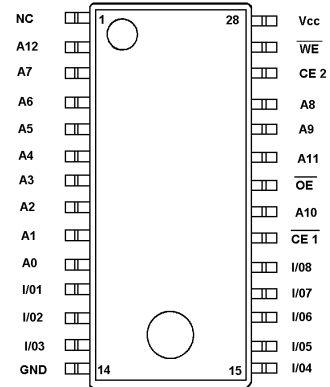
BLOCK DIAGRAM

**CONTROL BOARD (AEGIS)  
FLASH E<sup>2</sup>PROM ( U4 )  
28F020**

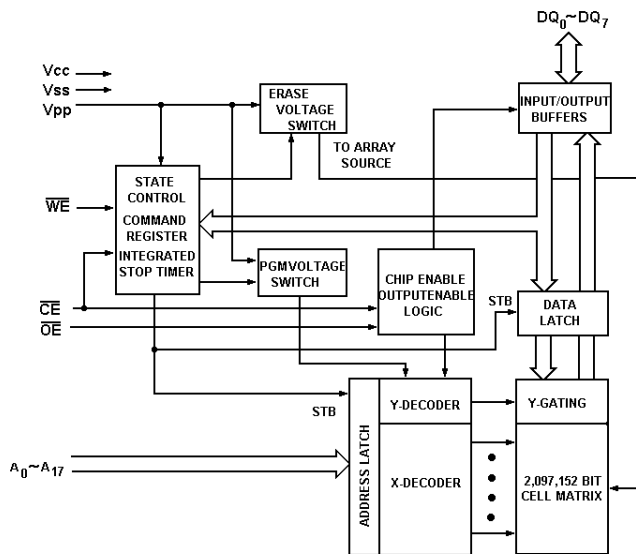


( TOP VIEW )

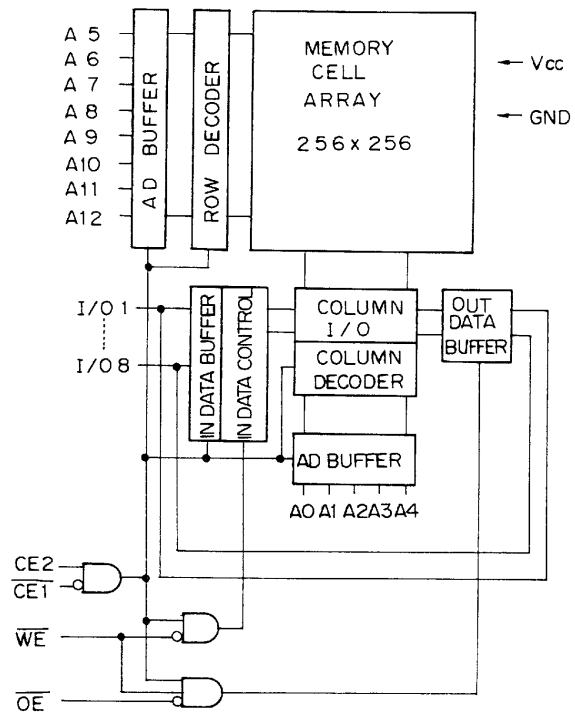
**CONTROL BOARD  
CMOS SRAM ( U5 )  
CONTROL BOARD  
CMOS SRAM ( U5 )**



( TOP VIEW )



BLOCK DIAGRAM



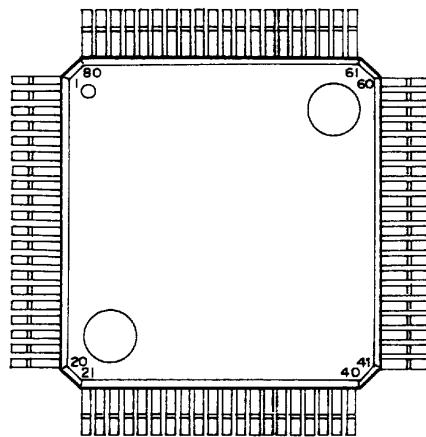
BLOCK DIAGRAM

The block diagram illustrates the memory system architecture. It features a central 512 X 512 MEMORY CELL ARRAY. Address lines A5 through A14 are connected to an AD BUFFER, which is also connected to the ROW DECODER. Address lines A0 through A4 are connected to the COLUMN DECODER. Data lines I/O 1 through I/O 8 are connected to the IN DATA BUFFER and OUT DATA BUFFER. Control signals CS, WE, and OE are connected to the memory array and buffers. The diagram also shows connections to Vcc and GND.

The block diagram illustrates the internal architecture of the 24C02 I2C EEPROM. It features a central **CONTROL LOGIC** block that manages the device's operation. External pins include **VCC** and **VSS** for power, and **SDA**, **SCL**, and **WC** for I2C communication. The **CONTROL LOGIC** is connected to a **SLAVE ADDRESS REGISTER & COMPARATOR** and a **WORD ADDRESS COUNTER**. The **WORD ADDRESS COUNTER** provides a **Word Address** to the **256 X 64 MEMORY CORE** and a **Word Increment** signal. The **MEMORY CORE** is also connected to a **DATA REGISTER** and a **Y DECODER**. The **Y DECODER** outputs a **64-bit Data** to the **DATA REGISTER** and a **256-bit Data** to the **MEMORY CORE**. The **DATA REGISTER** is connected to the **CONTROL LOGIC** and the **Y DECODER**. The **CONTROL LOGIC** also manages the **ACK** signal and the **CLOCK** and **DI/O** signals. A **HIGH VOLTAGE GEN. TIMING & CONTROL** block is connected to the **CONTROL LOGIC** and the **MEMORY CORE**.

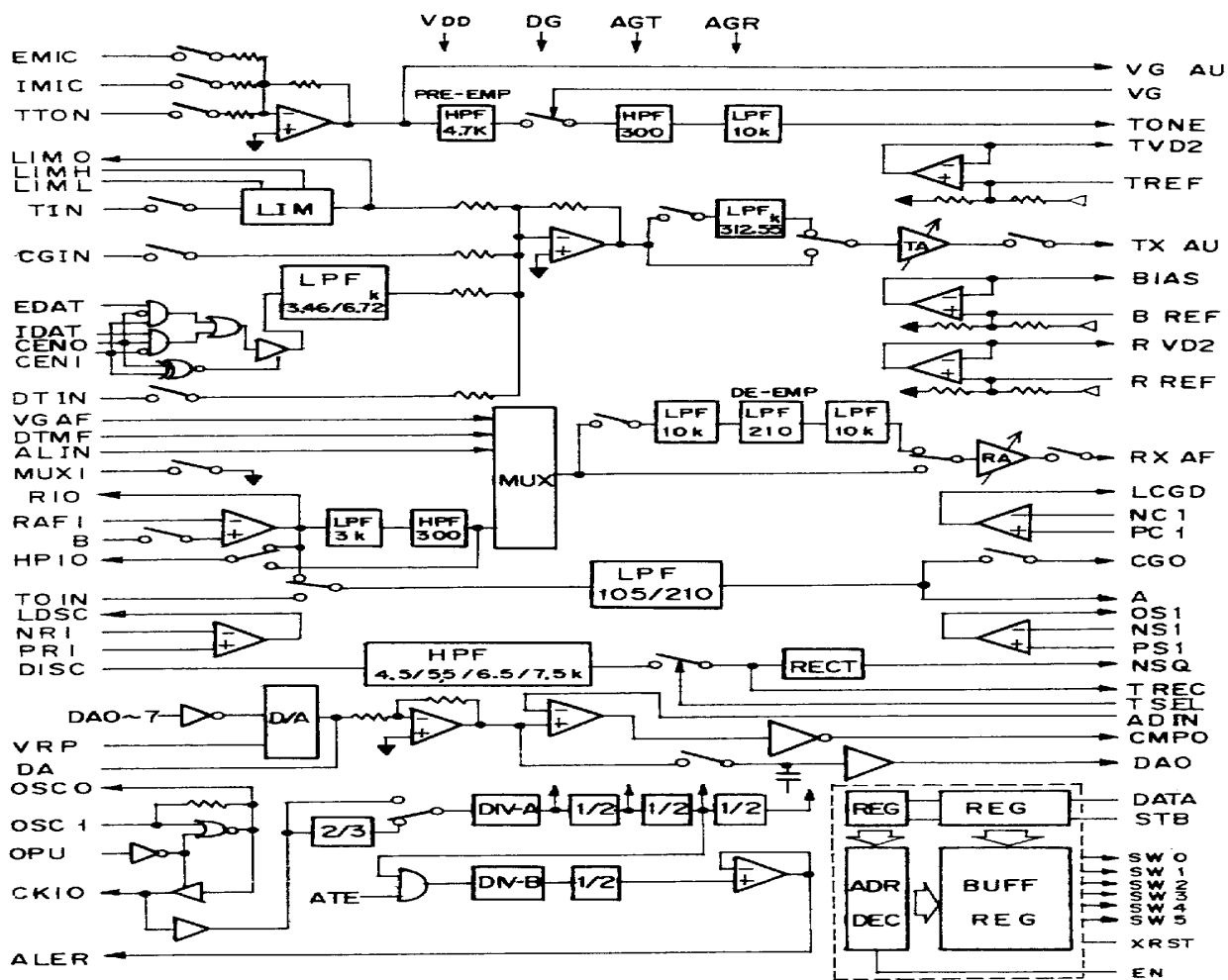
27

# CONTROL BOARD AUDIO PROCESSOR (U7)



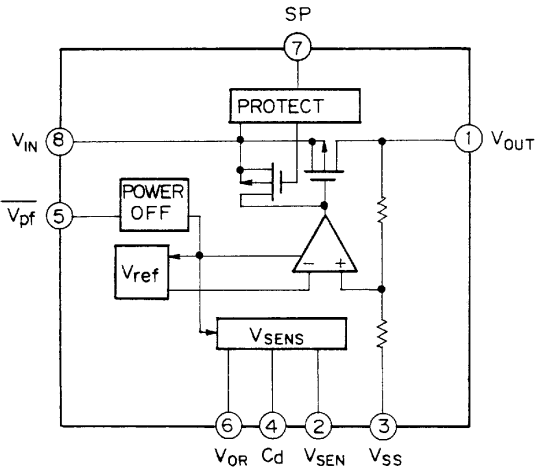
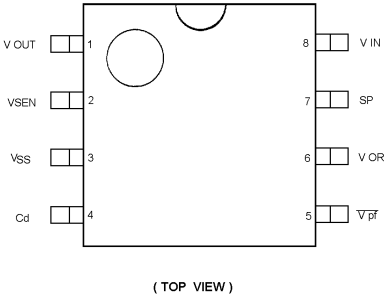
( TOP VIEW )

No	IO	name	No	IO	name	No	IO	name	No	IO	name
1	-	NC	21	O	LDSC	41	G	AGR	61	-	NC
2	I	OPU	22	O	LCGO	42	AO	MUX1	62	G	AGT
3	G	DG	23	O	CMPO	43	AO	R10	63	AO	TVD2
4	I	OSCI	24	-	NC	44	AI	RAFI	64	AO	TREF
5	O	OSCO	25	I	TSEL	45	AO	HP10	65	AO	BIAS
6	IO	CKIO	26	VD	VDD	46	AI	VRP	66	AO	BREF
7	G	DG	27	AO	RXAF	47	AO	DA	67	AO	LIMH
8	VD	VDD	28	AI	VGAF	48	AO	DAO	68	AO	LIML
9	I	XRST	29	AI	DTMF	49	AI	ADIN	69	AO	LIMO
10	I	EN	30	AI	ALIN	50	AI	DISC	70	AO	TONE
11	I	STB	31	AI	NR1	51	IO	TREC	71	-	NC
12	I	DATA	32	AI	PR1	52	AO	NSQ	72	AO	VG AU
13	O	SW5	33	-	NC	53	AO	OS1	73	AI	EMIC
14	O	SW4	34	AI	NC1	54	AI	NS1	74	AI	IMIC
15	O	SW3	35	AI	PC1	55	AI	PS1	75	AI	TTON
16	O	SW2	36	AO	A	56	-	NC	76	AO	ALER
17	O	SW1	37	AO	CGO	57	AI	TIN	77	VD	VDD
18	O	SW0	38	AI	TOIN	58	AI	CGIN	78	I	VG
19	VD	VDD	39	AO	RREF	59	AI	DTIN	79	I	EDAT
20	G	DG	40	AO	RVD2	60	AO	TXAU	80	I	IDAT

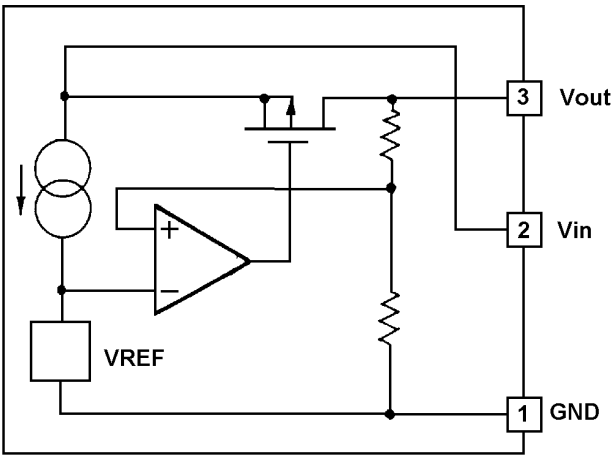
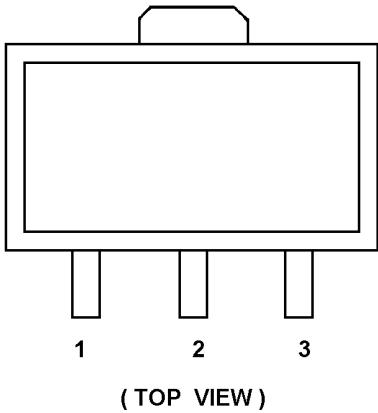


BLOCK DIAGRAM

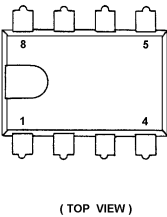
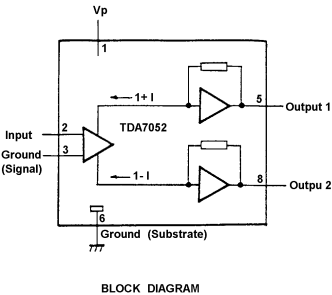
CONTROL BOARD  
VOLTAGE REGULATOR ( U9 )



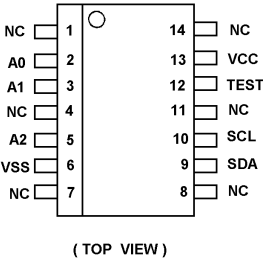
CONTROL / RF BOARD  
VOLTAGE REGULATOR ( U10 )



CONTROL BOARD  
INTEGRATED CIRCUIT /  
AF POWER AMPLIFIER ( U11 )

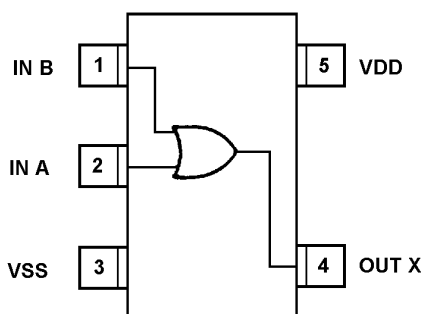


CONTROL BOARD  
E<sup>2</sup>PROM ( U6 )

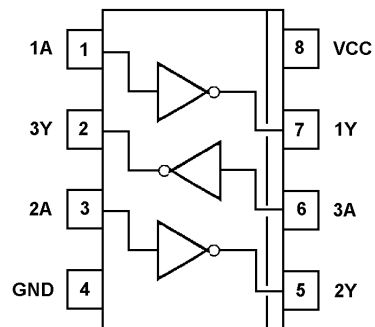


PIN NAMES

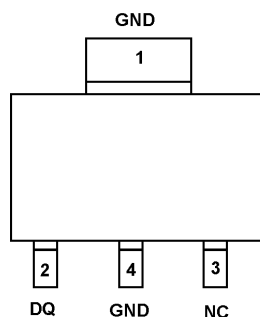
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock
TEST	Hold at Vss
VSS	Ground
VCC	+ 3.5V to + 6V
NC	No Connect

**CONTROL BOARD**  
**2 INPUT OR GATE ( U15 )**


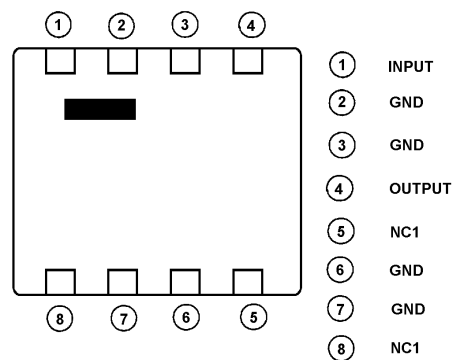
( TOP VIEW )

**CONTROL BOARD**  
**3 INVERTERS ( U12 ) ( U20 )**


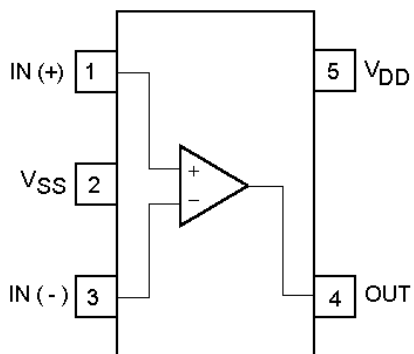
( TOP VIEW )

**CONTROL BOARD**  
**SERIAL NUMBER ( U16 )**


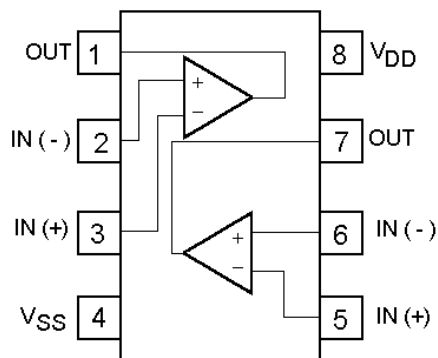
( TOP VIEW )

**RF BOARD**  
**BAND PASS FILTER ( FL201 )**


( TOP VIEW )

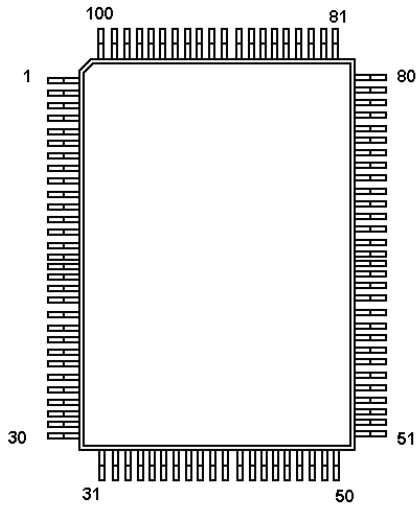
**CONTROL BOARD (AEGIS)**  
**OP AMP ( U18 )**


( TOP VIEW )

**CONTROL BOARD (AEGIS)**  
**OP AMP ( U18 )**  
**FROM ASSY REV. B**


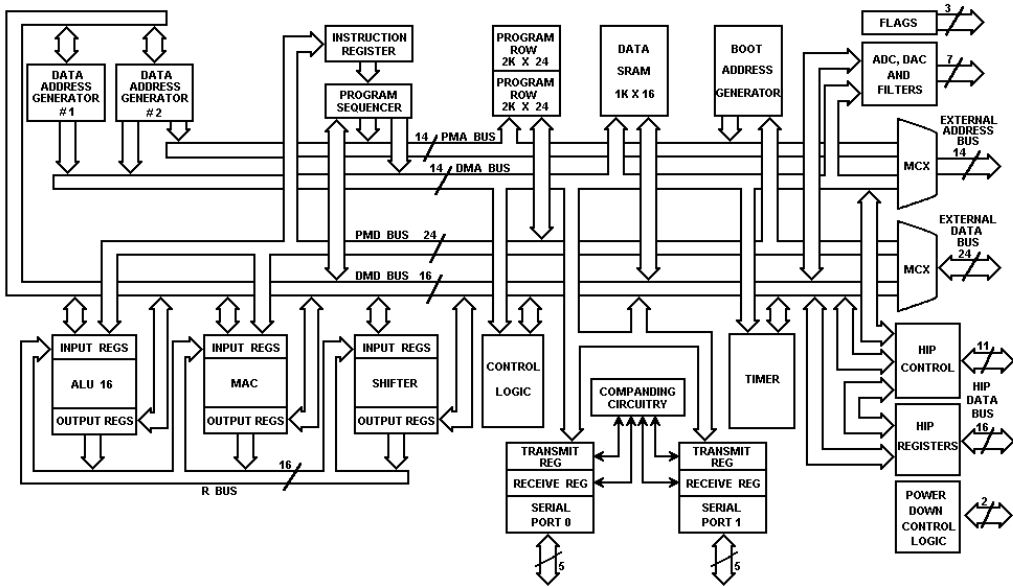
( TOP VIEW )

CONTROL BOARD (AEGIS)  
ADSP ( U17 ) FROM ASSY REV. B



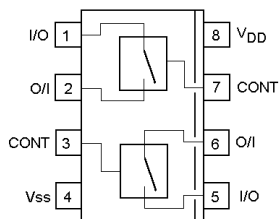
( TOP VIEW )

POFP NUMBER	PIN NAME	POFP NUMBER	PIN NAME	POFP NUMBER	PIN NAME	POFP NUMBER	PIN NAME
1	VDD	26	HA1	51	REF_FILT	76	D11
2	A4	27	HA0	52	VINAUX	77	D12
3	A5	28	HSEL	53	DECOUPLE	78	D13
4	A6	29	HWR/HDS	54	VINNORM	79	D14
5	A7	30	HRD/HRW	55	VCC	80	D15
6	A8	31	VDD	56	VREF	81	GND
7	A9	32	DT0	57	VOUTP	82	D16
8	A10	33	TFSO	58	VOUTN	83	D17
9	A11	34	RFSO	59	GNDA	84	D18
10	A12	35	DRO	60	BMODE	85	D19
11	A13	36	SCLKO	61	PWD	86	D20
12	GND	37	GND	62	BR	87	D21
13	VDD	38	DT1 / FO	63	BG	88	D22
14	XTAL	39	TFS1/RQ1	64	D0	89	D23
15	CLKIN	40	RFS1/RQ0	65	D1	90	VDD
16	CLKOUT	41	DR1/F1	66	D2	91	PMS
17	HD7	42	SCLK 1	67	D3	92	DMS
18	HD6	43	FLO	68	D4	93	BMS
19	HD5	44	HACK	69	D5	94	RD
20	HD4	45	HMD 1	70	D6	95	WR
21	HD3	46	HMD 0	71	D7	96	GND
22	HD2	47	IRQ 2	72	GND	97	A0
23	HD1	48	RESET	73	D8	98	A1
24	HD0	49	MMAP	74	D9	99	A2
25	HA2/ALE	50	GNDA	75	D10	100	A3



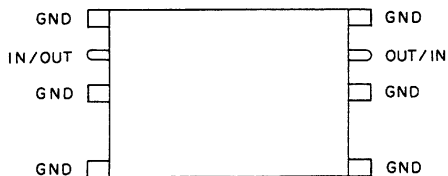
BLOCK DIAGRAM

**CONTROL BOARD (AEGIS)**  
**2 BI - LATERAL SWITCH ( U19 )**  
**FROM ASSY REV. B**

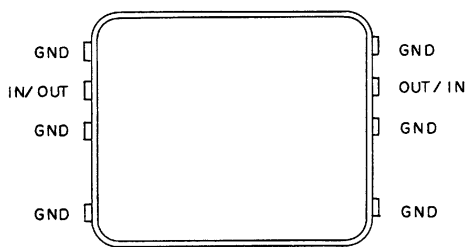


( TOP VIEW )

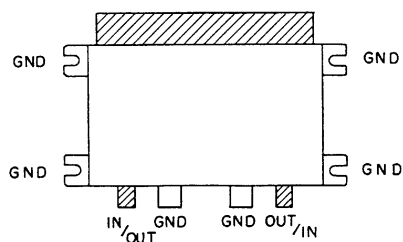
**RF BOARD**  
**BAND PASS FILTER**  
**( FL301, FL302 )**



VHF ( TOP VIEW )

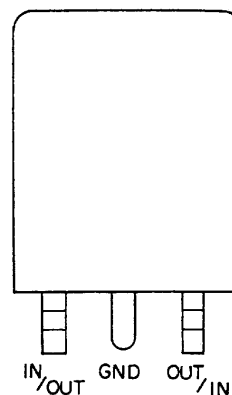


UHF ( TOP VIEW )

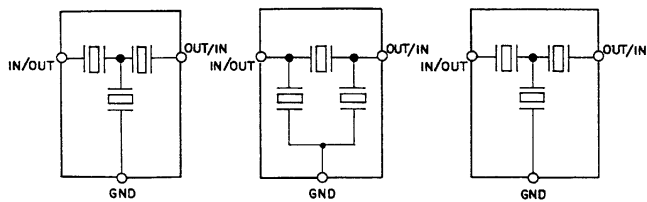


800 / 900 MHz ( TOP VIEW )

**RF BOARD**  
**BAND PASS FILTER**  
**( FL305, FL306, FL307 )**



( TOP VIEW )



FL 305

FL 306

FL 307



**BLOCK DIAGRAM**

The diagram illustrates the internal architecture of the PLL/FSS. It features a central 'Control Logic' block that manages the system. Key components include:

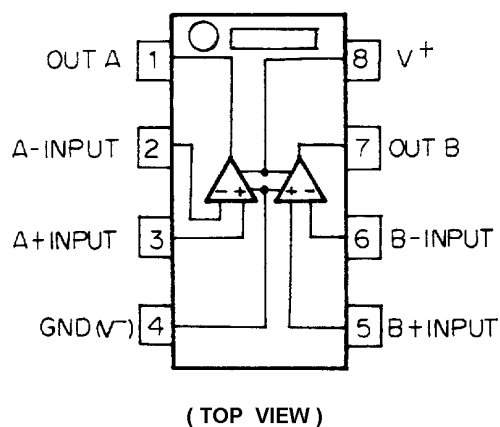
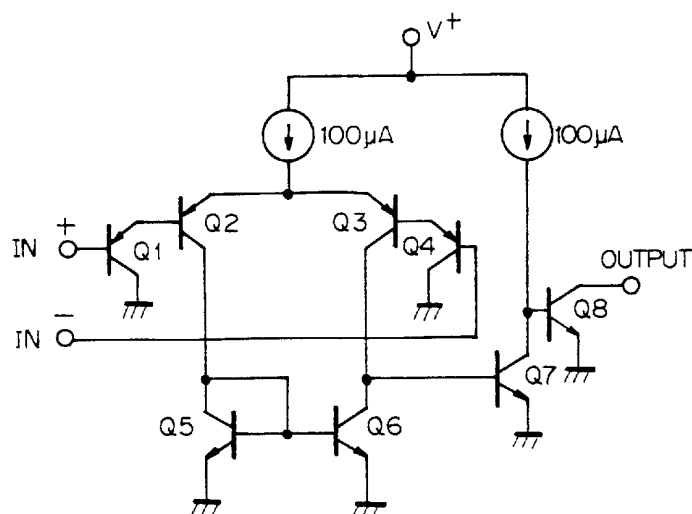
- 14-Bit S/R** (Shift Register) and **14-Bit Latch** for frequency division.
- 14-Bit  $\div$  R Counter** for frequency division.
- 7-Bit +A Counter** and **10-Bit  $\div$  N Counter** for frequency steering.
- 7-Bit Latch** and **10-Bit Latch** for data storage.
- 7-Bit S/R** and **10-Bit S/R** for data shift registers.
- 1 Bit S/R** for data shift register.
- Analog Phase Detector** for frequency locking.
- Digital Frequency Steering** for frequency control.
- Lock Detector** for lock status monitoring.

**Pin Connections:**

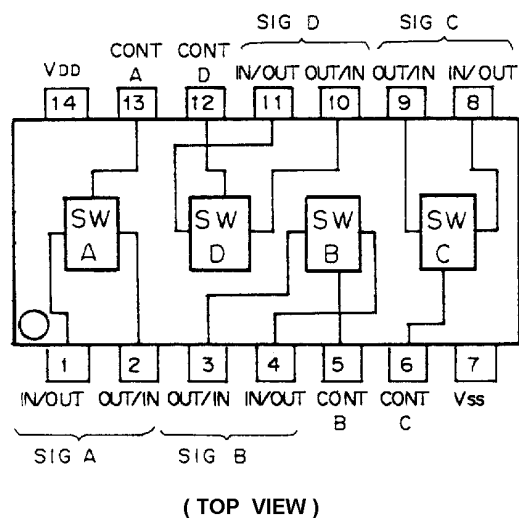
- Enable** (Pin 13): Connected to the 14-Bit S/R.
- OSC OUT** (Pin 3): Connected to the 14-Bit Latch.
- OSC IN** (Pin 2): Connected to the 14-Bit  $\div$  R Counter.
- f IN** (Pin 10): Connected to the 14-Bit  $\div$  R Counter.
- Data** (Pin 12): Connected to the 1 Bit S/R.
- Clock** (Pin 11): Connected to the 7-Bit S/R.
- SR Out** (Pin 14): Connected to the 14-Bit S/R.
- Charge** (Pin 4): Connected to the 14-Bit Latch.
- CH VDD** (Pin 5): Connected to the 14-Bit Latch.
- RR VDD** (Pin 19): Connected to the 14-Bit Latch.
- Ro Vss** (Pin 7): Connected to the 14-Bit Latch.
- CR Vss** (Pin 16): Connected to the 14-Bit Latch.
- APDout** (Pin 17): Connected to the Analog Phase Detector.
- VDD** (Pin 19): Connected to the Analog Phase Detector.
- Vss** (Pin 16): Connected to the Analog Phase Detector.
- Modulus Control** (Pin 8): Connected to the Analog Phase Detector.
- Frequency Steering Out** (Pin 6): Connected to the Digital Frequency Steering.
- LD** (Pin 9): Connected to the Lock Detector.

**RF BOARD**  
**DUAL OP - AMPLIFIER**  
 (U4, U9)

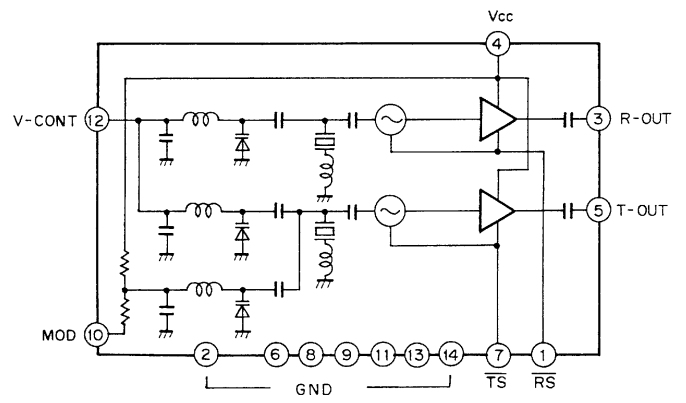
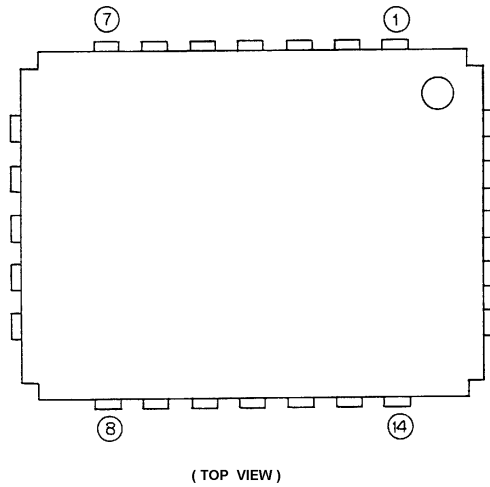
Equivalent Circuit (1/2 Circuit)



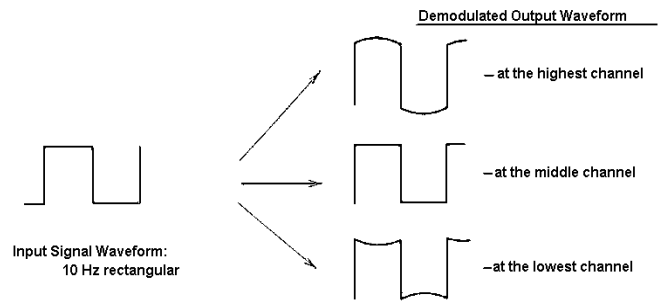
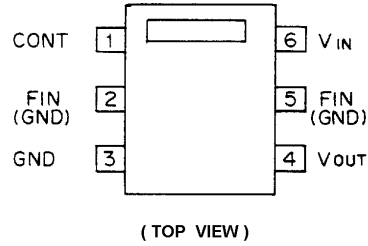
**RF BOARD**  
**QUAD / BI - LATERAL SWITCH**  
 (U3)



**RF BOARD  
VCO MODULE ( U5 )**

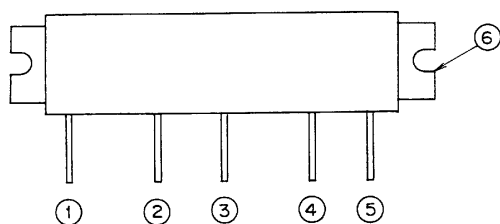


**RF BOARD  
REGULATOR ( U6 )**

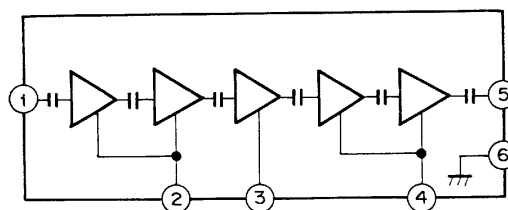


## RF BOARD

## POWER AMPLIFIER MODULE (U7)



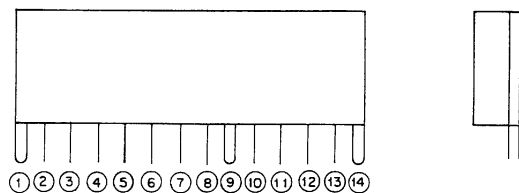
- ① RF INPUT ( 50  $\Omega$  )
- ② Vcc 1 (V-CONT)
- ③ Vcc 2 ( 7.5 V )
- ④ Vcc 3 ( 7.5 V )
- ⑤ RF OUTPUT ( 50  $\Omega$  )
- ⑥ FLANGE IS GROUND



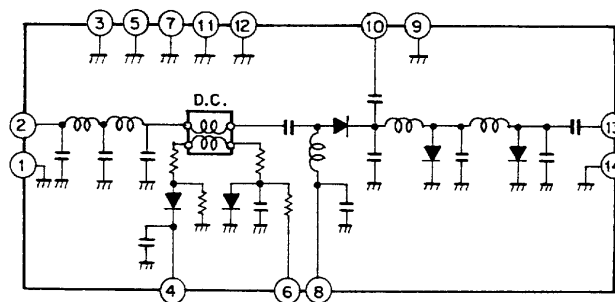
INTERNAL DIAGRAM

## RF BOARD

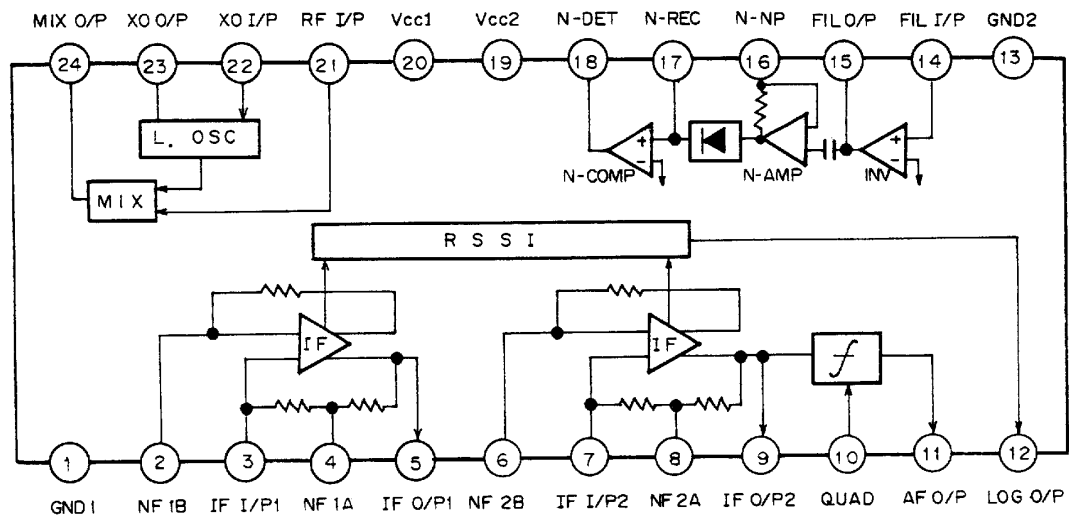
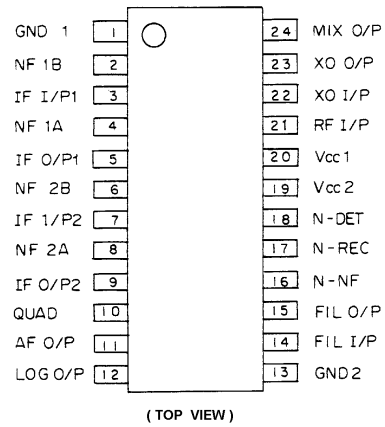
## LPF / DC / TR SWITCH MODULE (U8)



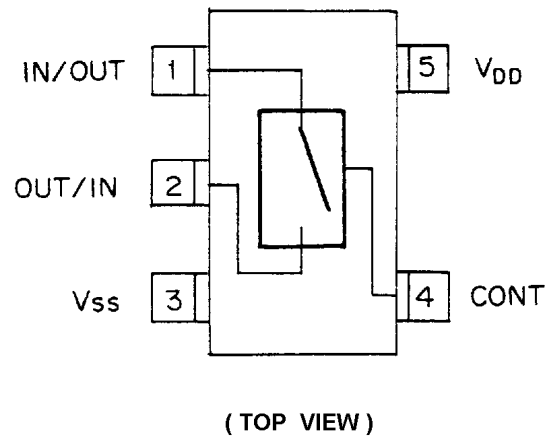
- ① CASE GND
- ② TX IN
- ③ GND
- ④ Vpf OUT
- ⑤ GND
- ⑥ BIAS ( 5 V )
- ⑦ GND
- ⑧ T/R SWITCH
- ⑨ CASE GND
- ⑩ ANT
- ⑪ GND
- ⑫ GND
- ⑬ RX OUT
- ⑭ CASE GND



**RF BOARD**  
**IF IC (U11)**

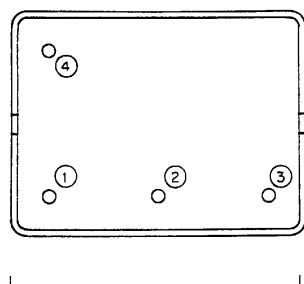


**RF BOARD**  
**BI - LATERAL SWITCH (U12)**

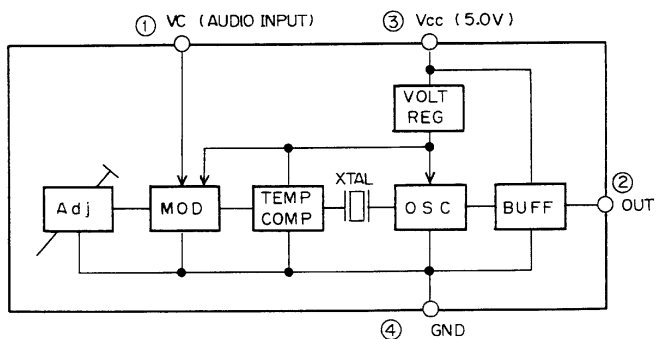


## RF BOARD

## VC TCXO MODULE (Z1)

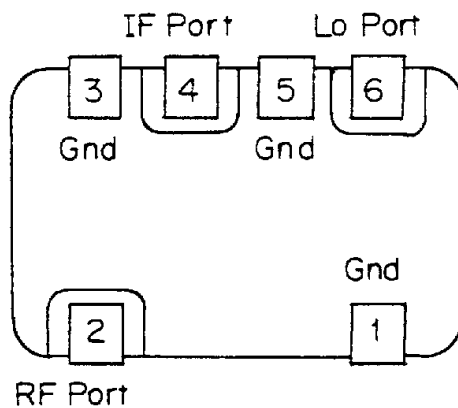
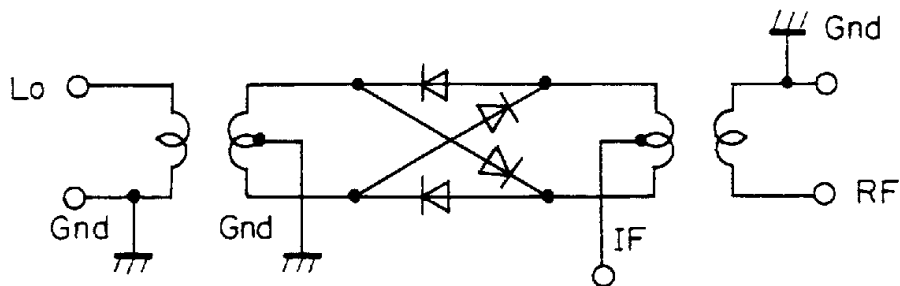


( BOTTOM VIEW )



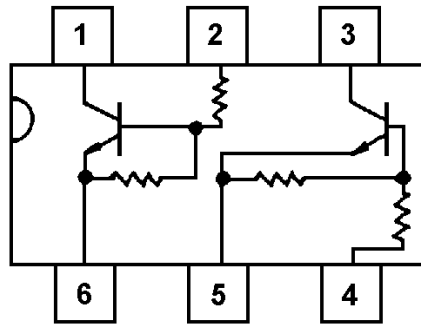
## RF BOARD

## DOUBLE BALANCED DIODE MIXER (DBM) (Z2)



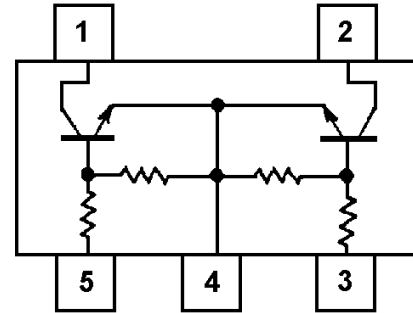
( BOTTOM VIEW )

**RF BOARD Q102, Q201  
LED FLEX BOARD Q2**



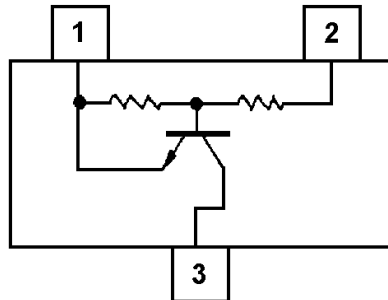
**( TOP VIEW )**

**CONTROL BOARD Q3  
LCD / KB FLEX BOARD Q5 ~ Q11**



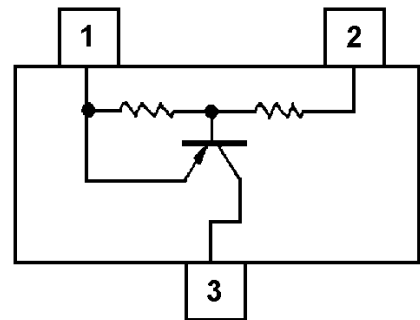
**( TOP VIEW )**

**RF BOARD Q105  
CONTROL BOARD Q8  
LCD / KB FLEX BOARD Q4**



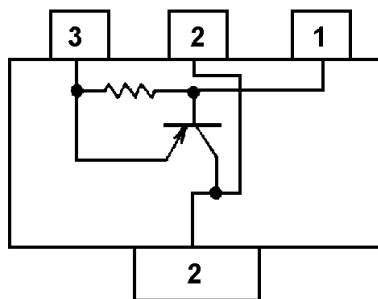
**( TOP VIEW )**

**RF BOARD Q205  
LCD / KB FLEX BOARD Q1, Q3  
LED FLEX BOARD Q1**



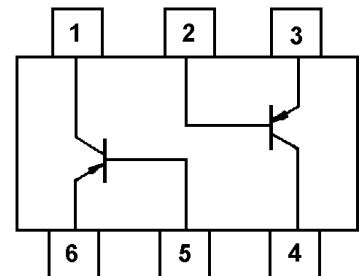
**( TOP VIEW )**

**CONTROL BOARD  
Q1, Q5, Q6**



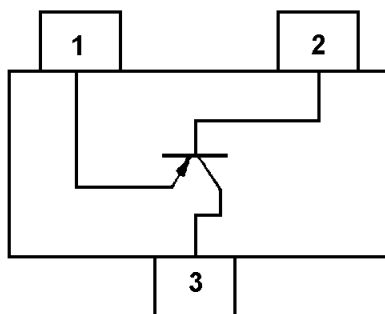
**( TOP VIEW )**

**CONTROL BOARD  
Q4, Q7**



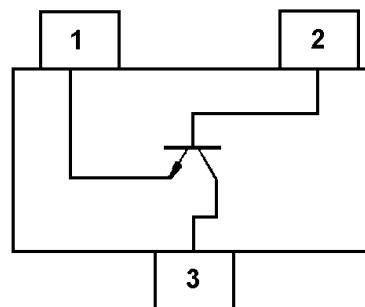
**( TOP VIEW )**

RF BOARD  
Q203 ( VHF, UHF )



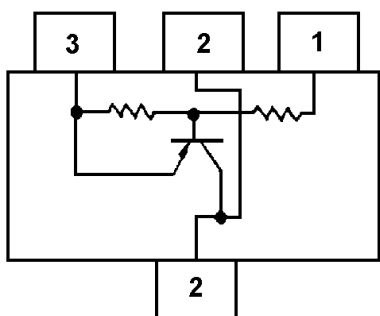
( TOP VIEW )

RF BOARD Q101, Q103, Q104, Q106, Q107, Q204,  
Q301 ( VHF, UHF ), Q302,  
CONTROL BOARD Q2  
LCD / KB FLEX BOARD Q2



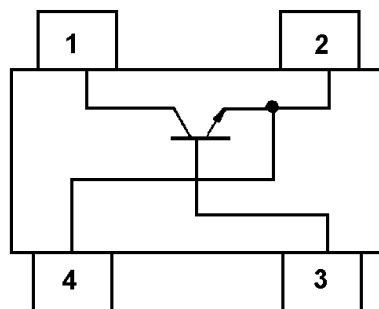
( TOP VIEW )

RF BOARD  
Q202



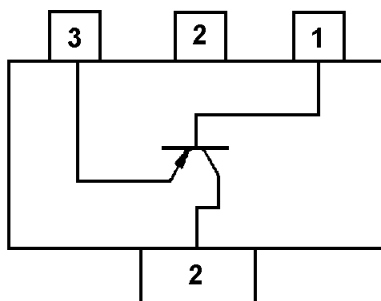
( TOP VIEW )

RF BOARD  
Q301 ( 800, 900 MHz )



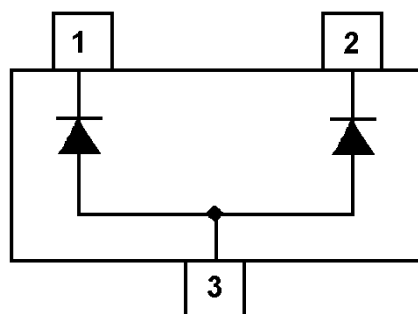
( TOP VIEW )

RF BOARD  
Q203 ( 800, 900 MHz )



( TOP VIEW )

CONTROL BOARD  
CR7 ~ 11, CR12



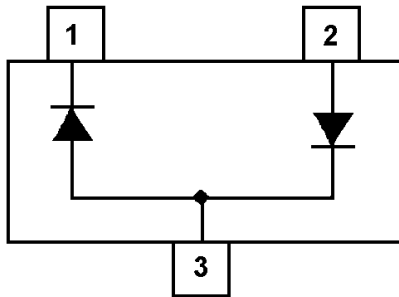
( TOP VIEW )



**CONTROL BOARD**

CR1 ~ 6, CR13 ~ 15

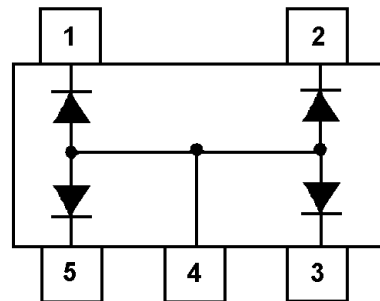
LCD / KB FLEX BOARD CR1



( TOP VIEW )

**LCD / KB FLEX BOARD CR3**

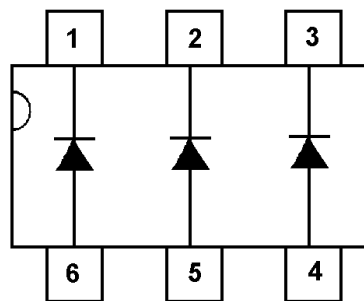
LED FLEX BOARD CR3



( TOP VIEW )

**LCD / KB FLEX BOARD CR2, CR4**

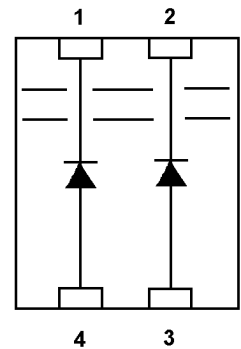
LED FLEX BOARD CR4



( TOP VIEW )

**LED FLEX BOARD**

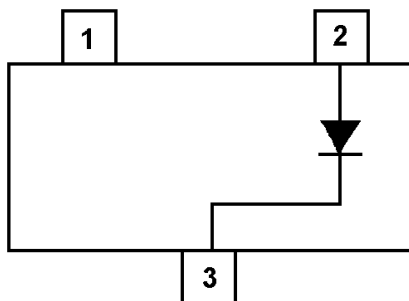
DS2, DS3



( TOP VIEW )

**RF BOARD**

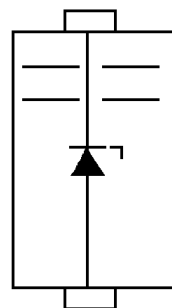
CR301



( TOP VIEW )

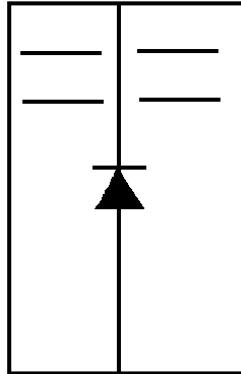
**CONTROL BOARD**

CR16



( TOP VIEW )

**LCD / KB FLEX BOARD DS1 ~ 4**  
**LED FLEX BOARD DS1**



**( TOP VIEW )**