ERICSSON

MAINTENANCE MANUAL
CONTROL BOARD
19D903081G1

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DESCRIPTION

Aegis™ M-PA™ radios consist of Control Board 19D903081G1 and Aegis Module 344A3659P3 or P4 installed in Front Cover Assembly 19D903620G1 or 19D438676G5. This assembly is joined to the appropriate Rear Cover Assembly to form a complete radio unit.

This manual describes Control Board 19D903081G1 and how it is interconnected to the Aegis Module and the Front and Rear Cover Assemblies. Component level troubleshooting information for the Control Board is also included.

The Aegis Module is electrically connected to the Control Board by three (3) single-in-line connectors. Located just above the speaker, it contains the digitizing circuitry for the radio. Radios equipped with option PAVS also utilize the encrypt/decrypt capability of the module. Detailed information on the appropriate Aegis Module is contained in a separate maintenance manual as listed in Table 1.

The Control Board is the largest and most complex board in the Front Cover Assembly. It contains all microcomputer circuitry which controls the radio. All of the audio circuitry in the radio, with the exception of the microphone, speaker and volume control, is also located on this board.

Aegis M-PA radios utilize an LCD Board located behind the display bezel. The Control Board serially communicates with this board to transfer display update information to it. The Keypad Flex is also located in the Front Cover Assembly. This flex circuit interfaces all operating controls to the Control Board. It also provides the interconnections between the Control Board and the LCD Board. Other assemblies and components in the Front Cover Assembly include the Emergency Button Board, the UDC and Speaker Flex circuits, the speaker, microphone and Battery Plate.

CIRCUIT ANALYSIS

CONTROL BOARD

The Control Board is a multi-layered circuit board primarily manufactured using surface-mounted components. This board is electrically connected to the Keypad Flex, LCD Board and UDC Flex circuits by two (2) flex connectors at the top of the board, J1 and J4. Single-in-line connectors P1 and P2 connect the Control Board to the RF Board in the Rear Cover Assembly. A 3-pin speaker audio connector, J3, and the battery power connections, H1 and H2, are located at the bottom of the board. Three (3) single-in-line connectors J5, J6 and J7, interface digital and audio signals to and from the Control Board and the Aegis Module. The Control Board is well shielded from the RF portions of the radio and the outside environment by the die-cast aluminum casting and the metallic shield.

On the Control Board, I/O Microcontroller U7, Microprocessor U18, and Audio Processor U8 communicate by serial data lines. The two microprocessors control all radio functions and the audio chip is primarily responsible for transmit/receive audio routing and filtering. Factory programmed PROM U15 stores the operating program for U18. RAM U16 provides operating memory. Personality information programmed into the radio from the IBM PC or compatible computer is stored in EEPROM U17. Support circuitry includes modem U19, voltage regulators, microprocessor reset, and the microphone and speaker audio amplifiers.

I/O Microcontroller U7

I/O Microcontroller U7 is a 68HC705 8-bit processor that has four I/O ports to provide direct logic control to the radio. I/O lines from the four ports serially interface the Keypad Flex, Audio Processor IC, LCD Board and the synthesizer chip on the RF Board. Several other digital I/O lines from U7 control various other radio functions, generate DTMF and GE-STAR tones, and perform Channel Guard decoding. The operating program stored in U7's internal PROM configures all ports for either input, output, or bidirectional use on a bit-by-bit basis.

Four (4) serial lines between I/O Microcontroller U7 and Microprocessor U18 provide the interprocessor communications path between the chips. See **Interprocessor Communications** for details.

Operating power (5.0 Vdc) is supplied to U7 pin 38 from the VCC supply and a power-on reset pulse is applied to U7 pin 41. See **Regulator Circuits** and **Microprocessor Reset Circuits** for details.

An oscillator circuit in U7 is set to 2 MHz by crystal Y2. This oscillator circuit provides internal clocking for the chip. The clock signal can be monitored on U7 pin 36 (TP4).

Audio Processor U8 Interfacing

Three (3) I/O lines from U7 ports A and C provide serial interfacing to the Audio Processor IC. The serial bus consists of the clock (CAC_CLK from U7 pin 4), a data output line (CAC_DATA from U7 pin 5) and a chip-select output (CAC_EN from U7 pin 20). All control data from U7 is transferred to U8 using these I/O lines.

Microcontroller U7 uses a digital-to-analog converter in Audio Processor U8 to check the voltage levels of the analog inputs to U8. The four (4) analog inputs are: squelch (COMPA or AOUT, U8 pin 55); UDC resistor (COMPB, U7 pin 58); volume control position

(COMPC, U8 pin 59); and battery voltage (COMPD, U8 pin 2). U7 first loads U8 with data to select one of the four analog inputs and it loads data into U8 to generate an output voltage from U8's internal D/A converter. A comparator inside U8 then compares the selected analog input (COMPA - COMPD) to the D/A generated voltage. U7 then samples the D/A comparators's output of U8 (DA_COMP or COMPOUT, U8 pin 43) and it then loads new data into U8 to step the D/A analog voltage up or down and determine the exact transition point of the comparator, and thus the selected input voltage.

Microcontroller U7 also generates DTMF tones and GE-STAR signals for radios programmed with these features. Using the associated summing resistors, five output lines from port C (U7 pins 21, 23 - 26) generate staircase waveforms. The staircase waveforms are sent via the DTMF line to the TONEC input of the Audio Processor (U8 pin 15). Circuitry in U8 provides the necessary filtering to convert the staircase wave to a sine wave.

Channel Guard and Digital Channel Guard signals are decoded by U7. Filtered and limited tones from U8 pin 11 are applied to U7 pin 34 via CG_LIM.

Keypad Flex and LCD Board Interfacing

Serial interfacing to the Keypad Flex and LCD Board is accomplished by seven (7) I/O lines to and from U7 ports A, B and D. The five (5) lines from ports A and B are outputs from U7. The two (2) port D lines are inputs to U7.

Shared with the Audio Processor, the clock (CLOCK, U7 pin 4) and data (DATA_OUT, U7 pin 5) lines are also used by the Keypad Flex output shift register IC and the LCD Board controller IC. Separate chip-select outputs are provided for the keypad output shift register (SR_STB, U7 pin 10) and the input shift register (SR_ENA, U7 pin 15). U7 also has a chip-select output to the LCD Board controller IC (DISP_ENA, U7 pin 6), a display busy input (DISP_BUSY, U7 pin 32), and a keypad data input (DATA_IN, U7 pin 30).

Synthesizer Loading and Lock Monitoring

The loading of frequency data into the synthesizer IC on the RF Board occurs when a new receive frequency is selected, when the radio changes from receive to transmit, or when the radio changes from transmit to receive. This is accomplished by clocked serial lines from U7 port B. The clock (SYN_CLK, U7 pin 11), data (SYN_DATA, U7 pin 12), and enable (SYN_EN, U7 pin 13) outputs load the synthesizer chip with new frequency data. SYN_DATA is configured as an output when synthesizer loading occurs. Data on SYN_DATA is serially clocked into the synthesizer IC by SYN_CLK and latched by SYN_EN.

When U7 wishes to check the lock status of the synthesizer, it reconfigures SYN_DATA (U7 pin 12) as an input. U7 then monitors the synthesizer's LOCK DETECT output on J102/P2 pin 8 using operational amplifier U10D. LOCK DETECT goes low or pulses when the synthesizer is not locked. Op-amp U10D is wired to latch low if LOCK DETECT goes low. Its output will return high only when SYN_EN pulses if LOCK DETECT has also returned high. Resistors R39 and R65 isolate the respective circuits during the input and output modes. R87 provides hysteresis for the latch circuit.

Microcontroller U7 also supplies a band-switch logic line to RF Boards which require this. The SYN_BSW output from U7 pin 8 is applied to J102/P2 pin 3 (SYN BSW). See the appropriate Rear Cover Assembly maintenance manual for details on the logic level verses VCO operating frequency.

Table 1 - Related Assemblies For Aegis M-pa Radios

OPTION NO.	FRONT COVER ASSEMBLY	CONTROL BOARD	AEGIS MODULE	
			PART NO.	MANUAL
PAVS	19D438676G5 * or 19D903620G1	19D903081G1	344A3659P3	LBI-38829
PAVE and PAV0	19D438676G5 * or 19D903620G1	19D903081G1	344A3659P4	LBI-38830

* earlier radios used Front Cover Assembly 19D438676G5

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T/R Output

Port C of U7 provides an additional output on pin 18. T/R is used in several points throughout the Control Board to enable and disable various circuitry during transmit and receive modes. T/R is high when the radio is transmitting and low when the radio is receiving. U9F buffers and inverts T/R and applies the inverted level to J1/P1 pin 8, the UDC Flex and UDC pin 10.

PWR_CNTL Output

PWR_CNTL is an output from U7 pin 14 that is delivered to the RF Board via J102/P2 pin 4 (5.4V ENABLE). Using this logic line, the I/O Microcontroller can power-down most of the circuitry of the RF Board to conserve battery power. PWR_CNTL is low when the RF Board is powered-down.

VGCONV Output

The VGCONV output on U7 pin 19 is high when the radio is operating in Aegis digital or private mode and it is low when the radio is in clear mode. VGCONV is connected to two control inputs of triple 2-channel analog switch U1.

When the radio is in clear mode, with VGCONV low, U1C pin 14 is switched to pin 12. This action routes the internal or external microphone audio from U1B pin 15 to the microphone pre-emphasis amplifier/limiter U5C, and then the Audio Processor. Also, when VGCONV is low, U1A pin 4 is switched to pin 5. This switch action tailors the response of audio buffer/filter U5D for clear mode receive audio.

When the radio is in Aegis digital or private mode, with VGCONV high, U1C pin 14 is switched to pin 13. This action grounds the input of U5C to prevent any clear (analog) mic audio from entering the Audio Processor. In addition, U1A pin 4 is switched to pin 3 to tailor the response of U5D for the Aegis digital or private receive audio.

DSP_PWR and FLOAT Outputs

The DSP_PWR and FLOAT outputs from U7 pins 3 and 9 are connected to the Aegis Module via J7/P7 pins 4 an 3 respectively. Power-down operation of the DSP and related ICs on the Aegis Module is controlled by these two logic lines. Both outputs are high when the radio is operating is clear mode.

When the radio switches to Aegis digital or private mode, DSP_PWR transitions low. This enables the 5-Volt regulator IC (U12) on the Aegis Module. Next, FLOAT transitions low to enable hex buffer U6 and 4-bit counter U4 on the module.

UDC_MUTE Output

Pin 44 of U7 provides the UDC_MUTE line to UDC pin 11. This output line is low when the speaker audio is muted. The UDC Flex provides the interconnection between J1/P1 pin 2 and the UDC. Several of the UDC connectable audio accessories that contain a speaker amplifier use this line to mute their internal speaker amplifier.

Microprocessor U18, PROM, RAM and EEPROM

Microprocessor U18 is an 80C52 8-bit processor. U18 reads the personality information programmed into EEPROM U17 and controls the radio by communicating with the I/O Microcontroller. It also controls all Aegis related functions of the radio.

Four (4) serial lines between I/O Microcontroller U7 and Microprocessor U18 provide the interprocessor communications path between the chips. See **Interprocessor Communications** for details.

External memory for U18 includes 64K x 8-bit PROM U15, 8K x 8-bit EEPROM U17 and 8K x 8-bit static RAM U16. U18's control program is located in the PROM and the EEPROM stores personality information. The RAM is primarily used for buffering digital data.

Connectors J6/P6 interconnect the 8-bit address/data bus, one address line, and several microprocessor control lines between U18 and the Aegis Module. U18 transfers data between the Aegis Module and itself using these interconnections.

Operating power (5.0 Vdc) for U18 is applied to pin 38. The power-on reset pulse is applied to U18 pin 4. See **Regulator Circuits** and **Microprocessor Reset Circuits** for details.

An 11.0592 MHz clock signal for U18 is generated from the oscillator circuit in modem U19 and crystal Y3. This clock signal is applied to U18 pin 15 from pin 14 of the modem.

Address And Data Bus

The 80C52 has a multiplexed low-order address and 8-bit data bus provided by port 0 of U18, latches U13 and U14. When U18 access external memory it latches address lines A0 - A7 from the address/data bus into the latches. These lower address lines appear on the eight outputs of U13 and U14 (pins 9, 10, 15 and 16) when the latch enable (ALE) pulse from U4 pin 27 is high; the low-order address is latched when the pulse returns low. Data is then transferred to and from U18 after the address is latched.

The ALE pulse is applied to the two latches, the PROM and modem. Pulse frequency is 1/6 of the clock frequency at U18 pin 15; however, one out of every six pulses is skipped when U18 accesses memory.

Port 2 of U18 provides the high-order address lines, A8 - A15. These eight (8) address lines are applied to the external memory and the address decoding logic.

Chip-Enable and Address Decoding Logic

PROM U15 chip-enable pulses from U18 include the ALE pulse on U15 pin 22 and the PSEN pulse on U15 pin 24. RAM U16 chip-enable pulses include the read and write control lines from U18 pins 12 and 13 and a chip-select line from decoder U20 pin 14. Modem U19 chip-enable lines from U18 also include the read and write control lines from U18 and a chip select line from decoder U20 pin 13. All of these lines are active when low.

Address lines A13 - A15 are applied to address decoder U20. This IC provides the memory mapped chip-enable pulses to the modem and RAM via pins 13 and 14 respectively. U20 also supplies the Aegis Module with two enable pulses via pins 12 and 15.

Inverter U9E buffers the pulse from U20 pin 12 to provide the CRYPT_CS pulse on J6/P6 pin 12. CRYPT_CS is active when high.

DSP_CS pulse on J6/P6 pin 13 is a logical OR of the enable pulse from U20 pin 15 and the DSP_PWR line from the I/O Microcontroller. NOR gate U24D and inverter U9A form the OR gate. Both inputs must be active (low) before the DSP_CS will become active (low).

Interrupt Inputs

Two interrupt inputs to U18 provide immediate program control when needed. Modem U19 interrupts U18 using its output on pin 24. This interrupt signal is applied to U18 pin 9. An interrupt line from the DSP IC on the Aegis Module, DSP INT on J5/P5 pin 10, is used when the DSP requires immediate attention from U18. DSP INT is applied to U18 pin 8.

Interprocessor Communications

I/O Microcontroller U7 and Microprocessor U18 communicate using four interconnecting lines. UP_HS_OUT, UP_HS_IN, UP_DATA and UP_CNTL provide all handshake, data and control signals for message transfers between the two chips. Messages transfers consist of one or more byte transfers.

Each processor has a handshake input and a handshake output. A common bidirectional data line, UP_DATA, is shared by the chips. A control line, UP_CNTRL, is an output from U18 to U7.

Message transfers from U18 to U7 are primarily commands which cause U7 to execute a commanded function. Some examples include power-up status, Keypad Flex scan, LCD load, Audio Processor A/D converter write/read, synthesizer load, and tone generation. All U18 to U7 message transfers are initiated by a low pulse on UP_CNTL.

Message transfers from U7 to U18 include status data such as power-up status report, key(s) pressed, UDC device connected, volume control position, synthesizer lock status and squelch status. U7 to U18 transfers are initialized by U7 pulling its handshake output (UP_HS_IN) low.

Modem U19

Modem U19 is connected to U18 by the 8-bit data bus. This chip provides the data link when digital communications are in process. It also provides the data link to and from the site controller equipment over the control channel in trunking applications. U19 performs the parallel-to-serial and serial-to-parallel conversions for transmit and receive modes respectively. The serial baud rate is 9600 bps.

Table 2 - Interprocessor Communication Lines

NAME	USE	U18 DIRECTION	U7 DIRECTION
UP_DATA	Data Line	Bidirectional	Bidirectional
UP_HS_IN	Handshake Input	Input	Output
UP_HS_OUT	Handshake Output	Output	Input
UP_CNTL	Control Line	Output	Input

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In receive mode, discriminator audio/data (RX_DISC) from J101/P1 pin 4 is amplified by U5B and applied to the data demodulator circuit comprised of comparator U12C, capacitor C3 and the associated resistors. Data pulses from U12C pin 14 are applied to the U19 pin 19 for serial-to-parallel conversion via RX_DATA. U19 then interrupts U18 so it can read the data and act accordingly.

When transmitting digital data, U18 loads U19 with data. U19 then performs the parallel-to-serial conversions and the serial data (RF_TX_DAT) appears on pin 21. RF_TX_DAT is applied to filter U10C to "round-off" the pulses. The filtered signal from U10C pin 8 is then routed through the Audio Processor to filter U10A. The output on U10A pin 1 (RF_TX_AUD) is applied to the modulation circuitry on the RF Board via J102/P2 pin 1.

Audio Processor U8

Audio Processor U8 performs most audio functions and all digital-to-analog and analog-to-digital conversions for the radio. U8 also has several switched outputs (open-drain) that are used to control various radio functions. I/O Microcontroller U7 directly controls U8 via the serial bus. See **I/O Microcontroller U7** for details on the serial bus interface.

Audio functions performed by the chip include transmit and receive audio routing, transmit audio limiting, transmit deviation level control, and receive audio volume control. Channel Guard and Digital Channel Guard features of U8 include an encode/decode filter, limiter, and a receive audio CG reject filter. U8 also performs squelch operations using its high-pass filter, rectifier, comparator and A/D conversion circuity.

D/A And A/D Conversions

When the radio is transmitting, a digital-to-analog converter and a sample-and-hold circuit inside U8 are used to control transmitter power. I/O Microcontroller U7 generates a voltage via the D/A converter corresponding to the programmed RF output power. The output of the sample-and-hold circuit is on U8 pin 51 (RF_PWR_SET) and is connected to J101/P1 pin 1 (PWR SET).

The I/O Microcontroller uses this D/A converter, a comparator and a multiplex switch in U8 to sample any one of four analog inputs to U8. The four (4) analog inputs are: squelch (COMPA or AOUT, U8 pin 55); UDC resistor (COMPB, U7 pin 58); volume control position (COMPC, U8 pin 59); and battery voltage (COMPD, U8 pin 2). U7 first loads U8 with data to select one of the four analog inputs and it loads data into U8 to generate an output voltage from U8's internal D/A converter. A comparator inside U8 then compares the selected analog input (COMPA - COMPD) to the D/A generated voltage. U7 then samples the D/A comparators's output of U8 (DA_COMP or COMPOUT, U8 pin 43) and it then loads new data into U8 to step the D/A analog voltage up or down and determine the exact transition point of the comparator, and thus the selected input voltage.

Oscillator Circuit

An oscillator circuit in U8 and crystal Y1 provide an 8 MHz clock for U8's internal timing. The crystal is connected to U8 pins 30 and 31.

This oscillator's frequency can be slightly shifted to move clock harmonics or "birdies" relative to desired radio operating frequency. This feature is programmable into the radio on a per-channel basis. The oscillator's frequency is shifted by switching load capacitors C89 and C90 into or out of the circuit using pin diodes D4 and D5. With the SW4 output of Audio Processor low (U8 pin 37), U3A pin 1 is near ground. This reverse biases the pin diodes which disconnects C89 and C90 from the low impedance to ground provided by C15. When SW4 is switched high, the pin diodes are forward biased, thus slightly shifting the oscillators frequency. Integrator R73/C92 insures a gradual change of the control voltage providing oscillator stability during the frequency shift.

Switched Outputs

The Audio Processor has six (6) switch outputs, SW0 - SW5, that control various functions on the Control Board. The outputs are open-drain type and are pulled high by the associated pull-up resistor. See Table 3 for details.

Table 3 - Audio Processor Switched Outputs

NAME	U7 PIN	PULL-UP RESISTOR	USE	OUTPUT HIGH (Or Hi-Z)	OUTPUT LOW
SW0	33	R35	Audio Amplifier U21 Switched Power	On	Off
SW1	34	R40	UDC Switched Battery Power (UDC pin 4)	On	Off
SW2	35	none	Conventional Squelch Response	Fast	Slow
SW3	36	none	Conventional Mode - Channel Guard Trunked Mode - Low-Speed Data Decode	Decode Enabled	Encode Enabled
SW4	37	R124	U8/Y1 Oscillator Shift	Shifted	Not Shifted
SW5	39	R36	Internal Or External Microphone Select	Internal	External

Regulator Circuits

Four (4) linear regulator circuits on the Control Board develop regulated dc supplies from the radio's battery supply. Surface-mounted regulator ICs make-up two of the regulator circuits. A precision dc reference IC, 1/2 of a quad operational amplifier IC, and several transistors form the other two.

VCC and VFNT Supply

Regulator IC U2 supplies 5.0 Vdc (VCC) to the digital circuits on the Control Board. Input battery power (Vbat, typically 7.5 Vdc) is supplied to U2 pin 8. The regulator's output is on pin 1. This low drop-out voltage regulator IC can maintain a well regulated output even if the battery voltage falls to approximately 5.6 Vdc. The IC also provides output over-voltage and current limit protection.

Regulator IC U4 supplies 5.5 Vdc (VFRNT) to the Keypad Flex and LCD Board circuits in the Front Cover Assembly. Input battery power (Vbat) is supplied to U4 pin 6. The regulator's output from pin 4 (VFRNT) is delivered to the Front Cover Assembly by J4/P4 pin 1. This IC also has low drop-out voltage regulation and current limit protection.

VCCA and RF5.4 Supply

The two regulated supplies formed by the precision dc reference IC, 1/2 of a quad operational amplifier IC, and the driver transistors power the analog circuits on the Control Board (VCCA), and the RF Board in the Rear Cover Assembly (RF5.4 and 5.4_TX). Integrated circuit U11 is a precision voltage reference device that supplies a 2.5 Vdc reference (Vref) to the VCCA and RF5.4 regulator circuits (operational amplifier U3 pins 5 and 9).

Operational amplifier U3B, transistors Q6 and Q7, and associated components form the VCCA regulator circuit. U3B operates as an error amplifier by sensing the 2.5 Vdc reference voltage on its non-inverting input (pin 5) and the divided-down output of the supply (via R17 and R137) on its inverting input (pin 6). By sensing these two voltages, U3B increases or decreases the base current into the buffer and pass transistors, Q6 and Q7 respectively. This action maintains a regulated 5.4 Vdc output at the collector of Q7.

Operational amplifier U3C, transistors Q5 and Q9, and associated components form the RF5.4 supply for the RF Board. This 5.4 Vdc supply is applied to the RF Board by J102/P2 pin 6. Operational amplifier U3C operates as an error amplifier similar to U3B. Its output drives pass transistor Q9. Transistor Q5 limits the current of the supply to approximately 250 mA maximum.

When the radio is transmitting, 5.4 Vdc from Q9's collector is also applied to J101/P1 pin 5. This source (5.4_TX) powers the transmitter circuits on the RF Board. When the radio is transmitting, the T/R line from Microcontroller U7 is high. This saturates (turns on) transistors Q2B and Q10.

VCCA/2 Reference Voltage

Op-amp U5A develops a voltage reference equal to one-half the VCCA supply. This 2.7 Vdc reference voltage is used on several points on the Control Board for the audio circuits. Resistors R94 and R95 divide the VCCA supply by two. The divided voltage is connected the non-inverting input of U5A. Configured as a voltage follower, U5A then buffers this voltage to form the VCC/2 reference voltage.

Microprocessor Reset Circuits

A reset pulse, RESET_IN (high = reset, low = run), is applied to modem IC U19 when the radio is turned on. Logic circuitry in U19 resets its internal circuitry and a reset output from U19 resets all of the microprocessor circuitry on the Control Board. RESET_IN will also pulse if the battery voltage falls below approximately 6.0 Vdc. RESET_IN is developed from comparators U12A and U12B. When a fully charged battery pack is connected to the radio and it is turned on, RESET_IN will go high for approximately 20 ms; it then transitions and stays low.

At turn on, comparator U12A samples the divided-down battery voltage (via R142 and R139) on its non-inverting input. This voltage is compared to the 2.5 Vdc reference voltage (Vref) applied to U12A's inverting input. If the battery voltage (Vbat) is at least 6.0 Vdc, U12A pin 2 goes high. This high reverse biases diode D6 and allows R75 to charge C31. U12B compares C31's charge to Vref. Approximately 20 ms after turn on, C31 charges to 2.5 Vdc and the RESET_IN output at U12B pin 1 goes low. NOTE: All of U12's outputs are open-collector type that are pulled high by the associated pull-up resistors.

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The RESET_IN pulse is applied to modem U19 pin 25. Logic in U19 resets its internal circuitry and a second reset pulse, (high = reset, low = run), appears on U19 pin 3 (RSTOUT). This output from U19 pin 3 resets Microprocessor U18 through R135, and I/O Microcontroller U7 and Audio Processor U8 through inverter U12D. The RESET/ output (low = reset, high = run) from U12D is applied to U7 pin 41 and U8 pin 49.

Modem U19 has an internal "watch dog timer" circuit that will pulse pin 3 (RSTOUT) high for 50 us if it is not serviced by U18 at least every 1.75 seconds. This pulse will reset all of the microprocessors, and thus the radio.

RF Bypassing

Numerous bypassing capacitors are located throughout the Control Board. These capacitors primarily suppress digital noise generated on the board from entering the RF circuits and prevent radiated RF power from upsetting circuits on the board.

Clear Mode Transmit Audio Path

When the radio is transmitting in clear mode, microphone audio passes through Audio Processor U8 before it is routed to the Rear Cover Assembly as a modulating signal. Audio from the internal microphone will be applied to U8 unless an external microphone is connected to the UDC. If an external microphone is connected when the radio is turned on, audio from the external microphone will be routed to U8 for processing and the internal microphone will be disabled.

Internal And External Mic Audio Amplifiers U6A and U6B

Internal and external microphone audio (MIC HI and EXT MIC HI) are amplified by U6A and U6B respectively. Typical signal levels on the mic high audio inputs are 10 - 30 mV rms with average speech into the mic. Both stages have a voltage gain of approximately seven (7).

The electret microphones used in/with the Aegis M-PA radios require a dc bias for operation. Resistors R90 and R89 provide dc mic bias from the VCCA/2 source for the mic audio lines. Approximately 2.2 Vdc will appear on a mic high audio line when a microphone is connected. The output of both microphone amplifiers is applied to U1B for internal/external mic selection (U1B pins 1 / 2 respectively).

Internal/External Mic Audio Selection

When the radio is turned on, I/O Microcontroller U7 checks the UDC to determine if any external option (such as a microphone) is connected to the UDC. U7 monitors the COMPB input on U8 pin 58 to determine the voltage on UDC pin 9. See **I/O Microcontroller U7**, **Audio Processor U8 Interfacing** for details on the A/D conversion process. This voltage is developed by the voltage divider formed by R31, R58 and the resistor in the external option (if connected).

If no option is connected to the UDC when the radio is turned on, U8 pin 58 (UDC VOLT) will be pulled to 5.4 Vdc by R31; U7 will then route the internal microphone audio to U8 and disable the external mic audio. U7 performs this by loading data into U8 to switch its SW5 output on pin 39 high. This high switches the internal mic audio signal on U1B pin 1 to the common terminal on U1B pin 15. The internal mic audio signal is then routed to clear/digital mic audio switch U1C.

If an external microphone is connected to the UDC when the radio is turned on, U8 pin 58 will be approximately 2.5 Vdc; U7 will route the external microphone audio to U8 and disable the internal mic audio. U7 performs this by loading data into U8 to switch its SW5 output on pin 39 low. This low switches the external mic audio signal on U1B pin 2 to the common terminal on U1B pin 15. The external mic audio signal is then routed to clear/digital mic audio switch U1C.

Clear/Digital Mic Audio Switch U1C

When clear transmit mode is enabled, the VGCONV output from U7 is low. This switches U1C to allow the mic audio from U1B pin 15 to pass to the input of pre-emphasis amplifier/limiter U5C. Mic audio is routed through U5C in clear mode only.

Amplifier/Limiter U5C

When clear transmit mode is enabled, mic audio is pre-emphasized, amplified, and limited by U5C. This stage provides an approximate voltage gain of seven (7). The mic audio on U5C pin 8 is limited to approximately 1.2 Vp-p. This output is applied to U8 pin 14. Additional limiting is performed by U8.

Audio Processor U8

Clear microphone audio from U5C is applied to Audio Processor U8 pin 14. U8 has audio limiting stages for the mic audio. This IC also combines tones generated by the microprocessors and routes the combined transmit audio signal to filter U10A. The Audio Processor also has a digital deviation level control for the transmit audio.

Channel Guard, Digital CG or low-speed data generated by walsh bit summer R131 and R132 are applied to U8 pin 5 as CG_IN. High-frequency components are removed by U8 and the output appears at pin 6. From here the signal is applied to U8 pin 20 where it is then summed with the transmit (mic) audio.

Radio models equipped with DTMF and/or GE-STAR features apply these microprocessor generated tones from U7 to U8 pin 15. See **I/O Microcontroller U7**, **Audio Processor U8 Interfacing** for details.

Filter U10A

The transmit audio output from U8 pin 26, with the appropriate tones, is filtered by U10A before being sent to the Rear Cover Assembly as the modulating signal. The output on U10A pin 1 is riding on a 2.7 Vdc bias. This audio signal is approximately 1500 mVp-p at full deviation.

Digital/Private Mode Transmit Audio Path

When the radio is transmitting an Aegis digital or a private (encrypted) signal, clear microphone audio does not pass through the Audio Processor. Instead, it is routed directly to the Aegis Module. Microprocessor U18 and the Aegis Module digitize and encrypt (if optionally equipped and operating in private mode) the mic audio and pass it to modem U19. The modem then passes 9600 bps data to the Audio Processor via filter U10C. The Audio Processor routes the transmit data to the Rear Cover Assembly via filter U10A.

Internal/external mic audio amplification and selection is identical to clear mode except the mic audio does not pass through U5C.

Clear/Digital Mic Audio Switch U1C

VGCONV is high when Aegis digital or private transmit mode is enabled. This causes U1C pin 14 to switch to pin 12, thus grounding the input of U5C to prevent any clear mic audio from passing to the Audio Processor. The mic audio passes to buffer amplifier U10B via the VG_TX line.

Buffer Amplifier U10B

Mic audio from switch U1B pin 15 is routed to buffer amplifier U10B via the VG_TX line. The output of U10B is applied to the Aegis Module for digitalization and compression via connector J5/P5 pin 4 (CODEC_IN).

Encryption (Optional)

Details on the encryption process can be found in the manual associated with the Aegis Module. See Table 1. After the signal is encrypted, it is applied to modem U19 for parallel-to-serial conversion.

Serial Data Path

The serial data signal (Aegis digital or private) from modem U19 is then routed to the Rear Cover Assembly to modulate the transmitter via U10C, U8 and U10A. Trunked mode data from the modem is also routed to the transmitter (trunked radios only) using this path.

The data signal from the modem, RF_TX_DATA, is applied to filter U10C. This stage rounds the square-wave pulses from the modem, thus preventing any high-frequency components from reaching the modulating circuits. U10C's output is on pin 8. The filtered data signal is applied to U8 pin 21. U8 routes this signal to the TXOUT output, U8 pin 26.

Additional filtering of the transmit audio signal is performed by U10A. The output from U10A pin 1 is routed to the Rear Cover Assembly via connector J102/P2 pin 1. This signal, RF_TX_AUD, modulates the transmitter. RF_TX_AUD is typically 1000 mVp-p when the radio is transmitting a digital signal.

Clear Mode Receive Audio Path

Audio signals from the RF Board appear on P1 pin 4 (RX_DISC). A standard modulated RF signal at the receiver's antenna produces approximately 300 mVp-p on P1 pin 4. The radio will operate according to the following paragraphs when a valid digital voice signal is not detected.

Buffer Amplifier U5B

The RX_DISC signal is amplified by U5B on the Control Board and applied to the Audio Processor, the RX_DATA demodulator U12C, and UDC pin 34. Clear mode receive audio will not generate valid data signals on the output of U12C; therefore, the modem will not interrupt U18 and the radio will operate in clear mode.

Operational amplifier U5B and associated components provide an approximate voltage gain of 3.5 for the RX_DISC signal. Audio signals appearing on the output (U5B pin 7) are riding on a 2.7 Vdc bias as set by the VCCA/2 dc voltage on U5B's non-inverting input. Transistor Q4B prevents feedback from the receiver from interfering with the transmit audio. This transistor turns on when the radio is transmitting (when T/R is high).

Audio Processor U8

The amplified RX_DISC signal at U5B pin 7 is applied to Audio Processor U8 pin 12 for processing. Processing for the audio that will be applied to the speaker includes squelch, CG rejection, and volume control.

When squelch operation is based on receiver noise, the noise squelch circuit in the Audio Processor operates as follows: The received signal is attenuated by voltage divider R119/R81 and the higher frequency components are applied to U8 pin 3. This signal is high-pass filtered and rectified in U8 and applied to pin 4. Integrator C12, C25 and R82 filter the rectified signal to provide a dc voltage proportional to receiver

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noise. The SW2 output on U8 pin 35 is switched off (high-impendance)

on radios equipped and operating in conventional priority scan mode. This provides faster squelch response which is needed during priority scan. The rectified/filtered signal is next applied to a dc amp, multiplexer switch and the squelch comparator in U8. The amplifier's output can be monitored on U8 pin 55. This dc voltage is then compared to squelch threshold value from the D/A converter and the output appears on D/A_COMP (U8 pin 43). The I/O Microcontroller reads the D/A_COMP line to determine if the noise level is low enough to unsquelch the receiver. If it is, U7 commands U8 to allow the audio to pass via U8's squelch switch.

When receive Channel Guard (CG) or Digital Channel Guard (DCG) is enabled, audio applied to the Audio Processor U8 pin 12 is routed through a CG low-pass filter. This filter removes voice components and the tones appear on U8 pin 11 (CG_LIM). U7 then decodes the CG_LIM signal as described in **I/O Microcontroller U7**, **Audio Processor U8 Interfacing**. If the tone programmed for the selected channel is decoded, U7 opens the squelch gate inside U8.

The I/O Microcontroller reads the volume control on the Keypad Flex via the VOLUME input on U8 pin 59. VOLUME is approximately 0 Vdc when the volume control knob is fully counter-clockwise and it is approximately 5.4 Vdc when the control is fully clockwise. This analog voltage is digitized by U7 and U8. I/O Microcontroller U7 then loads the digitized value into U8 to set the digital volume attenuator in U8.

After passing through the squelch, CG reject filter, and the volume attenuator circuits, the audio signal is applied to U8 pin 27.

Audio Buffer/Filter U5D

The receive audio output at U8 pin 27 is de-emphasized by audio buffer/filter U5D. De-emphasized RX_AUDIO is routed to speaker amplifier U21 via C2. RX_AUDIO is also coupled to UDC pin 3 via C28 and the UDC Flex.

Speaker Amplifier U21

Speaker amplifier U21 amplifies the de-emphasized audio to provide a minimum of 1/2 Watt of audio power to the speaker. Differential outputs from U21 drive the speaker via J3/P3 pins 2 and 3 and the Speaker Flex. Typical signal level at each differential output (referenced to ground) is 5.0 Vp-p at full volume.

U21 is switched off when the radio is squelched to conserve battery power. It is powered-up when the SW0 output from U8 pin 33 is high. Battery power (Vbat) to U21 pin 2 is switched on by transistors Q3B, Q12B and Q13. Transistor Q3B provides control signal buffering from the SW0 output from U8, Q13 is the switch, and Q12B provides current limiting.

Transistors Q3A, Q12A and Q11 form an identical circuit for powering a speaker/microphone audio accessory, or the PC interface during programming. This microprocessor switched battery power (UDC_SW_BATT) is applied to UDC pin 4.

Digital/Private Mode Receive Audio Path

When receiving, the radio will switch to Aegis digital or private mode when a valid data format is received. The digital/private mode receive audio path is as follows:

Demodulator U12C And Modem U19

When the radio is receiving data, comparator U12C and associated components demodulate the RX_DISC signal to provide the 9600 bps RX_DATA signal to the modem. R98 and C3 form an integrator that applies a dc level to U12C's inverting input. This dc level is an average of the received (data) signal. The comparator transitions according to the "non-return to zero" signal on its non-inverting input. Hysteresis for the circuit is provided by R77. RX_DATA pulses from U12 pin 14 are applied to the modem for serial-to-parallel conversion.

Modem U19 contains a synchronization circuit that allows it to sync to an incoming data signal. Upon sync, U19 interrupts U18. U18 then reads the data from the modem and transfers it to the Aegis Module via connectors J6/P6.

Decryption (Optional)

Details on the decryption process can be found in the manual associated with the Aegis Module. See Table 1.

Receive Audio Path

After the data is decoded (and decrypted if in private mode), the expanded and converted analog audio from the Aegis Module appears on J5/P5 pin 3 and is applied to Audio Processor U8 pin 13. The audio is then routed through U8 to pin 27. From this point, the path of the audio (through U5D and U21) to the speaker is identical to the normal clear mode audio. Audio buffer/filter U5D's audio response is controlled by the VGCONV output from I/O Microcontroller U7. See **I/O Microcontroller U7**, **VGCONV Output** for details.

TROUBLESHOOTING

The following outline will help lead the service technician to a problem with the Control Board, Aegis Module or another associated circuit in the Front Cover Assembly. The Control Board should be removed and electrically extended for troubleshooting access. Use the adapter board and the extender cable in SPK9011 Front Cover Test Accessory Kit.

TESTING WITHOUT THE AEGIS MODULE

All clear mode tests may be performed with the Aegis Module removed from the Control Board. The Control Board senses that the Aegis Module is not present and it operates normally in clear mode. The radio will display one of several errors if it is powered-up on a group (trunked radios only) or channel programmed for Aegis digital or private operation. Details on the error messages can be found in the maintenance manual for the Aegis Module. See Table 1.

CAUTION

ALWAYS remove the battery pack before disassembling the unit to avoid blowing the fuse or causing other component damage.

This radio contains CMOS ICs that can be damaged by static electricity. Observe static handling precautions.

SYMPTOM AND CAUSE OUTLINE

Completely Inoperative Radio

Check Power Supplies

Power supplies should be the first area to check in the event of a completely inoperative unit. The battery fuse is located in the Battery Plate on the bottom of the radio. If the radio is dead, check the fuse. Table 4 lists supply current for various operating modes.

Power into the radio (7.5 Vdc battery voltage) can be tested by monitoring the input connections H1 and H2 (screw mounting points) located at the bottom of the Control Board. If dc power is not present at this point, suspect fuse F1 or the battery connections.

Regulated supplies included on the Control Board are the digital 5.0 Vdc supply (VCC), the analog 5.4 Vdc supply (VCCA), a 5.5 Vdc supply for the Keypad Flex and LCD Board (VFRNT), and a 5.4 Vdc supply used to power the RF Board in the Rear Cover Assembly (RF5.4).

Both of the 5.4 Vdc supplies (VCCA and RF5.4) can be tested by monitoring the voltage at the collector (center terminal) of the associated pass transistor (Q7 and Q9). These regulated supplies should be stable to within 0.1 Vdc during each operating mode (transmit, receive, standby, program). If both are in error, check zener reference U11. Pin 8 of U11 should be 2.5 Vdc ±0.05 Vdc.

The 5.0 Vdc (VCC) and 5.5 Vdc (VFRNT) regulated supplies should be within ±0.25 Vdc. Supply failure may indicate a shorted decoupling capacitor on the associated supply rail. In addition, failure of the 5.5 Vdc supply U4 may indicate a short on the Keypad or LCD Board. Temporarily disconnect the J4/P4 flex connection to verify there is no short on the Keypad Flex or the LCD Board.

Table 4 - Typical Battery Current

OPERATING MODE	BATTERY CURRENT (at 7.5 Vdc)
Program	< 100 mA
Receive (Squelched)	< 100 mA
Receive (Rated Audio)	< 300 mA
Transmit (Low Power)	< 1250 mA
Transmit (High Power)	<1900 mA

Check Reset Logic

When the radio is powered up, monitor the reset pulse at TP5 (U18 pin 4) from the modem's reset output (U19 pin 3, RSTOUT). Trigger the scope on the rising 7.5 Vdc power supply. This pulse should stay high 10 - 30 milliseconds, then transition and stay low. If TP5 remains high the radio will be inoperative since the microprocessors are not released from reset. Also verify that the RESET/ pulse at U7 pin 41 from inverter U12D is an inverted pulse.

If a problem exists with the pulse on TP5 check RESET_IN at TP9 (U12B pin 1). TP9 should also stay high for 10 - 30 ms after turn on. If this signal is good, suspect a problem in the modem IC or a shorted input on U18 pin 4 or U12D pin 10. If the pulse at TP9 is not good, troubleshoot the reset comparators U12A, U12B and the associated RC networks. NOTE: U12 has open-collector outputs. If TP9 remains high, it can be temporarily shorted to ground to eliminate a problem with the reset comparator circuit.

Slowly lower the battery supply voltage until TP9 transitions high. This should occur at an approximate battery voltage of 5.7 Vdc. Next, slowly raise the supply voltage and verify that TP9 returns low. There should be approximately 0.2 Vdc hysteresis.

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Check Clocks

Monitor TP4 near crystal Y2 on the component side of the printed wire board. This is the 2.00 MHz clock for the I/O Microcontroller. NOTE: Use an oscilloscope with a x10 probe or a frequency counter that has a high input impedance (at least 10M ohms). Replace Y2 if this clock frequency is in error. Suspect Y2 or U7 if no signal is present. Generally, if the crystal is defective (open), ≈2.5 Vdc will be present at TP4 and no signal will be present.

Check TP8 (U19 pin 14) for an 11.0592 MHz clock from the modem IC to the U18. NOTE: Use an oscilloscope or a frequency counter that has a high input impedance. Suspect Y3 if this clock frequency is in error. Suspect Y3 or U19 if no signal is present.

The Audio Processor's clock will also have to be operating for proper audio and A/D converter operation. This 8 MHz clock signal is also applied to the Aegis Module. Monitor J5/P5 pin 7 for an 8 MHz square-wave output from U8. Replace crystal Y1 if this clock frequency is in error. Suspect Y1 or U8 if the signal is not present.

Check Keypad Scanning

Approximately every 50 milliseconds pulse activity should be present on the serial lines to and from the Keypad Flex. See Figure 1. These pulses are loading a data byte into shift register U2 and reading U1 on the Keypad Flex. The Audio Processor is also being read and written to at this time. If these signals are not present, I/O Microcontroller U7 is not operating properly and it may not be communicating with Microprocessor U18.

1. Verify U7 pin 38 and U18 pin 38 are 5.0 Vdc. Troubleshoot the VCC regulator if incorrect.

2. Verify all clocks are operating.

3. Check TP5. After the initial reset pulse, TP5 should stay low. If TP5 goes low at the initial reset pulse, but then pulses high for 50 microseconds every two (2) seconds, U18 is not operating.

4. See "Check Inter-processor Communication".

Check Inter-Processor Communication

Inter-processor communication failure will generally cause the unit to appear dead at power-up or flash all of the segments in the display and beep. If this symptom occurs, first double-check power, clock and reset inputs to U7 and U18 before suspecting a failed U7 or U18.

I/O Microcontroller U7 is most likely good if keypad scanning is good. U18 or its support circuitry may be at fault. Check the PROM, RAM and EEPROM for VCC power and monitor the ALE pulse from U18 pin 27. ALE pulse frequency is 1/6 of the clock frequency at U18 pin 15; however, one out of every six pulses is skipped when U18 accesses memory. If the ALE pulses are not present and the VCC, reset and clock to U18 are good, suspect U18.

Synthesizer Not Locking Properly

Each time the channel is changed, the PTT Button is pressed or the PTT Button is released, the I/O Microcontroller serially loads the synthesizer IC on the RF Board with new TX or RX data. If the synthesizer does not lock or stay locked, the following should be observed:

- the radio continuously or intermittently beeps
- "NO LOCK" flashes in the display
- LOCK DETECT (J102/P2 pin 8) is low or pulsing flagging the I/O Microcontroller of the unlocked condition

If the above condition occurs, the I/O Microcontroller should continue to try to reload the synthesizer IC with data until the synthesizer locks.

Synthesizer lock failure can be caused by a problem on the RF or Control Boards. If the radio locks only on some frequencies (for example high-side channels) the problem is most likely on the RF Board (the VCO or prescaler circuits for example). The below checks deal with problems associated with the Control Board.

Table 5 - Clock Test Points

TEST POINT	CRYSTAL/IC	FREQUENCY (MHz)	MAX. ERROR (Hz)
TP4	Y2 / U7	2.0000	±300
TP8	Y3 / U19	11.0592	±800
J5 pin 7	Y1 / U8	8.0000	±600

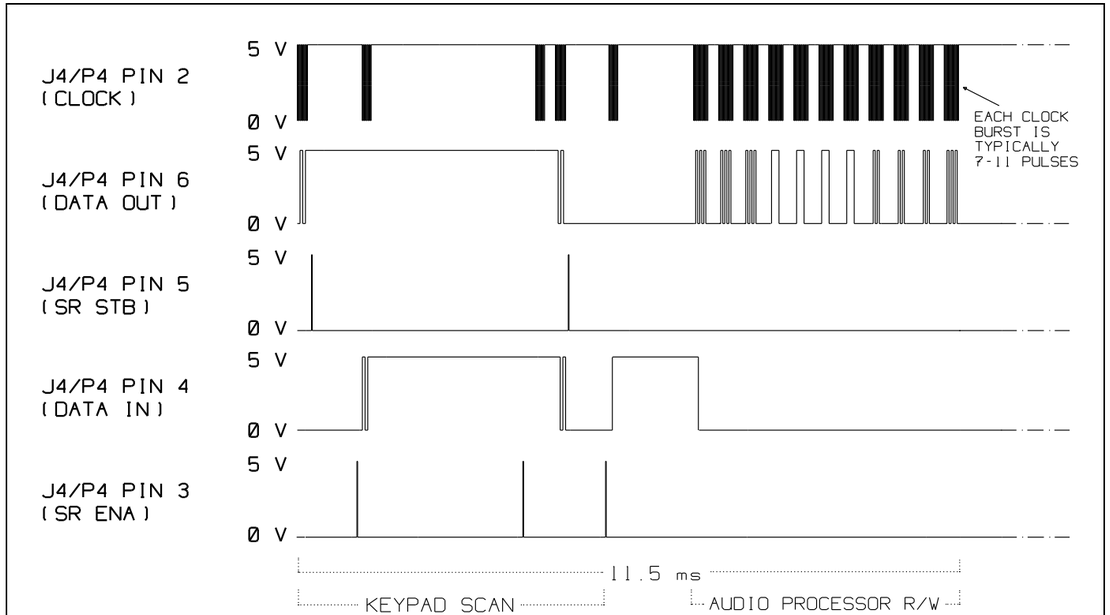

Figure 1 - Keypad Scanning Waveforms

1. Read the radio personality with the PC Programmer and reprogram the unit to verify there is

   good Channel Data for each channel programmed into the radio. If channels are in error, suspect EEPROM U17 or previous programming.

2. On connectors J101/P1 and J102/P2, verify the 5.4 Vdc supply (RF5.4V) to the RF Board is within ±0.1 Vdc, 7.5 Vdc BATT is present, and TX 5.4 V is low (RX mode).

3. Monitor the synthesizer load pulses (J102/P2 pins 9, 10 and 11) for pulse activity when a channel is changed. See Figure 3. If these signals are not present, suspect a defective I/O Microcontroller. A failure of only one signal points to an open series resistor on the Control Board or a defective output from U7. NOTE: Temporarily connect LOCK DETECT (J102/P2 pin 8) to ground to view these waveforms.

4. Verify the band switch line, SYN BSW (J102/P2 pin 3), is at the correct logic level. See the Rear Cover Assembly maintenance manual for details on the logic level versus VCO output frequency. Suspect the I/O Microcontroller if there is a problem. Note that some RF Boards do not use the SYN BSW line.

5. Suspect the RF Board if all of the outputs to it are good.

Radio Will Not Program

Check PC Programmer Power

The Control Board must first recognize the programming resistor (short to ground at UDC pin 9) with the PC Interface connected. It should then supply 7.5 Vdc (battery power, current limited by Q12A) to the PC Interface via UDC pin 4 (SW BAT / UDC_SW_BATT).

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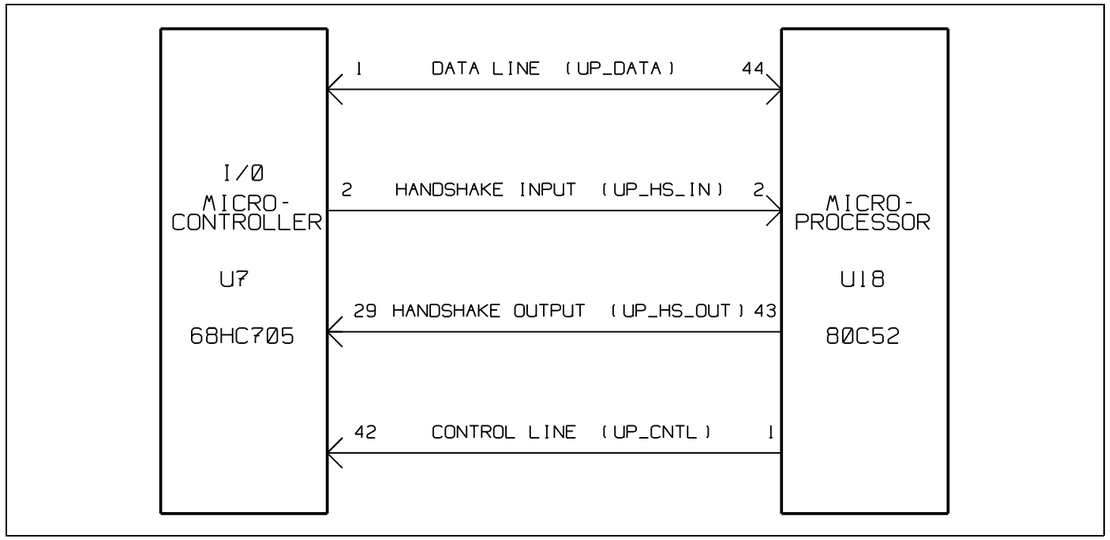

Figure 2 - Inter-Processor Communication

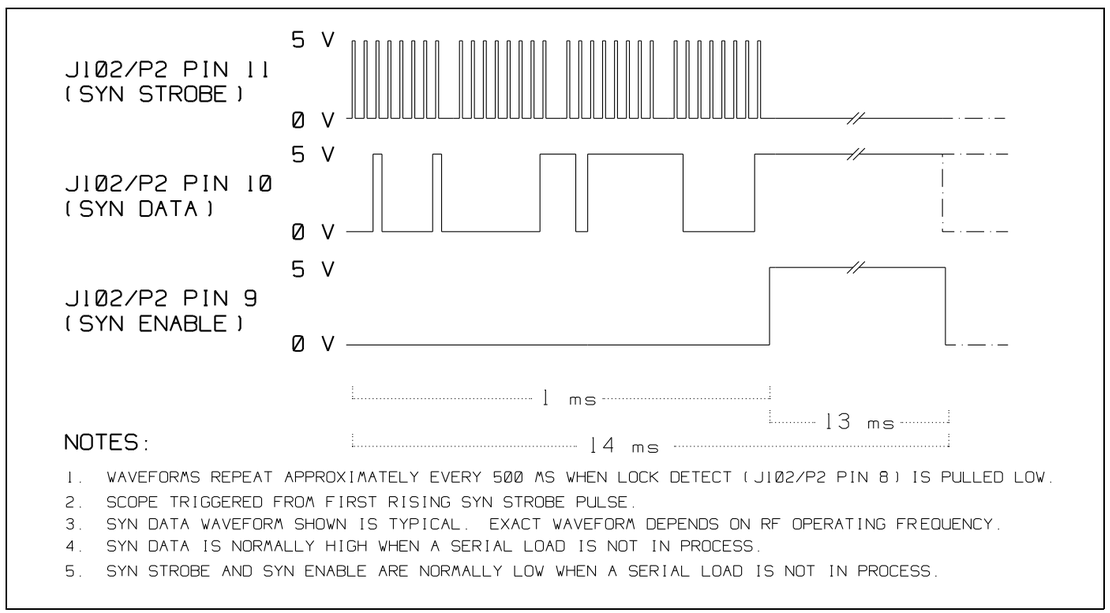

Figure 3 - Synthesizer Load Pulses

1. Attempt to reprogram the unit with the external PC Interface power adapter; if successful, suspect transistors Q3A, Q11, or the SW1 output from U8 pin 34. U8 pin 34 should be ≈ 2.4 Vdc in programming mode and less than 0.1 Vdc otherwise.

2. Less than 0.6 Vdc should be on U8 pin 58 with the PC Interface connected to enable programming mode. If incorrect suspect R31, R58 or the UDC Flex. Most of the A/D conversion circuitry is operational if the volume control and low battery detector is functional.

3. Check TX and RX DATA to and from the radio and PC Programmer.

Check TX DATA

To check the TX DATA input, connect the PC Interface and computer and proceed as follows:

1. Check for logic 0 at J1/P1 pin 5 (UDC_TX_DATA). Pulses should be seen here when a radio read is attempted. Suspect the UDC Flex if pulses are not present and the pin is high all the time.

2. Check for logic 1 at U9D pin 8 (inverted UDC_TX_DATA). Pulses should be seen when a radio read is attempted. Suspect U9D, R3, R113, or D12 if they are not. If pulses are present on U9, suspect U18 or the A/D converter circuits of U8; the Control Board may not be recognizing program mode.

Check RX DATA

Attempt to read the radio repeatedly and check for a short serial data burst at the following points:

- U18 pin 7 (signal origin)
- Inverter U9C pin 6 (UDC_RX_DATA)
- J1/P1 pin 7 (RX DATA).

Check UDC Flex continuity from J1/P1 pin 7 to UDC J101 pin 7. The short data burst should be present at the UDC pin.

Transmit Audio Problems

No Internal Mic Audio
(External Mic Audio Good)

With no external option connected to the UDC, U8 pin 58 should be 5.4 Vdc. The I/O Microcontroller should enable the internal mic circuit via the Audio Processor's SW5 output.

1. Check MIC HI (J1/P1 pin 14) for an internal mic dc bias of ≈ 2.2 Vdc. If this voltage is near 2.7 Vdc, suspect an open UDC Flex or MK1.

2. Average speech into the front cover should produce 10 - 30 mV rms on MIC HI.

3. Amplifier U6A should provide a signal level 7 to 10 times greater than MIC HI. This amplifier's output is applied the internal/external mic audio switch U1B at pin 1.

4. Switch U1B pin 10 should be greater than 4.5 Vdc to select the internal microphone audio. Verify the amplified mic audio is present on switch U1B pin 15 and switch U1C pin 12.

No External Mic Audio
(Internal Mic Audio Good)

1. Verify the I/O Microcontroller is recognizing the externally connected option. The voltage on U8 pin 58 should be approximately 2.5 Vdc with the external mic connected. This voltage is developed from voltage divider R31, R58 and the resistor in the external option.

2. Check for ≈ 2.7 Vdc microphone bias at UDC pin 12 and J1/P1 pin 12 (≈ 2.2 Vdc with the external microphone attached). If this bias is incorrect, suspect resistor R89.

3. If the internal microphone is operating normally, suspect the UDC Flex or amplifier U6B. Connect an external microphone and check the audio level at J1/P1 pin 12. Average speech in the microphone should produce 10 - 30 mV rms here. Signal on U6B pin 7 should be 7 to 10 times greater than EXT MIC HI.

Complete Mic Audio Failure
(All Modes)

If the radio has complete microphone audio failure in all modes of operation, check J102/P2 pin 1 for a modulating signal to the RF Board in the Rear Cover Assembly. If good modulation is present, troubleshoot the RF Board's modulation circuitry. If no or incorrect modulation is on J102/P2 pin 1, suspect the Audio Processor, or filter U10A.

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Complete Mic Audio Failure (Clear Mode Only)

1. Apply an ac coupled 10 mV rms, 1 kHz tone to EXT MIC HI. Use the TQ-0609 Test Box. Select switch position 6 (external mic) on the Test Box and turn the radio off and back on so it will recognize the external option. Place the radio in clear mode and key it from the switch on the Test Box. Typical signal levels are shown in Table 6.

2. Verify the amplified mic audio is present on U1C pin 12 and 14. If mic audio is present on pin 12 and not on pin 14, the radio may be in Aegis digital or private transmit mode. U1C pin 11 should be less than 0.5 Vdc in clear transmit mode and greater than 4.5 Vdc in digital and private transmit mode.

3. Check the output on U5C pin 8. This signal should also be on U8 pin 14.

4. With the radio keyed, check the audio level on U8 pin 18 and 19. The audio level on pin 19 should be 1/3 the audio level on pin 18. If no audio is present on pin 18, suspect U8. If the audio level is incorrect on pin 19, suspect C16, R72 or R126.

5. Check for signal on U8 pin 26. If absent, suspect U8.

6. Check the output on U10A pin 1 and J102/P2 pin 1.

Complete Mic Audio Failure (Aegis Digital And Private Modes)

1. Verify the radio unit under test and the receiving unit have identical outside addresses programmed and the correct data polarity. If the problem is only in private mode, verify the correct cryptographic keys are loaded and the group/channel-to-key selection is correct.

2. Verify the radio is operating in Aegis digital or private mode by monitoring J102/P2 pin 1. Transmit data should be present when the radio is keyed. If transmit data is not present, troubleshoot the modem circuitry.

3. The microphone audio should be present at the output of buffer amplifier U10B. Monitor U10B pin 7 and J5/P5 pin 4.

4. Suspect a problem in the Aegis Module if there is microphone audio on J5/P5 pin 4.

Transmit Channel Guard Or Trunked Low-Speed Data Problems

1. Channel the radio to a conventional channel that has tone Channel Guard encode programmed.

2. Monitor CG_IN at U8 pin 5. There should be a 400 mVp-p staircase wave here when the radio is keyed. This signal is generated from the two walsh bit outputs from U18 (pins 41 and 42) and resistors R131 and R132. CG_IN is dc biased to 2.5 Vdc by R37 and R38. U18 pins 41 and 42 should both be toggling high and low.

3. If U18 pin 42 is not toggling, verify U8 pin 36 is low. This low keeps Q1 off. If incorrect, suspect a shorted Q1 or a defective output from U18.

4. Check U8 pins 6 and 20. There should be a 400 mVp-p sine wave here. The filtered output (pin 6) is connected directly to the input (pin 20). This input is then summed with the microphone audio within the Audio Processor. The external components are not used in encode mode.

5. Channel the radio to a conventional channel that has Digital Channel Guard encode programmed.

6. Monitor U18 pins 41 and 42. Only pin 41 should be toggling for DCG or trunked low-speed data transmissions.

Receive Audio Problems

No Clear Receive Audio

1. Verify audio from the RF Board is present at J101/P1 pin 4. Typical signal level is 100 - 150 mV rms (≈ 350 mVp-p) for 1 kHz tone, 3 kHz deviation. Noise only levels will typically be 1300 mVp-p.

2. There should be a dc voltage on U8 pin 4 between 2.7 Vdc and 5.0 Vdc. This dc voltage will be proportional to receiver noise.

3. Check the squelch opening Tracking Data parameters using the PC Programmer. Higher numbers should make squelch open at lower signal levels, and lower numbers should make squelch open at higher signal levels. Typical squelch opening Tracking Data values are 90 to C0 hex. Values below 78 should always squelch the radio and values above E0 should always unsquelch the radio. If the radio does not operate as described, suspect C12, C25, R82 or the Audio Processor.

4. Table 7 lists tests locations with no RF signal applied and with a strong RF signal applied.

5. Typical audio levels with the volume control fully clockwise and 350 mVp-p, 1 kHz tone from the discriminator are shown in Table 8.

Table 6 - Clear Mode Transmit Audio Signal Levels
(With A 10 mV rms, 1 kHz EXT MIC HI Input)

TEST LOCATION	LEVEL (mVp-p)	COMMENT
U6 pin 7	210	External Mic Amp Output
U1 pin 15	210	Int./Ext. Mic Audio Switch (Common)
U10 pin 7 (J5 pin 4)	210	Bandpass Filter Output To Aegis Module (CODEC_IN)
U8 pin 14	230	Audio Processor Clear Mic Audio Input
U8 pin 18	230	Audio Processor Coupling Output
U8 pin 26	1800 *	Audio Processor TX Audio Output
U10 pin 1 (P2 pin 1)	1200 *	TX Audio To RF Board (RF_TX_AUD)

* Signal levels with no Channel Guard modulation and modulation Tracking Data value set to 10 Hex.

Table 7 - Approximate Noise And Signal Levels

TEST LOCATION	NO RF SIGNAL (noise levels)	STRONG RF SIGNAL (no modulation)
J101/P1 pin 4	1300 mVp-p	0 Vp-p
U5 pin 7	4000 mVp-p	0 Vp-p
U8 pin 3	1200 mVp-p	0 Vp-p
U8 pin 56	3.6 Vdc	2.7 Vdc
U8 pin 55	4.0 Vdc	2.7 Vdc

Receive Channel Guard Or Trunked Low-Speed Data Problems

Filtering and limiting of Channel Guard and trunked low-speed data occurs in Audio Processor U8. A Channel Guard signal is decoded by I/O Microcontroller U7. Microprocessor U18 decodes trunked low-speed data that the radio receives.

1. Channel the radio to a conventional test channel that has CG decode programmed. Apply an on frequency RF signal from a signal generator.

2. Modulate the signal generator with a CG tone. Set CG deviation to 0.750 kHz.

3. Monitor U8 pin 6. The CG tone should be present at a level of 300 mVp-p. The pin is biased to 2.5 Vdc. If the signal or the dc bias is incorrect, suspect the Audio Processor U8.

4. Check U8 pins 7 and 9 for a dc level of 2.7 Vdc.

5. Monitor U8 pin 11 for a 0-to-5 Volt square-wave at the CG frequency. This is the output of the CG demodulator

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Table 8 - Typical Receive Audio Levels At Full Volume

TEST LOCATION	LEVEL (mVp-p)	COMMENT
J101/P1 pin 4	350	RX Discriminator Output (RX_DISC)
U5 pin 7	1200	U5B Buffer Amplifier Output
U8 pin 18	1130	Audio Processor Output
U8 pin 19	370	Audio Processor Input
U8 pin 27	1850	Audio Processor RX Output
U5 pin 14	940	Audio Preamp Output
U21 pin 7	130	Speaker Audio Amp Input
U21 pin 1	5000	Speaker Audio Amp Output (Differential)
U21 pin 3	5000	Speaker Audio Amp Output (Differential)

circuit in the Audio Processor. This signal is applied to I/O Microcontroller U7 pin 34 for decoding via CG_LIM.

6. When the radio is receiving low-speed data, transistor Q1 inverts the signal on U8 pin 11 and applies the inverted signal to Microprocessor U18 pin 42 via CG_LIM_X. U18 then decodes the low-speed data.

No Aegis Digital Or Private Mode Receive Audio

1. Verify the radio under test and the transmitting unit are programmed with identical outside addresses and the correct data polarity. If the problem is only in private mode, verify the correct cryptographic keys are loaded and the group/channel-to-key selection is correct.

2. Transmit a clear signal to the radio under test and verify the transmission is received, the receiver unsquelches and it is heard in the speaker. If not, troubleshoot the clear mode failure before attempting to troubleshoot an Aegis digital or a private mode failure - there may be a common cause.

3. If the radio does not recognize an Aegis digital or a private signal (observe the "BSY" and "PVT" status flags), suspect modem U19 or the associated circuitry. If the radio is equipped with an encrypt/decrypt option, the "PVT" status flag should flash when it receives a valid private signal. If the "PVT" status flag flashes but no audio is heard in the speaker, the cryptographic key, outside address, etc. may be incorrect or there may be an audio problem in the radio.

4. If the radio appears to receive a transmission ("BSY" status flag turns on and "PVT" status flag flashes if an encrypted signal) but no audio is heard in the speaker, suspect a problem in the Control Board's audio circuitry or a problem with CODEC U7 on the Aegis Module. Audio should be present on J5/P5 pin 3 (VG_RX) at a level of 500 - 1000 mVp-p with average speech into the transmitting radio. If no audio is present on this pin, the CODEC on the Aegis Module may be at fault. If audio is present, troubleshoot the digital/private mode receive audio path circuitry on the Control Board.

5. Check U8 pin 13 for a similar signal with a 2.7 Vdc bias. If incorrect suspect C106 or R102.

6. With average speech into the radio transmitting the Aegis digital or private signal, clear audio should be present on U8 pin 27 at a level of 800 - 1500 mVp-p with the volume control set to maximum. Suspect U8 if incorrect.

7. With the exception of the de-emphasis characteristics of U5D, the audio path from U8 pin 27 to the speaker is identical to the clear mode audio. The de-emphasis response of U5D is controlled by the VGCONV line from the I/O Microcontroller and switch U1A. If the radio is unusually low-pitched sounding when in Aegis digital or private modes, check U1A pin 9. It should be high when the radio is decoding an Aegis digital signal or decrypting a private transmission. This switches C11 and R68 into the feedback path of the amplifier circuit and switches C1 out of the circuit.

Volume Control Problems

The volume control operates by digitizing the dc voltage from the volume potentiometer wiper and varying the digital attenuator in the Audio Processor.

1. Check the dc voltage at J4/P4 pin 9. It should be near 0 Vdc with the volume control fully counterclockwise and near 5.5 Vdc with the control fully clockwise. If not, check the volume control and Keypad Flex.

2. The volume control wiper voltage should also be present at U8 pin 59. If not, suspect J4/P4 or R60.

3. If there is a problem with volume control and wiper voltage is present at U8 pin 59, suspect U8.

Speaker Amplifier Problems

1. Check the Battery Plate speaker contacts.

2. If the speaker is inoperative and audio is present on UDC pin 3 (or U8 pin 27 and U5D pin 14, see Table 8), check U21 pin 2 for battery power from Q13. Audio should be on U21 pin 7.

3. Check U21's differential outputs on pins 1 and 3. Replace U21 if power and audio inputs are good and the differential outputs are not.

The internal speaker can be quickly tested by applying audio from a signal generator to the appropriate pins on the Battery Plate with the battery removed. With the Front Cover face-down on the bench, apply audio from a signal generator to the second and third pins from the left. The speaker impedance is 24 ohms and it is a 1/2 Watt device.

Digital/Private Mode And Trunked Mode Problems

The modem circuitry is the data link for 9600 baud digital communications. Failure of all digital communications indicates a problem with the modem or its related circuitry. This section will help isolate a problem to the modem circuitry or other circuity related to the particular mode of operation.

NOTE

If servicing a non-trunked radio, disregard the trunked mode troubleshooting information.

1. Verify programming.

2. Test the radio to verify it will correctly transmit and receive clear voice trunked mode calls. If there is a problem, troubleshoot the modem circuitry. See **Modem Receive Data Check** and **Modem Transmit Data Check**.

3. If the radio can initiate clear voice trunked mode transmissions but they are dropped by the system, suspect a problem with the transmit low-speed data encoding circuitry. See **Transmit Channel Guard Or Trunked Low-Speed Data Problems** in the **Transmit Audio Problems** section. Low-speed data is not used when the radio is operating in Aegis digital or private modes.

4. If the radio initially receives clear voice trunked mode transmissions but reception is quickly lost, suspect a problem in the trunked low-speed data decoding circuity. See **Receive Channel Guard Or Trunked Low-Speed Data Problems** in the **Receive Audio Problems**. Low-speed data is not used when the radio is operating in Aegis digital or private modes.

5. If the radio operates normally in trunked clear voice mode but not in Aegis digital or private mode, the problem may be with the Aegis Module or in the circuitry on the Control Board that interfaces both together. Also suspect Audio Processor U8; the clear mode audio path through U8 differs from the Aegis digital and private mode audio path.

Modem Receive Data Check

1. Monitor U19 pin 19 (RX_DATA) for demodulated data when the radio is receiving a 9600 baud data transmission. Signal level should be approximately 5.0 Vp-p. If no pulses are present, suspect U12C or integrating capacitor C3.

2. U19 should interrupt U18 when it receives valid data. Check U19 pin 24 for low going pulses when the radio is receiving data transmissions. Suspect U19 if the data pulses are present and U19 does not interrupt U18.

3. If U18 is being interrupted by U19 when a valid data transmission is received and the radio does not recognize the transmission, suspect U18 or the radio's personality programming.

Modem Transmit Data Check

1. Monitor modem U19 pin 21 (RF_TX_DAT) for 9600 baud pulses when a trunk call, Aegis digital or private call is attempted. Signal level should be > 3 Vp-p with rise and fall times < 100 microseconds. If no pulses are present there is a communication problem between U18 and U19, or U19 is defective.

2. Filter U10C and associated RC networks filter or "round" the RF_TX_DAT digital pulses to a signal which can be passed to the FM transmitter. Check U10C pin 8 for a 9600 baud "rounded" signal at 12 mVp-p. Suspect C9, C85, C107, C108 or U10C if this signal is incorrect.

3. Verify the 9600 baud signal is on U8 pin 26 at a level of 2.0 Vp-p. Suspect U8 if the signal level is incorrect.

4. Check U10A pin 1 (RF_TX_AUD) for the 9600 baud signal to the RF Board. Signal into the RF Board should be 800 mVp-p.

CONTROL BOARD
19D903081G1
ISSUE 2

SYMBOL	PART NUMBER	DESCRIPTION
		——— CAPACITORS ———
C1	19A149896P15	Ceramic: 3300 pF ±5%, 50 VDCW.
C2	19A702052P130	Ceramic: 0.022 µF ±5%, 50 VDCW.
C3 and C4	19A702052P33	Ceramic: 0.1 µF ±10%, 50 VDCW.
C5	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C6	19A705205P5	Tantalum: 6.8 µF, 10 VDCW; sim to Sprague 293D.
C7	19A149897P39	Ceramic: 100 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C8 and C9	19A702061P99	Ceramic: 1000 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C10	19A702052P130	Ceramic: 0.022 µF ±5%, 50 VDCW.
C11	19A702052P6	Ceramic: 1500 pF ±10%, 50 VDCW.
C12	19A705205P12	Tantalum: .33 µF, 16 VDCW; sim to Sprague 293D.
C13 thru C18	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C21 thru C24	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C25 and C26	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C27	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C28 and C29	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C30	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C31	19A702052P33	Ceramic: 0.1 µF 10%, 50 VDCW.
C32	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C33	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C34 and C35	19A702052P33	Ceramic: 0.1 µF ±10%, 50 VDCW.
C36 and C37	19A702052P22	Ceramic: 0.047 µF ±10%, 50 VDCW.
C38 and C39	19A702052P33	Ceramic: 0.1 µF ±10%, 50 VDCW.
C40	19A705205P6	Tantalum: 10 µF, 16 VDCW; sim to Sprague 293D.
C41	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C42 and C43	19A705205P6	Tantalum: 10 µF, 16 VDCW; sim to Sprague 293D.
C44	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C45 thru C69	19A149897P55	Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C70 and C71	19A702052P33	Ceramic: 0.1 µF ±10%, 50 VDCW.
C72 thru C86	19A149897P55	Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C87	19A149897P15	Ceramic: 10 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C88	19A149896P11	Ceramic: 1500 pF ±5%, 50 VDCW.
C89 and C90	19A149897P23	Ceramic: 22 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C91	19A149897P11	Ceramic: 4.7 pF ±0.25 pF, 50 VDCW, temp coef 0 ±60 PPM/°C.
C92	19A149896P15	Ceramic: 3300 pF ±5%, 50 VDCW.
C95	19A702052P33	Ceramic: 0.1 µF ±10%, 50 VDCW.
C96	19A705205P13	Tantalum: 4.7 µF, 10 VDCW; sim to Sprague 293D.
C97	19A705205P19	Tantalum: 2.2 µF ±20%, 10 VDCW.
C99 and C100	19A149897P25	Ceramic: 27 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C102	19A702061P45	Ceramic: 47 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C103	19A702052P33	Ceramic: 0.1 µF ±10%, 50 VDCW.
C104	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C105	19A149897P55	Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C106	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C111 and C112	19A149897P43	Ceramic: 150 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C113	19A702061P99	Ceramic: 1000 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C114	19A705205P6	Tantalum: 10 µF, 16 VDCW; sim to Sprague 293D.
C115	19A702052P33	Ceramic: 0.1 µF ±10%, 50 VDCW.
C116 and C117	19A702061P45	Ceramic: 47 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C118	19A702052P33	Ceramic: 0.1 µF ±10%, 50 VDCW.
C119	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C120	19A149897P43	Ceramic: 150 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
		——— DIODES ———
D1 thru D3	19A149946P1	Silicon: sim to R OHM DA204K.
D4 and D5	19A702525P2	Silicon: PIN; sim to MMBV3401.
D6	19A149946P1	Silicon: sim to R OHM DA204K.
D7	19A149615P1	Silicon: Diode Bridge; sim to BGX50A.
D11 thru D14	19A705377P4	Silicon: Hot Carrier; sim to HSMS-2802.
		——— JACKS ———
J1		Part of Printed Wire Board.
J3	19A702517P5	Contact: Horizontal Mount, Gold Plated; sim to Berg 75121-001. (Quantity of 3 required.)
J4		Part of Printed Wire Board.
J5	19B801451P10	Socket Strip: 10 Contacts, Gold Plated.
J6	19B801451P6	Socket Strip: 13 Contacts, Gold Plated.
J7	19B801451P2	Socket Strip: 5 Contacts, Gold Plated.
		——— INDUCTORS ———
L1	19A705470P25	Coil: 1 µH ±20%, sim to 38LB-IR0M.o 38OLB-I.
		——— PLUGS ———
P1	19A704852P202	Connector: 5-Pin, Gold Plated; sim to Dupont Berg 65646-105.
P2	19A704852P203	Connector: 11-Pin, Gold Plated; sim to Dupont Berg 65646-111.
		——— TRANSISTORS———
Q1	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q2 thru Q4	19A705945P1	Silicon, Dual NPN: sim to R OHM IMH4.
Q5	19A700059P2	Silicon, PNP: sim to MMBT3906, low profile.

* COMPONENTS, ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

SYMBOL	PART NUMBER	DESCRIPTION
Q6	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q7	19A700059P2	Silicon, PNP: sim to MMBT3906, low profile.
Q9 thru Q11	19A134577P2	Silicon, PNP: sim to BCX51-16.
Q12	19A705944P1	Silicon, Dual PNP; sim to ROHM IMT1.
Q13	19A134577P2	Silicon, PNP: sim to BCX51-16.
Q14	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
		——— RESISTORS ———
R1	19A149818P470	Metal film: 47 ohms ±5%, 1/16 w.
R2	19A149818P391	Metal film: 390 ohms ±5%, 1/16 w.
R3 and R4	19A149818P221	Metal film: 220 ohms ±5%, 1/16 w.
R5 and R6	19B801251P105	Metal film: 1M ohms ±5%, 1/10 w.
R7 and R8	19B801251P4R7	Metal film: 4.7 ohms ±5%, 1/10 w.
R9	19B801251P1	Jumper.
R10 and R11	344A3304P1003	Metal film: 100K ohms ±1%, 1/10 w.
R12	19B801251P106	Metal film: 10M ohms ±10%, 1/10 w.
R13	344A3304P2373	Metal film: 237K ohms ±1%, 1/10 w.
R14	19A149818P473	Metal film: 47K ohms ±5%, 1/16 w.
R15	19B801251P475	Metal film: 4.7M ohms ±10%, 1/10 w.
R16	19A149818P471	Metal film: 470 ohms ±5%, 1/16 w.
R17 and R18	344A3304P3012	Metal film: 30.1K ohms ±1%, 1/10 w.
R19	344A3304P2672	Metal film: 26.7K ohms ±1%, 1/10 w.
R20	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R21	19B801251P221	Metal film: 220 ohms ±5%, 1/10 w.
R22	19A149818P102	Metal film: 1K ohms ±5%, 1/16 w.
R23	19B801251P331	Metal film: 330 ohms ±5%, 1/10 w.
R24	19A149818P102	Metal film: 1K ohms ±5%, 1/16 w.
R25	19A149818P222	Metal film: 2.2K ohms ±5%, 1/16 w.
R26 thru R28	19B801251P2R2	Metal film: 2.2 ohms ±5%, 1/10 w.
R29 and R30	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R31	344A3304P1002	Metal film: 10K ohms ±1%, 1/10 w.
R32 thru R36	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R37 and R38	344A3304P1002	Metal film: 10K ohms ±1%, 1/10 w.
R39 and R40	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R41	19A149818P102	Metal film: 1K ohms ±5%, 1/16 w.
R42	19A149818P471	Metal film: 470 ohms ±5%, 1/16 w.
R43 and R44	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R45	344A3304P1002	Metal film: 10K ohms ±1%, 1/10 w.
R46 thru R51	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R52 thru R65	19A149818P102	Metal film: 1K ohms ±5%, 1/16 w.
R66	19A149818P105	Metal film: 1M ohms ±5%, 1/16 w.
R67	19A149818P474	Metal film: 470K ohms ±5%, 1/16 w.
R68	19A149818P124	Metal film: 120K ohms ±5%, 1/16 w.
R69	19A149818P274	Metal film: 270K ohms ±5%, 1/16 w.
R70	19A149818P124	Metal film: 120K ohms ±5%, 1/16 w.
R71 thru R75	19A149818P474	Metal film: 470K ohms ±5%, 1/16 w.
R76	19A149818P563	Metal film: 56K ohms ±5%, 1/16 w.
R77	19B801251P106	Metal film: 10M ohms ±10%, 1/10 w.
R78	19A149818P271	Metal film: 270 ohms ±5%, 1/16 w.
R79 thru R83	19A149818P223	Metal film: 22K ohms ±5%, 1/16 w.
R84 thru R86	19A149818P154	Metal film: 150K ohms ±5%, 1/16 w.
R87	19A149818P224	Metal film: 220K ohms ±5%, 1/16 w.
R88	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R89 thru R93	19A149818P222	Metal film: 2.2K ohms ±5%, 1/16 w.
R94 and R95	344A3304P1003	Metal film: 100K ohms ±1%, 1/10 w.
R96 thru R103	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R104 and R105	344A3304P1003	Metal film: 100K ohms ±1%, 1/10 w.
R106	19B801251P822	Metal film: 8.2K ohms ±5%, 1/10 w.
R107	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R108	19B801251P822	Metal film: 8.2K ohms ±5%, 1/10 w.
R109	344A3304P1003	Metal film: 100K ohms ±1%, 1/10 w.
R110 thru R112	19A149818P104	Metal film: 100K ohms ±5%, 1/16 w.
R113	19A149818P223	Metal film: 22K ohms ±5%, 1/16 w.
R114	19B801251P100	Metal film: 10 ohms ±5%, 1/10 w.
R115	19A149818P272	Metal film: 2.2K ohms ±5%, 1/16 w.
R116	19A149818P334	Metal film: 330K ohms ±5%, 1/16 w.
R117 thru R119	19A149818P473	Metal film: 47K ohms ±5%, 1/16 w.
R120	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R121	19B801251P182	Metal film: 1.8K ohms ±5%, 1/10 w.
R122 thru R124	19A149818P473	Metal film: 47K ohms ±5%, 1/16 w.
R125	19A149818P152	Metal film: 1.5K ohms ±5%, 1/16 w.
R126	19A149818P224	Metal film: 220K ohms ±5%, 1/16 w.
R127	19A149818P103	Metal film: 10K ohms ±5%, 1/16 w.
R128	19A149818P105	Metal film: 1M ohms ±5%, 1/16 w.
R129	19A149818P333	Metal film: 33K ohms ±5%, 1/16 w.
R130	344A3304P1212	Metal film: 12.1K ohms ±1%, 1/10 w.
R131	344A3304P1623	Metal film: 162K ohms ±1%, 1/10 w.
R132	344A3304P6812	Metal film: 68.1K ohms ±1%, 1/10 w.
R133 and R134	19B801251P470	Metal film: 47 ohms ±5%, 1/10 w.
R135 and R136	19A149818P102	Metal film: 1K ohms ±5%, 1/16 w.
R137	344A3304P2672	Metal film: 26.7K ohms ±1%, 1/10 w.
R138	19A149818P105	Metal film: 1M ohms ±5%, 1/16 w.
R139	344A3304P4992	Metal film: 49.9K ohms ±1%, 1/10 w.
R140	344A3304P2322	Metal film: 23.2K ohms ±1%, 1/10 w.
R141	344A3304P1872	Metal film: 18.7K ohms ±1%, 1/10 w.
R142	344A3304P6812	Metal film: 68.1K ohms ±1%, 1/10 w.
R143	19A149818P102	Metal film: 1K ohms ±5%, 1/16 w.
R144	19B801251P1	Jumper.
R145	19B801251P282	Metal film: 470K ohms ±5%, 1/16 w.
R146	19A149818P474	Metal film: 470K ohms ±5%, 1/16 w.
		——— SWITCHES ———
SW1	19A705164P1	Switch.
		——— INTEGRATED CIRCUITS ——
U1	19A702705P5	Digital: Triple 2-Channel Analog Multiplexer; sim to 4053BM.
U2	344A3404P101	Linear: +5.0 Volt Regulator; sim to TL751L05.
U3	19A702293P1	Linear: Quad Op Amp; sim to LM324D.
U4	344A3303P202	Linear: +5.5 Volt Regulator; sim to TK11455.
U5	19A705798P2	Linear: Quad JFET Op Amp; sim to TLO64CD.
U6	19A705798P1	Linear: Dual JFET Op Amp; sim to TLO62CD.
U7	349A9567G1	Digital: Microcontroller; sim to MC68HC705C8FB. (Programmed)
U8	19A705851P1	Audio Processor: sim to STC9140FOB.
U9	19A703483P304	Digital: Hex Inveter; sim to 74HC04.
U10	19A705798P5	Linear: Quad JFET Op Amp; sim to TLO64CD.
U11	19A149634P1	Linear: 2.5 Volt Reference; sim to LM385D-2.5.
U12	19A704125P1	Linear: Quad Comparator; sim to LM339D.
U13 and U14	19A703471P303	Digital: Dual 2-Bit Transparent Latch; sim to 74HC75.
U15	19A705963P2	Digital: 64K x 8 EEPROM; sim to N28F512-200.
U16	19A705603P7	Digital: 8K x 8-Bit RAM; sim to TC5565AFL-15L.
U17	344A4600P101	Digital: 8K x 8-Bit EEPROM; sim to X28C64.
U18	19A705557P5	Digital: 8-Bit Microcomputer; sim to F80C52.
U19	19A704727P5	Digital: Modem.
U20	19A703471P320	Digital: 3-Line To 8-Line Decoder; sim to 74HC138.
U21	19A705452P2	Linear: Audio Amplifier; sim to NJM 2073D.
U23	19A703483P302	Digital: Quad 2-Input NAND Gate; sim to 74HC00.
U24	19A703483P301	Digital: Quad 2-Input NOR Gate; sim to 74HC02.
		——— CRYSTALS ———
Y1	19A702511G27	Quartz: 8.00 MHz.
Y2	19A702511G61	Quartz: 2.0 MHz.
Y3	19A702511G26	Quartz: 11.059 MHz.

PRODUCTION CHANGES

This addendum incorporates Revision Letter changes A - F to Control Board 19D903081G1. The following changes have been made:

REV. A CONTROL BOARD 19D903081G1

To improve the decrypted audio quality, changed C11 at U5 pin 13 from 1000 pF (19A702052P5) to 1500 pF (19A702052P6). Also changed crystal Y2 from 19A702511G40 to 19A702511G61.

REV. B CONTROL BOARD 19D903081G1

To incorporate changes necessary for Aegis, changed the following components: At U10.2 (U10B) changed R140 from 18.7K ohms (344A3304P1872) to 23.2K ohms (344A3304P2322), changed R141 from 23.2K ohms (344A3304P2322) to 18.7K ohms (344A3304P1872), deleted 3300 pF capacitor C93 (19A149896P15), deleted 0.022 µF capacitor C94 (19A702052P130), and added jumper R144 (19B801251P1) at C94's previous location. Also added 150 pF capacitor C120 (19A149897P43) in parallel with R126, and added 470 pF capacitor C121 (19A149897P55) between U12 pin 9 and ground.

REV. C CONTROL BOARD 19D903081G1

To improve receiver response time, changed C27 at P1 pin 4 (RX_DISC) from 1 µF (19A705205P2) to 0.1 µF (19A702052P33). The new capacitor is a non-polarized device.

REV. D CONTROL BOARD 19D903081G1

To improve operation with the Keyloader, changed UDC_TX_DATA pull-up resistor R113 at U9 pin 9 from 100K ohms (19A149818P104) to 22K ohms (19A149818P223).

REV. E CONTROL BOARD 19D903081G1

To improve operation of the transmit data filter circuit, changed R25 from 10K ohms (19A149818P103) to 2.2K ohms (19A149818P222) and changed R87 from 150K ohms (19A149818P154) to 220K ohms (19A149818P224). Also deleted R145 (19B801251P103) and added R146 between U10 pin 2 and the VCCA supply line. R146 is a 470K ohm resistor (19A149818P474). Changed U10 from an LM324 device (19A802293P1) to a TLO64CD device (19A705798P5).

REV. F CONTROL BOARD 19D903081G1

To improve operation, changed personality EEPROM U17 from 19A149755P5 to 344A4600P101.

REV. G CONTROL BOARD 19D903081G1

To improve receiver audio output, C27 changed from 19A702052P33 (0.1 µf) to 19A705205P2 (1µF).

REV. H CONTROL BOARD 19D903081G1

To meet ETSA Standards Controller Boards re-aligned. Added was R145 (19B801251P2R2). Changes made are R146 (19A702293P1) to R146 (19A149818P474). R115 (19A149818P222) to R115 (19A149818P272).

REV. J CONTROL BOARD 19D903081G1

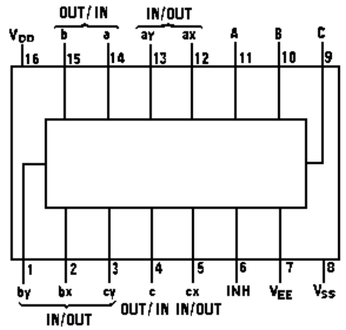
To enable 081 boards to be used in Conventional Radios, the software in OTP processor has been modified. Changed U7 from 19A149861G3 to 349A9567G1.

U1

TRUTH TABLE

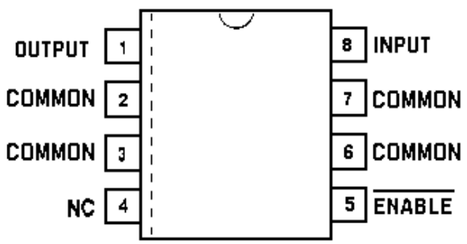
INHIBIT	C	B	A	"ON" CHANNELS
0	0	0	0	cx, bx, ax
0	0	0	1	cx, bx, ay
0	0	1	0	cx, by, ax
0	0	1	1	cx, by, ay
0	1	0	0	cy, bx, ax
0	1	0	1	cy, bx, ay
0	1	1	0	cy, by, ax
0	1	1	1	cy, by, ay
1	X	X	X	none

X = 0 or 1



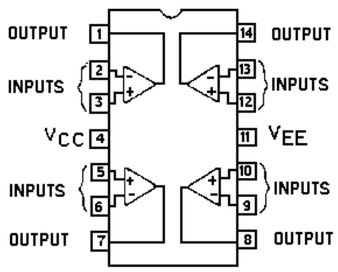
ANALOG MULTIPLEXER
19A702705P5

U2



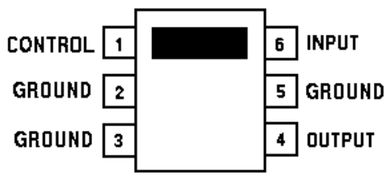
5.0 VOLT REGULATOR
344A3404P101

U3



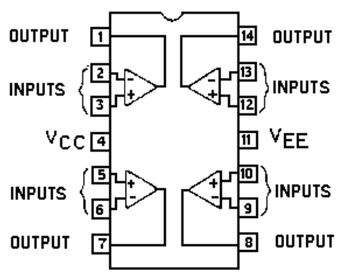
QUAD OP AMP
19A702293P1

U4



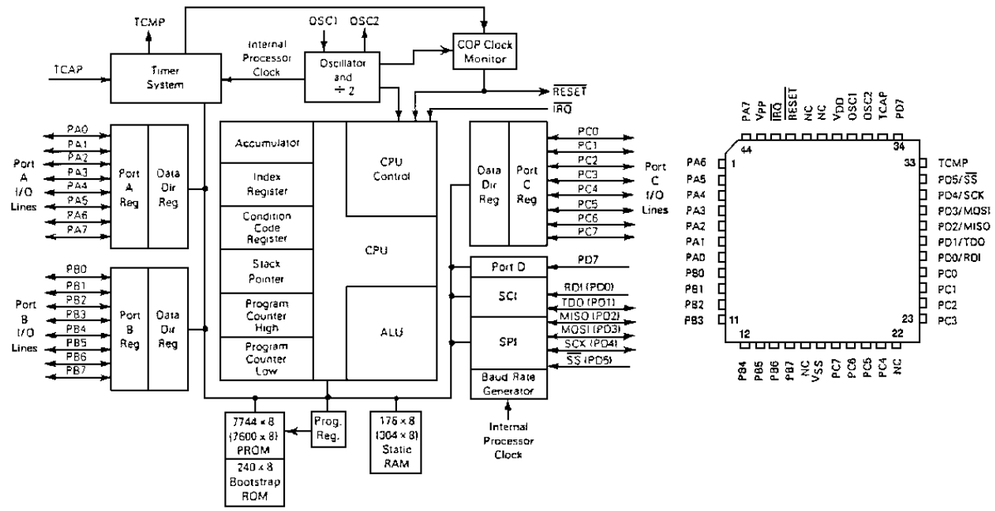
5.5 VOLT REGULATOR
344A3303P202

U5, U10



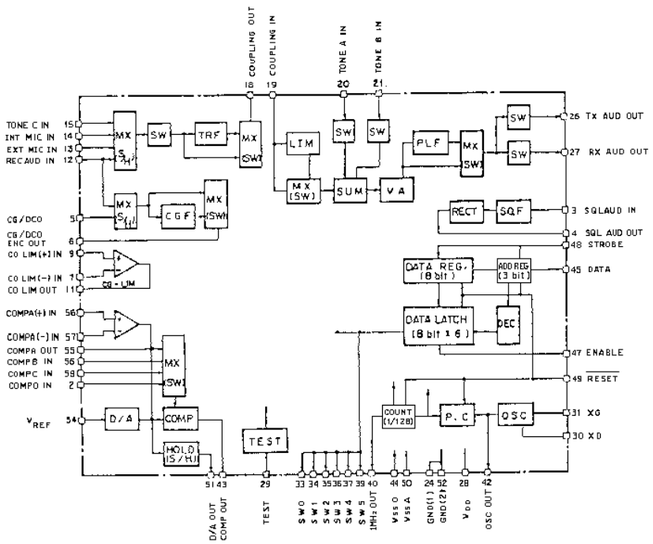
QUAD OP AMP
19A705798P2

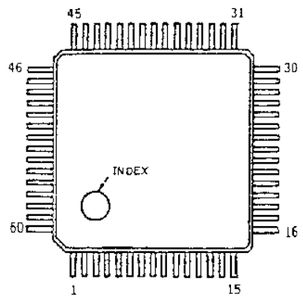
U7



MICROCONTROLLER
349A9567G1

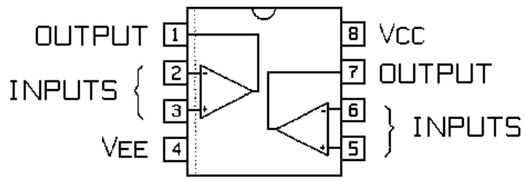
U8





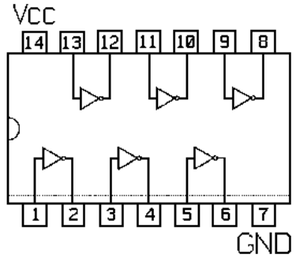
AUDIO PROCESSOR
19A705851P1

U6



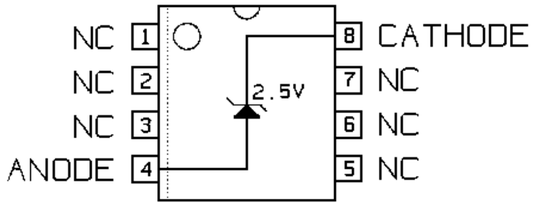
DUAL OP AMP
19A705798P1

U9



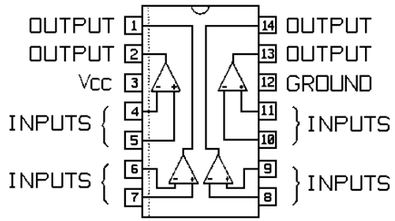
HEX INVERTER
19A703483P304

U11



2.5 VOLT REFERENCE
19A149634P1

U12



NOTE : ALL OUTPUTS ARE OPEN COLLECTOR

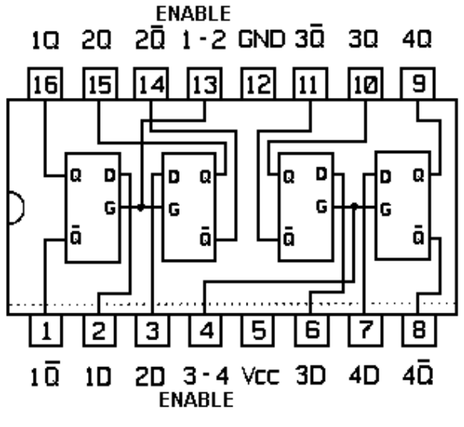
QUAD COMPARATOR
19A704125P1

U13, U14

TRUTH TABLE

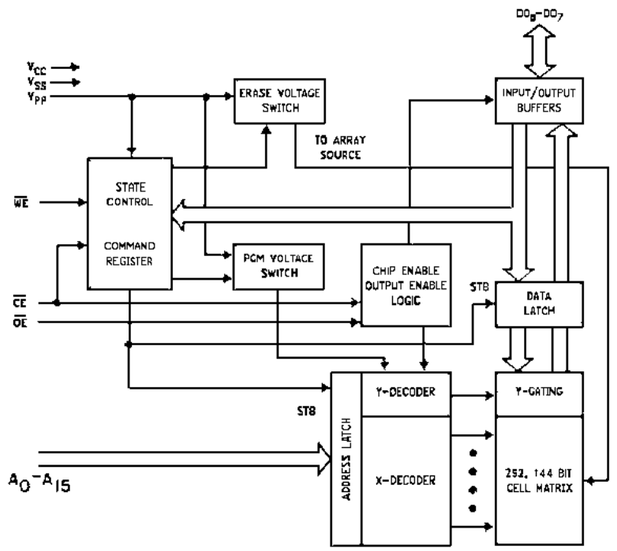
INPUTS		OUTPUTS	
D	G	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	$Q_{\emptyset}$	$\bar{Q}_{\emptyset}$

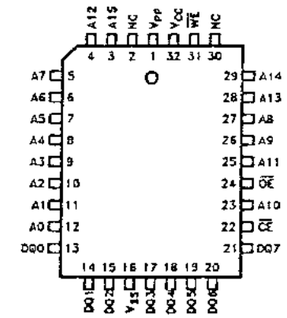
H = HIGH LEVEL
L = LOW LEVEL
X = DON'T CARE
$Q_{\emptyset}$ = THE LEVEL OF Q BEFORE THE TRANSISTION OF G



4-BIT LATCH
19A703471P303

U15





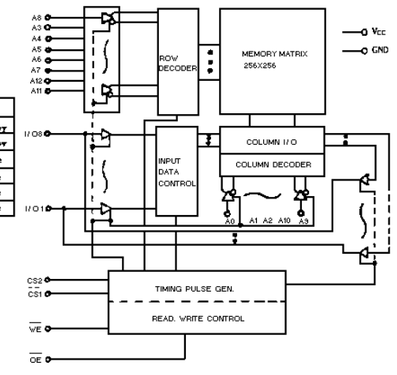
64K x 8-BIT PROM
19A705963P2

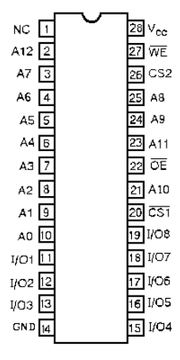
U16

TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O	Icc
X	H	X	X	Not Selected	High z	Standby
X	X	L	X	Not Selected	High z	Standby
H	L	H	H	Output Disabled	High z	Active
H	L	H	L	Read	Dout	Active
L	L	H	H	Write	Din	Active
L	L	H	L	Write	Din	Active

X= H or L

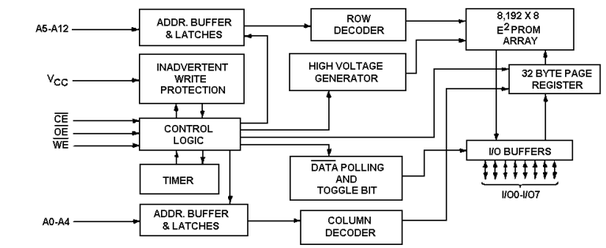




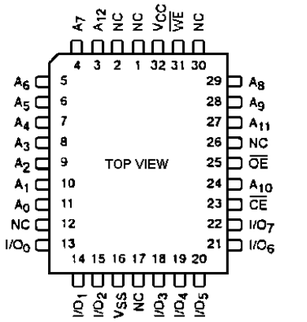
8K x 8-BIT STATIC RAM
19A705603P7

U17

BLOCK DIAGRAM



PLCC Package



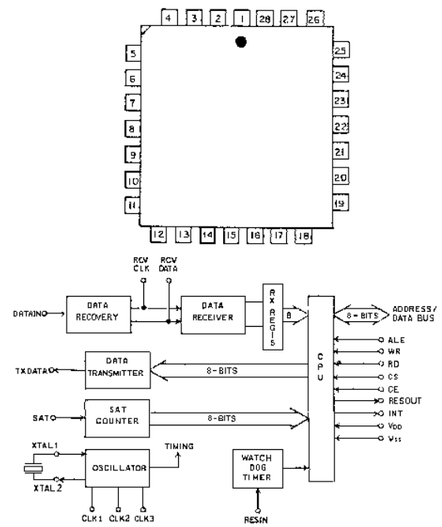
PIN FUNCTIONS

Pin Name	Function
A0-A12	Address Inputs
I/O0-I/O7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	5V Supply
Vss	Ground
NC	No Connect

8K x 8-BIT EEPROM
344A4600P101

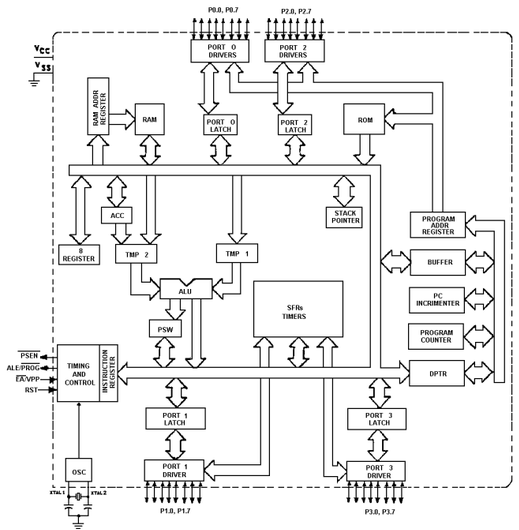
U19

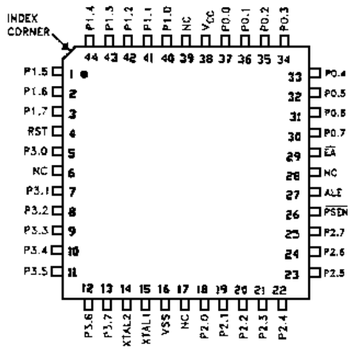
PIN	NAME	FUNCTION
1	RD	READ ENABLE (ACTIVE LOW)
2	CE	CHIP ENABLE (ACTIVE LOW)
3	RESOUT	RESET OUTPUT (ACTIVE HIGH)
4	AD0	BI-DIRECTIONAL A/D BUS
5	AD1	BI-DIRECTIONAL A/D BUS
6	AD2	BI-DIRECTIONAL A/D BUS
7	AD3	BI-DIRECTIONAL A/D BUS
8	AD4	BI-DIRECTIONAL A/D BUS
9	AD5	BI-DIRECTIONAL A/D BUS
10	AD6	BI-DIRECTIONAL A/D BUS
11	AD7	BI-DIRECTIONAL A/D BUS
12	ALE	ADDRESS LATCH ENABLE (ACTIVE HIGH)
13	V_{SS}	GROUND
14	CLK1	BUFFERED OSCILLATOR OUTPUT
15	V_{DD}	+5 VOLT SUPPLY
16	XTAL1	OSCILLATOR INPUT
17	XTAL2	OSCILLATOR OUTPUT
18	CLK2	CLOCK OUTPUT
19	RXDATA	RECEIVED DATA INPUT
20	SAT	RECEIVED SAT INPUT
21	TXDATA	TRANSMIT DATA OUTPUT
22	RCVCLK	RECOVERED CLOCK OUTPUT
23	RCVDAT	RECOVERED DATA OUTPUT
24	INT	INTERRUPT REQUEST (ACTIVE LOW)
25	RESIN	RESET INPUT (ACTIVE HIGH)
26	CS	CHIP SELECT (ACTIVE LOW)
27	CLK3	TRANSMIT CLOCK OUTPUT
28	WR	WRITE ENABLE (ACTIVE LOW)



MODEM
19A704727P5

U18



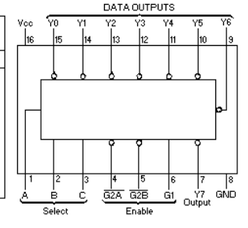


8-BIT MICROCOMPUTER
19A705557P5

U20

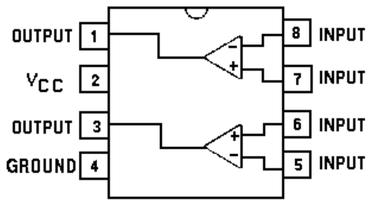
Inputs				Outputs							
Enable		Select									
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* $\overline{G2}$=G2A+G2B
H=high level, L=low level, X=don't care



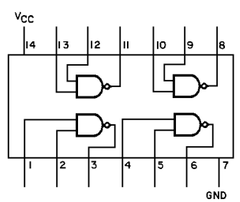
3-TO-8 LINE DECODER
19A703471P320

U21



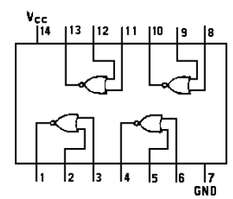
AUDIO AMPLIFIER
19A705452P2

U23

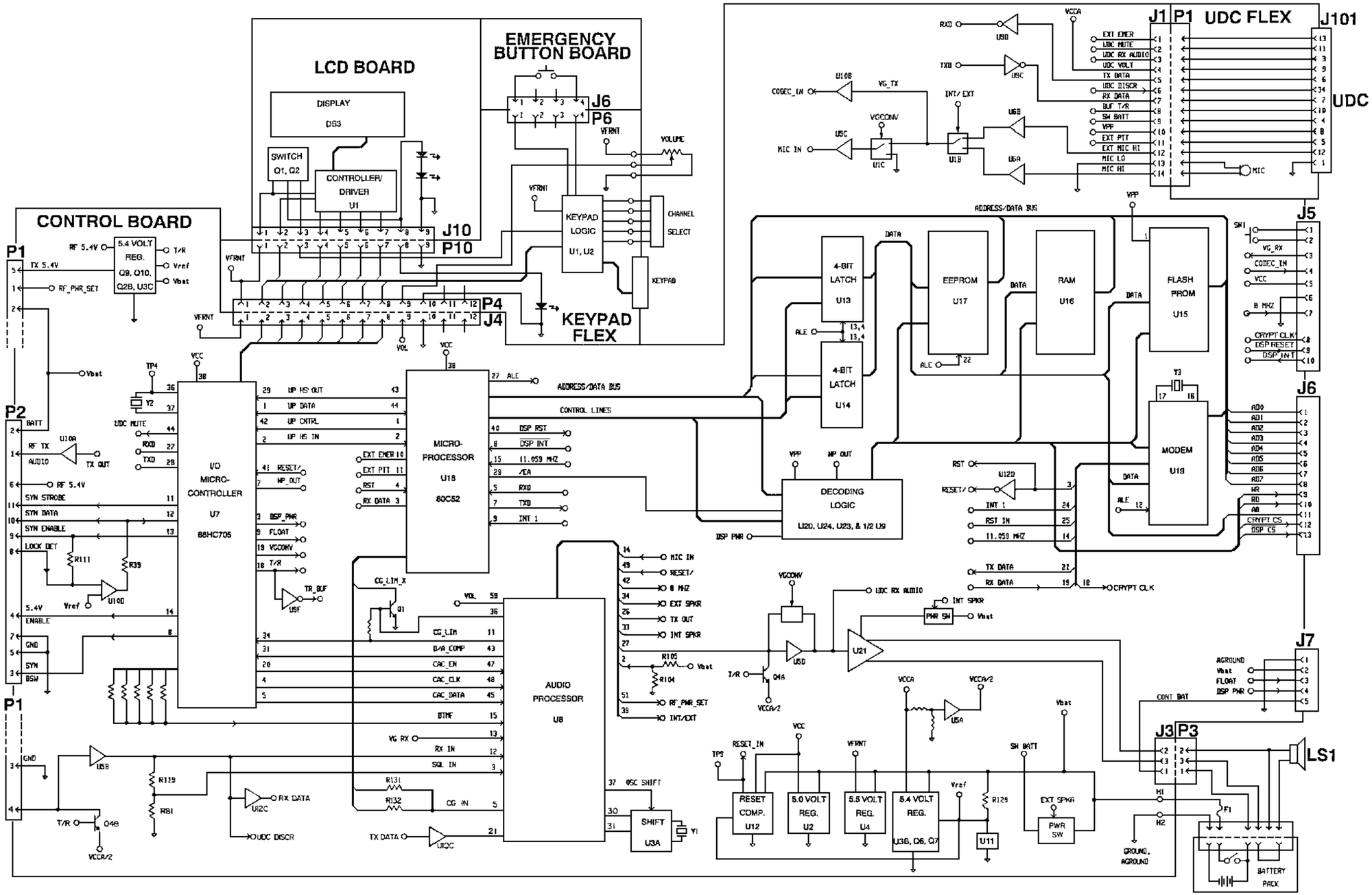


QUAD 2-INPUT NAND GATE
19A703483P302

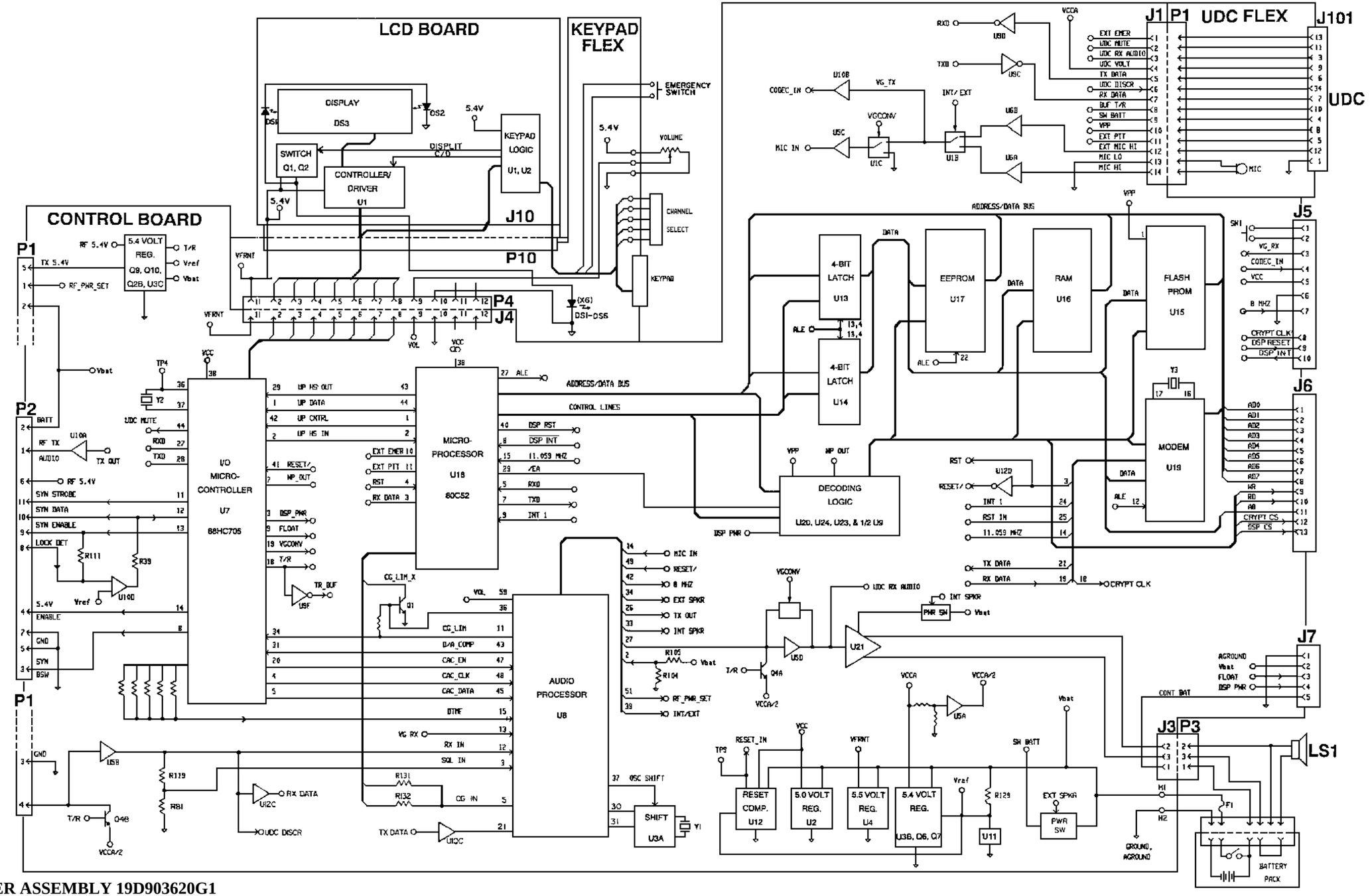
U24



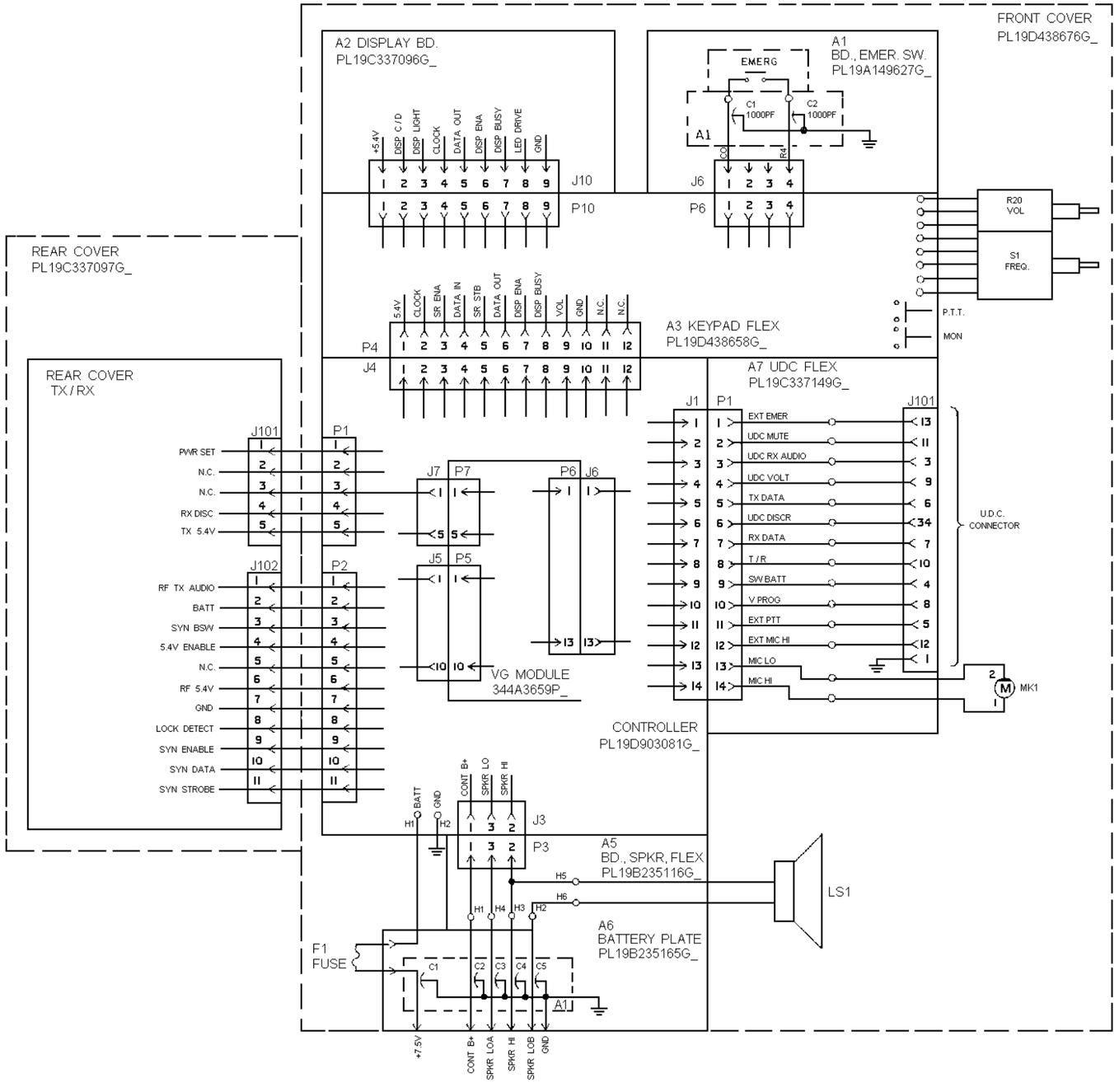
QUAD 2-INPUT NOR GATE
19A703483P301

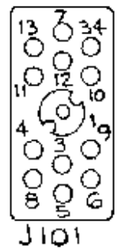


FRONT COVER ASSEMBLY 19D438676G5
AND CONTROL BOARD 19D903081G1

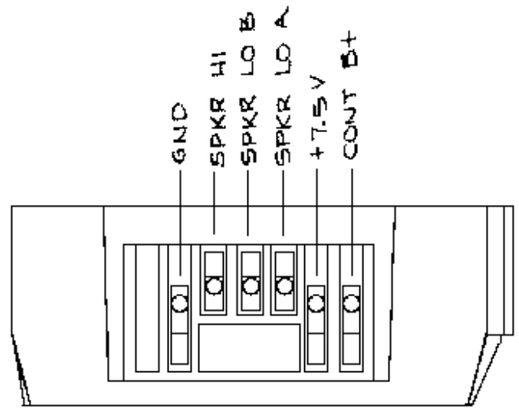


FRONT COVER ASSEMBLY 19D903620G1
AND CONTROL BOARD 19D903081G1





UDC CONTACT IDENTIFICATION
VIEWED FROM OUTSIDE OF CASE



BATTERY CONTACT IDENTIFICATION
VIEWED FROM OUTSIDE OF CASE

COMPLETE RADIO INTERCONNECTION
(19D902383, Sh. 2, Rev. 1)

J5 pin 5 = 5.0 Vdc Regulated Supply From U2 (VCC)

J5 pin 7 = 8 MHz Clock Output From Audio Processor U8 (8MHZ)

TP4 = 2.0 MHz Clock From I/O Microcontroller U7

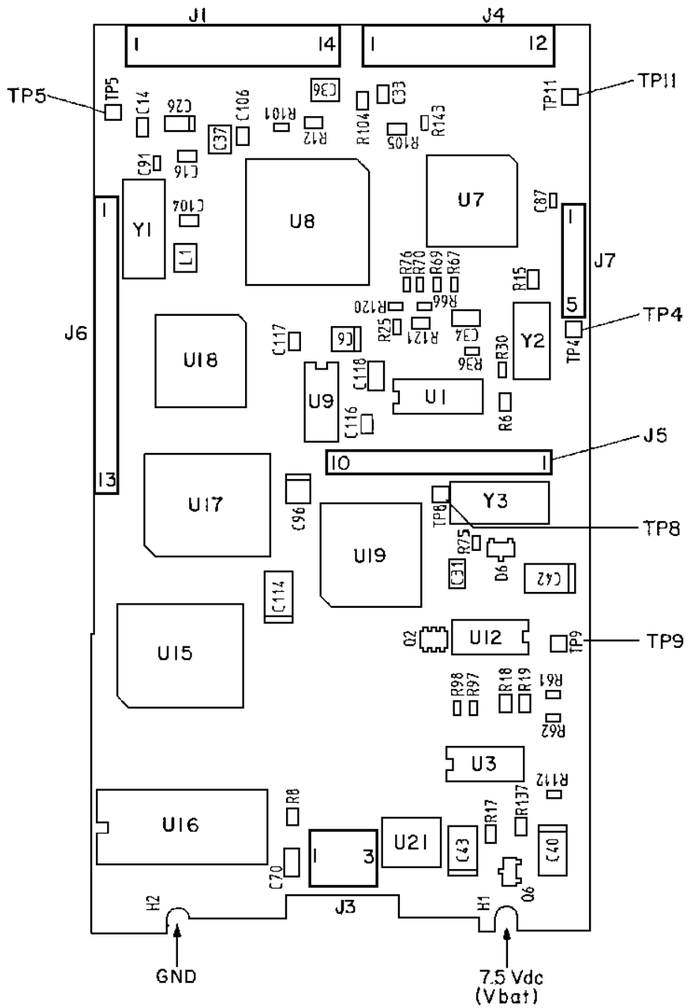
TP5 = Reset Output From Modem U19

TP8 = 11.0592 MHz Clock From Modem U19

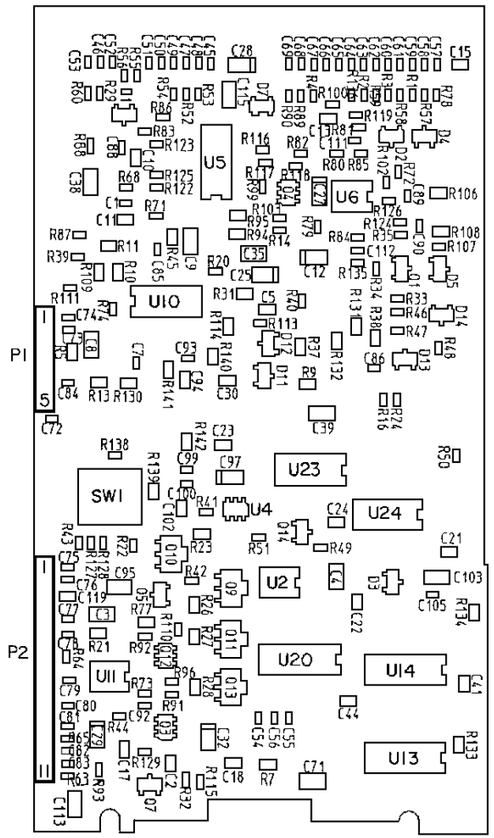
TP9 = Reset Input To Modem U19 (RESET_IN)

TP11 = 5.4 Vdc Regulated Supply (VCCA)

COMPONENT SIDE



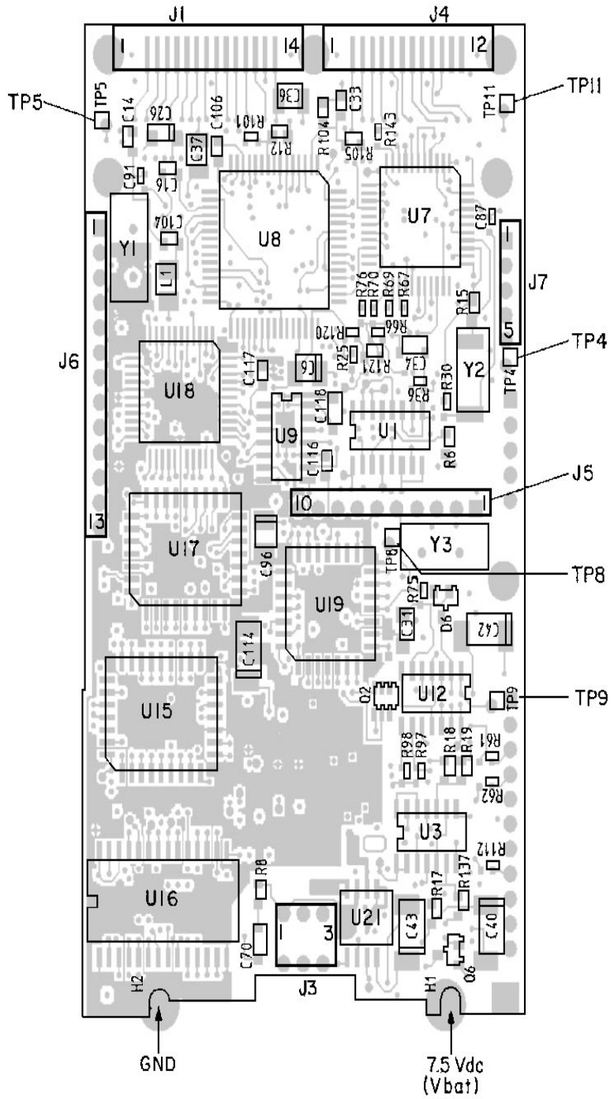
SOLDER SIDE



TEST POINTS

CONTROL BOARD
19D903081G1

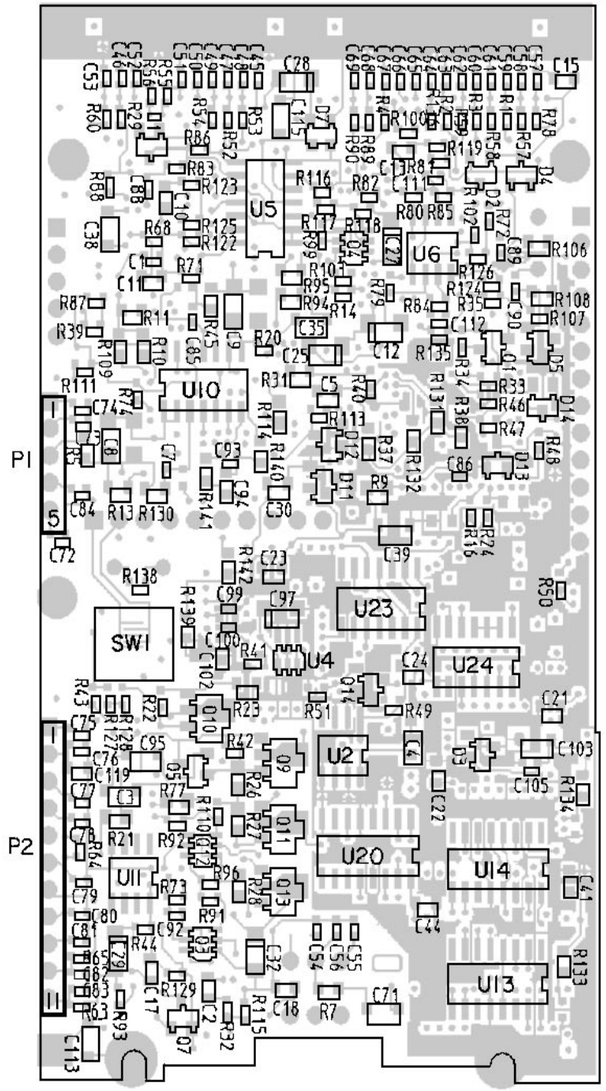
COMPONENT SIDE



(19D903081, Sh. 1, Rev. 7)
(19D903082, Layer 1, Rev. 0)

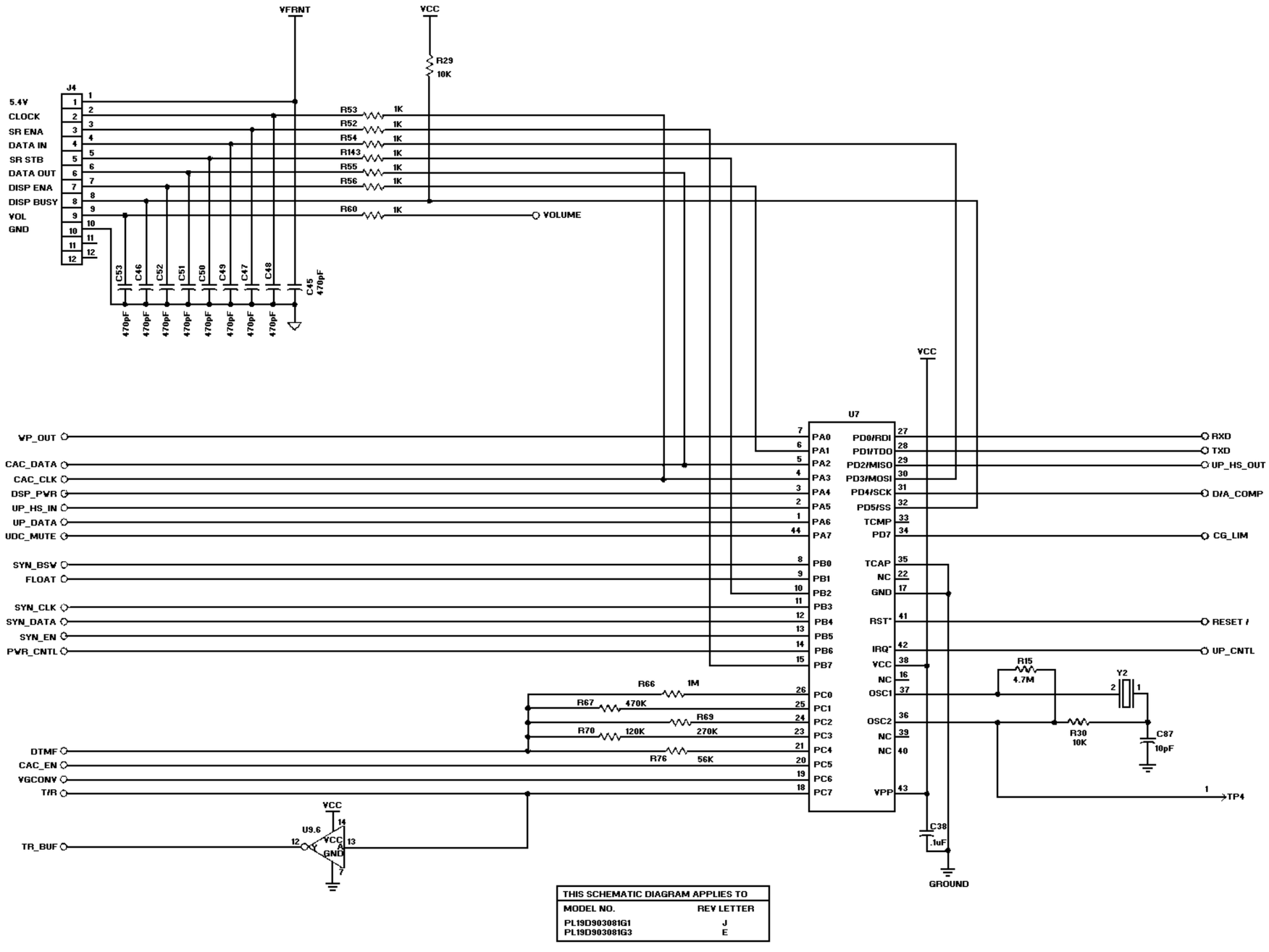
CAUTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES

SOLDER SIDE



(19D903081, Sh. 1, Rev. 7)
(19D903082, Layer 8, Rev. 0)

CONTROL BOARD
19D903081G1
(19D903081, Sh. 1, Rev. 0)



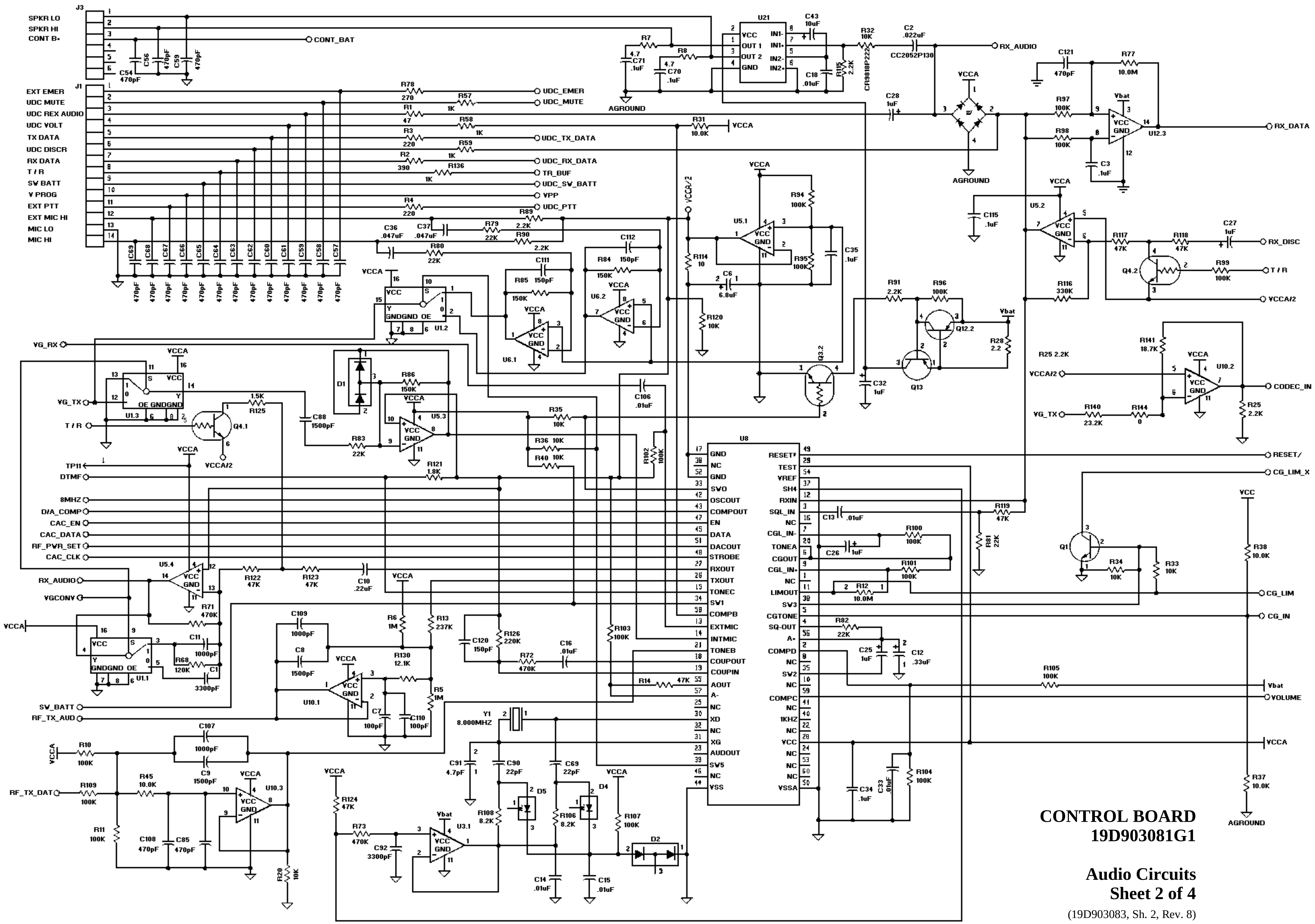
THIS SCHEMATIC DIAGRAM APPLIES TO

MODEL NO.	REV LETTER
PL19D903081G1	J
PL19D903081G3	E

CONTROL BOARD
19D903081G1
I/O Microcontroller U7

Sheet 1 of 4

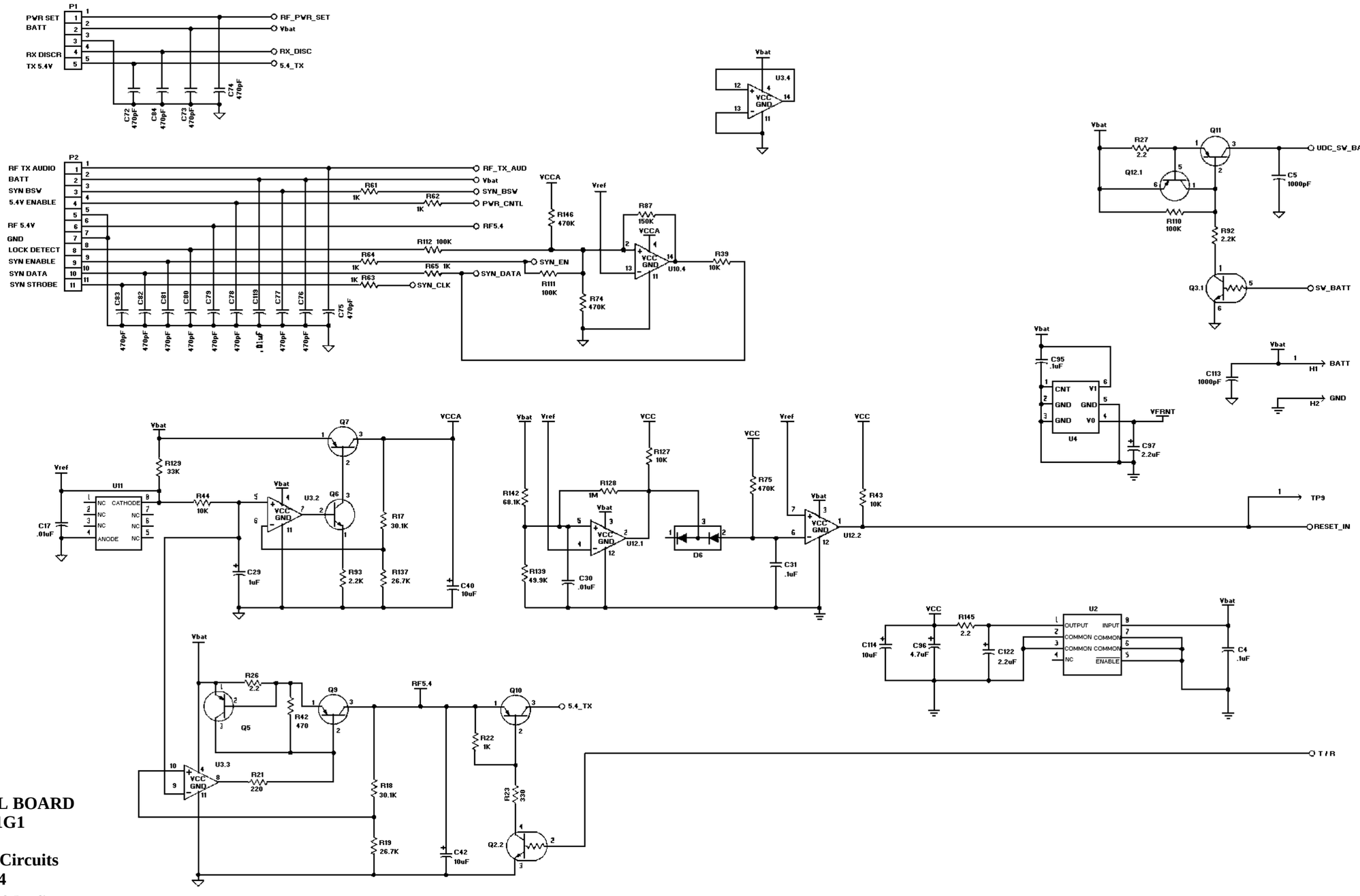
(19D903083, Sh. 1, Rev. 9)



CONTROL BOARD
19D903081G1

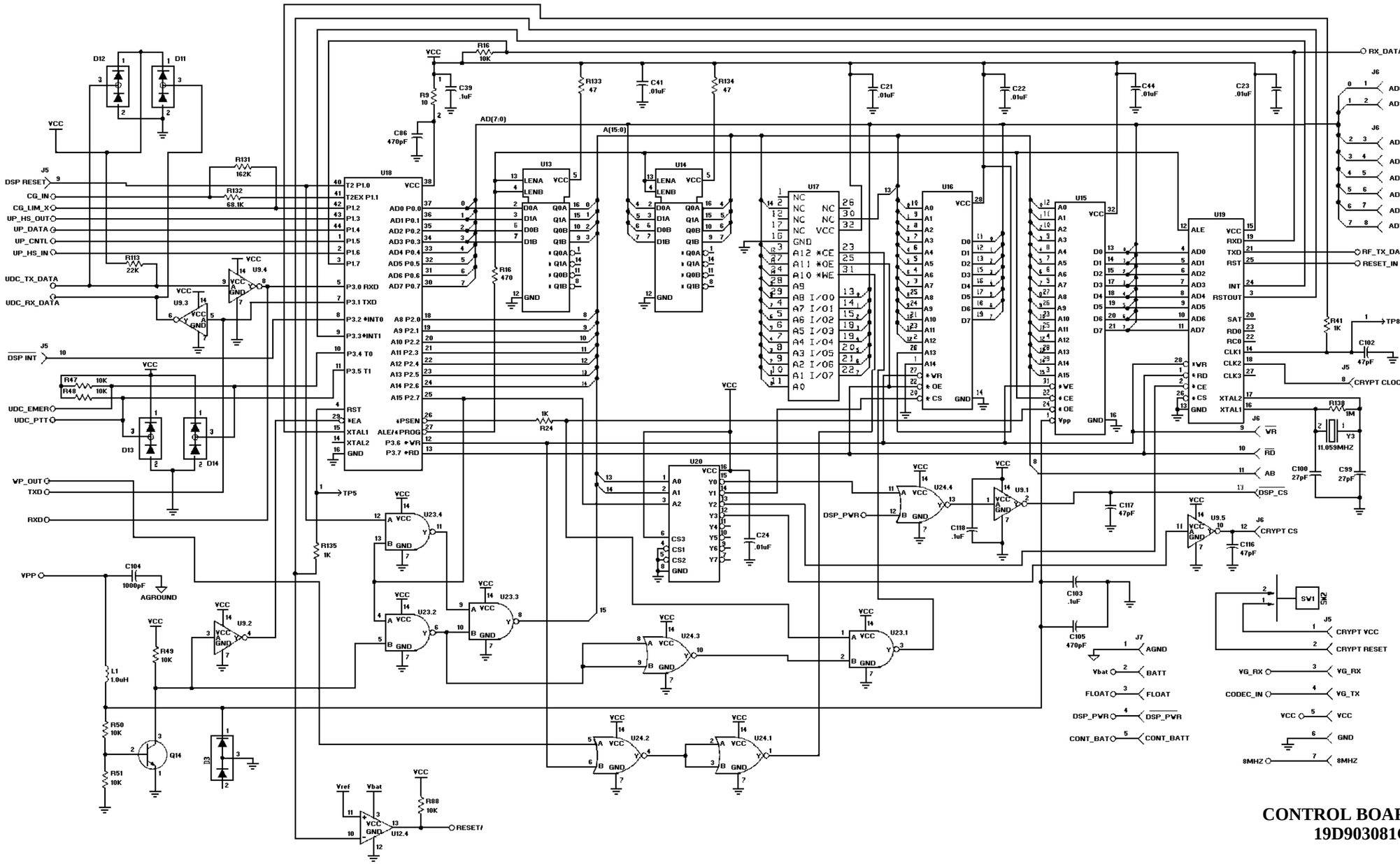
Audio Circuits
Sheet 2 of 4

(19D903083, Sh. 2, Rev. 8)



CONTROL BOARD
19D903081G1

Regulator Circuits
Sheet 3 of 4
(19D903083, Sh. 3, Rev. 3)



CONTROL BOARD
19D903081G1

Microprocessor Circuits
Sheet 4 of 4

(19D903083, Sh. 4, Rev. 2)