MAINTENANCE MANUAL

AEGIS MODULE
344A3659P3

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DESCRIPTION

Aegis M-PA radios equipped with DES encrypt/decrypt option PAVS require Aegis Module 344A3659P3. This module is also used in the M-PA Voice Guard radios equipped with DES encrypt/decrypt option PAVG. The Aegis Module is electrically connected to the Control Board by single-in-line connector pairs J5/P5, J6/P6 and J7/P7. The module is located just above the speaker in the assembled radio. This maintenance manual describes the module and how it is interfaced to the Control Board to provide Aegis digital and private (encrypt/decrypt) voice operation for the Aegis M-PA and M-PA Voice Guard radios.

The module contains circuitry that digitizes and compresses microphone audio when the radio is transmitting Aegis digital signals and the reverse process for receive audio when the radio is receiving Aegis digital signals. The Data Encryption Standard (DES) IC is also located on the module and it is utilized when the radio is operating in private mode. The module is directly controlled by the microprocessor circuitry on the Control Board.

When the radio is operating in private transmit mode, the Aegis Module provides voice A/D conversion, compression and DES encryption. It provides the reverse process (DES decryption, expansion and D/A conversion) when the radio is operating in private receive mode. The DES encrypt/decrypt process is bypassed when the radio is operating in Aegis digital mode.

Three (3) integrated circuits on the module, CODEC U7, DSP U2 and DES IC U1, are "chip-on-board components". The leads on these ICs are not directly accessible for troubleshooting and the ICs cannot be replaced.

CIRCUIT ANALYSIS

DATA BUS AND CONTROL LINE INTERFACE

Data is transferred between the Aegis Module and the Control Board by the 8-bit bidirectional data bus. Connector P6 on the Aegis Module mates with J6 on the Control Board to provide this interconnection.

DES IC U1 is directly connected to this data bus for data transfers. The read ($\overline{RD}$) and write ($\overline{WR}$) lines from the 80C52 on the Control Board control the direction of the data transfers.

Data transferred to and from DSP U2 and the 80C52 is buffered by octal TRI-STATE® transceiver U3. This transceiver's direction is controlled by the read ($\overline{RD}$) line from the 80C52. When the 80C52 reads data from U2 it pulls $\overline{RD}$ low and U3 buffers data from U2 to the 80C52's data bus. This process is reversed when the 80C52 writes to U2 ($\overline{RD}$ is high). Transceiver U3 data lines are floated when the 80C52 is not communicating with U2. The 80C52 does this by pulling the $\overline{DSP\ CS}$ line on J6/P6 pin 13 high.

Integrated circuit U6 is a hex TRI-STATE® buffer that buffers five (5) control lines from the 80C52 to the DSP. In addition, one buffer in the IC buffers the 8 MHz clock signal from the Control Board (J5/P5 pin 7). This buffered clock signal is applied to the clock inputs of DSP U2 and counter U4. U6's outputs (pins 3, 5, 7, 9, 11 and 13) are floated when the DSP and CODEC ICs are powered down (when the switched 5.0 Vdc supply is turned off). This occurs when the FLOAT line from the I/O Microcontroller on the Control Board is high. This action prevents the control line signals and the 8 MHz clock signal from passing to the powered down circuits.

CODEC U7

CODEC (COder/DECoder) U7 provides input anti-alias filtering, speech A/D and D/A conversion and output reconstruction filtering.

During Aegis digital transmit or private transmit operation, microphone audio from the selected microphone amplifier on the Control Board is applied to the CODEC's input via the VG_TX line. U7 then supplies an 8-bit mu-law companded sample of the input signal to the DSP every 172.4 microseconds. This sample is shifted into the serial input (SI) of the DSP.

During Aegis digital receive or private receive operation, U7 receives an 8-bit sample from the serial output (SO) of the DSP. U7 then supplies the D/A converted signal on its output. This analog output is the D/A converted signal. It is applied to the Control Board via the VG_RX line (J5/P5 pin 3). On the Control Board, this signal is then filtered, amplified, and applied to the speaker.

DSP U2

Digital Signal Processor U2 is a 7725 DSP that is programmed with a proprietary adaptive multiband encoding (AME) bandwidth compression/expansion algorithm for Aegis operations. The IC will also operate using the proprietary sub-band coding (SBC) algorithm for Voice Guard operations. The DSP compresses the digitized mic audio from the CODEC when the radio is transmitting in Aegis digital or private mode and when the radio is receiving, it expands the digitized signal before it is applied to the CODEC. U2 is directly controlled by, and exchanges data with, the 80C52 Microprocessor on the Control Board. The 8-bit data bus provides the data path between the two ICs.

When transmitting an Aegis digital or private signal, digitized mic audio from the CODEC is applied to the serial input (SI) of the DSP at a rate of 46400 bps. The DSP then compresses the data to approximately 9200 bps and the 80C52 reads the compressed data via the 8-bit data bus.

When receiving an Aegis digital or a private signal, the 80C52 transfers data to the DSP. The DSP then expands the data from a rate of approximately 9200 bps to a rate of 46400 bps. The expanded data is then applied to the CODEC via the serial output (SO) of the DSP.

DES IC U1

DES IC U1 provides DES encryption and decryption for both Aegis private and Voice Guard private operation. The 80C52 on the Control Board transfers data to and from U1 for DES encryption/decryption. This IC is certified by the National Bureau of Standards (NBS).

The DES IC also stores the cryptographic keys that are transferred into the radio from the Keyloader. These keys are maintained in a low-power RAM within the IC. Continuous battery power (CONT BATT) from J7/P7 pin 5 is regulated by U11 to 5.0 Vdc. This continuous 5.0 Vdc supply is applied to U1 for key storage. Capacitors C22 and C23 store a sufficient charge to retain the keys through battery changes (typically three minutes). Thirty (30) second power interrupt key retention is guaranteed.

DES keys must be zeroed or "dumped" when the radio is disassembled. This requirement is achieved using key dump switch SW1 on the Control Board. SW1 connects to J5/P5 pins 1 and 2 when the radio is assembled. When the radio is disassembled, SW1 opens and the connection between pins 1 and 2 opens. This causes the key clear ($\overline{POC}$) input of U1 to be pulled low by R9; the keys are zeroed.

DES chip-select (CRYPT CS) pulses from the Control Board on J6/P6 pin 12 are buffered and inverted by Q1. Transistor Q7 isolates U1 from undesirable chip-selects when the radio is powered down. This is accomplished by turning Q7 on via the $\overline{DSP\ PWR}$ line, thus preventing the CRYPT CS pulses from passing through Q1.

CLOCK CIRCUITS

Counters U4 and U5, and inverter U8 provide clock pulses to DSP U2 and CODEC U7. These clock pulses allow the two IC's serial interface to synchronize. Counter U5 also produces a 25 kHz clock for the negative power supply chopper circuit.

Integrated circuit U4 is a dual 4-bit decade counter; only one counter in this IC is used. The 8 MHz clock pulses from the Control Board (J5/P5 pin 7) are buffered by U6 and applied to U4 pin 4. U4 pin 6 produces 1.6 MHz clock pulses for the CODEC master clock. This signal is buffered by U8A and applied the master clock input of U7. A second clock signal from U4 is applied to U5 at pin 13.

Integrated circuit U5 is a dual 4-bit binary counter. Both counters in this IC are used. U5 pin 9 produces a 100 kHz shift clock pulses for the CODEC and the DSP ICs. U5 pin 5 produces 6.25 kHz frame sync pulses for the CODEC. U5 pin 6 produces interrupt pulses to the DSP at the completion of each data transfer. The DSP then resets U5's counter chain for the next data transfer via U8F.

REGULATOR CIRCUITS

Switched 5-Volt Regulator U12

Regulator U12 supplies switched 5.0 Vdc power to several ICs on the module. Battery power from J7/P7 pin 2 (typically 7.5 Vdc) is applied to U12's input (U12 pin 8. U12's output on pin 1 is switched on when $\overline{DSP\ PWR}$ (J7/P7 pin 4) is low. This will supply regulated 5.0 Vdc to ICs U2, U5 and U7 via the SW5 line. U12 is a low drop-out voltage regulator IC that can maintain a well regulated output (±0.25 Vdc) even if the battery voltage falls to approximately 5.6 Vdc. It also provides output over-voltage and current limit protection.

To conserve battery power when the radio is in standby or clear modes, I/O Microcontroller U7 on the Control Board pulls $\overline{DSP\ PWR}$ high. This powers down U2, U5 and U7 by turning U12's 5.0 Vdc output off.

Chopper and -5.0-Volt Power Supply

CODEC U7 requires a -5.O Vdc regulated supply for operation. Transistors Q2 - Q6, regulator U10, and associated components generate this negative supply from the positive (with respect to ground) BATT source at J7/P7 pin 2.

A 25 kHz clock signal from U5 pin 3 is applied to the chopper circuit. This signal is applied directly to transistors Q2 and Q4 via R16, C8 and C9. Transistor Q6 buffers the 25 kHz clock signal to provide an out-of-phase signal to transistors Q3 and Q5 via R17, C10 and C11. The resulting chopper action charges C14 to approximately -10 Vdc.

Regulator U10 regulates the -10 Vdc source from the chopper circuit to -5.0 Vdc. This regulated negative supply is applied to the CODEC.

TROUBLESHOOTING

CAUTION

Unplug the Aegis Module from the Control Board by lifting it straight up. DO NOT lift or pry it up at an angle. This will prevent bending of the male contacts on the Aegis Module and damage to the female contacts on the Control Board.

The Aegis Module contains CMOS ICs that can be damaged by static electricity. Observe static handling precautions.

NOTE

If the radio is disassembled for service, anti-tamper switch SW1 on the Control Board must be bypassed by shorting J5/P5 pins 1 and 2 or by securing the rubber switch actuator in a depressed position. This must be done before loading a cryptographic key and operating the radio in the private mode. After service is completed, the bypassing must be eliminated.

SYMPTOM AND CAUSE OUTLINE

Radio Does Not Display "KEY LOAD"

The radio must be turned on after the Keyloader is attached to the UDC. When the radio is powered-up, it samples the UDC VOLT pin (J101 pin 9) and recognizes that the Keyloader is attached. The radio will not recognize the Keyloader if it is attached after the radio is powered-up.

1. Verify the UDC contacts on the radio and the Keyloader's cable are clean.
2. Check the UDC VOLT flex connection between the UDC and the Control Board.
3. Check the UDC VOLT circuitry. This can be done by connecting a speaker/microphone to the UDC, turning the radio on, and verifying correct speaker/mic operation.

Transferred Key Is Not Recognized

If "GOOD TRANSFER" is displayed after a key transfer is executed, the selected key has most likely been transferred into one (1) of the seven (7) possible key storage locations in the radio. The selected group/channel may be programmed to use a different key (different storage location) than the one transferred. In this case, the radio will display "NO KEY x" (where "x" is programmed cryptographic key number) when the group/channel is selected.

1. Transfer all necessary keys and/or verify the radio's personality programming for group/channel-to-key selection.
2. A problem may exist with the DSP circuitry on the Aegis Module. This circuitry is utilized after the keys are transferred. The radio may display "DSP ERR". The Keyloader will not display an error code if there is a problem with the DSP circuitry. See **DSP Circuitry Problems** for details.

Keyloader Displays Error Code

If the Keyloader displays "ERROR 1" after an attempted transfer the problem is generally in the serial interface circuity between the radio and the Keyloader. The M-PA uses the following UDC connections for key transfers: TX DATA, RX DATA, EXT PTT, EXT EMER.

Keyloader error codes other than "ERROR 1" indicate a possible problem with the cryptographic circuits on the Aegis Module. Such problems will generally cause the radio to display "DES ERR" at power-up.

1. Verify the Keyloader and cable are good by testing on a known good Aegis radio.
2. Check the UDC contacts for dirt, corrosion, etc.
3. Check the flex connections between the UDC and the Control Board.
4. Using the PC programmer, verify correct operation of the UDC TX DATA, RX DATA and EXT PTT circuitry. Using the TQ-0609 Test Box, verify correct operation of the UDC EXT PTT and EXT EMER circuitry. If a problem exists see the troubleshooting information in LBI-38828. NOTE: To test the EXT EMER circuitry with the TQ-0609 Test Box, the radio must be programmed for lanyard operation.
5. See **Radio Displays "DES ERR"** troubleshooting information.

Keys Are Not Retained When Powered-Off

DES cryptographic keys are stored in volatile memory (RAM) within DES IC U1 on the Aegis Module. This IC is powered from the continuous (unswitched) battery power line from the battery pack and regulator U11. U11 regulates the 7.5 Vdc (±20%) battery voltage on CONT BATT to 5.0 Vdc required by the DES IC. Since the DES IC will often operate from power supplied through other pins (such as the data bus), a lack of power-off key retention may be the only indication of continuous 5.0 Vdc power failure.

The continuous power output from the battery pack is current limited by a resistor inside the battery pack.

1. Connect a battery pack to the radio. The battery eliminator test accessory may not be used for this test, as it does not provide continuous power to the radio.
2. Turn the radio off.
3. Check the CONT BATT voltage at J7/P7 pin 5. If no power is present, there is an open between this pin and the battery's continuous power pin. This connection follows this path: Battery Plate CONT B+ connection, Speaker Flex H1 to P3 pin 1, Control Board J3 pin 1 to J7 pin 5.
4. Check U11 for a 7.5 Vdc input and a 5.0 Vdc output.

Keys Are Not Retained When Battery Is Changed

A DES radio should normally retain cryptographic keys for several minutes (typically three) after the battery pack is removed. The charge stored in capacitors C22 and C23 on the Aegis Module provide the necessary power for the DES IC during a battery change. Thirty (30) second power interrupt key retention is guaranteed.

1. Check for an open or leaky C22 and C23.
2. Check for a leaky C7, C24 or Q1.
3. Check for leaky bypass capacitors on the Control Board (CONT_BAT) and on the Battery Plate (CONT B+).

Radio Displays "DES ERR"

A DES circuit malfunction may cause the radio to display "DES ERR" when it is powered-up or when a private transmission is attempted.

1. Verify proper operation of anti-tamper switch SW1 on the Control Board. When the switch is depressed, Control Board connector J5 pins 1 and 2 should short.
2. Verify the DES +5V supply is 5.0 Vdc ±0.3 Vdc. If not, check regulator U11 and associated components.
3. With the anti-tamper switch depressed, verify the $\overline{\text{POC}}$ input (active low) of DES IC U1 is greater than 4.0 Vdc. If not, suspect the anti-tamper switch, C6, R9 or R12.
4. Monitor J5/P5 pin 8, CRYPT CLK, for 614 kHz 2/3 duty cycle clock pulses from modem U19 on the Control Board.
5. Verify the DES chip select circuit is operating by preforming the following steps:
   a. Turn the radio off and connect the Keyloader to the UDC. Power-up the radio and Keyloader.
   b. Monitor J6/P6 pin 12 (CRYPT CS). Pulse activity should occur when the radio is turned on. If no activity is present, suspect inverter U9E or decoder U20 on the Control Board.
   c. Verify a similar inverted signal is on the collector of Q1 when the radio is turned on. If not, suspect Q1, Q7, the $\overline{\text{DSP PWR}}$ line, or the associated components. Transistor Q7 holds Q1 off when the $\overline{\text{DSP PWR}}$ line is high.
6. Check the data bus (J6/P6 pins 1 - 8) for pulse activity. If any of the data lines are not pulsing and are at ground, suspect an open in the associated contact or on the Control Board.
7. Replace the Aegis Module if all of the above checks are correct.

Radio Will Not Transmit Aegis Digital Or Private

1. Verify correct programming of TX data polarity and TX outside addresses.
2. Microphone audio from the Control Board should be on J5/P5 pin 4 (VG TX). If no audio is present, troubleshoot the mic audio circuity on the Control Board. See LBI-38828 for details.

3. Monitor R10 at the terminal connected to U7 pin 14. A signal should be present which is approximately 3.3 times the level of the mic audio signal on J5/P5 pin 4. U7 pins 14 - 16 are pins of an op amp inside U7. If the amplified signal is not present, suspect C1, R11, R10 or U7. This point should be 0 Vdc.

Radio Will Not Receive Aegis Digital Or Private

1. Verify correct programming of RX data polarity and RX outside addresses.

2. If the radio does not recognize an Aegis digital or a private signal suspect modem U19 or associated circuitry on the Control Board. When the radio receives a private signal the "PVT" status flag should flash.

3. If the radio appears to receive a transmission ("BSY" status flag turns on and "PVT" status flag flashes if an encrypted signal) but no audio is heard in the speaker, suspect a problem in the Control Board's audio circuitry or a problem with CODEC U7 on the Aegis Module. Decrypted audio should be present on J5/P5 pin 3 (VG RX) at a level of 500 - 1000 mVp-p with average speech into the transmitting radio. If no audio is present on this pin, the CODEC is most likely defective and Aegis Module replacement will be required. If audio is present, troubleshoot the digital/private mode receive audio path circuity on the Control Board. See LBI-38828 for details.

Radio Will Not Transmit Or Receive Aegis Digital And Private

Complete Aegis digital and private failure may be a problem with modem U19 on the Control Board, or a DSP or CODEC circuit failure on the Aegis Module. In addition, programming related problems include incorrect TX and RX outside addresses, incorrect TX and RX data polarity, or incorrect cryptographic key number selection. If available, substitute the suspected problem Aegis Module with a known good Aegis Module.

1. If the radio is a trunking radio and it operates normally in clear voice trunked mode, the modem is functioning properly.

   If the radio is a conventional radio equipped with an encrypt/decrypt option, observe the "PVT" and "BSY" status flags when the radio is receiving a valid encrypted transmission.

   a. If the "PVT" status flag does not flash and "BSY" status flag stays on continuously, check the modem circuits. Also verify outside address and data polarity programming.

   b. If "PVT" and "BSY" both flash, verify the correct cryptographic key number selection is programmed into the personality of the radio. Verify the same cryptographic key is loaded in both transmitting and receiving units. Also see **DSP Circuitry Problems**

   c. If "PVT" flashes and "BSY" stays on continuously, check the CODEC and audio circuits on the Aegis Module as follows:

2. Verify the -5.0 Vdc supply to the CODEC is present at U10 pin 1. If this negative supply is low or missing, suspect chopper circuit Q2 - Q6 and associated components. U5 pin 3 supplies 25 kHz pulses to this circuit which converts the positive battery voltage to a negative voltage of approximately -10 Vdc. This -10 Vdc source is regulated to -5.0 Vdc by U10.

3. Verify the clock pulses are present on the outputs of inverters U8A, U8C and U8E. See the **CIRCUIT ANALYSIS** for details.

DSP Circuitry Problems

DSP problems may cause the radio to display "DSP ERR" or one of the following may be observed:

- after transferring a key, the radio frequently appears to have no key, even if the Keyloader displays "GOOD TRANSFER"
- the "TX" status flag continuously blinks during private transmit; for a trunking radio, this condition should not be confused with normal retry and queueing activities
- the "PVT" and "BSY" status flags both blink during private receive

1. If available, substitute the Aegis Module or the Control Board with a known good unit.

2. Visually inspect the connectors between the two boards for broken or damaged pins and sockets. Check the continuity of each pin between the Control Board and the Aegis Module. Also check between the related circuity on each board.

3. Verify the logic on the Control Board for $\overline{\text{DSP\_CS}}$ (J6/P6 pin 13) is operating correctly.

4. If substitution reveals a problem with the Aegis Module, check the $\overline{\text{DSP PWR}}$ and FLOAT circuits. These logic lines power-up and activate DSP U2 and related circuits only when needed.

   a. Connect the Keyloader to the UDC and turn the radio on. This will continuously power-up the DSP circuits to allow troubleshooting.

   b. Check regulator U12 for a 5.0 Vdc output.

   c. Verify the 8 MHz clock from the Control Board is present on U6 pin 11.

   d. Check the $\overline{\text{RD}}$, $\overline{\text{WR}}$ and $\overline{\text{DSP CS}}$ lines for occasional low-going pulses. Also verify A8 is transitioning.

   e. DSP RESET on J5/P5 pin 9 should be high.

   f. $\overline{\text{DSP INT}}$ on J5/P5 pin 10 should be low with the Keyloader attached.

   g. Verify there is pulse activity on the DSP side of octal transceiver U3 (pins 11 - 18).

   h. Verify a 1.6 MHz clock is present on U4 pin 6 and U8A pin 2.

   i. Verify an 800 kHz clock is present on U4 pin 3 and U5 pin 13.

5. DSP operation occurs when DSP RESET at J5/P5 pin 9 is low. Verify DSP start-up by transferring a key or initiating an Aegis digital or a private transmission.

   a. During a key transfer, hex buffer U6 is continuously enabled (the outputs are not floating) and the DSP RESET signal appears on U6 pin 13. Verify DSP RESET (J5/P5 pin 9) and U6 pin 13 pulse low briefly when a key is transferred.

   b. When the radio is keyed in Aegis digital or private mode, DSP RESET transitions from high to low and the DSP operates for the duration of the transmission (or until a hardware failure is detected). The buffered DSP RESET signal on U6 pin 13 may appear to be low when the outputs are not enabled at the start of a transmission, transition high when U6 is enabled, and transition low again simultaneously with J5/P5 pin 9.

   c. After DSP RESET transitions low, verify $\overline{\text{DSP INT}}$ (active low) on J5/P5 pin 10 goes high within 2 microseconds and verify U8F pin 13 goes high in approximately 100 microseconds. If not, and the signals in step 4 are correct, DSP U2 is defective and the Aegis Module must be replaced.

6. Check counter U5, the P0 output (counter reset), and P1 output ($\overline{\text{DSP INT}}$) from the DSP. The P0 pulse resets the outputs of counter U5 to a low level in response to a low-to-high transition from U5 pin 6. U2 sets its P1 output ($\overline{\text{DSP INT}}$) low when it has data for U18 on the Control Board. This line goes high after the data has been read by U18.

   a. Verify the counter reset pulses are present on U8F pin 12. Also check pin 13 for inverted pulses. Pulses should occur at approximately 170 microsecond intervals and should be approximately 10 microseconds wide. During a key transfer, only a burst of pulses should occur. A continuous stream of pulses should occur during Aegis digital or private mode transmissions. The outputs of counter U5 are reset low when U8F pin 12 goes high.

   b. If U5 pin 6 remains low, this counter is probably defective. If a 320 microsecond period square-wave is present, U2's INT input is defective and the Aegis Module must be replaced. When the DSP and counter circuits are operating correctly the signal on U5 pin 6 is a stream (or a single burst for key transfers) of 1 microsecond wide, active high pulses approximately every 170 microseconds.

   c. Trigger the scope on high-to-low DSP RESET transitions while monitoring the counter reset pulses at U8F pin 13 during key transfers, Aegis digital or private mode transmit start-up. U8F pin 13 should start its active-low reset pulses 160 microseconds after its initial low-to-high transition. After the third pulse, U8F pin 13 should remain low, then it should resume pulsing after a delay of 50 - 60 milliseconds. The pulses should continue for approximately 85 milliseconds for key transfers, and continuously for Aegis digital or private mode transmissions. If the initial three (3) pulses are incorrect, recheck the counter reset pulse and counter U5 using DSP RESET as the triggering source. If the 50 - 60 millisecond delay is incorrect, recheck transceiver U3 and buffer U6. Suspect U2 if U3 and U6 are operating correctly.

d. If the second group of counter reset pulses is missing or if there are only a few pulses after the delay, trigger the scope on high-to-low DSP RESET transitions and monitor DSP INT on J5/P5 pin 10. At the start of the second group of counter reset pulses, DSP INT should pulse low for 70 - 80 microseconds, and every 32 counter reset pulses thereafter (every 5.5 milliseconds). If DSP INT does not go low, recheck buffer U6, particularly buffered DSP CS and WR signals. Also recheck transceiver U3 and the DSP CS circuits on the Control Board. If DSP INT goes low at the correct time but remains low, recheck buffer U6, particularly the DSP CS and RD signals, and recheck U3. Also suspect the DSP INT input of U18 on the Control Board. If there are only a few DSP INT pulses or if the pulse spacing is incorrect, recheck transceiver U3.

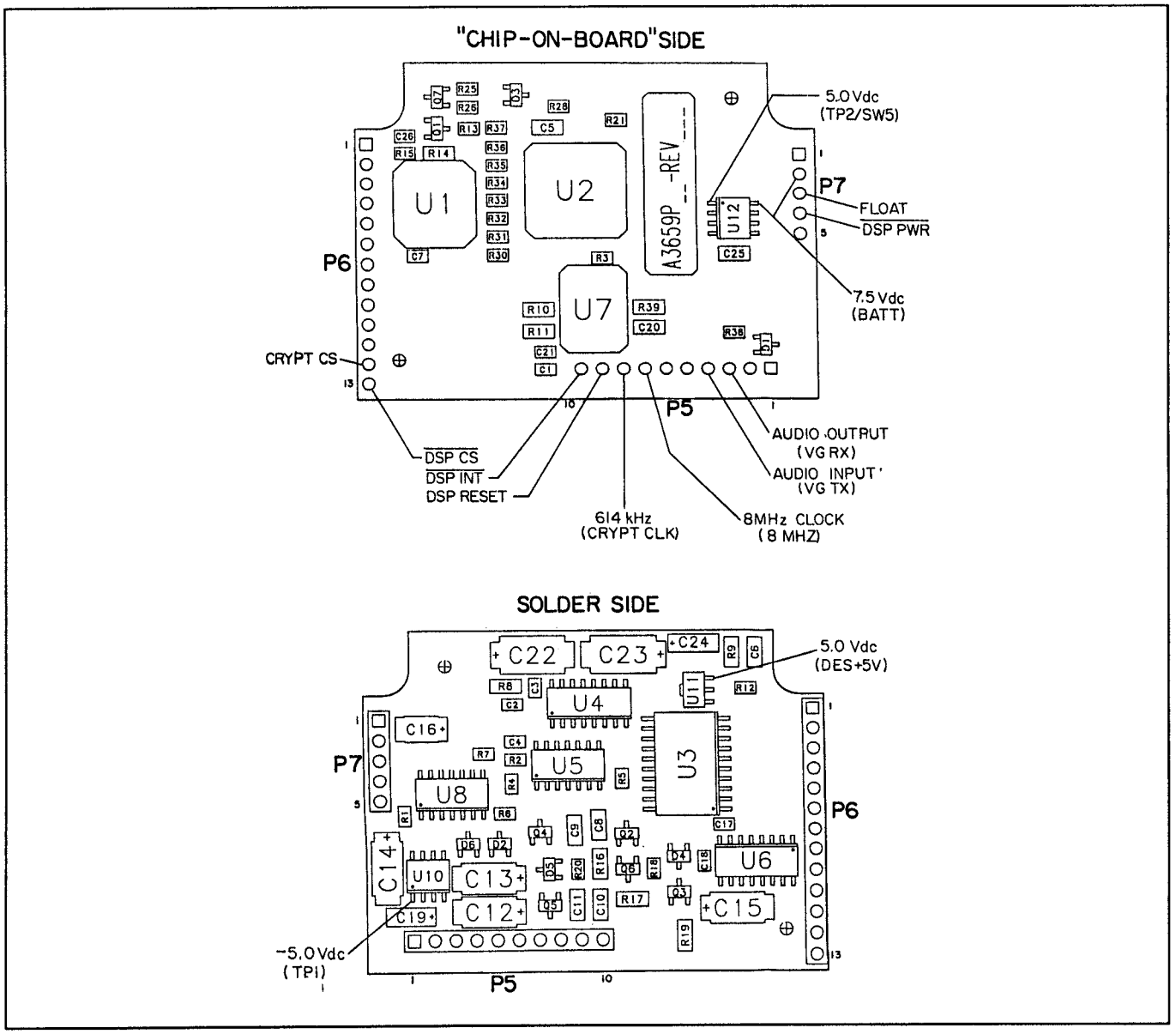
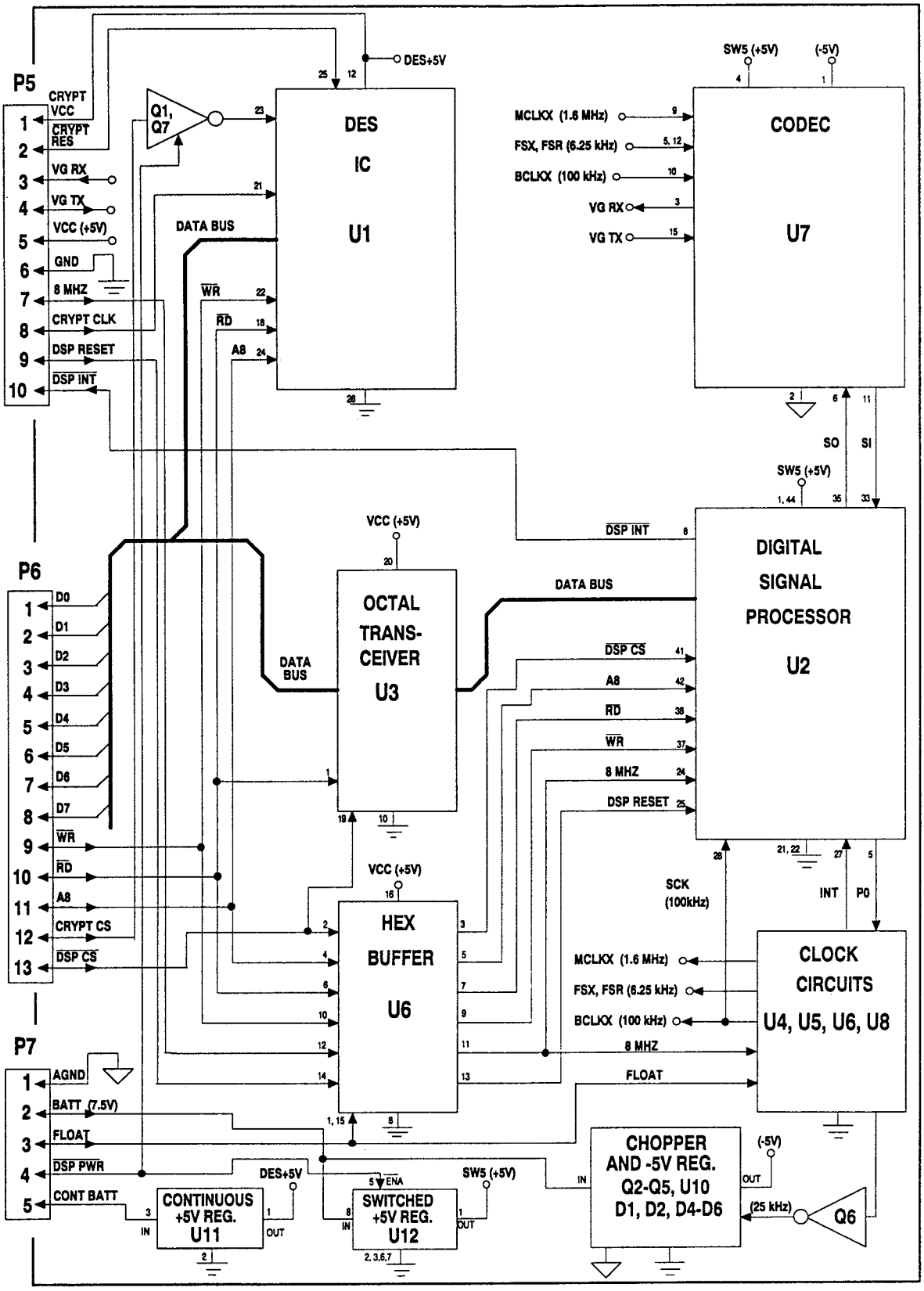


Figure 1 - Test Points

ERICSSON

Ericsson GE Mobile Communications Inc.
Mountain View Road • Lynchburg, Virginia 24502

Printed in U.S.A.



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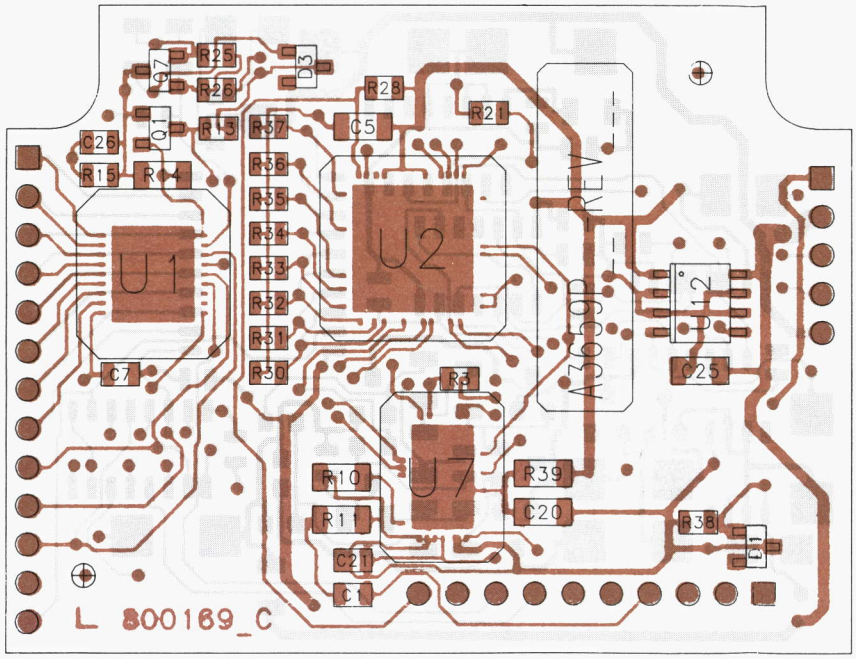
"CHIP-ON-BOARD" SIDE

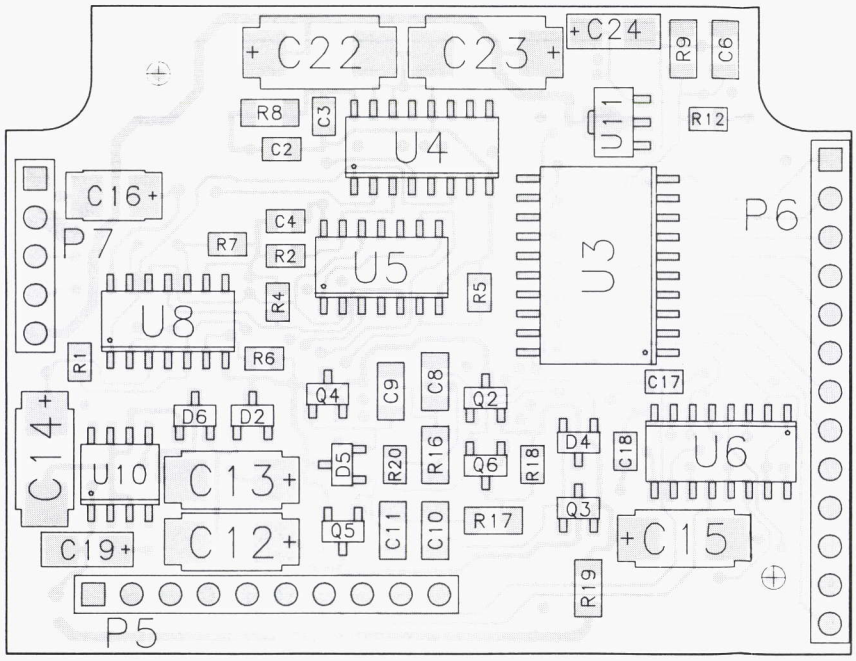


(900169-ASO-B-OC, Sh. 1, Rev. C)

(800169-CU-OC, Layer 1, Rev. C)

(800169-CU-OC, Layer 4, Rev. C)

SOLDER SIDE



(900169-ASO-B-OC, Sh. 2, Rev. C)

(800169-CU-OC, Layer 4, Rev. C)

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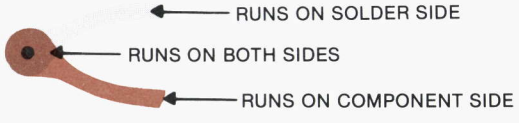
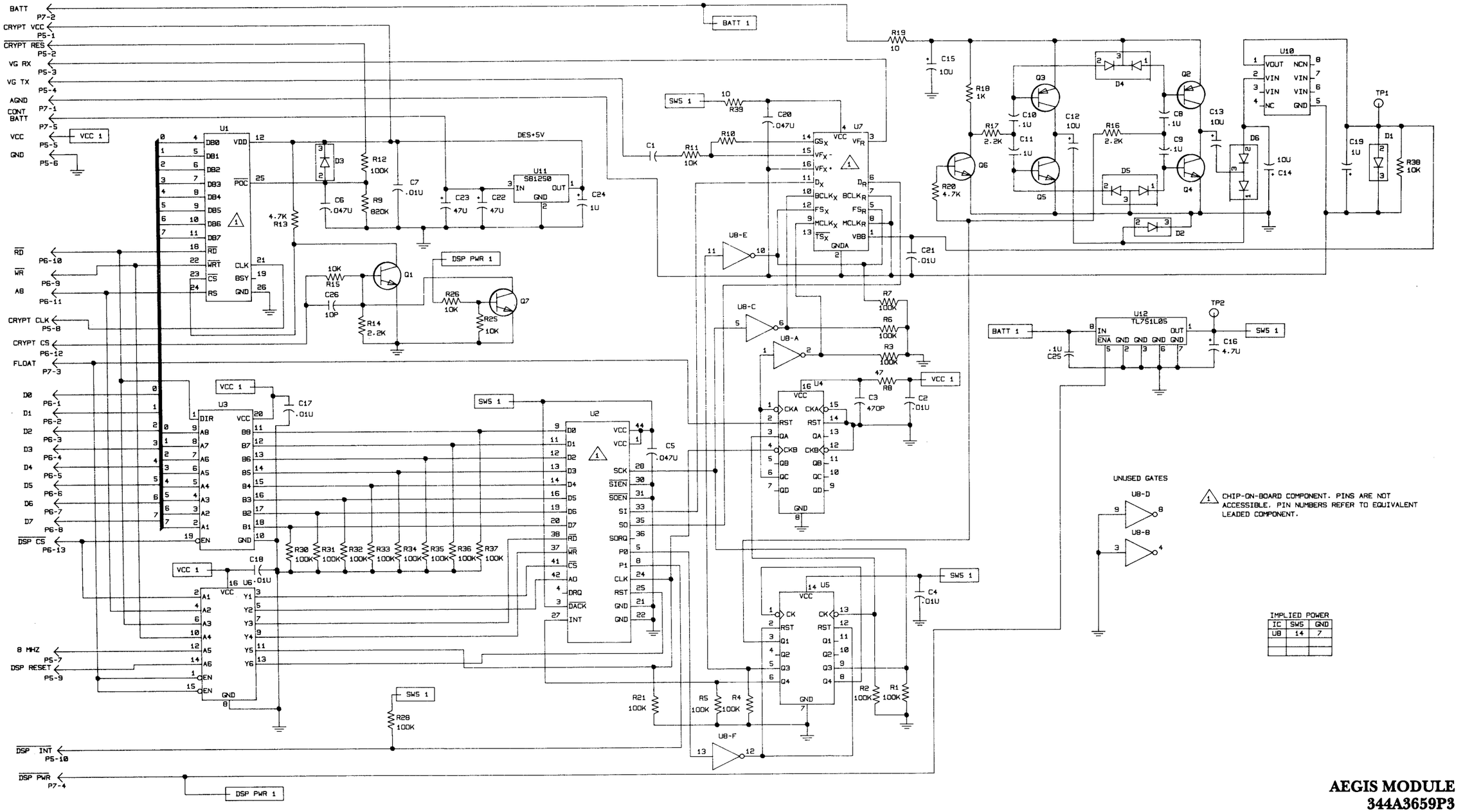
(900169-AS0-B-0C, Rev. C)

CAUTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES





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(19D903571, Sheet 1, Rev. 0)

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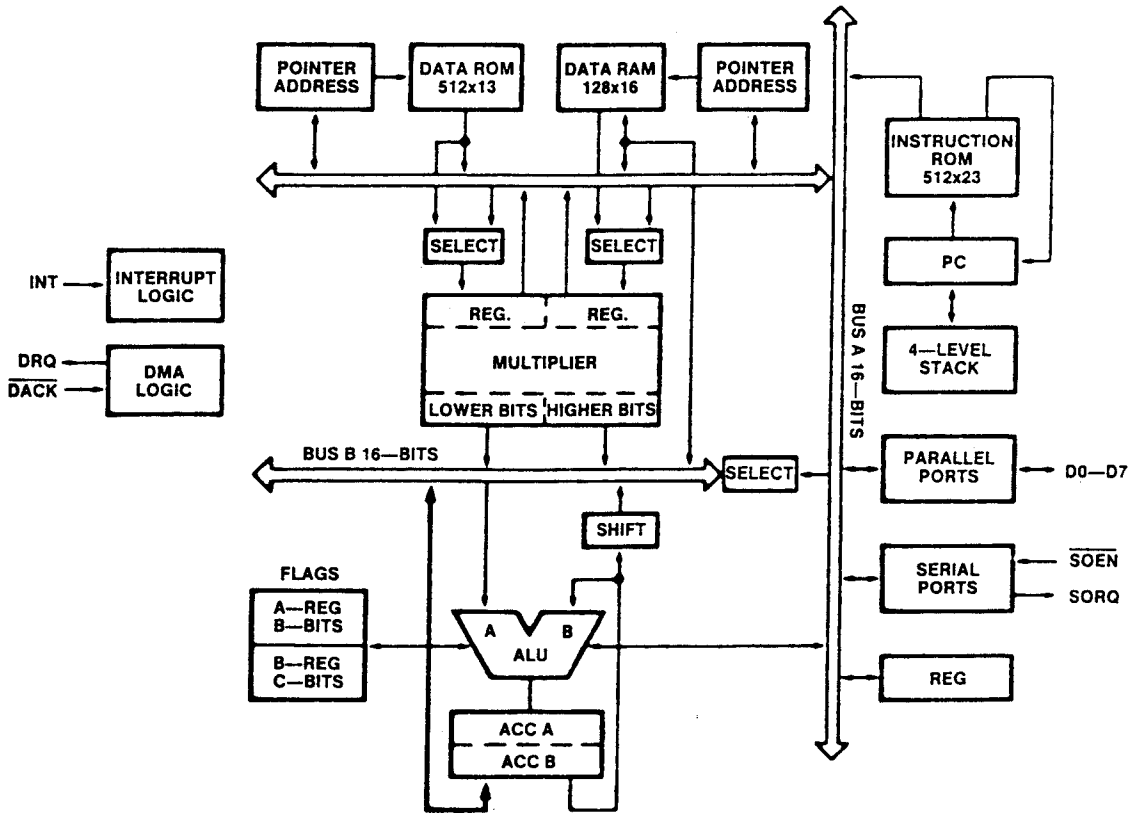
ISSUE 1

SYMBOL	PART NUMBER	DESCRIPTION
		——— CAPACITORS ———
C1	19A702052P16	Ceramic: 0.015 µF ±10%, 50 VDCW.
C2	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C3	19A702052P3	Ceramic: 470 pF ±10%, 50 VDCW.
C4	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C5 and C6	19A702052P22	Ceramic: 0.047 µF ±10%, 50 VDCW.
C7	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C8 thru C11	19A702052P33	Ceramic: 0.1 µF ±10%, 50 VDCW.
C12 thru C15	19A705205P6	Tantalum: 10 µF, 16 VDCW; sim to Sprague 293D.
C16	19A705205P13	Tantalum: 4.7 µF, 10 VDCW; sim to Sprague 293D.
C17 and C18	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C19	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C20	19A702052P22	Ceramic: 0.047 µF 10%, 50 VDCW.
C21	19A702052P14	Ceramic: 0.01 µF 10%, 50 VDCW.
C22 and C23	19A705205P111	Tantalum: 47 µF, 10 VDCW; sim to Sprague 293D.
C24	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C25	19A702052P33	Ceramic: 0.1 µF ±10%, 50 VDCW.
C26	19A702061P13	Ceramic: 10 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
		——————— DIODES ———————
D1	19A705377P2	Silicon, hot carrier: sim to BAS70.
D2 and D3	19A700155P2	Silicon: 100 mA, 35 PIV.
D4	19A134587P2	Silicon: 2 Diodes In Series, Common Cathode; sim to BAV70.
D5	19A703561P2	Silicon: 2 Diodes In Series, Common Anode; sim to BAW56.
D6	19A700053P2	Silicon: 2 Diodes In Series; sim to BAV99.
		——————CONNECTORS ———————
P5	19B801235P4	Terminal: 10-Pin, Gold Plated.
P6	19B801235P9	Terminal: 13-Pin, Gold Plated.
P7	19B801235P5	Terminal: 5-Pin, Gold Plated.
		——————TRANSISTORS ———————
Q1	19A700078P2	Silicon, NPN: sim to MMBT3904, low profile.
Q2 and Q3		Silicon, PNP: sim to BCX17.
Q4 and Q5		Silicon, NPN: sim to BCX19.
Q6 and Q7	19A700078P2	Silicon, NPN: sim to MMBT3904, low profile.

SYMBOL	PART NUMBER	DESCRIPTION
		——————— RESISTORS ———————
R1 thru R7	19B801251P104	Metal film: 100K ohms ±5%, 1/10 W.
R8	19B800607P470	Metal film: 47 ohms ±5%, 1/8 W.
R9	19B800607P824	Metal film: 820K ohms ±5%, 1/8 W.
R10	19A702931P351	Metal film: 33.2K ohms ±1%, 1/8 W.
R11	19A702931P301	Metal film: 10K ohms ±1%, 1/8 W.
R12	19B801251P104	Metal film: 100K ohms ±5%, 1/10 W.
R13	19B801251P472	Metal film: 4.7K ohms ±5%, 1/10 W.
R14	19B800607P222	Metal film: 2.2K ohms ±5%, 1/8 W.
R15	19B801251P103	Metal film: 10K ohms ±5%, 1/10 W.
R16 and R17	19B800607P222	Metal film: 2.2K ohms ±5%, 1/8 W.
R18	19B801251P102	Metal film: 1K ohms ±5%, 1/10 W.
R19	19B800607P100	Metal film: 10 ohms ±5%, 1/8 W.
R20	19B801251P472	Metal film: 4.7K ohms ±5%, 1/10 W.
R21	19B801251P104	Metal film: 100K ohms ±5%, 1/10 W.
R25 and R26	19B801251P103	Metal film: 10K ohms ±5%, 1/10 W.
R28	19B801251P104	Metal film: 100K ohms ±5%, 1/10 W.
R30 thru R37	19B801251P104	Metal film: 100K ohms ±5%, 1/10 W.
R38	19B801251P103	Metal film: 10K ohms ±5%, 1/10 W.
R39	19B800607P100	Metal film: 10 ohms ±5%, 1/8 W.
		——— INTEGRATED CIRCUITS ———
		NOTE: U1, U2 and U7 are non-replacable "chip-on-board" components.
U1		Microprocessor: DES Encryption/Decryption.
U2		Digital Signal Processor; sim to 7725.
U3	19A703471P108	Digital: Octal Transceiver; sim to 74HC245D.
U4	19A703987P113	Digital: Dual 4-Bit Decade Counter; sim to 74HC390D.
U5	19A703987P114	Digital: Dual 4-Bit Binary Counter; sim to 74HC393D.
U6		Digital: Hex TRI-STATE Buffer; sim to 74HC365D.
U7		Digital: Coder-Decoder; sim to HC3054.
U8	19A703483P4	Digital: Hex Inverter; sim to 74HC04D.
U10	19A704971P4	Linear: Negative 5-Volt Regulator; sim to LM79L05.
U11		Linear: 5-Volt Regulator; sim to S81250HG-RD.
U12	344A3404P101	Linear: 5-Volt Regulator; sim to TL751L05D.

★ COMPONENTS, ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

U2



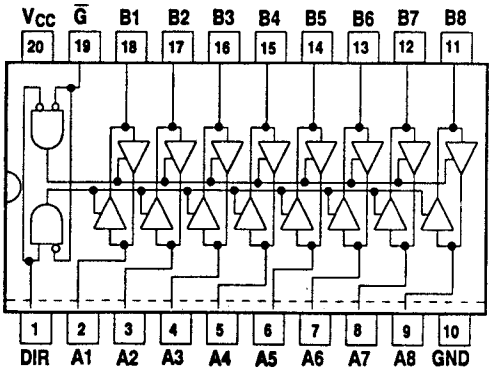
DIGITAL SIGNAL PROCESSOR
(7725)

U3

TRUTH TABLE

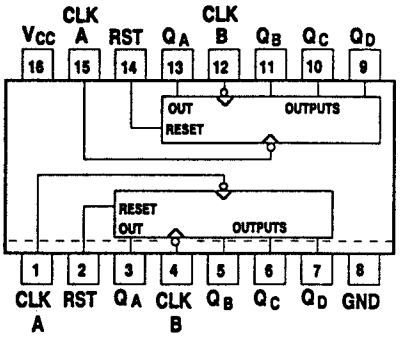
Control Inputs		Operation
$\overline{G}$	DIR	
L	L	A<<B
L	H	A>>B
H	X	Z

X=H or L
Z= High Impedance



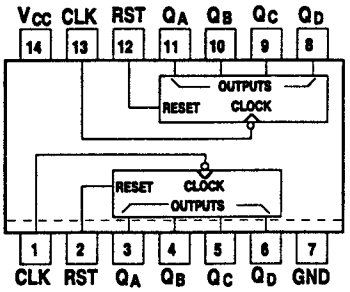
OCTAL TRANSCEIVER
19A703471P108

U4



DUAL 4-BIT DECADE COUNTER
19A703987P113

U5



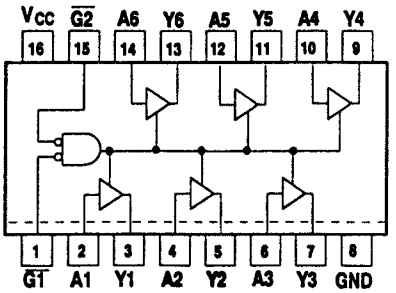
DUAL 4-BIT BINARY COUNTER
19A703987P114

U6

TRUTH TABLE

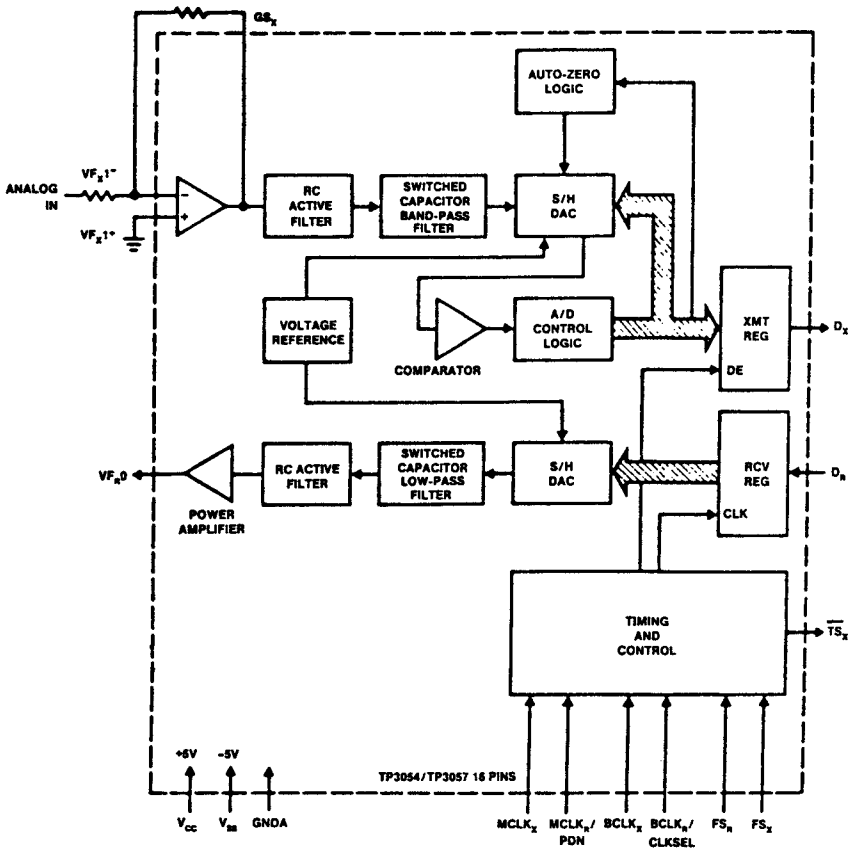
Inputs			Output
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

X = H or L
Z = High Impedance



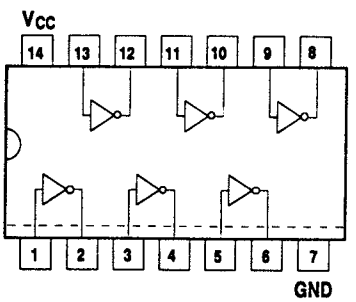
HEX TRI-STATE BUFFER
(74HC365D)

U7



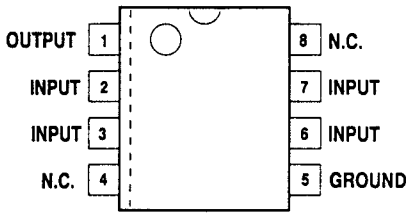
CODER-DECODER (HC3054)

U8



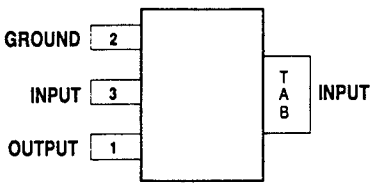
HEX INVERTER 19A703483P4

U10



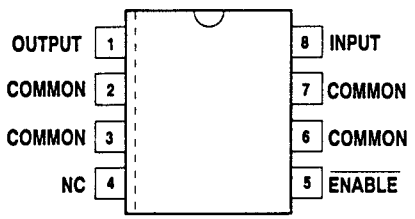
NEGATIVE 5-VOLT REGULATOR
19A704971P4

U11



5-VOLT REGULATOR
(S8125HG-RD)

U12



5-VOLT REGULATOR
344A3404P101