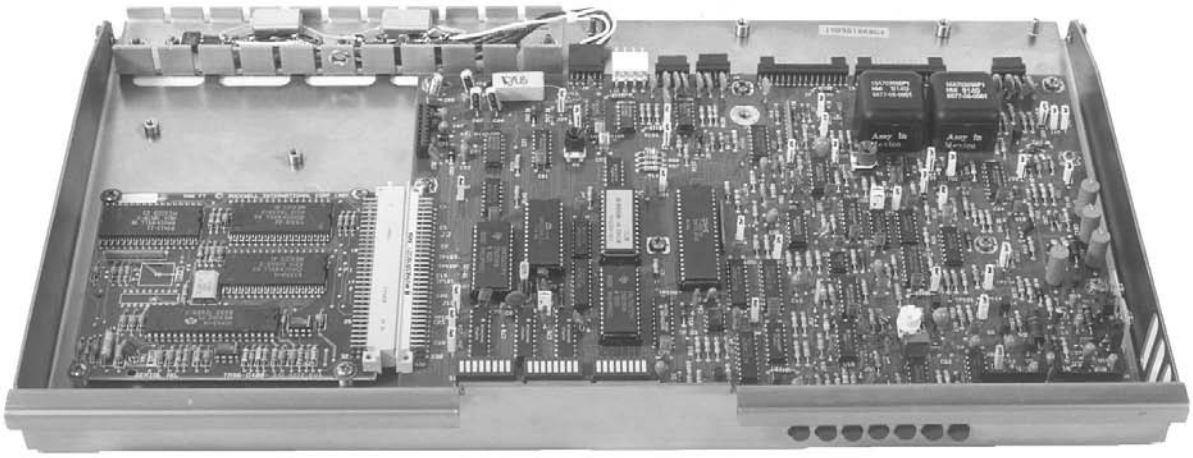
Maintenance Manual

GETC™ TRUNKING CARD

19D901868G3 and G4



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ERICSSON

NOTE

RADIO FREQUENCY INTERFERENCE

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna (i.e., the antenna for radio or television that is "receiving" the interference).
- Increase the separation between the equipment and receiver experiencing the interference.
- Connect the equipment into an outlet on a circuit different from the equipment receiving the interference.

WARNING

No one should be permitted to handle any portion of the equipment that is supplied with high voltage; or to connect any external apparatus to the units while the units are supplied with power. KEEP AWAY FROM LIVE CIRCUITS.

High-level RF energy in the transmitter Power Amplifier assembly can cause RF burns. KEEP AWAY FROM THESE CIRCUITS WHEN THE TRANSMITTER IS ENERGIZED!

NOTICE!

This manual covers Ericsson and General Electric products manufactured and sold by Ericsson Inc.

NOTICE!

Repairs to this equipment should be made only by an authorized service technician or facility designated by the supplier. Any repairs, alterations or substitution of recommended parts made by the user to this equipment not approved by the manufacturer could void the user's authority to operate the equipment in addition to the manufacturer's warranty.

NOTICE!

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SPECIFICATIONS*

ITEM	SPECIFICATION
INPUT VOLTAGE	+13.8 ±20% Vdc
CURRENT DRAIN	
Without 9600 baud modem	900 mA (typical), 1.5 A (maximum)
With 9600 baud modem	1.5 A (typical), 2 A (maximum)
OPERATING TEMPERATURE	-22°F to + 140°F (-30°C to + 60°C)
DIMENSIONS (H x W)	1.75 x 19 inches (4.5 x 48.3 cm)
DATA TRANSMISSION	
High Speed	9600 ±1 bps (EDACS Wideband) 4800 ±1 bps (EDACS Narrow band)
Low Speed	150 ±1 bps
COMMUNICATION INTERFACE	
Site Controller (Trunked)	
Protocol	RS-232C
Data Format	1 start bit, 1 stop bit, and 8 data bits
Data Rate	19.2 kilobaud
Back-up Serial Link (Failsoft)	
Data Levels	0 to 13.8 Vdc swing (nominal)
Data Format	1 start bit, 1 stop bit, and 8/9 data bits
Data Rate	19.2 kilobaud

* These specifications are intended for use during servicing. Refer to the appropriate Specification Sheet for the complete Specification.

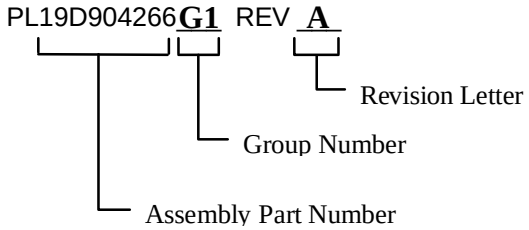
INTRODUCTION

This manual contains maintenance and servicing information for the Ericsson **GE T**runking **C**ard (GETC) Shelf Assembly 19D901868G3 and G4. Currently all production models of the shelf consist of the following subassemblies:

- Shelf 19C851587G1
- Logic Board (A1) .....19D904266G1 or G4
- Regulator Assembly (A2) 19C336816G2
- Turbo Board..... 19D903536G1

IDENTIFICATION

To properly identify the board, locate the "PL" number silk-screened on the logic board. Look for the designation (as shown below) on the left side of the logic board, toward the front of the GETC shelf, and just below the three DIP switches.



Use the Assembly Part Number to determine the applicable maintenance manual. A Revision Letter stamped on the board indicates an improvement or production

change. Refer to the Production Change section (located after the Parts List) for a description of the changes and affected parts.

NOTE

GETCs with the "MODIFIED FOR EUROPEAN OPERATION" label have been modified to be European Technical Standards Institute (ETSI) compliant for adjacent channel power requirements. Refer to the Modifications section of this manual for technical details.

OPTIONS

Depending on the application, the GETC may be equipped with one or more of the following optional boards:

- Rockwell Modem Board 19A705178
- GETC LSD Filter 19C852138P1
- EDACS Voter Interface Board..... 19D438719
- Digital Voice Voting Tone Board 19C336900

In addition to optional boards, the GETC may be equipped with different or modified interface cables. Consult the application LBI whenever maintenance is performed on the GETC.

RELATED PUBLICATIONS

The GETC is used in several applications, which broadly includes voting, **E**nhanced **D**igital **A**ccess **C**ommunications **S**ystems (EDACS™), Aegis, and Digital Voice. In each of these applications the same GETC is used, however, the Logic Board operates differently because of different jumper configurations, interfacing hardware, and software. Refer to the appropriate technical manual for additional information on each application.

LBI-33031 - Rockwell Modem 19A705178 (Model R96FT)

LBI-31981 - Digital Voice Voting Tone Board Maintenance Manual

LBI-38462 - EDACS Voter Interface Board Maintenance Manual

LBI-38822 - Turbo Board (GETC 1e) Maintenance Manual

LBI-38895 - EDACS Terminal-Switch Interface Node (TSIN) GETC Configuration Manual

LBI-38896 - EDACS Site Downlink and CEC/IMC Uplink Configuration Manual

LBI-38954 - EDACS Voter Digital Receiver and Selector GETC Configuration Manual

LBI-38985 - EDACS Site Controller Maintenance Manual

LBI-38986 - GETC Conventional Network Interface (CNI) Configuration Manual

LBI-38987 - EDACS Single Channel Autonomous Trunking (SCAT) GETC and Downlink GETC Configuration Manual

LBI-38988 - EDACS Station GETC Configuration Manual

LBI-38989 - EDACS Test Unit and Alarm Interface (TUAI) GETC Configuration Manual

LBI-39004 - EDACS Guardog Installation and Operation Manual

SRN-1002 - Software Release Notes for GETC 1e Software, 19A149256G( )

SRN-1010 - Software Release Notes for GETC Turbo Board Software (344A4414G1 only)

SRN-1024 - Software Release Notes for GETC 900 MHz Software, 19A705595G( )

SRN-1060 - Software Release Notes for GETC 1e Software, 349A9607G( )

SRN-1061 - Software Release Notes for Link Software, 344A4895G1 (or later) and Link Turbo Software 350A1121G4 (or later).

SRN-1062 - Software Release Notes for GETC Turbo Board Software (344A4414G2 or later)

TQ-3357 - GETC Shelf Programming Manual

DESCRIPTION

The GETC is essentially a processor board with audio filtering and specialized I/O capability. Because of this flexibility in design, the GETC can be integrated into many applications.

The Logic Board, Regulator Board, Turbo Board, and Modem are mounted on a tray and enclosed in a slide-out shelf as shown in Figure 1. The GETC Shelf is a one-rack-unit assembly (1.75-inches x 19-inches) which is mounted in a standard 19-inch wide equipment cabinet.

The GETC Logic Board uses Metal-Oxide Varistors (MOV's) for lightning protection on all RS-232C inputs and outputs. However, maximum lightning protection is achieved when the GETC is grounded to the cabinet earth-ground using the GETC Lightning-Protection Circuitry Grounding Kit 344A4500 and the Cabinet Grounding Strap Kit 344A4730. Specific details for installing these grounding kits are found in the Modifications section of this manual.

FRONT PANEL INDICATORS

The seven front panel LED indicators (L1 thru L7) display the state of operation of the GETC. The interpretation of the indicators depends on the system application (refer to the configuration manual for the specific application).

ROCKWELL MODEM BOARD

The 9600 Baud Rockwell Modem Board, 19A705178, is used in the GETC shelf to generate a fast-train, synchronous, serial data stream suitable for transmission over audio (phone) lines or microwave. The data stream is sent to a full-duplex, four-wire, dedicated 3002 grade telephone line.

Receive and transmit Phone Line Data lines (J6-6,7,8,9,) are two balanced pairs carrying Modem data to and from the station where the data is combined with station (voice) audio and routed to the Remote Line input and Line output.

In addition to the GETC provided transformer isolation and conditioning, the modem provides automatic adaptive signal equalization allowing normal operation using input signal levels from -40 dBm to 0 dBm. The Rockwell Modem demodulates the input signal and the resulting data is transferred using a serial interface between the Rockwell Modem and GETC. The physical connections for the interface are at J3C-22, J11-1, J11-2, and U19-19.

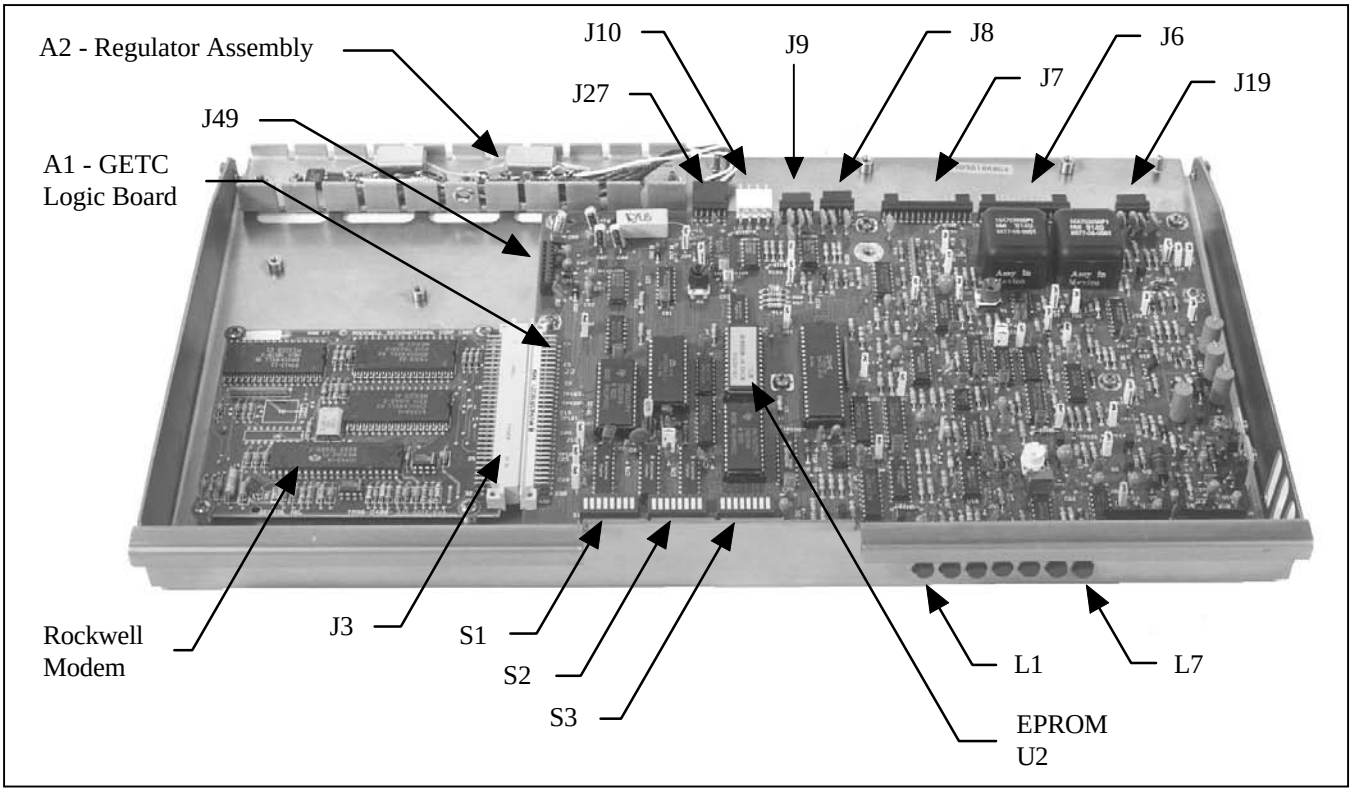


Figure 1 - Basic GETC Shelf Assembly (Turbo Board not shown)

The modem senses a received signal by initiating a training state upon detecting an increase in the input signal level. The modem begins processing data at the end of the training state if the input signal is still above the nominal -40 dBm receiving threshold value. Otherwise, the modem returns to an idle mode at the end of the training state if the input signal is below the nominal receiving threshold value.

The duration of the modem's training state is determined through GETC control signals at the time of power up. Resetting the GETC (pressing S4) or cycling the GETC Shelf's operating power initializes the Rockwell Modem for proper operation.

INTERFACE POINTS

There are ten connectors on the GETC board used for interface connections. These connectors are identified in Table 1.

Table 1 - Interface Connections

Connector	Interface Connection
J3	9600 baud (Rockwell Modem) interface
J27	Regulator board interface
J49	Voting board interface
J10	13.8 Vdc power connection
J9	External modem interface
J8	Site Controller interface
J7	RF station interface
J6	RF station interface
J19	Site Controller interface
XU3	Turbo Board Interface

GETC COMMUNICATION LINKS

The following are communication modes available to the GETC:

(1) The GETC can communicate with other devices such as the Site Controller, IMC, and RF station. Communication occurs primarily through an RS-232C serial interface normally operating at 19.2 kilobaud.

(2) The GETC can communicate with other GETCs, in the Failsoft mode of operation, over a backup serial link (BSL). The link uses 0-13.8 Vdc levels and operates at 19.2 kilobaud and is ordinarily used in a bus configuration.

(3) A timing signal called the Frame Sync Line (FSL) helps arbitrate the use of the BSL serial bus in the Voter configuration. The FSL is also used for timing purposes. In the Station configuration, FSL signals use 0-13 Vdc levels to produce a periodic negative going pulse.

(4) A 9600/4800 baud full-duplex, synchronous communication interface over an RF channel.

(5) A 9600 baud phone line or microwave communication interface through a Rockwell modem.

NOTE

GETC interface functions vary from application to application and between EDACS systems using a MASTR II or MASTR III repeaters. Therefore, it is necessary to refer to the application's configuration manual for details regarding the specific hardware and software configuration of the GETC.

CIRCUIT ANALYSIS

Theory of operation for each circuit card assembly and module used in GETC shelf is described in the following paragraphs. Refer to the schematic diagram 19D904198 and block diagram (Figure 4).

GETC LOGIC BOARD

The logic board contains all GETC functions except the power supply.

Reset Circuitry

The GETC Logic board contains a Power-on/ Manual reset for initializing the programmed code and hardware devices on the board. The reset circuit (Figure 2) consists of a comparator U17B, Zener diode D9, RESET switch S4, driver Q2, and associated circuitry.

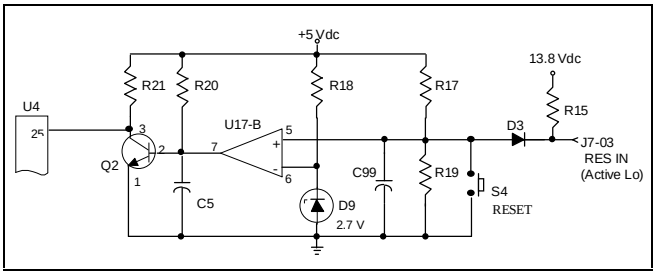


Figure 2 - Reset Circuit

A GETC reset may be initiated in one of four ways:

1. During power-on.
2. By manually pressing S4.
3. By the watchdog timer in U4.
4. By an external device.

During power-on, the comparator U17B compares the +5.0 Vdc line with a reference level to generate a reset to the GETC logic board.

A reference level of 2.7 Vdc is set up on pin 6 of the comparator by Zener diode D9. After power-up, the steady-state level on pin 5 is set to 3.2 volts by the resistor divider (R17 and R19). The output of comparator U17B is pulled up through resistor R20. Normally, Q2 is on and the base-emitter junction clamps U17-7 to +0.8 Vdc.

When the RESET button S4 is pressed, U17-5 goes to ground and the comparator output (U17-7) goes to zero (0) volts (nominal logic 0) turning transistor Q2 off. The collector of Q2 is pulled high by R21, sending a pulse to the reset input (RES IN) of the modem (U4-25). The modem RES OUT line (U4-3) is the logical-OR of the RES IN line and the internal watchdog-timer pulse (if not serviced by microcomputer U1).

The reset out (RES OUT) of the modem is sent to the microcomputer and other logic devices on the GETC logic board. When the RESET button is released, the level on U17-5 returns to +3.2 volts after C99 charges. The comparator output (U17-7) turns off, allowing the base of Q2 to be pulled high (to 0.8 volt) as C5 charges. The time constant set up by R20 and C5, results in a 140 millisecond turn-on delay for Q2. After the reset pulse is gone, the microcomputer restarts operation from program counter address 0.

A reset may occur automatically if the microcomputer fails to service the watchdog timer in modem U4. This reset will occur if the microcomputer misses a service for a two-second period (jumper P62 on J62 pins 1 & 2) or a four-second period (P62 on J62 pins 2 & 3).

A reset may also be generated by an external device, such as the Guardog™ option. The external device resets the GETC by applying a logic low on J7-3, which is diode-coupled (D3) to the comparator. The reset circuit then operates similar to that described for the RESET switch (S4).

Clock Circuitry

The clock drive for the GETC logic board originates in modem U19. The clock oscillator consists of crystal Y1, modem U19, and associated circuitry (see Figure 3). A built-in oscillator circuit within the modem runs at 11.059 MHz as determined by crystal Y1. The CLK 1 line (U19-14) provides clock signals to both microcomputer (U1) and RF data modem (U4).

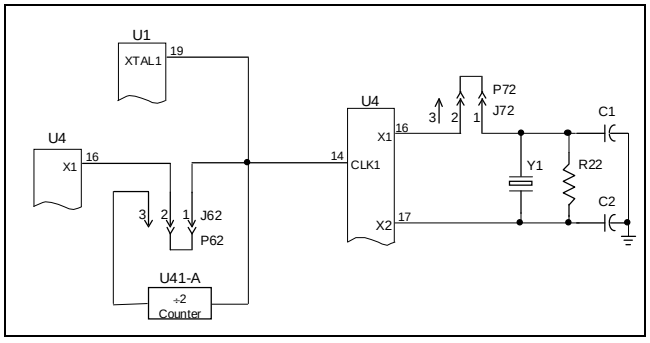


Figure 3 - Clock Circuit

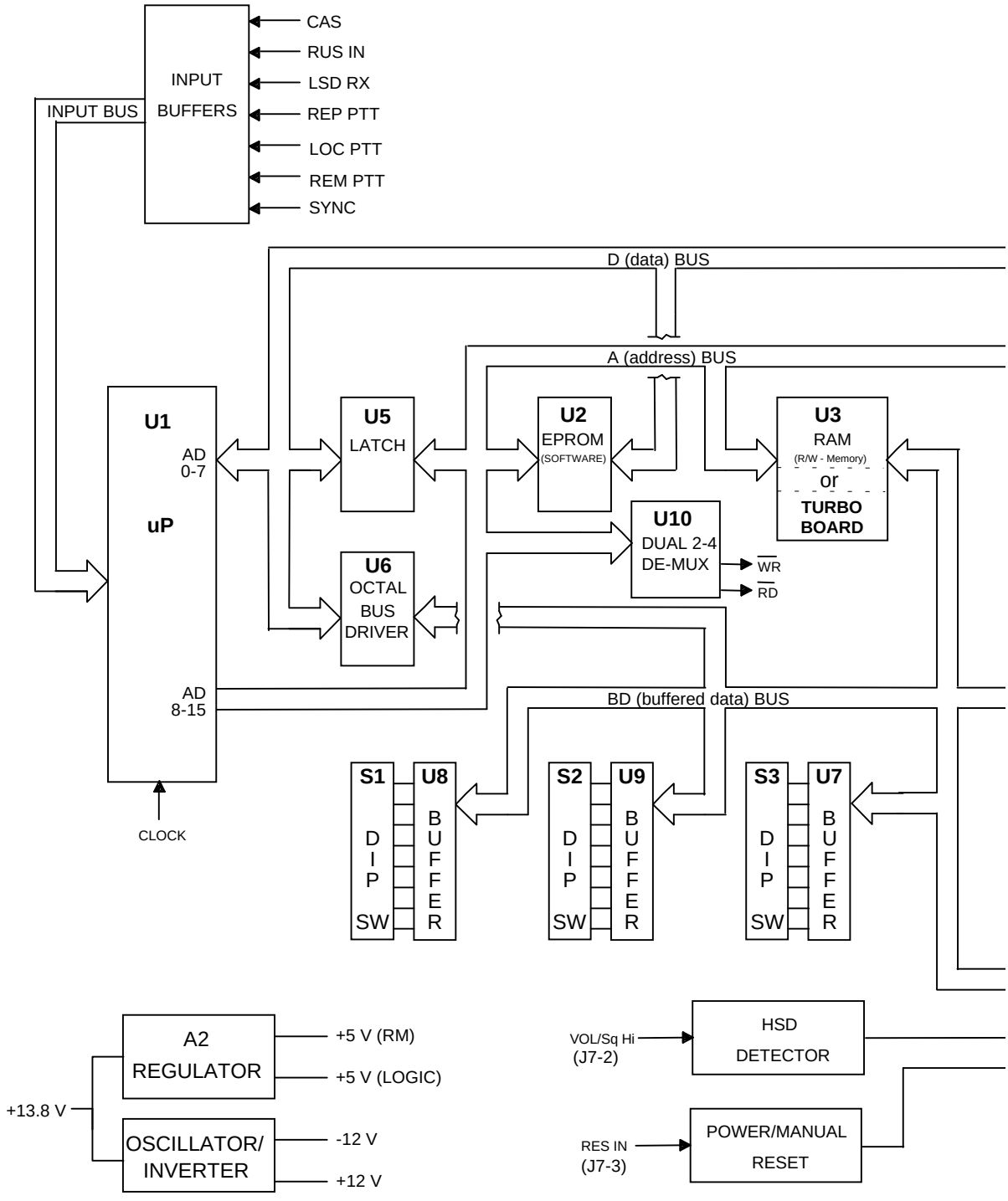


Figure 4A - Simplified GETC Block Diagram

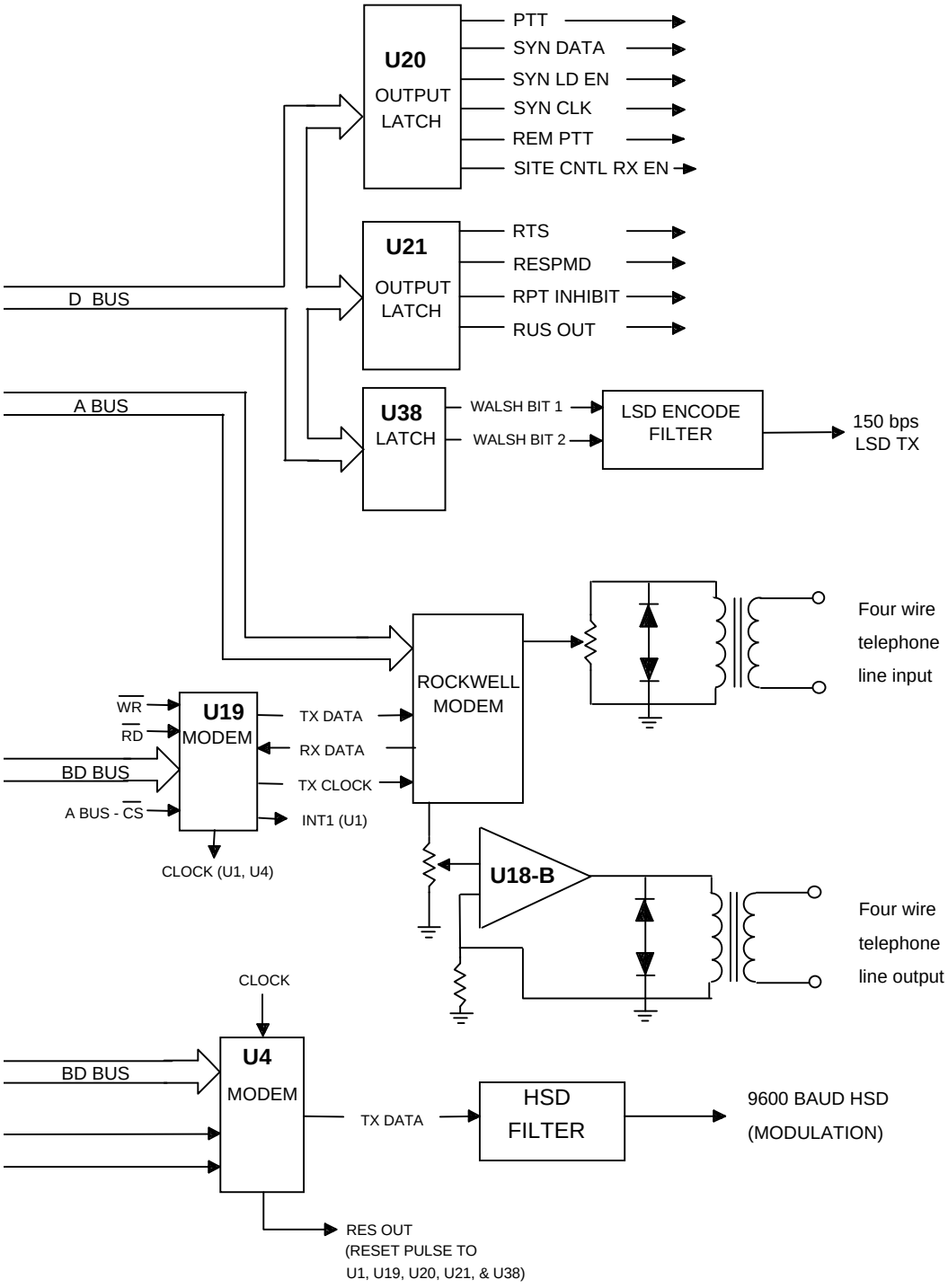


Figure 4B - Simplified GETC Block Diagram

For 9600 baud operation, a jumper P62 is placed on J62 pins 1 & 2. This provides an 11.059 MHz clock signal to drive the RF modem (U4-16). When J62 pins 2 & 3 are jumpered, the divide-by-two counter (U41-A) uses the output from U19 to generate a 5.5296 MHz clock. This clock signal is required to drive the RF modem (U4) for 4800 baud operation. Placing jumper P72 on J72 pins 1 & 2 selects the internal oscillator, on J72 pins 2 & 3 is for slaving to an external oscillator.

Jumper Configuration

There are several jumpers on the GETC logic board used for configuring the GETC for different applications. For the proper jumper settings , always refer to the Software Release Notes covering the specific application and software version.

NOTE

Jumper settings contained in this manual are for bench test and alignment only. Refer to applicable SRN for operational jumper configuration.

Switch Settings

There are three eight-position DIP switches (S1 thru S3) located on the GETC logic board. These switches are used to configure the GETC for different applications. Refer to the Software Release Notes for the specific application when setting the DIP switches. Settings contained in this manual are for test and alignment only.

NOTE

DIP switch settings contained in this manual are for test and alignment only. Refer to applicable SRN for operational DIP switch configuration.

Power Supplies And Regulators

The GETC receives its primary power from the station power supply (13.8 volt nominal) through connector J10-1. Regulated +5.0 volts, +12.0 volts and the -12.0 volts are derived from this source.

Generation of the regulated +5.0 volts is accomplished through the Regulator Assembly (19C336816G2). This assembly (Figure 5) gets 13.8-volt station power through connector J27-4. Regulated +5.0 volts is returned to the GETC logic board devices through J27-6. Regulated +5.0 volts used to power the 9600 baud Rockwell Modem is returned at connector J27-1.

Resistors R1 and R2 are used to lower the voltage across the regulators, reducing their dissipation. Terminal strips TB1 and TB2 serve as interconnect points for the harness (W1) that mates into the GETC logic board (P1/J27).

Regulator U2 is the power source for the GETC logic board devices, while U1 is the power source for the 9600 baud modem board. Ripple filtering for the +5.0 volt regulators is provided on the GETC logic board by capacitors C47 thru C49 and C51 thru C53. Diodes D22 and D23 provide back-bias protection on the +5 volt power regulators.

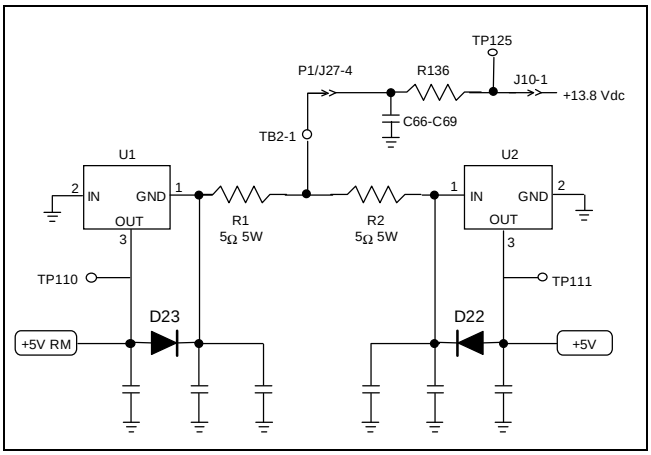


Figure 5 - 5 Volt Regulator Circuit

Regulated +12.0 and -12.0 volts are generated using the oscillator-inverter circuitry. These sources supply power to the analog circuits and RS-232C driver devices on the GETC Logic Board, as well as the 9600 baud Rockwell Modem.

The oscillator-inverter circuit, shown in Figure 6, obtains a 9600 Hz (or 4800 Hz if P62 is on pins J62-2 & 3) square wave input from modem U4-27, which is sent to the base of transistor Q14. Transistor Q14 translates the TTL square wave to a 0 to 13.8 volt square wave. Transistor Q8 and Q9 provide additional buffering to drive Q11 and Q10, respectively. Transistor Q11 and Q10 drive Q12 and Q13 to obtain a push-pull, high-level drive output. CapacitorC56 and diode D28 are used to quickly turn off Q13. The output at the collectors of transistors Q12 and Q13 is a highdrive 9600 Hz (4800 Hz if P62 is on pins J62-2 & 3) square wave which swings from 0 to 13.8 volts. Capacitors C57 thru C60 and diodes D31 thru D34 comprise a negative voltage doubler, which maintains a nominal value of -23 volts to the input of the negative voltage regulator U39. Capacitors C62 and C63, and diodes D29 and D30 comprise a positive voltage doubler, which maintains a nominal value of +25 volts to the input of the

positive voltage regulator U40. Resistor R128 is used as a current limiting resistor to reduce the case temperature of regulator U40.

The two voltage regulator, U39 and U40, reduce the input voltage to obtain a regulated -12.0 volts and a regulated +12.0 volts, respectively. Capacitors C61 and C64 provide additional ripple filtering on the -12.0 and +12.0 volt lines.

Logic

The GETC Logic board provides the station control and interfacing in the system. The main controller on the GETC shelf is the microcomputer (U1) found on the GETC logic board. The microcomputer obtains its instructions from the program stored in PROM U2. The upper eight address lines of the microcomputer (U1) go directly to the PROM, while the lower address lines are latched into register U5. The output of U5 supplies the lower eight address lines to the PROM. The microcomputer accesses the data from the PROM using the control line PSEN (Program Store Enable) on U2-22. An external RAM (U3) holds data and tables. The address lines to the RAM are identical to that of PROM U2.

Microcomputer U1 accesses the modem (U19) to interface to the 9600 baud Modem board or 9600 baud RS-232 link. This provides a remote data interface. Modem U4 provides the high-speed data encode to the transmitter in the station, as well as the high-speed data decode from the station receiver.

Configuration of the GETC is partly determined by the settings of switches S1 thru S3. The microcomputer reads these settings through octal buffers U7 thru U9. Resistor packs R8, R9, and R39 are pull-ups for the switch lines.

The microcomputer accesses data to or from RAM (U3), modem U19, modem U4, and octal buffers U7 thru U9, through octal transceiver U6. Transceiver U6 connects switches and RAM to the BD (buffered data) bus. Data going to or from the PROM, and octal registers U20, U21, and U38 is handled by the D (data) bus.

Program memory is selected by the PSEN(-) strobe (U1-29). Address Latch Enable (ALE) addresses the devices on the A (address) bus by latching the lower eight bits of the address through U5. The upper eight bits of the address are sent directly to the devices. The two-to-four demux/decoder (U10) is used to decode the upper address lines (A11 thru A13). When gated by RD(-) or WR(-), the demux/decoder enables the desired device to transmit or receive data. The devices on the microcomputer bus are addressed according to Table 2.

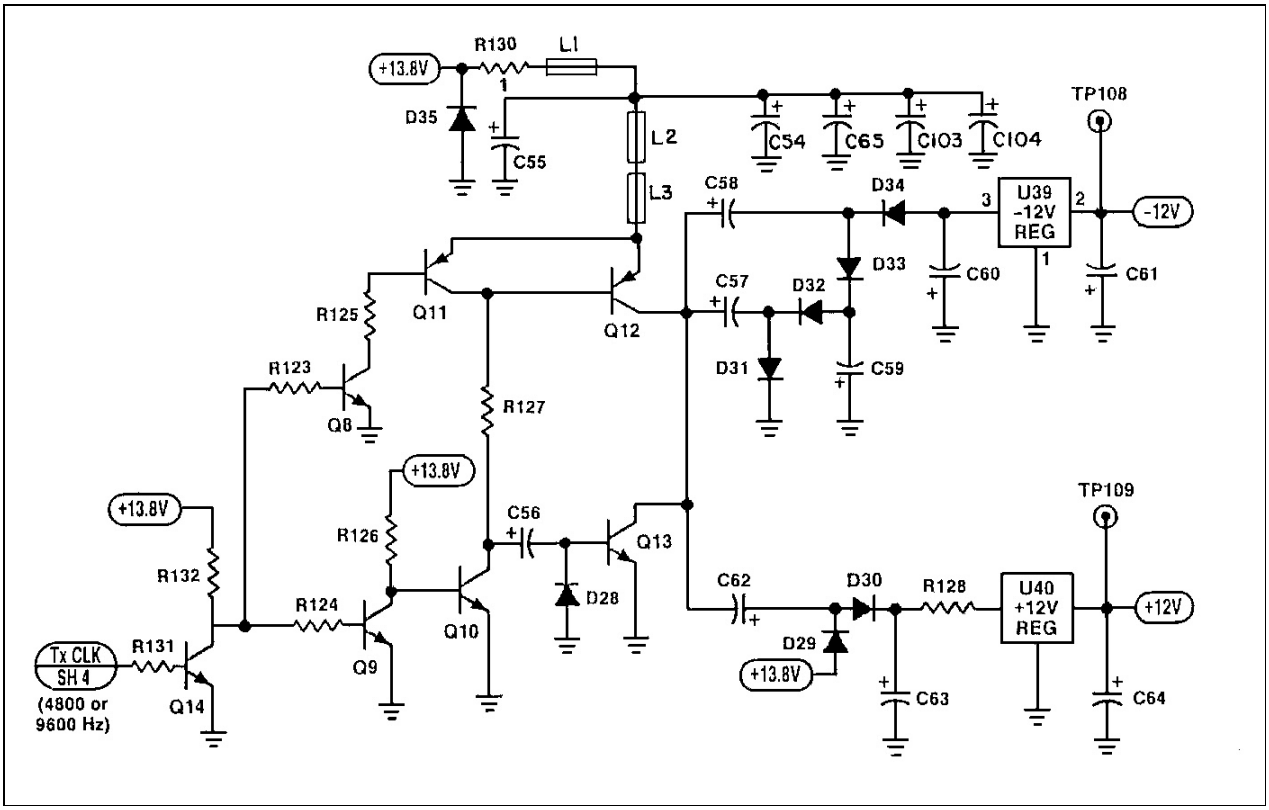


Figure 6 - Oscillator/Inverter Regulated ±12 V Power Supply Circuit

Low-Speed Data Encode Filter

The low-speed-data encode filter (Figure 7) is comprised of U30, U32A, U32D, and associated circuitry. This filter is a low-frequency response filter consisting of a two-stage gyrator section. The filter is used to smooth out the transitions of data which is impressed upon the voice audio. Low-speed data is a 150 bit per second data stream generated by the microcomputer, and used to produce subaudible data on the voice audio.

Low-speed data is generated by the microcomputer on Walsh bit 1 and 2 on octal register U38 (pins 2 and 5). For low-speed data, two Walsh bits are scaled and summed through the analog switch (U34C) to the input of the low-speed-data encode filter. The LSD Tx output of the filter leaves the GETC logic board on J19-5, and goes to transmitter where the filtered data is added to the voice audio. The audio (plus low-speed data) combination comes back to the GETC logic board, where the analog and digital paths are controlled by the microcomputer through switch U15A. The frequency response of the low-speed-data encode filter is shown in Figure 9.

Table 2 - Device Addresses

DEVICE	HEXADECIMAL ADDRESS
U3	0000 - 1FFF
U4	A170 - A172
U7	B800
U8	B000
U9	A800
U19	A0F0 - A0F2
U20	A800
U21	B000
U38	B800
9600 baud modem	A1E7

Low-Speed Data Decode Filter

The low-speed-data-decode voice-reject filter shown in Figure 8 is comprised of U33, U32B, U32C, and associated circuitry. This filter is a low-frequency response filter, consisting of a two-stage gyrator section. The filter is used to reject the voice audio and obtain the low-speed data or subaudible signaling.

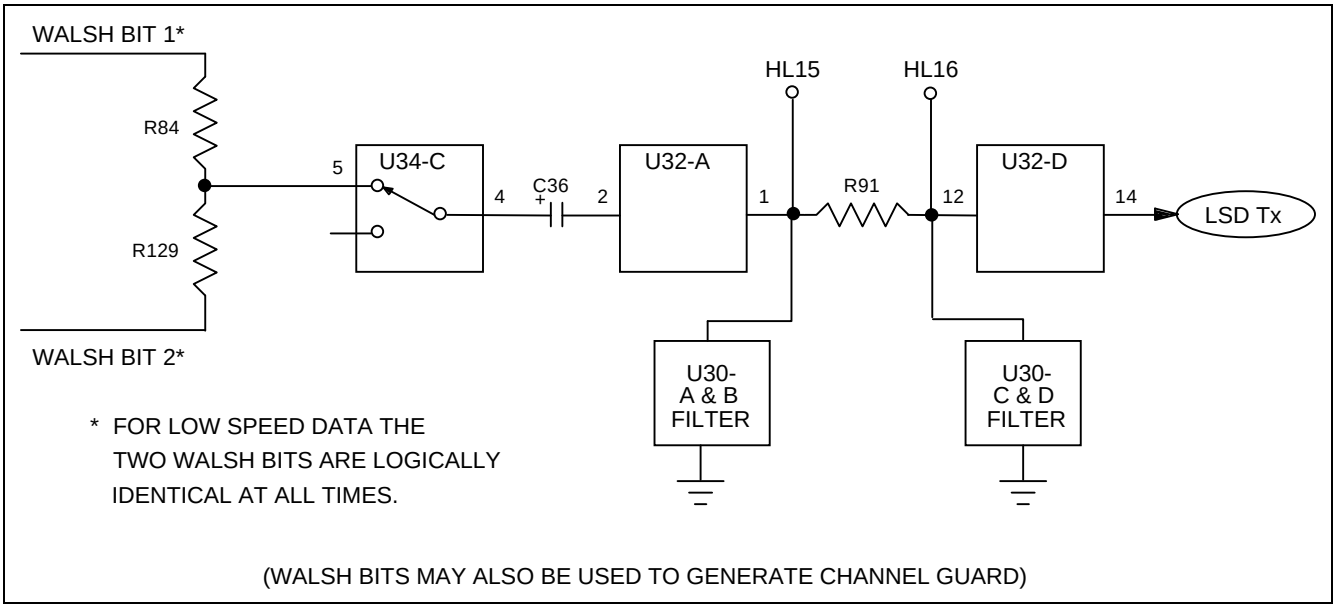


Figure 7 - Low-Speed Data Encode Filter

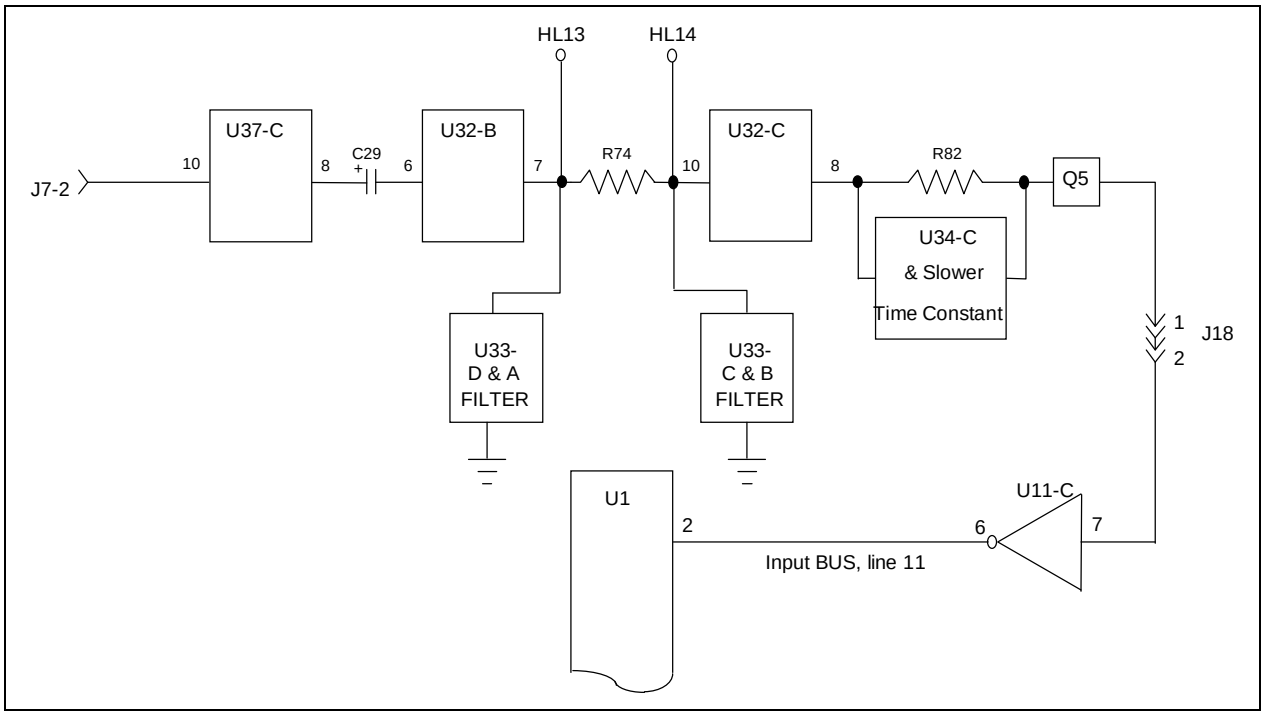


Figure 8 - Low-Speed Data Decode Filter

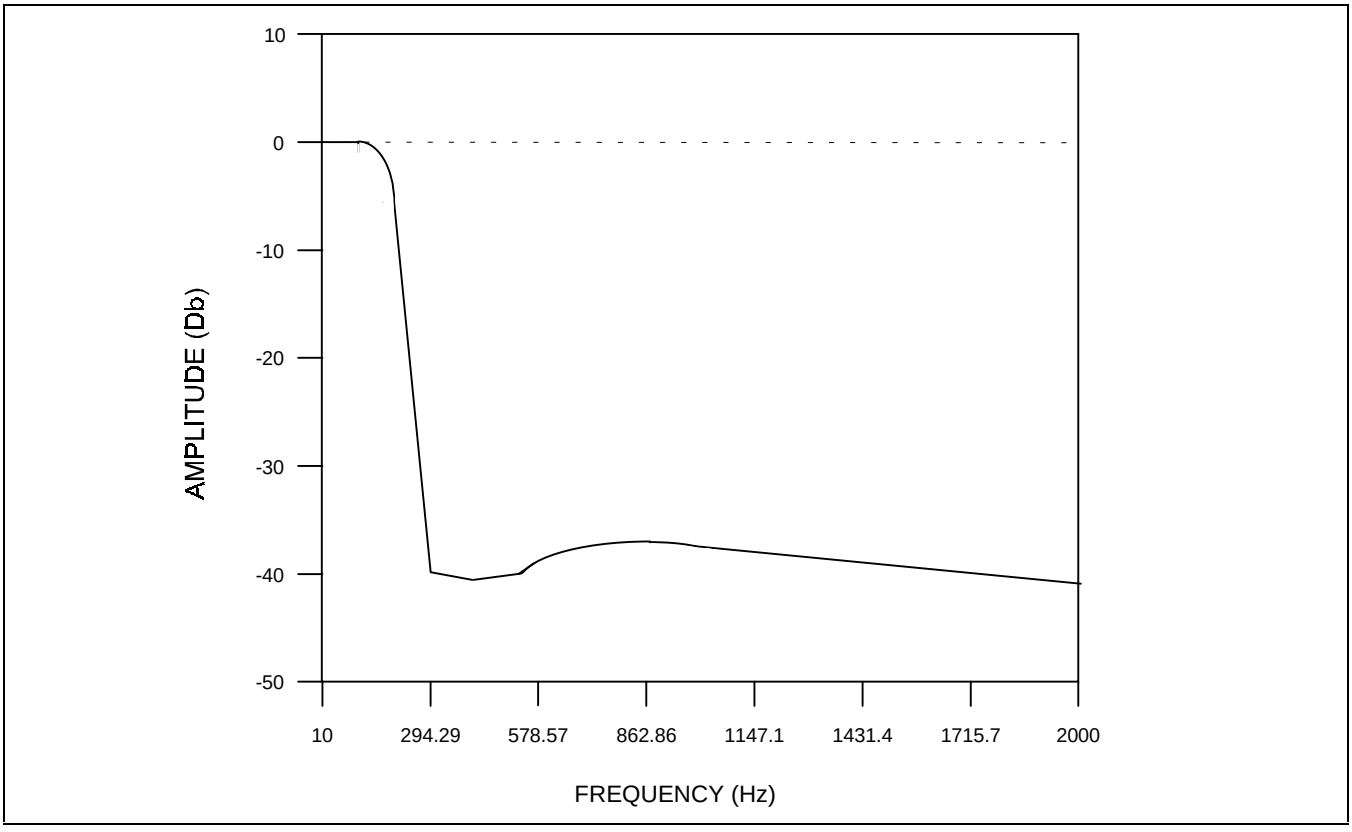


Figure 9 - Low-Speed Data Encode/Decode Filter Response

The station received (demodulated) audio, VOL/SQ HI, is routed to the GETC logic board through connector J7-2. The VOL/SQ HI audio is sent to the voice-reject filter, via U37C, where the voice audio (300-3000 Hz) is attenuated leaving only the low-speed or subaudible data at U32-8.

The low-speed data goes to a limiter consisting of U31A and associated circuitry. Analog switch U34B switches the low-speed data acquisition time constant from a higher rate to a slower rate. The output at U31-1 is a data waveform swinging from -12 volts to about 1 volt. This waveform is converted to a TTL waveform by Q5, and sent to buffer U11-7 and then to the microprocessor. The microcomputer software decodes the low-speed data. The frequency response of the low-speed-data decode filter is shown in Figure 9.

High-Speed-Data Filter

The high-speed-data filter (Figure 10) is comprised of U16 and associated circuitry. High-speed data is a 9600 or 4800 bit per second data stream generated by the microcomputer through the RF data modem (U4).

NOTE

The component values shown in Figure 10 are for standard GETCs. For GETCs modified for European operation, refer to the Modifications section of this manual.

The four sections of U16 serve as the transmit filter and buffer/driver/ Integrated circuit U16A is a voltage follower, and U16B and U16C provide the Bessel (constant-phase) filtering of the high-speed data. High speed data is driven into switch U15A-12 by U16D. (In MII and MIIe systems, audio from the TX synthesizer-exciter board is fed into J7-5 and routed to U15A-13). The MODCNTL signal, controlled by the microprocessor, switches U15A, enabling or disabling the HSD (or audio) sent to the TX modulator.

Variable resistor R31 is used to set the high-speed data deviation in the station. This is the only deviation control on the GETC logic board. The voice and low-speed data deviation is set on the synthesizer-exciter board at the station transmitter.

High-Speed Data Detector

The high-speed-data detector is comprised of U17A and associated circuitry. The received input (VOL/SQ HI) enters the GETC logic board at J7-2. This signal is sent to the data limiter (U17A). The microcomputer controls the acquisition rate of the high-speed-data detector through switch U15C. A low acquisition rate is set when the microcomputer brings U21-16 low, similarly a high on U21-16, sets the rate high. A low on U21-16 causes a high on U15-9.

Low acquisition rate is used if the GETC logic board has locked into mobile/portable transmissions. The high acquisition rate is used if the GETC is looking for mobile/portable transmissions. Speeding up the acquisition rate is achieved by allowing the bias level on U17A to adapt quickly to the DC bias level on the incoming VOL/SQ HI received signal.

Baud Modem Board And Telephone Line Interface

The GETC interfaces to the 9600 baud Rockwell Modem Board through connector J3. Address and control of the 9600 baud modem board is over the A bus (lower seven address lines), the BD bus, and Phone Modem U19. The microcomputer addresses the Rockwell Modem Board to set the modem board timing for external clock, and sends data to the Rockwell Modem Board through U19. When data is to be sent, the microcomputer sends a request to send (RTS) and waits for a clear to send (CTS) from the modem board. The RTS line is sent to the modem board from latch U21-2, and is an active-low TTL signal.

The CTS signal back to the microcomputer is read on U1-15, and is an active-low signal from the modem board. The telephone line transformers T1 and T2, couple the four-wire telephone line to the Rockwell Modem Board.

Transformer T1 receives data from the telephone line and couples the data to the modem board at J3A-32. A voltage follower (U18A) drives the data to the modem board. Resistor R1 is used to adjust the telephone line level to the proper modem reference level. The reference level is 0.16 volts rms at U18-1. Diodes D10 and D11 are used for surge protection.

Transformer T2 transmits data from the modem board to the telephone line. The serial transmit data is obtained from J3C-32, and sent to U18B for coupling to the telephone line. Resistor R2 is used to adjust the telephone line level to the proper transmit reference level. The reference level is usually 0.77 volts rms (0 dBm) across J6-8 and J6-9 (balanced). Diodes D12 and D13 are used for surge protection.

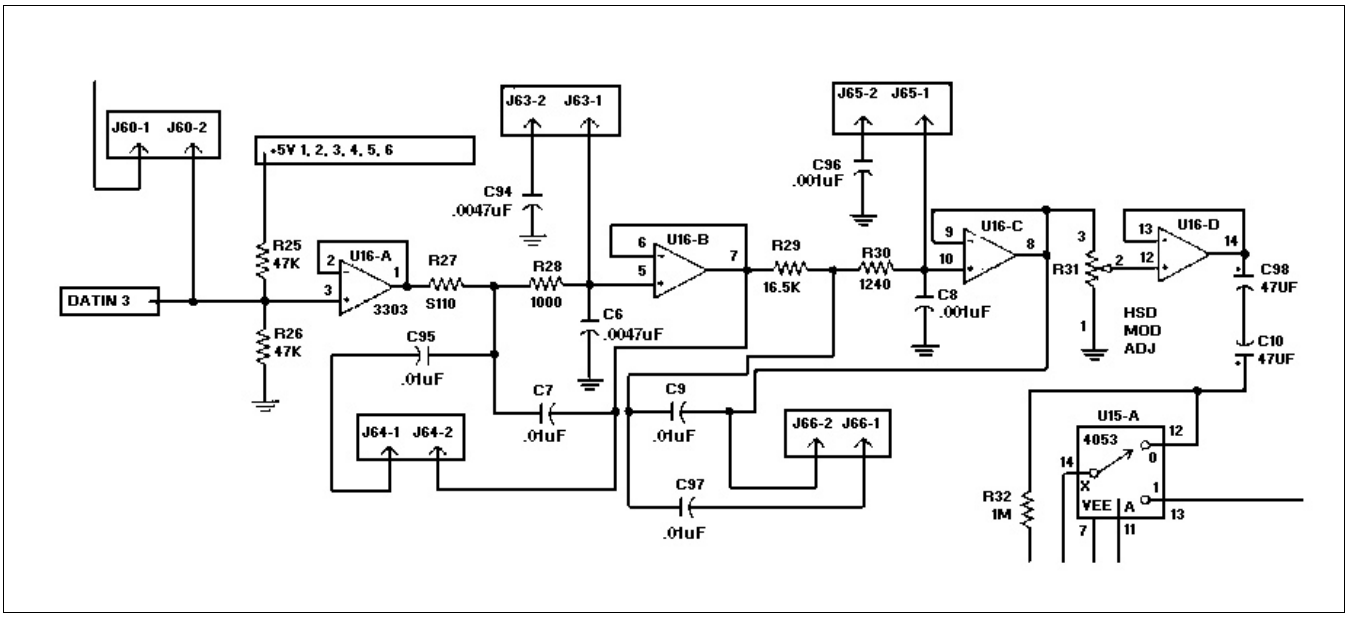


Figure 10 - High Speed Data Filter

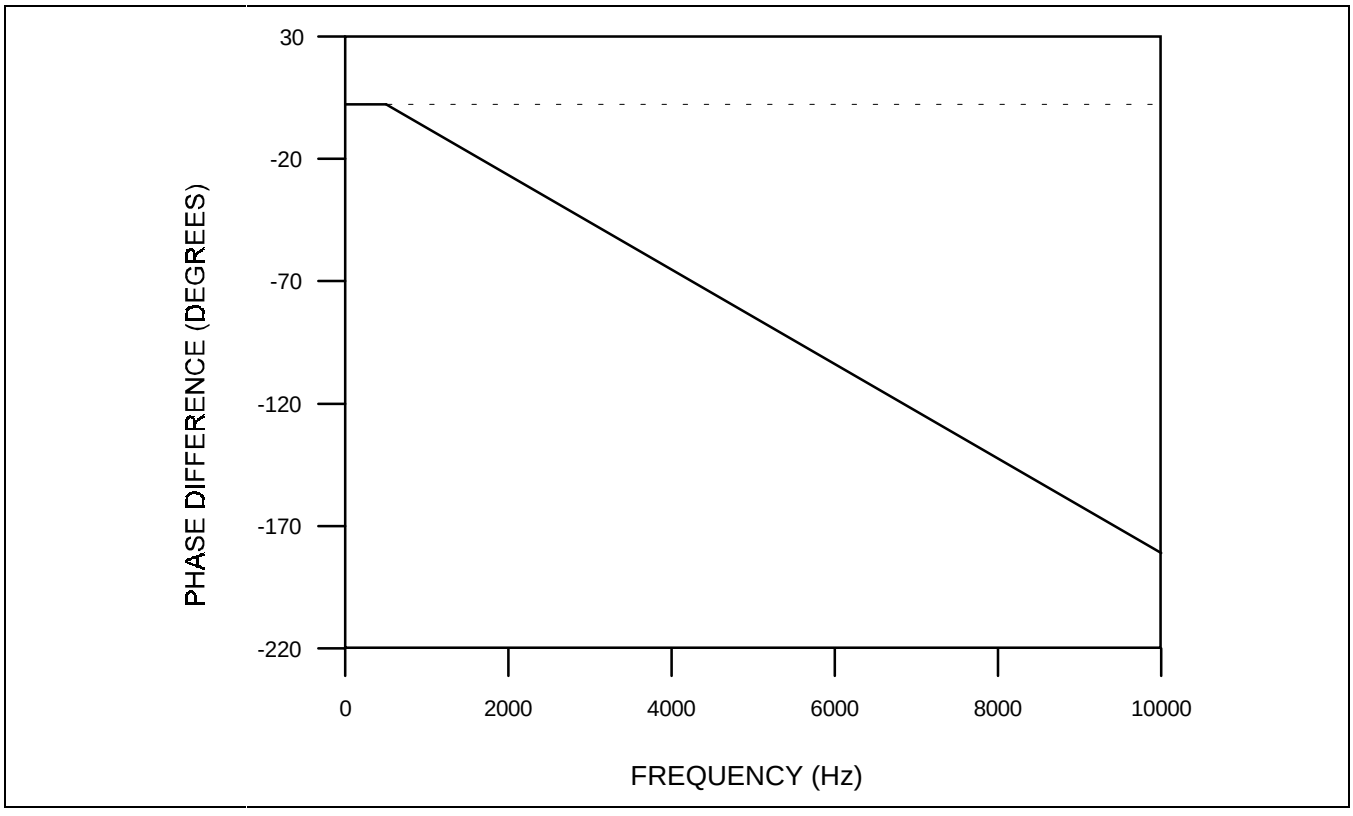


Figure 11 - Typical High-Speed Data Filter Response

INTERFACE

STATION CONTROL INTERFACE

The following lines are available to the GETC for interface to a trunked station:

J6-1	DELAY PTT	Keys the station transmitter.
J6-10	DET DIS	Routes HSD and enables or disables LSD.
J6-11	SYNTH DATA	Synthesizer-exciter data line (MII/IIe only).
J6-12	SYNTH CLK	Synthesizer-exciter clock line (MII/IIe only).
J6-13	SYNTH LCK DET	Synthesizer-exciter lock detect indicator (MII/IIe only).
J6-15	SYNTH LD EN	Synthesizer-exciter load enable pulse line (MII/IIe only).
J6-5	1950 DIS	For EDACS Voting System to enable or disable the 1950 Hz Tone (squelch tone).
J7-13	PA FAIL	RF power amplifier failure sensing line.
J7-15	RUS OUT	Mutes or unmutes receiver audio.
J7-2	VOL\SQ HI	Unfiltered receiver audio including 9600 baud High Speed Data (HSD), voice, and 150 bps Low Speed Data (HSD).
J7-4	MOD OUT (EXT HSD)	Filtered HSD or Digital Voice to be transmitted.
J19-5	CG HI (EXT LSD)	Low Speed Data to be transmitted along with voice.

Synthesizer-Exciter Board Interface

The GETC logic board loads the transmit (800 MHz applications) and transmit/receive (900 MHz applications) frequency information into the station synthesizer(s) (MII/IIe only). The SYNTH DATA (J6-11), SYNTH CLK (J6-12), SYNTH LD EN (J6-15), and SYNTH LCK DET (J6-13) signals are used. The microcomputer loads the frequency code into the synthesizer-exciter board at power-up, reset, or whenever an out-of-lock indication is obtained from the synthesizer-exciter board. The frequency code is generated by the microcomputer based upon the settings of the DIP switches or Personality Programming on the GETC logic board.

A 32-bit pattern consisting of a reference number (R), the synthesizer divide-by-N counter value (N), the synthesizer divide-by-A counter value (A), and a control bit, make up the frequency code. A single 32-bit load is made to the transmit synthesizer in 800 MHz applications. For 900 MHz applications, a 64-bit load is made (32 bits for transmit and 32 bits for receive).

The sequence of entering data into the synthesizer-exciter board is shown below. This sequence is repeated once for the transmitter and once for the receiver in 900 MHz applications.

MSB LSB

R VALUE (14 BITS)	N VALUE (10 BITS)	A VALUE (7 BITS)	CONTROL (1 BIT)

Data Load To Synthesizer-Exciter

The clock, data, and load enable lines (for MII and MIIe only) are initialized to logic 0 at octal register U20. The data is presented on U20-16 (bit 6). After about 40 microseconds, the data is then changed to reflect the next data bit of the synthesizer load. After 32/64 bits have been clocked into the synthesizer-exciter, the load enable line changes states for a 20 millisecond period, and then returns to its previous state. Lock detect is checked at U13-2. If lock is not achieved, then the GETC attempts to reload the synthesizer-exciter board until a lock-detect is established.

The data, clock, and load enable lines are inverted as they leave the GETC and become SYNTH DATA (J6-11), SYNTH CLK (J6-12), and SYNTH LD EN (J6-15). The open-collector drivers on the GETC (U23A-2, U23B-4, and U23F-12) drive the SYNTH DATA, SYNTH CLOCK, and SYNTH LD EN lines to the synthesizer-exciter board over a bus which includes a pull-up to 7.6 volts. The SYNTH LCK DET (J6-13) line is a high (low for 900 MHz) for a positive lock-detect indication. This signal arrives at U13-3 which inverts the logic level so that the microcomputer detects a lock-detect indication by a logic 0 (1 for 900 MHz) on U13-2.

Station Control Interface

The microcomputer on the GETC logic board controls a MASTR II, IIe, or III station operation using the following control and interface lines:

The **SYNTH DATA**, **SYNTH CLK**, **SYNTH LD EN** and **SYNTH LCK DET** lines enable the microcomputer to load the frequency code to the synthesizer-exciter board (MII or IIe only).

The **DELAY PTT** line (J6-1) enables the microcomputer to turn on the station transmitter by pulling J6-1 low (logic high on U20-19). The station transmitter is turned on to 90% of full power in less than 10 milliseconds.

The **RUS OUT** line (J7-15) disables the voice audio from the transmitter (0 volts on J7-15 or logic high on U21-6). The line is grounded when High Speed Data is being transmitted, no "on channel" carrier is being received, or in the absence of received Low Speed Data. This stops the receiver from routing audio (vol/sq) to the transmitter and the Line output (using RUS_MUTE and STOP RUS_PTT). This signal is gated directly back to the station from Sys RUS Out but the GETC can control it. In MASTR II (IIe) systems, the MODULATION line is the direct FM signal from the GETC to the synthesizer-exciter board.

The **VOL/SQ HI** input line (J7-2) carries unfiltered receiver audio. This includes 9600 BAUD data, Voice and Low Speed Data. Once in the GETC, this signal is routed to the RF Data Modem U4 where it detects High Speed Data and to the Low Speed Data Decode Filter where it separates the audio from the Low Speed data. The High speed data received can be control signaling or digital voice (encrypted or not). Low speed data indicates valid channel activity.

The **LSD TX** line (J19-5) routes the Low Speed Data to the transmitter for transmission along with voice (from the receiver or the Line input). Low speed data goes into the station and through the channel guard pot and to the transmitter. The Low speed data from the GETC is transmitted to accompany voice as an indicator of valid channel activity or to pass on priority scan information.

The **PA FAIL** line (J7-13) is normally high when the RF transmitter is keyed. Low power output or too much reflected power will cause the line to go low. The line is always low when the transmitter is off.

The **RUS IN** line (J7-14) is set high (+5 Vdc) when the receiver unsquelched by an "on channel" carrier. It is reporting carrier activity. It is low when the receiver is squelched.

The **REP**EAT **PTT** (J7-7) line is high (+5 Vdc) when the MASTR III Receiver Synthesizer is locked. When the Receiver Synthesizer is unlocked for 200 mS, the station grounds this line indicating a fault status to the GETC.

The **1950 DISABLE OUT (RPT INHIBIT)** line (J6-5) is only used in an EDACS voting system. In a voting system, when this line is high (+5 Vdc) it mutes the 1950 Hz tone (squelch tone) which is on the Line output in the absence of a clear voice, working channel call. The 1950 Hz tone will however, remain active during digital voice calls such as AEGIS or Voice Guard.

The **REM PTT** line (J7-9) is grounded when the station decodes a 2175 Hz Secur-it tone on the Line input. This signal alerts the GETC to the presence of a call from a remote source (CEC/IMC) for the duration of the 2175 hold tone

The **DELAY PTT** line (J6-1) is pulled low when the GETC wants to key the station for any reason

The **REM PTT** line (J6-16) is connected to the same line as the System Module's REM PTT switch. When the GETC grounds this line, the station executes a Rem PTT which is a higher priority than the Delayed PTT (EXT PTT). This will route audio from the Line input and will key the station if it is not already transmitting.

The **DETECT DISABLE** line (J6-10) is connected to the Modulation Control line (U25D-9) for MIII EDACS. This line is high (+5 Vdc) when High Speed Data is being routed to the transmitter (see EXT HSD) and Low Speed Data is disabled. When this line is high, the transmitter EXT HSD is set forcing the System Module to use High Speed Data regardless of the state of the EDACS system. When this line is grounded, High Speed Data is not routed and Low Speed Data is enabled.

The **EXT HSD** (J7-4) is the High Speed Data sent to the transmitter. A low MODCNTL signal (U25D-8) switches U15A (pin 12 to 14) routing filtered High Speed Data. This audio is not filtered at all in the MASTR III. The High Speed Data can be high speed control signaling or digital voice (encrypted or not).

SITE CONTROLLER INTERFACE

The GETC uses the following lines to communicate with the Site Controller:

SITE CNTRL TX 1	RS-232C transmit line to the master site controller.
SITE CNTRL RX 1	RS-232C receive line from the master site controller.
SITE CNTRL TX 2	RS-232C transmit line to the backup site controller.

SITE CNTRL RX 2	RS-232C receive line from the backup site controller.

The GETC communicates with the Site Controller (both the master and the backup Site Controllers) through the RS-232C communication ports (see Table 3). The characteristics of the communication link are given below:

TYPE	RS-232C
Baud rate	19.2 kilobaud
Start bit	1
Stop bit	1
Data bits	8
Parity	None
Data Type	Binary

The GETC communicates to the master and backup Site Controllers through U14B, U27C, U28B and U27D. The serial transmit data (TXD) from the microcomputer (U1-11) is sent to the RS-232C drivers (U14B and U28B). The TX output (U14B-6) to the primary controller leaves the logic board at J8-1, and the output to the backup controller (U28-6) leaves the board at J19-1. The serial receive data from the master Site Controller, enters the logic board at J8-2 and goes to the RS-232C receiver (U27C-10). The serial receive data from the backup Site Controller, enters the logic board at J19-2 and goes to the RS-232C receiver (U27D-13). The output of the master Site Controller receiver (U27C-8) is OR-tied with the output of the backup Site Controller receiver (U27-11). This common output is sent to the analog switch (U15B-1). The output of the analog switch (U15B-15) is sent to the receive data input (RXD) of the microcomputer (U1-10). The other input to the analog switch is derived from the backup serial link, and sent to U15-2. The microcomputer selects which path to route over to the RXD input (U1-10).

The decoding scheme used by the microcomputer to select the serial path to be routed to the RXD input (U1-10) is given in Table 3.

A high on U20-2 will turn on the open-collector driver (U25-12) and pull the control line (U27-9) to ground, disabling the output line (U27-8). A logic high on U38-12 will turn on the open-collector transistor (Q15), and pull the control line (U27-12) to ground, disabling output line U27-11. If either of the control lines, U27-9 or U27-12, are left floating, the appropriate device driver output will be enabled.

The signal at U20-15 is inverted by the open-collector driver (U23D) and sent to analog switch U15B. If the control line U15-10 is grounded, the path selected is the backup serial link.

Table 3 - Decoding Scheme

LOGIC LEVEL			SIGNAL TO U15-5	PATH SELECTED
U20-2 (11/73-1)	U38-12 (11/73-2)	U20-15 (FAILSOFT EN)		
O	1	0	U27C-8	Master Site Controller
1	0	0	U27D-11	Backup Site Controller
X	X	1	U29A-2	Backup Serial Link

GETC INTERFACE

The GETC uses the following lines to communicate with other GETC's during Failsoft operation:

BACKUP TX LINK	Backup serial link, transmit output.
BACKUP RX LINK	Backup serial link, received input.
SYNC	Provides working channel-to-control channel data synchronization in trunked stations.

Failsoft mode of operation is selected by the microcomputer (via analog switch U15B) by grounding the control line U15-10. This happens by setting U20-15 high.

Communication between GETCs along the Backup Serial Link (BSL) takes the place through J8-5 and J8-6. The characteristics of the communication link are given below:

Level	0 to 13.8 volts (nominal)
Mark/Space	13.8 volts (mark)/0 volts (space)
Baud rate	19.2 kilobaud
Start bit	1
Stop bit	1
Data bits	8/9
Parity	None
Data type	Binary

PERSONALITY PROGRAMMING

A *personality* is simply a computer file generated (created) by the user. The computer file (or personality) is downloaded into the GETC and contains data that will direct certain operating characteristics of the GETC unit. This allows each GETC to be programmed as required to meet the criteria of the application. The GETC's Personality includes system configuration information such as channel frequencies, call parameters, operating modes, and identification information.

The Personality Programming process stores data in a non-volatile region of memory. The Lightning GETC's non-volatile memory consists of an EEPROM installed in the XU35 socket. For applications using the Turbo Board, Personality data is stored in the Turbo Board's battery backed memory instead of the Lightning GETC's U35 EEPROM.

The following equipment is required when programming the GETC's Personality:

- IBM PC/XT/AT/286/386/486 or any true compatible with MS-DOS version 3.3 or later, and having the following minimum configuration:
  1. Two Disk Drives, a single floppy with fixed (hard) disk drive system.
  2. 640K Internal RAM.
  3. One Serial Port.
  4. One Parallel Port for connection to a printer (optional, but recommended).
- Serial Programming Cable (TQ-3360).
- Programming Software (TQ-3357).
- Printer (optional, but recommended).

The PC reads the Personality information from the computer file on the PC and serially transfers the Personality information through an RS-232 cable to the GETC. The TQ-3360, RS-232 cable, is connected between the computer and GETC connector J100 or J104 depending on the software version and the GETC configuration.

COMPUTER HOOK-UP

Follow the instructions in the TQ-3357 Programming Manual to set up and install the programming software into the personal computer. The GETC PC Programming Software communicates with the GETC through a serial port on the computer.

Connect the TQ-3360 programming cable between the PC's COM1 or COM2 connector and the GETC Shelf J100. Use a DB-25 to DB-9 adapter if required. Essentially, this configuration connects the PC to J8 of the GETC through cable TQ-3360 and harness 19C336863G1.

If the GETC is equipped with a Turbo Board and you are using TQ-3357 version 4 (or later), we recommend

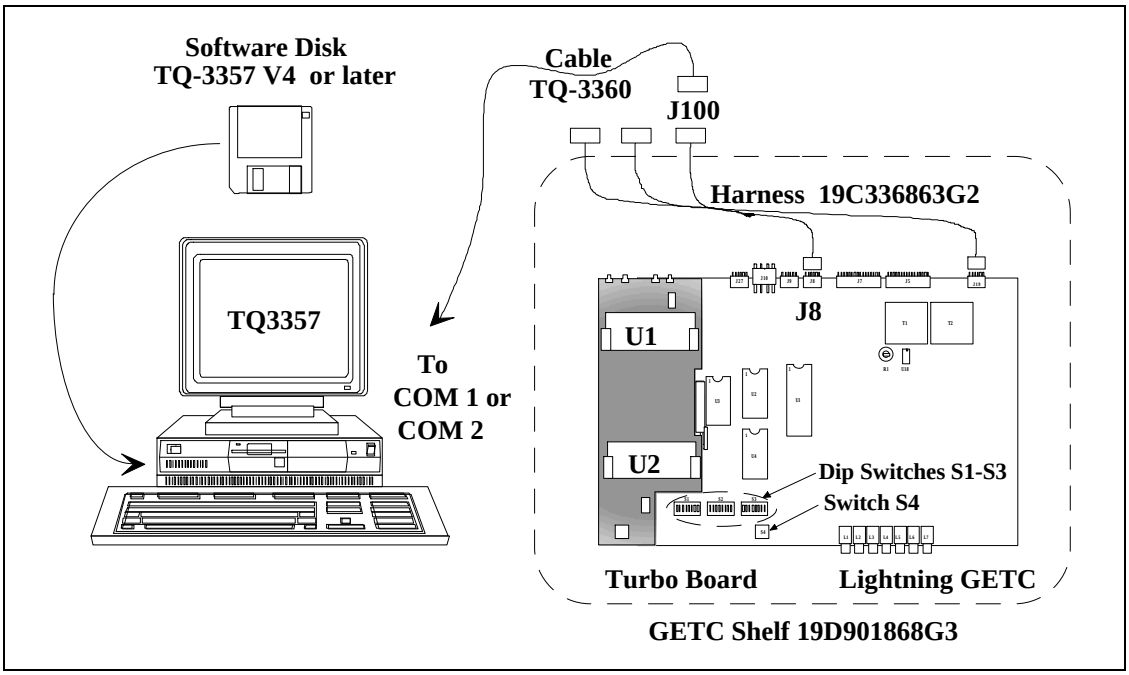


Figure 12 - System Hook-Up Using J100

programming the Personality through J104. The TQ-3357 version 4 enables you to upload the GETC's Personality, without changing the DIP switch settings, and upgrade the Turbo Board's software.

Programming a Personality Through J100

Use the following procedures when programming the GETC Personality through J100. Refer to TQ-3357 for specific programming details.

1. One end of the serial programming cable (TQ-3360) should be connected to the computer. The other end of the serial cable connects to the GETC Shelf connector J100, see Figure 12.
2. Set the GETC DIP switches S1, S2, and S3 for the programming mode as shown in Figure 13. DIP switches S1-S3 are located near the front of the GETC Shelf, see Figure 12.

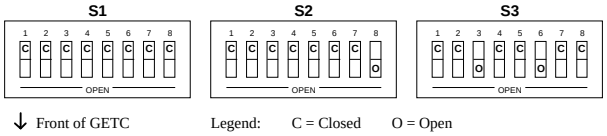


Figure 13 - DIP Switch Settings

3. Reset the GETC by either applying power or pressing the GETC RESET switch S4, located just below the DIP switches. See Figure 12. Resetting the GETC, in combination with the DIP switch settings, places the GETC into the Personality Programming mode.
4. Verify that front panel LEDs L3, L4, and L5 are ON, as shown in Table 4. This indicates the GETC is ready for programming.

Table 4 - Indicators in Programming Mode

LED Indicators	L1	L2	L3	L4	L5	L6	L7
Programming Mode	❍	❍	●	●	●	❍	❍

Legend: ❍ = OFF ● = ON ❇ = FLASHING

5. Proceed with the Personality programming as described in TQ-3357.

NOTE

When programming CNI or SCAT stations, all LEDs are off.

Programming a Personality Through J104

1. One end of the serial programming cable (TQ-3360) should be connected to the computer. The other end of the serial cable connects to the GETC Shelf connector J104. See Figure 14.

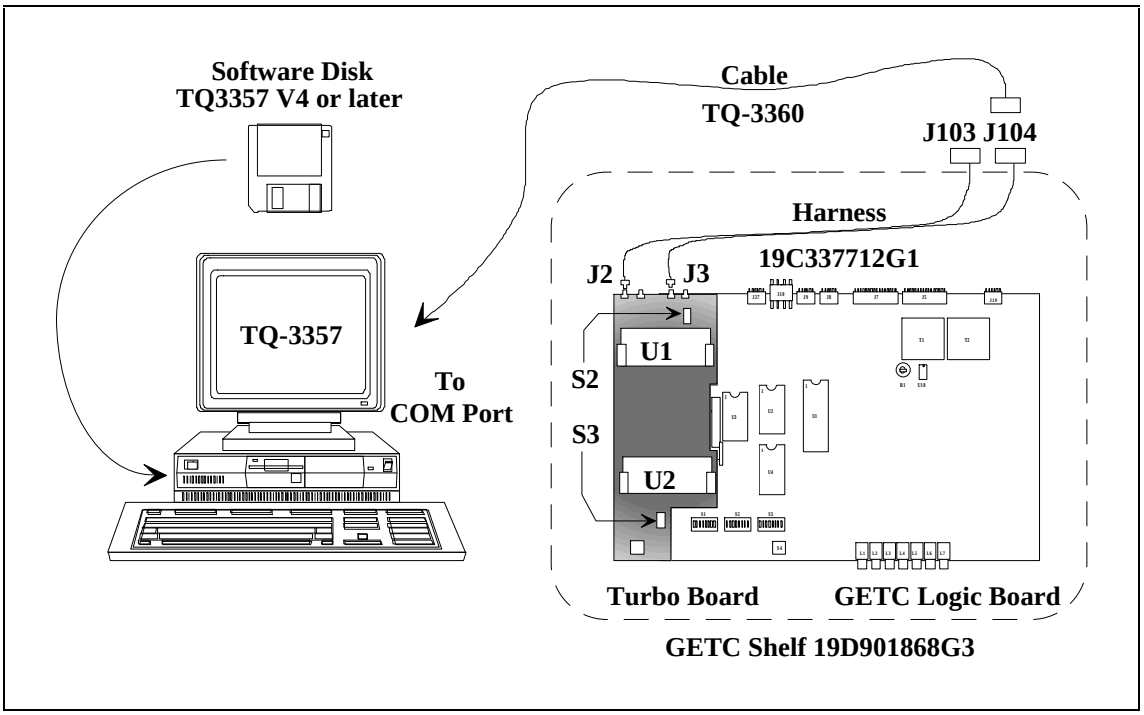


Figure 14 - System Hook-Up Using J104

2. Move Switch S2 on the Turbo Board to the front placing the GETC into the Personality Programming mode. See Figure 14.

3. Verify that front panel LEDs L6 and L7 are flashing, as shown in Table 5. This indicates the GETC is ready for programming.

Table 5 - Indicators in Programming Mode

LED Indicators	L1	L2	L3	L4	L5	L6	L7
Programming Mode	❍	❍	❍	❍	❍	❇	❇

Legend: ❍ = OFF ● = ON ❇ = FLASHING

4. Proceed with the Personality programming as described in TQ-3357.

NOTE

LEDs only flash when GETC has 349A9607G4 (station) or 344A4895G4 (link) software installed.

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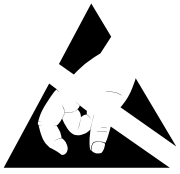
MAINTENANCE

The Maintenance Section provides procedures for maintaining the GETC and for the removal and reinstallation of defective subassemblies.

SUBASSEMBLY REMOVAL AND REPLACEMENT

The following procedures provide step-by-step instructions for the removal and reinstallation of GETC subassemblies.

CAUTION



Observe precautions for handling **ELECTROSTATIC SENSITIVE DEVICES**

WARNING

Before attempting to remove any subassembly, disconnect all power from the GETC.

Turbo Board

This procedure details the steps for removing and installing the Turbo Board. Additional maintenance information regarding the Turbo Board assembly may be found in LBI-38822.

Remove:

1. Disconnect the ribbon cable from the GETC Logic Board XU3 socket.
2. Disconnect the Turbo Board harness (19C337712) from the Turbo Board connectors J2 and J3.
3. Remove the Turbo Board guard (secured by three flat head screws).
4. Remove the three threaded inserts and the two pan head screws securing the board. The board may now be removed from the GETC.

Install:

1. Reinstall the Turbo Board using the following procedure. Refer to the Installation Diagram (19D438125) in LBI-38822 for parts identification.
2. Align the Turbo Board holes over the threaded spacers (orient the Turbo Board so connectors J2 and J3 are toward the rear of the GETC Shelf).
3. Secure the Turbo Board by installing two (2) pan head screws (item #6) and two (2) lock washers (item #7) through the board and into the threaded inserts located near the front of the GETC Shelf (near S1 and Y1).
4. Install three threaded inserts (item #3) through the board into the remaining spacers. These will be used to mount the guard.
5. Install the guard (item #1) using three (3) flat head screws (item #4).
6. Plug the ribbon cable from J1 on the Turbo Board into the XU3 socket on the GETC Logic Board.
7. Connect plugs P2 and P3 on the Turbo Board Harness (19C337712G1) to the Turbo Board J2 and J3 connectors, respectively.
8. Reprogram the Turbo Board and GETC Personality as required.

Rockwell Modem

This procedure details the steps for removing and reinstalling the Rockwell Modem.

Remove:

1. Remove the Turbo Board if installed.
2. Remove the four screws securing the modem. If the GETC has a Turbo Board, remove two threaded inserts and two screws.
3. Slide the modem out of Logic Board connector J3 and lift out of GETC.

Install:

1. Insert the Rockwell Modem into J3 on the GETC Logic Board and align the mounting holes over the GETC shelf standoffs.

   Isolate the modem by installing the eight (8) fiber washers (4035306P25). Insert four washers between the board and the GETC shelf mounting standoffs and place four washers on top of the modem board over the mounting holes.

NOTE

Ensure the modem is insulated from its mounting standoffs using the eight 4035306P25 washers. Four washers mount on top of the modem's printed circuit board and four washers mount on the bottom between the modem's printed circuit board and the GETC shelf standoffs.

3. Secure the modem by installing two screws through the washers and modem board into the standoffs located on the end opposite J3.
4. On the connector side (J3) of the modem, install the two (2) threaded inserts when also installing the Turbo Board or two screws to complete the modem installation.
5. Install the Turbo Board if previously removed.

Power Supply, A2

This procedure details the steps for removing and reinstalling the GETC Power Supply, A2.

Remove:

1. Unplug the Power Supply cable A2W1P1 from the GETC Logic Board connector A1J27.
2. Remove the Power Supply mounting hardware (nut and lockwasher) securing the Power Supply to the shelf (3 places).
3. Lift the Power Supply out of the GETC.

Install:

1. Mount the Power Supply in the GETC shelf as shown in Assembly Diagram 19D901868G3.
2. Secure the assembly using the three #6 nuts and lock washers.
3. Plug the Power Supply Cable A2W1P1 into the GETC Logic Board connector A1J27.

Logic Board, A1

This procedure details the steps for removing and reinstalling the GETC Logic Board, A1.

Remove:

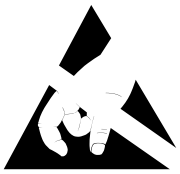
1. Disconnect the cables from the Logic Board connectors J19, J6, J7, J8, J9, J10, and J27.
2. Remove the Turbo Board if installed.
3. Remove the Rockwell Modem if installed.
4. Disconnect the cable from J49 if installed.
5. Remove the eleven pan head screws securing the Logic Board to the GETC shelf.
6. The Logic Board may now be removed from the shelf.

Install:

1. Mount the Logic Board in the GETC shelf as shown in Assembly Diagram 19D901868G3.
2. Secure the board to the shelf using the eleven mounting screws.
3. Reconnect the cable to J49 if applicable.
4. Install the Rockwell Modem if removed.
5. Install the Turbo Board if removed.
6. Reconnect the cables to the Logic Board connectors J19, J6, J7, J8, J9, J10, and J27.

TEST AND ALIGNMENT

CAUTION



Observe precautions for handling **ELECTROSTATIC SENSITIVE DEVICES**

GETC TESTING

The test procedures use the SIMON Test program and simulate the operation of a GETC configured for use in an EDACS Station.

Test Equipment Required

The equipment necessary for the test is listed below. This is a list of suggested equipment only. Substitutions may be made as necessary. Equivalent test equipment means you may use equipment that performs an equivalent function as required in the test. For example, the frequency counter substituted for a Fluke-1920A need only cover the required frequency range and provide the proper resolution for the test - it does not need to be equivalent to the 1920A in all aspects.

1. DC Power Supply with current limiting, HP-6286A (or equivalent), capable of producing 13.8 Vdc @ 2A.

2 Digital Multimeter, Data Technology Model 30 (or equivalent) with 20 Vdc range.

3. Oscilloscope, Tektronix-465 (or equivalent) medium bandwidth, non-storage.

4. Frequency Counter, Fluke-1920A (or equivalent) capable of measuring 12 MHz.

5. Function Generator, HP-3312A (or equivalent), capable of producing a 0 to 10 kHz sine wave.

6. Distortion Analyzer, HP-334A (or equivalent).

7. Triplett Model 630-PL Type 5 (or equivalent) AC Volt-Ohm Meter.

8. ASCII Terminal or Personal Computer (PC) with terminal emulation program.

9. Interconnecting Cable (PC to GETC) (see Terminal Connection, step 2, for fabrication details).

10. SIMON Test PROM, 349A9607G2 (see Software Requirements for details).

11. Miscellaneous materials:

    - Jumpers 19A702104P2, 2-pin. Normally supplied as part of 344A3450G9 Hardware Kit.
    - Capacitor, coupling, 10 μF.
    - Resistor, 100 ohm, 5 watt.
    - Resistor, 680 ohm, 1/4 watt.
    - Resistor, 10K ohm, 1/4 watt (2 required).

Terminal Connection

The GETC Test Procedure uses an ASCII terminal or a PC, running a terminal emulation program to communicate with the GETC. The following steps set up the terminal and provide instructions for connecting the terminal to the GETC.

1. Configure the terminal for the following communication protocol:

Baud Rate	2400 baud
Data Bits	7
Stop Bits	1
Parity	Odd
Characters	Uppercase
Data Transfer	Full Duplex

2. Fabricate a Terminal (PC) to GETC cable if necessary. Terminal and GETC pin assignments are listed in Table 6.

NOTE

If the GETC has GETC Cable 19C336863 installed between the Logic Board and J100 thru J103, then use the TQ-3360 PC Programming cable connected between the PC and J100 or J101.

Fabricate a cable with a 25-pin DB-25(M) connector (similar to AMP # 205207) on one end and a 6-pin connector (similar to Molex 22-01-2065-P(F)) on the other end as shown in Figure 15.

This fabricated cable (or TQ-3360) must be installed any time the terminal communicates with the GETC and connects between the Terminal's output port and J8 or J19 (J100 or J101) as directed by the test procedure.

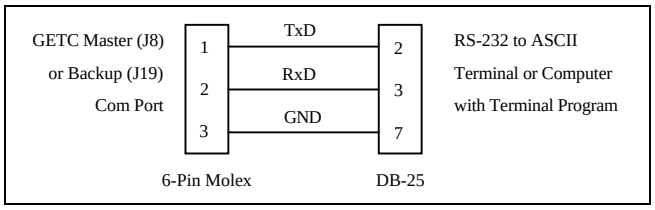


Figure 15 - Terminal-to-GETC Connection Cable

Table 6 - GETC and RS-232C Pin Assignments

SIGNAL FROM GETC	GETC LOGIC BD PIN NUMBER (Using fabricated cable)	GETC SHELF PIN NUMBER (Using TQ-3360 PC Programer cable)	TERMINAL EIA RS-232C D-TYPE CONNECTOR PIN NUMBER
TXD	J8-1 (MASTER)	J100-3 (MASTER)	PIN 3
TXD	J19-1 (BACKUP)	J101-3 (BACKUP)	PIN 3
RXD	J8-2 (MASTER)	J100-2 (MASTER)	PIN 2
RXD	J19-2 (BACKUP)	J101-2 (BACKUP)	PIN 2
GND	J8-3 (MASTER)	J100-1 (MASTER)	PIN 7
GND	J19-3 (BACKUP)	J101-1 (BACKUP)	PIN 7

Software Requirements

The test procedures described in this manual require firmware (EPROM U2) that includes the SIMON Test code. The following PROMS contain the SIMON Test code:

19A705595GXX	EDACS 900 MHz
19A149256G16 (or later)	PST (EDACS and BASIC EDACS)
349A9607G2 (or later)	PST (EDACS and BASIC EDACS)

If the PROM installed in the GETC does not contain SIMON, the PROM will have to be changed to one of those listed above.

Although the PROM's listed above contain the SIMON program, not all versions are capable of performing all of the tests listed. Therefore, it is recommended that only the 349A9607G2 or later versions be used.

Using SIMON

To use SIMON properly, please observe the following conventions:

- Characters that are typed from the keyboard are followed by RETURN (ENTER).
- A key press on the keyboard (such as ESC, TAB, or RETURN) is indicated in this procedure by the key name enclosed in square brackets [KEY PRESS].
- Control functions are indicated by CTRL - <CONTROL CHARACTER>, such as CTRL-Z to indicate the Z is pressed while holding down the CTRL key.
- If variable data or commands are to be entered, they will be enclosed in angle brackets <VARIABLE DATA> or <COMMAND>. Variable data depends on the particular application or test. Type the appropriate response (do not include brackets) followed by pressing the RETURN key, if required.

Test Preparation

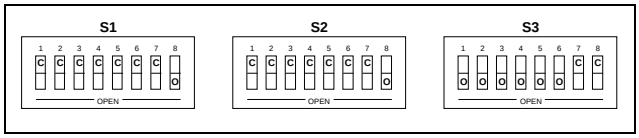
Before starting tests, prepare the GETC by reconfiguring the jumpers and DIP switches. When the DIP switches are set to the Terminal SIMON settings, the GETC will automatically invoke SIMON.

1. Make a record of all current jumper locations and DIP switch settings.

2. Reconfigure the jumpers to the test configuration as shown in Table 7.

   The location of the jumpers may be found by using the Logic Board layout diagram in Figure 16. This figure also provides the locations of test points refered to throughout the Test and Alignment section.

3. Set the DIP switches S1-8, S2-8, and S3-1 thru S3-6 to the OPEN (logical 1) position as shown below:



   All other switches should be in the OFF (logical 0) position.

4. On the GETC Logic Board, adjust R1, R2, and R141 to mid-position.

5. Verify the correct PROM is installed in XU2.

6. Disconnect cables from J6 thru J8 and J19 and connect the Terminal (or PC) output port to the GETC Logic Board Master Communication Link (MCL) at J8. If using the TQ-3360 cable, disconnect cables from J100 thru J103 and connect the PC to J100.

Table 7- Jumpers For Test Configuration

Jumper Position	Initial Test Position	FUNCTION
P11*	1&2	Receive data from 9600 baud modem board.
P12*	1&2	Clear to send from 9600 baud modem board.
P13	1&2	BSL Tx output to BSL Rx input.
P14	1&2	Master site controller path selection enable.
P15	1&2	Backup site controller path selection enable.
P16	1&2	BSL selection enable.
P17	1&2	LSD encode path enable.
P18	1&2	LSD decode path enable.
P20	OMIT	
P21	1&2	Enable high-speed data acquisition rate control, HSACQ.
P24	1&2	BSL selection (Failsoft) enable.
P25	1&2	LSD encode path enable.
P26	1&2	Lock-detect path enable.
P28	1&2	Sync line input path enable.
P29	1&2	Enable site controller RxD, J8-4.
P44	1&2	Use for 256K or 512K EPROM.
P46	1&2	INTO for voter concentrator.
P47	1&2	BSL select.
P48	1&2	BSL select.
P50	1&2	Enable tone control for voted system
P51	1&2	Morse code ID enable.
P52	2&3	TxD polarity select.
P53	1&2	RxD polarity select.
P54	1&2	Enable MODCNTL local control.
P55	OMIT	
P60	1&2	Enables HSD path.
P61	2&3	Use for 512K EPROM.
P62	1&2	Selects 11.059 MHz clock Freq. for 9600 baud data, 5.5296 MHz for 4800 baud data.
P63	OMIT	ON for Narrow HSD Filter, OMIT for Wide HSD Filter.
P64	OMIT	Same as P63.
P65	OMIT	Same as P63.
P66	OMIT	Same as P63.
P67	1&2	Receive telephone line termination.
P68	1&2	Selects Local (on)/Remote (off) control of station PTT.
P69	1&2	Enables COMB PTT IN.
P71	1&2	Enables telephone modem RTS control.
P72	1&2	Selects internal oscillator.
P73	2&3	Enables NOR gate U22B for PST appl.
P74	2&3	Selects CAS input to microprocessor.

Legend: LSD = Low Speed Data BSL = Backup Serial Link
RxD = Receive Data HSD = High Speed Data
MSL = Main Serial Link TxD = Transmit Data
* = For Rockwell Modem communications

POWER SUPPLY TEST

1. Connect power supply to GETC connector J10 (pin 1 is +13.8 V and pin 2 is ground).

2. Turn on the power supply and verify the current drawn does not exceed 1.0A (2.0A with modem board installed). If current is exceeded, check for shorts before proceeding.

3. Connect a frequency counter or oscilloscope to TP104 and verify the presence of the 9600 Hz clock. If the clock is missing, check modem U4 and associated circuitry.

4. Measure the following regulated power supply voltages with respect to ground (J10-2):

Monitor Point	Voltage	Check if missing/incorrect
TP110	+5.0 ±0.25 V	Regulator Board (A2)
TP111	+5.0 ±0.25 V	Regulator Board (A2)
TP108	-12.0 ±1.2 V	-12 Volt Regulator (U39)
TP109	+12.0 ±1.2 V	+12 Volt Regulator (U40)

5. Move jumper P62 to J62 pins 2 and 3. Using an oscilloscope or frequency counter, verify the presence of the 4800 Hz clock on TP104. If the clock is missing, check modem U4 and U41.

6. Move P62 back to J62 pins 1 and 2.

LOGIC BOARD TEST

These tests may be used to bench-test the GETC or test the GETC when it is installed in a station. If the tests are performed while the GETC is in a station, connectors J6 thru J8 and J19 must be disconnected.

Serial Link Test

1. Apply power to the GETC (or press RESET switch S4 if power is already applied). The terminal will display the SIMON welcome message. If the welcome message does not appear check the following:
   - Check terminal hookup to J8 (J100).
   - Be sure DIP switches (S1 - S3) are set correctly.

- Check for +5 volts at U14-4 (SITE RX EN).
- Check for proper operation of the reset circuitry,
- Check for serial data on the TX and RX lines (see Site Controller Interface)

2. Execute the <BCL> command (backup communications link) on the terminal. Press [RETURN] and verify terminal communication to the master link is inoperative (i.e. no SIMON welcome message).

3. Move the terminal connection from the master link J8 (J100) to the backup link J19 (J101). Press [RETURN] and verify the terminal communication on the backup link is operative. The terminal will display the SIMON welcome message.

4. Execute the <MCL> command (master communications link) on the terminal. Press [RETURN] and verify terminal communication to the backup link is inoperative.

5. Move the terminal connection from the backup link J19 (J101) to the master link J8 (J100). Press [RETURN] and verify the terminal communication on the master link is operative. The terminal will display the SIMON welcome message.

Modulation Setting Test

1. Execute the command <XBY B000=10>. This connects the High Speed Data Filter's output from U16 to J7-4 through U15-A.

2. Execute the command <FNT3>. The modem generates a 4800 Hz signal at U4-21.

3. Connect an oscilloscope to J7-4. Adjust R31 for a scope indication of 1 Vpp ±10%.

4. Enter CTRL-Z or [ESC] to end the test.

RAM (U3) Test

1. Execute the command <TMX 0000-1FFFF> to check U3.

2. Verify the terminal response of:

SIX PATTERNS CHECK OK

Microprocessor Oscillator Test

1. Connect the frequency counter to J62 pin 1.

2. Verify the microcomputer clock frequency is 11.0592 MHz ±500 Hz.

Reset Circuit (U17) Test

1. Lower the power supply input voltage to +6 volts.

2. Slowly increase the voltage until the GETC resets and sends the SIMON welcome message to the terminal. The power supply voltage should be between +6 and +9 volts.

3. Return the power supply input voltage to +13.8 volts.

4. Press and release RESET switch S4. Verify the GETC resets and sends the SIMON welcome message to the terminal.

5. Momentarily ground J7-3. Verify the GETC resets and sends the SIMON welcome message to the terminal.

Watchdog Timer (U4) Test

1. Execute the command <WAT> to verify watchdog timer (U4) time out.

2. Verify the GETC sends the SIMON welcome message to the terminal after a two (2) second delay.

Transmit and Receive Data Test

This test verifies the operation of the 9600 baud modem (U4) and the High Speed Data (HSD) Filter. The 9600 baud data is generated at U4-21 and sent through HSD Filter U16.

1. Execute the command <XBY B000=10>. This causes switch U15-A to route any transmitted data to J7-4.

2. Connect a jumper from J7-2 to J7-4. This routes the transmit data to the receive data port.

3. Execute the command <MDS 0>. This command selects the RF modem (U4) for the Bit Error Rate (BER) command.

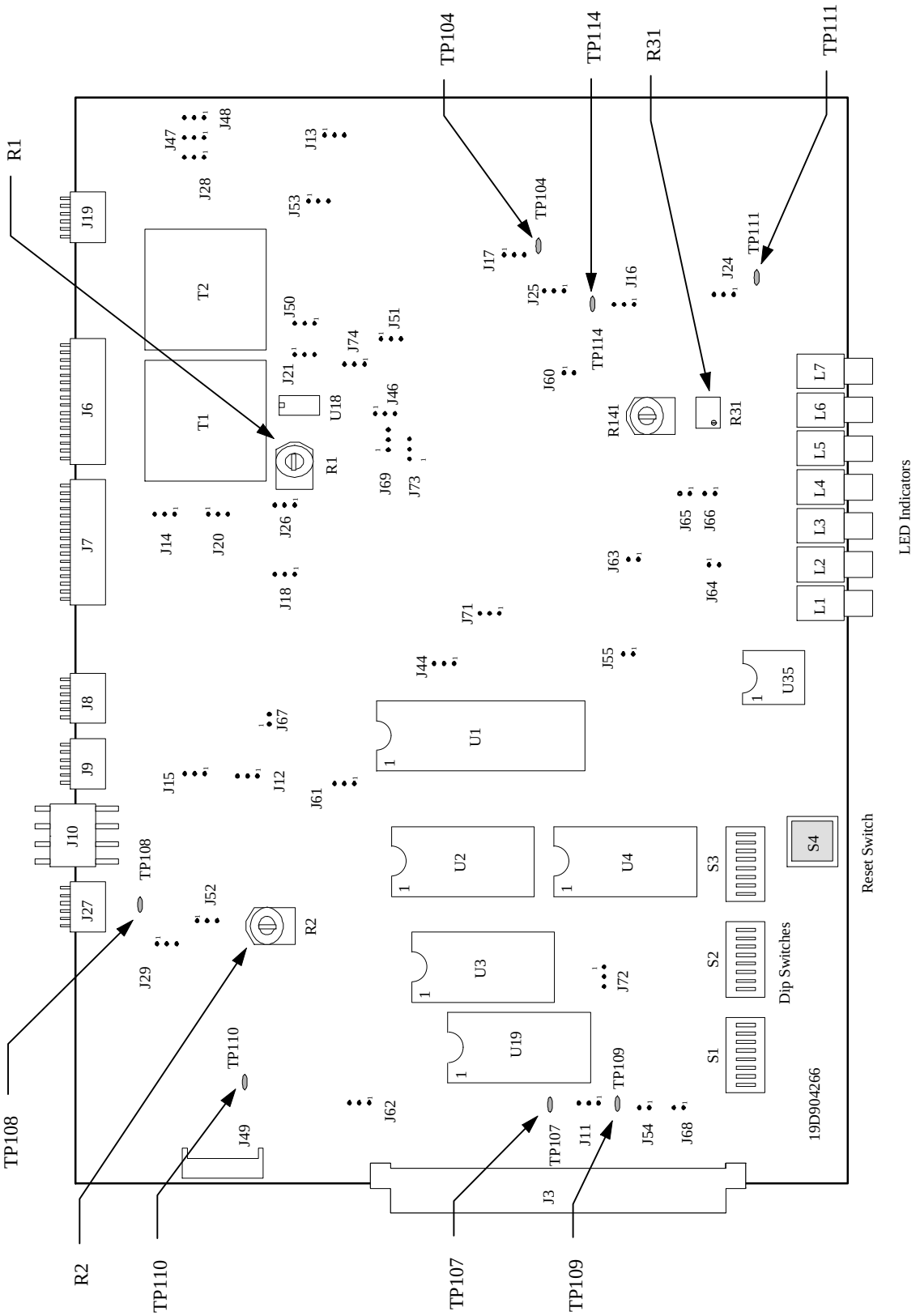


Figure 16 - Station GETC (19D904266) Jumper and Test Point Locations

4. Execute the command <BER DE-00=1>. This command transmits data and simultaneously checks for data being received.

5. After 10 seconds, Verify the terminal response of:

   ERROR COUNT = 0000 RECEIVE
   CHECKSUM = 00027C11

NOTE

The test will continually output data in 10 second intervals. Filtered data may be observed at J7-4

6. To end the test, press CTRL-Z or [ESC].

7. Remove the jumper between J7-2 and J7-4.

Octal Latch (U38) Output Test

This test verifies the ability of the Octal Latch (U38) to change states when directed.

1. Move the jumper P15 to J15 pins 2 and 3.

2. Connect a 10K ohm pull-up resistor between +13.8 V (TP125) and J15-1.

3. Execute the command <XBY B800=B6>.

4. Verify the logic levels at the following points using an oscilloscope or DC Voltmeter.

MONITOR POINT	**LOGIC LEVEL** LO = <0.5 V HI = >4 V, unless otherwise noted	**FUNCTION**
J15-1	LO	11/73-2 select
J19-6	HI(> 13.0 V)	SYNC
U34-10	LO	LS ACQ
U38-15	HI	EEPROM power
U38-16	LO	EEPROM clock
U38-19	HI	not used
U38-2	LO	Walsh bit 1
U38-5	HI	Walsh bit 2

5. Enter CTRL-Z or [ESC].

6. Execute the command <XBY B800=49>.

7. Verify the logic levels at the following points using an oscilloscope or DC Voltmeter.

MONITOR POINT	LOGIC LEVEL LO = <0.5 V HI = >4 V, unless otherwise noted	FUNCTION
J15-1	HI (>13.0 V)	11/73-2 select
J19-6	LO	SYNC
U34-10	HI (>10.0 V)	LS ACQ
U38-15	LO	EEPROM power
U38-16	HI	EEPROM clock
U38-19	LO	not used
U38-2	HI	Walsh bit 1
U38-5	LO	Walsh bit 2

8. Remove pull-up resistor from J15-1 and move the jumper P15 back to J15 pins 1 and 2.

9. Reset the GETC by pressing S4. The GETC should send the SIMON welcome message to the terminal.

10. After receiving the welcome message, execute the <BCL> command to select the backup communication link.

11. Move the terminal connection from J8 (J100) to J19 (J101).

12. Execute the <MCL> command to return to the master communication link.

13. The "MCL" command characters should be ehcoed on the screen. If no echo occurs, ensure jumper P15 is on J15 pins 1 and 2.

14. Move the terminal connection from J19 (J101) to J8 (J100).

Low Speed Handshaking Test

This test checks the operation of the Low Speed Data Encode Filter (steps 1 and 2) and the Low Speed Data Decode Filter (steps 3 thru 8).

1. Connect an oscilloscope and a voltmeter to J19-5.

2. Execute the commands for each case listed below and verify the output amplitude and symmetry. Enter CTRL-Z or [ESC] after verifying the parameters of each case.

Case	Command	Frequency (Hz)	Amplitude (Vrms), unless otherwise noted
1	LSH 1-1	10	0.99 to 1.00
2	LSH 1-2	100	0.80 to 1.00
3	LSH 1-3	200	0.44 to 0.54
4	LSH 1-4	1000	>32 dB below value measured in case 2
5	LSH 2-1	10	0.380 to 0.415
6	LSH 2-2	100	0.307 to 0.370
7	LSH 2-3	200	0.16 to 0.20
8	LSH 2-4	1000	>32 dB below value measured in case 6
9	LSH 3-1	10	1.04 to 1.20
10	LSH 3-2	100	0.92 to 1.18
11	LSH 3-3	200	0.51 to 0.63
12	LSH 3-4	1000	>32 dB below value measured in case 10

3. Connect a jumper from J19-5 to J7-2. Disconnect the oscilloscope and voltmeter.

4. Execute the <LSH 1-1> command.

5. Connect an oscilloscope to J18-1 and verify the square wave has a low level value <0.5 V and a high level value >4.5 V.

6. Enter CTRL-Z or [ESC] to terminate the test.

7 Repeat steps 5 and 6 for the following commands:

<LSH 1-2>

<LSH 1-3>

8. Disconnect the oscilloscope and remove jumper from J19-5 to J7-2.

DIP Switch Test

This test verifies the operation of the DIP switches and their associated buffers - S1/U8, S2/U9, and S3/U7.

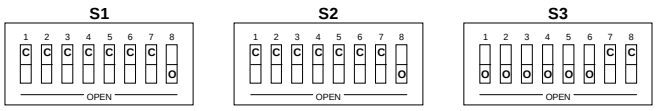
1. Execute the command <DSW>. The terminal will display the current DIP switch values (OPEN = 1 and CLOSED = 0) as shown below:

```
00000001    00000001    11111100
1      8    1      8    1      8
   S1          S2          S3
```

2. Check the open and closed position of each switch. An OPEN on the DIP switch is displayed as "1", while a CLOSED is displayed as a "0".

   This test continually updates the terminal display at each DIP switch setting change.

4. Return DIP switches S1-8, S2-8, and S3-1 thru S3-6 to the open position (shown below) to invoke SIMON.



5. Enter CTRL-Z or [ESC] to end the test.

Baud Divide by 2 Circuit (U41)

This test checks the divide by two function of U41 for applications requiring 4800 baud RF modem data.

1. Move P62 to J62 pins 2 and 3. This routes the 5.5925 MHz clock signal output of the divide by two circuit (U41) to the RF modem U4-16.

2 Install jumpers on J63 pins 1 and 2, J64 pins 1 and 2, J65 pins 1 and 2, and J66 pins 1 and 2.

3. Execute the command <XBY B000 = 10>. This connects the High Speed Data Filter's output (U16) to J7-4 through U15-A.

3. Execute the command <FNT3>. The causes the modem to generate a 2400 Hz signal at U4-21.

4. Connect an oscilloscope to J7-4 and verify the presence of a 2400 Hz signal.

5. Connect a Distortion Analyzer to J7-4 and measure the distortion of 2400 Hz signal. The distortion must be less than 10%.

6. Enter CTRL-Z or [ESC] to end the test.

7. Move P62 back to J62 pins 1 and 2. (Do not remove jumpers P63 thru P66 at this time.)

HSD Filter (U16) Frequency Response Test

This test verifies the frequency response of the Narrow and Wide High Speed Data (HSD) Filters.

NOTE

GETCs with the "MODIFIED FOR EUROPEAN OPERATION" label have been modified to be European Technical Standards Institute (ETSI) compliant. Refer to the Modifications section of this manual for the ETSI HSD Filter Frequency Response test procedure.

1. Execute the command <XBY B000=10>. This connects the filter output to J7-4 through switch U15-A.

2. Connect the function generator, through a 10 µF capacitor, to TP114 on the GETC logic board.

3. Adjust the function generator for a 1000 Hz, 1.0 Vrms signal at TP114.

4. Connect a distortion analyzer or AC voltmeter to J7-4.

5. Vary the input frequency while monitoring the output level. Verify the frequency response for the Narrow HSD Filter is within the limits listed in Table 8 (1000 Hz reference at 1.0 Vrms input).

6. Remove the jumpers from J63 thru J66 to select Wide HSD filtering.

Table 8 - Narrow HSD Filter Response

Frequency (Hz)	Response (dB)
10	0 ±1
500	0 (reference)
1500	0 ±1
3000	-2 ±1
3500	-3 ±1
10,000	<-20

7. Vary the input frequency while monitoring the output level. Verify the frequency response for the Wide HSD Filter is within the limits listed in Table 9 (1000 Hz reference at 1.0 Vrms input).

Table 9 - Wide HSD Filter Response

Frequency (Hz)	Response (dB)
10	0 ±1
1000	0 (reference)
3000	0 ±1
6000	-2 ±1
7000	-3 ±1
20,000	<-20

8. Disconnect test equipment.

Phone Modem (U19) Test

This test verifies the operation of the Phone modem (U19) by looping the transmit data to the receive data port.

1. Move the jumper P11 to J11 pins 2 and 3.

2. Install a jumper from J9-3 to J9-4.

3. Execute the command <MDS 1>. This selects the phone modem for the BER command.

4. Execute the command <BER DE-00=1>. This command causes the modem to transmit data and simultaneously verify the same data is being received.

6. Verify the terminal response of:

   ERROR COUNT = 0000 RECEIVE CHECKSUM 00027C11

NOTE

The test will continually output data in 10 second intervals. The data train may be observed at TP105 and TP107.

5. Enter CTRL-Z or [ESC] to end the test.

6. Move the jumper P11 back to J11 pins 1 and 2.

7. Remove the jumper from J9-3 to J9-4.

Output Latch And Buffer Test (U20 &U21)

This test verifies the ability of the output latches and buffers (U20 and U21) to change states and checks the front panel LED's for proper indications.

1. Move jumper P14 to J14 pins 2 and 3.

2. Move jumper P24 to J24 pins 2 and 3.

3. Move jumper P25 to J25 pins 2 and 3.

4. Remove jumper P20.

5. Install a 10K ohm resistor from J7-14 to ground

6. Connect another 10K ohm resistor between the test probe and +13.8 volts (TP125)

NOTE

All outputs, except as noted, are open collector and must be pulled up to +13.8 V before they will go high.

7. Execute the command <XBY A800 = 52>.

8. Execute the command <XBY B000 = 42>.

9. Connect J7-6 to ground.

10. Verify the logic state at the locations listed below:

Test Point	Logic Level	Remarks
J6-1	HI	
J6-2	HI	
J6-3	Hi	
J6-4	LO	No pull-up required
J6-5	HI	
J6-10	HI	
J6-11	LO	No pull-up required
J6-12	HI	
J6-13	LO	No pull-up required LO < 0.5 V
J6-14	HI	
J6-15	LO	
J6-16	HI	
J7-14	LO	Use 10K resistor to GND LO < 0.5 V
J7-15	LO	No pull-up required LO < 0.5 V
J7-16	LO	
J9-1	HI	No pull-up required HI > 10 V
J3A-25	LO	No pull-up required LO < 0.5 V
J3C-13	HI	No pull-up required HI > 3.5 V

11. Verify front panel LED's L3, L4, and L6 are ON as shown below:

	L1 (H7)	L2 (H6)	L3 (H5)	L4 (H4)	L5 (H3)	L6 (H2)	L7 (H1)
LED Indicators	❍	❍	●	●	❍	●	❍

Legend: ❍ = OFF ● = ON ❇ = FLASHING

12. Execute the command <XBY B000 = B9>.

13. Execute the command <XBY A800 = AD>.

NOTE

Ensure jumper is still connected between J7-6 and Ground.

14. Verify the logic state at the locations listed below:

Test Point	Logic Level	Remarks
J6-1	LO	
J6-2	LO	
J6-3	LO	
J6-4	HI	No pull-up required
J6-5	LO	
J6-10	LO	
J6-11	HI	No pull-up required
J6-12	LO	
J6-13	HI	No pull-up required HI > 3.5 V
J6-14	LO	
J6-15	HI	
J6-16	LO	
J7-14	HI	Use 10K resistor to GND HI > 7 V
J7-15	HI	No pull-up required
		HI > 7 V
J7-16	HI	
J9-1	LO	No pull-up required LO < -10 V
J3A-25	HI	No pull-up required HI > 3.5 V
J3C-13	LO	No pull-up required LO < 0.5 V

15. Verify front panel LED's L1, L2, L5, and L7 are ON as shown below:

	L1 (H7)	L2 (H6)	L3 (H5)	L4 (H4)	L5 (H3)	L6 (H2)	L7 (H1)
LED Indicators	●	●	❍	❍	●	❍	●

Legend: ❍ = OFF ● = ON ❇ = FLASHING

16. Execute the command <XBY A800 = 00>.

NOTE

Echoes will not occur during this command.

17. Execute the command <XBY B000 = 0C>.

18. Remove the jumper between J7-6 and ground.

19. Verify the logic state at the following locations:

Test Point	Logic Level	Remarks
J6-1	HI	
J6-2	HI	
J6-3	HI	
J6-4	HI	No pull-up required
J6-5	HI	

Test Point	Logic Level	Remarks
J6-10	HI	
J6-11	HI	No pull-up required
J6-12	HI	
J6-13	HI	No pull-up required HI > 3.5 V
J6-14	HI	
J6-15	HI	
J6-16	HI	
J7-14	HI	Use 10K resistor to GND HI > 7 V
J7-15	LO	No pull-up required LO < 0.5 V
J7-16	HI	
J9-1	HI	No pull-up required HI > 10 V
J3A-25	LO	No pull-up required LO < 0.5 V
J3C-13	LO	No pull-up required LO < 0.5 V

20. Verify all front panel LED's (L1 thru L7) are OFF.

21. Execute the command <XBY A800 = 80>.

22. Execute the command <XBY B000 = 08>.

23. Verify the logic state at the following locations:

Test Point	Logic Level	Remarks
J6-1	LO	
J6-2	LO	
J6-3	HI	
J6-4	HI	No pull-up required
J6-5	HI	
J6-10	HI	
J6-11	HI	No pull-up required
J6-12	HI	
J6-13	HI	No pull-up required HI > 3.5 V
J6-14	HI	
J6-15	HI	
J6-16	HI	
J7-14	HI	Use 10K resistor to GND HI > 7 V
J7-15	HI	No pull-up required HI > 7 V
J7-16	HI	
J9-1	HI	No pull-up required HI > 10 V
J3A-25	LO	No pull-up required LO < 0.5 V
J3C-13	LO	No pull-up required LO < 0.5 V

24. Verify all front panel LED's (L1 thru L7) are OFF.

25. Move jumper P14 from J14 pins 2 and 3 to J14 pins 1 and 2.

26. Move jumper P24 from J24 pins 2 and 3 to J24 pins 1 and 2.

27. Move jumper P25 from J25 pins 2 and 3 to J25 pins 1 and 2.

28. Press S4 and reset GETC.

Input Buffer And Port Pins Test

1. Move the following jumpers:
   - P26 to J26 pins 2 and 3
   - P28 to J28 pins 2 and 3
   - P12 to J12 pins 2 and 3.
2. Connect a jumper from J9-5 to J9-1 (RTS to CTS).
3. Execute command <XBY B000=08>. This pulls-up J7-14 and applies an RS-232 HI to J9-5.
4. Ground J7-7, J7-9, J7-11, and J7-13.
5. Execute the command <POR1> and verify the terminal response of:

   1010 1010

6. Execute the command <POR3> and verify the terminal response of:

   XX01 XXXX

   (X=DON'T CARE)

7. Remove the ground connection to J7-7, J7-9, J7-11, and J7-13.
8. Execute the command <XBY B000=01>. This pulls-up J7-14 and applies an RS-232 LO to J9-5.
9. Ground J7-6, J7-8, J7-10, J7-12 and J7-14.
10. Execute the command <POR1> and verify the terminal response of:

    0101 0101

11. Execute the command <POR3> and verify the terminal response of:

    XX10 XXXX

12. Move the following jumpers:
    - P26 to J26 pins 1 and 2
    - P28 to J28 pins 1 and 2
    - P12 to J12 pins 1 and 2.
13. Install jumper P20 on J20 pins 1 and 2.
14. Remove jumper from P9-5 to P9-1.
15. Remove the grounds from J7-6, J7-8, J7-10, and J7-12.

Comparator Test (U31-B)

This test checks the operation of the adjustable comparator used to sense external DC inputs on J7-10.

1. Move P74 to J74 pins 1 and 2 and ensure R141 is adjusted to its midrange position.
2. Apply a logic +5 Vdc (TP111) to J7-10.
3. Execute the command <POR1> and verify the terminal response of:

   XXX1 XXXX

4. Remove the 5 volts and connect J7-10 to ground.
5. Execute the command <POR1> and verify the terminal response of:

   XXX0 XXXX

6. Remove the ground connection from J7-10 and move P74 to J74 pins 2 and 3.

Transmit Clock Test

1. Connect an oscilloscope and frequency counter to J3C-16 and observe a 9600 Hz square wave.
2. The square wave frequency should be 9600 Hz ±1 Hz (104.17 µs period).
3. Verify the square wave's minimum amplitude is 0 Vdc and maximum amplitude is greater than 4.2 Vdc.

FSL & BSL Drive Test

1. Connect a 100 ohm 5 watt resistor between the +13.8 Vdc (TP125) and J19-6.
2. Execute the command <XBY B800 = 08>.
3. Measure the voltage at J19-6, voltage must be less than 0.8 Vdc.

4. Execute the command <XBY B800 = 00> and remove the 100 ohm resistor.

5. Connect a 10K ohm resistor between J19-6 and ground (TP124).

6. Measure the voltage at J19-6, voltage must be greater than 11.0 Vdc.

7. Remove the 10K resistor.

8. Remove P24 and connect a 100 ohm 5 watt resistor between the +13.8 Vdc (TP125) and J8-5.

9 Execute the command <XBY A800 = 20>.

10. Execute the command <POR3 = ED> (echoes will not occur).

11. Measure the voltage at J8-5, voltage must be less than 0.8 Vdc.

12. Reset the GETC either by depressing S4 or by momentarily grounding J7-3.

13. Remove the 100 ohm resistor and connect a 10K ohm resistor from ground (TP124) to J8-4.

14. Measure the voltage at J8-5, voltage must be greater than 11.0 Vdc.

15. Remove the 10 K resistor and install P24 on J24 pins 1 and 2.

ROCKWELL MODEM TEST

This test verifies the operation of the Rockwell modem by looping transmit data to the receive data port. If a Rockwell modem is not installed, skip this test and proceed to the next test.

NOTE

Rockwell modem board must be installed for this test.

1. Ensure P11 in installed on J11 pins 1 and 2.

2. Connect a jumper between J6-6 and J6-8 on the GETC Logic Board.

3. Connect a jumper between J6-7 and J6-9.

4. Connect a 680 ohm resistor between J6-8 and J6-9. This loads the transformer.

5. Adjust R1 (PH RX ADJ) and R2 (PH TX ADJ) to midrange.

6. Execute the command <TIM19>. This sets the time delay from RTS to beginning of data to 250 milliseconds.

7. Execute the command <MDS 1>. This command selects the Rockwell modem for the BER command.

8. Execute the command <BER DE-00=1>, and verify the terminal response of:

   ERROR COUNT = 0000 RECEIVE CHECKSUM = 00027C11

NOTE

The first response may be in error. The test runs continually outputting data in 10 second intervals.

9. Enter CTRL-Z or [ESC] to end the test.

10. Remove the 680-ohm resistor and jumpers on J6-6 thru J6-9.

TEST COMPLETION

1. Remove power from the GETC.

2. Restore the jumpers to the correct operational configuration recorded in step 1 in the Test Preparation section.

3. Set the DIP switches to the operational configuration for the station.

4. Install the correct operating firmware (EPROM) if the firmware was changed for the SIMON test.

5. Return the GETC to the GETC shelf. Make sure all required plugs P6 thru P8 and P19 are properly connected to J6 thru J8 and J19, respectively, at the rear of the logic board or system cables connected to J100 thru J102.

TROUBLESHOOTING

The hardware used in the GETC is extremely reliable, making component failure the unlikely cause of most problems. The most common causes of problems are programming errors and interface connections.

ON SITE TROUBLESHOOTING

Use the following guidelines when troubleshooting a GETC on site:

1. Verify the condition of front panel LEDs. In some applications these indicators will actually indicate the cause of the failure or identify communication problems.
2. If available, use the activity logging feature to isolate activity which might be contributing to the problem.
3. Verify that all cables are properly connected and secure. Refer to the applicable configuration manual.
4. Verify the GETC's personality is properly programmed for the specific application. Refer to the configuration manual and the software release notes.
5. Verify the Turbo Board is properly configured if applicable.
6. If you suspect that the GETC has failed, replace the GETC with a known good unit properly configured for this application.
7. If the replacement GETC resolves the problem, bench check the defective unit using the Test and Alignment procedures contained in this manual.

IN CASE OF DIFFICULTY

If you are unable to resolve a problem to your satisfaction, then contact the Ericsson Technical Assistance Center (TAC) at 1-800-528-7711 (outside USA, 804-528-7711).

MODIFICATIONS

As a result of the diversification of the GETC, the maintenance technician is apt to encounter a number of different variations of this unit.

The modifications presented in this section are some of the more common modifications which may be encountered in a basic GETC. However, it will be necessary to refer to the configuration manual for the specific GETC application in order to identify any unique modifications and the required interface cabling and harnesses.

GETC LSD FILTER, 19C852138P1

Description

The GETC LSD Filter is a four-pole elliptic filter with a nominal bandwidth of 50 Hz and a lower frequency peak ripple response of the filter centered at 75 Hz. This centering at a nominal 75 Hz is controlled by an on-board clock (9100 Hz). If the filter is installed in a system using test radios, their personality EPROMs (19A705272) must be Group 6 or higher.

Specifications

Temperature Range .....0 C to 70 C

Supply Voltage.....+5 Vdc to -12 Vdc

Input Audio Level.....0 dBm

Output Audio Level .....5.5 dBm ±4 dBm at 75 Hz

Frequency Response:	25 Hz and below	<-30 dB
(Ref. 0 dB at 75 Hz)	300 Hz to 4,000 Hz	<-30 dB
	105 Hz	±3 dB
	250 Hz	<25 dB

Installation

The installation of the LSD filter requires the removal of a couple of components, mounting the LSD Filter Board, and tacking the wires to the designated points on the GETC Logic Board.

Basically, the filter, shown in Figure 17 replaces the filter built around U33 (refer to Figure 8).

Refer to the drawings in the back of this manual for the LSD Filter Board's schematic and outline diagram.

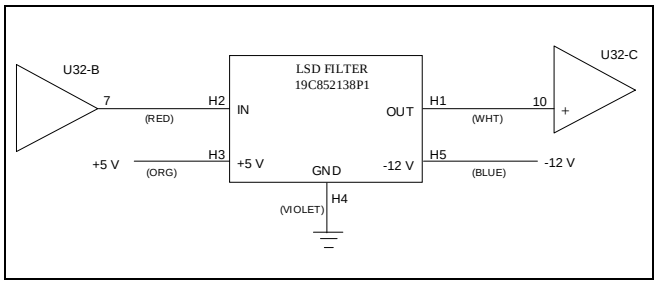


Figure 17 - LSD Filter 19C852138P1

The following steps summarize the LSD Filter Board installation:

1. Resistor R79 and capacitor C34 were removed.
2. Capacitors C18 and C21 were bent over so they would not interfere with the board's installation.
3. The LSD Filter Board was mounted on the Logic Board by using a stand-off and longer screw at the mounting location above J17.
4. The wires were connected between the LSD Board and the Logic Board at the following points:

LSD Board	COLOR	LOGIC BOARD
H1 (OUT)	White	R79 - end toward front of shelf.
H2 (IN)	Red	R68 - end toward front of shelf.
H3 (+5 V)	Orange	D27 - anode side.
H4 (GND)	Violet	R81 - end toward rear of shelf.
H5 (-12 V)	Blue	C13 - negative side.

Filter Testing

This filter board contains test pads and alignment holes to allow for easy test fixture design. Figure 18 shows the nominal frequency response for this board. A quick and easy way to verify the filter board's frequency response is to use an audio spectrum analyzer such as a Hewlett Packard HP3580A which contains its own audio tracking generator to apply to the audio input of the filter board. Besides power supplies, this is the only piece of test equipment needed. The HP3850A can display a reference filter board's frequency response plot besides the UUT response display for visual comparison.

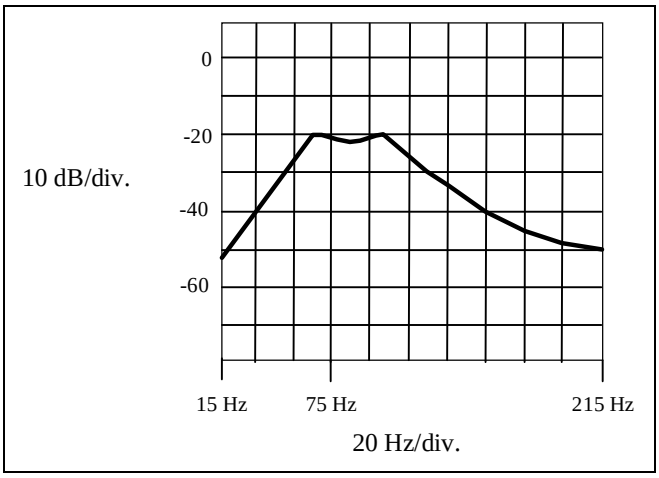


Figure 18 - LSD Filter Response

OPTION SXMK3L - ETSI GETC (HSD Filter Mod. 350A1127G1)

Description

In order to be in compliance with the European Technical Standards Institute (ETSI) requirements for adjacent channel power requirements, it is necessary to change the frequency response of the Narrow and Wide High Speed (HSD) Filters.

Specifically the capacitors C6 thru C9, C96, and C97, and resistors R28 thru R30 are replaced with the components listed in the Parts List section of this manual for Option SXMK3L.

ETSI HSD Filter (U16) Frequency Response Test

This test verifies the frequency response of the Narrow and Wide HSD Filters installed by option SXMK3L for ETSI compliance.

NOTE

This procedure replaces the procedure titled "HSD Filter (U16) Frequency Response Test" in the Service and Test section of this manual.

1. Execute the command <XBY B000=10>. This connects the filter output to J7-4 through switch U15-A.

2. Connect the function generator, through a 10 μF capacitor, to TP114 on the GETC logic board.

3. Adjust the function generator for a 1000 Hz, 1.0 Vrms signal at TP114.

4. Connect a distortion analyzer or AC voltmeter to J7-4.

5. Vary the input frequency while monitoring the output level. Verify the frequency response for the Narrow HSD Filter is within the limits listed in the table below (1000 Hz reference at 1.0 Vrms input).

Table 10 - Narrow HSD Filter (ETSI)

Frequency (Hz)	Response (dB)
10	0 ±1
500	0 (reference)
1,500	0 ±1
2,500	-2 ±1
3,000	-3 ±1
8,000	<-20

6. Remove the jumpers from J63 thru J66 to select Wide HSD filtering.

7. Vary the input frequency while monitoring the output level. Verify the frequency response for the Wide HSD Filter is within the limits listed in the table below (1000 Hz reference at 1.0 Vrms input).

Table 11 - Wide HSD Filter (ETSI)

Frequency (Hz)	Response (dB)
10	0 ±1
1,000	0 (reference)
2,500	0 ±1
4,000	-2 ±1
4,500	-3 ±1
12,000	<-20

8. Disconnect test equipment.

GUARDOG AUTOMATIC RESET

The EDACS Guardog™ option allows users to automatically or remotely reset an EDACS repeater via the Station GETC. Automatic resetting is accomplished when the Reset Unit senses the GETC has enabled Failsoft. When Failsoft is enabled, the Reset Unit initiates an automatic reset cycle to reset to station.

Remote resetting is accomplished when the Reset Unit decodes individual reset commands from a DTMF telephone connected to the site.

Installation

GETC's with this option can be identified by the offset Turbo GETC Bracket (19C337711P1) with four connectors. Two of the connectors (J103 and J104) are for the Turbo option and two (J3 and J4) are for the Automatic Reset option.

The installation modifies the GETC by installing the Automatic Reset cable 19B803258P1. The following steps summarize the cable's installation which is diagrammed in Figure 19:

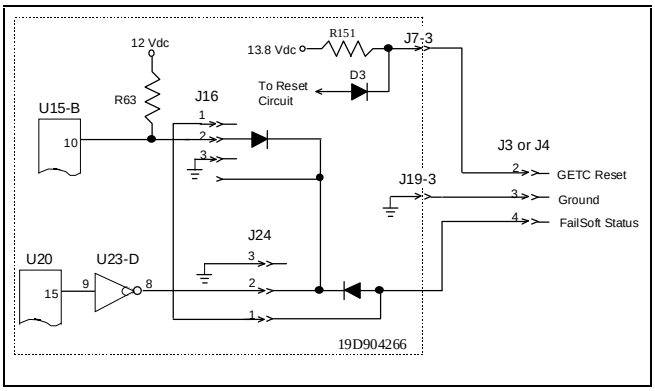


Figure 19 - GETC to Guardog Interface Diagram

1. The two 4-pin connector blocks are mounted in the GETC Turbo bracket at J3 and J4.
2. Jumpers from J16 and J24 are removed.
3. The cable's 3-pin plug (with the diode mounted on the side) is plugged onto J24. The plug's pin 1 (anode of diode) mates with J24 pin 1.
4. The cable's 4-pin plug is plugged onto J16. The plug's pin 1, 2, and 3 mate with J16's pin 1, 2 and 3 respectively.
5. The cable's red wire is inserted into J7-3 (RES IN).
6. The cable's black wire is inserted into J19-3 (GND).

Refer to LBI-39004 for complete details on installing the Guardog system and operation of the Reset Unit.

MICROPROCESSOR RYT 121 6060.

GETCs using the 349A9607G4 software (or later) require a faster microprocessor. This additional speed is provided by the Dallas *SpeedIt* µ*P* 80C320 microprocessor (RYT 121 6060/A). The processor is factory installed in GETC 19D904868G4.

For 19D904868G3 GETCs being upgraded to 349A9607G4 software, the microprocessor U1 (19A705557P1) must be replaced with the RYT 121 6060/A microprocessor. This modification is only applicable to GETC's used in the following product applications:

OPTION	DESCRIPTION
XXMD3D, XXMD3E	MASTR II/IIe Stations
XXPT1B	MASTR II/IIe Auxiliary Receivers
XXCP1H	Simulcast Control Point GETCs
STRB1H	900 MHz Stations
SXMD3J	MASTR III Stations
SRCP7E	MASTR III Auxiliary Receivers

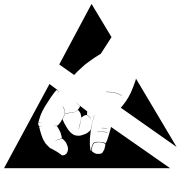
NOTE

The faster replacement microprocessor should not be installed in CNI, SCAT, or Uplink - Downlink GETCs. This processor and the operating software in these applications are currently incompatible.

Installation

Use the following procedure when installing the replacement microprocessor in U1.

CAUTION



Observe precautions for handling **ELECTROSTATIC SENSITIVE DEVICES**

1. Remove power from GETC.

2. Slide GETC shelf into service position.

3. Verify CMOS Modems U4 and U19 are EGE part number 19A704727P4 (manufactured by Texas Instruments). The faster microprocessor may not work properly with earlier versions of the modem.

4. Remove U1 (19A705557P1).

5. Install the new faster microprocessor (RYT 121 6060/A) into the XU1 socket. This processor is similar to the Dallas *SpeedIt* µ*P* (80C320).

6. Checkout GETC performance according to the test procedure in LBI-38894.

LIGHTNING PROTECTION GROUNDING

Maximum lightning protection is achieved when the GETC Lightning-Protection Grounding Kit (344A4500) is installed. This kit is normally installed at the factory for all GETC applications.

The following procedure summarizes the installation process:

1. Two wires (black 16 AWG hookup wire, 2-feet long) are prepared as follows:

   a. The wires are stripped and tinned 1/2-inch on one end and 1-inch on the other end.

   b. A solderless terminal (19B209260P1), bent approximately 30 degrees so it will clear the board mounting screw, is attached to the end stripped back 1/2-inch on each wire as shown in Figure 20.

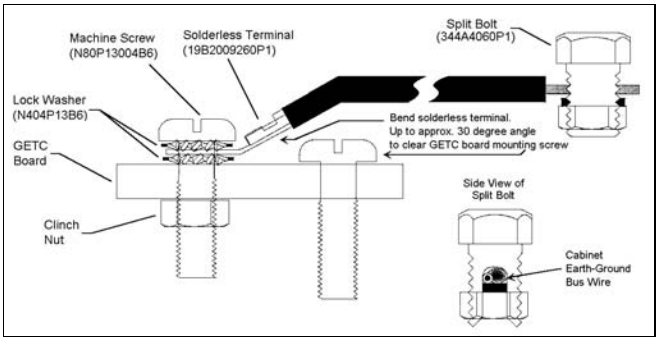


Figure 20 - Lightning-Protection Kit Installation Detail

2. The solderless terminal end of the wires is then attached to the GETC Logic Board using the lock washers and machinescrew as shown in Figure 20. A clinch nut is already mounted to the solder side of the board.

3. The wires are then routed out of the shelf as shown in Figure 21.

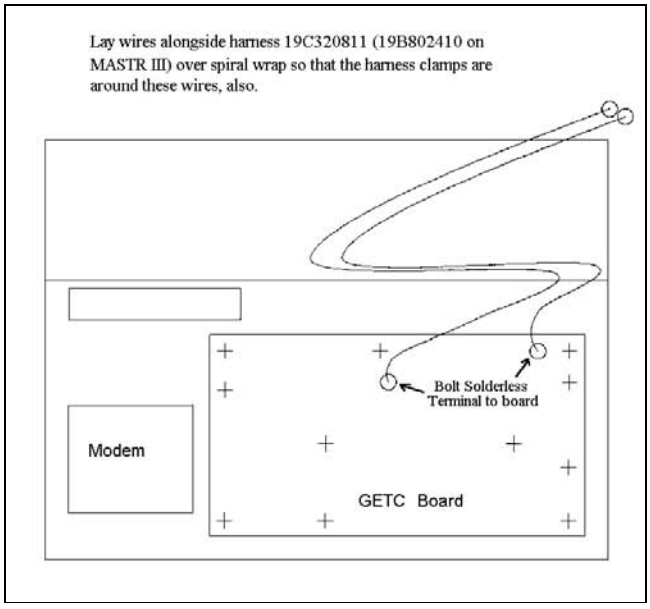


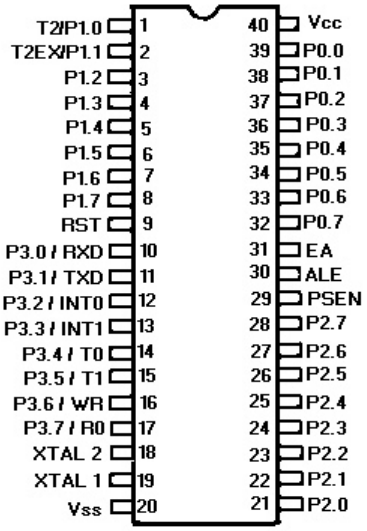
Figure 21 - Lightning-Protection Kit Cabinet Installation

4. When the shelf is installed in the rack, use the split bolts to attach the wires' end stripped 1-inch to the cabinet earth-ground bus wire (part of the Cabinet Grounding Strap Kit 344A4730) as shown in the split bolt side view in Figure 20.

NOTE

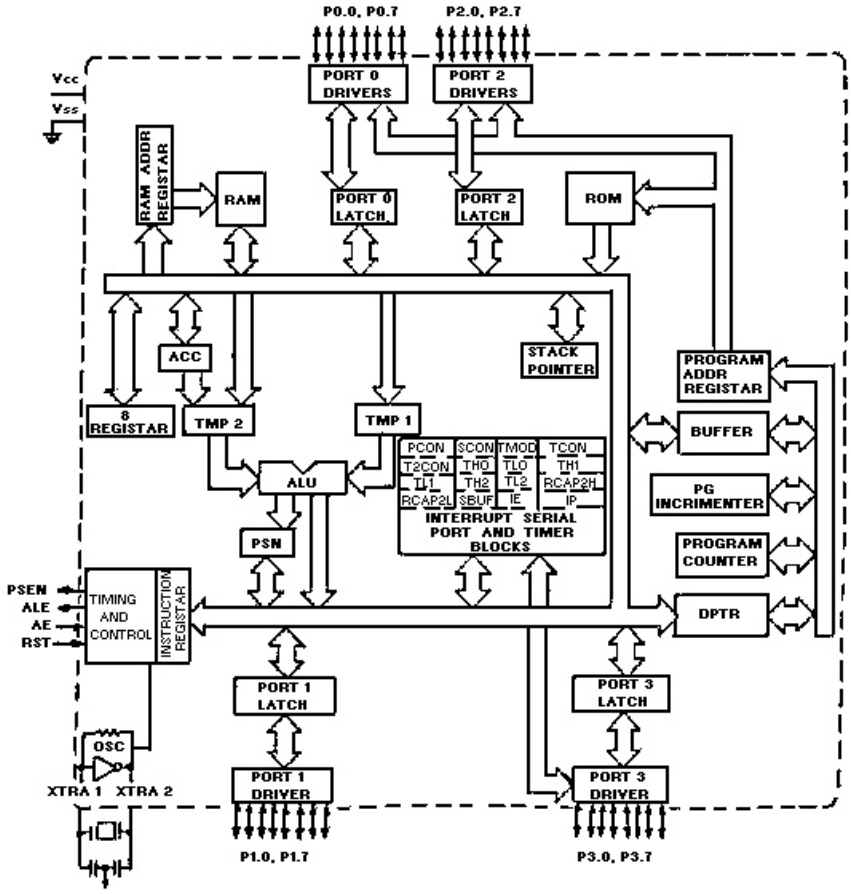
In order to be effective, the Cabinet Grounding Strap must be strapped to the building and/or earth ground.

8-BIT MICROPROCESSOR - U1
19A705557P1 (P80C32)



FUNCTION DIAGRAM

FUNCTION DIAGRAM



MICROCOMPUTER ABBREVIATIONS

PORT: PART OF THE I/O SECTION OF A PROCESSOR
P12, P1.2, P1-2 } MEANS PORT 1 BIT 2

RST: RESET PROGRAM COUNTER TO 0

RXD: RECEIVE DATA (SERIAL)

TXD: TRANSMIT DATA (SERIAL)

INT0: INTERRUPT 0

T0: INTERRUPT INPUT USUALLY USED FOR TESTING

WR: WRITE DATA TO EXTERNAL MEMORY

RD: READ DATA FROM AN EXTERNAL MEMORY

XTAL: CRYSTAL INPUT TO INTERNAL OSCILLATOR

EA: ENABLE

ALE: ADDRESS LATCH ENABLE OUTPUT USED FOR LATCHING

PROG: PROGRAMMABLE I/O STROBE

PSEN: PROGRAM STORE ENABLE USUALLY USED WITH EXTERNAL MEMORY

SS: SINGLE STEP USED FOR SINGLE STEPPING A PROGRAM

DB: DATA BUS

VSS: CIRCUIT GROUND POTENTIAL

VCC: + ? VOLTS POWER SUPPLY DURING OPERATION PROGRAMMING, & VERIFICATION

VPD: STANDBY POWER TO INTERNAL RAM

CS: CHIP SELECT-ENABLES INPUTS & OUTPUTS

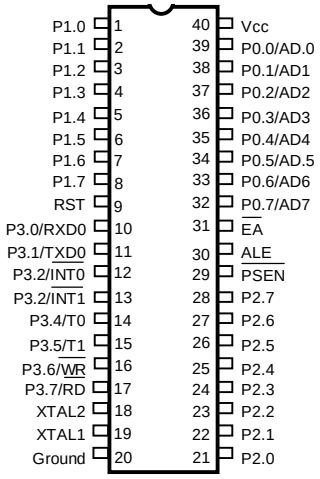
CE: CHIP ENABLE-ENABLES THE CHIP

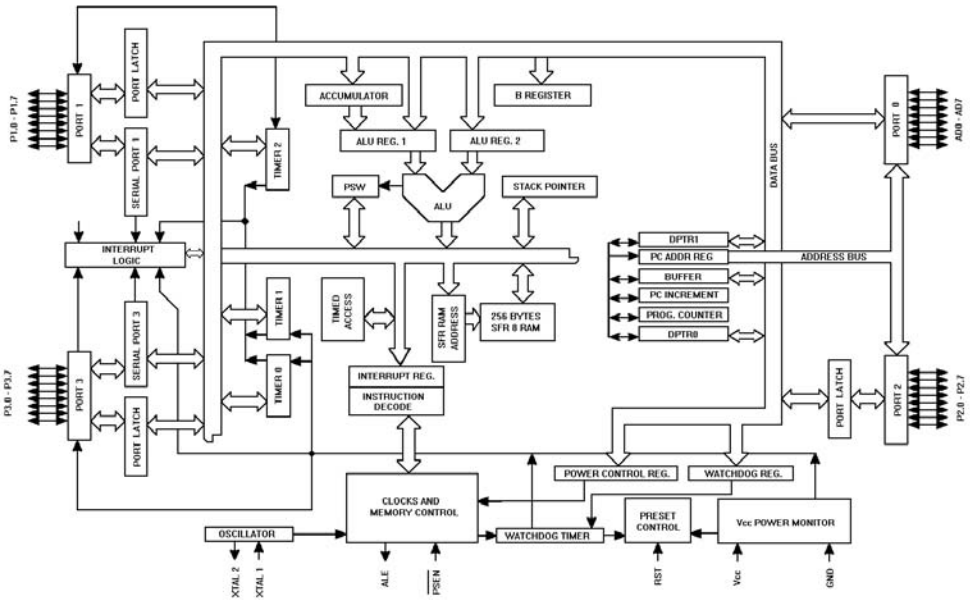
OE: OUTPUT ENABLE-ENABLES THE OUTPUTS

VPP: SUPPLY VOLTAGE DURING PROGRAMMING

PGM: PROGRAMMING-USED FOR PROGRAMMING

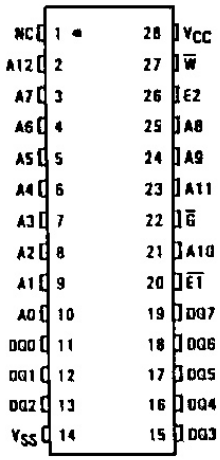
U1 - 8-BIT MICROPROCESSOR
RYT 121 6060/A (80C320)





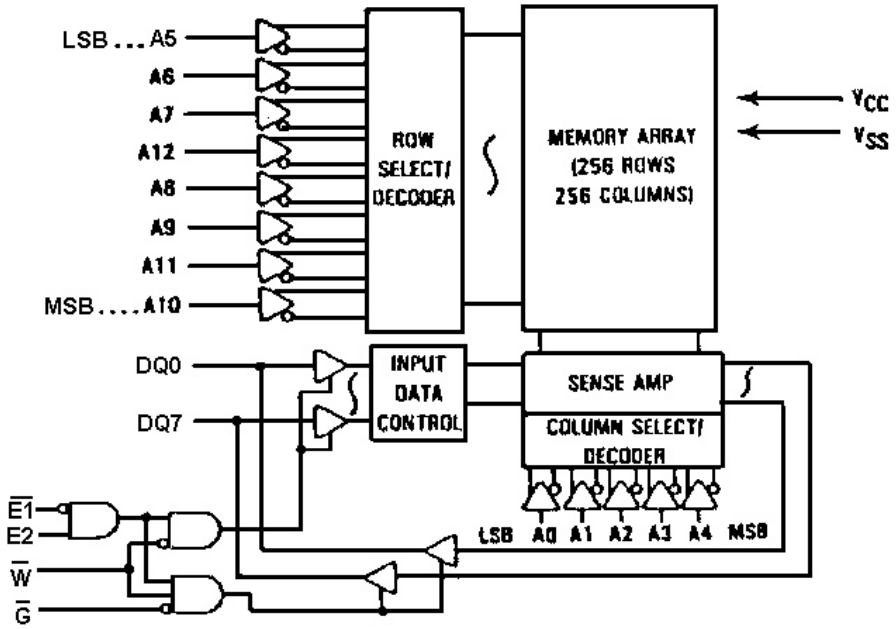
U3 - DIGITAL 8K X8 RAM
19A705558P12

PIN ASSIGNMENT

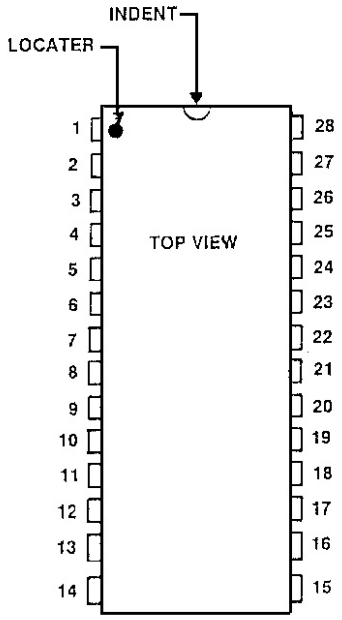


PIN NAMES	
A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



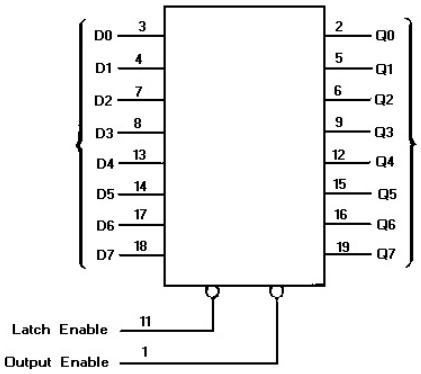
MODEM - U4/U19
19A704727P4



PIN NAME	28 PACK PIN	DESCRIPTION
RE	1	READ ENABLE (ACTIVE LOW)
EN	2	CHIP ENABLE (ACTIVE LOW)
RESOUT	3	RESET OUTPUT (ACTIVE HIGH)
AD0	4	BI-DIRECTIONAL ADDRESS/DATA BUS
AD1	5	BI-DIRECTIONAL ADDRESS/DATA BUS
AD2	6	BI-DIRECTIONAL ADDRESS/DATA BUS
AD3	7	BI-DIRECTIONAL ADDRESS/DATA BUS
AD4	8	BI-DIRECTIONAL ADDRESS/DATA BUS
AD5	9	BI-DIRECTIONAL ADDRESS/DATA BUS
AD6	10	BI-DIRECTIONAL ADDRESS/DATA BUS
AD7	11	BI-DIRECTIONAL ADDRESS/DATA BUS
ALE	12	ADDRESS LATCH ENABLE (ACTIVE HIGH)
VSS	13	GROUND
CLK1	14	BUFFERED OSCILLATOR OUTPUT
VDD	15	POWER SUPPLY
XTAL1	16	OSCILLATOR INPUT
XTAL2	17	OSCILLATOR OUTPUT
CLK2	18	640 KHZ OUTPUT
DATAIN	19	RECEIVED DATA INPUT
SAT/G1	20	RECEIVED SAT INPUT/G1 EN. HC138 (ACT. HI)
TXDAT	21	TRANSMIT DATA OUTPUT
RCVCLK/Q2	22	RECOVERED CLOCK OUTPUT/Q2 OUTPUT FOR HC138
RCVDAT/Q0	23	RECOVERED DATA OUTPUT/Q0 OUTPUT FOR HC138
INT	24	INTERRUPT REQUEST (ACTIVE LOW O.D.)
RESIN	25	RESET INPUT (ACTIVE HIGH)
CS	26	CHIP SELECT (ACTIVE LOW)
CLK3/4	27	TRANSMIT CLOCK OUTPUT/CLK1/6 OUTPUT
WR	28	WRITE ENABLE (ACTIVE LOW)

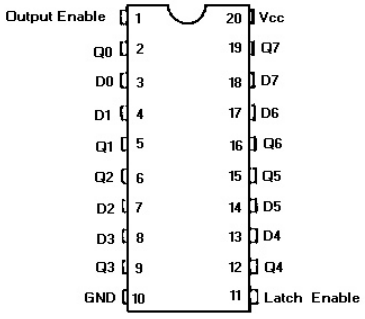
OCTAL DATA LATCH - U5
19A703471P2 (74HC373)

BLOCK DIAGRAM



Pin 20 = Vcc
Pin 10 = GND

PIN ASSIGNMENT



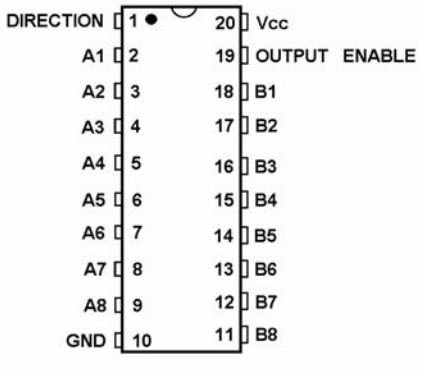
FUNCTION TABLE

Output Enable	Latch Enable	D	Output
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

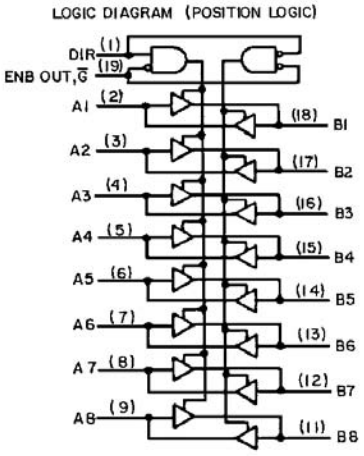
X = don't care
Z = high impedance

U6 - OCTAL TRI-STATE TRANSCEIVER
19A703471P8 (74HC245)

PIN ASSIGNMENT



LOGIC DIAGRAM (POSITION LOGIC)



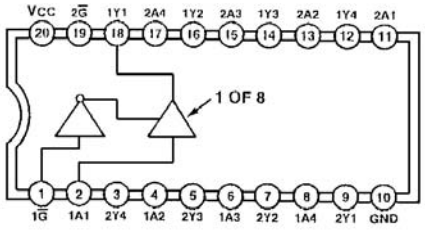
PIN 10 = GND
PIN 20 = Vcc

FUNCTION TABLE

CONTROL INPUTS		OPERATION
OUTPUT ENABLE	DIRECTION	
L	L	DATA TRANSMITTED FROM BUS B TO BUS A
L	H	DATA TRANSMITTED FROM BUS A TO BUS B
H	X	BUSES ISOLATOR (HIGH IMPEDANCE STATE)

X=DON'T CARE

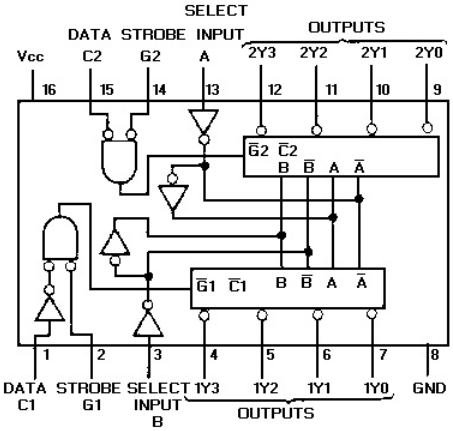
U7/U8/U9 - OCTAL TRI-STATE BUFFER
19A703471P1 (74HC244)



$\overline{1G}$	1A	1Y	$\overline{2G}$	2A	2Y
0	0	0	0	0	0
0	1	1	0	1	1
1	0	Z	1	0	Z
1	1	Z	1	1	Z

Z = HIGH IMPEDANCE

U10 - DUAL 2-TO-1 DECODER/DEMULTIPLEXER
19A700037P363 (74LS155)

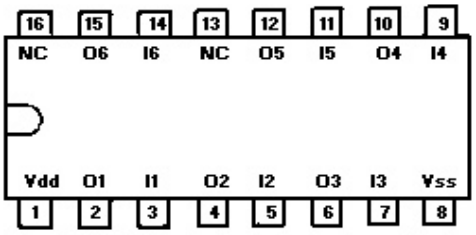


2-Line-to-4-Line Decoder
or 1-Line-to-4-Line Demultiplexer

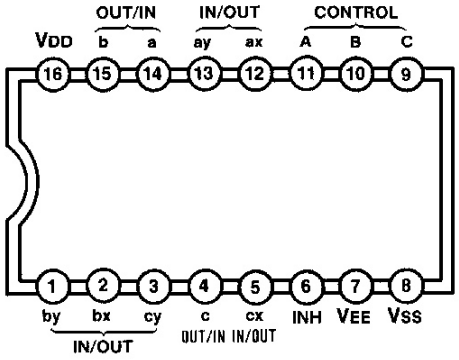
Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

U11/U12/U13/U29
HEX INVERTING BUFFER/CONVERTER
19A700176P1 (4049UB)

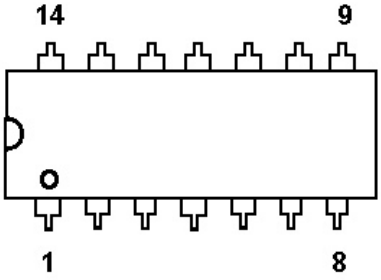


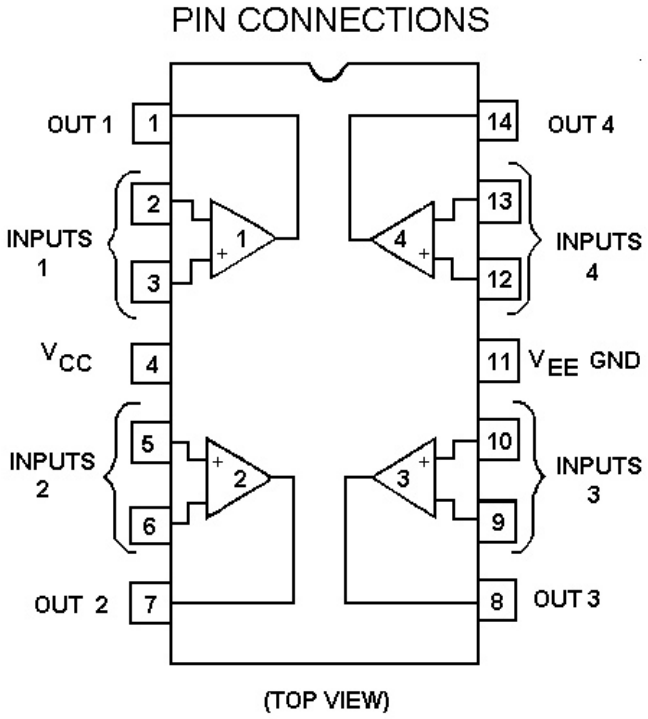
U15/U34
CMOS TRIPLE 2 CHANNEL
MULTIPLEXER
19A700029P38 (4053)



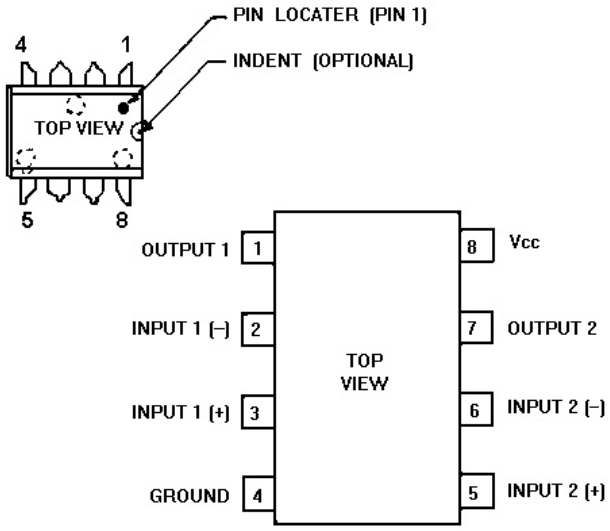
INPUT					"ON" CHANNELS		
INH	C	B	A		c	b	a
1	x	x	x		NONE	NONE	NONE
0	0	0	0		CX	BX	AX
0	0	0	1		CX	BX	AY
0	0	1	0		CX	BY	AX
0	0	1	1		CX	BY	AY
0	1	0	0		CY	BX	AX
0	1	0	1		CY	BX	AY
0	1	1	0		CY	BY	AX
0	1	1	1		CY	BY	AY

U16/U30/U32/U33/U37
QUAD OPERATIONAL AMPLIFIER
19A704883P1 (MC3303P)

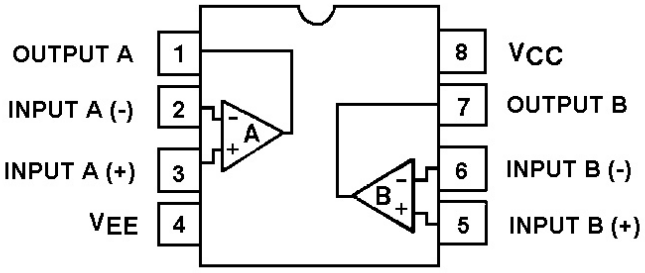




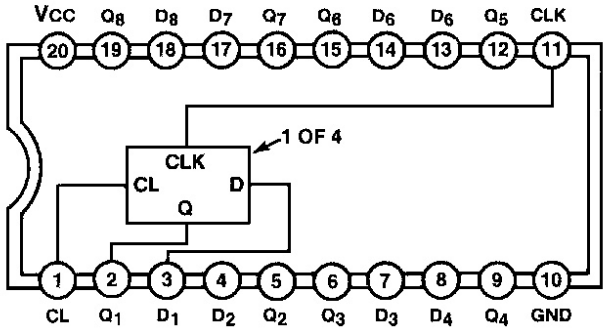
U17/U31
DUAL VOLTAGE COMPARATOR
19A134764P2 (LM393N)



U18
DUAL OPERATIONAL AMPLIFIER
19A700086P4 (4558)



U20/U21/U38
CMOS OCTAL DATA FLIP-FLOP
19A704380P11 (74HC273)

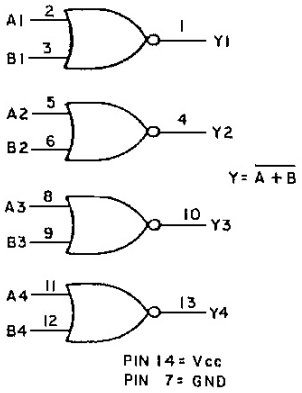


INPUTS		OUTPUTS	
CLEAR	CLOCK	D	Q
Ø	X	X	Ø
1		1	1
1		Ø	Ø
1	Ø	X	Q_0

X = DON'T CARE Q_0 = Q BEFORE

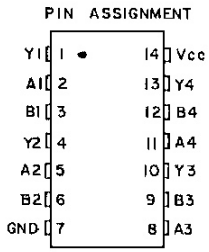
U22
CMOS QUAD 2-INPUT NOR GATE
19A703483P1 (74HC02)

LOGIC DIAGRAM



$Y = \overline{A + B}$

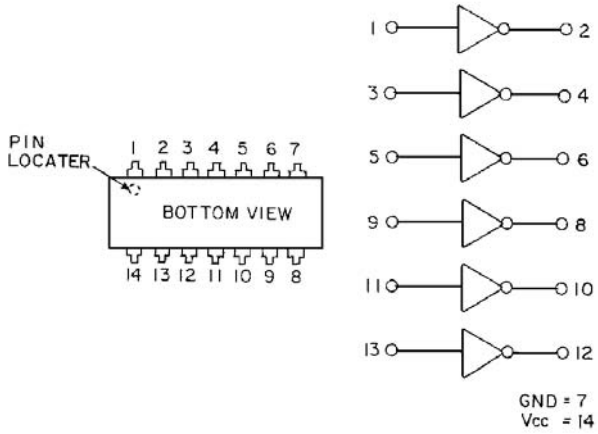
PIN ASSIGNMENT



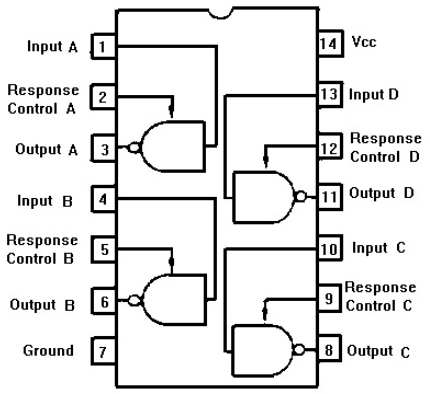
FUNCTION DIAGRAM

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

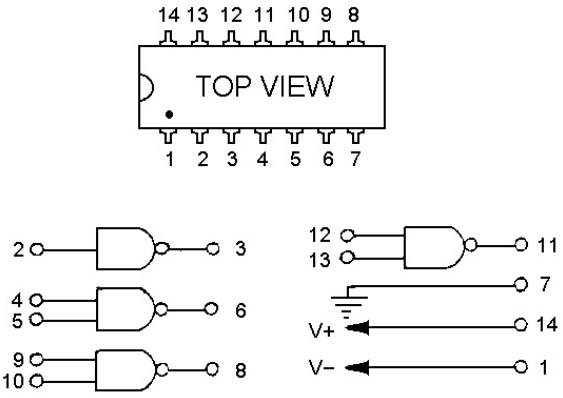
U23/U24/U25/U26
HEX OPEN COLLECTOR INVERTER
19A116180P75 (7406)



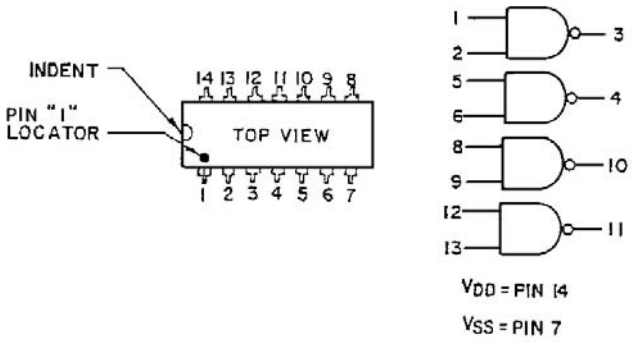
U27
QUAD LINE RECEIVER
19A116704P2 (1489)



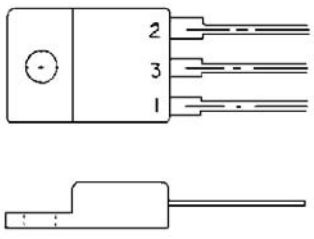
U14/U28
QUAD LINE DRIVER
19A116704P1 (1488)



U42
QUAD 2-INPUT NAND GATE
19A700029P7)

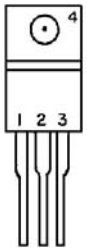


U39
-12 VOLT REGULATOR
19A134718P2 (A7912U)



1. COMMON
2. OUTPUT
3. INPUT

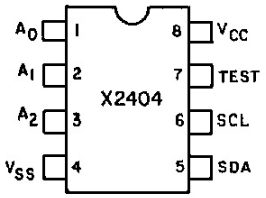
U40
12 VOLT REGULATOR
19A134717P2 (MC7812CT)



1. INPUT
2. COMMON
3. OUTPUT
4. TAB COMMON

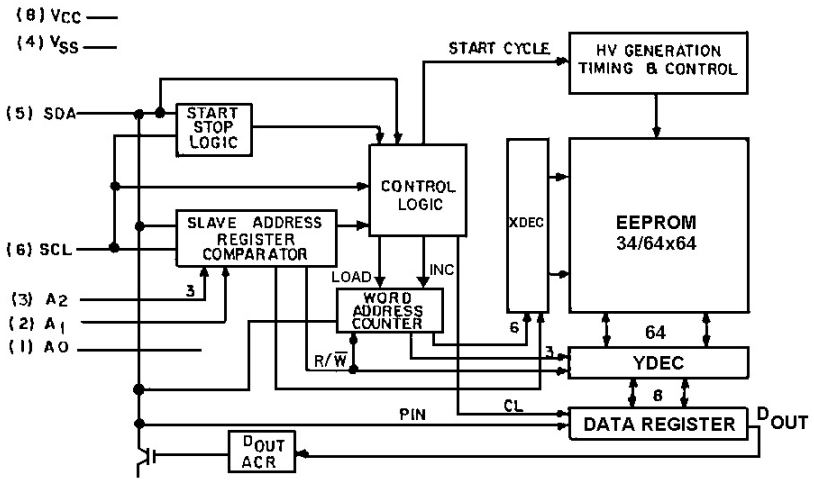
U35
EEPROM
19A704724P3 (MC3303P)

PIN CONFIGURATION



1 A_0 → TO V_{SS}
2 AND 3 A AND A ADDRESS INPUTS
4 V_{SS}
5 SDA SERIAL DATA — I^2C
6 SCL SERIAL CLOCK — BUS
7 TEST INPUT — TO V_{SS}
8 V_{CC}

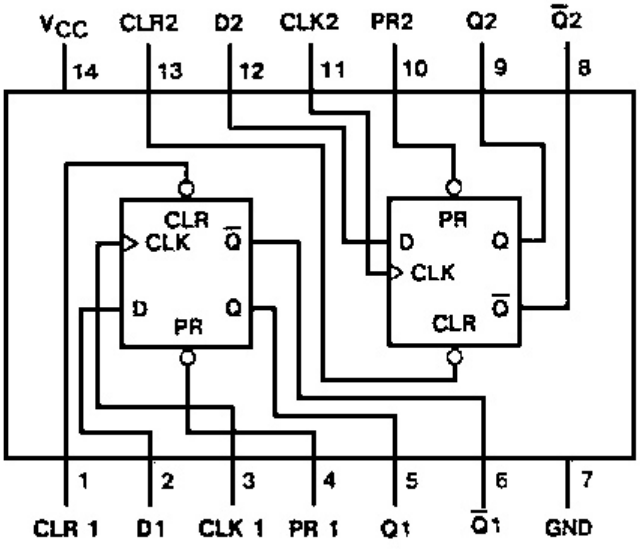
FUNCTION DIAGRAM



U41
DUAL DATA FLIP-FLOP
19A700037P335 (74LS74A)

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

Notes: Q0 = the level of Q before the indicated input conditions were established.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



GETC SHELF ASSEMBLY
19D901868G3
19D901868G4

SYMBOL	PART NUMBER	DESCRIPTION
		---------- ASSEMBLIES -------
A1		**GETC LOGIC BOARD 19D904266G1 (Used in G3) 19D904266G4 (Used in G4)**
		---------- CAPACITORS -------
C1 and C2	19A701624P118	Ceramic: 27 pF ±5%, 500 VDCW, temp coef N80 ±30 PPM/°C.
C3	19A702250P111	Polyester: .047 µF ±10%, 50 VDCW.
C5	19A701534P3	Tantalum: 0.47 µF ± 20%, 35 VDCW.
C6*	T644ACP247J	Polyester: .0047 µF ±5%, 50 VDCW.
C7*	T644ACP310J	Polyester: .010 µF ±5%, 50 VDCW.
C8*	T644ACP210J	Polyester: .0010 µF ±5%, 50 VDCW.
C9*	T644ACP310J	Polyester: .010 µF ±5%, 50 VDCW.
C10	19A701534P19	Tantalum: 47 µF ±20%, 16 VDCW.
C11 thru C13	19A701534P8	Tantalum: 22 µF ±20%, 16 VDCW.
C14 thru C26	T644ACP310K	Polyester: .010 µF ±10%, 50 VDCW.
C29	19A701534P7	Tantalum: 10 µF ±20%, 16 VDCW.
C30 thru C34	T644ACP310J	Polyester: .010 µF ±5%, 50 VDCW.
C35	19A701534P7	Tantalum: 10 µF ±20%, 16 VDCW.
C36	19A701534P9	Tantalum: 47 µF ±20%, 6.3 VDCW.
C37 thru C41	T644ACP310J	Polyester: .010 µF ±5%, 50 VDCW.
C47	19A701534P7	Tantalum: 10 µF ±20%, 16 VDCW.
C48	T644ACP310K	Polyester: .010 µF ±10%, 50 VDCW.
C49	19A701534P7	Tantalum: 10 µF ±20%, 16 VDCW.
C51	19A701534P7	Tantalum: 10 µF ±20%, 16 VDCW.
C52	T644ACP310K	Polyester: .010 µF ±10%, 50 VDCW.
C53	19A701534P7	Tantalum: 10 µF ±20%, 16 VDCW.
C54	5496267P20	Tantalum: 47 µF ± 20%, 35 VDCW; sim to Sprague Type 150D.
C55	19A701534P2	Tantalum: 0.22 µF ±20%, 35 VDCW.
C56	19A701534P4	Tantalum: 1 µF ± 20%, 35 VDCW.
C57	19A701534P8	Tantalum: 22 µF ±20%, 16 VDCW.
C58	19A701534P6	Tantalum: 4.7 µF ±20%, 35 VDCW.
C59	19A701534P8	Tantalum: 22 µF ±20%, 16 VDCW.
C60	19A701534P6	Tantalum: 4.7 µF ±20%, 35 VDCW.
C61 and C62	19A701534P8	Tantalum: 22 µF ±20%, 16 VDCW.
C63	19A701534P6	Tantalum: 4.7 µF ±20%, 35 VDCW.
C64	19A701534P8	Tantalum: 22 µF ±20%, 16 VDCW.
C65	5496267P20	Tantalum: 47 µF ± 20%, 35 VDCW; sim to Sprague Type 150D.
C66 thru C69	19A703314P4	Electrolytic: 47 µF -10+50% tol, 16 VDCW; sim to Panasonic LS Series.
C70 thru C93	T644ACP310K	Polyester: .010 µF ±10%, 50 VDCW.
C94*	T644ACP247J	Polyester: .0047 µF ±5%, 50 VDCW.
C95*	T644ACP310J	Polyester: .010 µF ±5%, 50 VDCW.
C96*	T644ACP210J	Polyester: .0010 µF ±5%, 50 VDCW.
C97*	T644ACP310J	Polyester: .010 µF ±5%, 50 VDCW.
C98	19A701534P19	Tantalum: 47 µF ±20%, 16 VDCW.
C99*	19A701534P8	Tantalum: 22 µF ±20%, 16 VDCW.
C100	T644ACP310K	Polyester: .010 µF ±10%, 50 VDCW.
C103 and C104	5496267P20	Tantalum: 47 µF ± 20%, 35 VDCW; sim to Sprague Type 150D.
		---------- DIODES ----------
D3 thru D8	19A700028P1	Silicon: 75 mA, 75 PIV; sim to 1N4148.
D9	19A700025P2	Silicon, zener: 400 mW max; sim to BZX55-C2V7.
D10 thru D13	19J706030P2	Silicon: sim to 1N4736A.
D14 thru D17	19A700028P1	Silicon: 75 mA, 75 PIV; sim to 1N4148.
D19 thru D21	19A700028P1	Silicon: 75 mA, 75 PIV; sim to 1N4148.
D22 and D23	T324ADP1041	Silicon: Rectifier; sim to 1N4004.
D24 thru D28	19A700028P1	Silicon: 75 mA, 75 PIV; sim to 1N4148.
D29 thru D35	T324ADP1041	Silicon: Rectifier; sim to 1N4004.
D36	19A700028P1	Silicon: 75 mA, 75 PIV; sim to 1N4148.
D37	19A700025P7	Silicon, zener: 400 mW max; sim to BZX55-C5V6.
		---------- LEDS ----------
H1 thru H7	162B3011P0002	Light Emitting Diode: Red; sim to GE 22L-2.
		---------- JACKS ----------
J3	19A705181P1	Connector: 64 contacts; sim to Burndx Cat. RP196B32R1G02Z1.
J6 and J7	19A704852P146	Connector, header: 16-pin, right-angle mount; sim to Molex 22-12-2164.
J8 and J9	19A704852P136	Connector, printed wire, two part: 6 contacts; sim to Dupont Berg 22-12-2064.
J10	19A116659P173	Printed wire, two part: 4 contacts, sim to Molex 09-75-1041.

* COMPONENTS ADDED, DELETED, OR CHANGED BY PRODUCTION CHANGES

SYMBOL	PART NUMBER	DESCRIPTION
J11 thru J18	19A703248P12	Post: Gold Plated, 13 mm length.
J19	19A704852P136	Connector, printed wire, two part: 6 contacts; sim to Dupont Berg 22-12-2064.
J20 and J21	19A703248P12	Post: Gold Plated, 13 mm length.
J24 thru J26	19A703248P12	Post: Gold Plated, 13 mm length.
J27	19A704852P136	Connector, printed wire, two part: 6 contacts; sim to Dupont Berg 22-12-2064.
J28 and J29	19A703248P12	Post: Gold Plated, 13 mm length.
J40	19A703248P12	Post: Gold Plated, 13 mm length.
J44	19A703248P12	Post: Gold Plated, 13 mm length.
J46 thru J48	19A703248P12	Post: Gold Plated, 13 mm length.
J49	19A704779P59	Connector, printed wiring: 10 contacts; sim to Molex 22-18-2103.
J50 thru J55	19A703248P12	Post: Gold Plated, 13 mm length.
J60 thru J69	19A703248P12	Post: Gold Plated, 13 mm length.
J71 thru J74	19A703248P12	Post: Gold Plated, 13 mm length.
		- - - - - - - - - - INDUCTORS - - - - - - - -
L1 thru L3	19A704921P1	Coil.
		- - - - - - - - - - - PLUGS - - - - - - - - - -
P11 thru P18	19A702104P2	Connector: Shorting Jumper, Gold Plated. (Housing Color: White).
P21	19A702104P2	Connector: Shorting Jumper, Gold Plated. (Housing Color: White).
P24 thru P26	19A702104P2	Connector: Shorting Jumper, Gold Plated. (Housing Color: White).
P28 and P29	19A702104P2	Connector: Shorting Jumper, Gold Plated. (Housing Color: White).
P44	19A702104P2	Connector: Shorting Jumper, Gold Plated. (Housing Color: White).
P46 thru P48	19A702104P2	Connector: Shorting Jumper, Gold Plated. (Housing Color: White).
P50 thru P54	19A702104P2	Connector: Shorting Jumper, Gold Plated. (Housing Color: White).
P60 thru P62	19A702104P2	Connector: Shorting Jumper, Gold Plated. (Housing Color: White).
P67 thru P69	19A702104P2	Connector: Shorting Jumper, Gold Plated. (Housing Color: White).

SYMBOL	PART NUMBER	DESCRIPTION
P71 thru P74	19A702104P2	Connector: Shorting Jumper, Gold Plated. (Housing Color: White).
		- - - - - - - - - - TRANSISTORS - - - - - -
Q2 thru Q6	19A700023P2	Silicon, NPN: sim to 2N3904.
Q7	19A702503P2	Silicon, NPN: sim to 2N4401.
Q8 thru Q10	19A700023P2	Silicon, NPN: sim to 2N3904.
Q11	19A700022P2	Silicon, PNP: sim to 2N3906.
Q12	19A116375P1	Silicon, PNP.
Q13	19A700054P1	Silicon, NPN, 60 w; sim to BD-201.
Q14 and Q15	19A700023P2	Silicon, NPN: sim to 2N3904.
Q16	19A702503P2	Silicon, NPN: sim to 2N4401.
Q17	19A700022P2	Silicon, PNP: sim to 2N3906.
Q18	19A700023P2	Silicon, NPN: sim to 2N3904.
		- - - - - - - - - - RESISTORS - - - - - - - -
R1	19B800784P106	Variable: 5K ohms ±20%, 1/2 w.
R2	19B800784P105	Variable: 1K ohms ±20%, 350 VDCW, .5 w.
R6 and R7	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R8 and R9	19A701630P2	Resistor, network: 9 resistors rated 10K ohms ±2%, 50 VDCW; sim to Bourns 4310R-101-103.
R10	H212CRP510C	Deposited carbon: 1M ohms ±5%, 1/4 w.
R12	19A701537P1	Composition: 10M ohms ±5%, 1/4 w.
R13	19A701250P446	Metal film: 294K ohm ± 1%, 250 VDCW, 1/4 w.
R14	H212CRP322C	Deposited carbon: 22K ohms ±5%, 1/4 w.
R15	19A701537P1	Composition: 10M ohms ±5%, 1/4 w.
R16	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R17	19A701250P273	Metal film: 5.6K ohms ±1%, 250 VDCW, 1/4 w
R18	H212CRP147C	Deposited carbon: 470 ohms ±5%, 1/4 w.
R19	19A701250P301	Metal film: 10K ohms ± 1%, 1/4 w.
R20 and R21	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R22	19A701537P1	Composition: 10M ohms ±5%, 1/4 w.
R25 and R26	H212CRP347C	Deposited carbon: 47K ohms ±5%, 1/4 w.
R27	19A701250P269	Metal film: 5.11K ohms ±1%, 1/4 w.
R28	19A701250P201	Metal film: 1K ohms ±1%, 250 VDCW, 1/4 w.
R29	19A701250P322	Metal film: 16.5K ohms ±1%, 250 VDCW, 1/4 w.
R30	19A701250P210	Metal film: 1240 ohms ±1%, 250 VDCW, 1/4 w
R31	19B235029P8	Variable: 10K ohms, ±10%, 1/2 w.
R32	H212CRP510C	Deposited carbon: 1M ohms ±5%, 1/4 w.

SYMBOL	PART NUMBER	DESCRIPTION
R33	H212CRP239C	Deposited carbon: 3.9K ohms ±5%, 1/4 w.
R36	19A701250P176	Metal film: 604 ohms ±1%, 1/4 w.
R38	H212CRP122C	Deposited carbon: 220 ohms ±5%, 1/4 w.
R39 and R40	19A701630P2	Resistor, network: 9 resistors rated 10K ohms ±2%, 50 VDCW; sim to Bourns 4310R-101-103.
R41	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R42	H212CRP222C	Deposited carbon: 2.2K ohms ±5%, 1/4 w.
R43	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R44 thru R53	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R54 thru R59	H212CRP156C	Deposited carbon: 560 ohms ±5%, 1/4 w.
R60	H212CRP312C	Deposited carbon: 12K ohms ±5%, 1/4 w.
R61	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R62	H212CRP147C	Deposited carbon: 470 ohms ±5%, 1/4 w.
R63	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R64	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R67	H212CRP247C	Deposited carbon: 4.7K ohms ±5%, 1/4 w.
R68	H212CRP318C	Deposited carbon: 18K ohms ±5%, 1/4 w.
R69	19A701250P388	Metal film: 80.6K ohms ± 1%, 250 VDCW, 1/4 w.
R70	19A701250P358	Metal film: 2.7 ohms ±5%, 1/4 w.
R71	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R72	19A701250P384	Metal film: 73.2K ohms ±1%, 1/4 w.
R73	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R74	19A701250P391	Metal film: 86.6K ohms ±1%, 1/4 w.
R75	19A701250P325	Metal film: 17.8K ohms ±1%, 1/4 w.
R76	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R77	19A701250P382	Metal film: 69.8K ohms ±1%, 1/4 w.
R78	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R79	19A701250P350	Metal film: 32.4K ohms ±1%, 1/4 w.
R80 thru R83	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R84	H212CRP382C	Deposited carbon: 82K ohms ±5%, 1/4 w.
R85	H212CRP318C	Deposited carbon: 18K ohms ±5%, 1/4 w.
R86	19A701250P388	Metal film: 80.6K ohms ± 1%, 250 VDCW, 1/4 w.
R87	19A701250P358	Metal film: 2.7 ohms ±5%, 1/4 w.
R88	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R89	19A701250P384	Metal film: 73.2K ohms ±1%, 1/4 w.
R90	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R91	19A701250P391	Metal film: 86.6K ohms ±1%, 1/4 w.
R92	19A701250P325	Metal film: 17.8K ohms ±1%, 1/4 w.
R93	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R94	19A701250P382	Metal film: 69.8K ohms ±1%, 1/4 w.
R95	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R96	19A701250P350	Metal film: 32.4K ohms ±1%, 1/4 w.
R97 and R98	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R99	H212CRP347C	Deposited carbon: 47K ohms ±5%, 1/4 w.
R100	H212CRP410C	Deposited carbon: 100K ohms ±5%, 1/4 w.
R101	H212CRP368C	Deposited carbon: 68K ohms ±5%, 1/4 w.
R103 thru R105	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R116	19A701250P201	Metal film: 1K ohms ±1%, 250 VDCW, 1/4 w.
R117 and R118	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R119	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R120	H212CRP133C	Deposited carbon: 330 ohms ±5%, 1/4 w.
R121	19A701630P2	Resistor, network: 9 resistors rated 10K ohms ±2%, 50 VDCW; sim to Bourns 4310R-101-103.
R123 thru R125	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R126	19A700113P63	Composition: 1K ohms ± 5%, 1/2 w.
R127	3R77P511J	Composition: 510 ohms ±5%, 1/2 w.
R128	19A700113P19	Composition: 15 ohms ± 5%, 1/2 w.
R129	19A701250P434	Metal film: 221 K ohms ±1%, 250 VDCW, 1 w.
R130	19A700050P13	Wirewound: 1 ohms ± 10%, 2 w.
R131	19A701250P301	Metal film: 10K ohms ± 1%, 1/4 w.
R132	19A701250P266	Metal film: 4.75K ohms ±1%, 1/4 w.
R133	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R134	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R135	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R136	5493035P2	Wirewound: 1 ohm ±5%, 5 w.
R137	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R138	H212CRP315C	Deposited carbon: 15K ohms ±5%, 1/4 w.
R139 and R140	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R141	19B800784P108	Variable: 10K ohms ±20%, 1/2 w.
R142	H212CRP322C	Deposited carbon: 22K ohms ±5%, 1/4 w.
R143	19A701537P1	Composition: 10M ohms ±5%, 1/4 w.
R144	H212CRP347C	Deposited carbon: 47K ohms ±5%, 1/4 w.
R145	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R146	19A701250P176	Metal film: 604 ohms ±1%, 1/4 w.
R147	H212CRP368C	Deposited carbon: 68K ohms ±5%, 1/4 w.

SYMBOL	PART NUMBER	DESCRIPTION
R148	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R149	19A700184P1	Jumper.
R151 and R152	H212CRP312C	Deposited carbon: 12K ohms ±5%, 1/4 w.
R153	H212CRP239C	Deposited carbon: 3.9K ohms ±5%, 1/4 w.
R154 thru R161	H212CRP110C	Deposited carbon: 100 ohms ±5%, 1/4 w.
R163 and R164	H212CRP110C	Deposited carbon: 100 ohms ±5%, 1/4 w.
R168 and R169	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
		- - - - - - - - - - VARISTORS - - - - - - - -
RV1 thru RV13	19A705677P3	Arrester, Electrical Surge (MOV Varistor): Sim to Harris V39ZT1 (marked 39Z1).
		- - - - - - - - - - - SWITCHES - - - - - - - -
S1 thru S3	19B800010P2	Dual-Inline-Package: 8 Circuits; sim to CTS 206-8.
S4	19A701324P1	Push-Button: sim to IEE/Schadown 210091.
		- - - - - - - - TRANSFORMERS - - - -
T1 and T2	19A703656P1	Audio Frequency: sim to Nova Magnetics 5577-06-0001.
		- - - - - INTEGRATED CIRCUITS - - - -
U1	19A705557P1	Digital: 8-Bit Microcomputer; sim to P80C32 (Used in G1).
U1	RYT 121 6060/A	Digital: 8-Bit Microcomputer; sim to P80C320 (used in G4).
U3	19A705558P1	Digital: 8K x 8 RAM; sim to MCM6064P-12.
U4	19A704727P4	Integrated Circuit, Modem.
U5	19A703471P2	Digital: Octal Data Latch; sim to 74HC373.
U6	19A703471P8	Digital: Octal Tri-State Transceiver; sim to 74HC245.
U7 thru U9	19A703471P1	Digital: Octal Tri-State Buffer; sim to 74HC244.
U10	19A700037P363	Digital: Dual 2-to-1 Decoder/ Demultiplexer; sim to 74LS155.
U11 thru U13	19A700176P1	Digital: Hex Inverting Buffer/Converter; sim to 4049UB.
U14	19A116704P1	Digital: Quad Line Driver; sim to 1488.
U15	19A700029P38	Digital: CMOS Triple 2 Channel Multiplexer.
U16	19A704883P1	Linear: Quad Op Amp; sim to MC3303P.
U17	19A134764P2	Linear: Dual Voltage Comparator; sim to LM393N.
U18	19A700086P4	Linear: Dual Op Amp; sim to 4558.
U19	19A704727P4	Integrated Circuit, Modem.

SYMBOL	PART NUMBER	DESCRIPTION
U20 and U21	19A704380P11	Digital: CMOS Octal Data Flip-Flop; sim to 74HC273.
U22	19A703483P1	Digital: CMOS Quad 2-Input NOR Gate; sim to 74HC02.
U23 thru U26	19A116180P75	Digital: Hex Open Collector Inverter; sim to 7406.
U27	19A116704P2	Digital: Quad Line Receiver; sim to 1489.
U28	19A116704P1	Digital: Quad Line Driver; sim to 1488.
U29	19A700176P1	Digital: Hex Inverting Buffer/Converter; sim to 4049UB.
U30	19A704883P1	Linear: Quad Op Amp; sim to MC3303P.
U31	19A134764P2	Linear: Dual Voltage Comparator; sim to LM393N.
U32 and U33	19A704883P1	Linear: Quad Op Amp; sim to MC3303P.
U34	19A700029P38	Digital: CMOS Triple 2 Channel Multiplexer.
U35	19A704724P3	Digital, EEPROM:
U37	19A704883P1	Linear: Quad Op Amp; sim to MC3303P.
U38	19A704380P11	Digital: CMOS Octal Data Flip-Flop; sim to 74HC273.
U39	19A134718P2	Linear: -12 Volt Regulator; sim to uA7912U.
U40	19A134717P2	Linear: 12 Volt Regulator: sim to MC7812CT.
U41	19A700037P335	Digital: Dual Data Flip-Flop; sim to 74LS74A.
U42	19A700029P7	Digital: QUAD 2-INPUT NAND GATE.
		- - - - - - - - - - - SOCKETS - - - - - - - -
XU1	19A700156P5	Socket, IC: 40 Pins, Tin Plated.
XU2 thru XU4	19A700156P3	Socket, IC: 28 Pins, Tin Plated.
XU19	19A700156P3	Socket, IC: 28 Pins, Tin Plated.
XU35	19A700156P15	Socket, IC: 8 Pins, Tin Plated.
		- - - - - - - - - - - CRYSTALS - - - - - - -
Y1	19A702511G15	Quartz: 11.059200 MHz.
		- - - - - - - MISCELLANEOUS - - - - - - -
5	N402P35B6	Washer, Flat.
6	19A703248P12	Post: Gold Plated, 13 mm length.
7	N80P9005B6	Machine screw, pan head, steel, No. 4-40 UNC x 5/16".
8	N404P11B6	Lockwasher, internal tooth: No. 4.
9	7141225P2	Nut, Hex: 4-40.
11	19A134521P1	Lens, red. (XMIT).
12	19A134521P6	Lens.
13	19A702917P7	Heat Sink, Transistor: Sim to Thermalloy Cat 6030B-TT.
14	19B232901P2	Support.
18	19A116837P3	Nut, Clinch.
19	19A700068P1	Insulator, bushing.

SYMBOL	PART NUMBER	DESCRIPTION
A2		**REGULATOR ASSEMBLY 19C336816G2**
		- - - - - - - - - RESISTORS - - - - - - - - -
R1 and R2	5493035P1	Wirewound: 5 ohms ±5%, 5 watt; sim to Hamilton Hall Type HR-5W.
		- - - - - - TERMINAL BOARDS - - - - - -
TB1 and TB2	7775500P11	Phen: 5 terminals.
		- - - - - INTEGRATED CIRCUITS - - - -
U1 and U2	19A134717P1	Linear: 5 Volt Regulator; sim to MC7805CT.
		MISCELLANEOUS PARTS FOR 19D901868G3, G4
2	19C851553G1	Tray.
3	19C851587G1	Shelf Assembly.
7	19A115594P2	Grommet.
9	19A115204P1	Grease.
14	19B235048P1	Ground cable.
15	19B201109P1	Rivet, Blind
18	19B235310P5	Nameplate, Blank.

PRODUCTION CHANGES

Changes in the equipmentto improve performance or to simplify circuits are identified by a "Revision Letter," which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of the parts affected by these revisions.

REV. A - GETC LOGIC BOARD 19D904266G1

To improve the High Speed Filter response for use with Simulcast Systems, the filter capacitors C6 thru C9 and C94 thru C97 were changed as follows:

C6 Changed from T644ACP268J (.0068 µF) to T644ACP247J (.0047 µF).

C7 & C9 Changed from T644ACP315J (.015 µF) to T644ACP310J (.010 µF).

C8 Changed from T644ACP215J (.0015 µF) to T644ACP210J (.0010 µF).

C94 Changed from T644ACP222J (.0022 µF) to T644ACP247J (.0047 µF).

C95 & C97 Changed from T644ACP247J (.0047 µF) to T644ACP310J (.010 µF).

C96 Changed from 19A700233P5 (470 pF) to T644ACP210J (.0010 µF).

REV. B - GETC LOGIC BOARD 19D904266G1

To lenghten the reset pulse from 70 ms to >140 ms when the GETC is powered up:

C99 Changed from 19A701534P7 (10 µF) to 19A701534P8 (22 µF).

GETC LSD FILTER 19C852138P1, Rev. 1

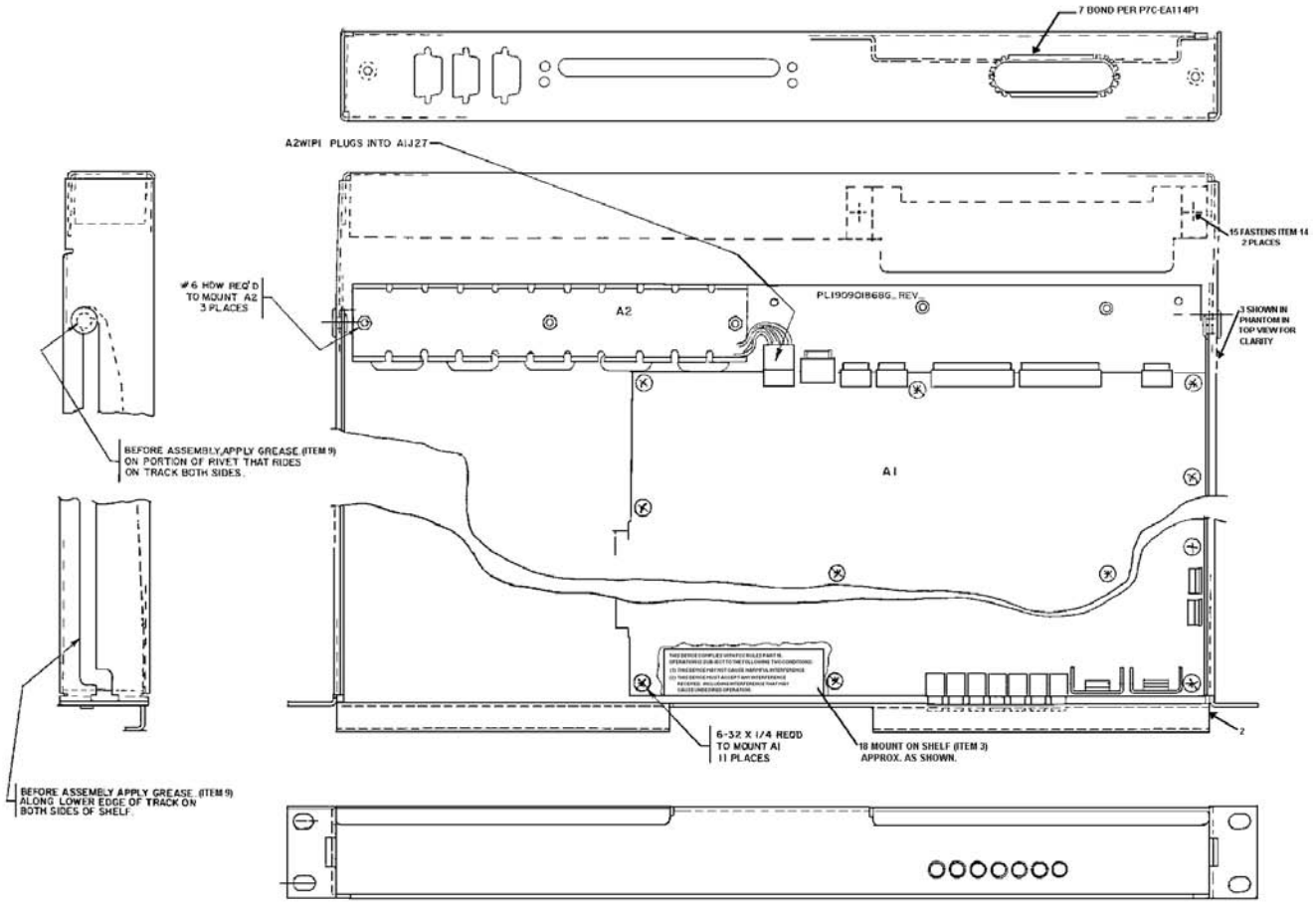
SYMBOL	PART NUMBER	DESCRIPTION
		- - - - - - - - - - CAPACITORS - - - - - - -
C1 and C2	19A705205P2	Tantalum: 1 µF ± 20%, 16 VDCW.
C3 and C5	19A702052P114	Ceramic: .01 µF ±5%, 50 VDCW.
C4	19A700010P5	Ceramic: 560 pF ± 5%, 35 VDCW.
		- - - - - - - - - - RESISTORS - - - - - - - -
R1 and R2	19A702931P301	Metal Film: 10.0K, 1%, 1/8w.
R3	19A702931P389	Metal Film: 82.5K 1%, 1/8w.
R4	19A702931P301	Metal Film: 10.0K, 1%, 1/8w.
R5	19A702931P377	Metal Film: 61.9K, 1%, 1/8w.
R6	19A702931P325	Metal Film: 17.8K, 1%, 1/8w.
R7	19A702931P310	Metal Film: 12.4K, 1%, 1/8w.
R8	19A702931P452	Metal Film: 340K, 1%, 1/8w.
R9	19A702931P314	Metal Film: 13.7K, 1%, 1/8w.
R10	19A702931P373	Metal Film: 56.2K, 1%, 1/8w.
R11	19A702931P301	Metal Film: 10.0K, 1%, 1/8w.
R12	19A702931P432	Metal Film: 210K, 1%, 1/8w.
R13	19A702931P301	Metal Film: 10.0K, 1%, 1/8w.
R14	19A702931P339	Metal Film: 24.9K, 1%, 1/8w.
R15	19A702931P201	Metal Film: 1.0K, 1%, 1/8w.
R16	19A702931P412	Metal Film: 130K, 1%, 1/8w.
R17	19A801251P1	Metal Film: 0 ohms, 1%, 1/8w.
		- - - - - INTEGRATED CIRCUITS - - - -
U1 and U2	LTC1059CS	IC, Switched Cap Filter.
U3	19A704971P4	Linear: -5 Volt Regulator; sim to MC79L05ACD.
U4	19A701865P101	Linear: Timer; sim to NE555.

OPTION SXMK3L - GETC ETSI MODIFICATION KIT
350A1127G1, Rev. 1

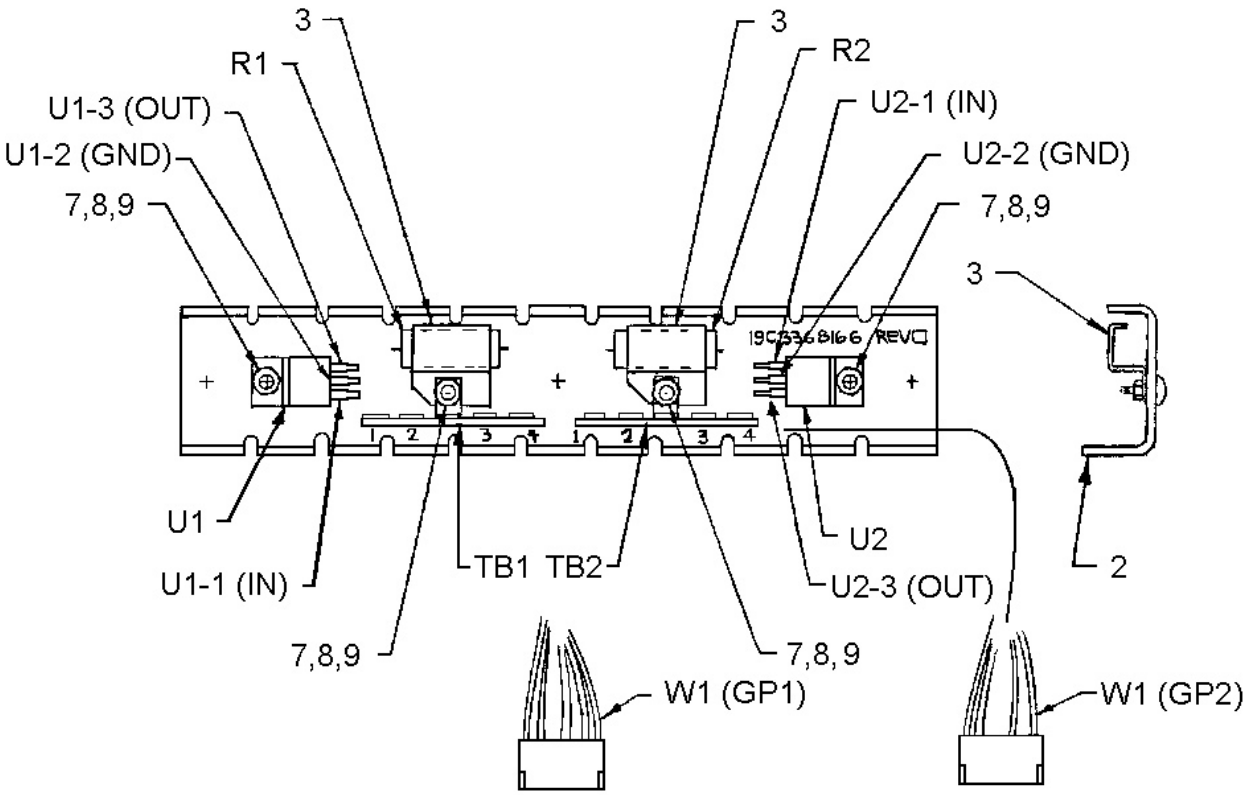
SYMBOL	PART NUMBER	DESCRIPTION
		---------- CAPACITORS ------
C6	T644ACP310J	Polyester: .010 µF ±5%, 50 VDCW.
C7	T644ACP322J	Polyester: .022 µF ±5%, 50 VDCW.
C8	T644ACP215J	Polyester: .0015 µF ±5%, 50 VDCW.
C9	T644ACP315J	Polyester: .015 µF ±5%, 50 VDCW.
C96	19A700233P6	Ceramic: 680 pF ±20%, 50 VDCW.
C97	T644ACP268J	Polyester: .0068 µF ±5%, 50 VDCW.
		---------- RESISTORS --------
R28	19A701250P205	Metal Film: 1.10K, 1%, 1/4w.
R29	19A701250P305	Metal Film: 11.0K 1%, 1/4w.
R30	19A701250P229	Metal Film: 1.96K, 1%, 1/4w.

GETC LIGHTNING-PROTECTION CIRCUITRY GROUNDING KIT
344A4500G1

SYMBOL	PART NUMBER	DESCRIPTION
2	N80P13004B6	Screw, Machine (qty 2).
3	19B209260P1	Solderless Terminal (qty 2).
4	N404P13B6	Lock Washer (qty 4).
5	19A116850P10	Wire, Stranded; 16AWG Black (qty 2 @ 2 ft each).
6	344A4060P1	Connector; Split Bolt (qty 2).



GETC SHELF ASEMBLY
19D901868G3
(19D901868, Sh. 2, Rev. 3)



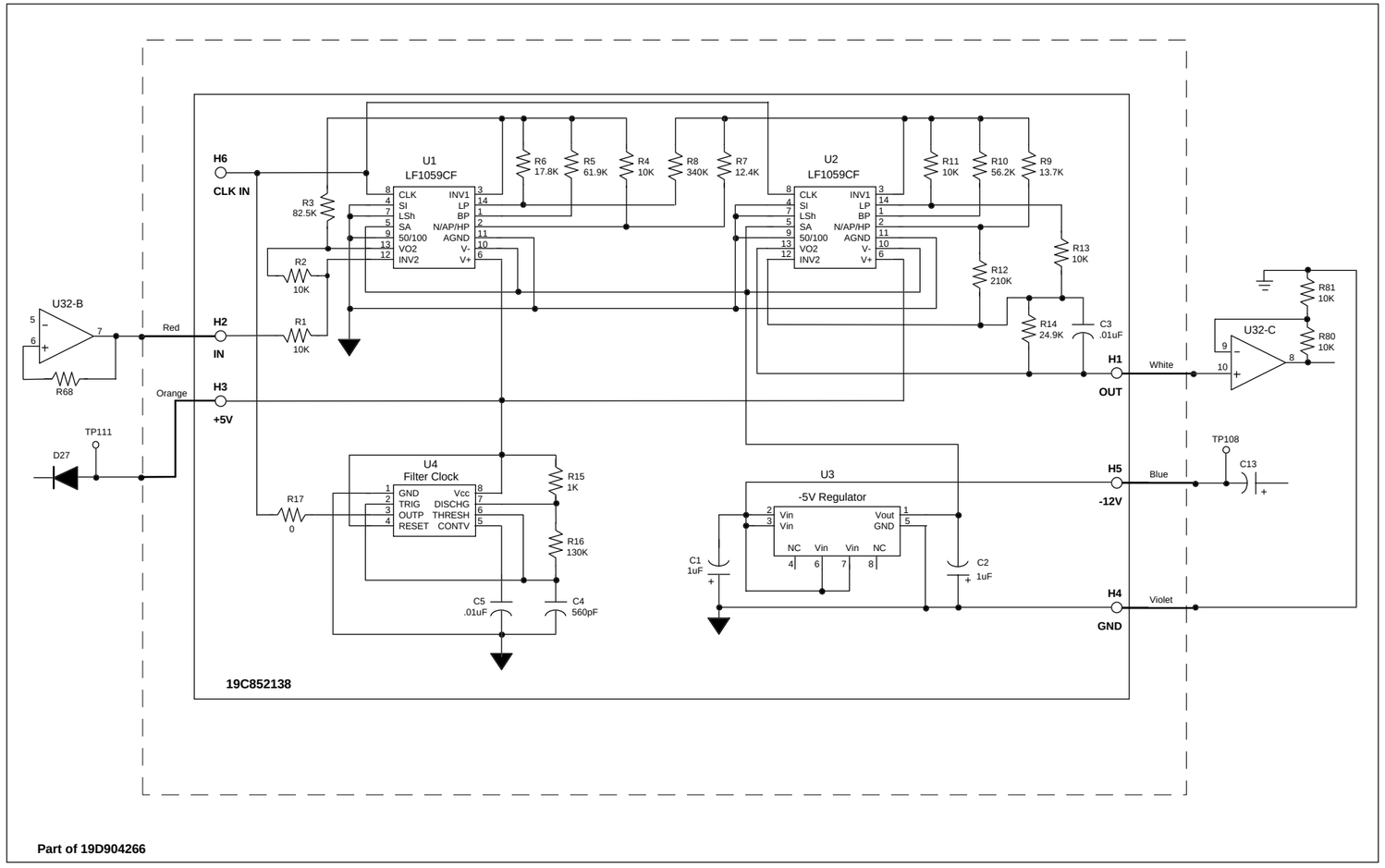
WIRING CHART

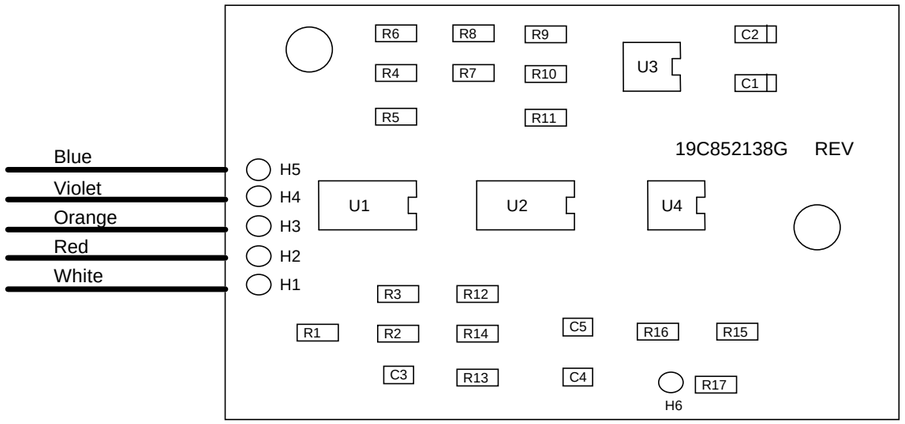
WIRE	FROM	TO	REMARKS
ST22-W	U1-1	TB1-1	+5V R.M. INPUT
R1	TB1-1	TB2-1	
W1-W	W1P1-2	TB1-1	+5V R.M. INPUT
ST22-BK	U1-2	TB1-2	GROUND
ST22-BK	TB1-2	TB2-2	
ST22-BK	U2-2	TB2-2	
W1-BK	W1P1-3	TB1-2	
ST22-R	U1-3	TB1-3	
W1-R	W1P1-1	TB1-3	+5V R.M.
ST22-W	U2-1	TB2-4	+5V INPUT
R2	TB2-1	TB2-4	
W1-W	W1P1-5	TB2-4	
ST22-BR	U2-3	TB2-3	+5V
W1-BR	W1P1-6	TB2-3	
W1-O	W1P1-4	TB2-1	+13.8V

REGULATOR ASEMBLY
19C336816G2
(19C336816, Rev. 6)

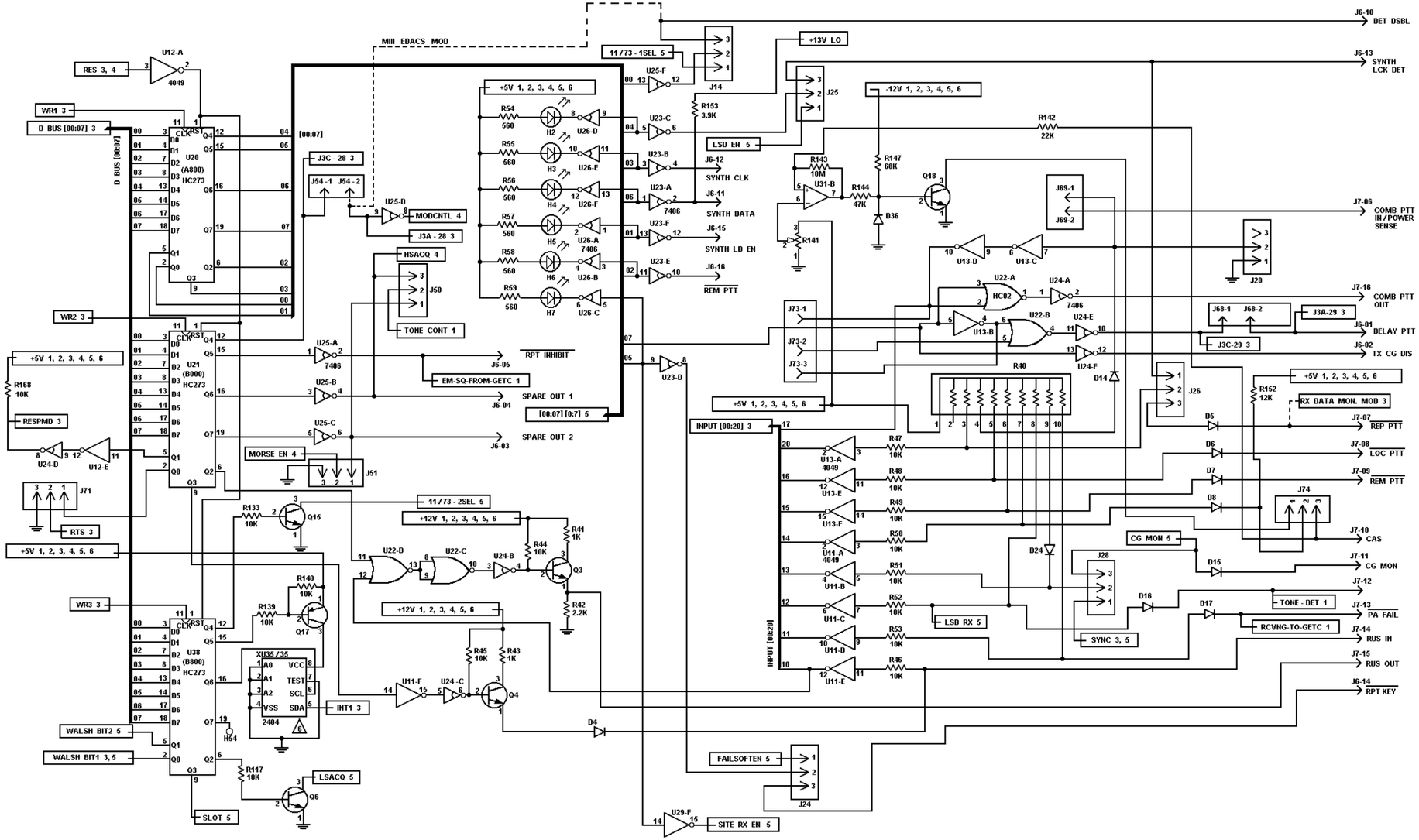
Ericsson Inc.
Private Radio Systems
Mountain View Road
Lynchburg, VA 24502
1-800-528-7711 (Outside USA, 804-528-7711)

Printed in U.S.A.



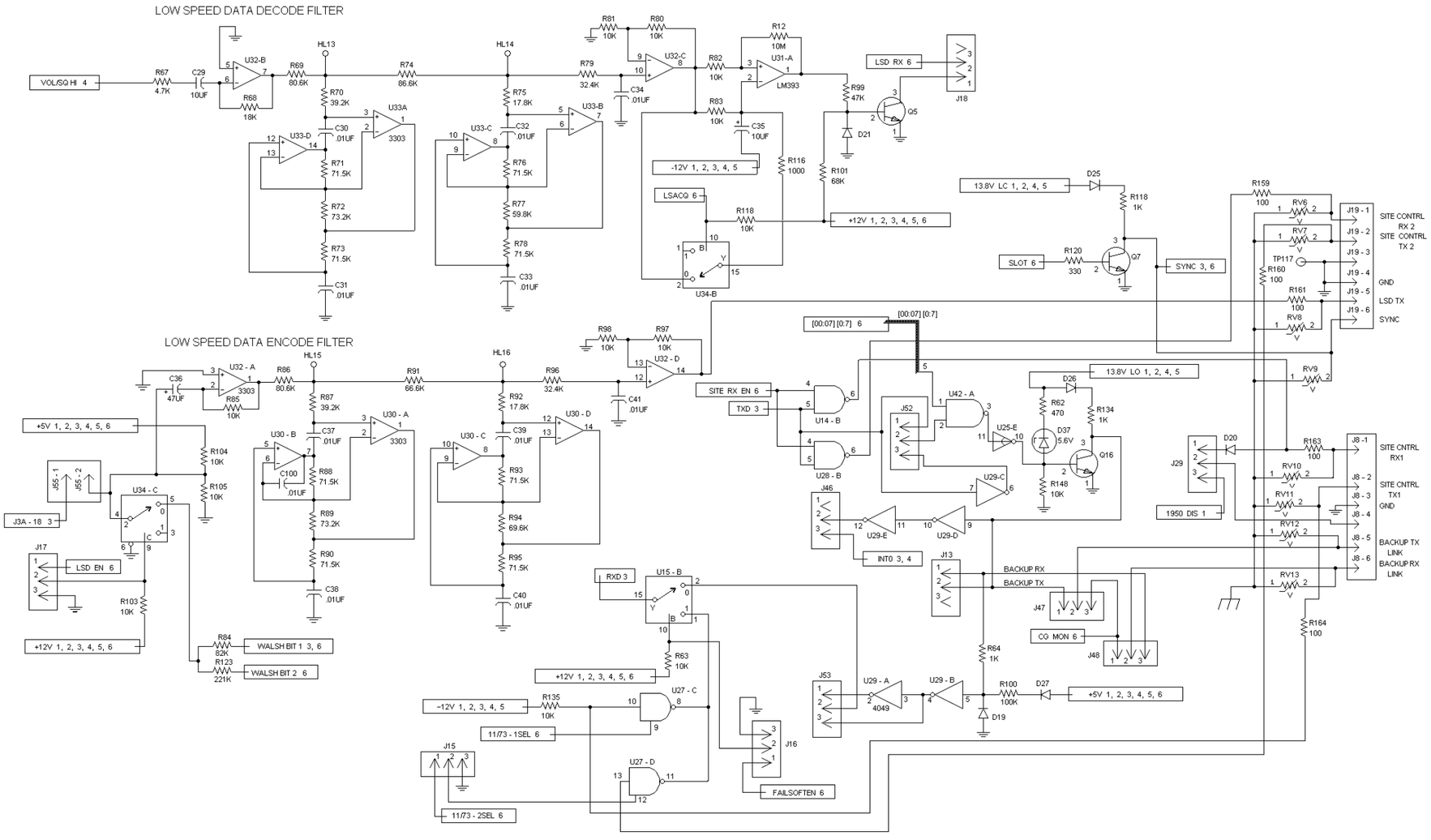


GETC LSD FILTER
19C852138P1
(Made from 19C852136, Sh. 1, Rev. 1 and 19C852138, Sh. 1, Rev. 3)



GETC SHELF ASSEMBLY
19D901868G3 and G4

(19D904198, Sh. 6, Rev. 5)



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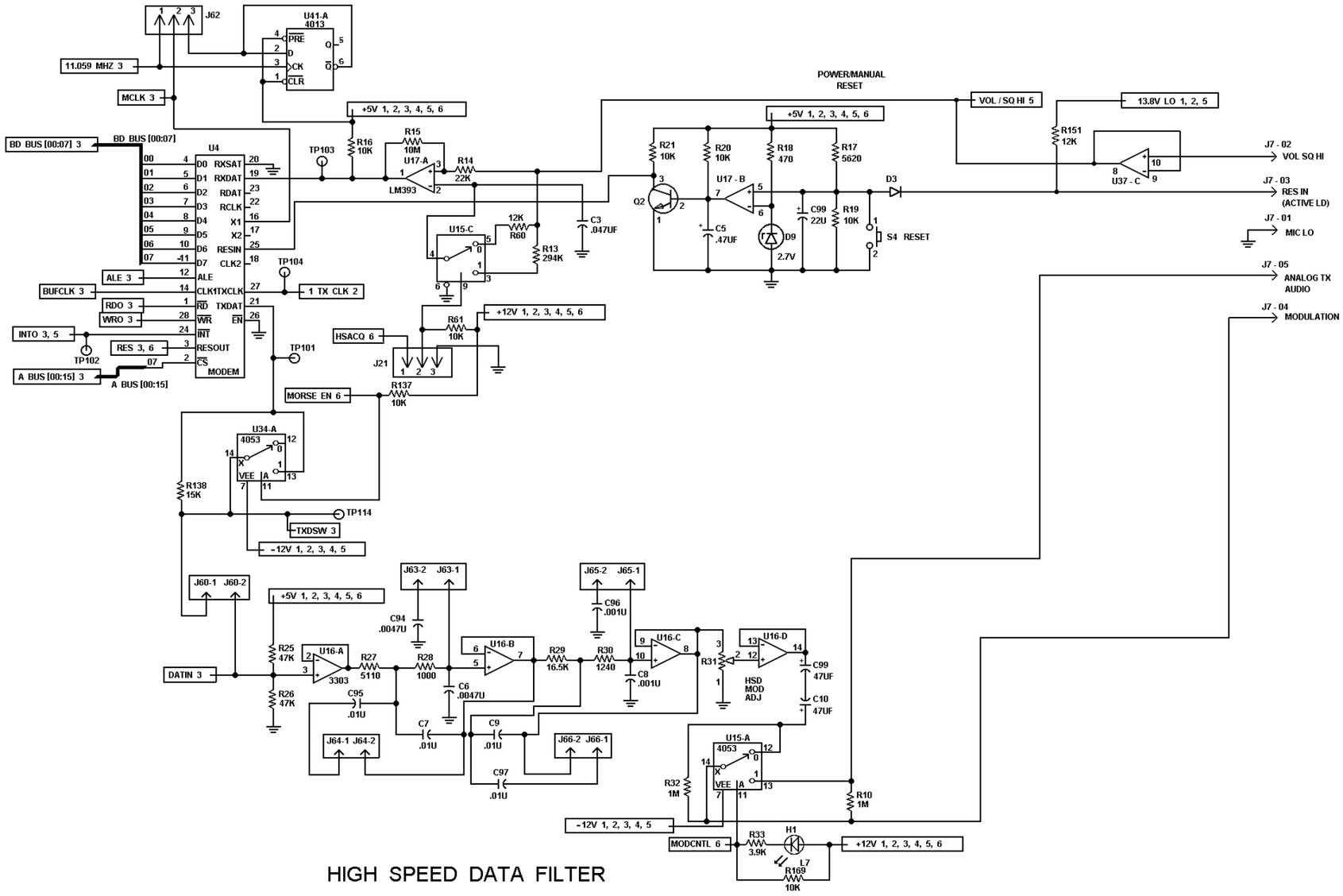
(19D904198, Sh. 5, Rev. 5)



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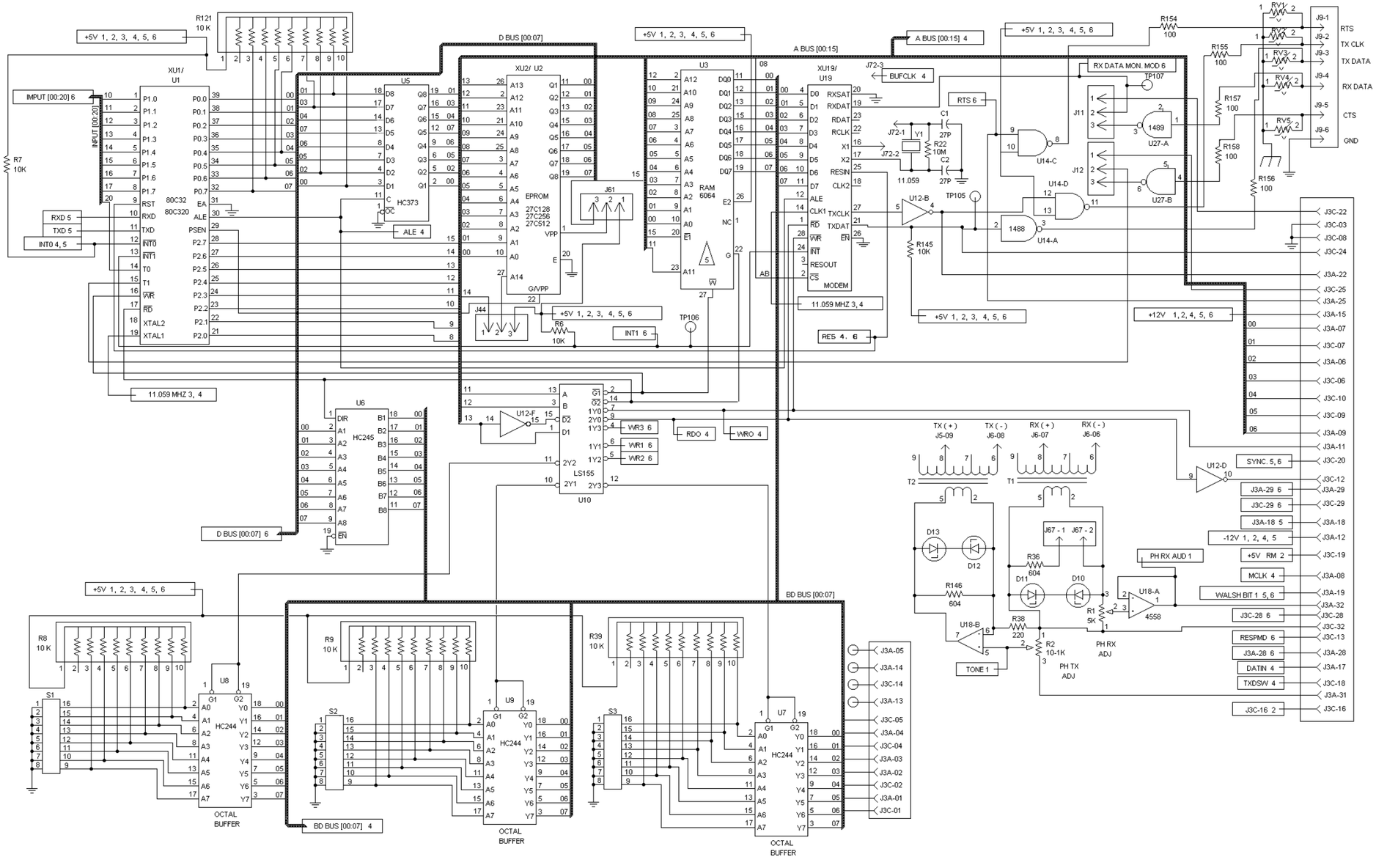
(19D904198, Sh. 4, Rev. 5)



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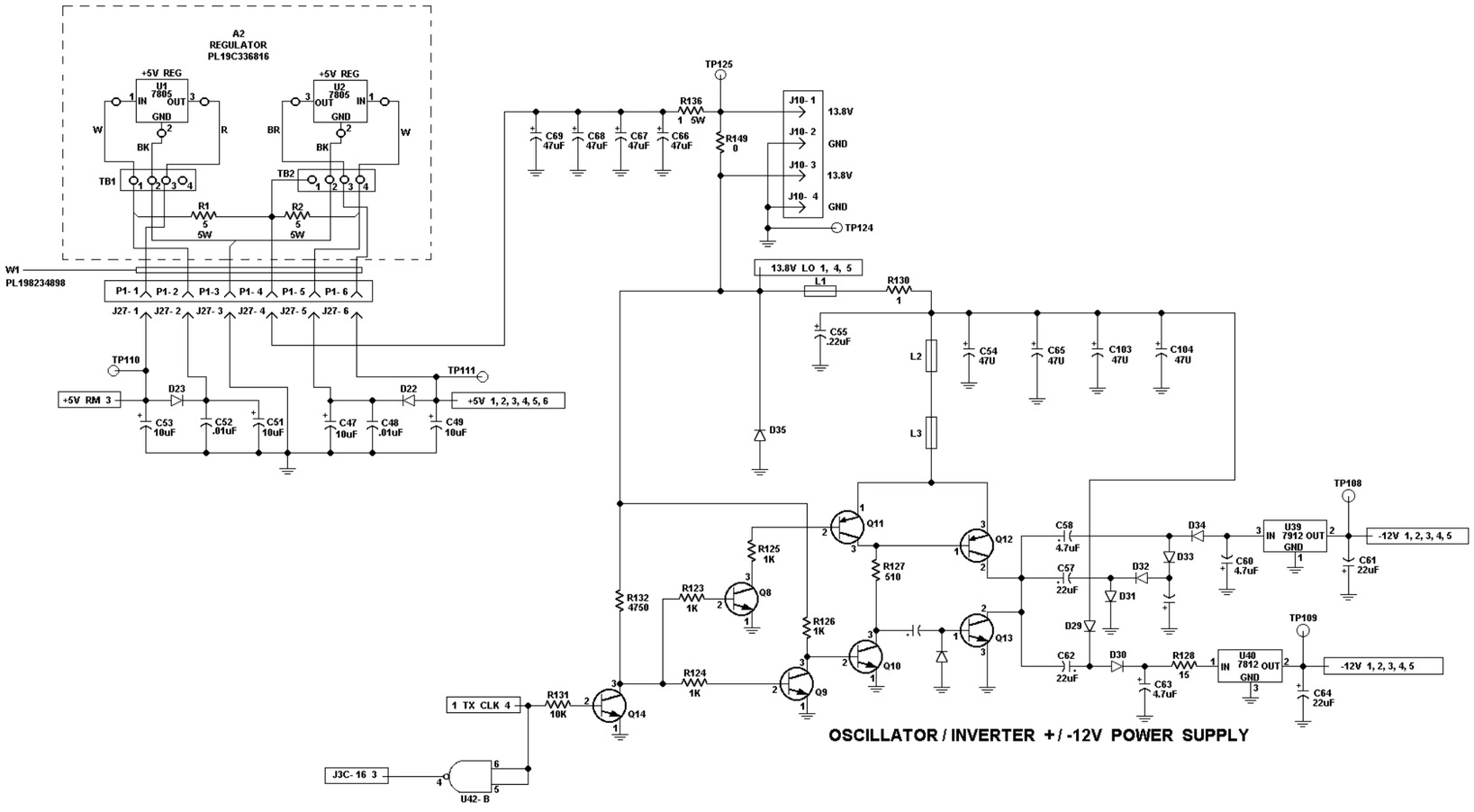
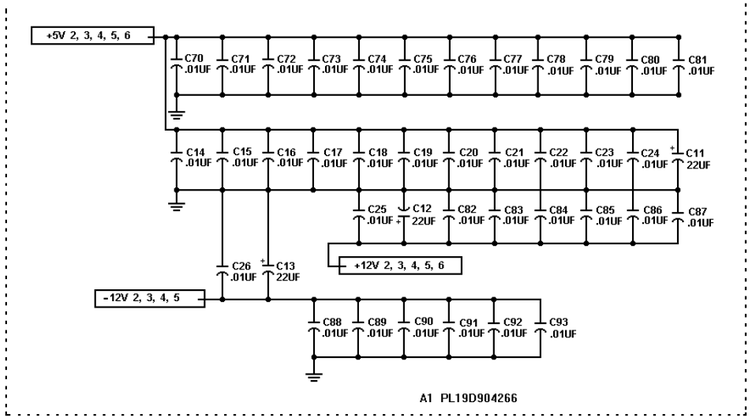


GETC SHELF ASSEMBLY
19D901868G3 and G4
(19D9041198, Sh. 2, Rev. 5)



MODEL NO.	REV LETTER
PL19D904266G1	B
PL19D904266G4	B

ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE INDICATED
RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY MULTIPLIER K OR M.
CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER U, N OR P.
INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER M OR U.

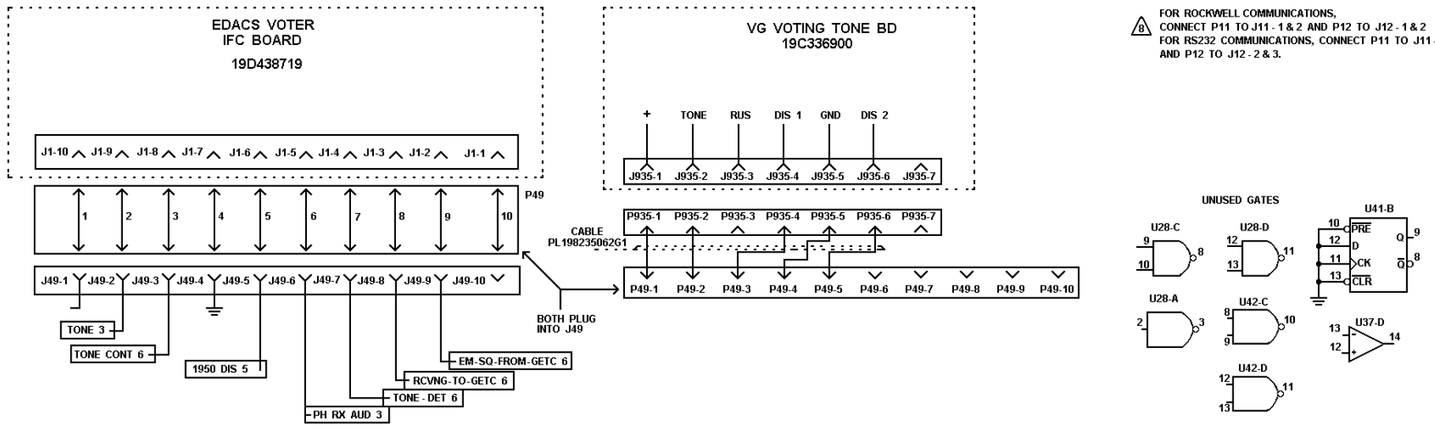
NOTES:

4 FOR JUMPER PLACEMENT, SEE 349A9793.

5 FOR A 6116 RAM (24 PINS), OFFSET DOWNWARD IN THE 28 PIN SOCKET.

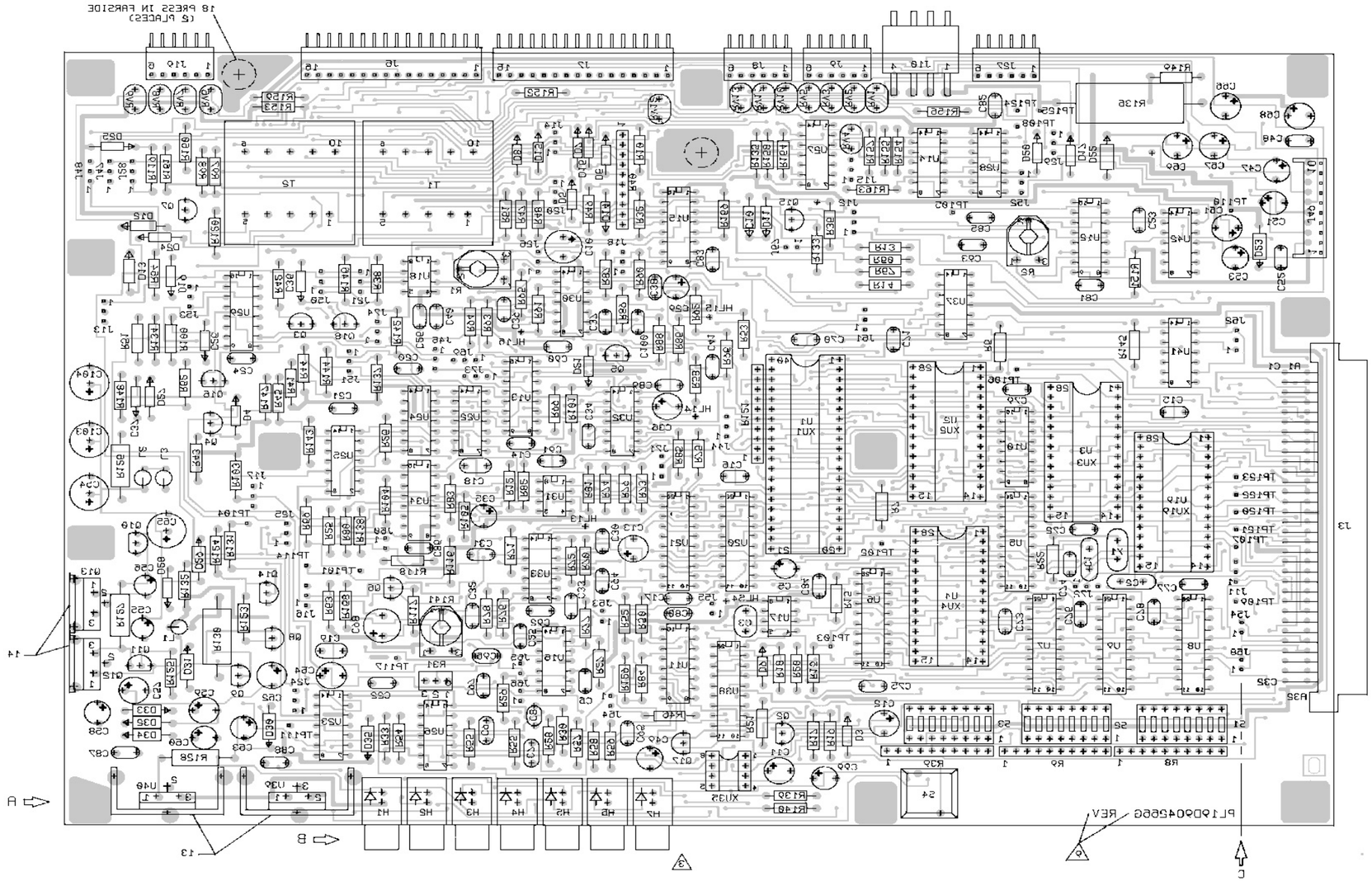
8 FOR ROCKWELL COMMUNICATIONS, CONNECT P11 TO J11 - 1 & 2 AND P12 TO J12 - 1 & 2
FOR RS232 COMMUNICATIONS, CONNECT P11 TO J11 - 2 & 3 AND P12 TO J12 - 2 & 3.

DEVICE	GND PIN NO	+5V PIN NO	+12 PIN NO	-12 PIN NO
U1	20	40		
U2	14	28		
U3	14	26,28		
U4	13	15		
U5	10	20		
U6	10	20		
U7	10	20		
U8	10	20		
U9	10	20		
U10	8	16		
U11	8	1		
U12	8	1		
U13	8	1		
U14	7		14	1
U15	6.8		16	7
U16			4	11
U17	4		8	
U18			8	4
U19	13	15		
U20	10	20		
U21	10	20		
U22	7	14		
U23	7	14		
U24	7	14		
U25	7	14		
U26	7	14		
U27	7	14		
U28	7		14	1
U29	8	1		
U30			4	11
U31			8	4
U32	3.5		4	11
U33			4	11
U34	6.8		16	7
U35	4			
U37			4	11
U38	10	20		
U41	7	14		
U42	7	14		



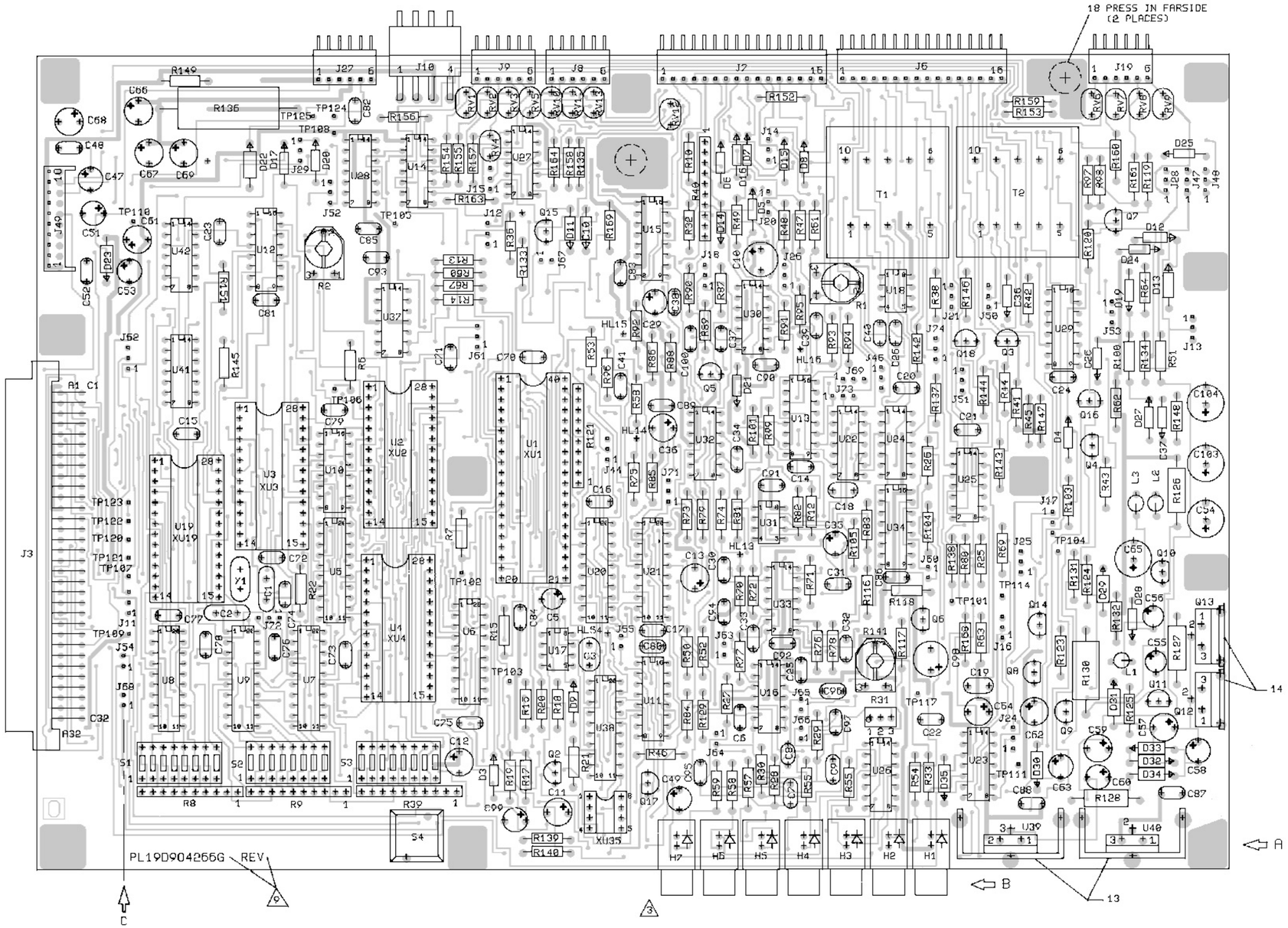
GETC SHELF ASSEMBLY
19D901868G3 and G4
(19D904198, Sh. 1, Rev. 5)

SOLDER SIDE

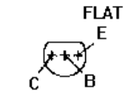


GETC LOGIC BOARD
19D904266
(19D904266, Sh. 1, Rev. 1, Solder Side)

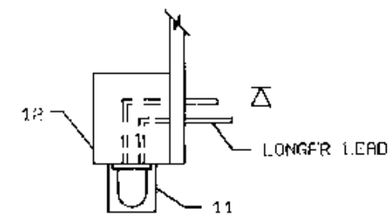
COMPONENT SIDE



LEAD IDENTIFICATION
FOR Q2 - Q11 AND Q14 - Q18

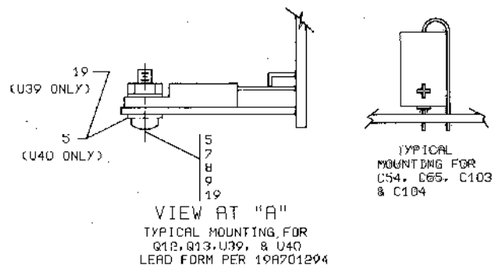


NOTE: CASE SHAPE IS DETERMINING FACTOR FOR LEAD IDENTIFICATION

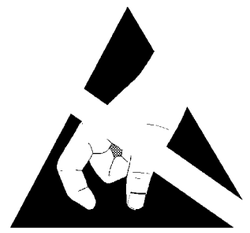


VIEW AT "B"

△7 TYPICAL MOUNTING FOR H1 THRU H7



VIEW AT "A"
TYPICAL MOUNTING FOR Q12, Q13, U39, & U40 LEAD FORM PER 19A701294



CAUTION

OBSERVE PRECAUTIONS FOR HANDLING

ELECTROSTATIC SENSITIVE DEVICES

GETC LOGIC BOARD
19D904266
(19D904266, Sh. 1, Rev. 1, Component Side)