

**MAINTENANCE MANUAL
FOR
800 MHz RECEIVER SYNTHESIZER MODULE
19D902781G5**

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DESCRIPTION

The Receiver Synthesizer Module, 19D902781G5, provides the low noise local oscillator signal (LO) to the Receiver Front End Module of the MASTR III base station. The module also provides the reference oscillator signal to the transmitter synthesizer.

Figure 1 is a block diagram of the Receiver Synthesizer Module. The synthesizer is connected in a phase-locked loop (PLL) configuration. The VCO operates at double frequency and its output is divided by U1.

The logic signals from the controller (U10, U12, and U13) determine the synthesizer frequency.

Additionally, the logic circuitry contains an out-of-lock indicator. During an out-of-lock condition, the PLL sends a signal to the controller and lights the FAULT LED on the front panel of the module.

Frequency stability is maintained by using either the internal reference oscillator Y1 or applying an external high precision reference signal to the EXT Reference Oscillator Port J4. The internal reference oscillator, Y1, is a temperature controlled crystal oscillator (TCXO) operating at 12.8 MHz. The oscillator has a stability of ± 1.0 ppm over the temperature range of -30°C to $+75^{\circ}\text{C}$.

Table 1 - General Specifications

ITEM	SPECIFICATION
FREQUENCY TUNING Mechanical	735.8 MHz-754.8 MHz
Electrical	500 kHz
Channel Spacing	12.5 kHz
FREQUENCY STABILITY	±1.0 ppm
LO POWER OUTPUT	2.0 dBm ±2 dBm
LO NOMINAL IMPEDANCE	50 ohms
PHASE NOISE @25 kHz Offset	> -136 dBc/Hz
HUM AND NOISE Companion Receiver	-55 dB
HARMONICS @ LO PORT	<-30 dBc
SWITCHING SPEED	< 50 ms
CURRENT DRAIN +13.8V	<350 mA
+12V	<20 mA
REFERENCE OSCILLATOR Frequency Output	12.8 MHz ±1.0 ppm
Power Output	1 dBm ± 2 dBm
Impedance	50 ohms
EXT. REFERENCE OSCILLATOR Frequency	5.00 MHz to 17.925 MHz (must be integer divisible by the channel spacing)
Power	+10 dBm ±3 dBm into 50 ohms
Impedance	50 ohms

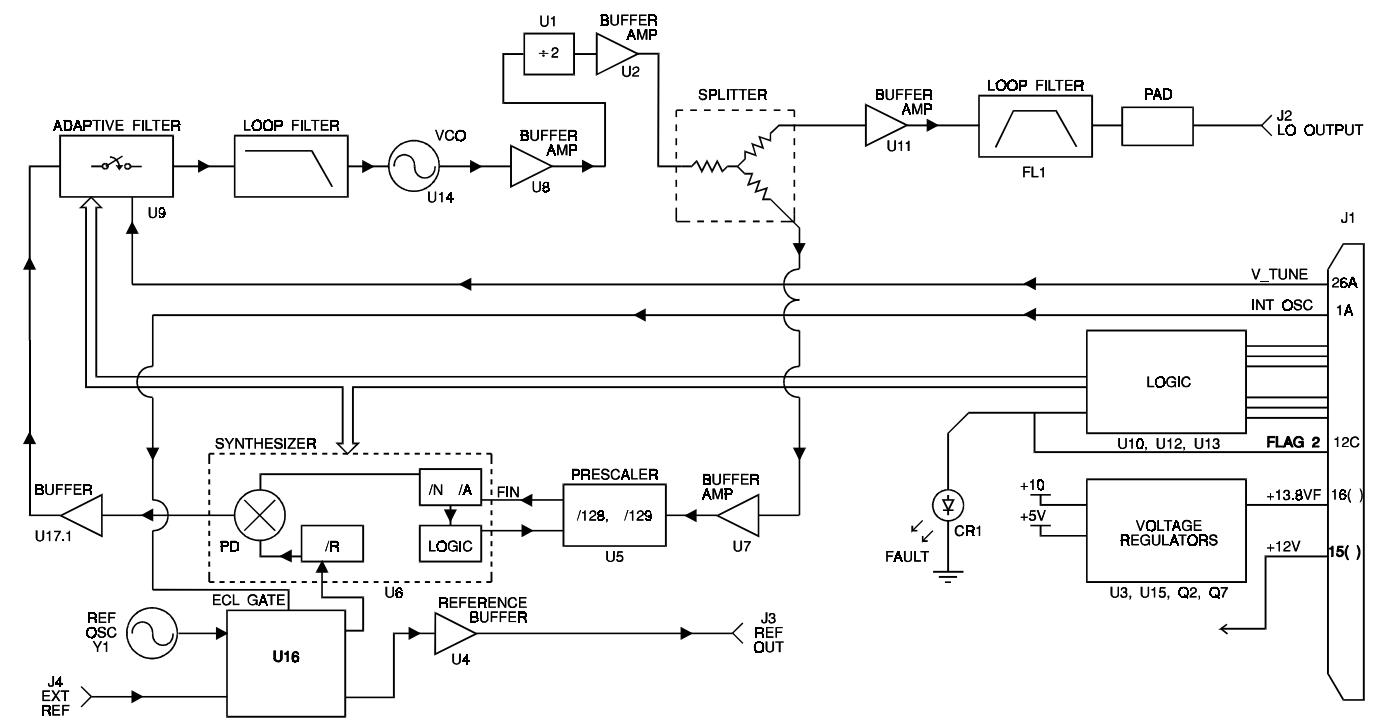


Figure 1- Receiver Synthesizer Block Diagram

CIRCUIT ANALYSIS

The Receiver Synthesizer Module consists of the following circuits:

- Voltage Controlled Oscillator
- VCO Buffer and Divider
- Synthesizer
- Loop Filter
- Reference Oscillator, Buffer, and Switch
- Digital Control Circuits
- Voltage Regulators

VOLTAGE CONTROLLED OSCILLATOR

The first section is an oscillator which runs at the second harmonic of the desired output frequency. The active element is U14 which is a monolithic amplifier. It has been optimized for very low phase noise. Varicaps D1 & D3 are lightly coupled into the main tank circuit to allow the control voltage to shift the frequency slightly. A one volt change on the control line will cause the oscillator frequency to shift around 200 to 300 kHz which is 100 to 150 kHz at the synthesizer output.

VCO BUFFER AMPLIFIER AND DIVIDER

The VCO output is then fed to the second section. It is buffered by MMIC U8 and is fed to divider U1 which divides the frequency by two. It is then buffered by MMIC U2 which drives a resistive splitter formed by R78 thru R81, R54, and R76. Part of the signal is routed to Buffer MMIC U7 which drives the synthesizer prescaler U5. The rest of the signal is fed to MMIC U11 which feeds bandpass filter FL1 which then passed thru a resistive attenuator R50, R51 and R55 which then drives the output BNC connector J2.

SYNTHESIZER

The third section consists of prescaler U5 and synthesizer IC U6. Buffered RF is fed to the prescaler by MMIC U7. The dual-modulus prescaler operates in the 128/129 mode. The prescaler then drives synthesizer IC U6. The phase detector inside U6 is usually programmed to run at 12.5 kHz. The difference between the divided down reference on U6 pin 2 and the divided down VCO signal on U6 pin 10, is compared by the internal sample-hold phase detector. The phase detector gain is set by R43, R44, C42 and C43. It is then fed to the loop filter from pin 17. The phase detector ramp voltage is fed thru buffer U17 which compares the instantaneous ramp voltage with a fixed voltage deter-

mined by R90, R91, and R57. If the ramp voltage gets too high, then we force the lock detect signal low to indicate out-of-lock (via diode D2). The normal lock detect is also combined by D2 and passed to lock detect latch U13. The synthesizer frequency is determined by programming the internal dividers of U6 with the clock, data and enable signals on U6 pins 11, 12 and 13.

LOOP FILTER

The VCO error voltage on U6 pin 17 is passed to the loop filter. Op Amp U17 is biased to keep its output voltage in the range of +1 volts to the upper rail. Bilateral switch U9 section 1 is normally closed, and sections U9-2, U9-3, U9-4 are normally open. The error voltage is filtered by R58, R3, C62, R2, and C61 and is then passed to the voltage controlled oscillator of section 1. When acquiring lock, the bilateral switches U9-3 and U9-4 are closed to change the loop time constants to allow faster lock. After a fixed time period as determined by the enable signal, the switches open which allow much cleaner control voltage which gives a lower noise synthesizer.

REFERENCE OSCILLATOR BUFFER AND SWITCH

The fifth section is the reference oscillator section. Reference oscillator Y1 is a 1.0 ppm 12.8 MHz temperature compensated reference oscillator. Its output is fed to the ECL IC U16. When "INT-OSC" (J1 pin 1A) is at logic "0", the NOR gate (U16), routes the reference oscillator Y1 signal to the output on U16 pins 12 & 19. When "INT-OSC" is at logic "1", the external reference signal on J4 is routed to U16 outputs on pins 12 & 19. The output on U16 pin 19 is fed to the synthesizer IC U6, while the output on pin 12 is passed to buffer MMIC U4. It is then low pass filtered by C45, C60, L2, and attenuated by R46, R52, and R47. The output drives BNC connector J3 which is used to drive external devices which need to use the same reference frequency as the RX synthesizer, (such as the TX synthesizer).

DIGITAL CONTROL CIRCUITS

The sixth section consists of various control logic circuitry. IC U13 is used as a lock detect latch. The lock detect signal on diode D2 is one input to a set-reset latch. The other input is from the enable signal fed to U13 pin 1. These inputs are normally at logic "1". During synthesizer loading, U13 pin 1 will be at logic "0" which forces U13 pin 3 to be logic "1" which is U13 pin 12. U13 pin 13 is also normally logic "1" so that U13 pin 11 is at logic "0". When U13 pin 1 returns to logic "1", U13 pins 3 & 11 will hold "0". When U13 pin 1 returns to logic "1", U13 pins 3 & 11 will hold their previous states. If U13-13 drops to logic "0" (while

U13-1 is at logic "1"), then U13-11 will latch at "1" indicating that the module is unlocked. Reloading the synthesizer (and in the process generating a logic "0" on U13-1) will reset the latch to indicate the normal locked condition. When unlocked, "FLAG2" on the 96 pin din connector J1 pin 12C is also pulled low to indicate to the controller in the base station that the RX synthesizer is out-of- lock.

IC U10 is used to decode the RX Synthesizer address present on lines "A0", "A1", and "A2" which are pins 6C, 7C and 8C of J1. The RX synthesizer is selected when "A0" and "A2" are at logic "0" and "A1" is at logic "1". This is address "2". When this address is present on the backplane, the "CLOCK", "DATA" and "ENABLE" signals on J1 pins 2C, 3C and 4C are passed thru level translators formed by U12 and Q3, Q4, and Q5 which convert the 0-5 Volt logic to the levels needed by synthesizer IC U6.

The signal "ENABLE-TEST" on J1 pin 22A is at logic "0" during normal synthesizer operation. In test mode it is desired to force the control voltage to a known voltage in order to set the center frequency of the VCO. This is done by setting "ENABLE TEST" to logic "1" which closes switch U9-2 and opens the switch U9-1. This allows the externally generated analog voltage on J1 pin 23A to be routed through the loop filter to force a known voltage on the control line.

VOLTAGE REGULATORS

The last section of the RX synthesizer is the voltage regulators. IC U3 is a 5 volt regulator which powers most of the logic circuitry. Op Amp U15 with Q1 and Q2 form a very low noise regulator to power the noise sensitive RF circuitry. Resistors R5 and R6 set the output voltage along with the reference voltage fed to U15 pin 3. Q2 is the pass transistor which is driven by Q7 which acts as a current source to allow good noise rejection. The collector of Q2 is sensitive to excessive capacitance and can become unstable if the load looks capacitive at frequencies on the order of 1 MHz. Each section of the circuit is isolated by resistors such as R38 in order to ensure that transistor Q2 sees a resistive load at 1 MHz.

MAINTENANCE

RECOMMENDED TEST EQUIPMENT

The following test equipment is required to test the Synthesizer Module:

1. Modulation Analyzer; HP 8901A, or equivalent
2. Power Supply; 12.0 Vdc @ 500 mA
Note: The synthesizer module normally requires +13.8 Vdc and +12 Vdc. For testing purposes it is sufficient to connect both the +13.8 Vdc input and the +12 Vdc input to a +12 Vdc power supply.

SERVICE NOTES

The following service information applies when aligning, testing, or troubleshooting the RX Synthesizer:

- Logic Levels:
 - Logic 1 = high = 4.5 to 5.5 Vdc
 - Logic 0 = Low = 0 to 0.5 Vdc
- Receiver Synthesizer Address = A0 A1 A2 = 010
- Synthesizer data input stream is as follows:

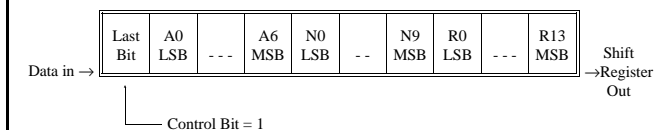
14-bit "R" divider most significant bit (MSB) = R13 through "R" divider least significant bit (LCB) = R0

10-bit "N" divider MSB = N9 through "N" divider LSB = N0

7-bit "A" divider MSB = A6 through "A" divider LSB = A0

Single high Control Bit (last bit)

DATA ENTRY FORMAT



- Synthesizer lock is indicated by the extinguishing of the front panel LED indicator and a logic high on the FLAG 2 line (J1 pin 12C).
- Always verify synthesizer lock after each new data loading.

3. Frequency Counter; 10 MHz - 1GHz
4. Panel Meter; -20dBm to +10dBm
5. Spectrum Analyzer; 0-3 GHz

TEST AND ALIGNMENT

Adjust the VCO Tuning Screw for 745 MHz ±100 kHz.

Initialization

Apply +12 Vdc to module pins 15A, 15B, 15C, 16A, 16B and 16C.

Current consumption

Measure the current through pins 15A, 15B, 15C, 16A, 16B, and 16C.

Verify the current is less than 350 mA. Total current is the +13.8 Vdc current and +12 Vdc current combined.

Reference Oscillator

Adjust Y1 for an output frequency of 12.8 MHz ±1 Hz. Measure the output power of the reference oscillator output (J3).

Verify the output power is 1dBm ±2 dB.

Oscillator Alignment

Ground the ENABLE TEST line (pin 22A). Apply +6 Vdc to the V_TUNE line (pin 26A.) Measure the frequency of the free running divided oscillator at the LO OUT port (J2).

Synthesizer Loading

Unground the ENABLE TEST line (pin 22A). Load the synthesizer IC for 745 MHz.

Verify the lock indicator (CR1) is off or the FLAG 2 line is high.

Hum and Noise

Initialize the HP 8901A for 300 Hz - 3 kHz, 750 μsec deemphasis, average FM deviation, and 0.44 dB reference for the deviation.

Verify the hum and noise (J2) is less than -55 dB.

Output Power and Harmonic Content

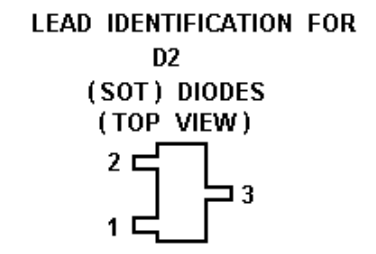
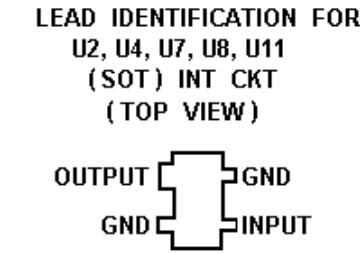
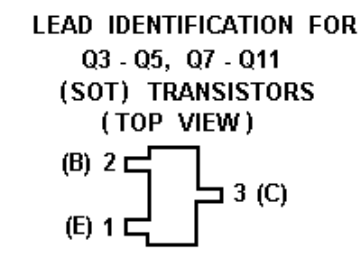
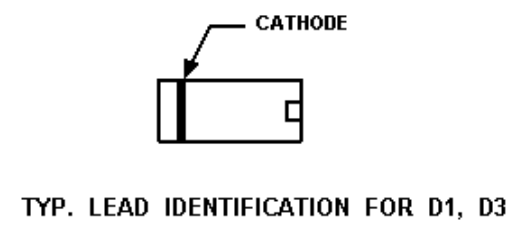
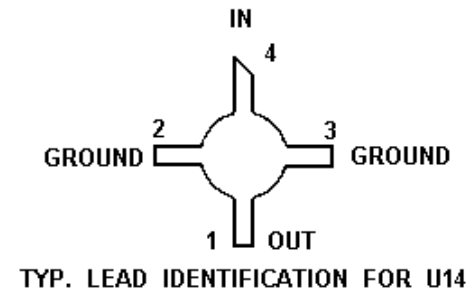
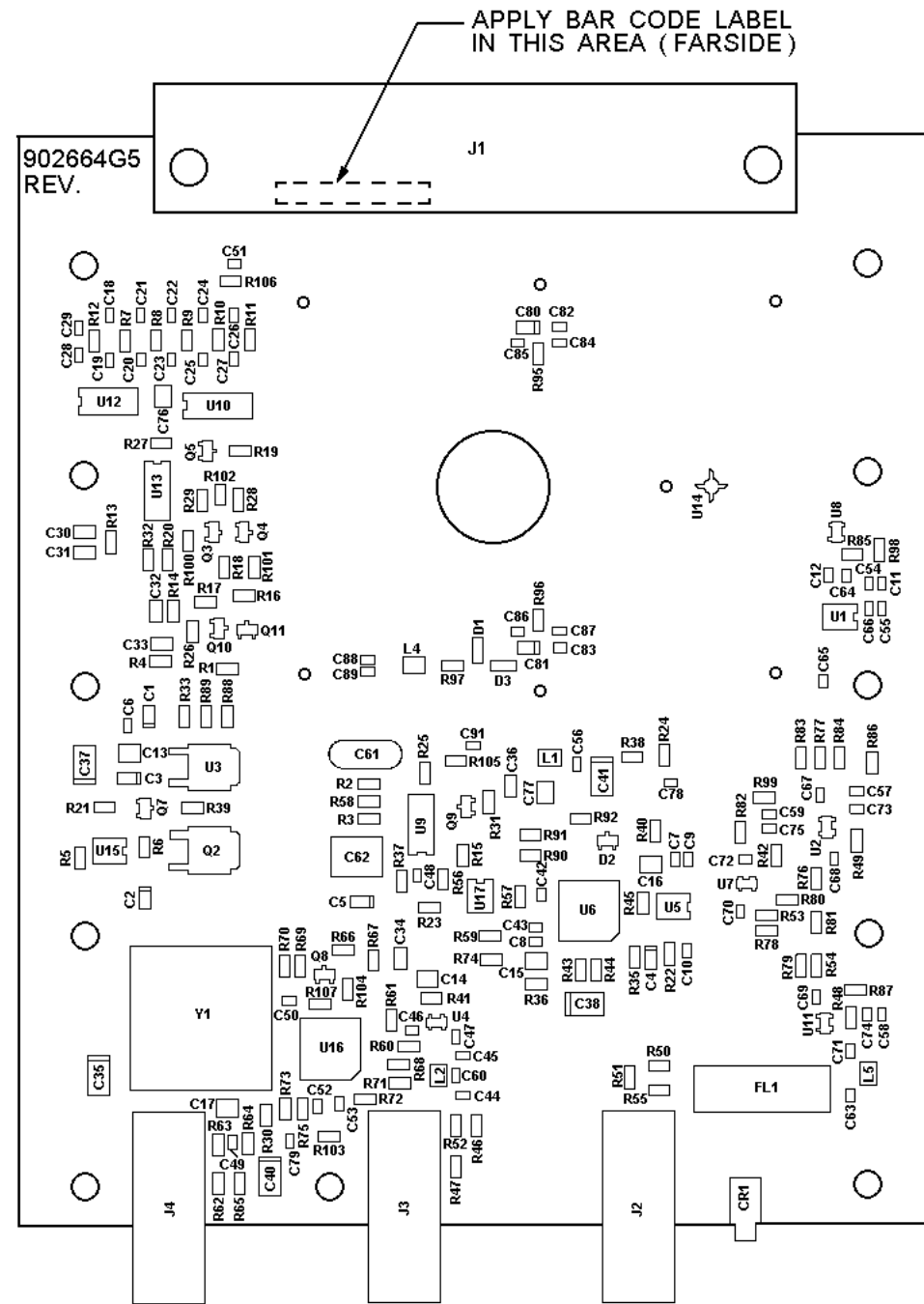
Verify the output power (J2) at the fundamental frequency is:

2 dBm ±2 dB

Verify the harmonic content is less than -30dBc.

TROUBLESHOOTING CHART

SYMPTOM	AREAS TO CHECK	INDICATIONS
I. Loop fails to lock.	<p>Check for: +5 Vdc at U3-3 +10 Vdc at Q2-C</p> <p>Check for LO output at J2, 735 to 755 MHz, 0 dBm nominal. Adjust LO freq if necessary</p> <p>Check for 12.8 MHz reference at U6-2. Typical level = 0.75 Vpp</p> <p>Check for prescaler output U5-4 approx 6 MHz, 1.25 Vpp</p> <p>Check for CLOCK, DATA, and ENABLE logic signals at U6-11, 12, and 13 0/8 V logic</p> <p>Check for ramp signal at U6-15. 12.5 kHz nominal</p>	<p>Bad regulator circuitry. Troubleshoot using standard procedures</p> <p>No oscillation, bad divider, or defective buffer chain. Proceed to LO section III</p> <p>Reference oscillator module or ECL gate defective. Proceed to reference oscillator section II</p> <p>If input is present then defective U5</p> <p>If all programming signals (CLOCK, DTA, ENABLE, A0, A1, and A2) are present at J1 then bad control logic or level shifters Q3, Q4, Q5</p> <p>If all U6 inputs are present, then defective U6</p>
II. Reference not present	<p>Check for reference signal at U16-14. Typical level = 1 Vpp</p> <p>Check for reference signal at U16-12 and U16-19. Typical level = 0.75 Vpp</p>	<p>Bad oscillator Y1</p> <p>Bad ECL gate</p>
III. Low LO power	<p>Check signal levels along divider/buffer chain UB-1 x 2 freq 0 dBm U1-7 - 10 dBm U2-1 0 dBm U11-1 5 dBm U7-1 0 dBm</p> <p>Check 3.2 Vdc bias at UB-1 U2-1 U11-1 U7-1</p>	<p>Defective oscillator, divider, or amplifier</p> <p>Defective amplifier</p>

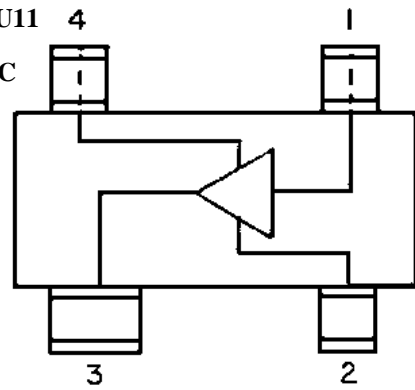


RECEIVER SYNTHESIZER BOARD

19D902664G5

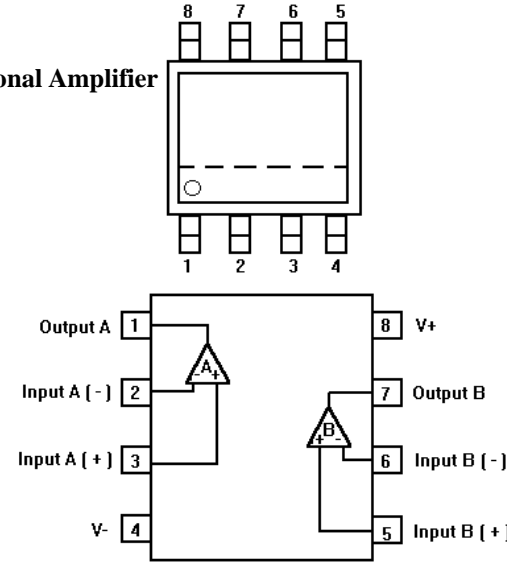
(19D902664, Sh. 3, Rev. 1)

U2, U4, U7, U8, U11
19A705927P1
Silicon Bipolar IC

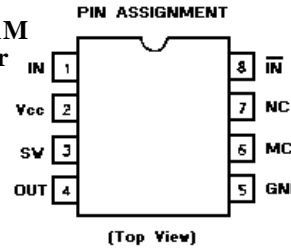


PIN 1. RF INPUT
2. GROUND
3. RF OUTPUT AND BIAS
4. GROUND

U15, U17
19A702293P2
Dual Operational Amplifier

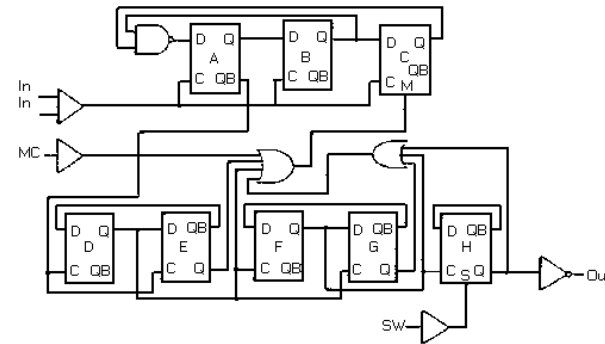


U5
19A149944P201M
odulus Prescaler

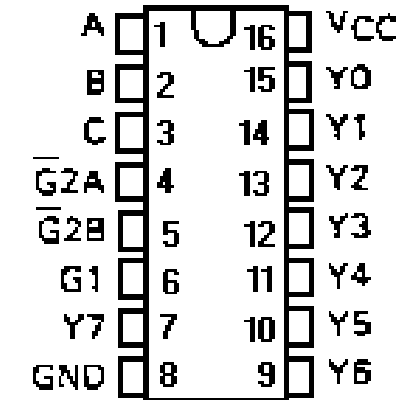
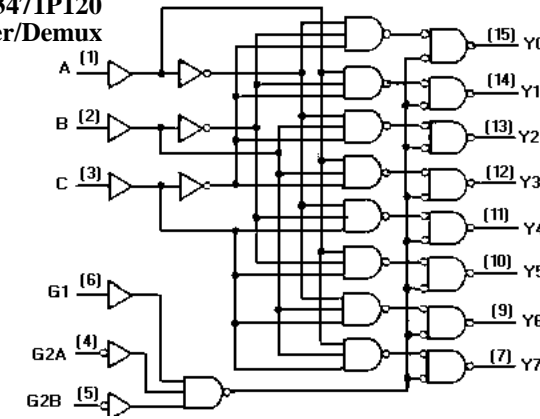


FUNCTION TABLE		
Sw	MC	DIVIDE RATIO
H	H	64
H	L	65
L	H	128
L	L	129

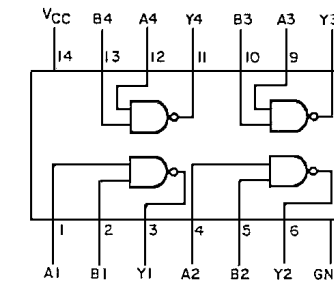
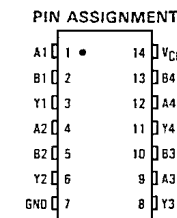
SW: H = Vcc L = OPEN
MC: H = 2.0V TO Vcc
L = GND TO 0.8V



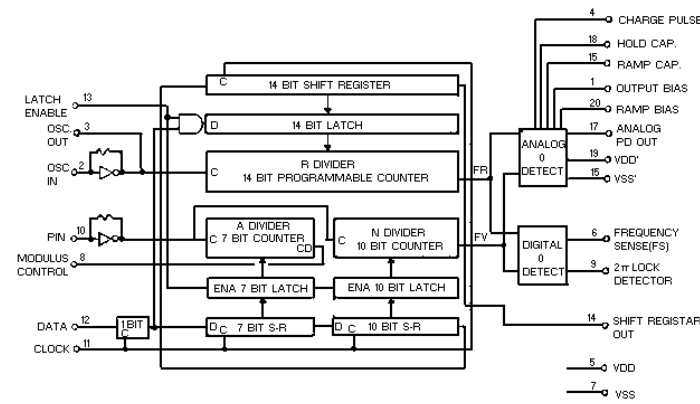
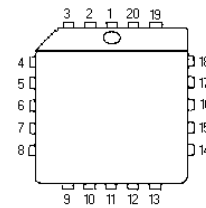
U10
19A703471P120
Decoder/Demux



U12 & U13
19A704383P302
Logic Gate/Inverter

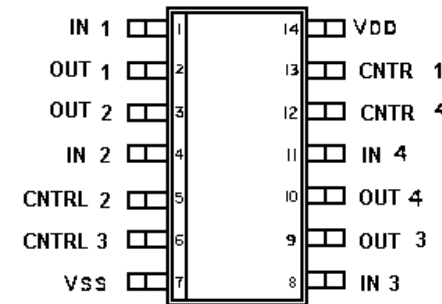


U6
19B800902P5
Synthesizer

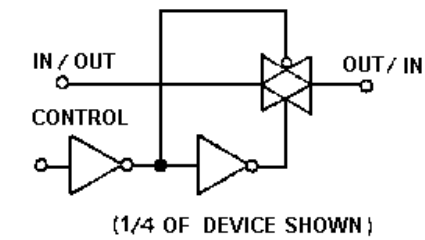


U9
19A702705P4
Quad Analog Switch

PIN CONFIGURATION

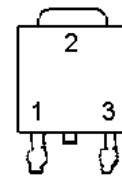


LOGIC DIAGRAM



CONTROL	SWITCH
0	OFF
1	ON

U3
19A704971P8
5V Regulator

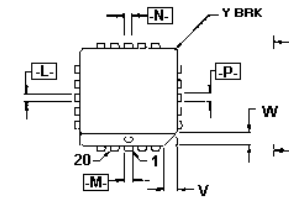


PIN	FUNCTION
1	INPUT
2	GROUND
3	OUTPUT

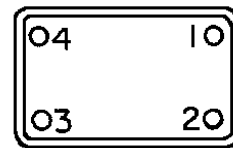
U16

RYT 403 006 / C.

TERMINAL	SYMBOL	FUNCTION
2	UCC1	SUPPLY VOLTAGE
20	UCC2	SUPPLY VOLTAGE
10	UEE	SUPPLY VOLTAGE
5,7,8,9	A1, B1, A2, B2	INPUTS
13,14,15,17	A3, B3, A4, B4	INPUTS
3,4,18,19	01, 02, 03, 04	OUTPUTS
12	04C	COMPLEMENTARY OUTPUT
1,6,11,16	NC	NO CONNECTIONS



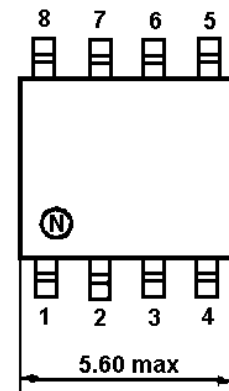
Y1
19B801351P12
Crystal Oscillator



PIN CONNECTIONS

1. COMMON & CASE
2. OUTPUT
3. + Vcc
4. MODULATION

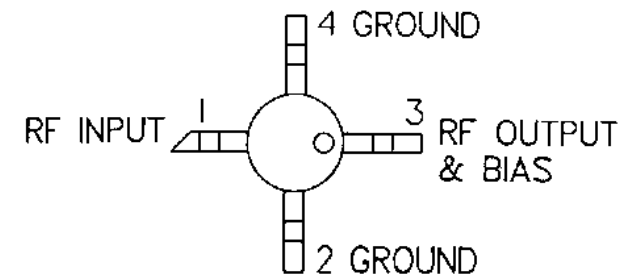
U1 RYT102217
÷2 Prescaler

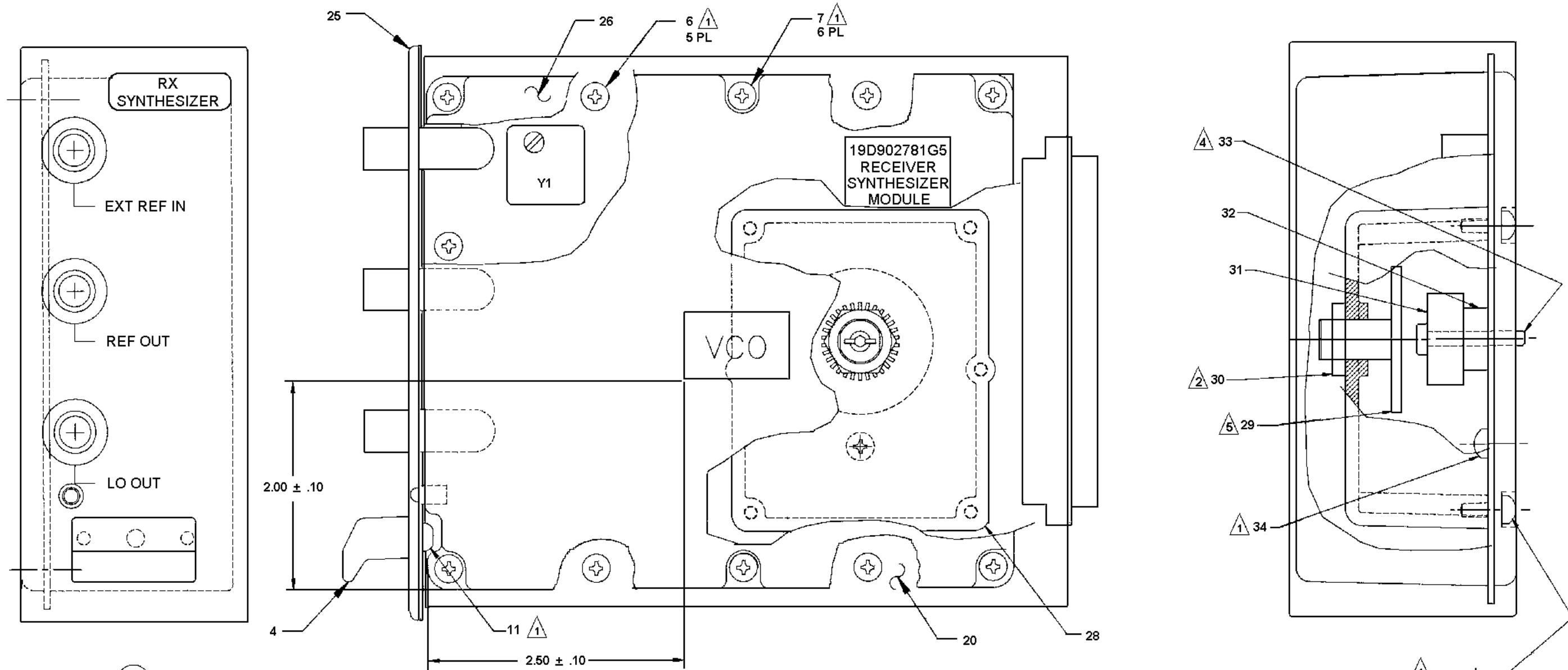


PIN CONNECTION

1. Us
2. Input
3. Bypass
4. GND
5. GND
6. NC
7. Output
8. NC

U14
19A705537P2





24 NOTES:

- 1 TORQUE SCREWS, ITEMS 6, 7 AND 27, TO 10.0 ± 1.3 INCH POUNDS.
TORQUE SCREWS, ITEM 11, TO 20 ± 1.3 INCH POUNDS.
TORQUE SCREWS, ITEM 34 TO 6 ± 1 INCH POUNDS.
- 2 TIGHTEN TUNING NUT, ITEM 30 SO THAT TORQUE ON TUNING SCREW,
ITEM 29 IS 100 IN. OZ. AT MIDDLE OF TUNING RANGE WITH POINTS
ON TUNING NUT BETWEEN RAISED SERATIONS ON COVER, ITEM 28.
- 4 TORQUE SCREW, ITEM 33 TO 3 INCH POUNDS AND LOCK USING ADHESIVE
PER EGE PROCESS P7C-EA147. THEN TRIM SCREW FLUSH TO 0.050 MAX
ABOVE SURFACE ON ITEM 25.

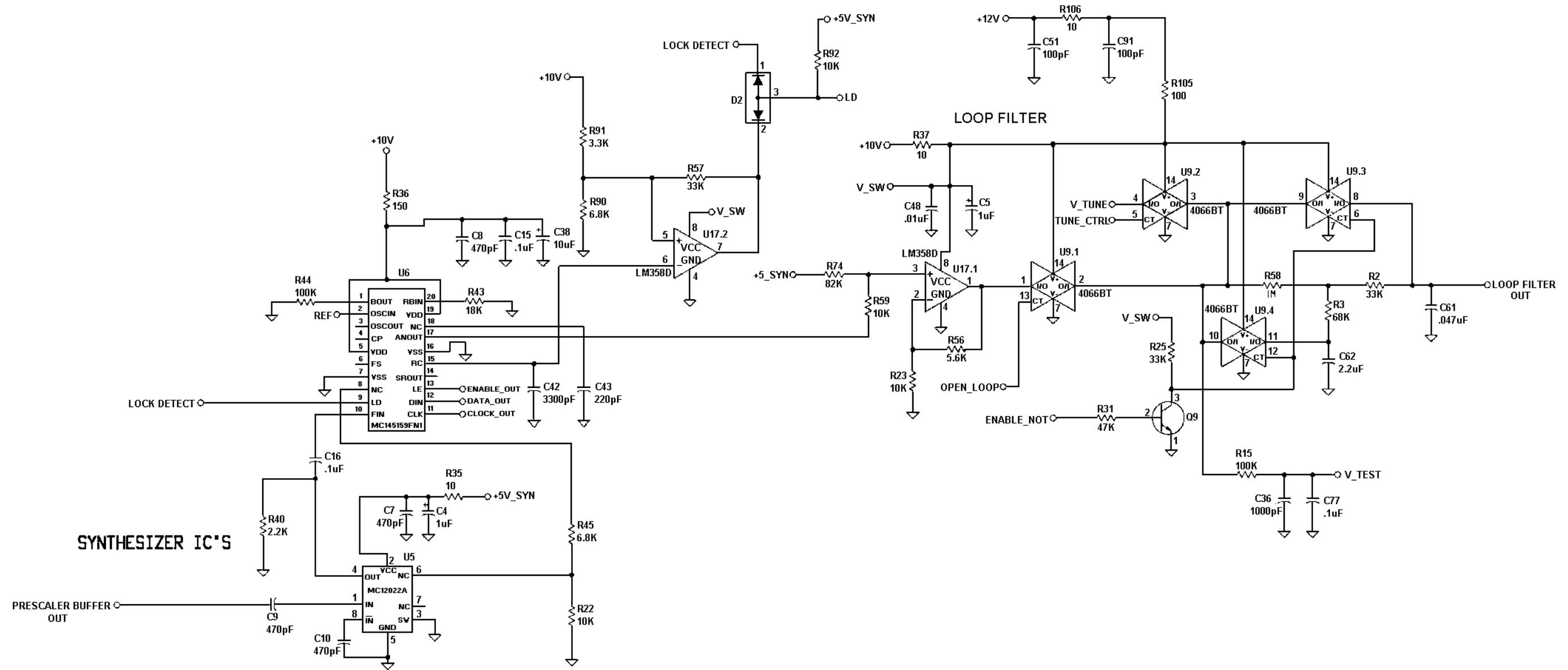
5 COAT THREADS OF TUNING SCREW, ITEM 29, WITH
WAX LUBRICANT.

1 27
6 PLACES
TO MOUNT
ITEM 28

RECEIVER SYNTHESIZER MODULE

19D902781G5

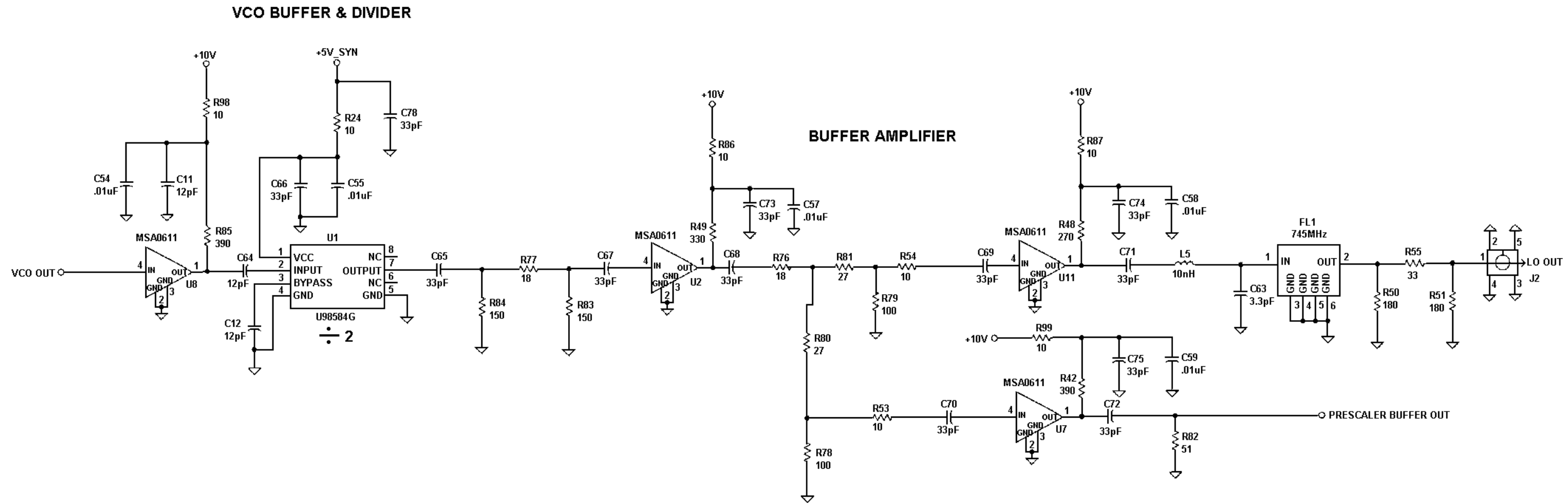
(19D902781, Sh. 3, Rev. 4)



RECEIVER SYNTHESIZER MODULE

19D902664G5

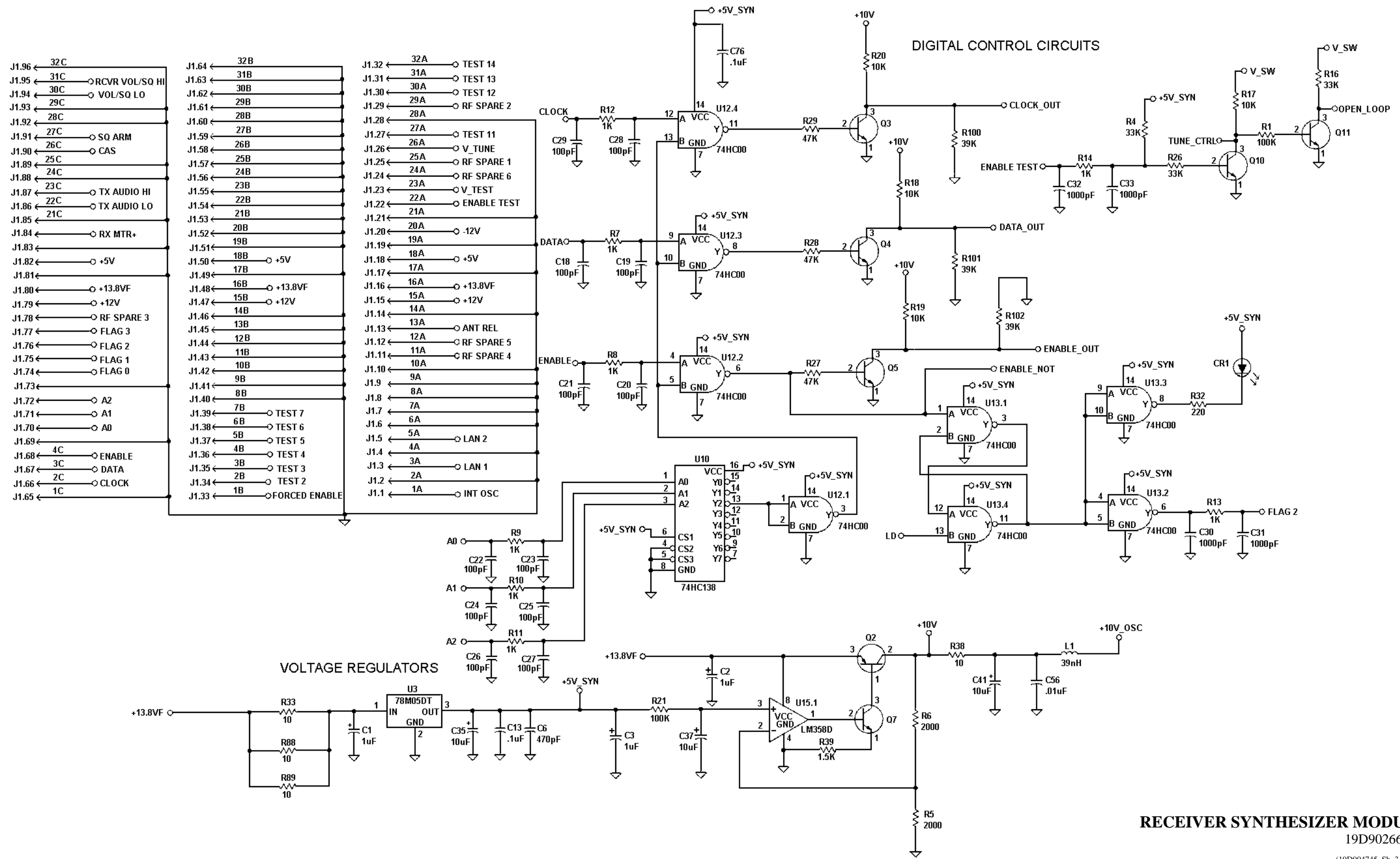
(19D904745, Sh. 1, Rev. 1)



RECEIVER SYNTHESIZER MODULE

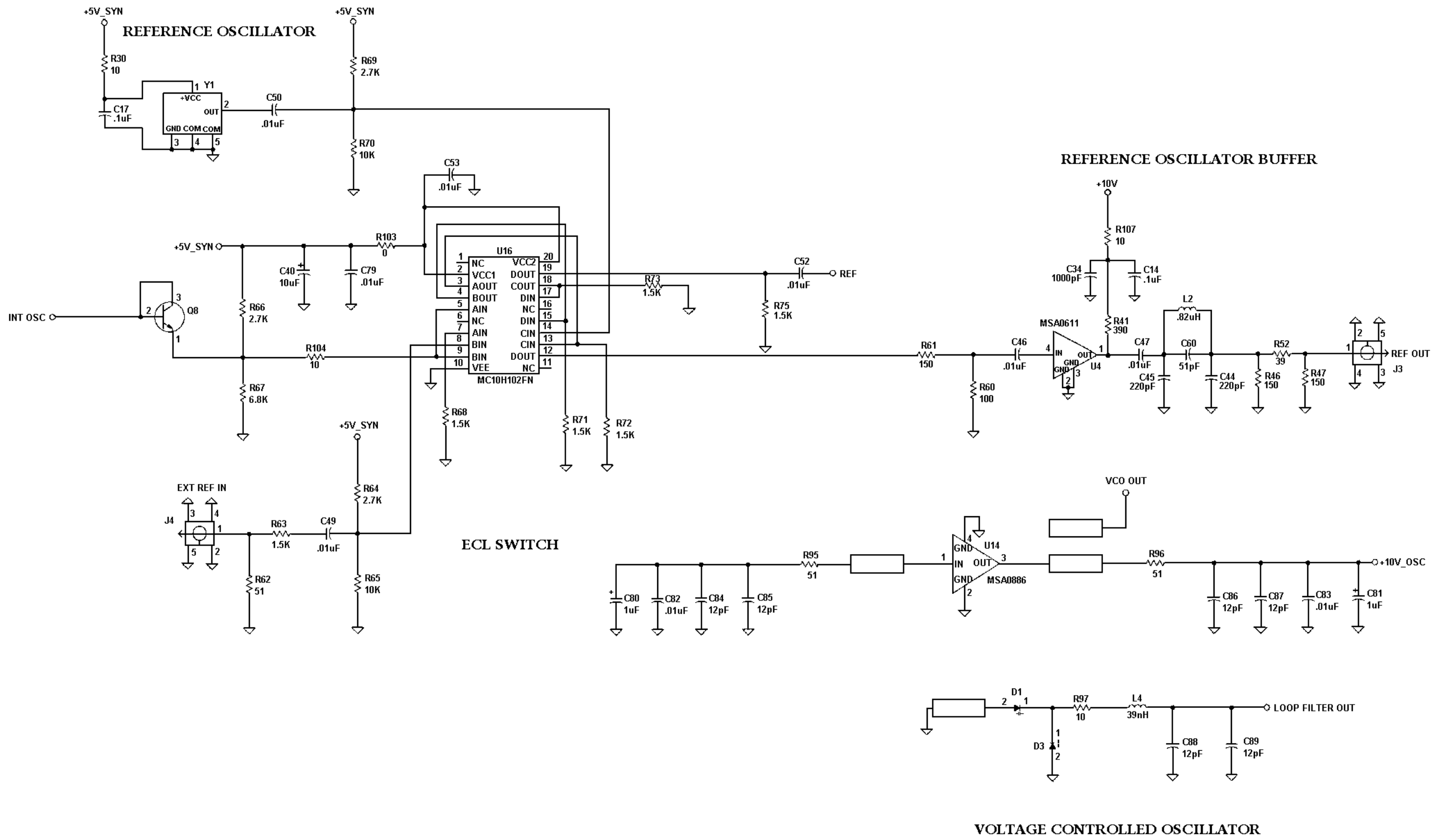
19D902664G5

(19D904745, Sh. 2, Rev. 0)



RECEIVER SYNTHESIZER MODULE
19D902664G5

(19D904745, Sh. 3, Rev. 1)



RECEIVER SYNTHESIZER MODULE

19D902664G5

(19D904745, Sh. 4, Rev. 1)

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