MAINTENANCE MANUAL
AEGIS MODULE
19D904871G1

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SPECIFICATIONS

INPUT VOLTAGE	13.8 VDC (nominal)

DESCRIPTION

The Aegis Module performs speech digitization and compression for Aegis-equipped MDR and MDX radios. It plugs onto the Audio/Logic Board. The interconnections are shown in Figure 1.

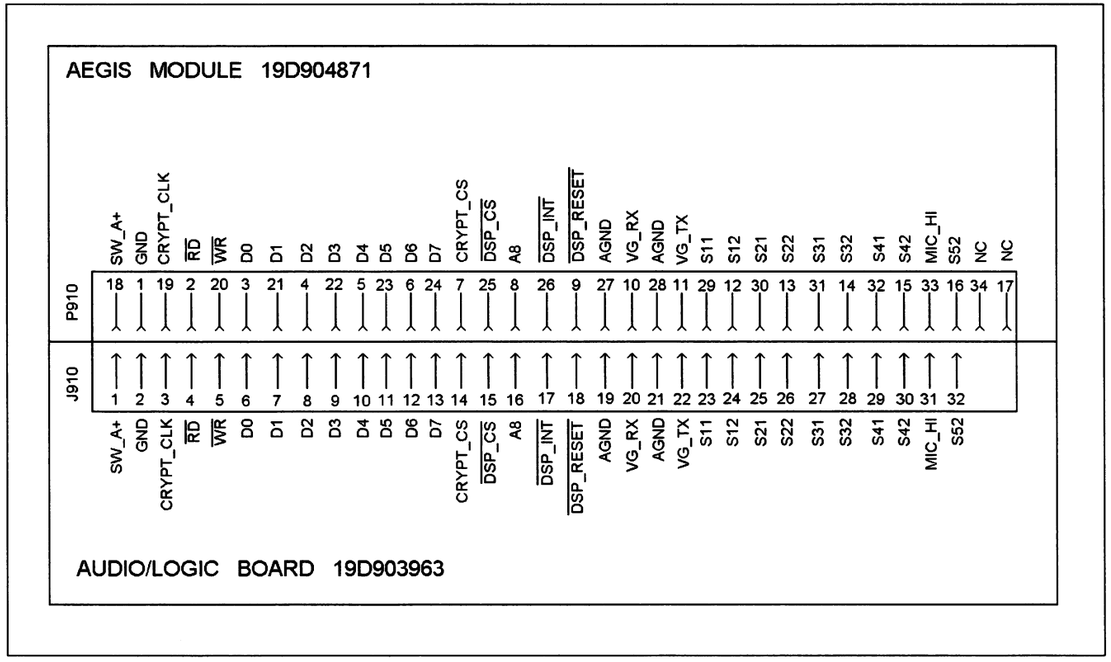


Figure 1 - Interconnection Diagram

Ericsson GE Mobile Communications Inc.
Mountain View Road • Lynchburg, Virginia 24502

Printed in U.S.A.

CIRCUIT DESCRIPTION

Most module functions are performed by Digital Signal Processor U701. U701 converts analog speech to and from a compressed digital form. U701 communicates with the Audio/Logic Board's Radio Control Processor (RCP, U701) through its 8-bit port HD0-HD7, which is connected to the RCP data bus. The WR, RD, and HSEL signals which control the port are direct inputs from the audio/logic board. The port requires 3 address inputs to select the registers in the port; however, the interface only provides one (HA0). HA2 and HA1 are latched by bus writes to a separate address latch port. The latch strobe is created by gates U703.1 and U703.2, and the addresses are latched in U702. The PWD and RESET inputs of U701 are also latched into U702. PWD is used to power U701 down during standby mode. RESET is used to reset U701 and mute the receive audio by turning off Q601.

The FL0 output provides an active-low interrupt to the RCP when speech data is available in transmit mode or requested in receive mode.

Y701, C701, and C702 provide a 9.8304 MHz clock for U701. Op-amp U601.3 is used to limit the mic audio before setting to U701. Op-amp U601.2 provides differential to single ended conversion of the analog speech output from U701. U601.1 provides a half-supply reference for U601.2, U601.3 and U601.4.

Regulator U23 and associated components provide a regulated +5V supply for the analog portion of U701. The digital portion of U701 is powered by the +5V regulator U21. Regulator U22 and associated components provide a regulated +8V supply for the analog +5V regulator (U23) and the op-amp (U601).

U701 must have software loaded into it at powerup by the controller RCP. This is performed automatically by the RCP each time the radio is powered up. This software is stored in the RCP Flash EEPROM along with the RCP operating software and radio personality.

TRANSMIT OPERATION

In transmit mode, microphone audio is routed to P910.33 (MIC-HI). It is limited by op-amp U601.3. Op-amp U601.3 and the associated circuitry provides a gain of 16 dB. With this gain, the output begins to clip with a mic level around 220 mV. The output is further conditioned by U701's internal input op-amp at VINNORM and VFBNORM. It is digitized and compressed (vocoded) by U701. The resulting data is read by the RCP over bus D0-D7 for formatting and transmission. The RCP adds preamble and frame header data to the data stream and loads the data into the modem ASIC (U702) for serial transmission. Serial data from U702 is filtered by the ASP before being sent to the transmitter modulator.

RECEIVE OPERATION

In receive mode, analog serial data from the receiver discriminator is amplified and limited by the ASP. The logic level data is applied to the serial receive input of the modem ASIC which detects sync patterns within the data and interrupts the RCP. The RCP reads the data from the modem ASIC, removes and analyzes the preamble and frame headers for validity, and writes the remaining speech data to U701. U701 performs decompression (vocoding) and digital-to-analog conversion. The differential analog speech signal is present at VOUTP and VOUTN and converted to single-ended by U601.2. The audio is then pre-emphasized by U601.4 and then output on P910-10. The audio is then routed through the ASP for volume control and deemphasis before being applied to the radio speaker amplifier.

DATA FORMAT

Preamble

At the start of a transmission (PTT), a preamble consisting of repeated sync, initialization vector (IV) and addressing information is sent before voice encryption begins. The preamble provides a high probability of correct reception of sync, IV and repeater address (see Figure 2).

Frame Header

The encrypted voice data frame header is shown in Figure 3. Information is provided at the beginning of a frame to insure maintenance of data and cryptographic sync and to allow late entry into a conversation during private receive. Following the 112 bits of the frame header are 2040 bits of encrypted SBC voice data. The frame header is then repeated with a new IV.

End of Message (EOM)

In order to signal the end of a transmission, an inverted sync-plus-dotting sequence is transmitted for about 50 msec. This allows for a long fade in the signal and still ensures that the receiver decodes the EOM correctly.

TROUBLESHOOTING

A test cable (19C852541P1) is available that will permit probing of the component side of the Aegis module.

Aegis problems can be quickly isolated by swapping the Aegis module with a known good module. If the problem disappears with a new module, the module was defective. If the problem remains, the problem is in the Audio/Logic Board or the radio was programmed incorrectly.

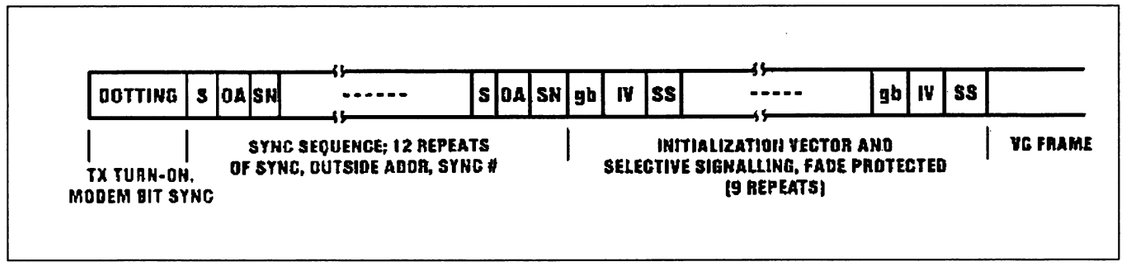


Figure 2 - Preamble Format

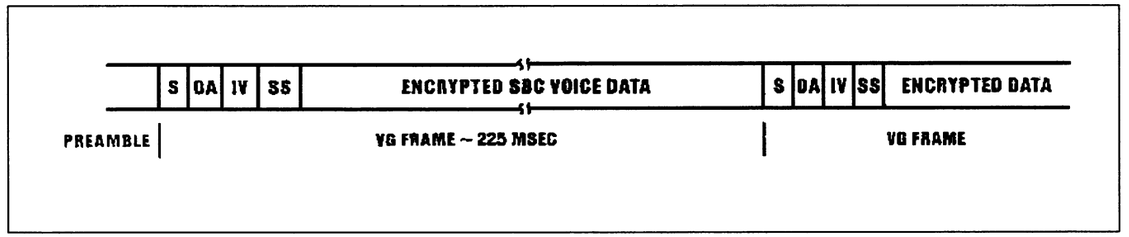


Figure 3 - Frame Header Format

Digital failures are difficult to troubleshoot with field test equipment and board replacement is the most cost-effective solution. Most digital failures result in a DSP ERR message and error code (ERR=xxxx) at power up of the radio unit. The error code indicates the type of failure:

ERR=0851 DSP software was not loaded into the RCP flash EEPROM. This can usually be corrected by reprogramming the radio.

ERR=0852 DSP software in the RCP flash EEPROM had a CRC error. This can usually be corrected by reprogramming the radio.

ERR=0853 The type of Aegis enabled in radio feature encryption does not match the DSP software programmed in the radio. If this option was not enabled or the Audio/Logic Board was changed, feature encryption will not be correct. Obtain new feature encryption data or DSP software.

NOTE

If Aegis feature encryption is not enabled or the EDACS-2 PC Software Programmer is not greater than V4.0, then no error is displayed at power up and Aegis digital does not work.

ERR=0854 The RCP was unable to successfully load operating software into the DSP. Either the data was corrupted during loading due to a hardware failure or the data stored in flash

EEPROM is corrupted. If a board swap indicates the problem is in the Audio/Logic Board, first try to reprogram the radio. Then check signals listed in ERR=0856.

ERR=0855 See ERR=0854.

ERR=0856 The RCP was unable to communicate with the DSP or the DSP failed its power-up tests. If a board swap indicates the problem is in the Audio/Logic Board, check the connectors, power (SW_A+), D0-D7, RD, WR, A8, CRYPT_CS and DSP CS, signals.

AUDIO FAILURES

Audio Failures generally will not result in error messages.

Transmit Audio

If there is a transmit audio problem, check for microphone audio at P910-33 when transmitting. The level should be approximately 550 mVRMS when the microphone input is adjusted to standard test conditions (1000 Hz tone, level equivalent to 3 kHz analog deviation). If audio is not present, check for audio on P701.4 of the audio amplifier board (19D904025).

Receive Audio

If there is a receive audio problem, check for recovered vocoded audio at P910-10. If audio is present, check the ASP on the Audio/Logic Board. The level should be approximately 300 mVRMS when a Aegis signal at the standard test condition level is transmitted.

Aegis Module

If the Aegis module is defective, replacement is recommended. In addition to obvious mechanical damage, the following may be checked before replacing the module.

1. Regulators U21 and U23 should produce 4.75 to 5.25 VDC at test points TP3 and TP4, respectively.

2. Regulator U22 should produce 7.5 to 8.5 VDC at test point TP6.

3. The 9.8304 MHz crystal oscillator operation can be checked at test point TP165. The oscillator should run briefly at power-up and continuously during Aegis transmit or receive operation.

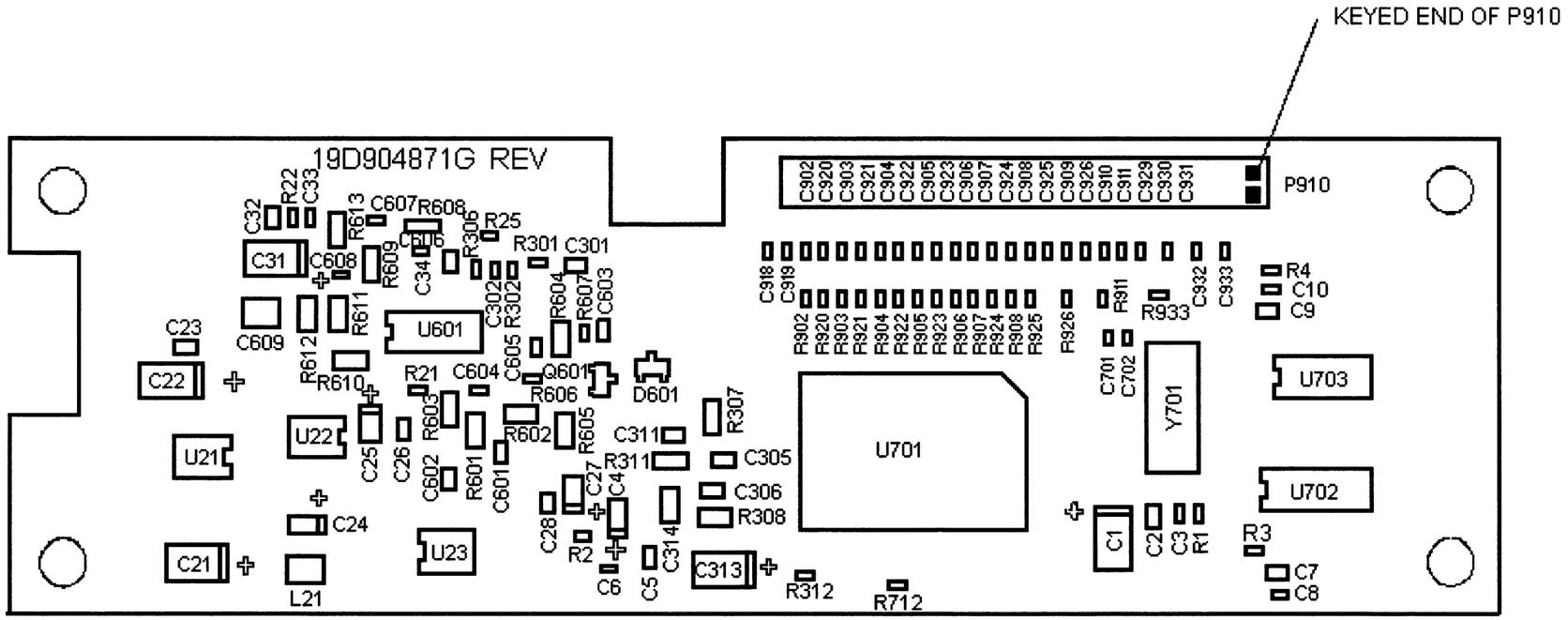
4. If receive audio is absent or highly distorted, check for 4 VDC bias at U601.1 (TP7). If incorrect, check the bias circuit consisting of R21, R22, C31 thru C34 and U601.1. Also check for recovered audio at U701-57 (TP166) and -58 (TP157). If present, check for audio at test point TP152. If not present, check R601-R605, C601, C602, C604, C605 and U601.2. If present, check for preemphasized audio at TP147. If not present, check R608-R613, C606-C609 and U601.4. If present, check U701-48 (TP149) (RESET). If RESET is at a low voltage level, the audio is being muted by the RCP on the Audio/Logic Board unless something is wrong with the latch circuitry of U702, U703.1 and U703.2. If is at a high voltage level, check Q601, R606, R607, D601 and C603.

5. If there is a problem with transmit operation, check for audio at TP134. If not present, check R301, R302, C301, C302 and U601.3. If audio is present at TP134, check R307, R308, C305 and C306.

AEGIS MODULE
19D904871G1
ISSUE 1

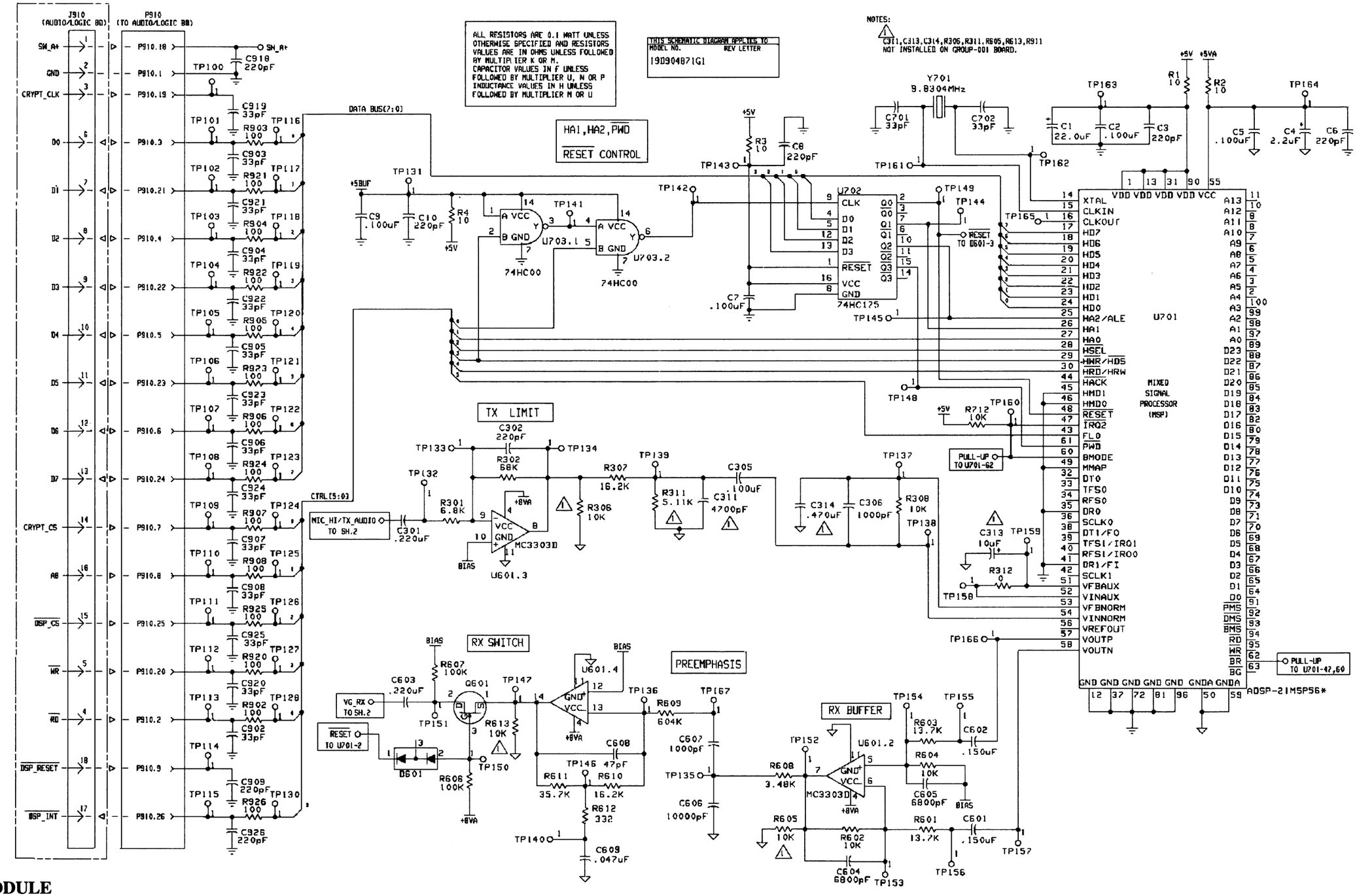
SYMBOL	PART NO.	DESCRIPTION
		------- CAPACITORS ----
C1	19A705205P223	Tantalum: 0.1 µF ±20%, 6 VDCW.
C2	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C3	19A149897P47	Ceramic: 220 pF ±5%, temp coef 0 ±30 PPM.
C4	19A705205P19	Tantalum: 2.2 µF ±20% 10 VDCW.
C5	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C6	19A149897P47	Ceramic: 220 pF ±5%, temp coef 0 ± 30 PPM.
C7	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C8	19A149897P47	Ceramic: 220 pF ±5%, temp coef 0 ± 30 PPM.
C9	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C10	19A149897P47	Ceramic: 220 pF ±5%, temp coef 0 ± 30 PPM.
C21	19A705205P206	Tantalum: 10 µF ±20% 16VDCW.
C22	19A705205P223	Tantalum: 0.1 µF ±20%, 6 VDCW.
C23	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C24	19A705205P226	Tantalum: 3.3 µF ±10% 16 VDCW.
C25	19A705205P19	Tantalum:2.2 µF ±20% 10 VDCW.
C26	19A702052P134	Ceramic: 0.1 µF ±10%, 25 VDCW.
C27	19A705205P19	Tantalum:2.2 µF ±20% 10 VDCW.
C28	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C31	19A705205P223	Tantalum: 0.1 µF ±20%, 6 VDCW.
C32	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C33	19A149897P47	Ceramic: 220 pF ±5%, temp coef 0 ± 30 PPM.
C34	19A702052P134	Ceramic: 0.1 µF ±5%, 25 VDCW.
C301	19A702052P45	Ceramic: 0.22 µF ±10%, 16 VDCW.
C302	19A149897P47	Ceramic: 220 pF ±5%, temp coef 0 ± 30 PPM.
C305	19A702052P34	Ceramic: 0.1 µF ±10%, 25 VDCW.
C306	19A702052P5	Ceramic: 1000 pF ±10% 50 VDCW.
C601 and C602	19A702052P143	Ceramic: 0.15 µF ±5% 16 VDCW.
C603	19A702052P45	Ceramic 0.22 µF ±10%, 16 VDCW.
C604 and C605	19A149896P19	Ceramic: 6800 pF ±5%, 50 VDCW.
C606	19A149896P21	Ceramic: 0.01 µF ±5%, 50 VDCW.
C607	19A149896P9	Ceramic: 1000 pF ±5%, 50 VDCW.
C608	19A149897P131	Ceramic: 47 pF ±1%, temp coef 0 ± 30 PPM.
C609	19A702052P122	Ceramic: 0.047 µF, ±5%, 50 VDCW.
C701 and C702	19A149897P27	Ceramic: 33 pF ±5% 50 VDCW temp coef 0 ± 30 PPM.
C902 thru C908	19A149897P27	Ceramic: 33 pF ±5% 50 VDCW temp coef 0 ± 30 PPM.
C909 thru C911	19A149897P47	Ceramic: 220 pF ±5%, temp coef 0 ± 30 PPM.
C918	19A149897P47	Ceramic: 220 pF ±5%, temp coef 0 ± 30 PPM.
C919 thru C925	19A149897P27	Ceramic: 33 pF ±5% 50 VDCW temp coef 0 ± 30 PPM.
C926	19A149897P47	Ceramic: 220 pF ±5%, temp coef 0 ± 30 PPM.
C929 thru C933	19A149897P47	Ceramic: 220 pF ±5%, temp coef 0 ± 30 PPM.
		------- DIODE -------
D601	19A700053P2	Silicon.
		-------- COIL ----------
L21	19A705470P25	Coil, Fixed: 1 µH ±20%; sim to Toko 380LB-IROM.
		-------- PLUGS --------
P910	19A116572P9	Connector:
		------- RESISTORS -----
R1 thru R4	19A149818P100	Metal Film: 10 ohms ±5%, 1/16w.
R21	19A149818P104	Metal Film: 100K ohms ±5%, 1/16w.
R22	19A149818P913	Metal Film: 91k ohms ±5%, 1/16w.
R301	19A149818P682	Metal Film: 6.8K ohms ±5%, 1/16w.
R302	19A149818P683	Metal Film: 68K ohms ±5%, 1/16w.
R307	19A702931P321	Metal Film: 16.2K ohms, ±1%, 1/8w.
R308	19A702931P301	Metal Film: 10K ohms ±1%, 1/8w.
R312	19A149818P0R0	Metal Film: 0 ohms.
R601	19A702931P314	Metal Film: 13.7K ohms ±1%, 1/8w.
R602	19A702931P301	Metal Film: 10K ohms ±1%, 1/8w.
R603	19A702931P314	Metal Film: 13.7K ohms ±1%, 1/8w.
R604	19A702931P301	Metal Film: 10K ohms ±1%, 1/8w.
R606 and R607	19A149818P104	Metal Film:100K ohms ±5%, 1/16w.
R608	19A702931P253	Metal Film: 3.48K ohms ±1%, 1/8w.
R609	19A702931P476	Metal Film: 604K ohms ±1%, 1/8w.
R610	19A702931P321	Metal Film: 16.2K ohms ±1%, 1/8w.
R611	19A702931P354	Metal Film: 35.7K ohms ±1%, 1/8w.
R612	19A702931P151	Metal Film: 332 ohms ±1%, 1/8w.
R712	19A149818P103	Metal Film: 10K ohms ±5%, 1/16 W.
R902 thru R908	19A149818P101	Metal Film: 100 ohms ±5%, 1/16w.
R920 thru R926	19A149818P101	Metal Film; 100 ohms ±5%, 1/16w.
R933	19A149818P0R0	Metal Film: 0 ohms.
		---- INTEGRATED CIRCUITS ----
U21	19A704971P9	Regulator: 5V; sim to MC78L05ACD.
U22	19A704971P11	Regulator: 8V; sim to MC78L08ACD.
U23	19A704971P9	Regulator: 5V; sim to MC78L05ACD.
U601	19A704883P2	Op-amp, Quad; sim to MC3303D.
U701	349A9662G1	ADI ROM: includes RYTUA1304001/2C.
U702	19A704380P310	Flip-Flop: CMOS Dual J-K w/reset; sim to 74HCT107.
U703	19A703483P302	Quad 2-Input NAND Gate; sim to 74HC00.
		------- CRYSTALS ------
Y701	19A702511G70	XTAL UNIT: 9.8304 MHz.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES



AEGIS MODULE
19D904871G1

(19D904871, Rev. 0)



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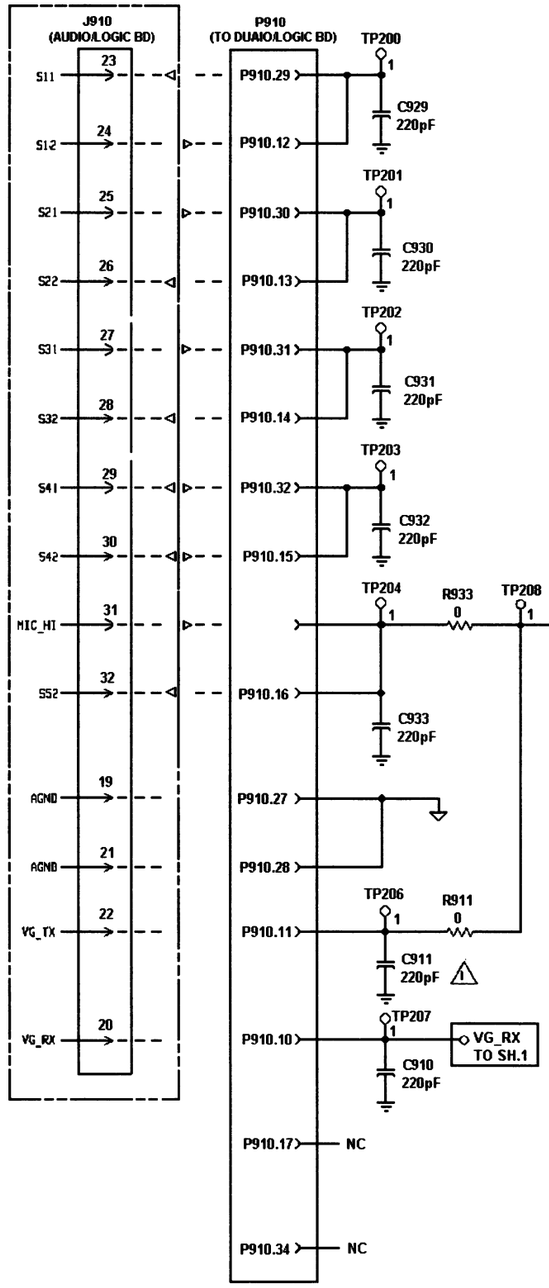
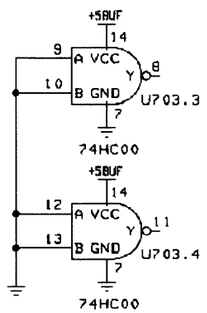
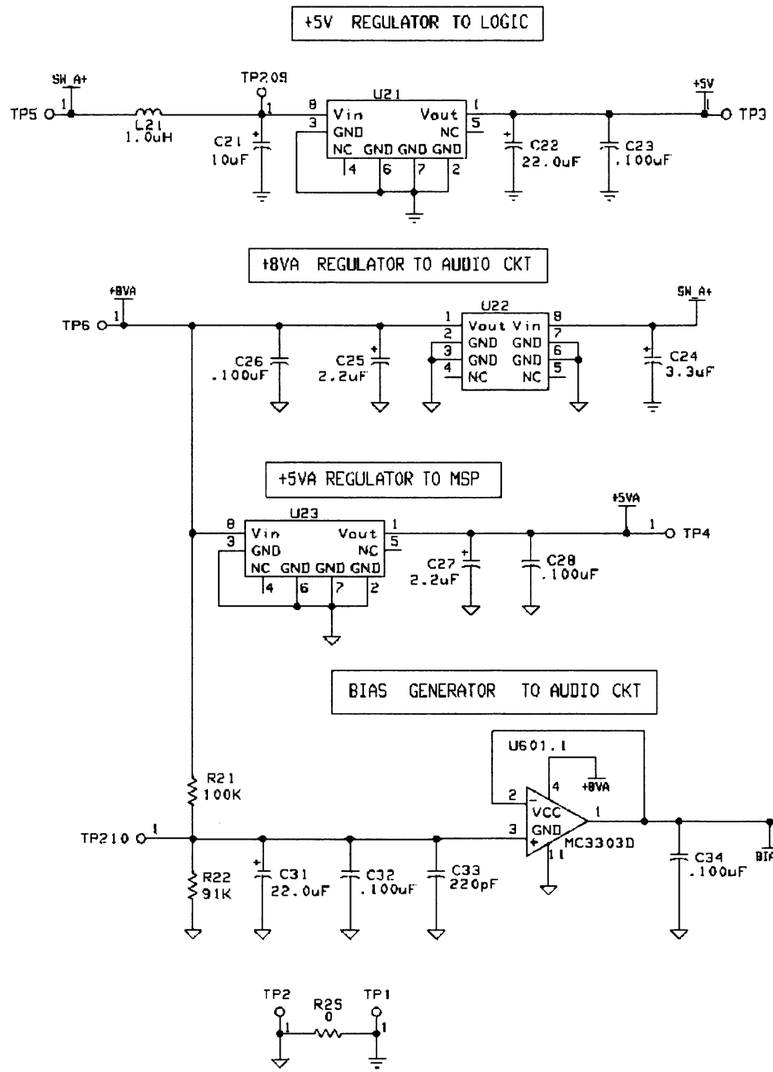
(19D904870, sh. 1, Rev. 0)



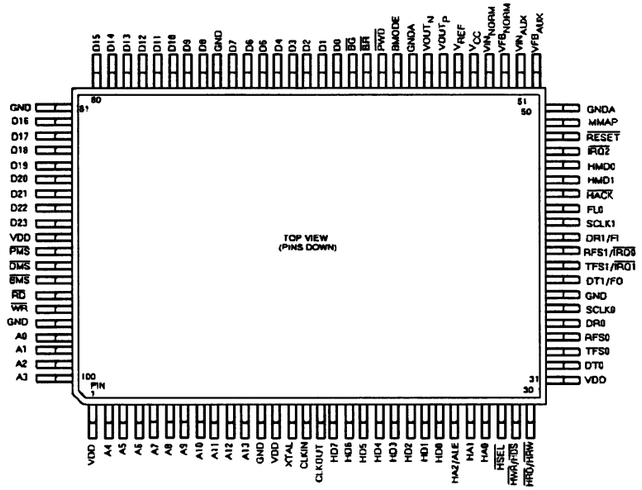




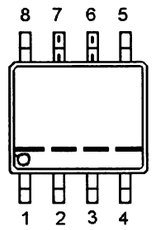
AEGIS MODULE
19D904871G1

(19D901870, Sh. 2, Rev. 0)

U701
RYTUA134001/1C
DIGITAL SIGNAL PROCESSOR

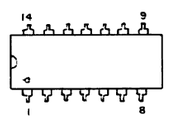


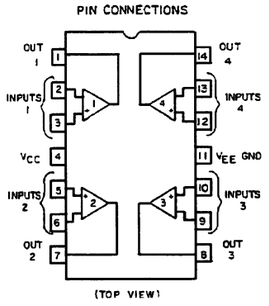
U21 & U23
19A704971P9
5 VDC REGULATOR



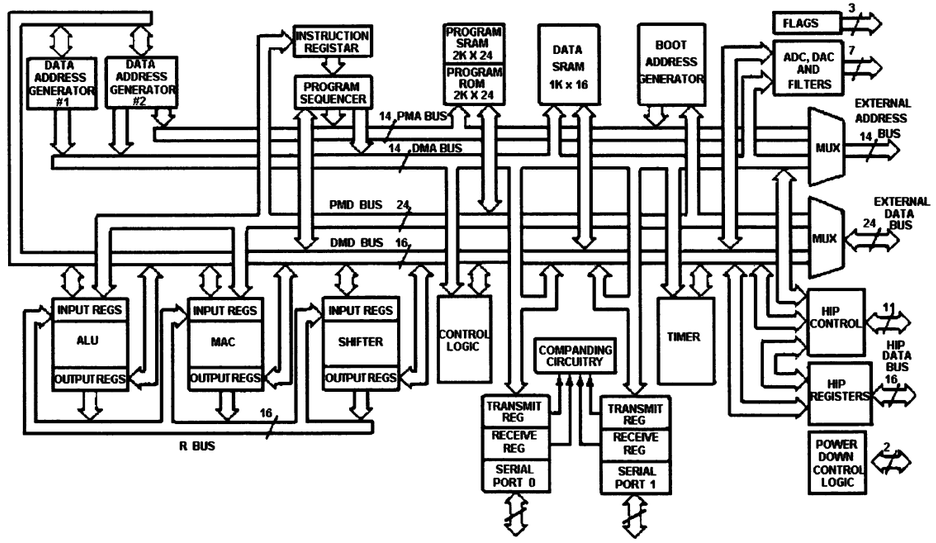
PIN	FUNCTION
1	Vout
2	GROUND
3	GROUND
4	N.C.
5	N.C.
6	GROUND
7	GROUND
8	Vin

U601
19A704883P2
OP AMP

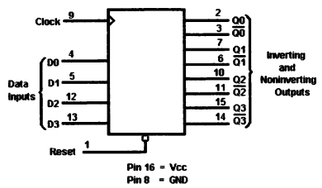




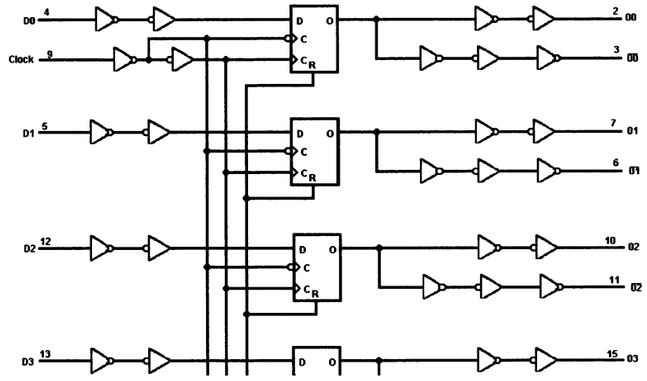
U702
19A704380P310
DUAL DATA F/F



LOGIC DIAGRAM

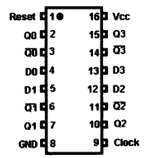


EXPANDED LOGIC DIAGRAM



U703
19A703483P302
QUAD 2-INPUT NAND GATE

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs	
Reset	Clock	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	no change