MAINTENANCE MANUAL

AUDIO MATRIX BOARD
P29/7720030000
(344A3927P33)

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TABLE 1 – AUDIO MATRIX BOARD FRONT PANEL CONNECTORS

CONNECTOR	FRONT PANEL LABELING	TYPE/STYLE	USE
J1	SUPERVISOR HEADSET	DB-9 subminiature	supervisor's headset connections
J2	OPERATOR HEADSET	DB-9 subminiature	operator's headset connections
J3	DESK MIC	DB-9 subminiature	desk microphone connections
J4	BOOM/GOOSE MIC	DB-9 subminiature	boom/gooseneck microphone connections
J5	COMPUTER	DB-37 subminiature	Personal Computer (PC) connections

DESCRIPTION

Audio Matrix Board P29/7720030000 is used in the C3 Maestro console's Audio Tower. The board's main function is to switch the console's audio from circuit-to-circuit, as needed, using a matrix of cross-point switches. The board contains the interface circuits for the:

- operator and supervisor headsets
- desk microphone
- boom or gooseneck microphone
- Call Director patch
- paging input
- tone input from PC
- external recorders

In addition, the board also contains:

- two (2) From-A relay output circuits (SPST normally open contacts)
- two (2) optoisolated digital input circuits

All board inputs and outputs are via the front panel DB-9 and DB-37 connectors and the Audio Tower's Backplane. The board contains only combinational logic circuitry and analog circuits – it is controlled entirely by the external PC system through the DB-37 connector located on the front panel.

CIRCUIT ANALYSIS

VOLTAGE REGULATOR AND REFERENCE CIRCUITS

+12-Volt Regulator

DC power is supplied through the Audio Tower's Backplane to connector J6 of the Audio Matrix Board. Fifteen-volts dc (15 Vdc) from J6 pins 5 and 6 is applied to the input of +12-volt linear regulator VR1. Capacitors C155 and C157 provide regulator input decoupling. The regulator's 12 Vdc output is applied to the analog circuits on the board via the +12V line, to the VCLAMP circuit, and to the VBIAS voltage reference circuit. Capacitors C156 and C138 provide decoupling for the regulator's output. Additional decoupling capacitors are located throughout the board. [Schematic Diagram sheet 1.]

+5-Volt Regulator

VR2 is a +5-volt linear regulator which is also supplied +15 Vdc from J6 pins 5 and 6. This regulator's output is fed to the digital circuits on the board via the +5V line. C140 is the input decoupling capacitor and C139 and C146 decouple the regulator's output. As with the +12V supply line, additional decoupling capacitors for the +5V line are located throughout the board. [Schematic Diagram sheet 1.]

VBIAS Voltage Reference

One-fourth of quad op amp U11 (pins 5, 6 & 7) and the associated components are used to generate a 6.0 Vdc voltage reference for the board. This voltage reference biases the op amp circuits on the board.

Resistors R60 and R61 form a voltage divider, applying 6.0 Vdc to the non-inverting (+) of U11 at pin 5. Through R61A, voltage follower U11 then charges C45 and the other large-value filter capacitors on the VBIAS line. As shown in the "POWER TABLE" on the schematic diagram, U11 is powered by the +12V supply line at U11 pin 4. [Schematic Diagram sheet 1.]

LOGIC BOARD INTERFACE

Logic Inputs (from Logic Board)

The Audio Matrix Board's logic inputs from the Logic Board within the PC consist of the address, chip select, data and strobe lines. These logic inputs control the audio switching circuits on the board. They are applied to the Audio Matrix Board's logic inputs via the interconnect cable and DB-37 connector J5.

Each input line (J5 pins 1 - 12) passes through an R-C filter network to provide signal conditioning and to reduce harmonic emissions from the interconnect cable. To ensure correct logic levels, each conditioned input is next applied a Schmitt-trigger buffer (inverter) within U18 or U19. The buffered logic lines are labeled ADDR0 through ADDR5 (address), SEL0 through SEL3 (chip select), DATA and STROBE. They are applied to logic inputs of various chips on the board such as the chip select decoder and the digital pots. [Schematic Diagram sheet 2.]

The address, data and strobe inputs are protected from voltage and current surges by two clamping diodes on each line and the VCLAMP circuitry. The lower diode (D29 for example) clamps negative surges directly to ground and the upper diode (D30 for example) clamps positive surges in excess of 10.5 Vdc to ground via the VCLAMP line. VCLAMP is generated from the +12V supply line using dropping resistor R91 and 10-volt zener diode ZD7. [Schematic Diagram sheets 1 and 2.]

Logic Outputs (to Logic Board)

Active-Low Outputs

Eleven (11) active-low logic outputs are applied to the Logic Board via J5 pins 15 thru 25 and the interconnecting cable. These outputs include PTT lines from the microphone connectors and other sense lines such as the boom/gooseneck microphone sense line. When inactive (for example – not PTTed), each output is pulled-up to a 12 Vdc level by a 470-ohm pull-up resistor. R-C networks on each line prevent flash Logic Board triggering from noise induced on the interconnect cable. They also perform switch de-bouncing. [Schematic Diagram sheet 3.]

The Logic Board delivers a current-limited 12 Vdc (±0.1 Vdc) power source to the Audio Matrix Board via J5 pin 35 (PTT_PWR_PC). This power is used to pull-up the active-low output lines, thus effectively isolating the output lines from any Audio Matrix Board power supply. As a result, the Audio Tower can be powered down without activating the Logic Board's PTT active-low input circuits.

Power Status Output

An Audio Tower power status logic signal (PWR_STAT_PC) is sent to the Logic Board in the PC via J5 pin 13 and the interconnecting cable. Op amp U12 (pins 8, 9 & 10) compares the eight (8) audio matrix chips' reset line and the VBIAS voltage reference. U12 pin 8 transitions high (to ≈ +12 volts) just after power-up and it remains high as long as the Audio Tower stays powered-up. The Logic Board constantly monitors PWR_STAT_PC to determine the Audio Tower's power state. If PWR_STAT_PC drops low and returns high, the Logic Board will reset and reload all cross-point switches within matrix chips U1 – U8. [Schematic Diagram sheet 1.]

I/O Board Digital Inputs (to Logic Board)

The Audio Matrix Board has two (2) optocouplers used to interface the digital inputs at front panel digital input connector J7 on the I/O Board to the Logic Board in the PC. Optocoupler U20 interfaces "DIG. IN 1" and optocoupler U24 interfaces "DIG. IN 2" (see I/O Board front panel labeling).

Inputs are applied to optocouplers via the Backplane interconnections and the associated interconnections on both plug-in boards. On the Audio Matrix Board, IO_DIGIN1_- (J6 pin 57) and IO_DIGIN1_+ (J6 pin 37) drives U20's LED and IO_DIGIN2_- (J6 pin 59) and IO_DIGIN2_+ (J6 pin 38) drives U24's LED. [Schematic Diagram sheet 3.]

The collector of each optocoupler's output transistor drives the logic line which is applied to the Logic Board. When no current is applied to the input terminals on the I/O Board, the respective pull-up resistor (R93 or R118) pulls the IO_DIGINx_PC logic line high (to +12 Vdc). If sufficient current (approximately 10 milliamps) is applied to the input terminals, the transistor's collector will pull the logic line low. The Logic Board can then read the activated digital input. R-C networks on the logic lines prevent flash Logic Board triggering from noise induced on the interconnect cable. They also perform de-bounce functions if switch or relay contacts are connected to the digital inputs.

Audio PA Board Digital Inputs (to Logic Board)

Interconnections present on the Audio Matrix Board interconnect the optocoupled digital inputs on the Audio PA Board(s) to the Logic Board. PA_DIGIN1_PC and PA_DIGIN2_PC interconnect Audio PA Board #1. If a second Audio PA Board is installed in the Audio Tower, PA_DIGIN3_PC and PA_DIGIN4_PC interconnect this #2 board's optocouplers. Interconnections are between Backplane connector J6 pins 39 thru 42 and DB-37 connector J5 pins 28 thru 31. [Schematic Diagram sheet 3.]

VU Meter Output

To provide a VU meter indication on the console's display monitor, an analog-to-digital converter circuit on the Logic Board reads a dc voltage generated on the Audio Matrix Board. This dc voltage is proportional to the level of the selected audio signal. The Logic Board selects the signal using the cross-point switches within U5 and U6. Typically, only the Line A audio input and microphone audio output lines are selected. [Schematic Diagram sheet 11.]

One-fourth of quad op amp U36 (pins 5, 6 & 7) and the associated components generate the VU_PC dc voltage at J5 pin 34. The selected audio signal is ac-coupled via C144 into the op amp's non-inverting (+) input. Since this input is held to a 0-volt bias by R215, the stage only amplifies the positive half of the audio signal applied to it. Pot R219 sets the amp's gain. With a 2.2 Vp-p, 1 kHz signal at U6 pin 6 (TP47), R219 is adjusted for a VU_PC voltage of 1.25 Vdc.

Tone Input (from Logic Board)

To provide console-generated tone support, an analog input from the Logic Board is located at J5 pin 14. This Audio Matrix Board tone input is not presently used in C3 Maestro console applications. The tones, which can be generated by the dual sine-wave generator circuits on the Logic Board, are ac-coupled via C98 and level-adjusted via R124 before being applied to the amplifier circuit formed by op amp U30 (pins 1, 2 & 3) and associated components. The TONE output line at U30 pin 1 is set by R124 for a 2.2 Vp-p level. TONE is applied to audio matrix chips. [Schematic Diagram sheets 2 and 9, 10 & 12.]

AUDIO MATRIX CONTROL

Power-Up Initialization

Capacitor C46 is located on the reset inputs of the audio matrix cross-point switch chips (pin 10 of U1 – U8). It produces reset function at power-up by temporarily holding the reset inputs low. This clears (opens) all cross-point switches. Pull-up resistors within each cross-point switch chip charges C46 via the RESET. The RESET level is monitored by the Logic Board using a comparator circuit and PWR_STAT_PC (J5 pin 13) as previously described. [Schematic Diagram sheets 1 and 9 thru 12.]

When the Logic Board senses an Audio Tower reset via PWR_STAT_PC, it initializes the Audio Matrix Board by reloading the cross-point switch chips. To ensure correct audio routing after the hardware power-up/reset, *all* switches are first sent "turn off" commands. Next, the switches that must be closed are sent "turn on" commands. Since each of the eight (8) cross-point switch chips has an 8 x 8 array, 512 "turn off" commands must be sent followed by several "turn on" commands. The address, chip select, data and strobe lines from the Logic Board load the switches as described in the following section.

Control Lines

Chip Selects

Buffered logic inputs SEL0 thru SEL3 serve as the chip select lines for the Audio Matrix Board. These logic lines drive the inputs of four-to-sixteen line decoder U23. U23's outputs select the correct chip during a switching operation. [Schematic Diagram sheets 2 and 8.]

The binary-coded nibble (4 bits) on SEL0 – SEL3 is decoded by U23 into a single mutually exclusive active output chip select. For example, if the nibble is 0111 (decimal 7), the CS7 output at U23 pin 8 will transition active (low); the other fifteen outputs will remain inactive (high). CS7 is the chip select line for cross-point matrix chip U7. [Schematic Diagram sheets 8 and 12.]

Addresses

Buffered logic inputs ADDR0 thru ADDR5 serve as the X and Y coordinates for setting the cross-point switches. ADDR0 thru ADDR2 address the X coordinate and ADDR3 thru ADDR5 address the Y coordinate. ADDR0 thru ADDR2 are also utilized to latch relay control data into addressable latches U28 and U33. [Schematic Diagram sheets 2 and 8 thru 12.]

Data and Strobe

During a matrix switch change, DATA controls on/off switch selection. It is set high to turn a switch on and low to turn a switch off. Schmitt trigger U18 (pins 5 and 6) buffers DATA_PC from the PC and applies DATA to pin 4 of each cross-point switch chip (U1 – U8). [Schematic Diagram sheets 2 and 9 thru 12.]

After the address, data and chip select on a cross-point switch chip are valid, the PC pulses STROBE to latch the switch position into the selected cross-point switch chip.

Cross-Point Switching Operation

In a switching operation, the Logic Board, under PC control, sets SEL0 thru SEL3 to the appropriate logic level to select the chip to be involved in the operation (U1 - U8). Next, DATA is set high (1) to turn on the switch or low (0) to turn off the switch and then the X and Y coordinate of the switch to be changed is addressed via ADDR0 thru ADDR5. Finally, STROBE is toggled to latch the switch in the correct position. This sequence is required for all switch operations in the cross-point switch matrix.

Because of the variety of inputs and outputs connected to the switch matrix, many combinations of audio routing are possible. On the schematic, a potentially valid connection is indicated by a dot over that particular cross-point X–Y coordinate.

RELAY CONTROL

The Logic Board can also direct the Audio Matrix Board to turn on or off its own relays (K1 thru K3) or the relays on the Audio PA Board (K1 and K2). All Audio Tower relays provide Form-A (SPST normally open) contacts for external device control. [Schematic Diagram sheet 8.]

On the Audio Matrix Board, relay K1 energizes each time the console is keyed. K2 is not supported in current firmware.

Audio Matrix Board relay K3 provides on-hook/off-hook status control to the Call Director. This relay provides a momentary contact closure for automatically placing the CD on-hook without operator intervention. This "on-hook" relay is energized when the console disconnects the CD from the CEC/IMC due to operator manual operation or site time-out. Since most CDs do not have an on-hook input, use of this relay is optional. Via Backplane interconnections, the contacts are available at CD connector J3 on the I/O Board. See LBI-39066 for specific connector pin-out details.

Latches within U28 and U33 latch the relay drive transistor states on their Q outputs. When a Q output is high, the respective drive transistor is driven into saturation (turned on) by the associated 1K ohm pull-up resistor. Thus, the relay energizes and its contacts close. All three (3) relays on the Audio Matrix Board are powered from the +12V supply line. Drive transistors are protected from reverse

voltage surges from the relays' coils at turn-off by diodes D43 thru D45.

U28 and U33 inputs include address lines ADDR0 thru ADDR2 which address the output to be changed, DATA which provides relay on/off control, and an active-low enable input at pin 14 of each chip. Each enable is produced by NORing STROBE with an active-low output from decoder U23. Therefore, the enable input is activated (pulsed low) when the respective chip select output from U23 is brought low and STROBE is pulsed low. For example, to close IO_K1_A and IO_K1_B contacts provided by relay K1, the following sequence occurs:

- DATA is brought high (logic 1)
- SEL0, SEL2 and SEL3 are brought high (logic 1) and SEL1 is pulled low (logic 0) to select the eleventh (11) chip select line at U23 pin 13
- ADDR0, ADDR1 and ADDR2 are all brought low to select the Q0 latch within U33 (Q0 output at pin 4)
- STROBE is pulsed low

To open K1's contacts, the above process is repeated, except DATA is brought low instead of high.

AUDIO INPUTS

Audio Matrix Board audio inputs are applied to the board by its front panel connectors and the Backplane connector. The Logic Board in the PC has master control of the audio input circuits, all of which condition the input audio and apply it to the audio switching matrix formed by cross-point switch chips U1 thru U8. All cross-point inputs operate on a 6-volt bias and the audio signals are adjusted for a nominal 2.2 Volts peak-to-peak signal level. Signals greater than 2.2 Vp-p may cause crosstalk problems within the audio matrix.

Supervisor Headset Mic

The supervisor's headset connects to DB-9 connector J1 on the front panel of the Audio Matrix Board. This connector is labeled "SUPERVISOR HEADSET".

The supervisor's headset can be keyed from the custom keyboard, footswitch, or the SUPR_PTT input at J1 pin 6. The Logic Board reads SUPR_PTT via SUPR_PTT_PC at J5 pin 15. [Schematic Diagram sheets 3 and 4.]

Headset microphone audio is applied to SUPR_MIC_IN at J1 pin 9. Resistor R1 supplies a dc bias from the +12V line which is required to power the headset. Fifteen-volt zener diodes ZD1 and ZD2 provide static discharge surge protection for the input amp. [Schematic Diagram sheet 4.]

The moderate-level (approximately 200 mVp-p) SUPR_MIC_IN mic audio signal is ac-coupled by C2 into an inverting buffer circuit formed by op amp U13 (pins 12, 13 & 14) and associated components. This stage does not provide any voltage gain. C25 sets the -3 dB roll-off point to approximately 3 kHz for voice audio frequencies. U13's non-inverting input (+) is biased to VBIAS (6.0 Vdc) and thus the output signal at pin 14 rides on a 6-volt bias. The output signal is level-adjusted by pot R55 before being applied to the supervisor headset mic AGC (automatic gain control) circuit via R56 and C42.

One-half of U16 (pins 9 – 16), a dual transconductance op amp, and the associated components form the supervisor headset mic AGC circuit. This circuit provides AGC for the mic audio, but its primary function is to pre-limit the mic audio to a safe level for the remainder of the supervisor headset mic amp circuits. The gain-controlled/limited output from U16 pin 12 is applied to op amp voltage follower U21. The output of this stage at U21 pin 14 is applied to another limiter stage.

Op amp U13 (pins 1, 2 & 3) and associated components form a fast-limiter circuit. This output is then scaled by divider network R73 and R74 and applied to a high-pass filter formed by U13 (pins 5, 6 & 7) and the associated components. This filter reduces any low-frequency signals such as 60 Hz hum which may exists on the mic audio. The output is fed to a low-pass filter formed by U13 (pins 8, 9 & 10) and the associated components. This filter reduces any high-frequency hiss present in the mic signal. All limiters and filters operate on the 6.0 Vdc bias.

The low-pass filter's output at U13 pin 8 is ac-coupled into the high-side of digital pot U25 at pin 11. This digitally-controlled potentiometer allows the supervisor's headset mic level to be set by commands from the Logic Board. Normally, the pot is set for no attenuation (wiper/pin 12 internally connected to high-side/pin 11). C117 ac-couples the signal on the wiper (U25 pin 12) into a mic buffer/filter circuit formed by U31 and associated components. The output of this circuit, SUPR_MIC_OUT (U31 pin 1), is applied to cross-point switch chips U1, U2, U3, U4 and U8 for distribution as needed. [Schematic Diagram sheets 4, 9, 10 and 12.]

SUPR_MIC_OUT is also applied to the supervisor sidetone level adjustment circuit consisting of potentiometers R178, one-half of U26, and the associated components. U26 is a digitally-controlled pot which can be set via the Logic Board using the Editor program.

NOTE

See LBI-39056 for specific details on the C3 Maestro Editor program.

A 2.5 Vdc bias for U25 and U26 is generated from the +5V supply line and the divider network formed by R151 and R152. Capacitor C104 provides decoupling. VPOTBIAS is applied to the low sides of both digital pots. [Schematic Diagram sheets 4 and 6.]

The attenuated sidetone signal, SUPR_SIDE-TONE_OUT (TP32), is applied to the cross-point switch chip U8 at pin 9. This sidetone signal is summed with other signals and applied to the supervisor's headset earphones. It may also be summed with other signals and applied to the operator's headset earphones. [Schematic Diagram sheet 12.]

See the section entitled "**DIGITAL POT CONTROL**" for circuit analysis details describing how the digital pots' settings are changed.

Operator Headset Mic

The operator's headset connects to DB-9 connector J2 on the front panel of the Audio Matrix Board. This connector is labeled "OPERATOR HEADSET".

This headset can be keyed from the custom keyboard, footswitch, or via the OPR_PTT input at J2 pin 6. The Logic Board reads OPR_PTT via OPR_PTT_PC at J5 pin 16. [Schematic Diagram sheets 3 and 5.]

Mic audio is applied to J2 pin 9, OPR_HEAD-SET_MIC_IN. Resistor R2 supplies a dc bias from the +12V line which is required to power the headset. Zener diodes ZD3 and ZD4 provide static discharge surge protection. [Schematic Diagram sheet 5.]

The moderate-level (approximately 200 mVp-p) OPR_HEADSET_MIC_IN mic audio signal is ac-coupled by C9 into a buffer circuit formed by U11 (pins 8, 9 & 10) and associated components. This op amp stage does not provide any voltage gain. C29 sets the -3 dB roll-off point to approximately 3 kHz. U11's non-inverting input (+) is biased to VBIAS (6.0 Vdc) and thus the output signal at pin 8 rides on a 6-volt bias. The output signal is level-adjusted by pot R59 before being applied to the operator headset mic AGC circuit.

This AGC circuit is formed by one-half of U16 (pins 1 – 8) and the associated components. The gain-controlled/limited output from U16 pin 5 is applied to voltage follower op amp U21. At an average voice signal into the microphone, the signal at U21 pin 8 (TP18) is adjusted to 2.2 Vp-p via R59. This signal, OPR_HEADSET_MIC, is applied to pin 22 of cross-point switch chip U6 for operator mic source selection. [Schematic Diagram sheets 5 and 11.]

Desk Mic

The console's desk microphone connects to DB-9 connector J3 on the front panel of the Audio Matrix Board. This connector is labeled "DESK MIC".

A desk mic can be keyed from the custom keyboard, footswitch, or the DESK_PTT input at J3 pin 6. The Logic Board reads DESK_PTT via DESK_PTT_PC at J5 pin 18. A boom/gooseneck mic has priority over a desk mic when no headset is plugged into the Audio Tower. [Schematic Diagram sheets 3 and 5.]

Mic audio is applied to J3 pin 9, DESK_MIC_IN. The network formed by R4, R5 and R18 applies a dc bias on DESK_MIC_IN which is required by the mic amplifier circuit inside the desk mic. C8 decouples the network's bias. Zener diodes ZD5 and ZD6 provide static discharge surge protection.

The high-level DESK_MIC_IN mic audio signal (approximately 750 mVp-p) is ac-coupled by C28 into a buffer circuit formed by U11 (pins 12, 13 & 14) and associated components. This op amp stage does not provide any voltage gain. C10 sets the -3 dB roll-off point to approximately 3 kHz. U11's non-inverting input (+) is biased to VBIAS (6.0 Vdc) and thus the output signal at pin 14 rides on a 6-volt bias. The output signal is next level-adjusted by pot R88 before being applied to the desk mic AGC circuit.

The desk mic AGC circuit is formed by one-half of U17 (pins 1 – 8), a dual transconductance op amp, and the associated components. The gain-controlled/limited output from U17 pin 5 is applied to buffer op amp U21. At an average voice signal into the microphone, the signal at U21 pin 7 (TP20) is adjusted to 2.2 Vp-p via R88. This signal, DESK_MIC, is applied to pin 7 of cross-point switch chip U6 for operator mic source selection. [Schematic Diagram sheets 5 and 11.]

Boom/Gooseneck Mic

If used, the console's boom/gooseneck microphone connects to DB-9 connector J4 on the front panel of the Audio Matrix Board. This connector is labeled "BOOM/GOOSE MIC".

A boom/gooseneck mic can be keyed from the custom keyboard, footswitch, or the B/G_PTT input at J4 pin 6. The Logic Board reads B/G_PTT via B/G_PTT_PC at J5 pin 19. [Schematic Diagram sheets 3 and 5.]

In addition, the Logic Board reads B/G_MIC_SENSE_PC (J5 pin 17) to determine if a boom or gooseneck microphone is connected to J4. If connected, a jumper inside the mic's DB-9 (male) connector grounds B/G_MIC_SENSE at J4 pin 3. In this condition, the Logic Board ignores the any PTT activity and mic audio from the

desk mic connector (J3 pins 6 and 9 respectively). The boom/gooseneck mic has priority over the desk mic when no headset is plugged into the Audio Tower.

NOTE

All boom/gooseneck mic connectors (male DB-9) must have pins 2 and 3 jumpered together so B/G_MIC_SENSE will be activated (grounded) when the mic is connected to J4.

Mic audio from the boom or gooseneck microphone is applied to J4 pin 9, B/G MIC HI. Since the microphone has a magnetic cartridge-type mic element, no dc bias is needed on B/G MIC HI. Diodes D5 and D6 provide static discharge surge protection.

Capacitor C13 ac couples the low-level mic signal (typically less than 10 mVp-p) into the mic amp circuit formed by U11 (pins 1, 2 & 3) and associated components. This stage provides approximately 30 dB of gain at voice frequencies. C12 sets the -3 dB roll-off point to approximately 3 kHz. U11's non-inverting input (+) is biased to VBIAS (6.0 Vdc) and thus the output signal at pin 1 rides on a 6-volt bias. The output signal is next level-adjusted by pot R86 before being applied to the AGC circuit.

The boom/gooseneck mic audio AGC circuit is formed by one-half of U17 (pins 9 – 16) and the associated components. The gain-controlled/limited output from U17 pin 12 is applied to buffer op amp U21. At an average voice signal into the microphone, the signal at U21 pin 1 (TP19) is adjusted to 2.2 Vp-p via R86. This signal, B/G_MIC, is applied to pin 23 of cross-point switch chip U6 for operator mic source selection. [Schematic Diagram sheets 5 and 11.]

Non-Supervisory Mic Audio Selection And Conditioning

The Logic Board selects one non-supervisory mic audio signal (OPR_HEADSET_MIC, DESK_MIC or B/G_MIC) based on the boom/gooseneck mic sense input (J4 pin 3) and the operator headset sense input (J2 pin 3). It connects the selected source to OPR_MIC using cross-point switch U6. The operator headset has the highest priority and the desk mic has the lowest. In other words, desk mic PTTs will be ignored if a headset is connected to J2. [Schematic Diagram sheets 5 and 11.]

The OPR_MIC signal from U6 pin 15 is applied to a fast-limiter circuit formed by U30 (pins 12, 13 & 14) and the associated components. This output is then scaled by divider network R143 and R144 and applied to a high-pass filter formed by U30 (pins 8, 9 & 10) and the associated components. This filter reduces any low-frequency signals such as 60 Hz hum which may exists on the non-supervisory mic audio. The output is fed to a low-pass filter formed by U30 (pins 5, 6 & 7) and the associated components. This filter reduces high-frequency hiss. Both filters and the limiter operate on the 6.0 Vdc bias. [Schematic Diagram sheet 6.]

The low-pass filter's output at U30 pin 7 is ac-coupled into the high-side of digital pot U25 at pin 2. This digitally-controlled potentiometer allows the selected non-supervisory mic level to be set by commands from the Logic Board. Normally, the pot is set for no attenuation (wiper/pin 4 internally connected to high-side/pin 2). C121 ac-couples the signal on the wiper (U25 pin 4) into a mic buffer/filter circuit formed by U31 and associated components. The output of this circuit, OPR_MIC_OUT (U31 pin 7), is applied to cross-point switch chips U1, U2, U3, U4 and U8 for distribution as needed. [Schematic Diagram sheets 6, 9, 10 and 12.]

OPR_MIC_OUT is also applied to the operator sidetone level adjustment circuit consisting of potentiometers R194, one-half of U26, and the associated components. U26 is a digitally-controlled pot which can be set via <Alt> <Vol ↑ > (increase sidetone) and <Alt> <Vol ↓ > (decrease sidetone) keystrokes at the C3 Maestro's custom keyboard. The Editor program can also set the pot. See the following section entitled "**DIGITAL POT CONTROL**" for circuit analysis details describing how the digital pots' settings are changed.

NOTE

See LBI-39056 for specific details on the C3 Maestro Editor program.

A 2.5 Vdc bias for U25 and U26 is generated from the +5V supply line and the divider network formed by R151 and R152. Capacitor C104 provides decoupling. VPOTBIAS is applied to the low sides of both digital pots. [Schematic Diagram sheets 4 and 6.]

The attenuated sidetone signal, OPR_SIDE-TONE_OUT (TP31), is applied to the cross-point switch chip U7 at pin 7. This sidetone signal is summed with other signals and applied to the operator's headset earphones. It may also be summed with other signals and applied to the supervisor's headset earphones. [Schematic Diagram sheet 12.]

Line Inputs

Each line input signal (LINE_A_IN thru LINE_D_IN) from the line receivers on the Audio PA Boards is buffered by an op amp within quad op amp U22 before application to the cross-point switch chip U6. U6 provides primary signal

distribution for the line inputs. [Schematic Diagram sheet 11.]

Line A & B signals are applied from Audio PA Board #1 and Line C & D signals are applied from Audio PA Board #2 (if installed). Backplane connector J6 pins 7, 8, 9 and 10 are the Line A, B, C and D inputs, respectively.

Call Director Mic

Balanced CD line input ("CD mic") audio signals from the Call Director are applied to the Audio Tower at DB-9 connector J3 on the I/O Board's front panel. These audio signals are routed to the Audio Matrix Board by the associated Backplane interconnections. CD_MIC_HI (J6 pin 29) and CD_MIC_LO (J6 pin 27) are applied to the primary or line-side of 600-ohm coupling transformer T2 via dc blocking capacitor C158. [Schematic Diagram sheet 8.]

NOTE

Jumper JP1 on the primary (line or output) side of T2 is *not* normally required. It should only be installed if the Audio Matrix Board is installed in an earlier Audio Tower (equipped with Backplane P29/5000058000). If JP1 is used, an external in-line isolation "transformer box" must also be installed in the CD mic line from the Call Director. JP1 installation is not required if the earlier Audio Tower is not connected to a Call Director.

Surge protection on the secondary side of T2 is performed by clamping diodes D37 thru D40 and zener diode ZD7. D37 and D40 clamp surges in excess of 10-volts to ground via ZD7. D38 and D39 clamp negative surges directly to ground. [Schematic Diagram sheets 1 and 8.]

To provide level adjustment, the CD mic signal on T2's secondary is applied across pot R182. The attenuated signal on the pot's wiper drives the input of a non-inverting op amp stage formed by U34 (pins 12, 13 & 14) and the associated components. Capacitor C128 in the op amp's feedback loop provides a -3 dB roll-off at 3 kHz.

The conditioned CD signal at U34 pin 14 is applied to the cross-point switch chips for distribution as required. During a Call Director patch, U3 routes the CD signal (at U3 pin 8) to the CEC/IMC's CIM via the LINE_D_OUT connection at J6 pin 20, the Backplane interconnections, and the Line B driver circuits on the second (#2) Audio PA Board. [Schematic Diagram sheet 10.]

Using U7 and U8, incoming CD audio may be summed with incoming radio audio so the dispatcher can monitor both sides of the conversation. [Schematic Diagram sheet 12.]

Pager

A pager input is furnished on the I/O Board's front panel terminal block J2. This terminal block has a removable screw-terminal connector. A single-ended audio input (600-ohm) and a pager PTT input are included. See LBI-39066 for J2 pin-out details.

The pager PTT input is routed through the Backplane to J6 pin 50 (PAGER_PTT) and then interfaced to the Logic Board as described in the section entitled "**LOGIC BOARD INTERFACE**". [Schematic Diagram sheet 3.]

Pager audio (usually tones) from J2 on the I/O Board enters the Audio Matrix Board at J6 pin 32. C149 provides ac-coupling, R200 loads the input to 600 ohms, and D46 and D47 provide surge protection. The audio is next applied to level adjustment pot R199 and then to the input of amplifier stage formed by U34 (pins 8, 9 and 10) and the associated components. [Schematic Diagram sheet 8.]

Conditioned pager audio on U34 pin 8 (PAGE) is applied to several of the cross-point switch chips. Normally, only U1 switches pager audio in and out to apply it to the Line A output. PAGE is switched in when PAGER_PTT becomes active. During the page, no other audio signals are applied to the Line A output (LINE_A_OUT). The paging signal is sent to the headsets and speakers approximately 16 dB lower than other audio signals. [Schematic Diagram sheet 9.]

DIGITAL POT CONTROL

To provide computer-controlled level settings, both the audio input circuits and the audio output circuits incorporate digitally-controlled potentiometers. These digital pots allow audio levels such as headset earphone volume to be set digitally via serial data signals from the Logic Board. There are three (3) dual potentiometer chips on the Audio Matrix Board for a total of six (6) individual pots.

Both pots within U14 are utilized in the headset earphone audio output amplifier circuits – one pot is in the supervisor amp circuit and the other is in the operator amp circuit. [Schematic Diagram sheet 7.]

Similarly, both pots within U25 are incorporated into the microphone amp input circuits – one pot is in the supervisor side and the other is in the operator side. Normally, both U25 pots are digitally set for no attenuation (high side internally connected to wiper) [Schematic Diagram sheets 4 and 6.]

Both pots within U26 are incorporated into the sidetone feedback circuits – again, one pot is in the supervisor side and the other is in the operator side. The operator sidetone pot (U26 pins 2, 3 & 4) can set via <Alt> <Vol ↑ > and <Alt> <Vol ↓ > key stokes at the console's custom

keyboard. In addition, both pots within U26 can be set via the Editor program as described in LBI-39056. [Schematic Diagram sheets 4 and 6.]

The Logic Board serially loads a new pot's settings when a change occurs. This is accomplished using the DIGITAL_POT_CS_9, DIGITAL_POT_CS_10 and DIGITAL_POT_CS_13 decoded chip select outputs from decoder U23, and the DATA and STROBE lines. As previously described, U23 outputs the chip select signals by decoding the buffered SEL0 thru SEL3 inputs from the Logic Board within the PC.

The serial data stream's length is 17 bits long. DATA is the serial data, STROBE provides the clock for synchronous loading, and the DATA_POT_CS_xx outputs from U23 control which pot is selected. For example, to load both pots within U26 with new settings, DATA_POT_CS_13 transitions high (inverted active-low output from U23) to enable the chip. Next, the required setting is clocked into U26 using the DATA and STROBE lines. Finally, DATA_POT_CS_13 returns low which latches the new pot setting and disables U26 from subsequent DATA and STROBE activity. Each pot has 256 positions. [Schematic Diagram sheets 4 and 8.]

AUDIO OUTPUTS

As with the audio input circuits, the Logic Board in the PC has master control of the Audio Matrix Board's audio output circuits. All cross-point outputs operate on a 6-volt bias and the cross-point audio signals are adjusted for a nominal 2.2 Volts peak-to-peak signal level. Signals greater than 2.2 Vp-p may cause crosstalk problems within the audio matrix.

Supervisor Headset Earphone

Using the audio matrix cross-point switch chips, the Logic Board selects the correct audio to send to supervisor's headset earphones. Cross-point switch chips U6, U7 and U8 are utilized. U6 can switch in a line input audio via the BOTH_RCVRS connection at pin 18. U7 can switch in operator sidetone via pin 18, with level adjustment provided by R213. U8 can switch in the supervisory sidetone audio via pin 12, and Call Director "mic" input audio or select speaker audio (SEL_SUM) via pin 11. All signals are summed at pin 2 of op amp U36. The summed and buffered output is applied to the supervisor's headset amplifier circuit via SUPR_RCVR output at U36 pin 1. [Schematic Diagram sheets 11 and 12.]

SUPR_RCVR audio is applied to a limiter circuit formed by op amp U15 (pins 8, 9 & 10) and associated components. The audio signal on the output (U15 pin 8) will not exceed approximately 4.4 Vp-p. This output is fed to a low-pass filter formed by U15 (pins 12, 13 & 14) and the associated components. This filter reduces any high-frequency hiss which may be present in the audio signal. [Schematic Diagram sheet 7.]

The low-pass filter's output at U15 pin 14 is ac-coupled into the high-side of digital pot U14 at pin 11. This digitally-controlled potentiometer allows the supervisor's headset earphone audio level to be set by commands from the Logic Board upon volume control changes. See the section entitled "**DIGITAL POT CONTROL**" for circuit analysis details describing how the pots' settings are changed.

C26 ac-couples the signal on the wiper (U14 pin 12) into the supervisor headset earphone amplifier, U9. This audio amp IC operates with a voltage gain of 20. U9's audio output, SUPR_RCVR_OUT, is applied to the headset via J1 pin 7. [Schematic Diagram sheets 4 and 7.]

Operator Headset Earphone

Using the audio matrix cross-point switch chips, the Logic Board selects the correct audio to send to operator's headset earphones. Cross-point switch chips U6, U7 and U8 are utilized. U6 can switch in a line input audio via the BOTH_RCVRS connection at pin 18. U7 can switch in operator sidetone via pin 16, and Call Director "mic" input audio or select speaker audio (SEL_SUM) via pin 15. U8 can switch in the supervisory sidetone audio via pin 16, with level adjustment provided by R90. All signals are summed at pin 6 of op amp U12. The summed and buffered output is applied to the operator's headset amplifier circuit via OPR_RCVR. [Schematic Diagram sheets 11 and 12.]

The OPR_RCVR audio is applied a limiter circuit formed by op amp U15 (pins 5, 6 & 7) and associated components. The audio signal on the output (U15 pin 7) will not exceed approximately 4.4 Vp-p. This output is fed to a low-pass filter formed by U15 (pins 1, 2 & 3) and the associated components. This filter reduces any high-frequency hiss which may be present in the audio signal. [Schematic Diagram sheet 7.]

The low-pass filter's output at U15 pin 1 is ac-coupled into the high-side of digital pot U14 at pin 2. This digitally-controlled potentiometer allows the operator's headset earphone audio level to be set by commands from the Logic Board upon volume control changes. See the section entitled "**DIGITAL POT CONTROL**" for circuit analysis details describing how the digital pots' settings are changed.

A 2.5 Vdc bias for U14 is generated from the +5V supply line and the divider network formed by R99 and R100. Capacitor C70 provides decoupling. POTBIAS2 is applied to the low sides of both digital pots within U14.

C27 ac-couples the signal on the wiper (U14 pin 4) into the operator headset earphone amplifier, U10. This audio amp IC operates with a voltage gain of 20. U10's audio

output, OPR_RCVR_OUT, is applied to the headset via J2 pin 7. [Schematic Diagram sheets 5 and 7.]

Line Outputs

Line signals from the Audio Matrix Board are routed through the Backplane to the line drivers on the Audio PA Board. Line A and B signals are applied to the line drivers on the first (#1) Audio PA Board and Line C and D signals are applied to the line drivers on the second (#2) Audio PA Board (if installed).

Cross-point switch chip U1 switches the Line A signals into the summing network formed by resistor pack RP3, and U2 switches the Line B signals into the summing network formed by RP4. Each signal is summed at the inverting (-) input of the respective op amp The buffered line signal is applied to the Backplane via J6. Capacitors in the op amps' feedback loops provide frequency roll-off above 3 kHz. Both output signals (LINE_A_OUT at J6 pin 19 and LINE_B_OUT at J6 pin 22) ride on a 6.0 Vdc bias. As previously stated, these output signals are applied to the line drivers on the corresponding Audio PA Board. [Schematic Diagram sheet 9.]

Cross-point switch chip U3 switches the Line C and D signals into resistor packs RP6 and RP5 respectively. These output stages are basically identical to the Line A and B outputs described above. [Schematic Diagram sheet 10.]

Select Recorder

Select recorder audio at J6 pin 33 (SEL_RCDR) is a summation of the non-conditioned summed select speaker audio signal (SEL_SUM) from op amp U12 (pins 1, 2 & 3) and several other audio signals that may be switched in by U4. The summation point is pin 2 of op amp U35. This stage amplifies the summed signal and it provides level adjustment via R202. On the output, high-frequency roll-off is provided by R206 and C152. The conditioned signal is then ac-coupled to J6 pin 33 (SEL_RCDR) via C150.

SEL_RCDR audio is routed to the terminal block J1 on the I/O Board via Backplane interconnections. This terminal block has a removable screw-terminal connector. As shown in LBI-39066, select recorder audio is available on J1 pins 3 (SEL_RCDR) and 4 (GND). [Schematic Diagram sheet 10 and 12.]

Unselect Recorder

The UNSEL_RCDR output at J6 pin 31 is the sum of many audio matrix signals. Resistor pack RP9 sums the signals to pin 6 of op amp U35. Level adjustment is provided by R187 and high-frequency roll-off is provided by R201 and C147 on the stage's output. The conditioned signal is then ac-coupled to J6 pin 31 via C148.

The resultant UNSEL_RCDR audio is routed to the terminal block J1 on the I/O Board via Backplane interconnections. This terminal block has a removable screw-terminal connector. Unselect recorder audio is available on J1 pins 1 (UNSEL_RCDR or U_SEL_RC) and 2 (GND). [Schematic Diagram sheet 11.]

Call Director Receiver

The Audio Matrix Board provides balanced line output connections to the Call Director. Transformer T1 provides the signal-ended to 600-ohm balanced line transformation for the output ("CD receiver") line. CD_RCVR_HI is located at J6 pins 34 and CD_RCVR_LO is located at J6 pin 30. These balanced line connections are routed through the Backplane to connector J3 on I/O Board's front panel. See LBI-39066 for connector pin-out details. [Schematic Diagram sheet 12.]

Cross-point switch chip U8 switches the Call Director output signals on and off. These signals sum at pin 1 of resistor pack RP10. The summed signal is routed through R204 for level adjustment and applied to the CD receiver line driver stage formed by op amp U36 (pins 8, 9 and 10) and associated components. Capacitor C143 in the feedback loop provides frequency roll-off above 3 kHz. U36 pin 8 drives the primary of T1 via R203 and C151.

NOTE

Jumper JP2 on the secondary (line or output) side of T1 is *not* normally required. It should only be installed if the Audio Matrix Board is installed in an earlier Audio Tower (equipped with Backplane P29/5000058000). If JP2 is used, an external in-line isolation "transformer box" must also be installed in the CD receiver line to the Call Director. JP2 installation is not required if the earlier Audio Tower is not connected to a Call Director.

TESTS AND ALIGNMENTS

RECOMMENDED TEST EQUIPMENT

General

The following list represents test equipment required for Audio Matrix Board test and alignment procedures. Other test equipment may be substituted provided it is electrically equivalent or superior in accuracy and operational range to that which is listed.

- Hewlett Packard 204C Audio Signal Generator (600-ohm output impedance)
- Fluke 87 True-RMS Handheld Multimeter
- Tektronix 2205 Portable 20 MHz Analog Oscilloscope
- Hewlett Packard E3615A Adjustable DC Power Supply (0 – 20 Vdc)
- Extender Board 344A3927P32 (not required if stand-alone tests are performed)

Other Items

- Capacitor, 0.1 µF
- 600-ohm resistor
- Test Leads

TESTS AND ALIGNMENTS

Listed below are the test and alignment procedures for the Audio Matrix Board. All input levels are adjusted so 2.2 Vp-p amplitude signals are applied to the audio matrix cross-point switch chips when a normal signal is applied to the input. Signals greater than 2.2 Vp-p may cause crosstalk problems within the matrix. Output signals are also adjusted given a 2.2 Vp-p level matrix output. All cross-point switch inputs and outputs are biased to 6.0 Vdc.

NOTE

The following test and alignment procedures are stand-alone procedures in which the board is not connected with any other C3 Maestro console hardware item. However, most procedures may be accomplish with the Audio Tower using the Extender Board listed in the previous section entitled "**RECOMMENDED TEST EQUIPMENT**". If the Extender Board test method is used, ***do not*** apply 15 Vdc power form an external power supply; use the Audio Tower's power supply.

Set-Up Procedure

- ❑ Remove ac power from the Audio Tower.
- ❑ Remove the Audio Matrix Board.
- ❑ Record present SW1 settings and then set all four (4) positions of SW1 "ON" (closed). This enables ALC (automatic level control) on all four mic audio inputs.

Test And Alignment Procedure

1. Power-Up

- ❑ Connect the ground lead of the scope and multimeter to the board's ground, TP13 (located near the bottom of the board). [Schematic Diagram sheet 1.]
- ❑ Apply +15 Vdc from the external power supply to TP49. Ground power supply to TP9 (located near the top of the top of the board). Alternately, if the Extender Board test method is being used, power-up the Audio Tower and ***do not*** apply any power from an external power supply.
- ❑ Verify regulator VR1's output (TP38) is 12 Vdc (±0.1 Vdc).
- ❑ Verify regulator VR2's output (TP37) is 5 Vdc (±0.1 Vdc).
- ❑ Verify TP6 (VBIAS) is 6.0 Vdc (± 0.1 Vdc).

2. Boom/Gooseneck Mic Audio

- ❑ Through a 0.1 µF capacitor, couple a 1 kHz, 7 mV peak-to-peak (±1 mVp-p) audio signal into the boom/gooseneck mic audio input at J4 pin 9 (TP5). Connect the ground lead of the signal source to J4 pin 5. Maintain minimum test lead length and use shielded test leads to prevent hum (i.e. 60 Hz) from being induced in the mic input. [Schematic Diagram sheet 5.]
- ❑ Monitor TP19 (U21 pin 1) with the scope.
- ❑ Adjust R86 for a 2.2 Vp-p (±0.1 Vp-p) indication on the scope. Verify the signal is not distorted, not clipping, and riding on a 6.0 Vdc bias.

3. Desk Mic Audio

- ❑ Through a 0.1 µF capacitor, couple a 1 kHz, 750 mV peak-to-peak (±100 mVp-p) audio signal into the desk mic audio input at J3 pin 9 (TP4). Connect the ground lead of the signal source to J3 pin 5. [Schematic Diagram sheet 5.]
- ❑ Monitor TP20 (U21 pin 7) with the scope.
- ❑ Adjust R88 for a 2.2 Vp-p (±0.1 Vp-p) indication on the scope. Verify the signal is not distorted, not clipping, and riding on a 6.0 Vdc bias.

4. Operator Headset Mic Audio

- ❑ Through a 0.1 µF capacitor, couple a 1 kHz, 200 mV peak-to-peak (±50 mVp-p) audio signal into the operator headset mic audio input at J2 pin 9 (TP2). Connect the ground lead of the signal source to J2 pin 5. Maintain minimum test lead length and use shielded test leads to prevent hum (i.e. 60 Hz) from being induced in the mic input. [Schematic Diagram sheet 5.]
- ❑ Monitor TP18 (U21 pin 8) with the scope.
- ❑ Adjust R59 for a 2.2 Vp-p (±0.1 Vp-p) indication on the scope. Verify the signal is not distorted, not clipping, and riding on a 6.0 Vdc bias.
- ❑ Using a short jumper lead, temporarily connect TP17 and TP18 together. [Schematic Diagram sheets 5 and 6.]
- ❑ Monitor TP34 (U31 pin 7) for a signal level of at least 0.8 mVp-p. Verify the signal is not distorted, not clipping, and riding on a 6.0 Vdc bias.
- ❑ Remove the jumper lead between TP17 and TP18.

NOTE

At board power-up, the digital pots have a mid-point wiper setting. This setting will not change if the Logic Board is not connected to the Audio Matrix Board.

5. Supervisor Headset Mic Audio

- ❑ Through a 0.1 µF capacitor, couple a 1 kHz, 200 mV peak-to-peak (±50 mVp-p) audio signal into the supervisor headset mic audio input at J1 pin 9 (TP1A). Connect the ground lead of the signal source to J1 pin 5. Maintain minimum test lead length and use shielded test leads to prevent hum (i.e. 60 Hz) from being induced in the mic input. [Schematic Diagram sheet 4.]
- ❑ Monitor U21 pin 14 with the scope.
- ❑ Adjust R55 for a 2.2 Vp-p (±0.1 Vp-p) indication on the scope. Verify the signal is not distorted, not clipping, and riding on a 6.0 Vdc bias.

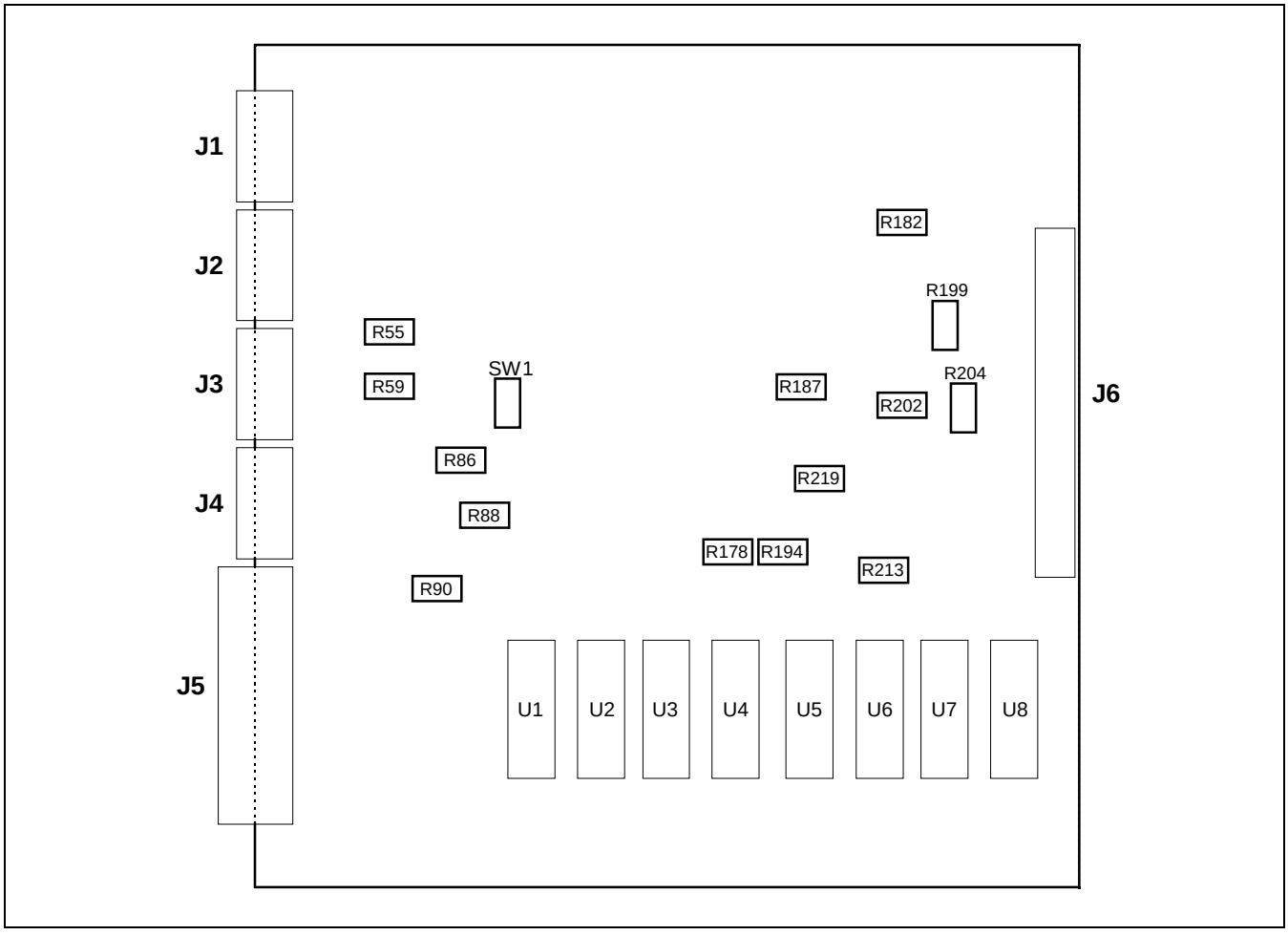

Figure 1 – Audio Matrix Board Potentiometer And SW1 Locations

- ❑ Monitor TP33 (U31 pin 1) for a signal level of at least 0.8 mVp-p. Verify the signal is not distorted, not clipping, and riding on a 6.0 Vdc bias.

6. CD Mic Audio

- ❑ Verify jumper JP1 on the Audio Matrix Board *is not* installed. Also, if testing with the Extender Board, verify a Call Director *is not* connected to the I/O Board.
- ❑ Apply a -25 dBm (124 mVp-p / 44 mVrms) 1 kHz sine wave signal to TP39 and TP40. Connections are not polarity sensitive, since this is a balanced line input. [Schematic Diagram sheet 8.]
- ❑ With the multimeter, measure across TP39 and TP40. Verify the signal across the 600-ohm balanced line input is actually 0.775 Vrms (±20 millivolts). If necessary, slightly readjust the signal generator's output level.
- ❑ Connect the scope probe to TP28 (U34 pin 14).
- ❑ Adjust R182 for a 2.2 Vp-p (±0.1 Vp-p) signal on the scope. Verify the signal is not distorted, not clipping, and riding on a 6.0 Vdc bias.
- ❑ If necessary, reinstall jumper JP1.

7. Pager Audio

- ❑ If testing with the Extender Board, verify a pager *is not* connected to the I/O Board.
- ❑ Through a 0.1 µF capacitor, couple a 2.2 Vp-p 1 kHz sine wave signal to TP42. [Schematic Diagram sheet 8.]
- ❑ Connect the scope probe to TP41 (U34 pin 8).
- ❑ Adjust R199 for a 2.2 Vp-p (±0.1 Vp-p) signal on the scope. Verify the signal is not distorted, not clipping, and riding on a 6.0 Vdc bias.

8. Tone Audio

- ❑ Verify the Logic Board *is not* connected to the Audio Matrix Board.
- ❑ Couple a 5.0 Vp-p 1 kHz sine wave signal to TP16. [Schematic Diagram sheet 2.]
- ❑ Connect the scope probe to TP21 (U30 pin 1).
- ❑ Adjust R124 for a 2.2 Vp-p (±0.1 Vp-p) signal on the scope. Verify the signal is not distorted, not clipping, and riding on a 6.0 Vdc bias.

9. VU Meter Level

- ❑ Verify the Logic Board *is not* connected to the Audio Matrix Board.
- ❑ Through a 0.1 µF capacitor, couple a 2.2 Vp-p 1 kHz sine wave signal to TP47 (U6 pin 6). [Schematic Diagram sheet 11.]
- ❑ Monitor TP29 with the multimeter.
- ❑ Adjust R219 for a 1.25 Vdc.

10. Operator Headset Earphone Audio

- ❑ Through a 0.1 µF capacitor, couple a 2.2 Vp-p 1 kHz sine wave signal to U7 pin 15 and U7 pin 18 (temporarily short pins 15 and 18 together). [Schematic Diagram sheet 12.]
- ❑ Connect a 600-ohm resistor between TP3 (J2 pin 7) and ground. [Schematic Diagram sheet 7.]
- ❑ Connect the scope probe to TP3.
- ❑ Verify the signal on the scope is 250 mVp-p (±50 mVp-p) and no distortion or clipping are present.
- ❑ Remove the 600-ohm load and connect a headset to operator headset jack J2. Listen for a loud undistorted 1 kHz tone.
- ❑ Connect a second headset to the supervisor headset jack J1. Listen for a strong sidetone in the headset's earphones. Adjustment of sidetone pots R194 and R213 is not recommended.

11. Supervisor Headset Earphone Audio

- ❑ Through a 0.1 µF capacitor, couple a 2.2 Vp-p 1 kHz sine wave signal to U8 pin 11 and U8 pin 16 (temporarily short pins 11 and 16 together). [Schematic Diagram sheet 12.]
- ❑ Connect a 600-ohm resistor between TP1 (J1 pin 7) and ground. [Schematic Diagram sheet 7.]
- ❑ Connect the scope probe to TP1.
- ❑ Verify the signal on the scope is 250 mVp-p (±50 mVp-p). Verify no distortion or clipping are present.
- ❑ Remove the 600-ohm load and connect a headset to supervisor headset jack J1. Listen for a loud undistorted 1 kHz tone.
- ❑ Connect a second headset to the operator headset jack J2. Listen for a strong sidetone in the headset's earphones. Adjustment of sidetone pots R90 and R178 is not recommended.

12. Completion

- ❑ If necessary, return SW1 to its previous settings recorded in the "**Set-Up Procedure**" section.
- ❑ Reinstall the board in the Audio Tower and test for proper operation.

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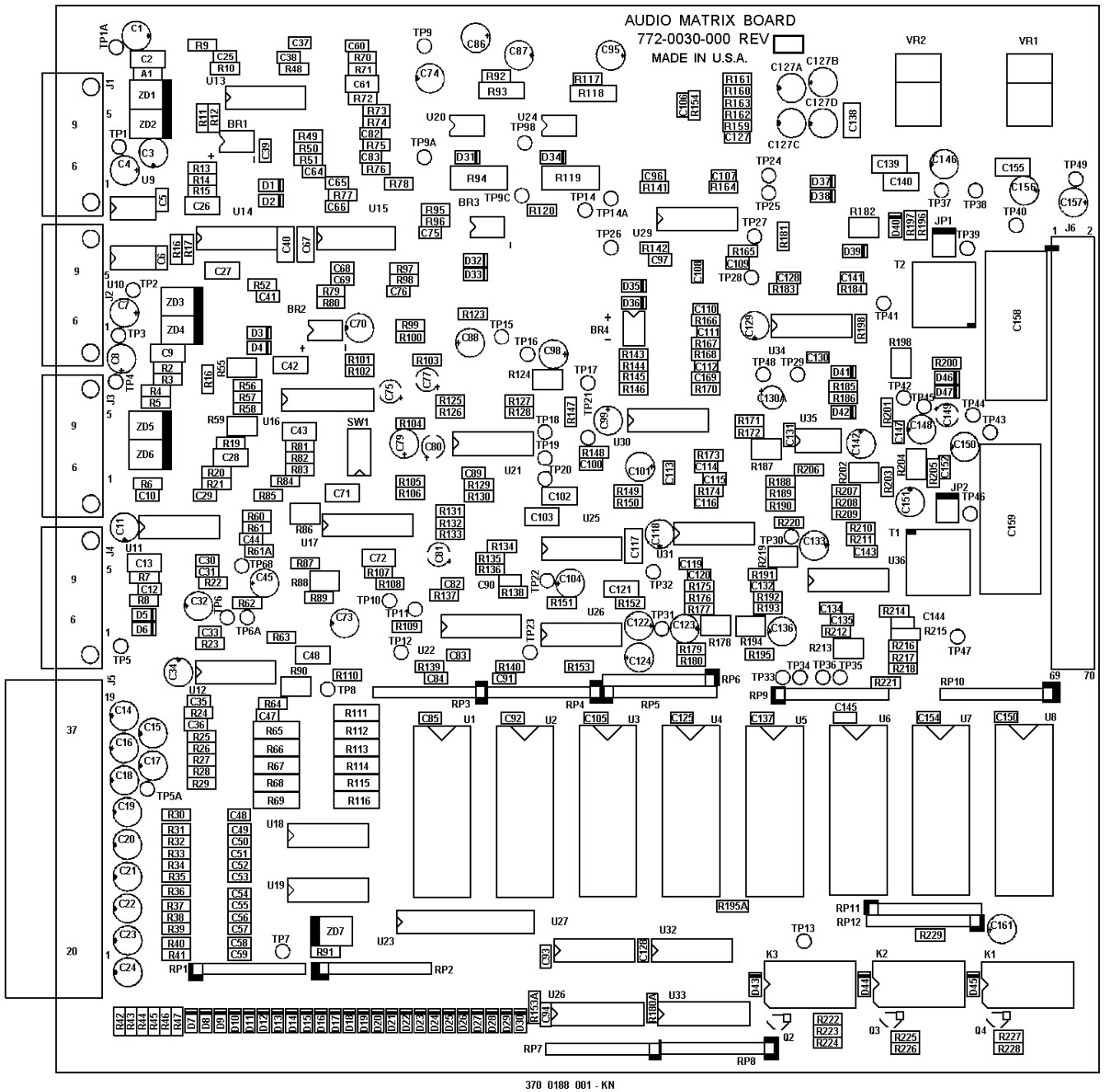

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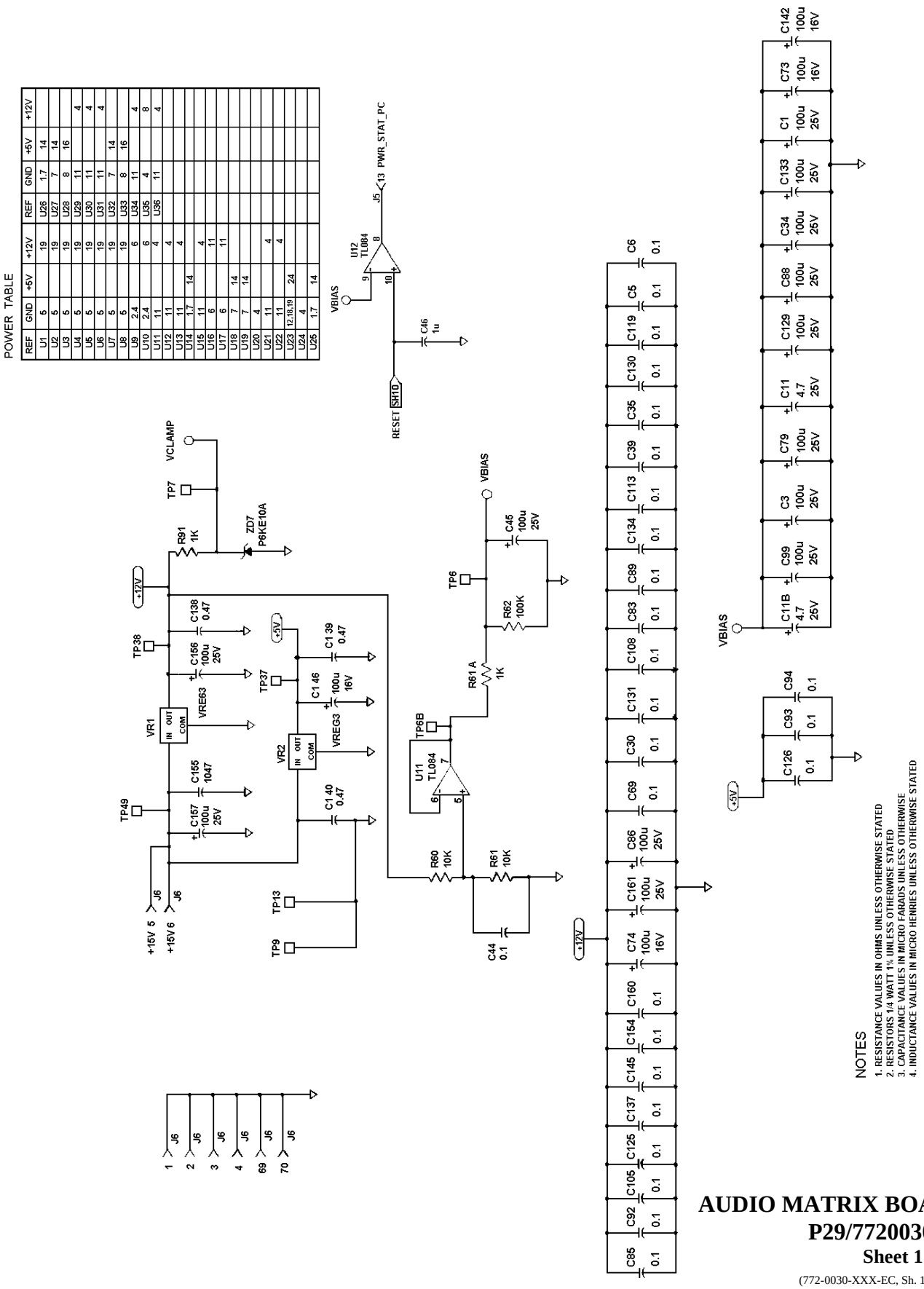
CAUTION

OBSERVE PRECAUTIONS FOR HANDLING

ELECTROSTATIC SENSITIVE DEVICES



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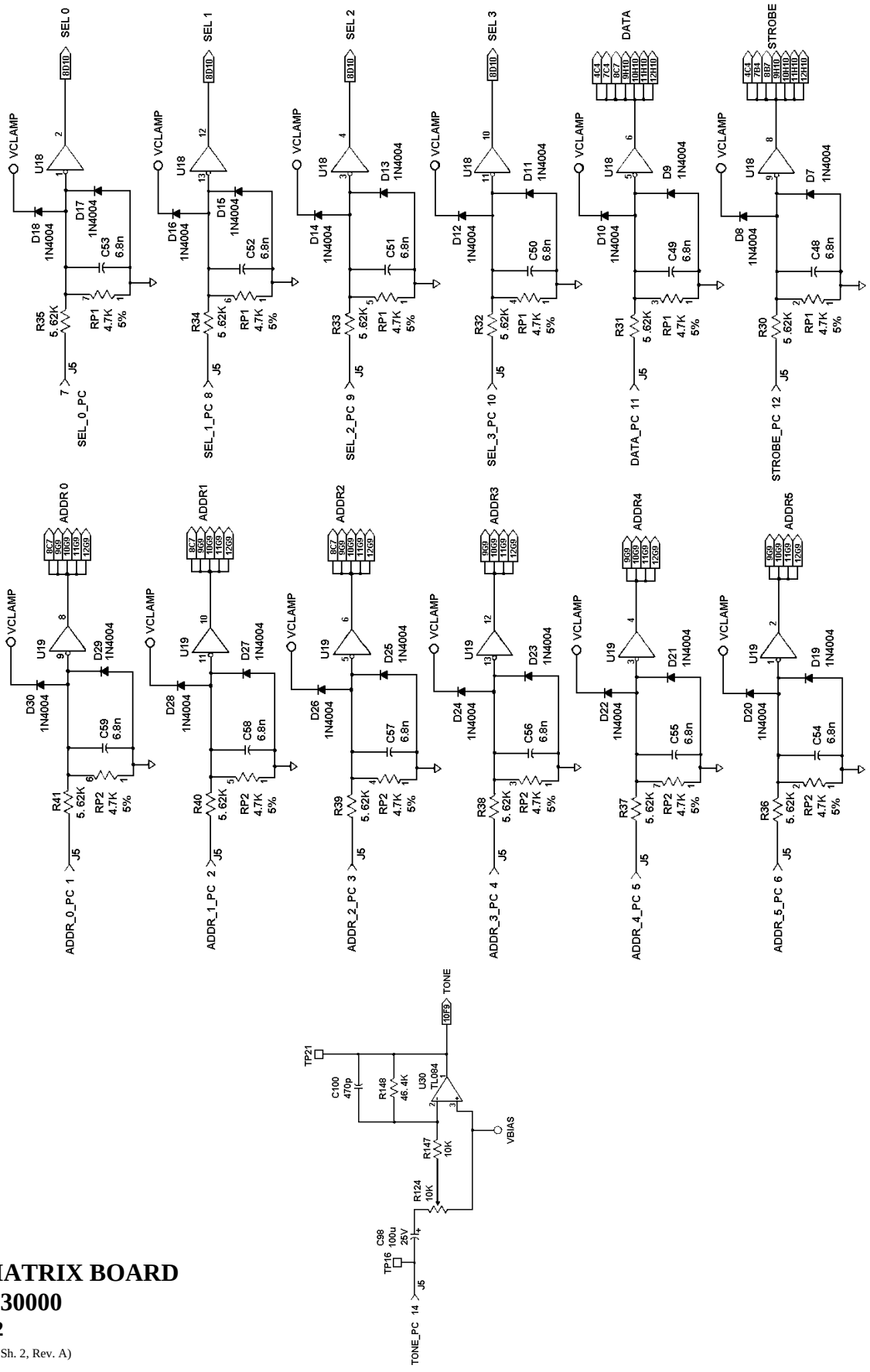

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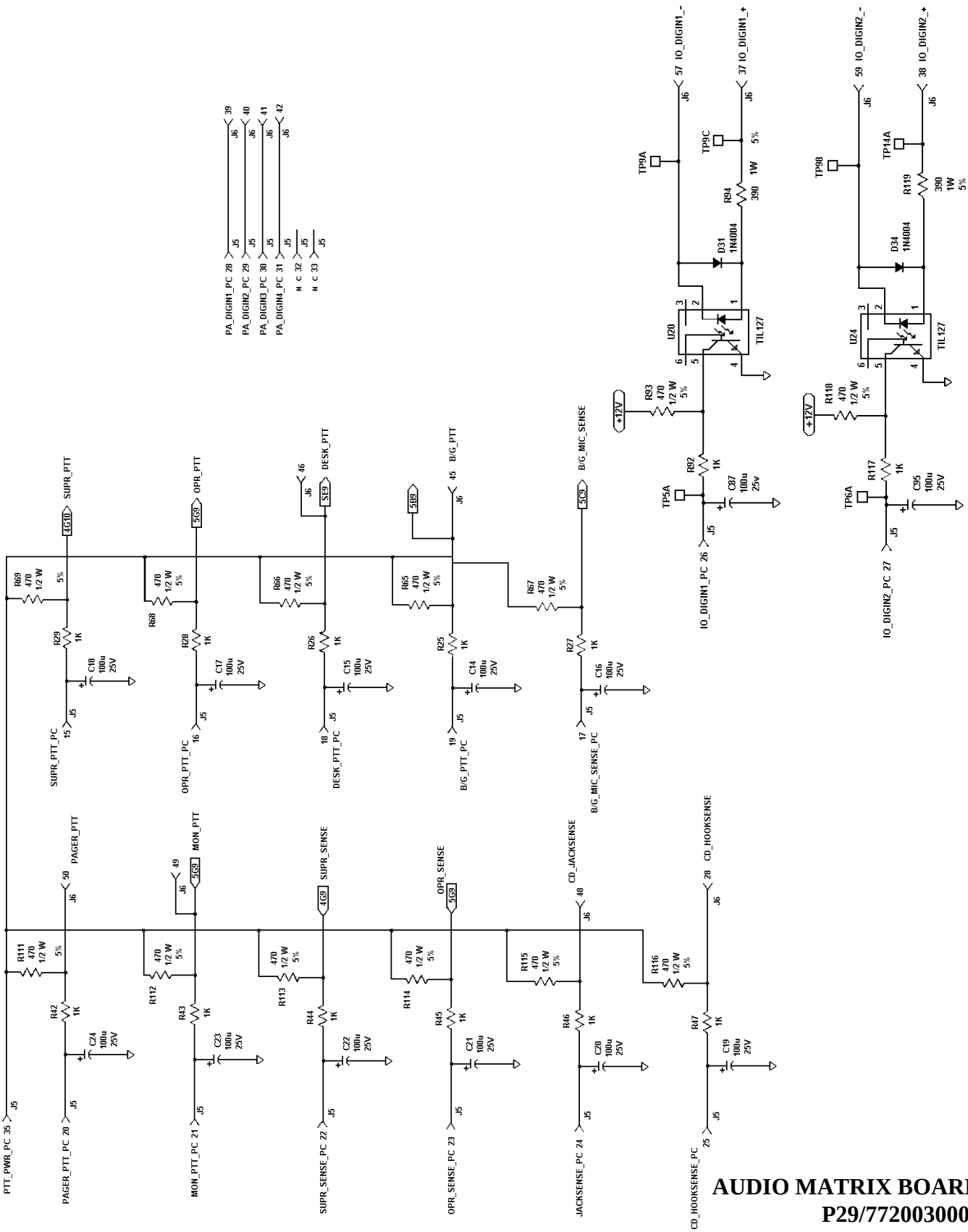

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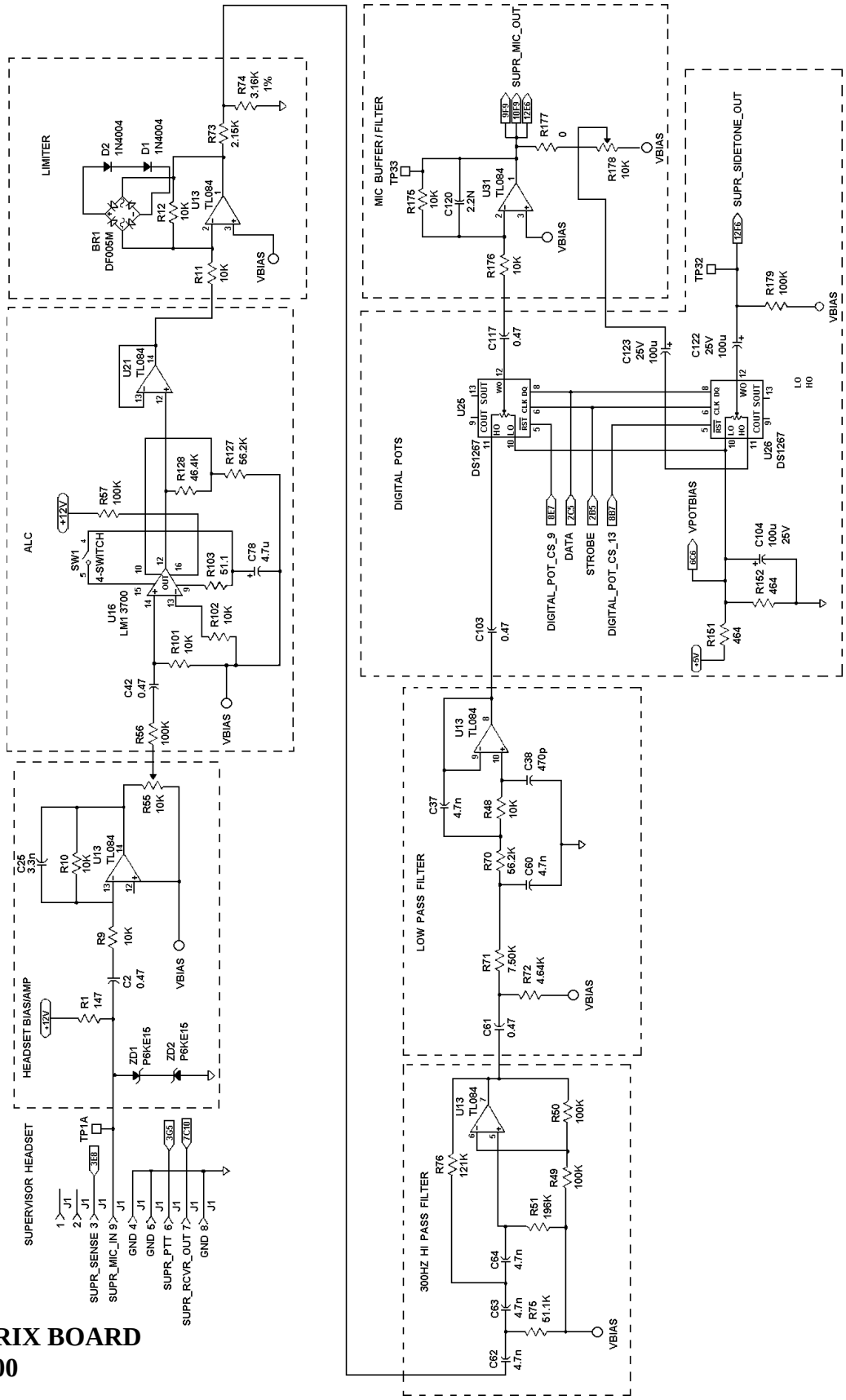

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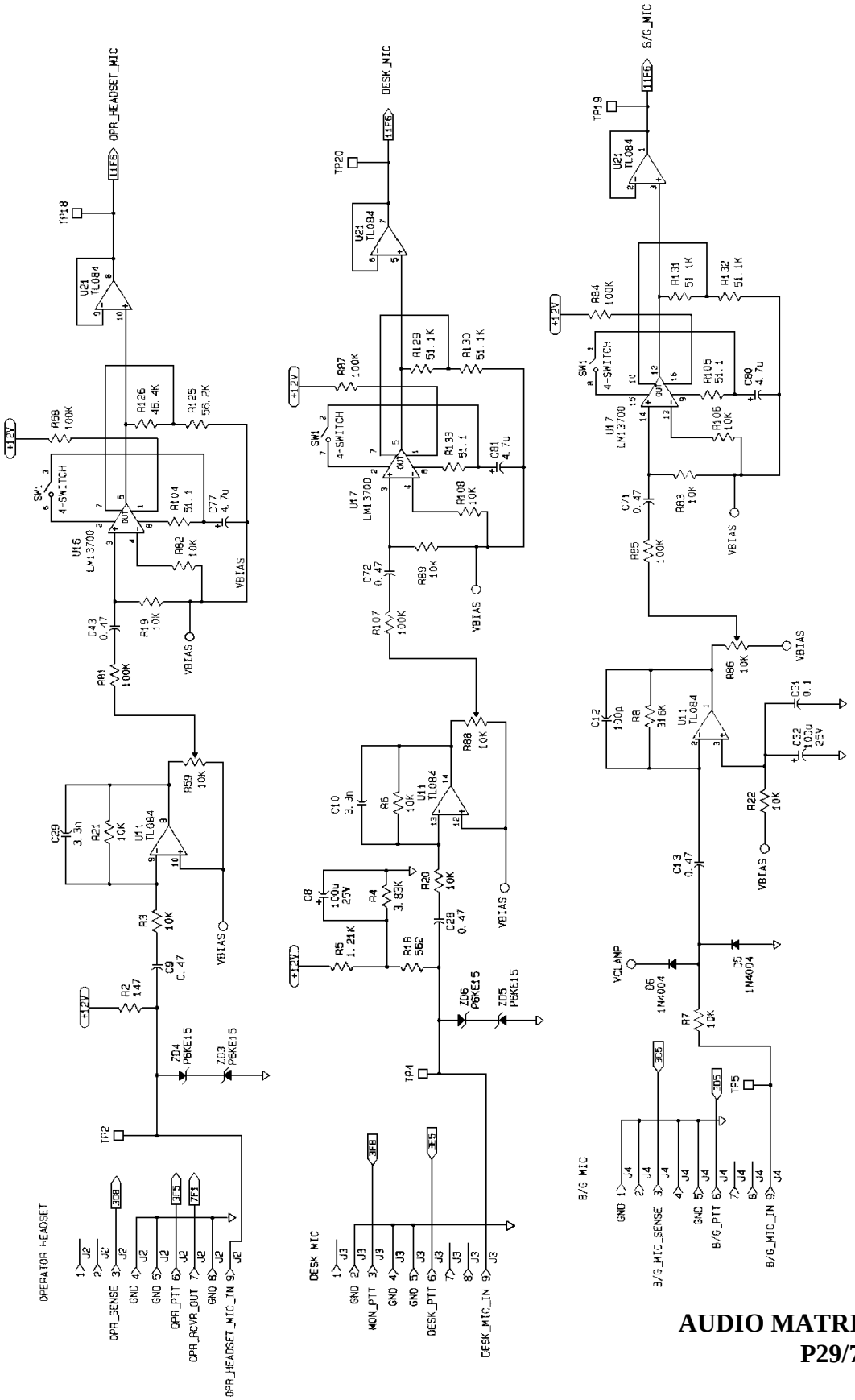

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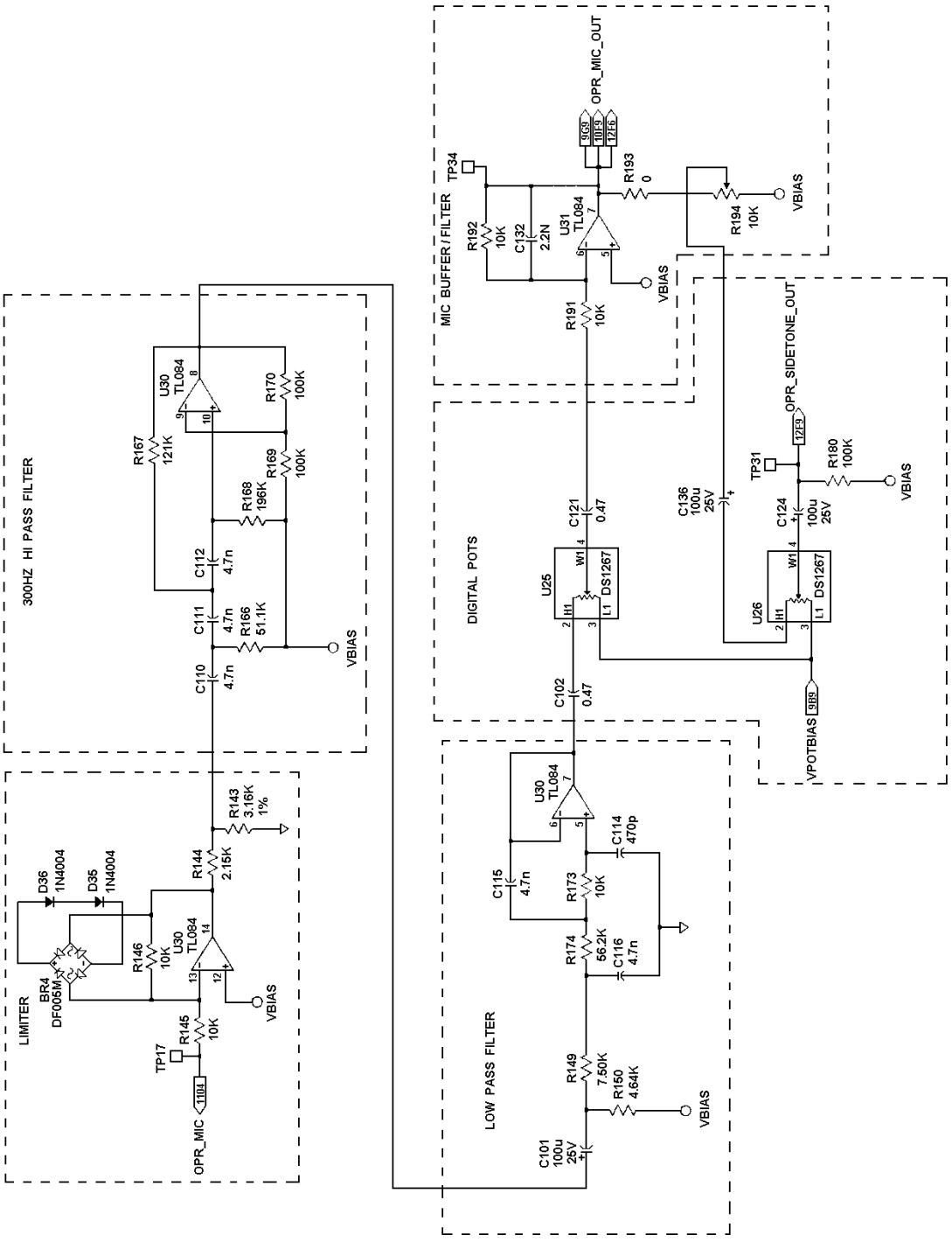

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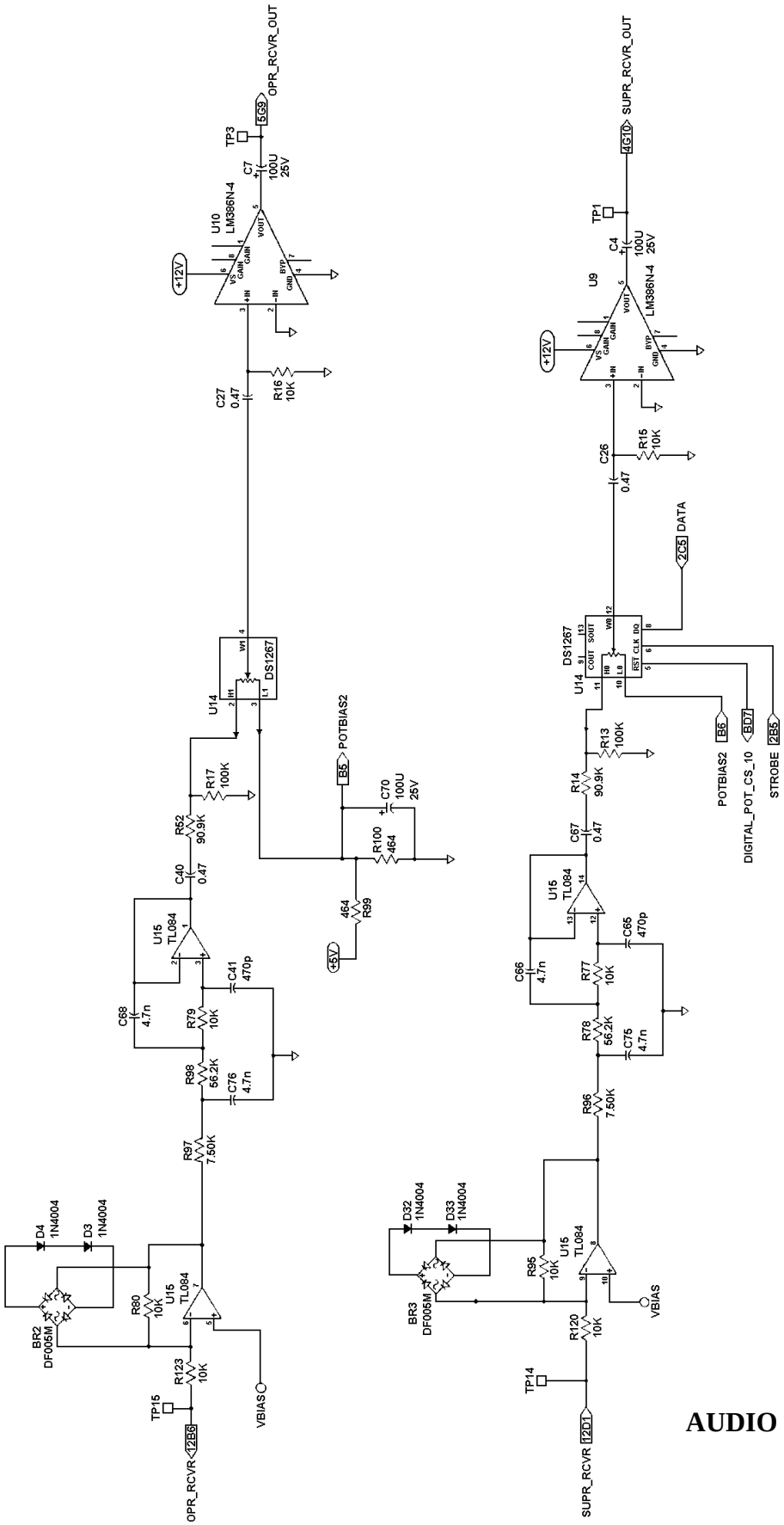

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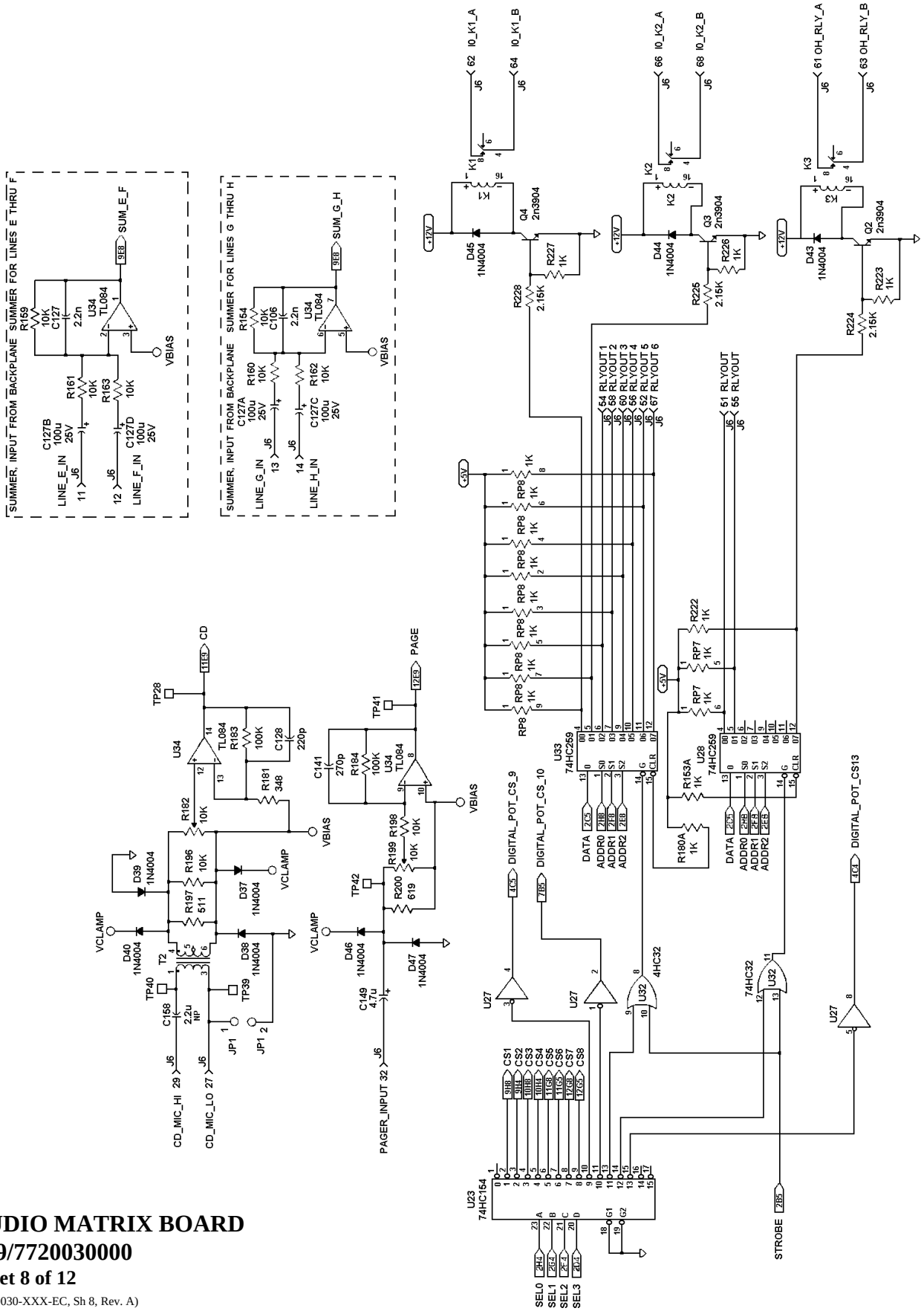

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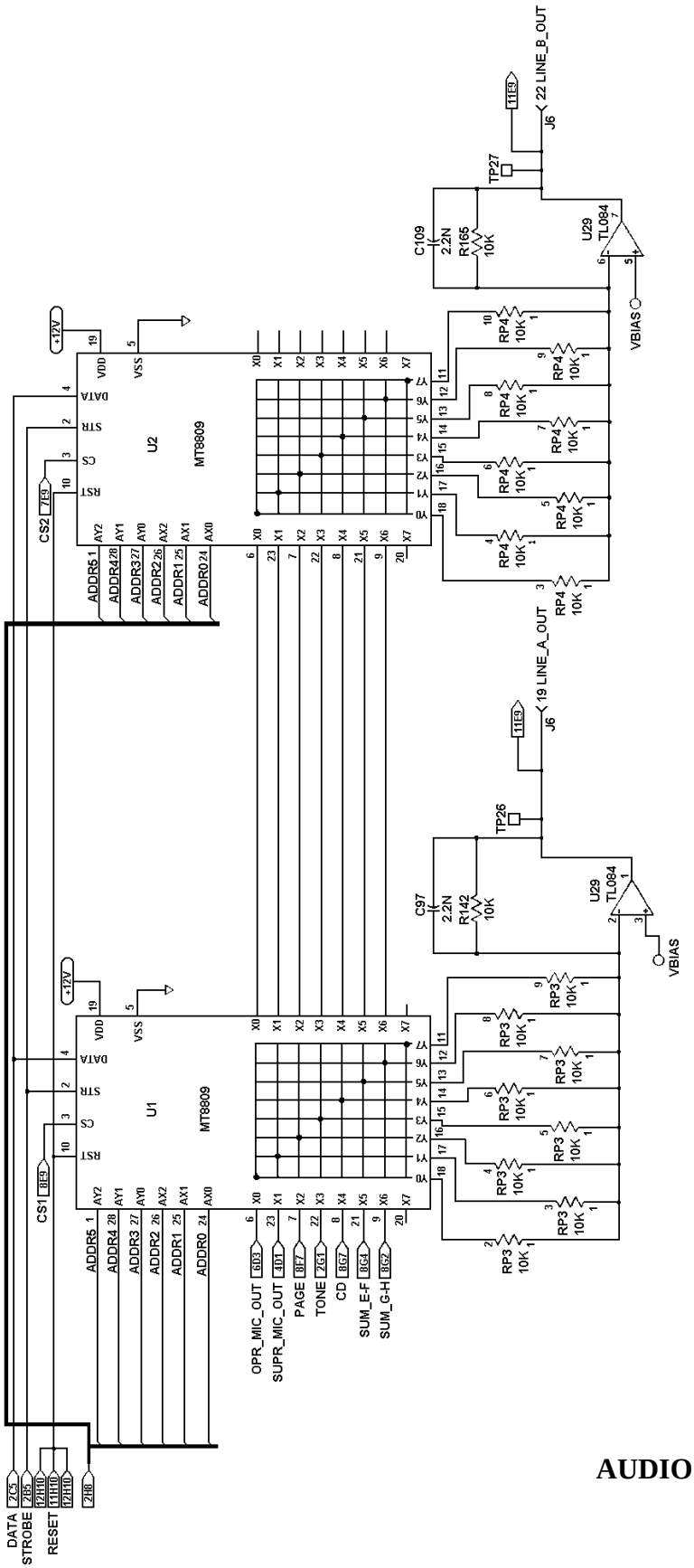

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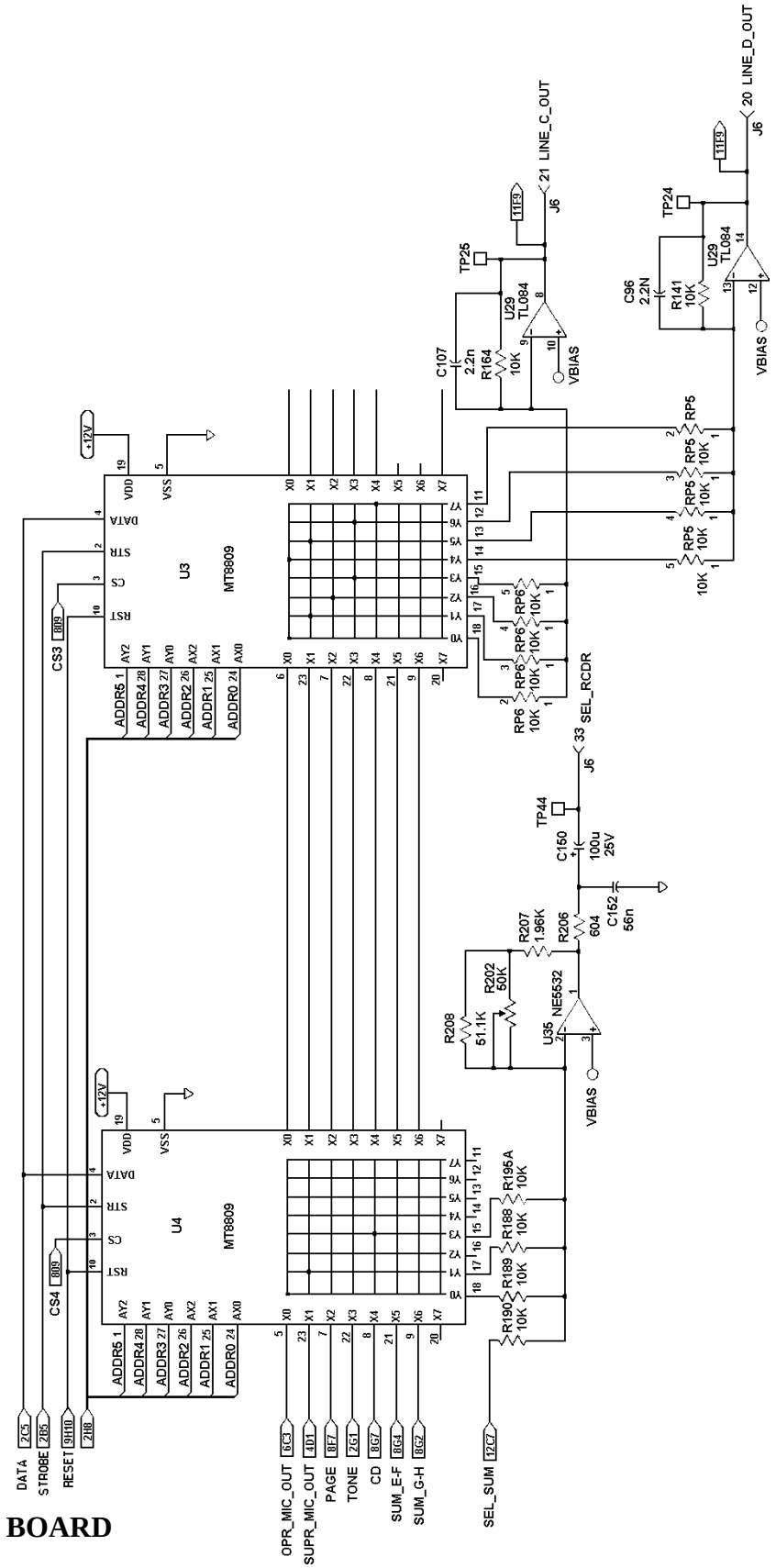

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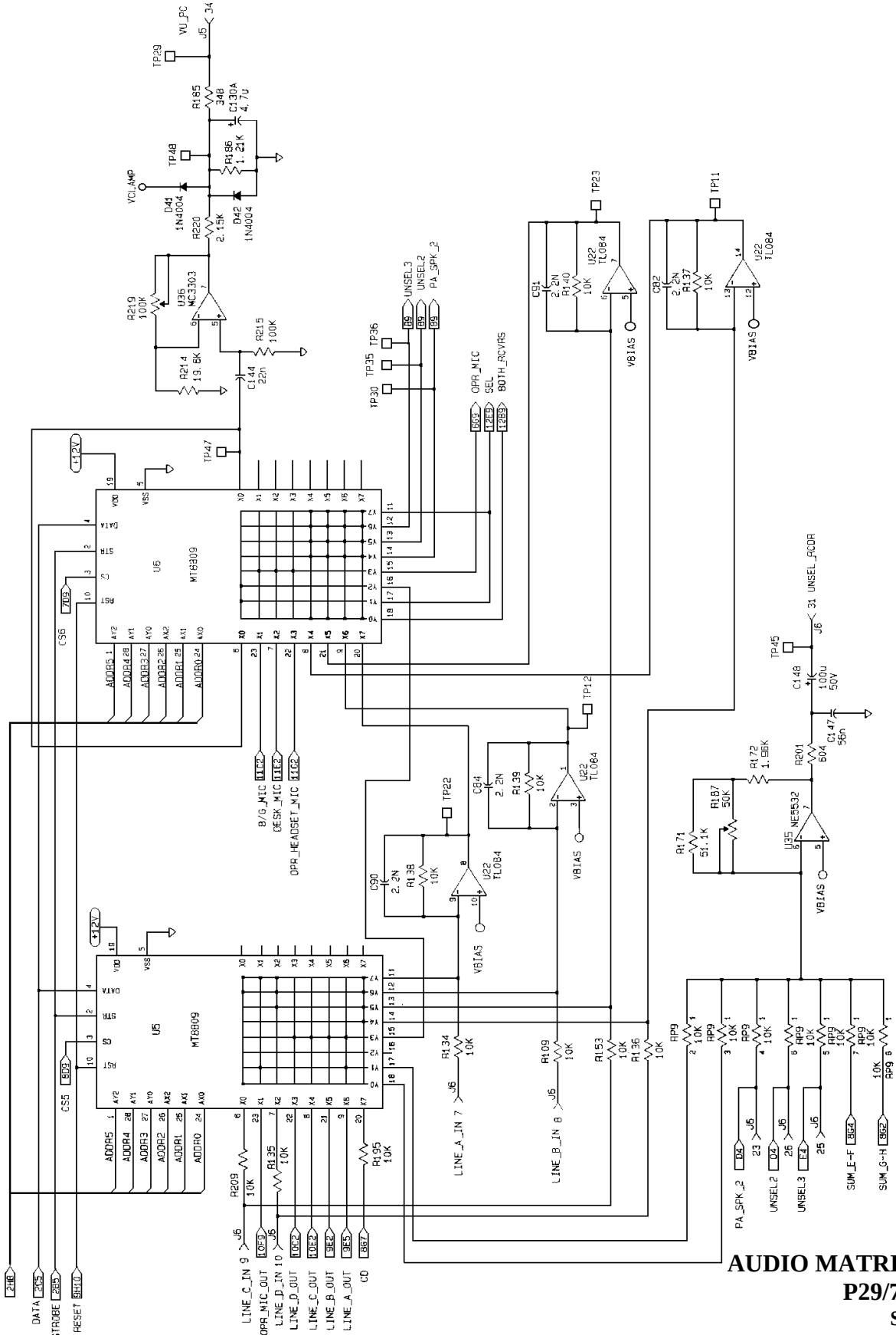

AUDIO MATRIX BOARD
P29/7720030000
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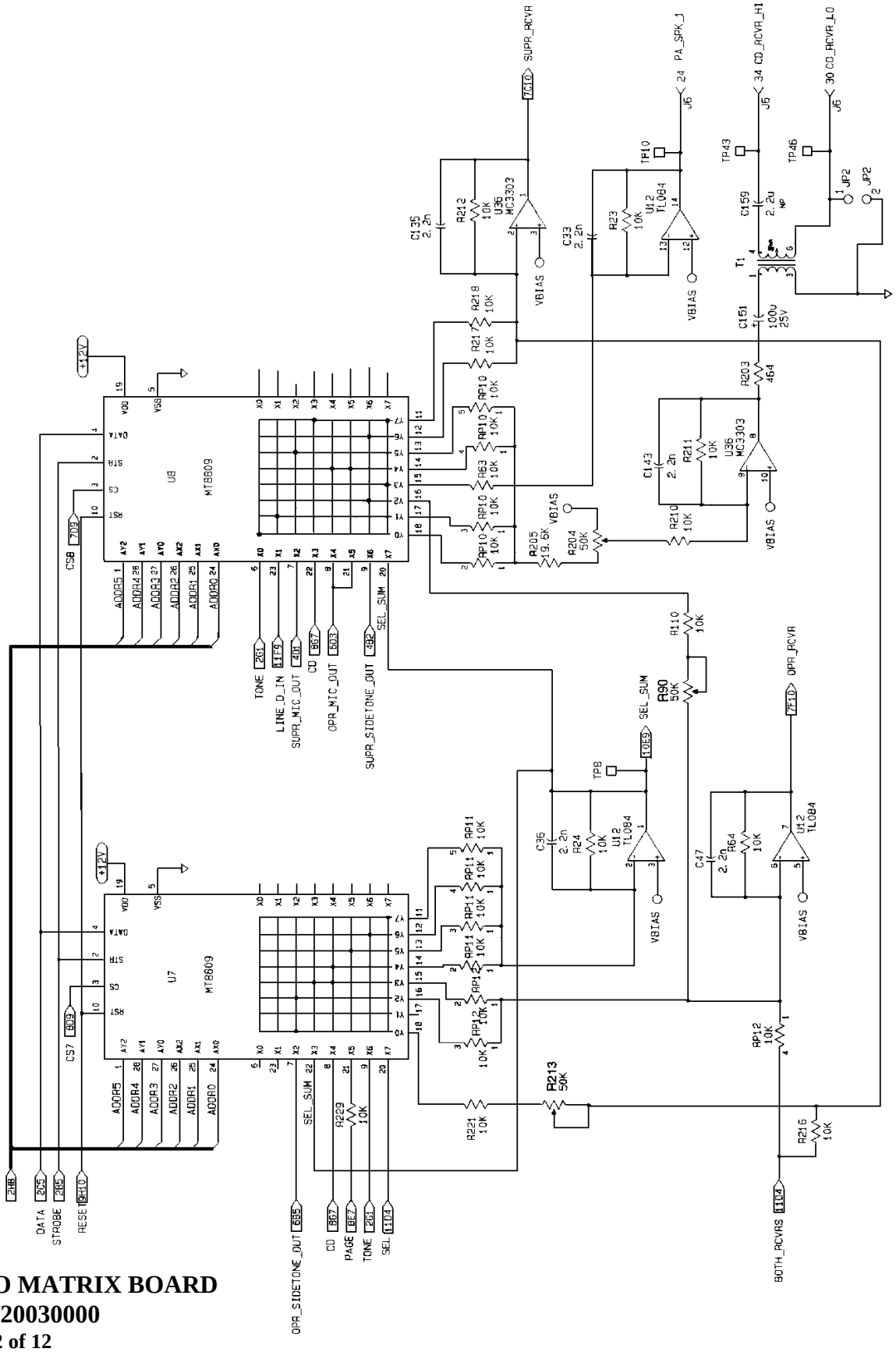

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P29/7720030000
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AUDIO MATRIX BOARD
P29/7720030000 Rev. A

ISSUE 1

SYMBOL	PART NUMBER	DESCRIPTION
		----------BRIDGE RECTIFIERS ----------
BR1 thru BR4	P29/2080001000	Silicon: 1-Amp. 50-Volts; General Instrument DF005M.
		---------- CAPACITORS ----------
C1	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C2	P29/3160186017	0.47 µF ±20%, 50 V; Kemet C430C474M5U5CA.
C3 and C4	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C5 and C6	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C7 and C8	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C9	P29/3160186017	0.47 µF ±20%, 50 V; Kemet C430C474M5U5CA.
C10	P29/3160186029	3.3 nF ±5%, 100 V; Kemet C410C332J1R5CA.
C11	P29/3170133000	4.7 µF ±20%, 35 V; Panasonic ECE-A1VU4R7.
C12	P29/3160186024	100 pF ±10%, 100 V; Kemet C410C101K1G5CA.
C13	P29/3160186017	0.47 µF ±20%, 50 V; Kemet C430C474M5U5CA.
C14 thru C24	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C25	P29/3160186029	3.3 nF ±5%, 100 V; Kemet C410C332J1R5CA.
C26 thru C28	P29/3160186017	0.47 µF ±20%, 50 V; Kemet C430C474M5U5CA.
C29	P29/3160186029	3.3 nF ±5%, 100 V; Kemet C410C332J1R5CA.
C30 and C31	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C32	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C33	P29/3160186030	2.2 nF ±10%, 100 V; Kemet C410C222K1R5CA.
C34	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C35	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C36	P29/3160186030	2.2 nF ±10%, 100 V; Kemet C410C222K1R5CA.
C37	P29/3160186028	4.7 nF ±5%, 100 V; Kemet C410C472J1R5CA.
C38	P29/3160186032	470 pF ±10%, 100 V; Kemet C410C471K2R5CA.
C39	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C40	P29/3160186017	0.47 µF ±20%, 50 V; Kemet C430C474M5U5CA.
C41	P29/3160186032	470 pF ±10%, 100 V; Kemet C410C471K2R5CA.
C42 and C43	P29/3160186017	0.47 µF ±20%, 50 V; Kemet C430C474M5U5CA.
C44	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C45	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C46	P29/3160128000	1 µF ±20%, 50 V; Kemet C440C105M5U5CA.
C47	P29/3160186030	2.2 nF ±10%, 100 V; Kemet C410C222K1R5CA.
C48 thru C59	P29/3160186033	6.8 nF ±10%, 100 V; Kemet C410C682K1R5CA.
C60	P29/3160186028	4.7 nF ±5%, 100 V; Kemet C410C472J1R5CA.
C61	P29/3160186017	0.47 µF ±20%, 50 V; Kemet C430C474M5U5CA.
C62 thru C64	P29/3160186028	4.7 nF ±5%, 100 V; Kemet C410C472J1R5CA.
C65	P29/3160186032	470 pF ±10%, 100 V; Kemet C410C471K2R5CA.
C66	P29/3160186028	4.7 nF ±5%, 100 V; Kemet C410C472J1R5CA.
C67	P29/3160186017	0.47 µF ±20%, 50 V; Kemet C430C474M5U5CA.
C68	P29/3160186028	4.7 nF ±5%, 100 V; Kemet C410C472J1R5CA.
C69	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C70	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C71 and C72	P29/3160186017	0.47 µF ±20%, 50 V; Kemet C430C474M5U5CA.
C73 and C74	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C75 and C76	P29/3160186028	4.7 nF ±5%, 100 V; Kemet C410C472J1R5CA.
C77 and C78	P29/3170133000	4.7 µF ±20%, 35 V; Panasonic ECE-A1VU4R7.
C79	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C80 and C81	P29/3170133000	4.7 µF ±20%, 35 V; Panasonic ECE-A1VU4R7.
C82	P29/3160186030	2.2 nF ±10%, 100 V; Kemet C410C222K1R5CA.
C83	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C84	P29/3160186030	2.2 nF ±10%, 100 V; Kemet C410C222K1R5CA.
C85	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C86 thru C88	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C89	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C90 and C91	P29/3160186030	2.2 nF ±10%, 100 V; Kemet C410C222K1R5CA.
C92 thru C94	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C95	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C96 and C97	P29/3160186030	2.2 nF ±10%, 100 V; Kemet C410C222K1R5CA.
C98 and C99	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C100	P29/3160186032	470 pF ±10%, 100 V; Kemet C410C471K2R5CA.
C101	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C102 and C103	P29/3160186017	0.47 µF ±20%, 50 V; Kemet C430C474M5U5CA.
C104	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C105	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C106 and C107	P29/3160186030	2.2 nF ±10%, 100 V; Kemet C410C222K1R5CA.
C108	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.

SYMBOL	PART NUMBER	DESCRIPTION
C109	P29/3160186030	2.2 nF ±10%, 100 V; Kemet C410C222K1R5CA.
C110 thru C112	P29/3160186028	4.7 nF ±5%, 100 V; Kemet C410C472J1R5CA.
C113	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C114	P29/3160186032	470 pF ±10%, 100 V; Kemet C410C471K2R5CA.
C115 and C116	P29/3160186028	4.7 nF ±5%, 100 V; Kemet C410C472J1R5CA.
C117	P29/3160186017	0.47 µF ±20%, 50 V; Kemet C430C474M5U5CA.
C118	P29/3170133000	4.7 µF ±20%, 35 V; Panasonic ECE-A1VU4R7.
C119	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C120	P29/3160186030	2.2 nF ±10%, 100 V; Kemet C410C222K1R5CA.
C121	P29/3160186017	0.47 µF ±20%, 50 V; Kemet C430C474M5U5CA.
C122 thru C124	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C125 and C126	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C127	P29/3160186030	2.2 nF ±10%, 100 V; Kemet C410C222K1R5CA.
C127A thru C127D	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C128	P29/3160186034	220 pF ±10%, 100 V; Kemet C410C221K1G5CA.
C129	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C130	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C130A	P29/3170133000	4.7 µF ±20%, 35 V; Panasonic ECE-A1VU4R7.
C131	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C132	P29/3160186030	2.2 nF ±10%, 100 V; Kemet C410C222K1R5CA.
C133	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C134	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C135	P29/3160186030	2.2 nF ±10%, 100 V; Kemet C410C222K1R5CA.
C136	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C137	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C138 thru C140	P29/3160186017	0.47 µF ±20%, 50 V; Kemet C430C474M5U5CA.
C141	P29/3160186036	270 pF ±10%, 100 V; Kemet C410C271K1G5CA.
C142	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C143	P29/3160186030	2.2 nF ±10%, 100 V; Kemet C410C222K1R5CA.
C144	P29/3160186035	22 nF ±10%, 100 V; Kemet C410C220K1G5CA.
C145	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C146	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C147	P29/3160186031	56 nF ±10%, 100 V; Kemet C410C560K1G5CA.
C148	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C149	P29/3170133000	4.7 µF ±20%, 35 V; Panasonic ECE-A1VU4R7.
C150 and C151	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C152	P29/3160186031	56 nF ±10%, 100 V; Kemet C410C560K1G5CA.
C154	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C155	P29/3160186017	0.47 µF ±20%, 50 V; Kemet C430C474M5U5CA.
C156 and C157	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
C158 thru C159	P29/3180055000	2.2 µF ±10%, 250 V; Mallory 150225K250PF.
C160	P29/3160186011	0.1 µF ±20%, 50 V; Kemet C410C104M5U5CA.
C161	P29/3170187005	100 µF ±20%, 25 V; Sprague 515D107M025AA64.
		----------DIODES----------
D1 thru D47	P29/3420027000	Silicon: 1N4004.
		----------JACKS----------
J1 thru J4	P29/3800548000	Connector: 9-pin right-angle mounting D-sub.; AMP 745781-5.
J5	P29/3800549000	Connector: 37-pin right-angle mounting D-sud.; AMP 745784-6.
J6	P29/3800418000	Connector: 70-position, right-angle mounting; AMP 532955-0.
		----------HEADERS ----------
JP1 and JP2	P29/3760012000	Tin-plated: 2-position; AMP 828214-2.
		----------RELAYS----------
K1 thru K3	P29/3230046005	DPDT (2 Form C) contacts, 12 V coil: Aromat DS2E-M-DC12V
		---------- TRANSISTORS ----------
Q2 thru Q4	P29/3440053000	Silicon, NPN: 2N3904.
		---------- RESISTORS ----------
R1 and R2	P29/3051470611	147 ohms ±1%, 1/4 W.
R3	P29/3051002611	10K ohms ±1%, 1/4 W.
R4	P29/3053831611	3.83K ohms ±1%, 1/4 W.
R5	P29/3051211611	1.21K ohms ±1%, 1/4 W.
R6 and R7	P29/3051002611	10K ohms ±1%, 1/4 W.
R8	P29/3053163611	316K ohms ±1%, 1/4 W.
R9 thru R12	P29/3051002611	10K ohms ±1%, 1/4 W.
R13	P29/3051003611	100K ohms ±1%, 1/4 W.
R14	P29/3059092611	90.9K ohms ±1%, 1/4 W.
R15 and R16	P29/3051002611	10K ohms ±1%, 1/4 W.
R17	P29/3051003611	100K ohms ±1%, 1/4 W.
R18	P29/3055620611	562 ohms ±1%, 1/4 W.
R19 thru R24	P29/3051002611	10K ohms ±1%, 1/4 W.
R25 thru R29	P29/3051001611	1K ohms ±1%, 1/4 W.

SYMBOL	PART NUMBER	DESCRIPTION
R30 thru R41	P29/3055621611	5.62K ohms ±1%, 1/4 W.
R42 thru R47	P29/3051001611	1K ohms ±1%, 1/4 W.
R48	P29/3051002611	10K ohms ±1%, 1/4 W.
R49 and R50	P29/3051003611	100K ohms ±1%, 1/4 W.
R51	P29/3051963611	196K ohms ±1%, 1/4 W.
R52	P29/3059092611	90.9K ohms ±1%, 1/4 W.
R55	P29/3100092103	Potentiometer: 10K ohms, 12-turn; Bourns 3266W-1-103
R56 thru R58	P29/3051003611	100K ohms ±1%, 1/4 W.
R59	P29/3100092103	Potentiometer: 10K ohms, 12-turn; Bourns 3266W-1-103
R60 and R61	P29/3051002611	10K ohms ±1%, 1/4 W.
R61A	P29/3051001611	1K ohms ±1%, 1/4 W.
R62	P29/3051003611	100K ohms ±1%, 1/4 W.
R63 and R64	P29/3051002611	10K ohms ±1%, 1/4 W.
R65 thru R69	P29/3070470050	Metal oxide: 470 ohms ±5%, 1/2 W.
R70	P29/3055622611	56.2K ohms ±1%, 1/4 W.
R71	P29/3057501611	7.5K ohms ±1%, 1/4 W.
R72	P29/3054641611	4.64K ohms ±1%, 1/4 W.
R73	P29/3052151611	2.15K ohms ±1%, 1/4 W.
R74	P29/3053161611	3.16K ohms ±1%, 1/4 W.
R75	P29/3055112611	51.1K ohms ±1%, 1/4 W.
R76	P29/3051213611	121K ohms ±1%, 1/4 W.
R77	P29/3051002611	10K ohms ±1%, 1/4 W.
R78	P29/3055622611	56.2K ohms ±1%, 1/4 W.
R79 and R80	P29/3051002611	10K ohms ±1%, 1/4 W.
R81	P29/3051003611	100K ohms ±1%, 1/4 W.
R82 and R83	P29/3051002611	10K ohms ±1%, 1/4 W.
R84 and R85	P29/3051003611	100K ohms ±1%, 1/4 W.
R86	P29/3100092103	Potentiometer: 10K ohms, 12-turn; Bourns 3266W-1-103
R87	P29/3051003611	100K ohms ±1%, 1/4 W.
R88	P29/3100092103	Potentiometer: 10K ohms, 12-turn; Bourns 3266W-1-103
R89	P29/3051002611	10K ohms ±1%, 1/4 W.
R90	P29/3100092503	Potentiometer: 50K ohms, 12-turn; Bourns 3266W-1-503
R91 and R92	P29/3051001611	1K ohms ±1%, 1/4 W.

SYMBOL	PART NUMBER	DESCRIPTION
R93	P29/3070470050	Metal oxide: 470 ohms ±5%, 1/2 W.
R94	P29/3070390150	Metal oxide: 390 ohms ±5%, 1 W.
R95	P29/3051002611	10K ohms ±1%, 1/4 W.
R96 and R97	P29/3057501611	7.5K ohms ±1%, 1/4 W.
R98	P29/3055622611	56.2K ohms ±1%, 1/4 W.
R99 and R100	P29/3054640611	464 ohms ±1%, 1/4 W.
R101 and R102	P29/3051002611	10K ohms ±1%, 1/4 W.
R103 thru R105	P29/3055112611	51.1K ohms ±1%, 1/4 W.
R106	P29/3051002611	10K ohms ±1%, 1/4 W.
R107	P29/3051003611	100K ohms ±1%, 1/4 W.
R108 thru R110	P29/3051002611	10K ohms ±1%, 1/4 W.
R111 thru R116	P29/3070470050	Metal oxide: 470 ohms ±5%, 1/2 W.
R117	P29/3051001611	1K ohms ±1%, 1/4 W.
R118	P29/3070470050	Metal oxide: 470 ohms ±5%, 1/2 W.
R119	P29/3070390150	Metal oxide: 390 ohms ±5%, 1 W.
R120	P29/3051002611	10K ohms ±1%, 1/4 W.
R123	P29/3051002611	10K ohms ±1%, 1/4 W.
R124	P29/3100092103	Potentiometer: 10K ohms, 12-turn; Bourns 3266W-1-103
R125	P29/3055622611	56.2K ohms ±1%, 1/4 W.
R126	P29/3054642611	46.4K ohms ±1%, 1/4 W.
R127	P29/3055622611	56.2K ohms ±1%, 1/4 W.
R128	P29/3054642611	46.4K ohms ±1%, 1/4 W.
R129 thru R132	P29/3055112611	51.1K ohms ±1%, 1/4 W.
R133	P29/3055112611	51.1K ohms ±1%, 1/4 W.
R134 thru R142	P29/3051002611	10K ohms ±1%, 1/4 W.
R143	P29/3053161611	3.16K ohms ±1%, 1/4 W.
R144	P29/3052151611	2.15K ohms ±1%, 1/4 W.
R145 thru R147	P29/3051002611	10K ohms ±1%, 1/4 W.
R148	P29/3054642611	46.4K ohms ±1%, 1/4 W.
R149	P29/3057501611	7.5K ohms ±1%, 1/4 W.
R150	P29/3054641611	4.64K ohms ±1%, 1/4 W.
R151 and R152	P29/3054640611	464 ohms ±1%, 1/4 W.
R153	P29/3051002611	10K ohms ±1%, 1/4 W.
R153A	P29/3051001611	1K ohms ±1%, 1/4 W.
R154	P29/3051002611	10K ohms ±1%, 1/4 W.

SYMBOL	PART NUMBER	DESCRIPTION
R159 thru R165	P29/3051002611	10K ohms ±1%, 1/4 W.
R166	P29/3055112611	51.1K ohms ±1%, 1/4 W.
R167	P29/3051213611	121K ohms ±1%, 1/4 W.
R168	P29/3051963611	196K ohms ±1%, 1/4 W.
R169 and R170	P29/3051003611	100K ohms ±1%, 1/4 W.
R171	P29/3055112611	51.1K ohms ±1%, 1/4 W.
R172	P29/3051961611	1.96K ohms ±1%, 1/4 W.
R173	P29/3051002611	10K ohms ±1%, 1/4 W.
R174	P29/3055622611	56.2K ohms ±1%, 1/4 W.
R175 and R176	P29/3051002611	10K ohms ±1%, 1/4 W.
R177	P29/3050000611	0 ohms (jumper).
R178	P29/3100092103	Potentiometer: 10K ohms, 12-turn; Bourns 3266W-1-103
R179 and R180	P29/3051003611	100K ohms ±1%, 1/4 W.
R180A	P29/3051001611	1K ohms ±1%, 1/4 W.
R181	P29/3053480611	348 ohms ±1%, 1/4 W.
R182	P29/3100092103	Potentiometer: 10K ohms, 12-turn; Bourns 3266W-1-103
R183 and R184	P29/3051003611	100K ohms ±1%, 1/4 W.
R185	P29/3053480611	348 ohms ±1%, 1/4 W.
R186	P29/3051211611	1.21K ohms ±1%, 1/4 W.
R187	P29/3100092503	Potentiometer: 50K ohms, 12-turn; Bourns 3266W-1-503
R188 thru R192	P29/3051002611	10K ohms ±1%, 1/4 W.
R193	P29/3050000611	0 ohms (jumper).
R194	P29/3100092103	Potentiometer: 10K ohms, 12-turn; Bourns 3266W-1-103
R195 thru R196	P29/3051002611	10K ohms ±1%, 1/4 W.
R197	P29/3055110611	511 ohms ±1%, 1/4 W.
R198	P29/3051002611	10K ohms ±1%, 1/4 W.
R199	P29/3100092103	Potentiometer: 10K ohms, 12-turn; Bourns 3266W-1-103
R200	P29/3056190611	619 ohms ±1%, 1/4 W.
R201	P29/3056040611	604 ohms ±1%, 1/4 W.
R202	P29/3100092503	Potentiometer: 50K ohms, 12-turn; Bourns 3266W-1-503
R203	P29/3054640611	464 ohms ±1%, 1/4 W.
R204	P29/3100092503	Potentiometer: 50K ohms, 12-turn; Bourns 3266W-1-503
R205	P29/3051962611	19.6K ohms ±1%, 1/4 W.
R206	P29/3056040611	604 ohms ±1%, 1/4 W.
R207	P29/3051961611	1.96K ohms ±1%, 1/4 W.
R208	P29/3055112611	51.1K ohms ±1%, 1/4 W.

SYMBOL	PART NUMBER	DESCRIPTION
R209 thru R212	P29/3051002611	10K ohms ±1%, 1/4 W.
R213	P29/3100092503	Potentiometer: 50K ohms, 12-turn; Bourns 3266W-1-503
R214	P29/3051962611	19.6K ohms ±1%, 1/4 W.
R215	P29/3051003611	100K ohms ±1%, 1/4 W.
R216 thru R218	P29/3051002611	10K ohms ±1%, 1/4 W.
R219	P29/3100074104	Potentiometer: 100K ohms, 12-turn; Bourns 3266W-1-104
R220	P29/3052151611	2.15K ohms ±1%, 1/4 W.
R222 and R223	P29/3051001611	1K ohms ±1%, 1/4 W.
R224 and R225	P29/3052151611	2.15K ohms ±1%, 1/4 W.
R226 and R227	P29/3051001611	1K ohms ±1%, 1/4 W.
R228	P29/3052151611	2.15K ohms ±1%, 1/4 W.
RP1 and RP2	P29/3080002000	Network, bussed: 4.7K ohms x 9; Bourns 4610X-101-472
RP3 thru RP6	P29/3080028000	Network, bussed: 10K ohms x 9; Bourns 4610X-101-103
RP7 and RP8	P29/3080045000	Network, bussed: 1K ohms x 9; Bourns 4610X-101-102
RP9 thru RP12	P29/3080028000	Network, bussed: 10K ohms x 9; Bourns 4610X-101-103
		----------JUMPERS----------
SP1 and SP2	P29/3800199000	AMP 531220-1.
		----------SWITCH----------
SW1	P29/3670009000	DIP: 4-position, SPST; C&K
		---------- TRANSFORMERS ----------
T1 and T2	P29/3380065000	Isolation, 600-ohm: Midcom BABT CR0090 671-8248.
		----------TEST POINTS ----------
TP1 thru T49	P29/3780023000	Test Point: Component Corp TP104-01-03
		----------INTEGRATED CIRCUITS ----------
U1 thru U8	P29/3580105000	Digital: 8 x 8 Analog Switch Array; Mitel MT8809AE.
U9 and U10	P29/3480079000	Linear: Audio Amp; LM386N-3.
U11 thru U13	P29/3480100001	Linear: Quad Op Amp; TL084ACN.
U14	P29/3080044000	Digital: Dual 10K Potentiometer; DS1267-10.
U15	P29/3480100001	Linear: Quad Op Amp; TL084ACN.

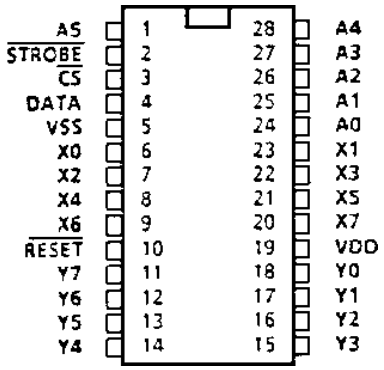
SYMBOL	PART NUMBER	DESCRIPTION
U16 and U17	P29/3480089000	Linear: Dual Transconductance Op Amp; LM13700.
U18 and U19	P29/3550003000	Digital: Hex Schmitt-Trigger Inverter; 74HC14.
U20	P29/3450015000	Linear: Optocoupler; TIL127.
U21 and U22	P29/3480100001	Linear: Quad Op Amp; TL084ACN.
U23	P29/3550033000	Digital: 4-to-16 Line Decoder/Demultiplexer; 74HC154.
U24	P29/3450015000	Linear: Optocoupler; TIL127.
U25 and U26	P29/3080044000	Digital: Dual 10K Potentiometer; DS1267-10.
U27	P29/3550003000	Digital: Hex Schmitt-Trigger Inverter; 74HC14.
U28	P29/3550034000	Digital: 8-Bit Addressable Latch; 74HC259.
U29 thru U31	P29/3480100001	Linear: Quad Op Amp; TL084ACN.
U33	P29/3550034000	Digital: 8-Bit Addressable Latch; 74HC259.
U34	P29/3480100001	Linear: Quad Op Amp; TL084.
U35	P29/3480144000	Linear: Dual Op Amp; NE5532N.
U36	P29/3480092000	Linear: Quad Op Amp; MC3303P.
		----------VOLTAGE REGULATORS ----------
VR1	P29/3460033000	Linear: 12-Volt Regulator; LT1086CT-12.
VR2	P29/3460034000	Linear: 5-Volt Regulator; LT1086CT-5.
		---------- ZENER DIODES----------
ZD1 thru ZD6	P29/3420129001	Silicon: 15-Volt; Motorola P6KE15.
ZD7	P29/3420129000	Silicon: 10-Volt; Motorola P6KE10A.
		----------MISCELLANEOUS ----------
2	P29/6110078000	Kit, Ejector; Scanbe S216-611.
3	P29/6120017000	Heatsink: Wakefiled 273-AB (Qty = 2).
4	P29/207A104C80	Nut: No. 4-40 x 3/16" (Qty = 12).
5	P29/6090280100	Panel, front.
6	P29/2100022000	Stud, pem: No. 4-40 x 3/8" (Qty = 12).
7	P29/208A104020	Lockwasher: No. 4, stainless steel (Qty = 12).

PRODUCTION CHANGES

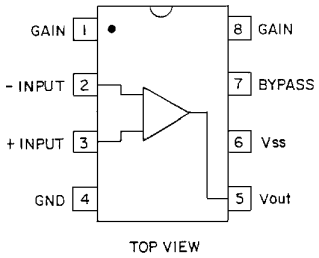
Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter" which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

Rev. A – <u>AUDIO MATRIX BOARD P29/7720030000</u>
Initial production release.

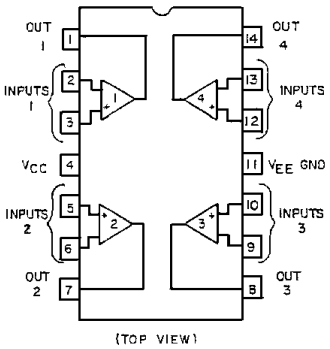
U1 - U8
8 x 8 ANALOG SWITCH
P29/3580105000 (MT8809AE)



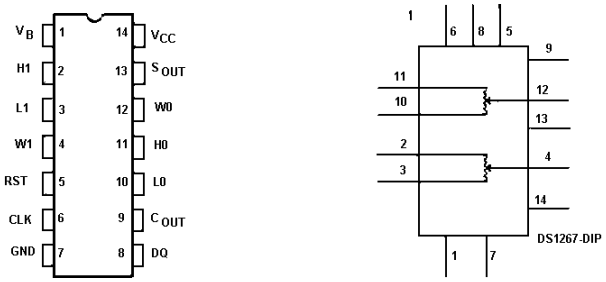
U9 & U10
AUDIO AMPLIFIER
P29/3480079000 (LM386N-3)



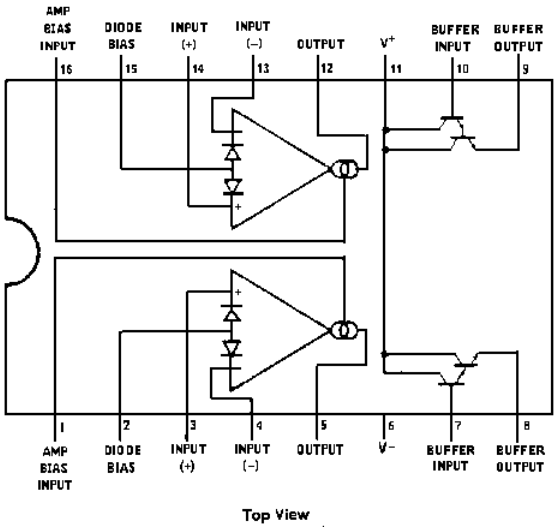
U11 - U13, U15, U21, U22,
U29 - U31 & U34, U36
QUAD OP AMPS
P29/3480100001 (TL084ACN)
P29/3480092000 (MC3303P)



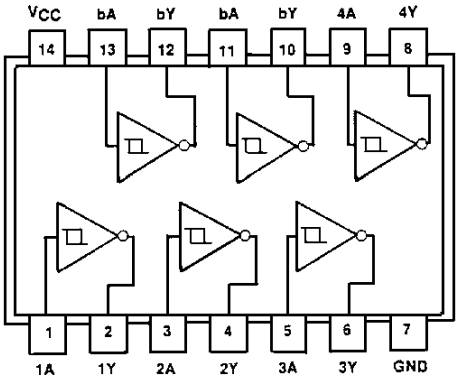
U14, U25 & U26
DIGITAL POTENTIOMETER
P29/3080044000 (DS1267-10)



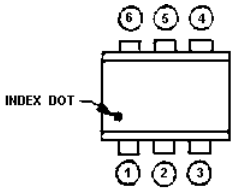
U16 & U17
DUAL TRANSCONDUCTANCE OP AMP
P29/3480089000 (LM13700)



U18, U19 & U27
HEX SCHMITT-TRIGGER INVERTER
P29/3550003000 (74HC14)



U20 & U24
OPTOCOUPLER
P29/3450015000 (TIL127)



Pin 1 identified by index dot.
Terminal connections:

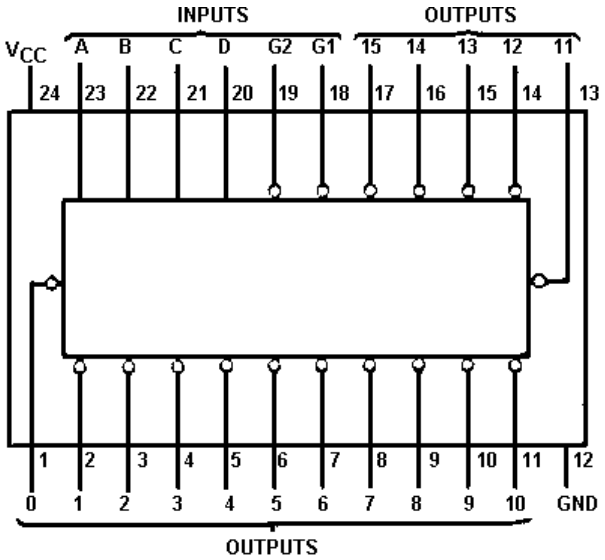
1. Anode
2. Cathode
3. No internal connection

Infrared - emit 1 diode

4. Emitter
5. Collector
6. TIL 127: Base

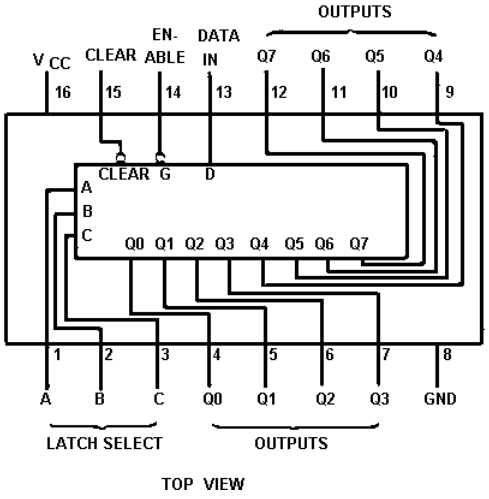
Photo-transistor

U23
4-TO-16 LINE DECODER
P29/3550033000 (74HC154)



TOP VIEW

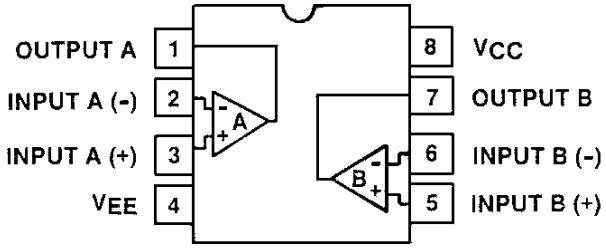
U28 & U33
8-BIT ADDRESSABLE LATCH
P29/3550034000 (74HC259)



TRUTH TABLE

Inputs		Outputs of Addressed Latch	Each Other Output	Function
Clear	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Decoder
L	H	L	L	Clear

U35
DUAL OP AMP
P29/3480144000 (NE5532N)



VR1 & VR2
VOLTAGE REGULATORS
P29/3460033000 (LT1086CT-12)
P29/3460034000 (LT1086CT-5)

FRONT VIEW