MAINTENANCE MANUAL

T1/E1 INTERFACE CARD
188D5909P1

TABLE OF CONTENTS

ERICSSON

TABLE OF CONTENTS (Continued)

SPECIFICATIONS*

FEATURES/CAPABILITY

T1/E1 Line Interface

Total Channels	
T1	24 full-duplex
E1 (CEPT)	31 full-duplex
Frame Formats	
T1 (1.544 Mbps full-duplex TDM)	4-Frame Multiframe (F4), 12-Frame Multiframe (F12, D3/4), Extended Superframe (ESF) and Remote Switch Mode (F72)
E1 (CEPT; 2.048 Mbps full-duplex TDM)	Double-frame and CRC multi-frame
Line Codes	
T1	B8ZS and AMI with ZCS
E1 (CEPT)	HDB3
Line/Channel Signaling	
T1	CAS-BR (Bit Robbing)
E1 (CEPT)	CAS-CC (channel 16 signalling)

T1/E1 Subrate Ports

Total Number	8 available if T1/E1 channels free
Synchronous Ports	Industry-standard DS0B subrate multiplexing across T1/E1 link at 9600 baud; Intraplex Inc. proprietary multiplexing method across CEC/IMC TDM network
Asynchronous Ports	Proprietary signalling across T1/E1 link at rates between 0 and 19,200 baud (inclusive)
Synchronous/Asynchronous Selection	Auto-configured by CEC/IMC Manager based on card mode, available T1/E1 channels, etc.

PCM Signal Format on CEC/IMC TDM Network

T1 Applications	μ-Law
E1 Applications	A-Law

Redundancy

System Clocks	Provided by CEC/IMC Clock Board and on-card clock monitoring and selection circuits

Diagnostics	T1/E1 signal active and frame sync acquired status indicators on front panel (See CEC/IMC Manager for detailed stats.)
Line Interfacing	Direct T1/E1 connection to PBX (Private Branch eXchange) telephone interconnect systems such as EDACS Jessica PBX Gateway equipment; CSU required for telephone company interface

T1/E1-to-CEC/IMC Clock Synchronization

External (slave mode)	CEC/IMC clocks frequency-locked to received T1/E1signal
Internal (master mode)	T1/E1 transmit signals frequency-locked to CEC/IMC clocks; external T1/E1 devices must be slaved to T1/E1 signal from CEC/IMC

CEC/IMC MANAGER (MOM PC) FUNCTIONS

User Configurable Parameters	CEC/IMC interface module mode, line type, frame format, line code, line length, signaling type, site channels' disbursements, slave clock mode.
Subrate Port Configuration	Auto-configured per user-configured parameters' settings
Monitoring Functions	T1/E1 signal active status, frame sync acquired status, frame error status, channel appropriations (logical/site channel(s), HSCX or subrate port(s)), subrate port sync/async configuration, detailed alarm and sync status, accumulated statistics

REGULATORY

Radio Frequency Interference	Meets FCC Part 15 and EN 55022 for Class A equipment
Line Interface	Meets CCITT G.703, G.732 and G.733

GENERAL

Card Physical Characteristics	Compatible with existing 6-rack unit CEC/IMC boards/cards (VME-like backplane) with two 96-pin DIN connectors
Operating Temperature	0 – 70° Celsius (32° – 158° Fahrenheit)
Power Supply Requirements	
+5-Volt Supply	1100 mA maximum
+15-Volt Supply & -15-Volt Supply	60 mA maximum each supply
Microprocessor	
Type	16-bit 80C186
Clock Rate	25 MHz
Reset Circuit	Power-up, manual and watch-dog reset circuits included
Memory Size (16-bit)	
ROM	
PEROM (flash)	128K (socketed)
EPROM	32K (socketed; not installed)
RAM	
Static	32K
Non-volatile	128K (socketed)
Clock Inputs	
System Clock Mode	Receives A/B 8 kHz frame sync clocks, A/B 2.048 MHz bit clocks and A/B 1.544 MHz T1 clocks generated by CEC/IMC Clock Board 19D903305P1 Rev. E (or later)
Required Stability for System Clock Inputs	±50 ppm for 2.048 and 1.544 MHz clocks
On-Card Clock Generation for T1/E1 Support	Generates a 4.096 MHz clock phase-locked to selected 2.048 MHz bit clock
Clock Selection	Selected per currently selected redundant system clock (A/B)
High-Speed Serial Link (HDLC)	
T1/E1 Interface Card-to-Controller Board	One 360 kbps half-duplex serial channel transfers control and diagnostic messages between the T1/E1 Interface Card(s) and the Controller Board within a CEC/IMC interface module

* These specifications are intended primarily for the use of the serviceman. See the appropriate Specifications Sheet for complete specifications.

DESCRIPTION

T1/E1 PORT

T1/E1 Interface Card 188D5909P1 provides a built-in T1 or E1 port for site-type CEC/IMC Digital Audio Switch interface modules (MIMs, NIMs, PIMs, etc.). This port allows direct interfacing to T1/E1 microwave, fiber-optic, or leased lines facilities. Consequently, co-located T1/E1 multiplexing (mux) equipment at the CEC/IMC is eliminated when the T1/E1 Interface Card is employed. In addition, CEC/IMC Audio Boards are also eliminated within the particular interface module.

Circuitry on the T1/E1 Interface Card can transfer PCM-encoded analog voice audio (clear voice) and PCM-encoded modem data signals on the CEC/IMC TDM network to and from the T1/E1 line. Examples of modem data signals include Aegis encrypted voice data and mobile data to/from an EDACS trunked site which has modem-equipped working channels.

Site-type CEC/IMC interface modules in which the T1/E1 Interface Card can be employed include MIMs (MASTR II/III Interface Modules), NIMs (Network Interface Modules) and PIMs (PBX Interface Modules). Within each of these CEC/IMC interface modules, one or more T1/E1 Interface Cards replace all Audio Boards.

The T1/E1 Interface Card furnishes twenty-four (24) full-duplex T1 channels in T1 mode and thirty-one (31) full-duplex E1 channels in E1 mode. T1/E1 mode selection is configurable at the CEC/IMC Manager (MOM PC) on a CEC/IMC-wide basis.

All CEC/IMC-related hardware is identical between T1 and E1 applications with the exception of unique Concentrator Cards which support T1/E1 connections into and out of the CEC/IMC cabinet; one Concentrator Card is required for T1 hook-ups and a different Concentrator Card is required for E1 hook-ups.

SUBRATE PORTS

In addition to its T1/E1 port, the T1/E1 Interface Card also contains eight (8) subrate ports which can provide modem-less data links over spare T1/E1 channels. Some, all, or none of these ports can be utilized depending upon card configuration. Five (5) of the subrate ports support synchronous or asynchronous data links and the remaining three (3) are synchronous-only ports. Subrate port available/not available and sync/async settings are auto-configured by the CEC/IMC Manager in accordance with the user-entered CEC/IMC Manager settings. These settings include T1 or E1 selection, card operating mode and the number of site channels required over the T1/E1 link.

The synchronous subrate data protocol conforms to the industry-standard DS0B subrate data multiplexing scheme. This standard allows multiplexing of five (5) 9600 baud synchronous ports on to a single T1/E1 channel. Any multiplexer conforming to this standard can transfer data to/from the synchronous subrate ports via the T1/E1 link. Only 9600 baud is supported on synchronous subrate ports. Port assignments are shown in Table 1 below.

Table 1 – Synchronous Subrate Port DS0B Assignments

← one DS0 (one T1/E1 channel; DS0B formatted) →				
sub-channel 1	**sub-channel 2**	**sub-channel 3**	**sub-channel 4**	**sub-channel 5**
If subrate ports 1 – 5:				
port 1	port 2	port 3	port 4	port 5
If subrate ports 6 – 8:				
(not used)	port 6	port 7	port 8	(not used)

The asynchronous subrate data protocol conforms to an Intraplex Inc. proprietary encoding/decoding format. Therefore, only an Intraplex mux or a second T1/E1 Interface Card can decode/encode asynchronous subrate data on the T1/E1 link. Each asynchronous subrate port requires one T1/E1 channel (DS0). Standard and non-standard baud rates up to 19,200 baud are supported. A typical example of data which may be transferred utilizing an asynchronous subrate port is System Manager-to-Site Controller data.

OPERATING MODE

In addition to T1 or E1 selection, T1/E1 Interface Card configuration includes the determination of a primary card operating mode referred to as “analog/modem mode”. Other primary card modes not discussed within this introductory text will be supported in subsequent software/firmware releases.

Analog/Modem Mode

In the analog/modem mode, the T1/E1 Interface Card transfers PCM-encoded signals between the CEC/IMC TDM network and the T1/E1 line. PCM-encoded signals transferred by this mode include analog (clear) voice signals, modem-encoded digital voice signals (for example, Aegis encrypted voice to/from a modem-equipped trunked site working channel), and/or modem-encoded data signals (for example, mobile data to/from a modem-equipped trunked site). In this mode each site channel is assigned to a T1/E1 channel. In addition, as described later, this mode

allows use of the T1/E1 Interface Card's subrate ports if T1/E1 channels are available after site channel assignments. See Figure 1. This mode is designated "Analog or Digital Voice using Modems" at the CEC/IMC Manager (MOM PC).

NOTE

Modems used throughout EDACS networks for digital voice (Aegis, Voice Guard, etc.), data (mobile data, etc.) and uplink/downlink data transfers employ Quadrature Amplitude Modulation (QAM) techniques. QAM modems use 4-level 4-phase signals to transfer data over twisted pairs.

Two (2) CEC/IMC TDM bus slots coincide to one full-duplex T1/E1 channel. This is exactly analogous to a CEC/IMC Audio Board channel where two TDM bus slots coincide to one full-duplex 4-wire 600-ohm audio channel provided by the Audio Board. The T1/E1 Interface Card extracts a signal from one bus slot and sends it out on a T1/E1 channel. Accordingly, signals received on this same T1/E1 channel are applied to a different CEC/IMC TDM bus slot.

For example, a clear voice individual call originating from a console is placed on TDM bus 8, time slot 10 via the console's CIM as a PCM-encoded audio signal. Simultaneously, the T1/E1 Interface Card within a MIM extracts the call from bus 8, time slot 10 and sends it out over T1/E1 channel 5 (for example) to mux equipment at the respective EDACS trunked site. The PCM-capable mux equipment at the site then performs T1/E1 to audio conversions and the audio is then applied to the EDACS station. In this example, T1/E1 channel 5 also transfers radio-originated audio from the EDACS trunked site to a different TDM bus and/or slot in the CEC/IMC. The CIM within the CEC/IMC extracts this radio-originated individual call audio from the TDM bus and slot and it applies the extracted audio (after PCM decoding) to the console. This completes the full-duplex audio link.

When compared to Audio Board-equipped CEC/IMC interface modules, T1/E1 Interface Card-equipped CEC/IMC interface modules require fewer Card Cage slots. For example, a 24-channel non-redundant Audio Board-equipped MIM requires seven (7) Card Cage slots – one for

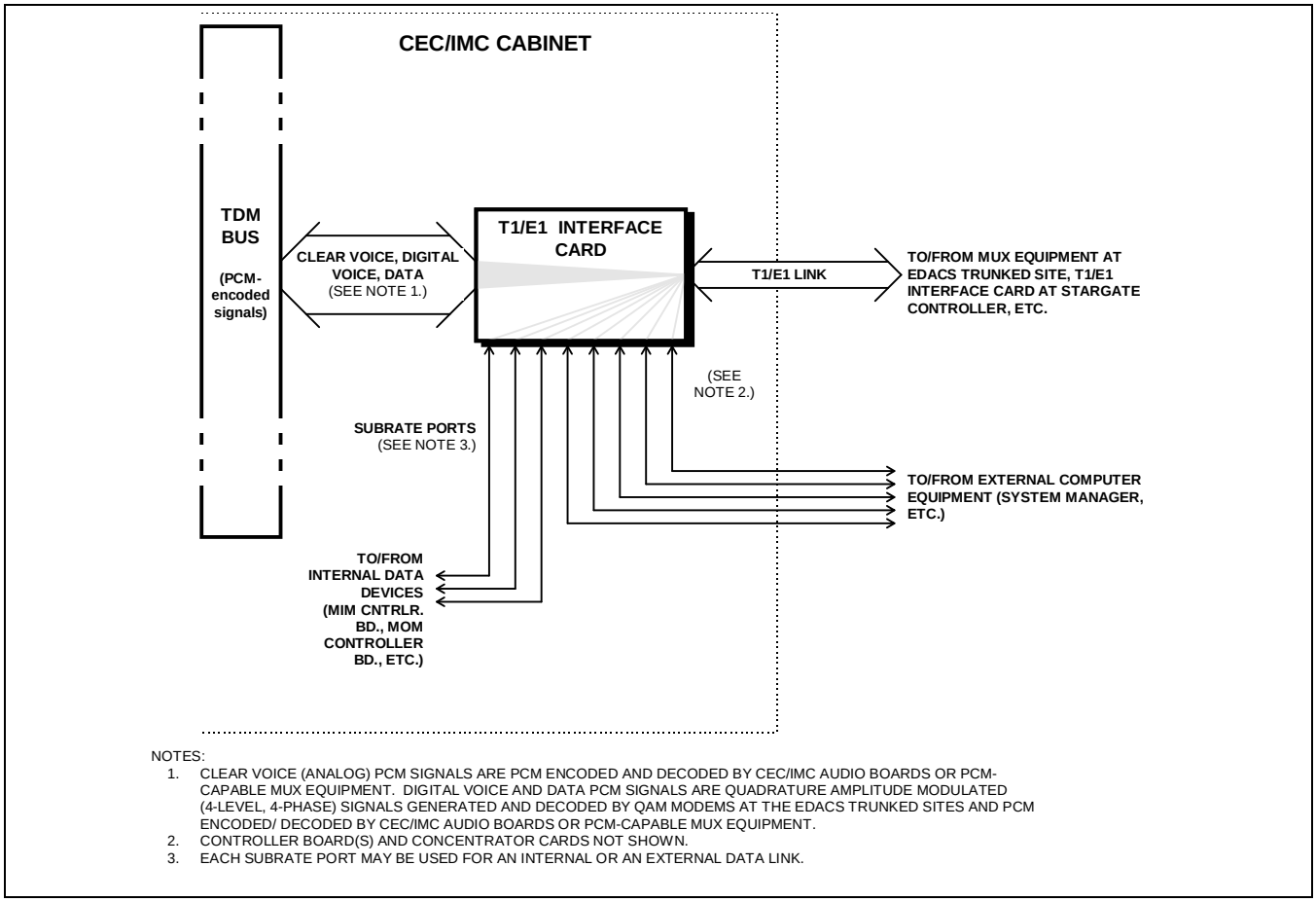


Figure 1 – Analog/Modem Mode

the Controller Board and six for the 4-channel Audio Boards whereas a 24-channel non-redundant T1/E1 Interface Card-equipped MIM operating in the analog/modem mode requires only two (2) Card Cage slots – one for the Controller Board and one for the T1/E1 Interface Card. This represents a savings of five (5) Card Cage slots.

As previously stated, free channels on each card's T1/E1 link are available for user data to/from the subrate ports. Subrate ports are auto-configured by the CEC/IMC Manager as shown in Table 2 in accordance with the number of free T1/E1 channels.

Table 2 – Subrate Port Assignments For Analog/Modem Mode

FREE CHANNELS (PER CARD)	SUBRATE PORT AUTO-CONFIGURATION *
0	no subrate ports available
1	port 1 = async ports 2 – 8 = not available
2	port 1 = async ports 2 – 5 = sync ports 6 – 8 = not available
3	ports 1 & 2 = async ports 3 – 5 = sync ports 6 – 8 = not available
4	ports 1 – 3 = async ports 4 & 5 = not available ports 6 – 8 = sync
5	ports 1 – 4 = async port 5 = not available ports 6 – 8 = sync
greater than 5	ports 1 – 5 = async ports 6 – 8 = sync

* "sync" = subrate port set for synchronous operation;
"async" = subrate port set for asynchronous operation.

CEC/IMC SYSTEM CLOCKS

A/B Redundant System Clocks

Redundant clocking for the CEC/IMC's TDM network and T1/E1 circuits is provided by separate system clock circuits identified "A" and "B" throughout the CEC/IMC. These redundant clocks, generated by the CEC/IMC Clock Board(s), are applied to all T1/E1 Interface Cards and all Audio Boards within the CEC/IMC via the CEC/IMC Backplane. Normally, a CEC/IMC is factory-equipped with two (2) Clock Boards so if one fails the other can provide clocking (with A/B redundancy) while the failed board is removed for service.

NOTE

T1/E1 Interface Card applications require Clock Board 19D903305P1 Rev. E (or later).

Redundant CEC/IMC system clock selection within a T1/E1 Interface Card-equipped interface module is accomplished identically to redundant system clock selection within an Audio Board-equipped interface module. Clock A/B selection is dictated by the CEC/IMC MOM Controller Board in accordance with the start-up default and any following clock A/B fail messages received from other CEC/IMC interface modules (MIM, CIM, NIM, LRIM, etc.) The initial start-up or default clock is B. Refer the circuit analysis section entitled "**CLOCK SELECTION AND GENERATION**" (page 21) for additional details.

All T1/E1 Interface Card firmware/software releases support system clock redundancy. Assuming the redundant clock feature has been enabled at the CEC/IMC Manager, redundant clock switching (B to A or A to B) will occur if several interface modules sense and report clock failures to the MOM Controller Board. Refer to the Circuit Analysis section of this manual for detailed circuit descriptions and additional high-level system clock redundancy information. System clock A/B redundancy *is not* available when the T1/E1 Interface Card operates in the stand-alone mode. This mode is not supported in the initial firmware/software release(s).

Network Synchronization Design

Within a given CEC/IMC network, all T1/E1-connected nodes utilizing T1/E1 Interface Cards must remain frequency-locked at all times. Therefore, the system design allows for total network synchronization by offering the following clock synchronization options. The term "node" in this text refers to equipment external to the CEC/IMC with T1/E1 line interfacing provided by a T1/E1 Interface Card at the CEC/IMC, or another CEC/IMC:

- **Master** – The *CEC/IMC is the master* source of network clock synchronization and all other nodes – for example, muxes at EDACS trunked sites – are *slaved* (synchronized) to it. A CEC/IMC Clock Board generates the master clocking for the CEC/IMC and for all of the nodes. Installed Clock Boards within the CEC/IMC basically "free run" since they are not synchronized to any external source. Redundant clocking within the CEC/IMC is provided by the A and B system clocks.

  Within a CEC/IMC, this clock sync option is selected by setting all Clock Board DIP switches to "master mode" and, via the CEC/IMC Manager, setting all T1/E1 Interface Cards' "slave clock mode" to "none".

- **Slaved To T1/E1 Line** – CEC/IMC redundant A/B system clocks generated on the installed Clock Board(s) are *synchronized to one T1/E1 line* from a node – for example, the telephone company. Redundant line synchronization may be provided by a second T1/E1 line interfaced via a second card. CEC/IMC system clocks are slaved to the (in use) line's external node. The T1/E1 Interface Card passes synchronization from its T1/E1 line to the installed Clock Boards via a set of redundant slave A and slave B sync lines on the CEC/IMC Backplane. These slave sync lines should not be confused with the redundant A/B system clock lines on the Backplane; they have similar designations but they are not directly related. For example, a CEC/IMC using this option may be operating off of its B system clocks but using the slave A sync line.

  Within the CEC/IMC, this option is selected by setting all Clock Board DIP switches to "slave to 8 kHz mode". Also, to set-up the driver source for each of the two sync lines, one T1/E1 Interface Card's "slave clock mode" must be set to "A" and another card must be set to "B" for sync redundancy, *or* for no sync redundancy, one card's "slave clock mode" can be set to "A & B". The "slave clock mode" setting is accomplished via the CEC/IMC Manager.

  If configured for sync redundancy with two T1/E1 Interface Cards the two T1/E1 Interface Cards must be connected to nodes which are *frequency-locked together*. For example: two EDACS trunked sites linked to the CEC/IMC via *a telephone company's T1/E1 lines*.

- **Slaved to External 1.544 MHz Clock** – CEC/IMC redundant A/B clocks generated on a Clock Board are *synchronized to one external 1.544 MHz clock source* from external equipment. Typical external equipment examples include a T1 multiplexer, microwave link equipment, or fiber-optic network equipment. In these equipment examples, the equipment's timing or clock output is utilized. Each Clock Board in the CEC/IMC must be supplied with an external 1.544 MHz clock either from the same piece of external equipment if no redundancy is required, or from different external equipment (one per Clock Board) for redundant slaving. 1.544 MHz clocking is applied to a Clock Board via RS-422 or RS-232 input connections at the board's 24-pin dual-in-line Backplane Card Cage slot connector.

  This option is entered by setting each installed Clock Board's DIP switches to "slave to external 1544 kHz mode" and, via the CEC/IMC Manager, setting all installed T1/E1 Interface Boards' "slave clock mode" to "none".

- **Slaved to External 2.048 MHz Clock (E1 only)** – This option is identical to the previously described option except a 2.048 MHz clock frequency is utilized. Also, this option is only available if CEC/IMC T1/E1 Interface Cards operate in E1 mode.

  This option is entered by setting each installed Clock Board's DIP switches to "slave to external 2048 kHz mode" and, via the CEC/IMC Manager, setting all installed T1/E1 Interface Boards' "slave clock mode" to "none".

The following guidelines must be followed for network synchronization. Here, the term "node" refers to any equipment interfaced to the CEC/IMC via a T1/E1 line using a T1/E1 Interface Card, the CEC/IMC itself, and/or any equipment supplying source clock timing to the CEC/IMC:

- One node in the system must be the MASTER source of network timing – "**the MASTER node**". The CEC/IMC will support a primary and a redundant (back-up) MASTER node source of timing as described in the preceding text.

- Examples of MASTER nodes include a CEC/IMC, an EDACS trunked site interfaced to the CEC/IMC via a T1/E1 Interface Card-equipped MIM, and EDACS Jessica PBX Gateway equipment interfaced to the CEC/IMC via a T1/E1 Interface Card-equipped PIM. **Again, there can be only one MASTER node in a system (plus a redundant MASTER node).**

- All leased T1/E1 line facilities from a telephone company are frequency-locked by the telephone company. If any phone company T1/E1 line connections exist in the network, one of the connections must be the MASTER node source of timing. Any other phone company T1/E1 line connection may be the redundant MASTER node source of timing. Leased line-interfaced node examples may include MIM-to-EDACS trunked site T1/E1 links, NIM-to-NIM T1/E1 links, and T1/E1 connections through an MD110 (Jessica).

- Any node using analog interfaces (including analog connections to/from an MD110 to the phone company) may be disregarded for synchronization purposes.

- If a node is not the MASTER node, it must be slaved to the T1/E1 line to/from the MASTER node.

CIRCUIT ANALYSIS

NOTE

This circuit analysis contains descriptions of hardware features which may not be available in the initial firmware/software release(s) of the T1/E1 Interface Card and CEC/IMC Manager.

MICROPROCESSOR CIRCUITS

Microprocessor

Control processing for the T1/E1 Interface Card is provided by U1, an Intel 80C186 (or equivalent) 16-bit microprocessor. It runs at 25 MHz as set by crystal Y1. DC operating power is provided by the +5 Vdc power received from the card's +5V power supply line. Support circuits include:

- reset circuit with watchdog timer
- address latches
- memory – ROM, RAM and non-volatile RAM
- a single-channel UART which provides a PC serial port for diagnostic operations
- two dual-channel high-speed serial controllers (HSCX)
- DIP switch interface
- an input/output (I/O) port

Reset Circuit With Watchdog Timer

Reset circuitry on the T1/E1 Interface Card consists of a microprocessor supervisory chip, a monostable multivibrator, several logic gates and an NPN transistor. This circuitry resets the microprocessor and the entire card at power-up, or if the 5 Vdc power supply falls below approximately 4.65 Vdc, or if the microprocessor fails to periodically write to the reset circuit. This last case is a

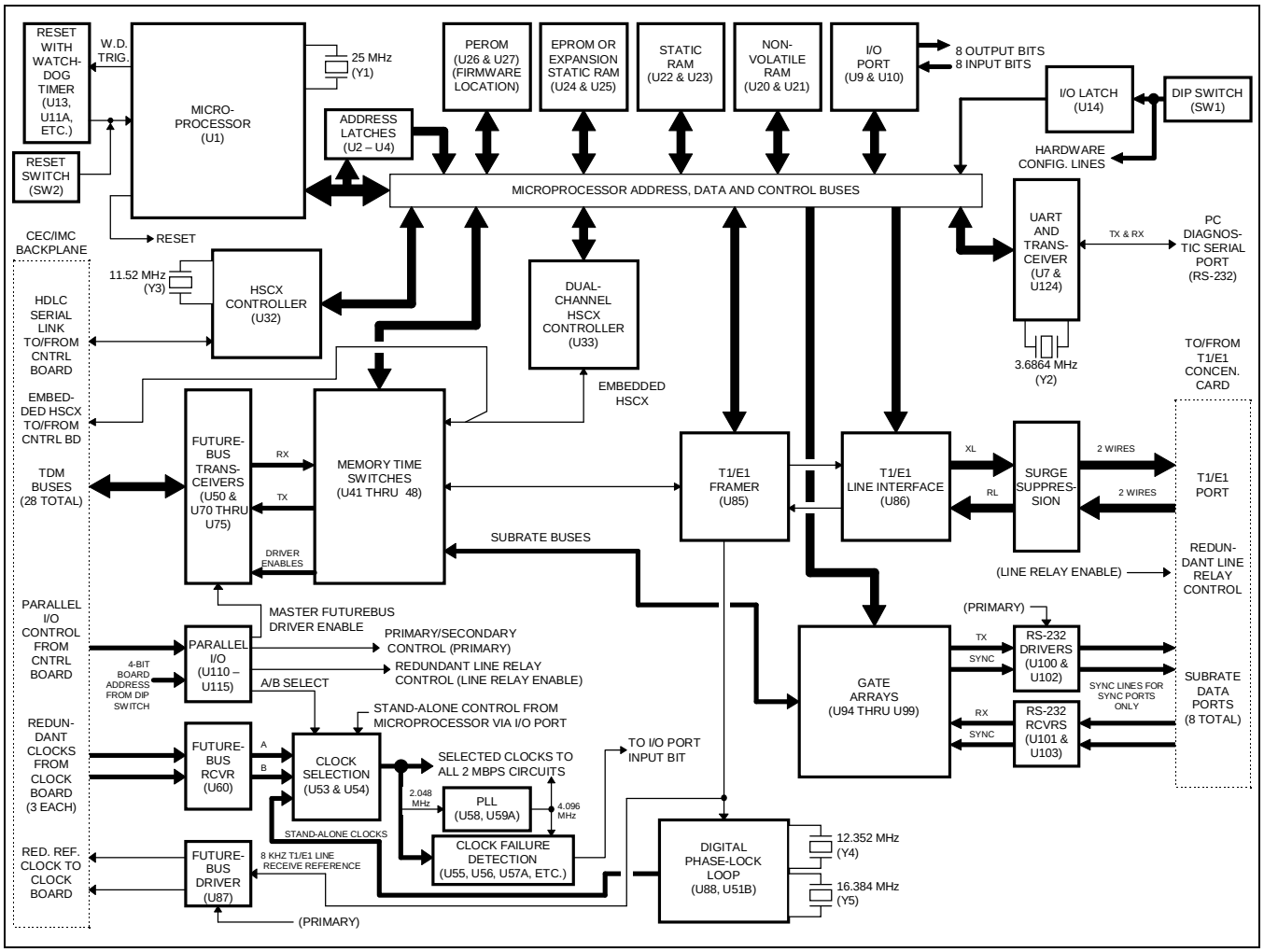


Figure 2 – T1/E1 Interface Card Block Diagram

"watchdog" timer function. The watchdog timer may be disabled by a DIP switch setting [schematic diagram sheet 1].

Integrated circuit U13 is a microprocessor supervisory chip that performs the power-up reset and most watchdog timer functions for the reset circuit. Microprocessor U1 is in the reset or inactive state whenever its reset input at pin 24 is low. !RES from U13 pin 15 drives this active-low processor input.

Manual resets may be performed by push-button switch SW2 which is mounted on the card's front panel. When pressed, SW2 simply grounds the !RES line. Switch contact debouncing is provided by C4 and R34.

Power-Up Reset

At power-up, U13 holds its active-low reset output at pin 15 (!RES line) low until approximately 50 milliseconds *after* the +5V power supply line stabilizes. The T1/E1 Interface Card is in a reset (non-operating) state during this time.

Unregulated +5V Reset

As previously stated, U13 will also reset U1 if the +5V supply line falls below approximately 4.65 Vdc. This resets the card and thus prevents unpredictable operating errors during unstable power supply conditions. Reset will be released approximately 50 milliseconds after the +5V line raises above 4.75 Vdc.

Watchdog Timer Reset

During normal card operation U1 periodically pulses (at least every 1.5 seconds) the watchdog timer circuit by writing to address 40000H. This causes active-low pulses to simultaneously appear at the micro's active-low !WR line (U1 pin 63) and at its active-low output identified !WDOG_TRIG (U1 pin 25). These logic lines are applied to the inputs of OR gate U6C. When !WR and !WDOG_TRIG transition low, U6C's output triggers monostable multivibrator U11A. This monostable is utilized to ensure valid triggering of U13's watchdog input; it extends the very narrow watchdog trigger pulse from U1.

The monostable's active-low output and a logic line from the watchdog enable/disable DIP switch are logically ANDed by U12A. The output of this gate drives transistor Q1 which in turn, drives U13's watchdog trigger input.

If watchdog enable/disable switch SW1 position 1 is in the "CLOSED" or "ON" position (watchdog disabled), the !WDOG_DIS line at U12A pin 2 remains low. This prevents the monostable's pulse from passing through the AND gate and thus Q1 remains off at all times. In this case, U13's watchdog input always floats. Circuitry inside U13 disables the watchdog reset function when the watchdog trigger input floats.

If watchdog enable/disable switch SW1 position 1 is in the "OPEN" or "OFF" position (watchdog enabled), the !WDOG_DIS line at U12A pin 2 remains high per pull-up resistor R29. This allows the pulse from monostable U11A to pass through the AND gate and Q1 and pulse U13's watchdog trigger input. Thus, the watchdog circuit is active and it will reset U1 if U1 does not periodically trigger it.

Microprocessor Reset Output

When microprocessor U1 is reset by U13, U1 pulls its reset output at U1 pin 57 high. This logic level is applied to the succeeding gates, U6A, U31E and U120D, which drive the RESET (active high) and !RESET (active low) lines. These two reset lines are used to reset all other logic circuitry on the card such as the HSCX controller chips.

NOVRAM Disable

U13 also outputs a logic signal at pin 12 (!CEOUT). This output is used to insure the NOVRAM (non-volatile RAM) chips on the card are not accessed during unstable power supply conditions. U13 pin 12 transitions low only when the +5V supply line is above the reset threshold voltage of approximately 4.65 Vdc. OR gate U30A gates !LCS on to the !NOVRAM_CS line only when !CEOUT is low [schematic diagram sheets 1 and 2].

Address Latches

The 80C186 microprocessor employs a multiplexed 16-bit address and data bus which is identified AD0 thru AD15. It uses this bus to transfer data to and from memory and I/O devices *and* it outputs the lower sixteen bits of the address to address latches U2 and U3. Two non-multiplexed address bits, A16/S3 and A17/S4, are also utilized. These bits are latched by dual flip-flop U4 [schematic diagram sheet 1].

During an external memory or I/O read or write, microprocessor U1 first applies the 18-bit address to its AD0 thru AD15, A16/S3 and A17/S4 outputs. Next, it latches the 18-bit address into the address latches on the falling edge of the ALE pulse (from U1 pin 61). Latched address lines are identified A[0] thru A[17] and the complete address bus is labeled A[0:17]. These lines are applied to memory and I/O chips on the card. The bidirectional data bus is identified D[0:15].

Memory

The T1/E1 Interface Card's memory map includes 128K x 16 bits of PEROM, 32K x 16 bits of EPROM (not normally used), 128K x 16 bits of non-volatile RAM

(NOVRAM), and 32K x 16 bits of static RAM. The PEROM chips store the operating firmware code. With the exception of the static RAM chips, all memory chips are socketed. A detailed memory map chart is included on the schematic diagram [schematic diagram sheet 2].

PEROM and EPROM

Currently, as noted on the schematic, no EPROM chips are installed and all operating firmware code is stored in two PEROM (Programmable Erasable ROM) chips, U26 and U27. PEROMs are very similar in functionality to 5-volt flash ROMs. Future upgrades of this card will support flash firmware programming. The EPROM sockets can be loaded with static RAM chips if volatile memory expansion is required.

U26 and U27 are each 128K x 8-bit PEROM chips which together provide the total 128K x 16 bits of firmware storage space. U26 handles the lower byte, D[0] thru D[7], and U27 handles the upper byte, D[8] thru D[15]. Chip selection is accomplished via the !UCS from U1 pin 34. This active-low chip select line is applied to pin 22 of both PEROMs. Therefore, both chips are selected simultaneously when a 16-bit op-code fetch occurs. Read/write control is provided by the active-low !RD and !WR lines from U1. The !WR line is only utilized during PEROM reprogramming.

NOVRAM and Static RAM

A two megabit sector of non-volatile RAM is used to store data which must be retained through a power loss cycle. U20 and U21, each a 128K x 8-bit device, provide the 128K x 16-bit NOVRAM sector. U20 stores low bytes and U21 stores high bytes.

As previously described, U13 in the reset circuit outputs a logic signal at pin 12 (!CEOUT) which is used to insure the NOVRAM chips on the card are not accessed during unstable power supply conditions. NOVRAM chip selection is generated by gating the !LCS line from U1 pin 33 through OR gate U30A using the !CEOUT line from U13 pin 12. !CEOUT normally remains low but it transitions high if the +5V supply becomes unstable. This prevents NOVRAM write errors.

Static RAMs U22 and U23 provide 32K x 16-bits of volatile RAM for the T1/E1 Interface Card. U22 stores lower bytes and U23 stores upper bytes. Chip selection is provided by the active-low !MCS0 line from U1 pin 38. !MCS0 is applied to the chip-select input at pin 20 of each static RAM chip.

Read/write control for the NOVRAM and static RAM is provided by the active-low !RD (read), !WRLB (write low byte), and !WRHB (write high byte) lines. !RD from U1 pin 62 is applied to the active-low output-enable inputs of all four RAM chips. During 8-bit RAM reads, U1 actually enables and reads both the upper and lower byte RAM chips – just like a 16-bit read – but it uses only the upper byte or the lower byte, as required. !WRLB and !WRHB are generated from A[0], !BHE and !WR by OR gates U30B and U30C. These two byte-oriented active-low write enable lines are also used for HSCX controller and gate array 8-bit writes. This design allows 8-bit or 16-bit writes in the 16-bit bus system.

PC Diagnostic Serial Port

DB-9 connector J5 [schematic diagram sheet 10], mounted on the front panel of the T1/E1 Interface Card, provides a serial port hook-up for a Personal Computer (PC) type interface. Using this port and custom software executing on a PC, diagnostic tests may be performed on the card.

Two (2) integrated circuits support the port, U7 and U124 [schematic diagram sheets 1 and 10]. U7 is a single-channel 8-bit UART which communicates with microprocessor U1 via the lower data bus byte, D[0] thru D[7]. U124 is an RS-232 (EIA-232-D) transceiver chip which contains three TTL-to-RS-232 drivers and three RS-232-to-TTL receivers; however, only one of each is utilized for the diagnostic port. Serial data from the PC is applied to J5 pin 2 (RX) and serial data is sent to the PC via J5 pin 3 (TX). A common ground for both signals is located at J5 pin 5.

RS-232-level serial data on J5 pin 2 is converted to TTL levels by the receiver. The receiver's converted output at U124 pin 15 drives the UART's TTL-level receive data input via RxD0. Similarly, TTL-level transmit data from the UART (U7 pin 4) is applied to U124 pin 14 via TxD0. The driver within U124 converts this TTL-level serial data to RS-232 levels and drives J5 pin 3 via the TX line.

As previously stated, UART U7 communicates with microprocessor U1 via the lower data bus byte. Control lines from U1 include the active-high RESET line, and the active-low !RD (read), !WR (write), and !SER_EN (serial enable) lines. U7's active-low interrupt output at pin 16 is inverted by U5A and applied to a U1's active-high interrupt input at pin 44 via the UARTXINT line.

Dual-Channel HSCX Controllers

Two Siemems 82525 (or equivalent) dual-channel HSCX controller chips, U32 and U33, furnish advanced high-speed serial communications links for the T1/E1 Interface Card. These channels are identified A and B at each HSCX controller chip. Channel A of U32 is not currently used [schematic diagram sheet 2].

U32 Channel B – Controller Board HDLC Link

Using an HDLC protocol, channel B of U32 links the T1/E1 Interface Card to the Controller Board via the AU_SER_CNTRL line. Within a CEC/IMC interface module (MIM, NIM, etc.) equipped with T1/E1 Interface Card(s), this 360 kbps single-wire half-duplex serial channel transfers control and diagnostic messages between the active Controller Board and the T1/E1 Interface Card(s) within the interface module. With the exception of the parallel I/O control lines from the Controller Board, all Controller Board-to-T1/E1 Interface Card control messaging occurs over this link.

Like the parallel I/O control lines, AU_SER_CNTRL is routed between the Controller Board and the T1/E1 Interface Card(s) via the CEC/IMC Backplane and the interface module's Local Bus Cable(s). If the interface module contains more than one T1/E1 Interface Card, a Controller Board polling scheme individually communicates with each T1/E1 Interface Card as needed.

Channel B of U32 is normally in a listening or slave mode and it only transmits to the Controller Board when specifically polled by it. This serial link configuration is the 82525's point-to-multipoint configuration mode. The Controller Board's HSCX port is the master and T1/E1 Interface Cards' ports are slaved to it. Serial baud rate is determined by 11.52 MHz crystal Y3 and U32 HSCX set-up programming from microprocessor U1.

Serial connections are located at U32 pins 13, 14 and 16. AU_SER_CNTRL line is applied to the CEC/IMC Backplane via 96-pin DIN connector J1 pin 8C. J1 is the top DIN connector at the rear of the card [schematic diagram sheet 10].

U33 Channels A & B – Embedded HSCX Links

NOTE

U33 circuitry described in this section is not functional with initial firmware/software release(s).

Channels A and B of U33 are utilized to synchronize 64 kbps data channels on a slotted two megabit bus. These proprietary-protocol channels can independently route data to/from the T1/E1 line or to/from the CEC/IMC TDM network.

Data from the CEC/IMC TDM network or the T1/E1 line is applied to U33 via HSCX_PCM_RX at U33 pin 9 (channel A input) and pin 16 (channel B input). Correspondingly, data is sent to the TDM network or the T1/E1 line via HSCX_PCM_TX from U33 pin 12 (channel A output) and pin 13 (channel B output). Switching or signal routing to and from U33 is accomplished via CMOS memory time switch (MTSC) chips which are described in detail later in this document. Basically, U33 HSXC channels A and B can be routed to/from TDM bus/slot channels or T1/E1 channels via the MTSC chips. One MTSC chip (U48) is used to route HSCX_PCM_TX data from U33 to the T1/E1 framer chip (U85). Also, one MTSC chip (U41) routes data from the framer chip to U33 via HSCX_PCM_RX.

The HSCX_PCM_TX and HSCX_PCM_RX signals are also present on the CEC/IMC Backplane so the interface module's Controller Board can directly access the HSCX TDM buses. In future software/firmware releases, this will allow direct embedded Controller Board 64 kbps HSCX channels over the T1/E1 line or over the CEC/IMC TDM network.

To provide redundant T1/E1 Interface Card pairing capability, HSCX_PCM_RX and two related clock signals, FSYNC and 20048KHZ, are buffered and gated by drivers U120A thru U120C before application to the CEC/IMC Backplane [schematic diagram sheet 10]. The buffered and gated signals, HSCX_RX_F, FSYNC_F and 2048_F are present at 96-pin DIN connector J1 pins 5C, 7C and 4C respectively. HSCX_PCM_TX is present on J1 pin 6C. Drivers U120A thru U120C are enabled by AND gate U57B. Inputs to U57B include card address bits ADDR[0], !ADDR[1] (inverted ADDR[1] via inverter U31F), and PRI/!SEC. These logic controls guarantee the drivers are not enabled unless the card address is 1 or 5 and it is in primary mode (PRI/!SEC = high). Cards 1 and 5 are configured as redundant paired cards. The active Controller Board's HSCX chip can transmit directly to the MTSC chips via HSC_PCM_TX.

Microprocessor Interface

As shown by the D[0] thru D[7] connections at U32 and the D[8] thru D[15] connections at U33, U32 is mapped into the lower byte of the microprocessor's data bus and U33 is mapped into the upper byte. Both chips are simultaneously selected, read, and written to by U1. This is accomplished by activating the active-low !PCS5 or !PCS6 (peripheral chip selects) signals from U1 pins 31 and 32 respectively. The OR function is provided by AND gate U12B and these active-low logic lines; if !PCS5 *or* !PCS6 transition low (active) the AND gate's output transitions low (active). The resultant active-low !HSCX_CS line is applied to the chip-select input at each HSCX controller chip (U32 and U33 pin 8). Two !PCS lines are required since the HSCX controller chips require more address space than one !PCS line can provide.

Each HSCX controller is equipped with an interrupt output which is used to signal U1 when HSCX service is

required. This active-low open-drain output at pin 28 of each HSCX chip is logically ORed by joining the two outputs together. The inverted and buffered signal from U31D is applied to U1's interrupt input at pin 41 via the HSCX_INT connection. When U1 is interrupted by HSCX_INT, it services the HSCX chip(s) as required via the data bus.

Configuration DIP Switch

SW1 is an 8-position DIP switch used to configure certain card parameters [schematic diagram sheet 1]. Although the entire switch is read by the microprocessor via U14 at card power-up or reset, current firmware only recognizes positions 5 thru 8 – the card address setting. Therefore, a card reset is not necessary after a position 1, 2 or 3 change; hardware connections to these three switches bypass the microprocessor circuits. Currently, SW1 position 4 is not used. Each switch position has a pull-up resistor which pulls the respective U14 logic input high when the switch position is "OPEN" or "OFF".

Microprocessor U1 reads the 8-position DIP switch via octal transceiver U14 and OR gate U6D. Chip selection for U14 is mapped to the same address as the watchdog timer circuit – 40000H – the !WDOG_TRIG line. U1 writes to address 40000H to trigger the watchdog timer circuit but it reads 40000H to enable U14 and read the DIP switch settings. OR gate U6D enables U14 when !RD and !WDOG_TRIG are both low via U14's active-low enable input at pin 19. As previously stated, current firmware only recognizes SW1 positions 5 thru 8 – the card address setting.

Positions 1 Thru 3

Positions 1 thru 3 enable/disable certain hardware functions. **All three of these switches should remain in the "OPEN" or "OFF" (enabled) position during normal operation; they are provided for testing and troubleshooting procedures only.**

SW1 position 1 enables/disables the watchdog timer via the !WDOG_DIS connection to AND gate U12A [schematic diagram sheet 1]. This gate is located in the reset circuit. When the switch is "OPEN" or "OFF", !WDOG_DIS is high and the watchdog timer is enabled. See previous circuit analysis descriptions on the watchdog timer reset circuit for additional details (page 10).

SW1 position 2 controls the !PRIMARY_EN line. When this line is low (test state), the card is forced into primary operation mode. !PRIMARY_EN is applied to the preset input of data flip-flop U111B [schematic diagram sheet 9]. This flip-flop generates the PRI/!SEC and !PRIMARY primary/secondary control lines which are distributed throughout the card to control primary/secondary operation. When !PRIMARY_EN is high (normal state), the parallel I/O control circuits can control the primary/secondary lines. See the section entitled "**PARALLEL I/O CONTROL**", subsection "**Primary/Secondary Mode Selection**" (page 34) for additional details.

SW1 position 3 controls the Futurebus driver enable line, !FBUS_DRV_EN. When "OPEN" or "OFF" this line is high (normal state) and the parallel I/O control lines from the Controller Board can enable and disabled the Futurebus drivers on the T1/E1 Interface Card. When "CLOSED" or "ON", !FBUS_DRV_EN is pulled low (test state) and the Futurebus drivers are always enabled. !FBUS_DRV_EN is applied to the preset input of data flip-flop U51A [schematic diagram sheet 4]. This flip-flop generates the !FBUS_EN line which controls (enables/disables) Futurebus transceivers U50 and U70 thru U75 [schematic diagram sheets 4 and 5]. Again, this switch should be left "OPEN" or "OFF" at all times.

Positions 5 Thru 8 – Card Address Setting

As shown in Table 3, positions 5 thru 8 specify the card address in a binary form. Only address 1 is valid with current firmware. Like the CEC/IMC Audio Boards, each T1/E1 Interface Card within a particular CEC/IMC interface module (MIM, NIM, etc.) must have a unique card address setting. ADDR[0] thru ADDR[3] at U14's inputs are also applied to 4-bit comparator U110 in the parallel I/O control circuit [schematic diagram sheet 9].

Table 3 – SW1 Positions 5 Thru 8; Card Address Setting

CARD ADDRESS	5 (MSB)	6	7	8 (LSB) *
1	0	0	0	1
2 **	0	0	1	0
3 **	0	0	1	1
4 **	0	1	0	0
5 **	0	1	0	1
6 **	0	1	1	0
7 **	0	1	1	1
8 **	1	0	0	0

* "0" = CLOSED/ON; "1" = OPEN/OFF

** Card addresses 2 thru 8 are not valid with initial software/firmware release(s). See SRN-1000-xx for specific details.

Input/Output Port

A 16-bit I/O port allows microprocessor U1 to monitor and control several card functions. Octal latch U10 and OR gate U6B form the 8-bit input side and octal latch U9 and OR gate U8A form the 8-bit output side [schematic diagram sheet 1].

Microprocessor U1 reads the eight input bits by reading address 40180H. The input bits are defined in Table 4. A read of this address activates !I0_EN (U1 pin 29) and !RD (U1 pin 62). These two active-low logic signals are ORed by U6B and the resultant low-going pulse is applied to the output enable input of U10. As a result, logic levels on U10's data inputs (pins 2 thru 9) are applied to the lower byte of the microprocessor's data bus, D[0] thru D[7]. U10's 3-state outputs to the data bus return to a high-impedance state when its enable input (U10 pin 1) returns high.

Table 4 – I/O Port Input Bits

U10 INPUT LABELING	MONITORED PARAMETER *
PRI/!SEC (U10 pin 2)	Primary/secondary card mode: 0 = secondary mode 1 = primary mode
CLOCKS_OK (U10 pin 3)	Clock monitor: 0 = one or more clocks has failed 1 = all selected clocks operating
CLK_SELA_!B (U10 pin 4)	Selected CEC/IMC clocks: 0 = B clocks selected 1 = A clocks selected
CARD_SEL (U10 pin 5)	Parallel I/O card select: 0 = not selected by parallel I/O 1 = selected by parallel I/O
none (U10 pin 6)	By adding/removing pull-down resistors, these bits are used to set a hardware revision number (in binary) which the processor can read.
none (U10 pin 7)	
none (U10 pin 8)	
none (U10 pin 9)	

* 0 = logic low; 1 = logic high

Microprocessor U1 writes to the eight output bits by writing a byte to address 40180H, the same address as the input port. A write to this address activates !I0_EN (U1 pin 29) and !WR (U1 pin 63). These two active-low logic lines are NORed by U8A and the resultant low-going pulse is applied to U9's latch enable input at pin 11. Consequently, the written data byte placed on D[0] thru D[7] by U1 latches at U9's outputs (pins 12 thru 19). Each output bit is defined in Table 5.

Table 5 – I/O Port Output Bits

U9 OUTPUT LABELING	CONTROLLED PARAMETER *
T1/!E1 (U9 pin 19)	T1/E1 mode select: 0 = E1 mode 1 = T1 mode
MASTER (U9 pin 18)	Stand-alone clock mode mstr/slave select: 0 = slave mode 1 = master mode
STAND_ ALONE (U9 pin 17)	Stand-alone clock mode enable/disable: 0 = disabled (uses Backplane clocks) 1 = enabled (uses clocks from on-card digital PLL circuit)
SYNCA_EN (U9 pin 16)	8KHZ_SYNCA clock line enable/disable: 0 = disabled 1 = enabled
SYNCB_EN (U9 pin 15)	8KHZ_SYNCB clock line enable/disable: 0 = disabled 1 = enabled
!LOS (U9 pin 14)	Controls SIGNAL ACTIVE indicator DS5: 0 = LED off 1 = LED on
FRAME_ SYNC (U9 pin 13)	Controls FRAME SYNC indicator DS6: 0 = LED off 1 = LED on
ID_LED_ON (U9 pin 12)	Controls ID indicator DS3: 0 = LED off 1 = LED on

* 0 = logic low; 1 = logic high

Status Indicators

The T1/E1 Interface Card is equipped with several LED (light-emitting diode) indicators on its front panel which display the status of various card operating conditions. See Table 6 for details.

MEMORY TIME SWITCHES

A group of Siemens PEB 2045 (or equivalent) CMOS memory time switch (MTSC) integrated circuits are utilized on the T1/E1 Interface Card to route PCM audio, subrate data, and embedded HSCX data as needed. These MTSC chips are basically 64 kbps channel exchanges. A number of two megabit buses (2.048 Mbps) are routed to and from each MTSC. Each two megabit bus contains

thirty-two (32), 64 kbps channels. The MTSC circuits can take any input channel/slot and route it to any output channel/slot. "Speech memory" within each MTSC chip stores incoming PCM audio or data during a frame and sends it out during the next frame. "Connection memory" stores input-to-output routing maps.

As shown in Figure 3, the MTSC chips establish channels between the T1/E1 framer and the TDM network, between the gate arrays and the T1/E1 framer, and between the gate arrays and the TDM network. Also, embedded HSCX support is provided by the channels between the HSCX controller (U33) and the TDM network, and between the HSCX controllers and the T1/E1 framer. The T1/E1 framer, not shown in the figure, is a part of the T1/E1 line interface which synchronizes signals to/from the T1/E1 line. The gate arrays provide the interfaces for the subrate ports.

The first stage of MTSC chips consists of U41 thru U47 [schematic diagram sheets 3 and 4]. As shown in Figure 3, these MTSC chips are designated MTSC 1 thru MTSC 7 respectively. All seven operate in a "primary access configuration" mode. In this mode, the each MTSC provides a 4 x 4 non-blocking switch. A primary access MTSC is broken into two interfaces, the system side and the synchronous side. The system sides of U41 thru U47 are used to interface to the CEC/IMC TDM network. The synchronous sides are used to interface to on-card peripherals including the HSCX controllers, the T1/E1 framer (via U48), and the gate arrays chips (U94 thru U99). The gate array chips interface the subrate ports to the MTSC chips. Refer to Table 7 for MTSC 1 thru 7 (U41 thru U47) I/O mapping.

The second stage consists of a single MTSC chip, U48 [schematic diagram sheet 4]. This MTSC, designated MTSC 8, operates in "standard configuration" mode to provide a unidirectional 16 x 8 switch – 16 inputs and 8 outputs; however, as shown in Figure 3, only ten (10) inputs and a single (1) output are utilized. U48's sole purpose is to consolidate traffic *to* the T1/E1 framer. Refer to Table 8 for MTSC 8 (U48) I/O mapping.

As shown in Figure 3 and Table 7, each MTSC in the first stage connects to four (4) TDM buses on its system side and each has access to on-card peripheral buses on its synchronous side. This provides each on-card peripheral (framer, HSCX controller, and gate arrays) connections to/from the four (4) backplane TDM buses interfaced by the particular MTSC. Therefore each peripheral may access any of the twenty-eight (28) TDM buses using MTSC 1 thru MTSC 7 (U41 thru U47 respectively). As shown in Figure 3 and Table 8, a single output from each first stage MTSC is applied to an MTSC 8 (U48) input so TDM bus data may be selectively transferred to the T1/E1 framer under microprocessor U1 control.

Table 6 – Status Indicators

LED	FRONT PANEL LABELING	SCHEMATIC DIAGRAM SHEET	FUNCTION
DS2	RUN	1	on = microprocessor is running (card not in reset)
DS3	ID	1	blinking = card ID (identify) has been enabled from CEC/IMC Manager (MOM PC) *
DS4	CLKS	4	on = all selected clocks are operational
DS5	SIG	6	on = a T1/E1 line signal is being received
DS6	SYNC	6	on = T1/E1 line frame sync is established
DS7	SEC	9	on = card in secondary mode
DS8	+5V	10	on = +5V power supply is present
DS9	+12V	10	on = +12V power supply is present
DS10	-12V	10	on = -12V power supply is present

* ID status indicator is also used to indicate proper board initialization at power-up.

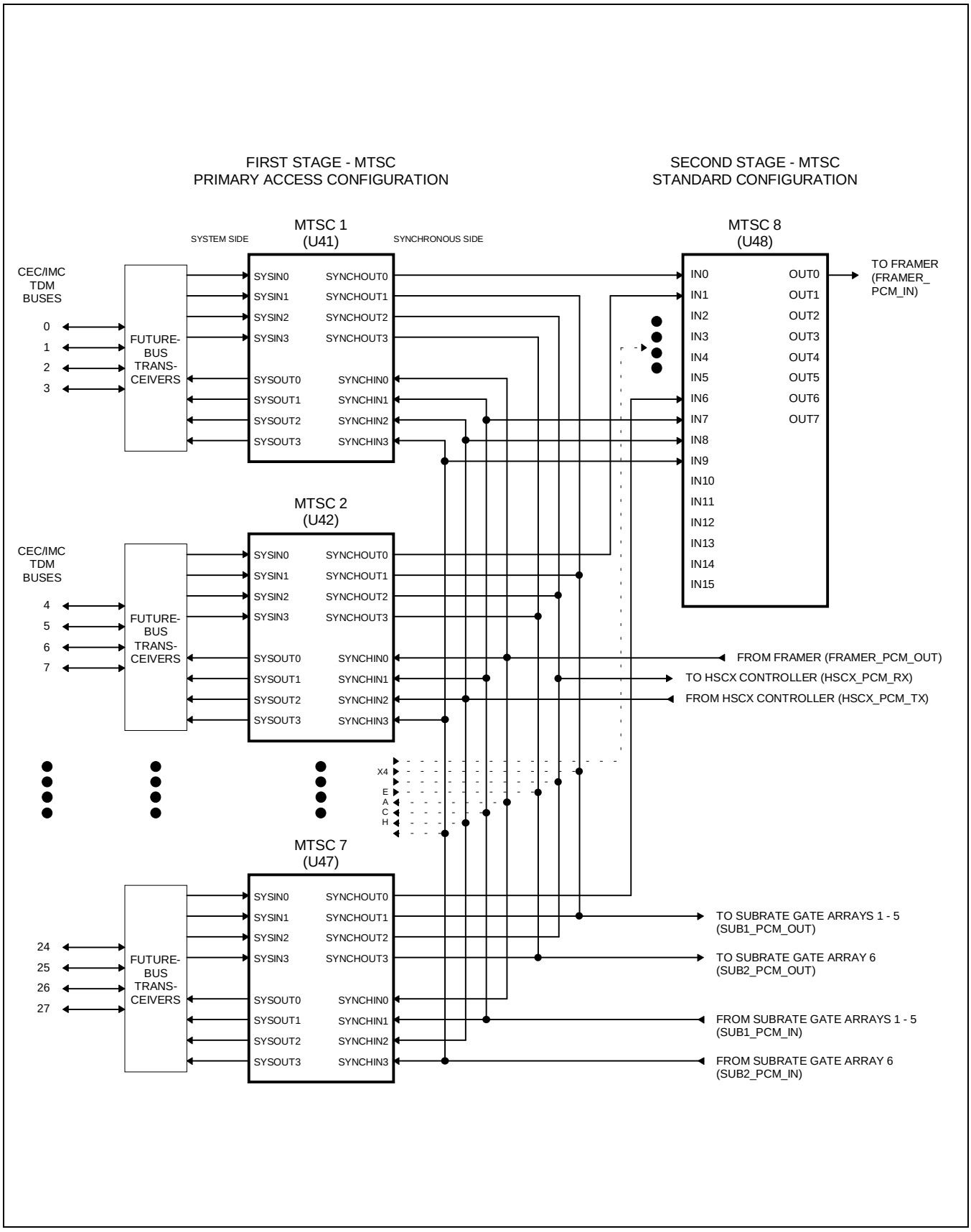


Figure 3 – Memory Time Switch (MTSC) I/O Paths

Table 7 – MTSC 1 Thru 7 I/O Mapping (First Stage)

MTSC SIDE	SCHEMATIC IC LABELING (Sheets 3 & 4)	MTSC CHIP						
		1 (U41)	2 (U42)	3 (U43)	4 (U44)	5 (U45)	6 (U46)	7 (U47)
System	SYSIN0	bus 0 in	bus 4 in	bus 8 in	bus 12 in	bus 16 in	bus 20 in	bus 24 in
System	SYSIN1	bus 1 in	bus 5 in	bus 9 in	bus 13 in	bus 17 in	bus 21 in	bus 25 in
System	SYSIN2	bus 2 in	bus 6 in	bus 10 in	bus 14 in	bus 18 in	bus 22 in	bus 26 in
System	SYSIN3	bus 3 in	bus 7 in	bus 11 in	bus 15 in	bus 19 in	bus 23 in	bus 27 in
System	SYSOUT0	bus 0 out	bus 4 out	bus 8 out	bus 12 out	bus 16 out	bus 20 out	bus 24 out
System	SYSOUT1	bus 1 out	bus 5 out	bus 9 out	bus 13 out	bus 17 out	bus 21 out	bus 25 out
System	SYSOUT2	bus 2 out	bus 6 out	bus 10 out	bus 14 out	bus 18 out	bus 22 out	bus 26 out
System	SYSOUT3	bus 3 out	bus 7 out	bus 11 out	bus 15 out	bus 19 out	bus 23 out	bus 27 out
Synchronous	SYNCHIN0	from framer	from framer	from framer	from framer	from framer	from framer	from framer
Synchronous	SYNCHIN1	from gate arrays 1 – 5	from gate arrays 1 – 5	from gate arrays 1 – 5	from gate arrays 1 – 5	from gate arrays 1 – 5	from gate arrays 1 – 5	from gate arrays 1 – 5
Synchronous	SYNCHIN2	from HSCX controller	from HSCX controller	from HSCX controller	from HSCX controller	from HSCX controller	from HSCX controller	from HSCX controller
Synchronous	SYNCHIN3	from gate array 6	from gate array 6	from gate array 6	from gate array 6	from gate array 6	from gate array 6	from gate array 6
Synchronous	SYNCHOUT0	to MTSC 8 (U48)	to MTSC 8 (U48)	to MTSC 8 (U48)	to MTSC 8 (U48)	to MTSC 8 (U48)	to MTSC 8 (U48)	to MTSC 8 (U48)
Synchronous	SYNCHOUT1	to gate arrays 1 – 5	to gate arrays 1 – 5	to gate arrays 1 – 5	to gate arrays 1 – 5	to gate arrays 1 – 5	to gate arrays 1 – 5	to gate arrays 1 – 5
Synchronous	SYNCHOUT2	to HSCX controller	to HSCX controller	to HSCX controller	to HSCX controller	to HSCX controller	to HSCX controller	to HSCX controller
Synchronous	SYNCHOUT3	to gate array 6	to gate array 6	to gate array 6	to gate array 6	to gate array 6	to gate array 6	to gate array 6

* Gate arrays 1 thru 5 = U94 thru U98 respectively. Gate array 6 = U99.

Table 8 – MTSC 8 I/O Mapping (Second Stage)

MTSC SIDE	SCHEMATIC U48 LABELING (Sheet 4)	SOURCE/DESTINATION OF SIGNAL
Input	IN0	from MTSC 1 (U41)
Input	IN1	from MTSC 2 (U42)
Input	IN2	from MTSC 3 (U43)
Input	IN3	from MTSC 4 (U44)
Input	IN4	from MTSC 5 (U45)
Input	IN5	from MTSC 6 (U46)
Input	IN6	from MTSC 7 (U47)
Input	IN7	from gate arrays 1 – 5 (U94 – U98)
Input	IN8	from HSCX controller (U33)
Input	IN9	from gate array 6 (U99)
Input	IN10	*
Input	IN11	*
Input	IN12	*
Input	IN13	*
Input	IN14	*
Input	IN15	*
Output	OUT0	to framer (FRAMER_PCM_IN)
Output	OUT1	*
Output	OUT2	*
Output	OUT3	*
Output	OUT4	*
Output	OUT5	*
Output	OUT6	*
Output	OUT7	*

* not used

In addition to TDM bus I/O on the MTSC system side, the first stage MTSC chips (U41 thru U47) provide transmit enables (!TE[0:27]) for the Futurebus drivers. These Futurebus drivers, located in the Futurebus transceiver chips, drive the CEC/IMC TDM buses on the Backplane. The enable lines are not indicated in Figure 3. Each enable line enables a driver when the respective MTSC system side output is valid and must be applied to the CEC/IMC TDM bus. Each system side output has a corresponding active-low transmit enable output. See the section entitled "**FUTUREBUS TRANSCEIVERS**", subsection "**TDM Bus Interfacing**" (page 20) for additional details.

For example, the BUS[0]_TX output from U41 pin 43 (SYSOUT0) [schematic diagram sheet 3] is applied to the input of a driver in U73 (at U73 pin 3) [schematic diagram

sheet 5]. The transmit enable line for bus 0 is !TE[0] from U41 pin 5. !TE[0] is applied to bus 0 driver enable input at U73 pin 17 (via inverter U78B). The driver's output is U73 pin 18, identified TDM_BUS[0]. It drives TDM bus 0 when !TE[0] is low. TDM_BUS[0] is applied to the CEC/IMC Backplane via 96-pin DIN connector J1 pin 9B [schematic diagram sheet 10].

MTSC Connection Examples

The following example connections through the MTSC chips are presented. Refer to Figure 3 and the schematic diagram as necessary [schematic diagram sheets 3 thru 5]:

- **Connect T1/E1 channel 1 (receive line) to CEC/IMC Backplane TDM bus 5, slot 3 –** Since MTSC 2 (U42) has physical access to TDM bus 5, U42 is utilized:

  Connect: synchronous side SYNCHIN0 at U42 pin 19 (from T1/E1 framer via FRAMER_PCM_OUT) during slot 1 (slot 1 = T1/E1 channel 1). Buffer in "speech memory" within MTSC 2 and send

  to: system side SYSOUT1 at U42 pin 41 (to TDM bus 5 transceiver U74 via BUS[5]_TX) during slot 3. During this connection, !TE(5) from U42 pin 8 will produce a low pulse for the TDM bus 5 driver in transceiver U74.

- **Connect TDM bus 13, slot 4 to T1/E1 channel 1 (transmit line) –** Since MTSC 4 (U44) has physical access to TDM bus 13, U44 is utilized:

  Connect: system side SYSIN1 at U44 pin 7 (from TDM bus 13 via BUS[13]_RX and Futurebus transceiver U73) during slot 4. Buffer in "speech memory" within MTSC 4 and send

  to: synchronous side SYNCHOUT0 at U44 pin 42 (to MTSC 8 via MTSC4_OUT) during slot 1 of the next frame (slot 1 = T1/E1 channel 1).

  MTSC 8 (U48) must also be involved in the connection to route the data to the T1/E1 framer (U85):

  Connect: IN3 at U48 pin 20 (from MTSC 4 via MTSC4_OUT) during slot 1

  to: OUT0 at U48 pin 43 (to T1/E1 framer via FRAMER_PCM_IN) during slot 1.

Microprocessor Interface

Each memory time switch is connected to the lower eight bits of the data bus, D[1] thru D7]. Via this bus, microprocessor U1 sends both configuration data and switch memory connection data to each MTSC chip.

All MTSC chips are located in microprocessor U1's address space selected by the active-low !MCS3 chip select line from U1 pin 35 [schematic diagram sheet 1]. All OR gates within U28 & U29 and inverters within U5 & U31 [schematic diagram sheet 2] gate !MCS3 with address lines A[4] thru A[11]. The resultant active-low !MTSC1_CS thru !MTSC8_CS chip selects are applied to MTSC 1 (U41) thru MTSC 8 (U48) respectively, at pin 22 of each MTSC chip.

Before application to the MTSC chips, the active-low read (!RD) and write (!WR) lines from microprocessor U1 are each gated with the active-low !RESET line via AND gates U12C and U12D [schematic diagram sheet 3]. This gating provides a hardware reset to all MTSC chips by simultaneously pulling the read and write inputs of each MTSC low during a card reset (when !RESET = low). The resultant gated active-low read (!RD_MTSC) and write (!WR_MTSC) lines are applied to MTSC chips U41 thru U48 at pins 24 and 25 of each MTSC chip [schematic diagram sheets 3 and 4].

Clock Inputs

The MTSC chips require two (2) system clock input signals. MTSC_FSYNC at pin 3 of each MTSC is an 8 kHz frame sync clock derived from the selected frame sync clock source – either the CEC/IMC Clock Board A or B frame sync clock. 4096KHZ at pin 44 of each MTSC is a 4.096 MHz clock from a PLL circuit locked to the selected bit clock (2.048 MHz). Clock source selection is dependent upon current card clock operating mode. See the clock generation section of this manual for additional details [schematic diagram sheets 3 and 4].

Monostable multivibrator U11B provides a frame sync clock pulse to the all of the memory time switches [schematic diagram sheet 4]. The falling-edge of the selected FSYNC clock pulses triggers U11B's active-low trigger input (U11 pin 9) every 125 microseconds (8 kHz). The monostable's output at U11 pin 5 is set to approximately 110 nanoseconds by the RC network at pin 7. This active-high output pulse is applied to pin 3 of each MTSC chip via MTSC_FSYNC. Basically, this circuit supplies a slightly modified frame sync pulse to the MTSC chips.

FUTUREBUS TRANSCEIVERS

All TDM bus and clock lines on the CEC/IMC Backplane utilize IEEE-896 Futurebus-compatible logic lines. This interface defines a logic high state at (or near) +2 volts and a logic low state at (or near) +1 volt. On the Futurebus side, drivers within the Futurebus transceiver chips have open-collector outputs. Individual pull-up resistors on the CEC/IMC Terminator Boards pull each respective Futurebus line to an approximate +2-volt level when the line is high (driver off).

The primary purpose of the Futurebus transceivers is to perform Futurebus-to-TTL level conversions between the CEC/IMC Backplane and the TTL-level chips on the T1/E1 Interface Card. The transceivers used for TDM bus interfacing also split the Backplane TDM buses into separate receive (RX) and transmit (TX) TDM bus lines on the T1/E1 Interface Card. These separated buses operate at TTL levels.

TDM Bus Interfacing

Integrated circuits U50 and U70 thru U75 are National Semiconductor DS3897M (or equivalent) quad Futurebus transceivers – four (4) transceivers are in each IC package [schematic diagram sheets 4 and 5]. These transceivers interface the Futurebus-level TDM buses on the CEC/IMC Backplane to the T1/E1 Interface Card's MTSC chips. The MTSC chips operate at TTL levels.

On the Futurebus transceiver's Backplane-side, bus lines TDM_BUS[0] thru TDM_BUS[27] correspond to TDM buses 0 thru 27 on the CEC/IMC Backplane. Connections are made via 96-pin DIN connectors J1 and J2 at the rear of the card [schematic diagram sheet 10].

NOTE

CEC/IMC Audio Boards utilize buses 0 thru 7 only. Initial T1/E1 Interface Card firmware/software will comply with this temporary limitation.

TTL-level TDM bus signals are transferred *from* the MTSC chips *to* the Futurebus transceivers' drivers via the BUS[0]_TX thru BUS[27]_TX bus lines. Likewise, TTL-level TDM bus signals are transferred *from* the Futurebus transceivers *to* the MTSC chips via the BUS[0]_RX thru BUS[27]_RX lines. Each RX line is equipped with a small low-pass RC network between the transceiver and the MTSC chip's input [schematic diagram sheets 3, 4 and 5].

Transmit/receive mode of each individual transceiver is controlled by the active-low transmit-enable outputs from the MTSC chips. These enables are identified !TE[0] thru !TE[27]. A transceiver drives its TDM Futurebus line when the respective !TE[x] enable is low and its logic input is high. These active-low transmit-enable outputs are inverted before application to the transceivers' active-high transmit-enable inputs.

For example, when !TE[3] from U41 pin 12 is low [schematic diagram sheet 3], the transceiver within U70 for bus 3 [schematic diagram sheet 5] drives TDM_BUS[3] (U70 pin 13 and J1 pin 15B) at the inverse BUS_TX[3] logic state. Inverter U76D inverts the !TE[3] transmit-enable [schematic diagram sheet 5].

A master Futurebus driver enable/disable control line, !FBUS_EN from data flip-flop U51A [schematic diagram sheet 4], is applied to the master transmit-enable input at each TDM Futurebus transceiver (pin 10 at U50 and U70 thru U75). When !FBUS_EN is high, all drivers within the TDM Futurebus transceivers are disabled. The drivers are disabled at power-up and they remain disabled until an enable command is received via a parallel I/O control sequence from the Controller Board.

Flip-flop U51A controls the state of !FBUS_EN via its active-low output at U51A pin 6. LD[0] and CF[6] from parallel I/O data latches U113 and U114 [schematic diagram sheet 9] provide the data and clock inputs to the flip-flop at U51A pins 2 and 3 respectively. The interface module's active Controller Board has direct control of LD[0] and CF[6] via the parallel I/O control connections between it and the T1/E1 Interface Card. See the section entitled "**PARALLEL I/O CONTROL**" (page 33) for complete details on the parallel I/O control lines and specific parallel I/O control sequences.

If the T1/E1 Interface Card enters a secondary or reset state (PRI/!SEC from U111B = low or !RESET from U120D = low), AND gate U65A drives U51A's clear input low. As a result, !FBUS_EN transitions high and all TDM bus-related Futurebus transceivers' drivers are disabled. This prevents the card from interfering with the Backplane's TDM buses when it is in a secondary or a reset state. Also, the !RESET input to the AND gate insures the flip-flop initializes correctly at power-up so the drivers are disabled.

During card testing, the transceivers' drivers may be manually enabled by setting DIP switch SW1 position 3 "CLOSED" or "ON". This setting pulls the flip-flop's active-low preset input low via the !FBUS_DRV_EN line from the DIP switch [schematic diagram sheets 1 and 4]. Thus, as long as the card is in primary mode (PRI/!SEC = high) and not reset (!RESET = high), !FBUS_EN is in its active state – logic low – and the drivers are master enabled. This control (manual enabling) should only be exercised during troubleshooting procedures.

Clock Inputs

Clock pulses on the CEC/IMC Backplane generated by the Clock Board are applied to Futurebus transceiver U60 via 96-pin DIN connectors J1 and J2 [schematic diagram sheets 4 and 10]. Transceiver U60 is a National Semiconductor DS3896M (or equivalent) octal Futurebus transceiver hard-wired for receive mode operation only; its transmit/receive control input ($T/\overline{R}$) at U60 pin 11 is tied to ground. The B-side pins (driver outputs/receiver inputs) are the Futurebus-level clock inputs from the Backplane. Pull-up resistors R158 thru R165, located on the TTL-level side (output) of U60, insure these clock pulses drive the CMOS inputs of U53 and U54 properly.

See the section entitled "**CLOCK SELECTION AND GENERATION**" for additional details on the clocks and the clock selection circuitry following U60.

Clock Outputs

Transceiver U87 is a quad Futurebus transceiver identical to the transceivers used for TDM bus interfacing. Only the driver portion of two (2) transceivers in this chip are utilized [schematic diagram sheet 6].

The 8 kHz reference clock pulses from framer U85 pin 7 (8KHZ_REF) feed inverter U15C. This inverter's output clocks both drivers' inputs – U87 pins 1 and 3. When enabled by an active-low !PRIMARY from data flip-flop U111B [schematic diagram sheet 9] *and* an active-high SYNCx_EN line (x = A or B) from octal latch U9 [schematic diagram sheet 1], each Futurebus driver clocks its respective 8KHZ_SYNCx Futurebus output to the CEC/IMC Backplane. The 8KHZ_SYNCA clock is applied to the Backplane via 96-pin DIN connector J2 (bottom DIN connector) pin 4A and the redundant 8KHZ_SYNCB clock is applied to the Backplane via J1 (top DIN connector) pin 27B [schematic diagram sheet 10]. Additional details on this circuitry are contained the section entitled "**T1/E1 LINE FRAMER AND LINE INTERFACE**" (page 25).

CLOCK SELECTION AND GENERATION

To provide redundant clocking for the TDM bus and T1/E1 circuits, the CEC/IMC is equipped two (2) identical but completely separate clock circuits. These redundant system clocks, generated by the CEC/IMC Clock Board(s), are identified “A” and “B” throughout the system. Clock A/B selection is dictated by the CEC/IMC MOM Controller Board in accordance with clock A/B fail messages received from other CEC/IMC interface modules (MIM, CIM, NIM, LRIM, etc.) The initial start-up or default clock is B.

For example, if the CEC/IMC is operating off the B clock circuits and one or more of the B clock pulses on the Backplane fail, the MOM Controller Board will receive clock B fail messages from most or all CEC/IMC interface modules within the CEC/IMC. The MOM Controller Board will then command all CEC/IMC interface modules to switch to the A clock circuit by sending an A clock-select message to all other Controller Boards in the CEC/IMC. Each Controller Board then switches its Audio Board(s) or its T1/E1 Interface Card(s) to the A clock circuits via parallel I/O control connections. Refer to LBI-38938 for additional information.

Redundant clocks originating from a CEC/IMC Clock Board and utilized by the T1/E1 Interface Card include the 8 kHz frame sync clock (FSYNCA and FSYNCB), the 2.048 MHz bit clock (BIT_CLKA and BIT_CLKB), and the 1.544 MHz T1 clock (1544A and 1544B). Two (2) other system clocks *not* utilized by the T1/E1 Interface Card but required by the CEC/IMC Audio Boards include a 256 kHz slot sync clock and a 2174/2175 Hz function tone clock. The 1.544 MHz clock is not used by the Audio Boards but it is required for T1 operation. All clocks are transferred over the Backplane at Futurebus levels. Table 9 summarizes clock usage by the T1/E1 Interface Card and an Audio Board.

Table 9 – Clock Utilization (System Clock Mode)

FREQ. FROM CLOCK BOARD	CLOCK LINE NAME *	USED BY T1/E1 INTERFACE CARD	USED BY AUDIO BOARD
8 kHz	FSYNCx	yes **	yes
2.048 MHz	BIT_CLKx	yes **	yes
1.544 MHz	1544x	yes **	no
256 kHz	SSYNCx	no	yes
2174/2175 Hz	2175x	no	yes

* x = A or B

** No Clock Board clock outputs are used by a T1/E1 Interface Card in stand-alone clock mode.

The T1/E1 Interface Card also has an on-card digital phase-locked loop (DPLL) circuit which generates all necessary clocks. These clocks are used only in a special mode referred to as "stand-alone clock mode" or simply "stand-alone mode". In this mode, the T1/E1 Interface Card *may not be* installed into a CEC/IMC; therefore, no clocks from a Clock Board (A or B) are available. See Figure 4. No software currently exists to support this feature.

System Clock Mode & Selection Circuits

In system clock mode, clocks generated at a Clock Board are utilized for synchronization of the T1/E1

Interface Card's TDM bus and T1/E1 line circuits. All A and B clocks are extracted from the CEC/IMC Backplane via Futurebus transceiver U60 [schematic diagram sheet 4]. This transceiver is hard-wired for receive operation only; its transmit/receive control input ($T/\overline{R}$) at U60 pin 11 is tied to ground.

Clocks from the Backplane (Futurebus levels) are applied to transceiver U60 at pins 12 thru 15 and 17 thru 19. The A clocks enter the T1/E1 Interface Card via 96-pin DIN connector J2 (bottom connector) and the B clocks enter via J1 (top connector) [schematic diagram sheet 10]. Receivers within transceiver U60 convert these Futurebus-level clocks to TTL-level clocks. TTL-level outputs from U60 pins 3, 4 and 6 thru 9 are applied to a clock selector circuit formed by dual 4-input multiplexers U53 and U54 (U53A, U53B and U54A).

Basically, each multiplexer section operates like a single-pole four-position switch controlled by the CLK_SELA_!B and STAND_ALONE logic lines applied to the A0 and A1 multiplexer inputs. These multiplexers not only select between the A or B clocks from the Backplane, but they are also used to select clocks from the on-card digital PLL circuit when the T1/E1 Interface Card is in stand-alone clock mode. Only one clock source is selected at a time – either the A or the B or the digital PLL stand-alone clocks depending upon the current clock mode. The digital PLL stand-alone clock circuits are discussed in greater detail in the following section. Multiplexer U53A, U53B and U54A output 8 kHz (FSYNC), 2048 kHz (2048KHZ) and 1544 kHz (1544KHZ) selected clocks respectively.

A, B and digital PLL clocks are applied to the selector circuit at the D0 thru D3 inputs of the multiplexers. The selected clock is sent out from the multiplexer's Y output (pin 7 or pin 9).

CLK_SELA_!B and STAND_ALONE are applied to the multiplexers' select control inputs at pins 14 and 2 respectively. Table 10 maps clock selection for the three (3) possible modes – A, B or stand-alone.

The CLK_SELA_!B logic line originates from the $\overline{Q}$ output of data flip-flop U115B (U115 pin 8) [schematic diagram sheet 9]. At card power-up or reset, !RESET sets CLK_SELA_!B low by pulsing the flip-flop's active-low preset input at U115 pin 10; thus, assuming the card is *not* in stand-alone clock mode (STAND_ALONE must = low), the B clocks are selected immediately after a card power-up or reset. See Table 10. After coming out of the reset condition, the T1/E1 Interface Card sends a message to its Controller Board over the HDLC link to communicate the foregoing reset.

Next, the interface module's active Controller Board uses the parallel I/O control connections to select (load) the system clock currently in use by the CEC/IMC – either A or B. This also occurs if/when the Controller Board receives a new clock-select message from the MOM Controller Board. This parallel I/O control is accomplished using octal data latches U112 thru U114, 4-bit card address comparator U110, etc., in the parallel I/O control interface circuits, and data flip-flop U115B [schematic diagram sheet 9].

For example, if the A clock is the current system clock after a T1/E1 Interface Card reset, the Controller Board will first set the LD[0] line from U113 pin 12 low. LD[0] is applied to the data input of flip-flop U115B. Next, the Controller Board pulses the clock select enable line – CLK_SEL_EN from U112 pin 15. This action sets U115B's output at pin 8 high. Thus, multiplexers U53 and U54 switch to and select the A clocks (assuming STAND_ALONE is low). See the section entitled "**PARALLEL I/O CONTROL**" (page 33) for additional details.

Table 10 – Clock Selection

	CONTROL INPUTS		MULTIPLEXERS' OUTPUTS (SELECTED CLOCK SOURCE)		
CLOCK MODE	CLK_SELA_!B LOGIC STATE *	STAND_ALONE LOGIC STATE *	FSYNC (U53A pin 7)	2048KHZ (U53B pin 9)	1544KHZ (U54A pin 7)
A clocks	1	0	FSYNCA **	BIT_CLKA **	1544A **
B clocks	0	0	FSYNCB **	BIT_CLKB **	1544B **
stand-alone	0 or 1	1	DPLL_8K ***	DPLL_2M ***	DPLL_15M ***

* 0 = logic low; 1 = logic high.
** Clock from Backplane via Futurebus transceiver U60.
*** Clock from on-card digital PLL.

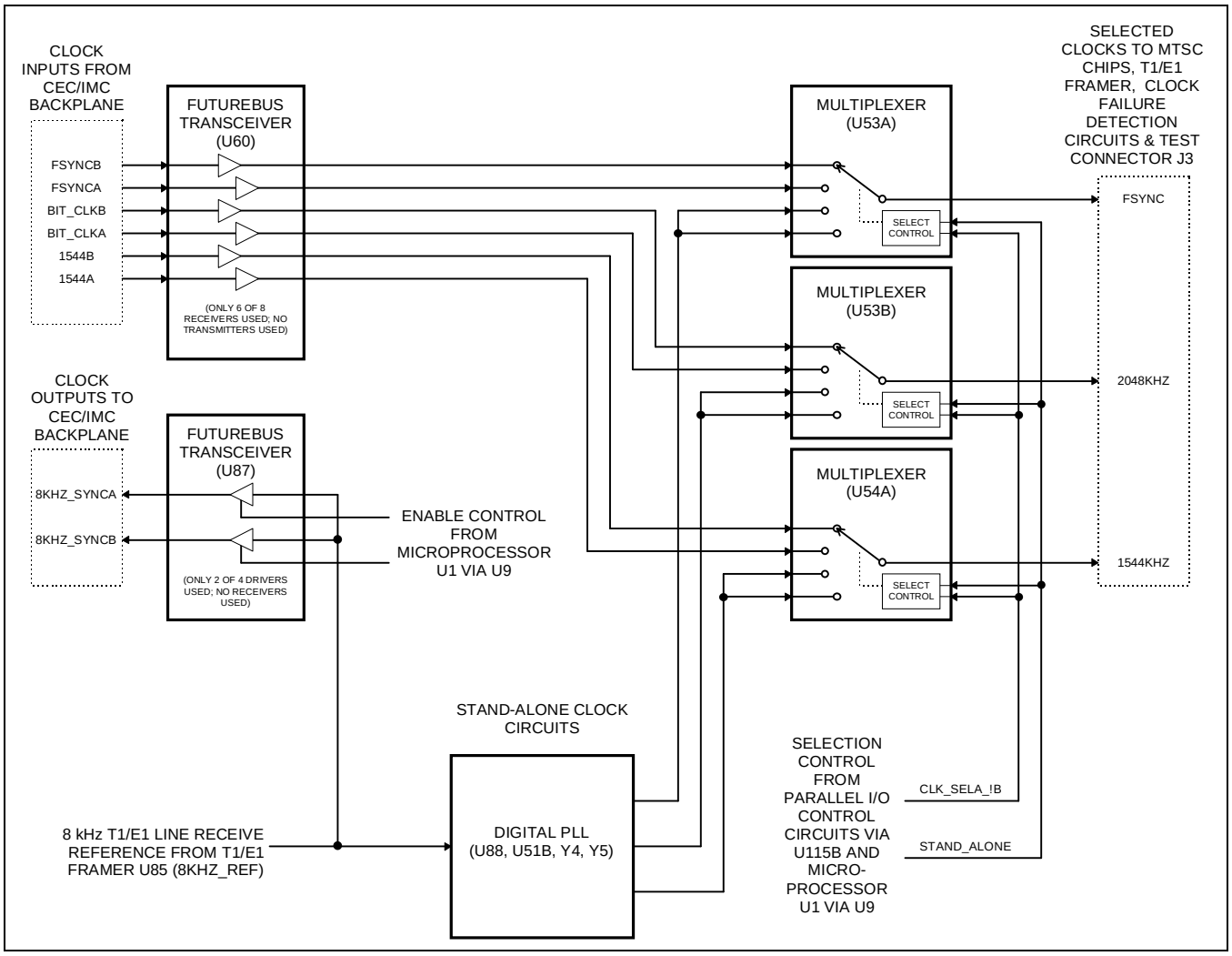


Figure 4 – Clock Selection Circuits

Stand-Alone Clock Mode

In stand-alone clock mode, the T1/E1 Interface Card operates from clocks generated by its on-card digital phase-lock loop (DPLL) circuit. This mode, not supported in initial T1/E1 Interface Card firmware/software release(s), is enabled when the STAND_ALONE logic line from U9 pin 17 is high. U9 is the octal latch within the microprocessor's I/O port output circuit [schematic diagram sheet 1]. As previously described, STAND_ALONE is applied to select control inputs of multiplexers U53 and U54 [schematic diagram sheet 4].

The stand-alone clock mode has two sub-modes - master and slave. In master mode, clocks from the DPLL circuit *are not* are synchronized to any external clocks; the digital PLL's outputs are phase-locked to two on-card crystal reference oscillators. In slave mode, clock outputs from the DPLL circuit are synced to the 8 kHz signal extracted by the T1/E1 framer; therefore, the T1/E1 Interface Card's clocks *are* slaved to an external signal. Master mode is enable when MASTER from U9 pin 18 is high. Slave mode is enable when MASTER is low [schematic diagram sheet 1].

Clock Generation

The DPLL circuit is formed by DPLL integrated circuit U88 – the heart of the circuit, crystal oscillators Y4 and Y5, and data flip-flop U51B [schematic diagram sheet 6]. This circuit generates the synchronized 8 kHz, 2.048 MHz and 1.544 MHz clocks for the T1/E1 Interface Card when it is operating in stand-alone clock mode. Clocks from the circuit appear on the lines labeled DPLL_8K, DPLL_2M and DPLL_15M respectively. These outputs are applied to the clock selection circuitry – multiplexers U53 and U54 [schematic diagram sheet 4].

Integrated circuit U88 is a Mitel MT8941 (or equivalent) digital trunk PLL chip. It contains two (2)

digital phase-lock loops, output control logic and mode selection logic circuits. Its 8 kHz, 2.048 MHz and 1.544 MHz clock outputs are located at U88 pins 8, 17 and 24 respectively. All three (3) outputs pass thru low-pass RC filters prior to application to multiplexers U53 and U54 and data flip-flop U51B. A 4.096 MHz output from U88 pin 13 (DPLL_4M) is not used.

To ensure proper 8 kHz frame synchronization with the 2.048 MHz bit clock, the 8 kHz output is first routed through data flip-flop U51B before application to the clock selector circuit. It is applied to the data input of the flip-flop (U51B pin 12). The 2.048 MHz bit clocks clock the flip-flop (at U51B pin 11) on the rising edges.

Inputs to U88 include two (2) reference signals from crystal oscillators Y4 and Y5, an 8 kHz reference signal from the T1/E1 framer (8KHZ_REF) which is extracted from the receive line, the master/slave select logic line (MASTER), and the card reset logic line (!RESET). Also, the filtered 8 kHz output from U88 pin 8 is fed-back to a frame pulse input at U88 pin 7 for 1.544 MHz clock generation.

TTL oscillators Y4 and Y5 supply 12.352 MHz and 16.384 MHz crystal reference frequencies to U88 at pins 3 and 10 respectively. The 12.352 MHz crystal reference drives the reference input of the first DPLL within U88 and the 16.384 MHz crystal reference drives the reference input of the second DPLL. When the T1/E1 Interface Card is in slave mode (MASTER = low), DPLL "speed-up" and "slow-down" logic signals are generated within U88 to ensure its clock outputs remain synchronized to the 8 kHz clock reference received from T1/E1 framer U85 (U85 pin 7). This clock reference is labeled 8KHZ_REF.

Four additional U88 inputs include MS0 thru MS3 at pins 2, 6, 9 and 20. These logic inputs set U88's operating mode. Since three of the four are hard-wired high or low, the MASTER line from U9 pin 18 [schematic diagram sheet 1] selects one of two possible modes – master or slave. As previously stated, when MASTER is low, the T1/E1 Interface Card is in the slave clock mode and U88 syncs to the 8 kHz clock reference received from the T1/E1 framer. When the T1/E1 Interface Card is operating in master mode (MASTER = high) its stand-alone clocks (the DPLL's outputs) are considered free-running since the T1/E1 Interface Card does not lock its clocks to an external source. The DPLL's outputs are, however, phase-locked to crystal reference oscillators Y4 and Y5.

4 MHz Clock

All MTSC chips and the T1/E1 framer circuit require a 4.096 MHz clock phase-locked to the 2.048 MHz bit clock. Phase-lock loop U58 and flip-flop U59 generate this 4 MHz clock (4096KHZ) from the selected 2 MHz bit clocks [schematic diagram sheet 4].

Bit clocks from the output of the clock selector circuit at U53B pin 9 (2048KHZ) are applied to one input of U58's phase comparator, U58 pin 14. This is U58's reference frequency input. The free-running frequency of the voltage-controlled oscillator (VCO) within U58 is set by C39 and R184 and the loop filter is formed by R182, R183, C38 and C40. Flip-flop U59A provides a divide-by two function between the output of the VCO at U58 pin 4 and the phase comparator's other input at U58 pin 3. The VCO's output drives the 4.096 MHz line – 4096KHZ – via R173. This clock is routed to pin 44 of each MTSC chip (U41 thru U48), to T1/E1 framer chip (U85 pin 28), and to an input of the clock failure detection circuit (U56A pin 2) [schematic diagram sheets 3, 4 and 6]. For monitoring purposes, 4096KHZ is also applied to test connector J3 at pin 39. The 4096KHZ clock is not generated on the Clock Board so propagation effects such as delay and noise do not limit system size. In addition, the 4.096 MHz clock from DPLL U88 (DPLL_4M) is not used to simplify clock selection circuitry.

Clock Failure Detection

Like a CEC/IMC Audio Board, the T1/E1 Interface Card is equipped with clock failure detection circuitry. This circuitry constantly monitors all selected clocks used by the T1/E1 Interface Card and if a failure occurs, it signals microprocessor U1 via an I/O port input bit. Microprocessor U1 then signals the interface module's Controller Board via the HDLC serial link. Next, the Controller Board then sends a clock failure message to the MOM Controller Board via the GSC bus. If the MOM Controller Board receives clock failure messages from three (3) or more Controller Boards within the CEC/IMC, it will issue a clock change by sending a new clock-select message to all Controller Boards within the CEC/IMC via the GSC bus.

The clock failure detection circuit is formed by dual retriggerable monostable multivibrators U55 and U56, and an AND gate within U57 [schematic diagram sheet 4]. During normal operation each of the selected clocks (FSYNC, 2048KHZ and 1544KHZ) and the phase-locked 4 MHz clock (4096KHZ) constantly retrigger their respective monostable. Therefore, all monostable Q outputs remain high and the CLOCKS_OK output from 4-input AND gate U57A pin 6 remains high. With CLOCKS_OK high, transistor Q5 turns LED DS4 on. This LED, mounted on the T1/E1 Interface Card's front panel, is labeled "CLKS". Microprocessor U1 regularly samples the state of CLOCKS_OK via the I/O input port bit at U10 in 3.

If any clock fails, its respective monostable times-out (Q output transitions low) and consequently, CLOCKS_OK transitions low. A low CLOCKS_OK signals microprocessor U1 of a failed clock. DS4 also turns off. For example, if the 1.544 MHz clock fails, 1544KHZ would no longer trigger U55A at pin 2. As a result, U55A pin 13 and CLOCKS_OK transition low and DS4 turns off.

T1/E1 LINE FRAMER AND LINE INTERFACE

The T1/E1 Interface Card's T1/E1-compatible line interface circuitry is primarily formed by integrated circuits U85, a Siemems PEB 2035 (or equivalent) Advanced CMOS Frame Aligner (ACFA) chip and U86, a Siemems PEB 2236 (or equivalent) ISDN Primary Access Transceiver (IPAT®-2) chip. For subsequent discussions in this manual, U85 will be referred to as the "framer" chip or "framer U85" and U86 will be referred to as the "line interface" chip or "line interface U86". Support circuitry includes several logic gates, surge suppression diodes, and the card's microprocessor and clock circuits [schematic diagram sheet 6].

Refer to the specifications listed near the beginning of this manual for frame formats, line codes, and line/channel signalling types supported over the T1/E1 link. Configuration is accomplished via the CEC/IMC Manager's (MOM PC's) "T1/E1 Node Configuration" screen. Microprocessor U1 programs selected user configuration into U85 and U86.

Framer U85

Basically, framer U85 provides an interface between a two megabit-per-second TDM bus and a T1 or E1 formatted data stream by adding or extracting the required T1 or E1 framing and line codes. The following subsections describe framer U85's microprocessor interface, MTSC interface and reset logic. The U85-to-U86 interface is discussed in the "**Line Interface U86**" section (page 26).

Microprocessor Interface

T1/E1 framer U85 interfaces to microprocessor U1 by the lower eight (8) bits of the data bus, four (4) address lines, the active-low read and write lines, an active-low chip-select line and two (2) interrupt lines. Using this interface, U1 programs configuration data into U85 by writing to control registers within it. In addition, via this interface, U1 sends and receives channel signalling data to/from U85. Channel signalling data is written to and read from signalling stacks within U85 [schematic diagram sheets 1 and 6].

The microprocessor interface also gives U1 the ability to read status registers within U85 to determine vital T1/E1 link status information. For example, U1 reads a status register within U85 to determine if a T1/E1 signal is being received. If so, among other actions, U1 turns "SIGNAL ACTIVE" LED DS5 on. This is accomplished using an output bit from U9 pin 14 (!LOS), and transistor Q6. DS5 is labeled "SIG" on the front panel.

A U85 status register also indicates to U1 if a valid T1/E1 receive framing sequence is detected. If so, among other actions, U1 turns "FRAME SYNC" LED DS6 on via another output bit from U9 (U9 pin 13; FRAME_SYNC) and transistor Q7. DS6 is labeled "SYNC" on the front panel.

Address lines A[1] thru A[4] from U1 (via address latch U2) are connected to U85's A0 thru A3 address inputs at U85 pins 18 thru 21 respectively. During a U1 read or write, microprocessor U1 uses these address lines to select which control register, status register or signalling stack will be read from or written to. Reads of U85 occur when U85 is chip selected by U1 and the active-low !RD line is low (U85 pin 22). Writes occur when U85 is chip selected by U1 and the active-low !WR line is low (U85 pin 25). Chip selection is furnished by the active-low !MCS2 line from U1 pin 36. !MCS2 is applied to U85's active-low chip-select input at U85 pin 26.

Framer U85 interrupt outputs to microprocessor U1 include ACFA_INT from U85 pin 5 and XREQ_INT from U85 pin 40. Both interrupts are active when high.

ACFA_INT, applied to U1 pin 42, signals U1 on T1/E1 line status changes such as loss of receiver frame sync. When interrupted by ACFA_INT, U1 reads U85 status registers and it acts accordingly. This action may include signalling the Controller Board of the status change and as previously described, turning LEDs DS5 and DS6 on or off.

XREQ_INT, applied to U1 pin 45, is used during channel signalling to inform U1 of empty U85 signalling stacks. Upon an active XREQ_INT, U1 must send additional signalling information to U85. Framer U85 will then automatically insert the new signalling information onto the T1/E1 data stream.

MTSC Interface

Two megabit-per-second audio/data signals are routed between MTSC chips U41 thru U48 and framer U85 via FRAMER_PCM_OUT and FRAMER_PCM_IN. The framer accesses the CEC/IMC TDM network using these connections and the MTSC chips [schematic diagram sheets 3, 4 and 6].

FRAMER_PCM_OUT at U85 pin 4 is U85's output to the MTSC chips. It is T1/E1 channel data from the T1/E1 receive line (via U86) less framing which U85 extracts. Correspondingly, FRAMER_PCM_IN at U85 pin 34 is U85's input from the MTSC chips. This unframed T1/E1 channel data is applied to U85 for framing and then routed to the T1/E1 transmit line via line interface U86. Refer to the section entitled "**MEMORY TIME SWITCHES**" (page 14) for MTSC chip circuit analysis details.

Reset Logic

At card power-up or reset, U85 is reset by the !RESET pulse applied to its active-low reset input at U85 pin 35. Upon being reset U85 initializes itself to a default configuration. Microprocessor U1 then loads configuration data into U85 after the current database is received from the interface module's (MIM, NIM, etc.) Controller Board. This database is configured via the CEC/IMC Manager.

Line Interface U86

Basically, line interface U86 interfaces framer U85 to T1/E1 line coupling transformers located on the T1/E1 Concentrator Card. The framer-side of U86 employs three (3) dual-rail connections and two (2) TTL-level clock connections. The T1/E1 line-side of U86 is considered the "ternary interface" since T1/E1 links transfer data signals via 3-level signals (+3V, 0V, -3V). The ternary interface consists of four (4) bipolar connections to/from transmit/receive line coupling transformers on the T1/E1 Concentrator Card plus a dc voltage reference connection for the receive coupling transformer. Since each T1/E1 Concentrator Card supports two (2) T1/E1 Interface Cards, each Concentrator Card has two transmit line coupling transformers and two receive line coupling transformers.

Framer Connections (U85-to-U86 Interface)

As previously stated, line interface U86 is connected to framer U85 by three dual-rail connections; each signal between the two chips has a positive and a negative connection. Dual-rail signals include a transmit data input from the framer, a transmit test data input from the framer, and a receiver output to the framer. The transmit test data input is not used during normal T1/E1 Interface Card operations [schematic diagram sheet 6].

The dual-rail transmit data input from the framer is located at U86 pins 19 (XDIN; negative) and 20 (XDIP; positive). Data on this input is clocked into U85 via the TTL-level transmit clock applied to U86 pin 21 (XCLK) from NOR gate U30D in the T1/E1 mode clock select circuitry. In T1 mode this transmit clock input is clocked at 1.544 MHz and in E1 mode it is clocked at 2.048 MHz. T1/E1 mode clock select circuitry is described later.

The dual-rail receive data output to the framer is located a U86 pins 25 (RDOP; positive) and 26 (RDON; negative). Synchronous clocking to the framer's receiver is furnished by TTL-level receive clock output (RCLK) from U86 pin 27. Timing control logic within framer U85 also uses this clock signal to generate the 8 kHz reference clock output, 8KHZ_REF from U85 pin 7. This 8 kHz reference clock is applied to the DPLL chip U88. It is also applied to the Backplane via U15C and U87 if an external slave clock is enable via the CEC/IMC Manager. This allows the CEC/IMC Clock Board(s) to sync to the T1/E1 receive line.

T1/E1 Line Interface

T1/E1 line connections between U86 and the line coupling transformers on the T1/E1 Concentrator Card are provided by four (4) bipolar connections identified XL1, XL2, RL1 and RL2. XL1 and XL2 are the ternary transmit connections to the transmit line coupling transformer. RL1 and RL2 are the ternary receive connections from the receive line coupling transformer.

XL1, XL2, RL1 and RL2 are routed out of and in to the card via 96-in DIN connector J2 (bottom DIN connector) pins 9B, 7B, 10B and 11B respectively. Surge suppression is provided by diodes D1 thru D6 [schematic diagram sheet 6].

U86 pin 3 outputs a 2.5 dc voltage reference, VDD2, for the receive line coupling transformer's center tap. Decoupling is provided by C83 and C84. VDD2 is routed out of the T1/E1 Interface Card via 96-pin DIN connector J2 pin 6B. J2 is the bottom DIN connector.

Microprocessor Interface

Microprocessor U1 writes to line interface chip U86 using the five (5) lowest bits of the data bus, D[0] thru D[4] and an active-low chip-select line, !PRACT_EN from U1 pin 28. !PRACT_EN is applied to U86 at pin 24. U86 accepts D[0] thru D[4] data when !PRACT transitions low. U1 cannot read U86.

For T1 applications, U1 writes line length settings to U86's line select inputs – LS0 thru LS2 at U86 pins 8 thru 10 respectively. This 3-bit selection basically sets the transmit pulse shape sent out by U86 onto the T1 line (XL1 and XL2). Any written value other than zero (binary 000) will select a specific T1 line length (capacitance) per AT&T specifications.

E1 applications do not support selectable line lengths. U1 sets U86 for E1 operation by writing all zeros (binary 000) to the line select inputs.

Local/remote loop-back inputs at U86 pins 5 and 15 are used just after a card power-up or reset to initialize U86 correctly. They are not used during normal T1/E1 Interface

Card operations. In later software/firmware releases, these inputs will be used for diagnostic purposes.

T1/E1 Mode Clock Switching

During T1 operation, a 1.544 MHz clock must be applied to the transmit clock inputs of U85 and U86 (U85 pin 33 and U86 pin 21 respectively). During E1 operation, a 2.048 MHz clock sync output from the framer (U85 pin 41) must be applied to the U86's transmit clock input. This T1/E1 mode clock switching is provided by AND gates U65B and U84A, OR gate U30D, inverter U15B and the T1/!E1 mode select line controlled by microprocessor U1 [schematic diagram sheet 6].

When in T1 mode, U1 pulls T1/!E1 high via the I/O port output bit at U9 pin 19 [schematic diagram sheet 1]. This action gates the 1.544 MHz clock (1544KHZ) through U65B to U85 pin 33. In addition, AND gate U84A pin 3 is low and thus the 1.544 MHz clock is gated through NOR gate U30D to U86 pin 21.

When in E1 mode, U1 pulls T1/!E1 low via U9 pin 19. This T1/!E1 logic level causes U65B to hold U85 pin 33 low. Also, the 2.048 MHz clock from U85 pin 41 is gated through AND gate U84A to OR gate U30D pin 13. Since U65B pin 6 is low, U30D passes the 2.048 MHz clock to U86 pin 21.

8 kHz Reference Clock Output

Framer U85 provides 8 kHz reference clock pulses which are synchronized to the data stream received on the T1/E1 line. This framer output, 8KHZ_REF from U85 pin 7, is applied to DPLL chip U88 within the on-card clock generator (stand-alone) circuit and to Futurebus transceiver U87 via inverter U15C. When in sync, 8KHZ_REF contains low-going 0.5 microsecond (approximate) pulses spaced at the 8 kHz rate. During loss of T1/E1 line sync U85 suppresses 8KHZ_REF pulses [schematic diagram sheet 6].

8 kHz Reference Clock To U88

When the T1/E1 Interface Card is in stand-alone mode and the slave sub-mode (STAND_ALONE = high and MASTER = low), U88 uses 8KHZ_REF to generate internal "speed-up" and slow-down" logic signals for its internal digital phase-lock loops. This guarantees all on-card generated clock pulses remain synchronized to the 8 kHz reference clock extracted from the T1/E1 receive data stream. See the section entitled "**CLOCK SELECTION AND GENERATION**", subsection "**Stand-Alone Clock Mode**" (page 23) for additional U88 details.

8 kHz Reference Clock To U87

As previously stated, 8KHZ_REF is also applied to Futurebus transceiver U87. Per CEC/IMC Manager (MOM PC) slave clock mode configuration, two (2) drivers within this transceiver can drive none, one or two Futurebus-level 8 kHz clock sync lines on the CEC/IMC Backplane – 8KHZ_SYNCA or 8KHZ_SYNCB. This allows the CEC/IMC Clock Board(s) to synchronize to a particular T1/E1 line connected to the CEC/IMC. Two separate sync lines are provided for redundancy. Driver enable/disable control is provided by microprocessor U1 via octal latch U9 in the I/O port output circuit. Outputs from U9 pins 15 (SYNCB_EN) and 16 (SYNCA_EN) are applied to U87's driver enable inputs at U87 pins 17 and 19 respectively. A driver drives its Futurebus line when the respective driver enable input is high. Also, the T1/E1 Interface Card must be in primary mode (!PRIMARY = low). See the section entitled "**FUTUREBUS TRANSCEIVERS**", subsection "**Clock Outputs**" (page 21) for additional U87 details.

Per system design and CEC/IMC Manager (MOM PC) configuration, each 8 kHz sync line on the Backplane can only be driven by one T1/E1 Interface Card. This configuration is set-up via the CEC/IMC Manager's "T1/E1 Node Configuration" screen.

For example, T1/E1 Interface Card 1 in MIM 3 is set-up to drive the A sync line and T1/E1 Interface Card 1 in NIM 1 is set-up to drive the B sync line. In this example no other T1/E1 Interface Card within the CEC/IMC can be configured to drive a sync line on the Backplane. Depending upon which system clock is selected (A or B), one of the T1/E1 Interface Cards will provide a primary 8 kHz sync line and one will provide a secondary 8 kHz sync line as follows:

System Clock A:	MIM 3 = primary sync NIM 1 = secondary sync
System Clock B:	NIM 1 = primary sync MIM 3 = secondary sync

In this example, when system clock B is the selected clock, all CEC/IMC clocks sync to the T1/E1 line connected to NIM 1. If a failure occurs in this T1/E1 line the Clock Board will switch to secondary sync (MIM 3). If any B clock circuit fails and redundant clock switching is enabled, the system will switch to the A clock circuits; thus, the T1/E1 line connected to MIM 3 will provide primary sync for the Clock Board. Therefore, all CEC/IMC clocks sync to the T1/E1 line connected to MIM 3. This feature is only available for the slave clock mode.

GATE ARRAYS, SUBRATE PORTS AND RS-232 DRIVERS/RECEIVERS

Six (6) Actel A1240 (or equivalent) field-programmable gate array (FPGA) chips support the T1/E1 Interface Card's subrate ports and DS0B packing/unpacking for T1/E1 channels [schematic diagram sheets 7 and 8]. U94 thru U98 support both the subrate ports and DS0B packing/unpacking. U99 provides only DS0B packing/unpacking functions. Basically, these gate array chips are placed in the circuitry between the MTSC chips [schematic diagram sheets 3 and 4] and the subrate ports' RS-232 drivers and receivers [schematic diagram sheet 8]. MTSC chips provide the data path to/from the TDM network on the CEC/IMC Backplane and to/from T1/E1 framer U85. Microprocessor U1 provides master control.

All gate arrays are identically configured with five (5) I/O interfaces and a DS0B packer/unpacker interface. However, depending upon the specific gate array and its mode of operation, each gate array does not use all of its programmed interfaces. For example, if U96 is operating in gate array mode 1, only its first I/O interface is used. See the subsection entitled "**Gate Array Modes**" (page 31) for additional details.

NOTE

A review of the "**DESCRIPTION**" (page 5) and "**OPERATING MODE**" (page 5) sections of this manual may be beneficial at this time.

Subrate Port Interfacing

To provide subrate port support, the gate arrays route and encode/decode data signals between the MTSC chips and the RS-232 drivers/receivers. As previously stated, the MTSC chips provide the data path to/from the CEC/IMC TDM network and to/from the T1/E1 framer chip.

Subrate ports' synchronous/asynchronous selections are auto-configured by the CEC/IMC Manager in accordance with the specific card mode selection, free T1/E1 channels and other parameters set at the CEC/IMC Manager. See the section entitled "**Gate Array Modes**" (page 31) for additional details.

Up to five (5) subrate ports operating in synchronous mode are DS0B packed/unpacked (encoded/decoded) to/from a single packed 64 kbps channel (DS0). Synchronous subrate ports operate at 9600 bps (baud). Therefore, each packed 64 kbps channel can contain up to five 9600 bps full-duplex signals. Gate arrays perform DS0B packing/unpacking and the required signal routing.

For a subrate port operating in an asynchronous mode, a gate array encodes/decodes subrate data into/from a single 64 kbps channel at the T1/E1 line interface. Asynchronous subrate ports support standard and non-standard baud rates up to 19,200 bps. A gate array samples the incoming asynchronous serial receive data at a 128 kHz rate to reconstruct the transmit data baud rate.

Each gate array chip has five (5) subrate interfaces for a total of thirty (30) possible subrate interfaces. However, due to DIN connector pin limitations, only eight (8) of the thirty are actually ever utilized. The first interface on each gate array can be configured for synchronous or asynchronous operation and the other four interfaces on each gate array are synchronous-only interfaces.

Table 11 maps U94 thru U98 utilization for each subrate port and valid synchronous/asynchronous mode. No U99 subrate interfaces are used. As shown in the table and as discussed in the "**DESCRIPTION**" section of this manual, subrate ports 1 thru 5 can operate in a synchronous (sync) or an asynchronous (async) mode; ports 6 thru 8 are reserved for synchronous operation only.

Table 11 – Subrate Port-to-Gate Array Utilization

SUBRATE PORT	GATE ARRAY				
	U94	U95	U96	U97	U98
1	A, S				
2	S	A			
3	S		A		
4	S			A	
5	S				A
6		S			
7		S			
8		S			

S = Gate array chip utilized for synchronous operation.
A = Gate array chip utilized for asynchronous operation.

The specific gate array chip and gate array I/O pins used for a particular subrate port are dependent upon if the port is auto-configured by the CEC/IMC Manager for synchronous or asynchronous operation. See Table 11 and the schematic diagram. For example, if subrate port 3 is auto-configured for asynchronous operation, U96 pins 20 and 21 are utilized but if subrate port 3 is auto-configured for synchronous operation, U94 pins 29 thru 32 are utilized. However, for subrate port 1, both synchronous and asynchronous conversions are accomplished within the same gate array chip – U94. U94 pins 16 thru 21 provide the connections. Also, U94 is dedicated to ports 1 thru 5 if

all five are synchronous ports. U95 is dedicated to synchronous subrate ports 6 thru 8.

Receive Data And Clock Gate Array Inputs

RS-232 receivers convert RS-232-level receive subrate data serial signals to TTL-level serial signals [schematic diagram sheet 8]. Receivers are described in greater detail later. With the exception of subrate ports 6 thru 8, each TTL-level serial receive data signal is then applied to two (2) gate array I/O pins programmed as inputs – one for synchronous interfacing and one for asynchronous interfacing. These two pins may be on separate gate arrays or the same gate array. Subrate port sync/async auto-configuration determines which gate array input pin is utilized for receive data. For example, if subrate port 3 is auto-configured for asynchronous operation, the receive data input at U96 pin 20 (RX3) is used and the paralleled asynchronous input at U94 pin 29 (also RX3) is ignored. Subrate ports 6 thru 8 each require only one receive data input pin (at U95) since these three subrate ports are synchronous-only ports.

For synchronous support, a receive clock for a particular subrate port is only applied to one gate array I/O pin. Like a receive data gate array I/O pin, this I/O pin is also programmed as an input. For example, the receive clock gate array input pin for subrate port 3 is U94 pin 30 (RX3_CLK). Before application to the gate array circuits, receive clocks are also converted from RS-232 levels to TTL levels by the RS-232 receivers. A receive clock is ignored if the subrate port is auto-configured for asynchronous operation.

Transmit Data And Clock Gate Array Outputs

With the exception of subrate ports 6 thru 8, transmit data for each subrate port originates from one of two (2) separate gate array I/O pins programmed as outputs; one is the synchronous output and one is the asynchronous output. For example, subrate port 3's asynchronous transmit data output is located at U96 pin 21 (TX3_ASYNC) and its synchronous output is located at U94 pin 31 (TX3_SYNC) [schematic diagram sheet 7].

Since subrate ports 2 thru 5 sync and async transmit data outputs originate from separate gate array chips, additional logic is used to select either the synchronous output or the asynchronous output of each port. This logic includes quad 3-state drivers U104 & U105 and dual data flip-flops U91 & U92. Microprocessor U1 provides master control of this circuitry per subrate ports sync/async auto-configurations. Subrate port 1 does not require additional sync/async select logic since sync/async selection is accomplished within the same gate array – U94. U94 sets its unused subrate port 1 transmit data output (pin 18 or pin 21) to a high-impedance state. Also, since ports 6 thru 8 support synchronous operation only, no sync/async select logic is required for these transmit data outputs.

Like a subrate port's receive clock for synchronous support, each transmit clock requires only one gate array I/O pin. These I/O pins are programmed as outputs. Each transmit clock output is applied directly to an RS-232 driver input for TTL-to-RS-232 level conversion; no sync/async selection circuitry is required since a transmit clock output is only utilized if the subrate port is auto-configured for synchronous operation.

Subrate Ports 2 – 5 Sync/Async Transmit Data Selection

As previously mentioned, subrate ports 2 thru 5 each require additional logic to select either a synchronous or an asynchronous gate array transmit data output. The selected output for a given port is applied to the input of the respective RS-232 driver. Selection logic includes quad 3-state drivers U104 & U105 [schematic diagram sheet 8] and dual data flip-flops U91 & U92 [schematic diagram sheet 7]. Microprocessor U1 provides master control of this selection circuitry via octal latches U89 and U90 per the subrate ports' sync/async auto-configurations. U89 and U90 operation is described in the section entitled "**Microprocessor Interface**" (page 30).

For each subrate port 2 thru 5, two 3-state drivers' outputs are connected together to form a wired-OR function. Only one driver – the sync driver *or* the async driver – is enabled (selected) at a time; the disabled driver's output remains in a high-impedance state. The enabled 3-state driver's output drives the input of the respective RS-232 driver in accordance with the serial data signal from the gate array's I/O pin programmed as an output; thus, sync/async transmit data gate array output pin selection is fulfilled.

Complementary outputs (Q and $\overline{Q}$) from dual data flip-flops U91 and U92 generate eight active-high enables for the eight 3-state drivers. These flip-flops are loaded by microprocessor U1 via octal latches U89 and U90 [schematic diagram sheet 7]. For ports 2 thru 5 respectively, asynchronous enables are LCA2_ASYNC thru LCA5_ASYNC and synchronous enables are LCA2_SYNC thru LCA5_SYNC. For example, to select subrate port 3's asynchronous gate array output pin, LCA3_ASYNC from U91B pin 9 is set high. Since the complementary output from U91B pin 8 (LCA3_SYNC) is simultaneously low, driver U104C is enabled and driver U104D is disabled. Therefore, U104C applies TX3_ASYNC asynchronous transmit data from gate array U96 pin 21 to RS-232 driver U100 pin 22.

RS-232 Drivers

RS-232 drivers U100 and U102 convert subrate port transmit data and transmit clock TTL-level serial signals from the gate arrays to RS-232-level serial signals. U100 supports subrate ports 1 thru 4 and U102 supports subrate ports 5 thru 8.

To support redundant card capability, these drivers are only enabled if the T1/E1 Interface Card is in primary mode (!PRIMARY = low). This is accomplished by applying !PRIMARY to U100 and U102s' active-low enable inputs (pin 10). When !PRIMARY is high, all RS-232 drivers' outputs remain in a high-impedance state.

The RS-232 transmit data outputs are identified TX1_232 thru TX8_232 and the RS-232 transmit clocks are identified TX1_CLK_232 thru TX8_CLK_232. These lines are routed out of the T1/E1 Interface Card via 96-pin DIN connector J2 (bottom DIN connector) [schematic diagram sheet 10].

RS-232 Receivers

Subrate port receive data and receive clock signals are routed into the T1/E1 Interface Card via 96-pin DIN connector J2 (bottom DIN connector) [schematic diagram sheet 10]. For subrate ports 1 thru 8 respectively, the receive data lines are identified Rx1_232 thru Rx8_232 and the receive clock lines are identified Rx1_CLK_232 thru Rx8_CLK_232. A gate array only utilizes a receive clock if the respective subrate port is operating in (auto-configured for) synchronous mode.

Subrate port RS-232 serial receive signals coming into the T1/E1 Interface Card via J2 are applied to the receiver inputs of octal receivers U101 and U103 [schematic diagram sheet 7]. These integrated circuits provide RS-232-to-TTL level conversions. U101 supports ports 1 thru 4 and U103 supports ports 5 thru 8. These receivers are RS-232 and RS-423 compatible; however, they operate in an RS-232 mode since each receiver's + input is grounded.

TTL-level serial signals from the receivers' outputs are routed to gate array chips U94 thru U98 via RX1 thru RX8 (receive data) and RX1_CLK thru RX8_CLK (receive clock). Each receive signal is applied to an I/O pin on a gate array chip programmed as an input [schematic diagram sheets 7 and 8].

Microprocessor Interface

Octal (8-bit) latches U89 and U90 provide the microprocessor interface for the gate array chips and the sync/async selection flip-flops [schematic diagram sheet 7]. Microprocessor U1 can write data to the gate arrays and flip-flops using U89 and U90. When selected by U1, U89 latches the lower data bus byte. Similarly, U90 latches the upper data bus byte when it is selected.

U89 and U90 chip selection involves NORing the active low !TERM_MODE line from U1 pin 30 [schematic diagram sheet 1] with either the active-low !WRLB (write low byte) for U89 or the active-low !WRHB (write high byte) for U90. Each NOR gate output (U8B pin 4 and U8C pin 10) controls the latch-enable input of its octal latch (U89 pin 11 and U90 pin 11 respectively).

U89 latches 8-bit configuration data for the gate arrays and flip-flops. Latched output bits LCA_D[0] thru LCA_D[7] are defined as follows:

LCA_D[0] (U89 pin 19) — Subrate interface 1 mode selection:
0 = synchronous mode
1 = asynchronous mode

LCA_D[1] (U89 pin 18) — Synchronous port baud rate selection:
0 = 4800 bps (not supported)
1 = 9600 bps

LCA_D[2] (U89 pin 17) — Least-significant bit of gate array mode

LCA_D[3] (U89 pin 16) — Most-significant bit of gate array mode

LCA_D[4] (U89 pin 15) — Loop timing:
0 = normal
1 = TX data clocked by internal RX clock

LCA_D[5] (U89 pin 14) — Loop timing clock invert:
0 = normal
1 = inverted clock

LCA_D[6] (U89 pin 13) — (not used)

LCA_D[7] (U89 pin 12) — (not used)

U90 latches six (6) active-low chip-selects, one for each gate array. Only one output is active at a time. These outputs are identified !LCA1_CS thru !LCA6_CS. A gate array accepts the LCA_D[0] thru LCA_[7] latched byte from U89 at a high-to-low chip-select transition. Gate array data byte inputs are U94 thru U99 pins 55 thru 62 at all gate arrays. Chip-selects from U90 are applied to pin 54 at each gate array.

To control sync/async selection flip-flops U91 and U92, chip selects !LCA2_CS thru !LCA5_CS are also applied the clock inputs of these flip-flops [schematic diagram sheet 7]. Upon a low-to-high chip-select transition, a flip-flop latches the state of LCA_D[0] on its Q output. As previously described, these flip-flops' outputs provide subrate port sync/async selection for subrate ports 2 thru 5

by enabling/disabling 3-state drivers within U104 thru U105.

On-Card TDM Network

Four (4) on-card 32-slot TDM bus lines between the MTSC chips and the gate array chips form two (2) separate full-duplex data links between these integrated circuits. See Table 13. SUB1_PCM_IN and SUB1_PCM_OUT are U94 thru U98 inputs and outputs respectively for the first full-duplex TDM bus. SUB2_PCM_IN and SUB2_PCM_OUT are U99 inputs and outputs respectively for the second bus [schematic diagram sheets 3, 4, 7 and 8]. As previously stated, MTSC chips provide the data path to/from the CEC/IMC TDM network on the Backplane and to/from the T1/E1 framer.

Each gate array is assigned six (6) TDM bus time slots of the on-card bus. This assignment is established by the 3-bit hard-wired number set at pins 51 thru 53 of each gate array. Gate array U94 is assigned the first group of six slots (slots 0 thru 5), U95 is assigned the second group (slots 6 thru 11), etc.

Gate Array Modes

Using the LCA_D[2] and LCA_D[3] latched outputs from octal latch U89, microprocessor U1 individually sets each gate array to operate in one (1) of three (3) different gate array modes per CEC/IMC Manager configuration. See the previous section entitled "**Microprocessor Interface**" (page 30) for details on U1 control of LCA_D[2] and LCA_D[3].

Table 12 indicates card mode-to-gate array mode mapping. Table 13 shows data signal flow into and out of each gate array on a per gate array mode basis. As shown in the tables, gate array U99 only operates in mode 2. In the initial firmware/software release, only one gate array mode (U99 not used) and one card mode is available.

Table 12 – Card Mode-to-Gate Array Mode Mapping

CARD MODE	CEC/IMC MANAGER DESIGNATION	U94 – U98 GATE ARRAY MODE(S)	U99 GATE ARRAY MODE
Analog/ Modem (Figure 1)	"Analog or Digital Voice using Modems"	1	2
(reserved for future use) *	—	0	2
(reserved for future use) *	—	2 or 1	2

* Shaded areas indicate modes not supported in the initial firmware/software release(s).

Table 13 – Data Flow Into and Out Of Gate Arrays U94 Thru U98*

		ON-CARD TDM BUS LINES						
		SUB1_PCM_IN (U94 thru U98 inputs)			SUB1_PCM_OUT (U94 thru U98 outputs)			
GATE AR-RAY	TDM BUS TIME SLOT	GATE ARRAY MODE			GATE ARRAY MODE			SITE CHN. ***
		0	1	2	0	1	2	
U94	0		T1/E1 ⇒ subrate port 1 TX (async)			subrate port 1 RX (async) ⇒ T1/E1		
	1		(not used)			(not used)		30
	2		(not used)			(not used)		⇳
	3		(not used)			(not used)		26
	4		(not used)			(not used)		
	5		T1/E1 ⇒ U94 DS0B unpacker (to sync subrate ports 1-5**)			U94 DS0B packer (from sync subrate ports 1-5**) ⇒ T1/E1		

(Table Continued On Next Page)

Table 13 – Data Flow Into and Out Of Gate Arrays U94 Thru U98* (Continued)

		ON-CARD TDM BUS LINES						
		SUB1_PCM_IN (U94 thru U98 inputs)			SUB1_PCM_OUT (U94 thru U98 outputs)			
GATE ARRAY	TDM BUS TIME SLOT	GATE ARRAY MODE			GATE ARRAY MODE			SITE CHN. ***
		0	1	2	0	1	2	
U95	6		T1/E1 ⇒ subrate port 2 TX (async)			subrate port 2 RX (async) ⇒ T1/E1		
	7		(not used)			(not used)		25
	8		(not used)			(not used)		⇳
	9		(not used)			(not used)		21
	10		(not used)			(not used)		
	11		T1/E1 ⇒ U95 DS0B unpacker (to sync subrate ports 6 - 8)			U95 DS0B packer (from sync subrate ports 6 - 8) ⇒ T1/E1		
U96	12		T1/E1 ⇒ subrate port 3 TX (async)			subrate port 3 RX (async) ⇒ T1/E1		
	13		(not used)			(not used)		20
	14		(not used)			(not used)		⇳
	15		(not used)			(not used)		16
	16		(not used)			(not used)		
	17		(unpacker not used)			(packer not used)		
U97	18		T1/E1 ⇒ subrate port 4 TX (async)			subrate port 4 RX (async) ⇒ T1/E1		
	19		(not used)			(not used)		15
	20		(not used)			(not used)		⇳
	21		(not used)			(not used)		11
	22		(not used)			(not used)		
	23		(unpacker not used)			(packer not used)		
U98	24		T1/E1 ⇒ subrate port 5 TX (async)			subrate port 5 RX (async) ⇒ T1/E1		
	25		(not used)			(not used)		10
	26		(not used)			(not used)		⇳
	27		(not used)			(not used)		6
	28		(not used)			(not used)		
	29 ****		(unpacker not used)			(packer not used)		

* Signal from ⇒ signal to. Shaded areas not applicable to initial firmware/software release(s).
** Subrate ports auto-configured for asynchronous operation are not supported/available at this I/O time slot.
*** Site channel allocations applicable to gate array mode 2 only.
**** Time slots 30 and 31 not used by U94 thru U98.

Analog/Modem Mode
(Uses Gate Array Mode 1 Only)

As shown in Table 12, if the T1/E1 Interface Card is configured for the analog/modem mode for a modem-equipped system all gate arrays are set to mode 1 except U99. This is accomplished by setting LCA_D[2] high and LCA_D[3] low when each gate array's configuration byte is written (except U99's). As described on page 5 of this manual, analog/modem mode supports trunked site channel operations over the T1/E1 link (CEC/IMC TDM network ⇔ T1/E1 line) for analog voice and modem-encoded data signals. *These operations do not utilize any gate array resources.* In this card mode, one site channel is assigned to each T1/E1 channel and if T1/E1 channels are available after site channel allocations, subrate data may be transferred over T1/E1 channel(s) using gate array resources. The number of site channels which a T1/E1 Interface Card supports is equal to its "Set Site Channels Disbursement" setting at the CEC/IMC Manager.

In the analog/modem mode, packers and unpackers within U94 and U95 provide packing/unpacking functions for synchronous subrate ports, and U94 thru U98 support asynchronous subrate ports 1 thru 5 respectively. U99 is not used. Sync/async subrate port assignments are auto-configured via the CEC/IMC Manager. See Table 13 for signal flow into and out of the gate arrays.

PARALLEL I/O CONTROL

Within a particular CEC/IMC interface module (MIM, NIM, etc.) employing T1/E1 Interface Cards, sixteen (16) logic outputs from the interface module's Controller Board are applied to sixteen respective logic inputs at each T1/E1 Interface Card. This 16-bit unidirectional parallel interface, known as the parallel I/O control interface, grants the active Controller Board master control of certain critical T1/E1 Interface Card hardware functions *without* T1/E1 Interface Card microprocessor intervention. Critical control is ensured even if the T1/E1 Interface Card is not executing firmware code properly or the HDLC link is inoperative. Also, process loading of microprocessor U1 is slightly reduced since this control is accomplished exclusively via hardware on the T1/E1 Interface Card. T1/E1 Interface Card parallel I/O control includes:

- primary/secondary card mode selection
- system clock A/B selection
- redundant line relay control
- Futurebus drivers master enable/disable control

On the rear of the CEC/IMC Backplane, parallel I/O control connections are made via the Local Bus Cables. All boards/cards within a particular interface module are paralleled together via Local Bus Cables. These cables also provide the HDLC serial link connections between the Controller Board(s) and the T1/E1 Interface Card(s) within an interface module.

The 16-bit parallel I/O control lines are divided into two 8-bit groups – data and enable. Data lines are labeled DB[0] thru DB[7] and the enable lines are labeled ENBL[0] thru ENBL[7]. These TTL-level logic lines enter the T1/E1 Interface Card via 96-pin DIN connector J1 [schematic diagram sheet 10]. Specifically, data lines enter at J1 pins 13C (DB[0]) thru 20C (DB[7]) and enable lines enter at J1 pins 23C (ENBL[0]) thru 30C (ENBL[7]).

Parallel I/O control interface circuitry on the T1/E1 Interface Card includes octal data latches U112 thru U114, 4-bit binary comparator U110, dual data flip-flops U111 and U115, and several logic gates. [schematic diagram sheet 9].

Initial software/firmware release(s) allow cascading of up to four (4) T1/E1 Interface Cards within a single CEC/IMC interface module. Future releases will allow up to eight (8) cards. Therefore, parallel I/O control sent out from a Controller Board must include a method to select only one T1/E1 Interface Card at a time. Basically, this selection is accomplished by comparing the 4-bit card address number set by DIP switch SW1 positions 5 (MSB) thru 8 (LSB) on the T1/E1 Interface Card with a 4-bit card address number sent from the Controller Board. When the two addresses are equal (and other parallel I/O control bits are set correctly), the card is selected for parallel I/O control. The card address number is sent from the Controller Board to the T1/E1 Interface Card via parallel I/O data lines DB[0] thru DB[3]. The card remains selected for parallel I/O control until an unselect pulse is sent from the Controller Board over a parallel I/O control ENBL line.

NOTE

Like a CEC/IMC Audio Board, each T1/E1 Interface Card *within a particular CEC/IMC interface module* must have a unique card address number. The customer-specific system documentation print-outs define specific card address numbers on a per Card Cage slot basis. See LBI-38939 for additional details.

Parallel I/O card selection is accomplished using 4-bit binary comparator U110, AND gate U65C, inverter U49E and flip-flop U111A. These chips generate the CARD_SEL output at U111A pin 5. When CARD_SEL is high, the T1/E1 Interface Card is selected for parallel I/O control. In

this selected state, the Controller Board can latch certain lines on the T1/E1 Interface Card high or low as necessary.

CARD_SEL is applied to the latch-enable input of U112 [schematic diagram sheet 9] and to an I/O input port bit at U10 pin 5 [schematic diagram sheet 1]. When U112's latch enable pin is high (U112 pin 11), its data outputs (pins 12 thru 19) follow its data inputs (pins 9 thru 2 respectively). U113 and U114 operate identically; however, their latch enable inputs are driven by outputs from U112.

To set CARD_SEL high, the Controller Board first outputs a byte on parallel I/O data bus DB[0] thru DB[7]. DB[0] thru DB[3] contain the card address number of the T1/E1 Interface Card to be selected. Also, DB[7] is high. DB[0] thru DB[3] are applied to U110's B compare inputs. They are compared to the DIP switch card address lines applied to the A compare inputs. Next, the Controller Board outputs a byte on parallel I/O enable bus ENBL[0] thru ENBL[7]. This byte pulls ENBL[6] low and ENBL[7] high. This sets CARD_SEL at U111A pin 5 high. When CARD_SEL transitions high, the byte on ENBL[0] thru ENBL[7] appears on U112's Q outputs. CARD_SEL will remain high until the Controller Board unselects the T1/E1 Interface Card for parallel I/O by resetting U111A. This is accomplished by pulsing ENBL[6]. In addition, the card can be unselected by a card reset (!RESET = low) using U111A's clear input a U111A pin 1. Specific details on the DB and ENBL control bytes sent from a Controller Board to the T1/E1 Interface Card during a parallel I/O control sequence are included in the following subsections.

With the card selected for parallel I/O control (CARD_SEL = high) controlling logic signals can then be latched on the Q outputs of octal data latches U112 thru U114. U112 outputs several logic lines including latch enables for U113 and U114, a primary/secondary select line, and the card unselect line (CARD_UNSEL) to flip-flop U111A. See Table 14. U113 latches LD[0] thru LD[7] on its Q outputs; only LD[0] is used. It is applied to the data inputs of flip-flops U111B, U115A, U115B [schematic diagram sheet 9] and U51A [schematic diagram sheet 4]. These flip-flops control various logic lines as described in the following subsections.

Table 14 – U112 Output Bits' Functions

U112 INPUT BIT	U112 OUTPUT BIT	OUTPUT BIT FUNCTION
ENBL[0]	DATA_LATCH_EN	enables data latch U113 which drives LD[0] thru LD[7]; only LD[0] is used
ENBL[1]	(not used)	(none)
ENBL[2]	CH_FUNC_EN	enables card function latch U114 which drives CF[0] thru CF[7]; only CF[6] is used
ENBL[3]	RED_LIN_EN	clocks flip-flop U115A which selects a redundant T1/E1 line via a relay on the T1/E1 Concentrator Card
ENBL[4]	CLK_SEL_EN	clocks flip-flop U115B which drives the system A/B clock select line CLK_SELA_!B
ENBL[5]	PRI/SEC_SEL	clocks flip-flop U111B which drives the primary/secondary mode select lines PRI/!SEC and !PRIMARY
ENBL[6]	CARD_UNSEL	disables T1/E1 Interface Card for parallel I/O control by clocking flip-flop U111A so CARD_SEL transitions low
ENBL[7]*	(not used)	(none)

* The ENBL[7] output from the Controller Board gates the A=B output from binary comparator U110 to flip-flop U111A.

Primary/Secondary Mode Selection

Data flip-flop U111B outputs primary/secondary mode select logic lines PRI/!SEC and !PRIMARY in accordance with parallel I/O control sequencing received from the Controller Board. These two logic lines are always in an inverse state with each other since they are driven by the complementary Q and $\overline{Q}$ outputs from the flip-flop. When the card is in primary mode, PRI/!SEC is high and !PRIMARY is low.

When the card is in secondary mode (!PRIMARY = high), transistor Q8 turns LED DS7 on. On the card's front panel, this LED is labeled "SEC" [schematic diagram sheet 9]. A T1/E1 Interface Card in secondary mode only monitors TDM network, HSCX and subrate port activity; it never sends out any signals.

At card power-up or reset the card is set to secondary mode. This is accomplished by clearing flip-flop U111B with the !RESET pulse. !RESET is applied to U111B pin 13, the flip-flop's active-low clear input. Upon being cleared, PRI/!SEC is set low and !PRIMARY is set high; the card is in secondary mode.

Immediately after a card power-up or reset, the Controller Board loads the required mode into U111B via a

parallel I/O control sequence. This load occurs even if the required mode is secondary. U111B latches the state of LD[0] when clocked by the PRI/SEC_SEL output from U112 pin 14. DB and ENBL 8-bit output sequences from the Controller Board are as follows ("xxH" = hexadecimal value sent out by Controller Board):

1. DB = 80H + card address > sets DB[7] high and DB[0] thru DB[3] equal to 4-bit card address number
2. ENBL = 80H > causes ENBL[7] to transition high which gates A=B output from U110 to U111A; thus CARD_SEL transitions high
3. ENBL = 00H > ENBL[7] returns low
4. DB = 00H or 01H > 00H for secondary mode or 01H for primary mode
5. ENBL = 01H > causes DATA_LATCH_EN from U112 to transition high; thus, LD[0] output from U113 transitions to reflect the state of DB[0] set in step 4
6. ENBL = 00H > DATA_LATCH_EN returns low; thus, latch U113 is disabled and its outputs latch
7. ENBL = 20H > causes PRI/SEC_SEL from U112 to transition high; thus, PRI/!SEC output from U111B latches in the same state as the DB[0] line from the Controller Board and the latched LD[0] from U113
8. ENBL = 00H > sets PRI/SEC_SEL low

After this sequencing, additional parallel I/O control sequencing may follow to latch other data flip-flops. However, if this is the last sequence, the Controller Board will simply output an ENBL value of 40H (ENBL[6] = high, all other ENBLs = low) to unselect the card for parallel I/O control.

DIP switch SW1 position 2 controls the active-low !PRIMARY_EN (primary enable) line applied to U111B's preset input at U111B pin 10. This hardware-selectable setting is provided for diagnostic testing only. When low (SW1 position 2 "CLOSED" or "ON"), the card is forced into primary mode at all times no matter what mode is loaded by the Controller Board. **SW1 position 2 should always remain "OPEN" or "OFF"** [schematic diagram sheets 1 and 9].

Redundant Line Relay Control

To provide T1/E1 redundant line capability, the T1/E1 Interface Card is equipped with an open-collector relay control output. This output, LINE_RELAY_EN at J2 pin 8B, controls the two relays on the T1/E1 Concentrator Card connected to the T1/E1 Interface Card. Drive control (the ability to energize the relays) is only granted when the T1/E1 Interface Card is in primary mode. LINE_RELAY_ENables from two T1/E1 Interface Cards of a redundant T1/E1 Interface Card pair are paralleled together at the T1/E1 Concentrator Card. Components in this circuit include data flip-flop U115A, AND gate U65D and transistor Q9 [schematic diagram sheet 9].

During a parallel I/O control sequence for redundant line relay control, data flip-flop U115A latches the state of LD[0] on its Q output (U115A pin 5). This output state is gated with PRI/!SEC via AND gate U65D before driving Q9. This guarantees a T1/E1 Interface Card in secondary mode cannot energize the relays by pulling LINE_RELAY_EN low. DB and ENBL 8-bit output sequences from the Controller Board are as follows ("xxH" = hexadecimal value sent out by Controller Board):

1. DB = 80H + card address > sets DB[7] high and DB[0] thru DB[3] equal to 4-bit card address number
2. ENBL = 80H > causes ENBL[7] to transition high which gates A=B output from U110 to U111A; thus CARD_SEL transitions high
3. ENBL = 00H > ENBL[7] returns low
4. DB = 00H or 01H > 00H to turn relay off or 01H to turn relay on
5. ENBL = 01H > causes DATA_LATCH_EN from U112 to transition high; thus, LD[0] output from U113 transitions to reflect the state of DB[0] set in step 4
6. ENBL = 00H > DATA_LATCH_EN returns low; thus, latch U113 is disabled and its outputs latch
7. ENBL = 08H > causes RED_LINE_EN from U112 to transition high; thus, U115A latches to reflect the state of DB[0] from the Controller Board via the latched LD[0] state from U113
8. ENBL = 00H > sets RED_LINE_EN low

After this sequencing, additional parallel I/O control sequencing may follow to latch other data flip-flops.

However, if this is the last sequence, the Controller Board will simply output an ENBL value of 40H (ENBL[6] = high, all other ENBLs = low) to unselect the card for parallel I/O control.

System (A/B) Clock Selection

As previously described in the section entitled "**CLOCK SELECTION AND GENERATION**", subsection "**System Clock Mode & Selection Circuits**" (page 21), the $\overline{Q}$ output from data flip-flop U115B pin 8 drives system clock select line CLK_SELA_!B [schematic diagram sheet 9]. When CLK_SELA_!B is low, the T1/E1 Interface Card is clocked by the B clock pulses from the CEC/IMC Clock Board. When it is high, the A clock pulses are utilized. However, neither system clock is used if the card is operating in stand-alone clock mode.

Like the primary/secondary select and redundant line relay control flip-flops, flip-flop U115B latches to the state of the LD[0] output from U113 pin 12. CLK_SEL_EN from U112 pin 15 clocks U115B during the A/B clock select parallel I/O control sequence. The 8-bit parallel I/O control sequences from the Controller Board are as follows ("xxH" = hexadecimal value sent out by Controller Board):

1. DB = 80H + card address > sets DB[7] high and DB[0] thru DB[3] equal to 4-bit card address number
2. ENBL = 80H > causes ENBL[7] to transition high which gates A=B output from U110 to U111A; thus CARD_SEL transitions high
3. ENBL = 00H > ENBL[7] returns low
4. DB = 00H or 01H > 00H to select A clocks or 01H to select B clocks
5. ENBL = 01H > causes DATA_LATCH_EN from U112 to transition high; thus, LD[0] output from U113 transitions to reflect the state of DB[0] from the Controller Board set in step 4
6. ENBL = 00H > DATA_LATCH_EN returns low; thus, latch U113 is disabled and its outputs latch
7. ENBL = 10H > causes CLK_SEL_EN from U112 to transition high and DATA_LATCH_EN from U112 to transition low; thus, U115B latches to the state of the LD[0] latched output from U113
8. ENBL = 00H > sets CLK_SEL_EN low

After this sequencing, additional parallel I/O control sequencing may follow to latch other data flip-flops. However, if this is the last sequence, the Controller Board will simply output an ENBL value of 40H (ENBL[6] = high, all other ENBLs = low) to unselect the card for parallel I/O control.

Futurebus Drivers Master Enable/Disable Control

All drivers within the Futurebus transceivers responsible for TDM network interfacing (U50 and U70 thru U75) are master enabled/disabled by a parallel I/O control sequence from the Controller Board. All are disabled when the card is in secondary mode (!PRIMARY = high). Each driver also has an individual transmit enable line controlled by an MTSC chip output; both transmit enables (master and individual) must be active before a driver can drive its TDM bus line on the CEC/IMC Backplane. During a card reset condition (!RESET = low), all Futurebus drivers are disabled. [schematic diagram sheets 4 and 5].

The active-low latched output from flip-flop U51A, !FBUS_EN, is the master driver enable/disable control line [schematic diagram sheet 4]. It is applied to the transmit enable input of each Futurebus transciever which connects to TDM bus lines [schematic diagram sheets 4 and 5]. When !FBUS_EN is low the drivers are master enabled. See the section entitled "**FUTUREBUS TRANSCEIVERS**", subsection "**TDM Bus Interfacing**" (page 20) for additional details.

The Controller Board latches high/low logic states on U51A's !FBUS_EN output (U51A pin 6) using the following parallel I/O control sequence. Unlike the other data flip-flops latched via parallel I/O control sequences, U51A's clock input is driven by the CF[6] output from U114, not an output from U112:

1. DB = 80H + card address > sets DB[7] high and DB[0] thru DB[3] equal to 4-bit card address number
2. ENBL = 80H > causes ENBL[7] to transition high which gates A=B output from U110 to U111A; thus CARD_SEL transitions high
3. ENBL = 00H > ENBL[7] returns low
4. DB = 00H or 01H > 00H to master disable drivers or 01H to master enable drivers

5. ENBL = 01H > causes DATA_LATCH_EN from U112 to transition high; thus, LD[0] output from U113 transitions to reflect the state of DB[0] from the Controller Board set in step 3
6. ENBL = 00H > causes DATA_LATCH_EN from U112 to transition low; thus, LD[0] output from U113 latches to the same state as DB[0] set in step 3
7. DB = 40H > DB[6] transitions high
8. ENBL = 04H > causes CH_FUNC_EN from U112 to transition high; thus, CF[6] transitions to the same state as DB[6] – high, and U51A latches per the state of LD[0] latched in step 5
9. DB = 00H > DB[6] and CF[6] transition low
10. ENBL = 00H > sets CH_FUNC_EN low; U114 outputs latch

After this sequencing, additional parallel I/O control sequencing may follow to latch other data flip-flops. However, if this is the last sequence, the Controller Board will simply output an ENBL value of 40H (ENBL[6] = high, all other ENBLs = low) to unselect the card for parallel I/O control.

POWER SUPPLY

The T1/E1 Interface Card requires three (3) regulated dc power supplies: +5 Vdc, +12 Vdc and -12 Vdc. All CEC/IMC dc supply sources originate from the RPS units located at the bottom of the CEC/IMC cabinet. Power supply cables apply high-current +5 and medium-current ±15 Vdc outputs from the RPS units to the CEC/IMC Backplanes.

On the T1/E1 Interface Card, voltage regulator circuits are only utilized in the +12 and -12 Vdc supplies. These regulator circuits drop the ±15 Vdc RPS outputs to ±12 Vdc. On-card regulation of the +5 Vdc supply is not required since each RPS unit incorporates remote voltage sensing of the +5-volt supply at its respective Backplane.

+5 Vdc Supply Line

External +5 Vdc power (+5EXT) enters the T1/E1 Interface Card via 96-pin DIN connectors J1 pins 1C & 31C and J2 pins 1A & 31A [schematic diagram sheet 10]. J1 is the top DIN connector and J2 is the bottom DIN connector. From these pins, +5EXT is routed through 2-amp fuse F1 to a low-pass filter circuit formed by L2 and C100 thru C102. The output of this filter is the +5 Vdc supply line labeled +5V. This supply is applied to all digital ICs on the T1/E1 Interface Card.

Presence of +5V power lights LED DS8 via R304. This LED is labeled "+5V" on the front panel.

Capacitors C300 thru C409 (less C351) provide +5V decoupling. These capacitors are spread over the entire card [schematic diagram sheet 9].

+12 Vdc Supply Line

External +15 Vdc power (+15EXT) enters the T1/E1 Interface Card via 96-pin DIN connector J2 pin 27A [schematic diagram sheet 10]. From this point, +15EXT is routed through ½-amp fuse F2 to the input of 12-volt linear regulator U122 at pin 1. U122's regulated output at pin 3 drives the +12V supply line. This supply powers RS-232 subrate port drivers U100 & U102 [schematic diagram sheet 8], line monitor port drivers U125 thru U128 [schematic diagram sheet 10], and RS-232 transceiver U124 which supports the PC diagnostic serial port [schematic diagram sheet 10].

Resistor R305 lights LED DS9 when +12V power is present. This LED is labeled "+12V" on the front panel.

Capacitors C103 thru C106 provide filtering and decoupling functions at regulator U122's input and output. Capacitors C450 thru C459 (non-inclusive) decouple the +12V supply line [schematic diagram sheet 9].

-12 Vdc Supply Line

External -15 Vdc power (-15EXT) enters the T1/E1 Interface Card via 96-pin DIN connector J2 pin 29A [schematic diagram sheet 10]. From this point, -15EXT is routed through ½-amp fuse F3 to the input of negative 12-volt linear regulator U123 at pin 3. The -12 Vdc regulated output from U123 pin 2 drives the -12V supply line. Like the +12V supply, -12V powers RS-232 subrate port drivers U100 & U102, line monitor port drivers U125 thru U128, and RS-232 transceiver U124 which supports the PC diagnostic serial port.

Resistor R306 lights LED DS10 when -12V power is present. This LED is labeled "-12V" on the front panel.

Capacitors C107 thru C110 provide filtering and decoupling functions at the regulator's input and output. Capacitors C451 thru C463 (non-inclusive) decouple the -12V supply line [schematic diagram sheet 9].

EXTENDED POWER PINS

Several pins on each 96-pin DIN connector (J1 and J2) are slightly longer than the other pins. These elongated pins provide "make first – break last" contacting for the external +5 Vdc power applied to the T1/E1 Interface Card when the card is inserted into and extracted from a CEC/IMC Card Cage. Thus, the use of Live Insertion Cable 19B802612P1 *is not* required. Both +5 Vdc power (+5EXT) and ground (GND) pins are elongated.

TEST CONNECTOR

Test connector J3 provides convenient access to many T1/E1 Interface Card signals commonly used during card testing and troubleshooting procedures. This 40-pin miniature Champ-style connector is located near the bottom of the card's front panel [schematic diagram sheet 10]. Test Point Breakout Board 19D904176G1 mates with J3. This board contains test points for easy test access.

T1/E1 LINE MONITOR PORT

Transmitted and received signals on the T1/E1 line can be monitored from RJ-11 connector J4 located at the T1/E1 Interface Card's front panel. J4's pin-out is shown in the following table:

Table 15 – T1/E1 Line Monitor Port Pin-Out

J4 PIN	SIGNAL NAME	DESCRIPTION
1	XL1_MON	buffered transmit line (balanced pair) signal
2	XL2_MON	
3	GND	ground
4	RL1_MON	buffered receive line (balanced pair) signal
5	RL2_MON	
6	VDD2	2.5 Vdc reference applied to receive line coupling transformer

Both the XL (transmit line) and RL (receive line) monitor signals are J4 outputs. Voltage followers U125 thru U128 buffer the XL and RL signals prior to application to J4 [schematic diagram sheet 10]. U125 and U126 buffer the transmit line (XL1 & XL2) balanced pair signal sent out by the T1/E1 Interface Card and U127 and U128 buffer the receive line (RL1 & RL2) balanced pair signal coming into the card.

NOTE

Perform routine T1/E1 line monitoring at the T1/E1 Concentrator Card(s); signals at J4 are not 100% true representations of the signals on the T1/E1 line. **To prevent framing errors on the T1/E1 line, all outputs from J4 should only be loaded with high-impedance test loads.**

CONFIGURATION

DIP SWITCH SW1

DIP switch SW1 is factory-configured in accordance with the customer-specific system documentation print-outs. These print-outs are included with the CEC/IMC equipment when it ships from the factory. Basically, these print-outs specify the default settings for SW1 positions 1 thru 4 (open/off) and the 4-bit card address setting for positions 5 thru 8 per interface module card number.

In most cases, changes to the factory DIP switch settings should never be required. However, a card address setting change will be necessary if the card is moved to a different Card Cage slot which requires a different card address number. Refer to Table 3 in this manual and customer-specific system documentation print-outs for additional details.

Positions 1 thru 3 enable/disable certain hardware functions. **All three of these switches should remain in the "OPEN" or "OFF" (enabled) position during normal operation; they are provided for testing and troubleshooting procedures only.** See the section in this manual entitled "**Configuration DIP Switch**" (page 13) for additional details.

CEC/IMC MANAGER

Refer to the CEC/IMC Manager for Windows NT's operations guide (LBI-39224) or its on-line help for specific instructions on the set-up of the T1/E1 Interface Card. Also, as necessary, review the "**DESCRIPTION**" (pages 5 thru 7) and "**CLOCK SELECTION AND GENERATION"** (pages 21 thru 24) sections within this manual.

T1/E1 INTERFACE CARD
188D5909P1
(350A1158G1)

ISSUE 1

SYMBOL	PART NUMBER	DESCRIPTION
		---------- CAPACITORS ----------
C1	19A702061P33	Ceramic: 27 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C2	19A702061P25	Ceramic: 18 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C3	19A702052P1	Ceramic: 220 pF ±10%, 50 VDCW.
C4	19A705205P12	Tantalum: 0.33 uF, 16 VDCW; sim to Sprague 293D.
C5 and C6	19A702061P33	Ceramic: 27 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C7	19A702052P26	Ceramic: 0.1uF ±10%, 50 VDCW.
C15 and C16	19A702061P49	Ceramic: 56 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C25 thru C29	19A702061P45	Ceramic: 47 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C30 thru C33	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C34 thru C36	19A702061P45	Ceramic: 47 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C38	344A4010P3	Polyester: 0.33 uF ±5%, 250 VDCW.
C39	19A702236P50	Ceramic: 100 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C40	344A4010P3	Polyester: 0.33 uF ±5%, 250 VDCW.
C50 thru C73	19A702061P45	Ceramic: 47 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C80	19A702052P26	Ceramic: 0.1uF ±10%, 50 VDCW.
C81	19A703314P6	Electrolytic: 1 uF -10+50%, 50 VDCW; sim to Panasonic LS Series.
C82 thru C84	19A702052P26	Ceramic: 0.1uF ±10%, 50 VDCW.
C85 thru C88	19A702061P45	Ceramic: 47 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C100	19A703314P15	Electrolytic: 100 uF ±20%, 25 VDCW.
C101 and C102	344A4194P331250	Electrolytic: 330 uF ±20%, 25 VDCW.
C103	19A703314P4	Electrolytic: 47 uF -10+50%, 16 VDCW; sim to Panasonic LS Series.
C104	19A702052P26	Ceramic: 0.1uF ±10%, 50 VDCW.
C105	19A703314P4	Electrolytic: 47 uF -10+50%, 16 VDCW; sim to Panasonic LS Series.
C106	19A702052P26	Ceramic: 0.1uF ±10%, 50 VDCW.
C107	19A703314P4	Electrolytic: 47 uF -10+50%, 16 VDCW; sim to Panasonic LS Series.
C108	19A702052P26	Ceramic: 0.1uF ±10%, 50 VDCW.
C109	19A703314P4	Electrolytic: 47 uF -10+50%, 16 VDCW; sim to Panasonic LS Series.
C110	19A702052P26	Ceramic: 0.1uF ±10%, 50 VDCW.
C111 and C112	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C300 thru C350	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C352 thru C409	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C450 thru C463	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
		---------- DIODES ----------
D15	T324ADP1041	Silicon: Rectifier; sim to 1N4004.
D16 and D17	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99.
		---------- INDICATING DEVICES ----------
DS2 thru DS10	19A703595P9	Optoelectric: Green LED; sim to HLMP-1540-010.
		---------- FUSES ----------
F1	19A134961P20	Cartridge: 2.0 Amps Slow-Action; sim to Littelfuse 218 002.
F2 and F3	19A134961P10	Cartridge: 0.5 Amp Slow-Action; sim to Littelfuse 218.500.
		---------- JACKS ----------
J1 and J2	RPV403804/01	DIN, Rectangular: 96-pin; sim to AMP 536366-1.
J3	19B802174P2	Receptacle, Champ: 40-position, right-angle mounting; sim to AMP 5-175474-5.
J4	344A3288P3	Modular: 6-position; sim to AMP 555163-1.
J5	19B209727P37	Connector, D-subminiature: 9 contacts, sim to AMP 745781-4.
		---------- INDUCTORS ----------
L1	19A700021P28	Coil, fixed: 8.2 uH.
L2	REG70471/1	Coil, high current: 100 uH ±10%, 4.2 A.
		---------- TRANSISTORS ----------
Q1	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q3 thru Q9	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
		---------- RESISTORS ----------
R1 and R2	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R3 and R4	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R5	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R6 thru R8	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R9	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R10 and R11	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R12 and R13	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R14	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R15	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.

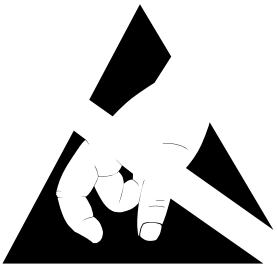
SYMBOL	PART NUMBER	DESCRIPTION
R16 and R17	19B800607P273	Metal film: 27K ohms ±5%, 1/8 w.
R18	19B800607P332	Metal film: 3.3K ohms ±5%, 1/8 w.
R19 and R20	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R21	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R22 thru R29	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R30	19B800607P273	Metal film: 27K ohms ±5%, 1/8 w.
R31	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R32 and R33	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R34	19A702931P401	Metal film: 100K ohms ±1%, 1/8 w.
R35 thru R38	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R40	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R41	19B800607P122	Metal film: 1.2K ohms ±5%, 1/8 w.
R42 thru R49	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R54 thru R61	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R66 thru R78	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R79	19B800607P222	Metal film: 2.2K ohms ±5%, 1/8 w.
R80	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R85 thru R91	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R96 thru R103	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R105 and R106	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R111 thru R118	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R123 thru R133	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R138 thru R151	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R152	19A702931P269	Metal film: 5110 ohms ±1%, 1/8 w.
R153	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R154 thru R157	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R158 thru R165	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R166 thru R169	19A702931P176	Metal film: 604 ohms ±1%, 1/8 w.
R170 thru R172	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R173	19B800607P1	Metal film: Jumper.

SYMBOL	PART NUMBER	DESCRIPTION
R174 thru R177	19A702931P401	Metal film: 100K ohms ±1%, 1/8 w.
R178	19B800607P273	Metal film: 27K ohms ±5%, 1/8 w.
R179	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R180	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R182	19A702931P409	Metal film: 121K ohms ±1%, 1/8 w.
R183	19A702931P165	Metal film: 464 ohms ±1%, 1/8 w.
R184	19A702931P285	Metal film: 7500 ohms ±1%, 1/8 w.
R185	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R186 thru R189	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R190	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R191 thru R194	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R195	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R196 thru R199	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R200	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R201 thru R204	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R205	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R206 thru R209	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R210	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R211 thru R214	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R215 thru R218	19A702931P176	Metal film: 604 ohms ±1%, 1/8 w.
R220 thru R225	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R227	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R228 thru R231	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R232 thru R235	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R236 and R237	19A702931P176	Metal film: 604 ohms ±1%, 1/8 w.
R238 and R239	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R240 and R241	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R242	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R244 thru R248	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R250 thru R254	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R255 and R256	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R270	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.

SYMBOL	PART NUMBER	DESCRIPTION
R271 and R272	19B800607P222	Metal film: 2.2K ohms ±5%, 1/8 w.
R281	19B800607P273	Metal film: 27K ohms ±5%, 1/8 w.
R282	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R283 and R284	19A702931P176	Metal film: 604 ohms ±1%, 1/8 w.
R285	19B800607P1	Metal film: Jumper.
R286	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R287	19B800607P1	Metal film: Jumper.
R288	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R289	19A702931P176	Metal film: 604 ohms ±1%, 1/8 w.
R290	19B800607P221	Metal film: 220 ohms ±5%, 1/8 w.
R301 thru R303	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R304	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R305 and R306	19B800607P182	Metal film: 1.8K ohms ±5%, 1/8 w.
R307 and R308	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R309 thru R312	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R344 thru R347	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
		---------- SWITCHES ----------
SW1	19A149955P1	DIP, rocker: 8-position; sim to Grayhill 76PSB08S.
SW2	19A149923P2	Pushbutton: Single-Pole Normally-Open; sim to ITT Schadow KSLOV311.
		---------- TEST POINTS ----------
TP1 thru TP17	344A3367P1	Metal loop w/orange insulator.
		---------- INTEGRATED CIRCUITS ----------
U1	19A149880P1	Digital: 16-Bit Microprocessor; sim to 80C186.
U2 and U3	19A703471P318	Digital: Octal Tri-State Transceiver/Latch; sim to 74HC573.
U4	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U5	19A703483P304	Digital: Hex Inveter; sim to 74HC04.
U6	19A703483P311	Digital: CMOS Quad 2-Input OR Gate; sim to 74HC32.
U7	344A3059P201	Digital: UART; sim to Signetics SCC2691A.
U8	19A703483P301	Digital: Quad 2-Input NOR Gate; sim to 74HC02.
U9 and U10	19A703471P318	Digital: Octal Tri-State Transceiver/Latch; sim to 74HC573.
U11	19A704380P321	Digital: Monostable Multivibrator; sim to 74HC123.
U12	19A703483P305	Digital: Quad 2-Input AND Gate; sim to 74HC08.
U13	19A149895P1	Digital: Microprocessor Supervisory; sim to MAX691C.
U14	19A703471P308	Digital: Octal Bus Transceiver; sim to 74HC245.
U15	19A703483P304	Digital: Hex Inveter; sim to 74HC04.
U20 and U21	344A3067P1	Digital: 128K x 8-Bit Nonvolatile RAM; sim to DS1245Y-120.
U22 and U23	19A705981P2	Digital: 32K x 8-Bit Static RAM; sim to HM62256-12.
U26	350A1591G1	Digital: 128K x 8-bit PEROM (Programmed).
U27	350A1588G1	Digital: 128K x 8-bit PEROM (Programmed).
U28 thru U30	19A703483P311	Digital: CMOS Quad 2-Input OR Gate; sim to 74HC32.
U31	19A703483P304	Digital: Hex Inveter; sim to 74HC04.
U32 and U33	19A149956P1	Digital: Serial Communication Controller; sim to 82525N.
U41 thru U48	RYT121355/C	Digital: Memory Time Switch, CMOS; sim to PEB2045.
U49	19A703483P304	Digital: Hex Inveter; sim to 74HC04.
U50	19A149953P202	Digital: 4-Channel Futurebus Transceiver; sim to DS3897.
U51	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U53 and U54	19A703471P322	Digital: Dual 4-Input Data Selector; sim to 74HC153.
U55 and U56	19A704380P321	Digital: Monostable Multivibrator; sim to 74HC123.
U57	19A703483P320	Digital: Dual 4-Input AND Gate; sim to 74HC21.
U58	RYT3041046/3C	Digital: PLL w/ VCO; sim to 74HCT4046A.
U59	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U60	19A149953P201	Digital: 8-Channel Futurebus Transceiver; sim to DS3896.
U65	19A703483P305	Digital: Quad 2-Input AND Gate; sim to 74HC08.
U70 thru U75	19A149953P202	Digital: 4-Channel Futurebus Transceiver; sim to DS3897.
U76 thru U79	19A703483P304	Digital: Hex Inveter; sim to 74HC04.
U84	19A703483P305	Digital: Quad 2-Input AND Gate; sim to 74HC08.
U85	344A3323P1	Digital: Advanced CMOS Frame Aligner; sim to PEB2035N-VC1.
U86	RYT109080/C	Digital: ISDN Primary Access Transceiver; sim to PEB2236.
U87	19A149953P202	Digital: 4-Channel Futurebus Transceiver; sim to DS3897.
U88	344A3379P101	Digital: T1/CEPT Dual Digital PLL; sim to MT8941A.
U89 and U90	19A703471P318	Digital: Octal Tri-State Transceiver/Latch; sim to 74HC573.
U91 and U92	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.

SYMBOL	PART NUMBER	DESCRIPTION
U94 thru U99	350A1585G1	Digital: Field Programmable Gate Array; sim to Actel A1240.
U100	RYT1096075/1	Digital : Octal RS-232/423 Line Driver; sim to NE5170A.
U101	RYT1096074/1	Digital: Octal RS-232/423 Line Receiver; sim to NE5180A.
U102	RYT1096075/1	Digital : Octal RS-232/423 Line Driver; sim to NE5170A.
U103	RYT1096074/1	Digital: Octal RS-232/423 Line Receiver; sim to NE5180A.
U104 and U105	19A703471P305	Digital: Quad 3-State Buffer; sim to 74HC126.
U110	19A703483P319	Digital: 4-Bit Magnitude Comparator; sim to 74HC85.
U111	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U112 thru U114	19A703471P318	Digital: Octal Tri-State Transceiver/Latch; sim to 74HC573.
U115	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U120	19A703471P305	Digital: Quad 3-State Buffer; sim to 74HC126.
U122	19A134717P2	Linear: 12-Volt Regulator: sim to MC7812CT.
U123	19A134718P2	Linear: -12-Volt Regulator; sim to uA7912U.
U124	344A3039P201	Digital: Driver/Receiver, EIA-232D/V.28; sim to MC145406.
U125 thru U128	RYT1016213/01	Linear: High-Speed Voltage Follower; sim to LM310M.

SYMBOL	PART NUMBER	DESCRIPTION
		---------- FUSE SOCKETS ----------
XF1 thru XF6	19A116688P2	Clip, Fuse: sim to Littelfuse 111501.
		---------- SOCKETS ----------
XU1	344A3339P5	Socket, IC: 68-pin PLCC surface mount; sim to AMP 822070-4.
XU20 and XU21	19A700156P17	Socket, IC: 32-pin, low-profile; sim to AMP 2-644018-3.
XU24 and XU25	19A700156P3	Socket, IC: 28-pin, tin plated.
XU26 and XU27	19A700156P17	Socket, IC: 32-pin, low-profile; sim to AMP 2-644018-3.
XU94 thru XU99	344A3339P7	Socket, IC: 84-pin, PLCC surface mount; sim to AMP 822152-1.
		---------- CRYSTALS ----------
Y1	19A702511G45	Quartz: 25 MHz.
Y2	19A702511G9	Quartz: 3.6864 MHz.
Y3	19A702511G5	Quartz: 11.5200 MHz.
Y4	RTL201614/1	Oscillator, TTL: 12.352 MHz.
Y5	RTL201614/2	Oscillator, TTL: 16.384 MHz.
		---------- MISCELLANEOUS ----------
	19C852616P1	Panel, front: aluminum, lettered.
		Handles, extraction, w/brackets: sim to Scanbe 60760-01.



CAUTION

OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

T1/E1 INTERFACE CARD
188D5909P1

OUTLINE AND SCHEMATIC DIAGRAMS

(Inside)

ERICSSON

Ericsson Inc.
Private Radio Systems
Mountain View Road
Lynchburg, Virginia 24502
1-800-528-7711 (Outside USA, 804-528-7711)

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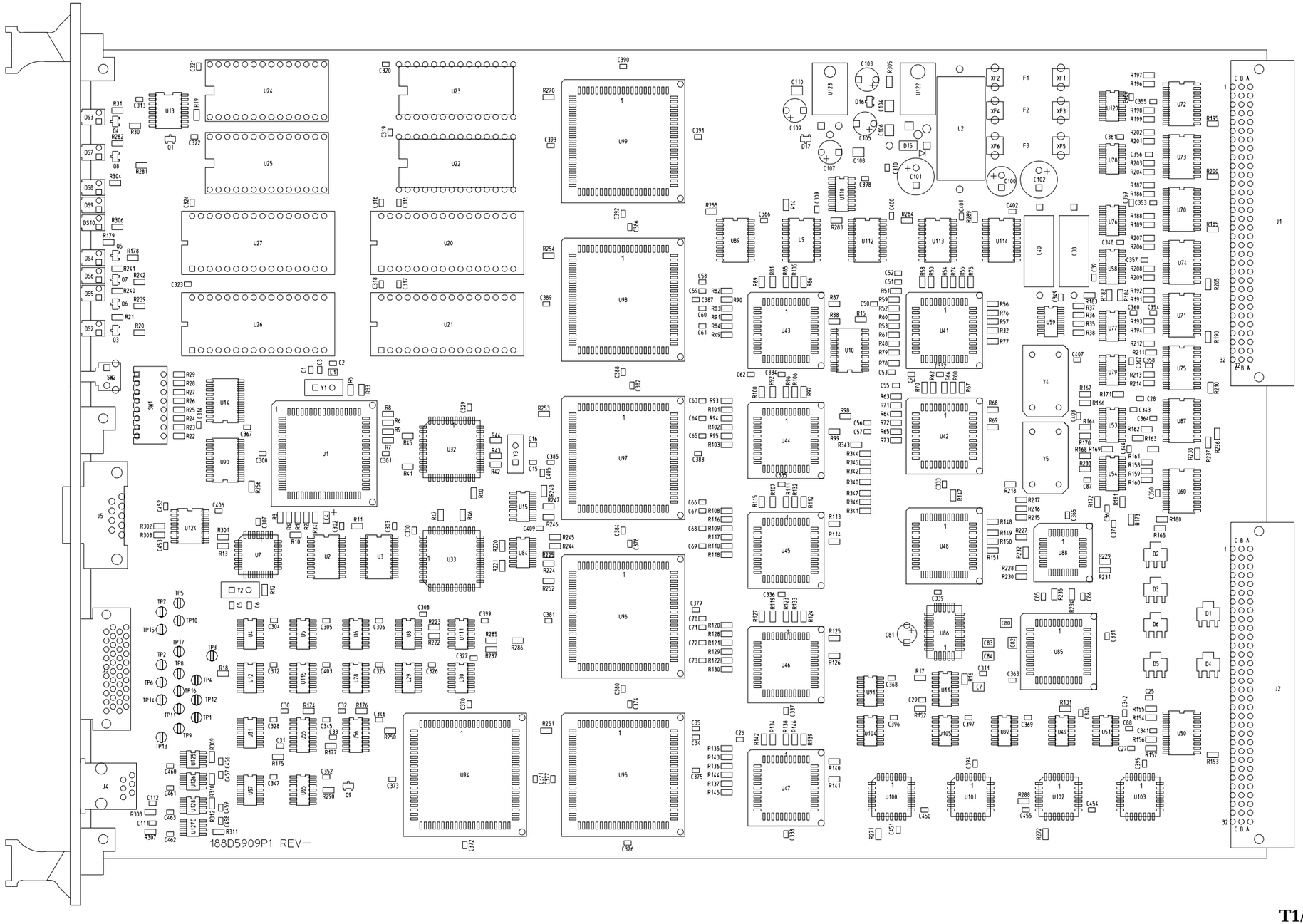
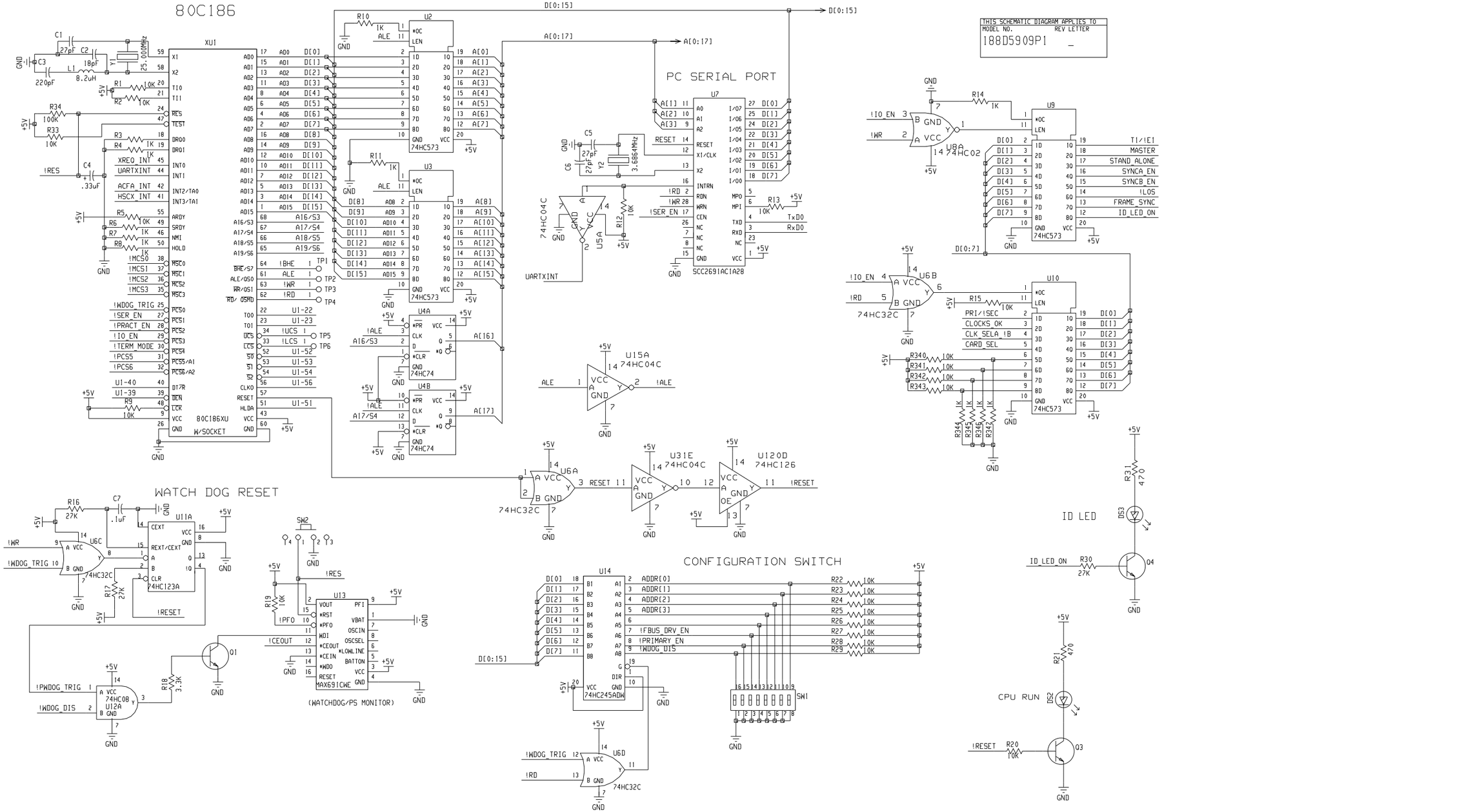


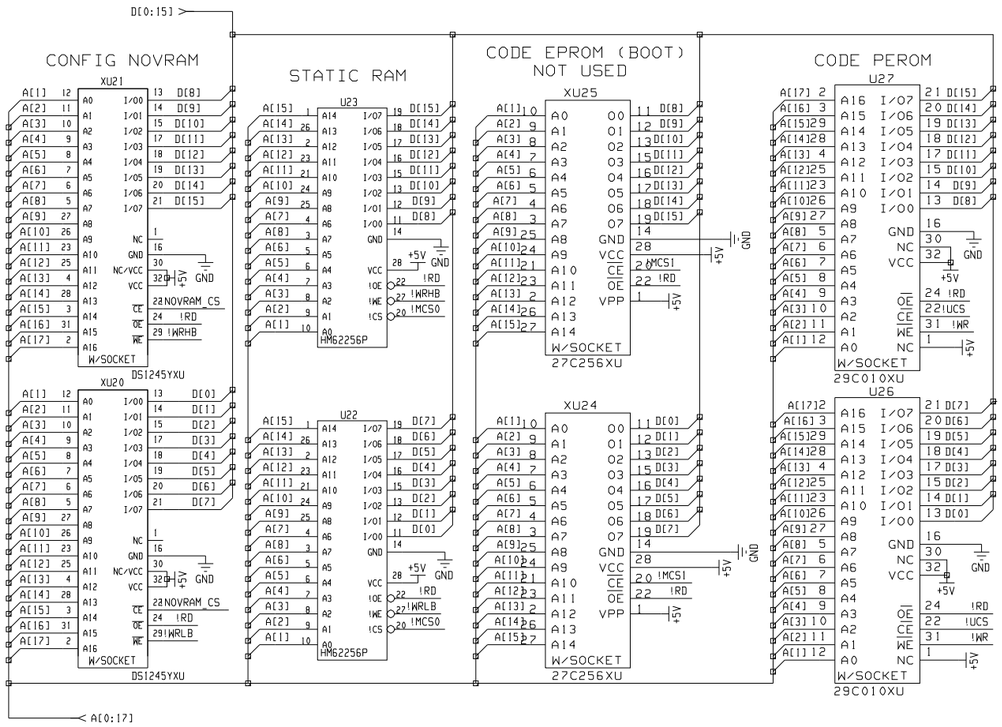
T1/E1 Interface Card
188D5909P1

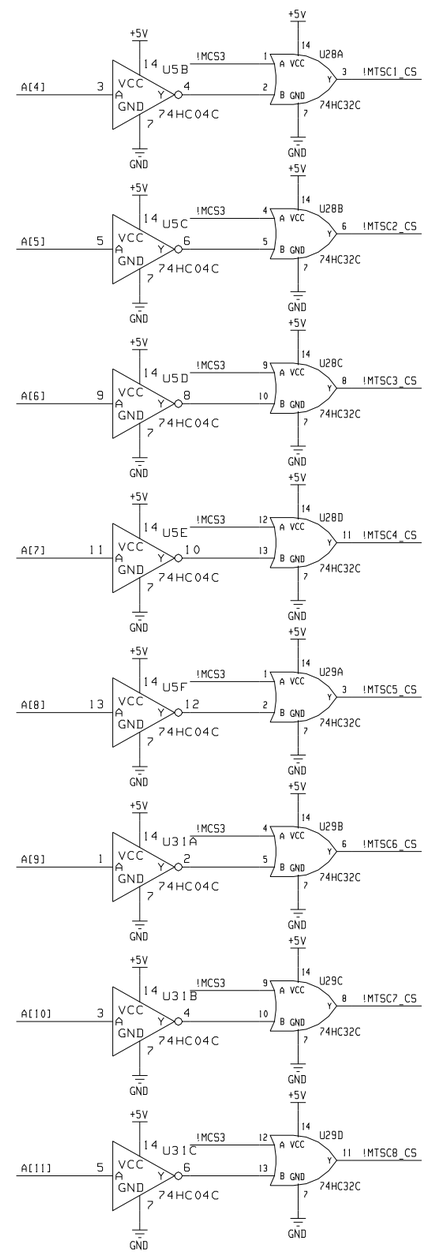
(188D5909, Rev. 3)

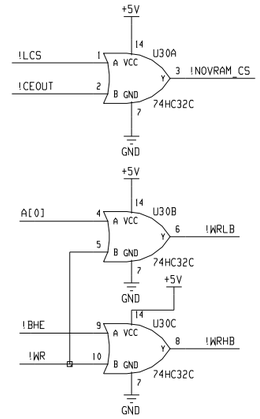


T1/E1 Interface Card
188D5909P1
Sheet 1 of 10

(188D5907 Sh. 1, Rev. 1A)

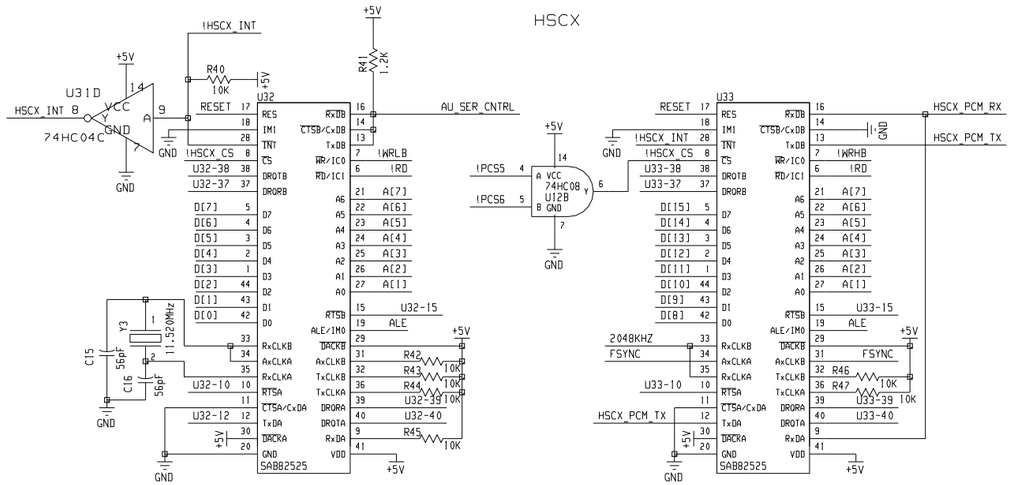






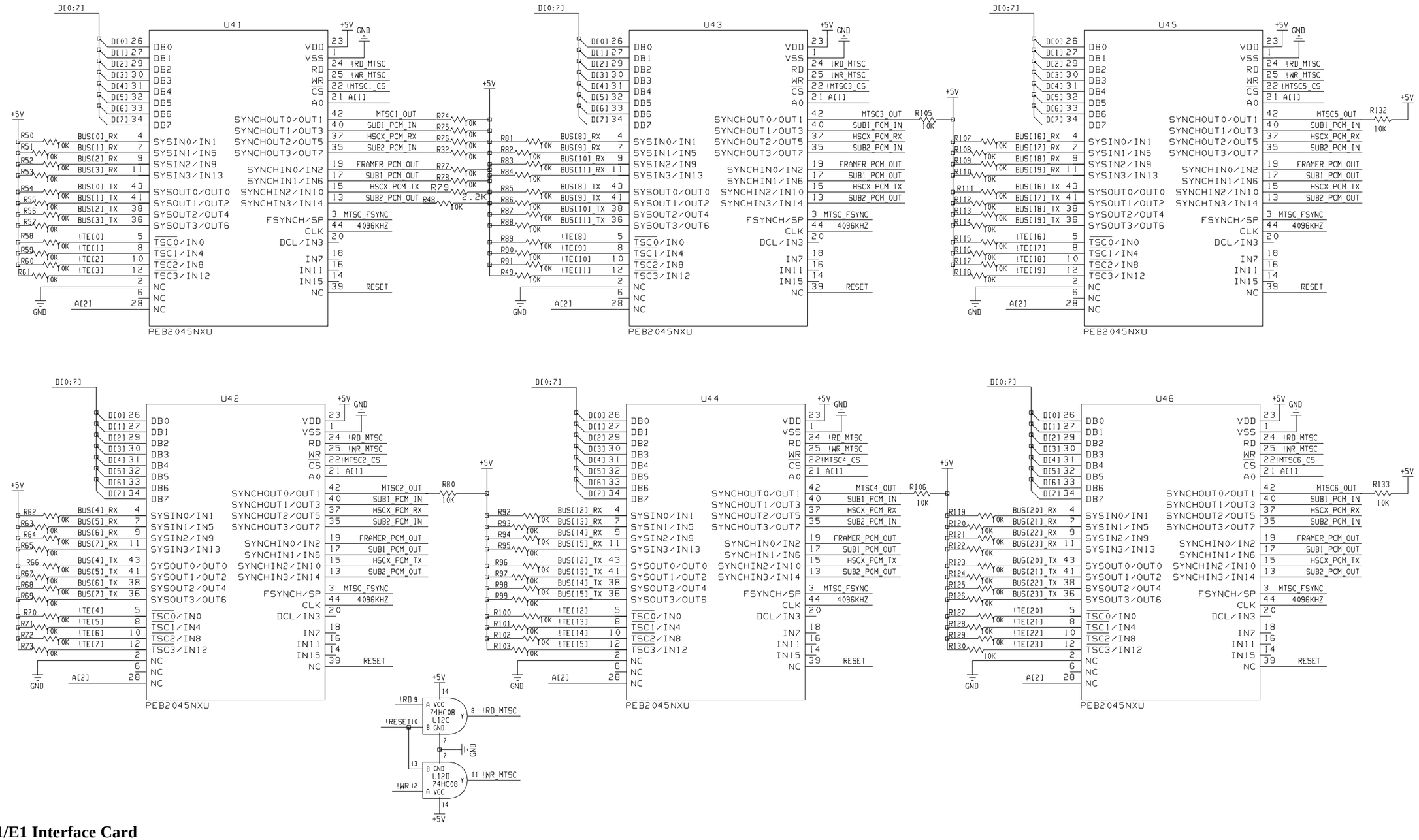
MEMORY MAP

```
CONFIG NOVRAM  : [00000-3FFFFH EVEN]          (LCS)
UNUSED         : [90000-9FFFFH]               (MCS1)
CODE PEROM     : [C0000-FFFFFH]               (UCS)
STATIC RAM     : [80000-BFFFFH]               (MCS0)
WATCH DOG      : [40000-4007FH] WRITE ONLY    (PCS0)
uP SERIAL PORT : [40080-400FFH EVEN]          (PCS1)
LINE FRAMER    : [A0000-AFFFFH EVEN]          (MCS2)
LINE INTERFACE : [40100-401?FH]               (PCS2)
DIP SWITCH     : [40000-4007FH] READ ONLY     (PCS0)
HSCX CONT. 2   : [40280-4037FH ODD]           (PCS5,6)
HSCX CONT. 1   : [40280-4037FH EVEN]          (PCS5,6)
MTSC1          : [B0010-B001FH EVEN]          (MCS3)
MTSC2          : [B0020-B003FH EVEN]          (MCS3)
MTSC3          : [B0040-B007FH EVEN]          (MCS3)
MTSC4          : [B0080-B00FFH EVEN]          (MCS3)
MTSC5          : [B0100-B01FFH EVEN]          (MCS3)
MTSC6          : [B0200-B03FFH EVEN]          (MCS3)
MTSC7          : [B0400-B07FFH EVEN]          (MCS3)
MTSC8          : [B0800-B0FFFH EVEN]          (MCS3
I/O PORT       : [4018O-401FFH]               (PCS3)
TERM. PORT MODE: [40200-4027FH]               (PCS4)
UNUSED         : [403B0-7FFFFH, B1000-BFFFFH]
```



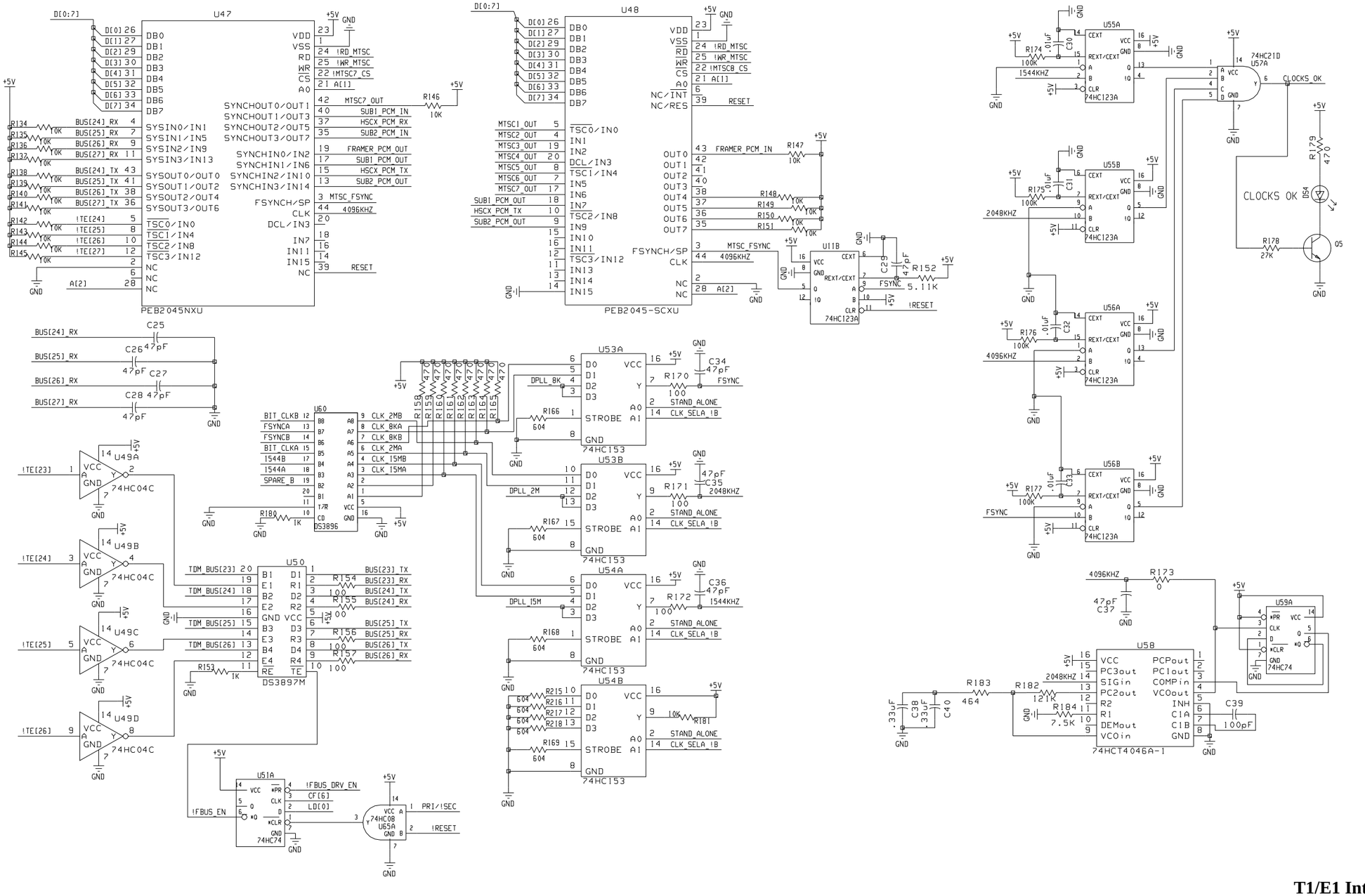
T1/E1 Interface Card
188D5909P1
Sheet 2 of 10

(188D5907 Sh. 2, Rev. 1A)



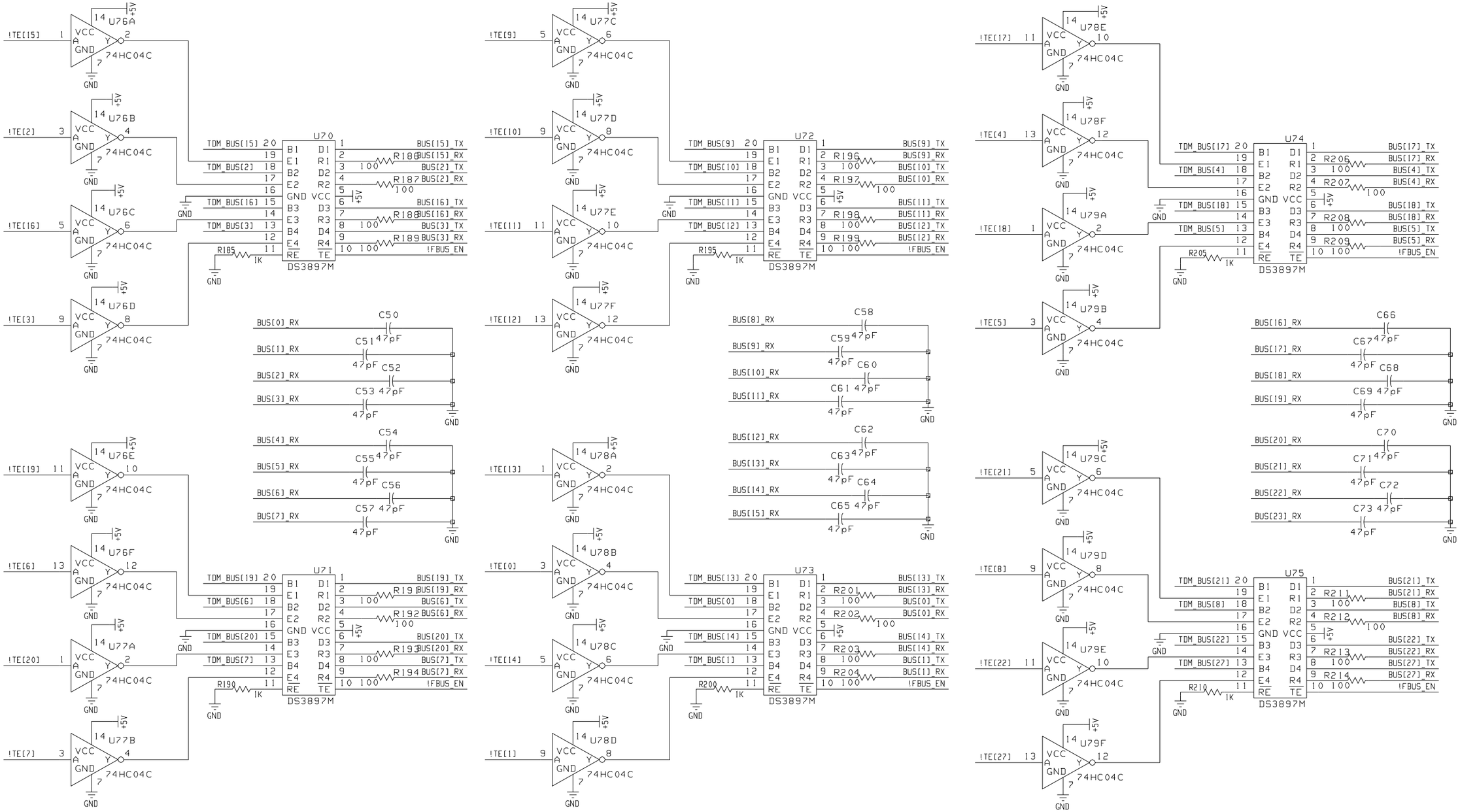
T1/E1 Interface Card
188D5909P1
Sheet 3 of 10

(188D5907 Sh. 3, Rev. 1A)



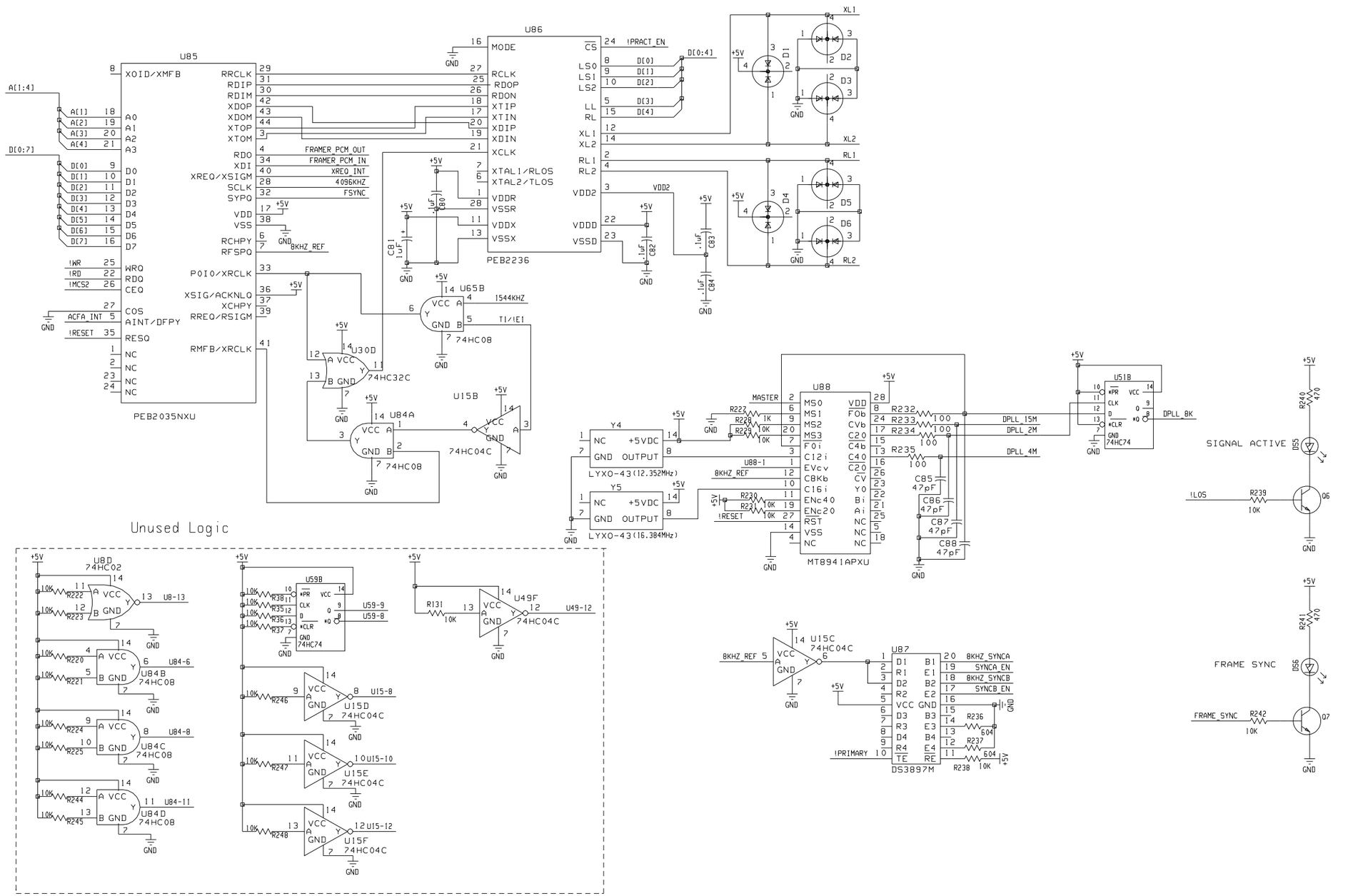
T1/E1 Interface Card
188D5909P1
Sheet 4 of 10

(188D5907 Sh. 4, Rev. 1A)



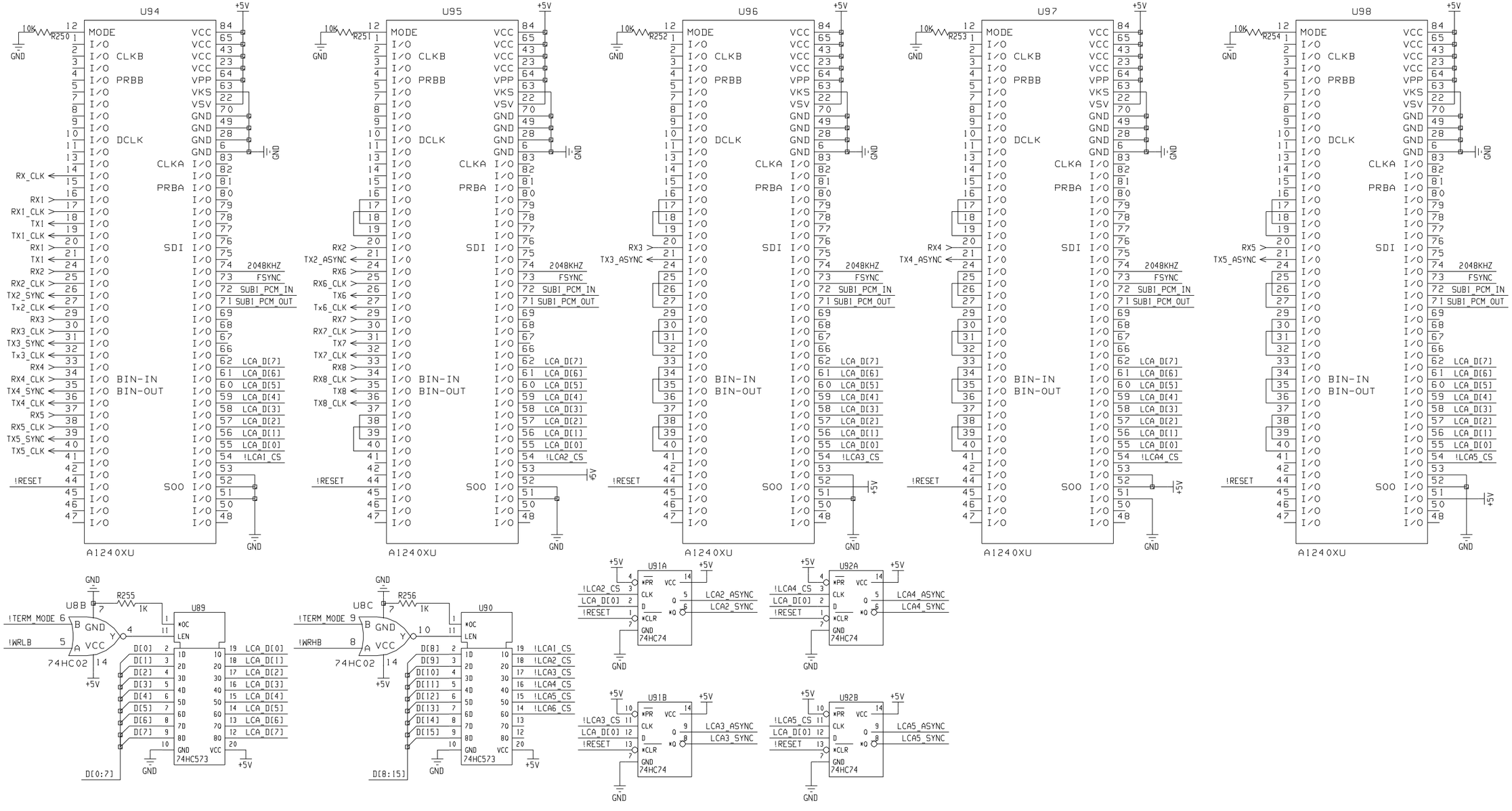
T1/E1 Interface Card
188D5909P1
Sheet 5 of 10

(188D5907 Sh. 5, Rev. 1A)



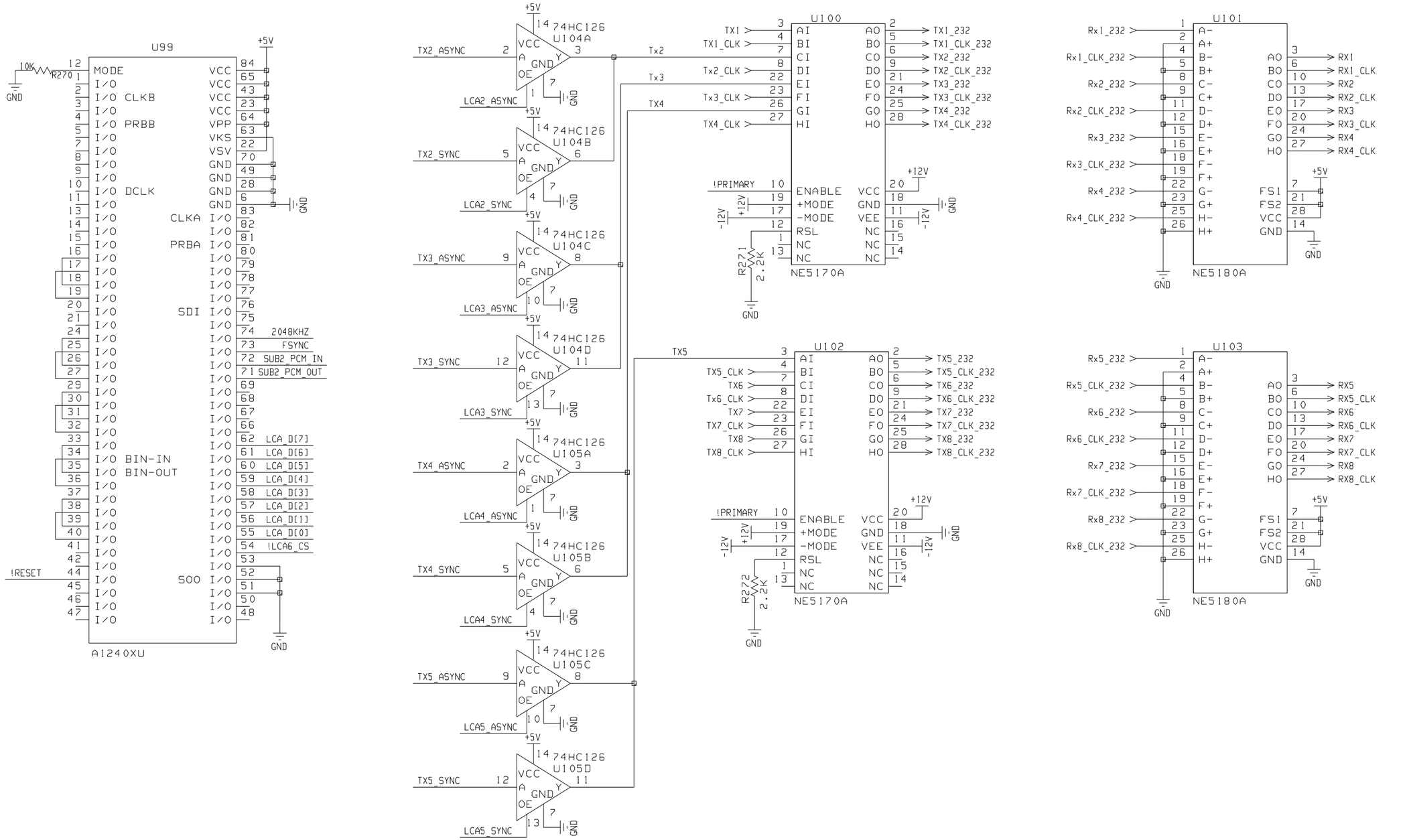
T1/E1 Interface Card
188D5909P1
Sheet 6 of 10

(188D5907 Sh. 6, Rev. 1A)



T1/E1 Interface Card
188D5909P1
Sheet 7 of 10

(188D5907 Sh. 7, Rev. 1A)



T1/E1 Interface Card
188D5909P1
Sheet 8 of 10

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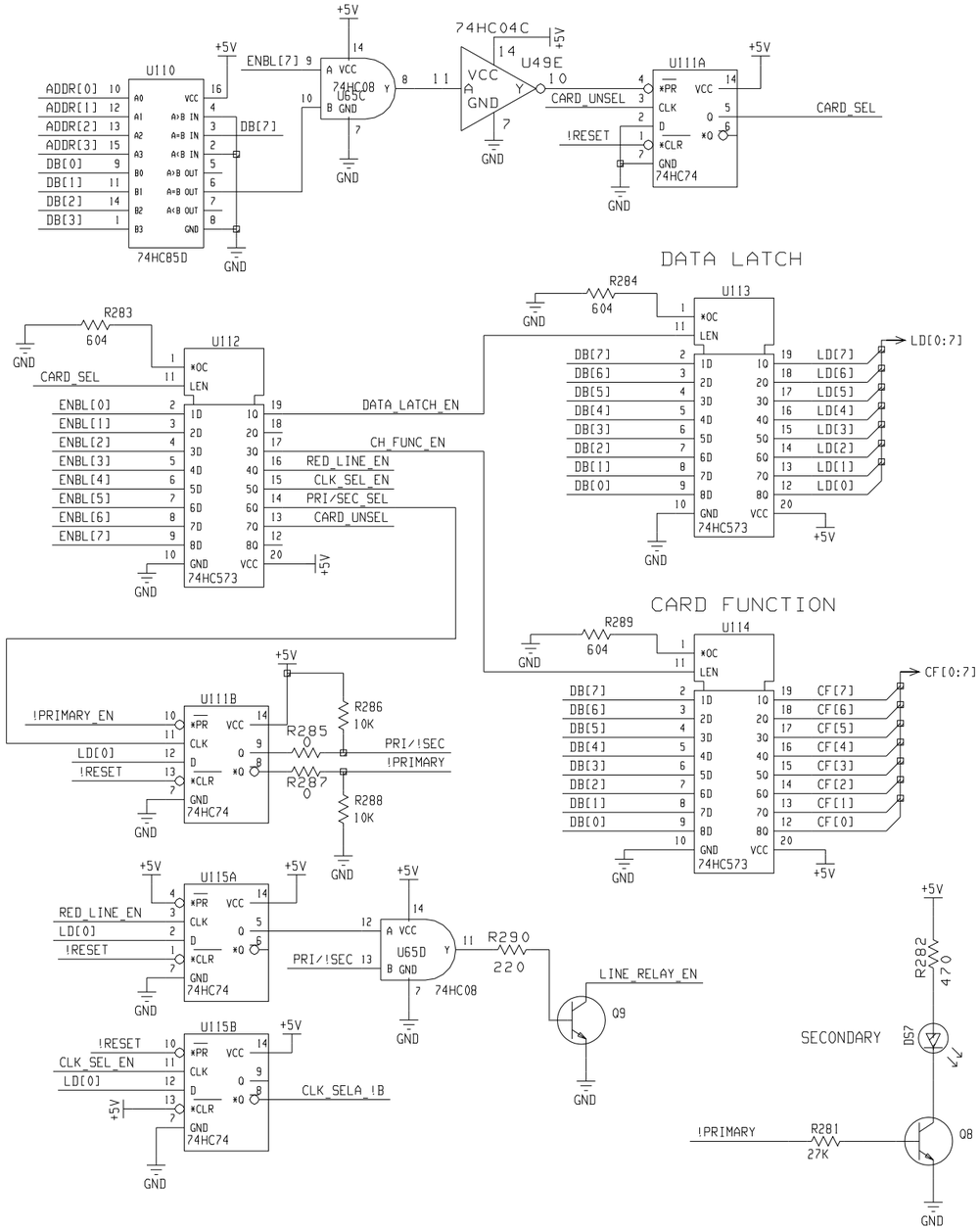

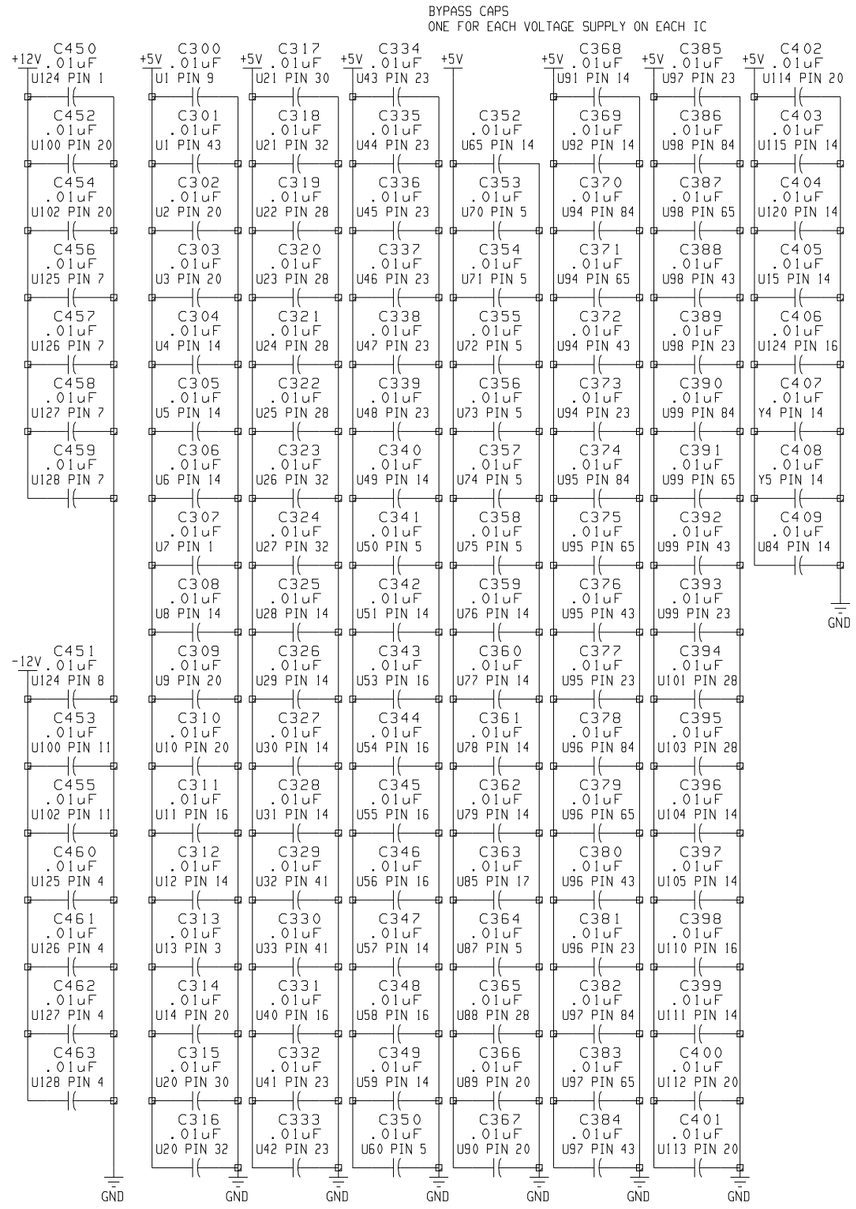

T1/E1 Interface Card
188D5909P1
Sheet 9 of 10

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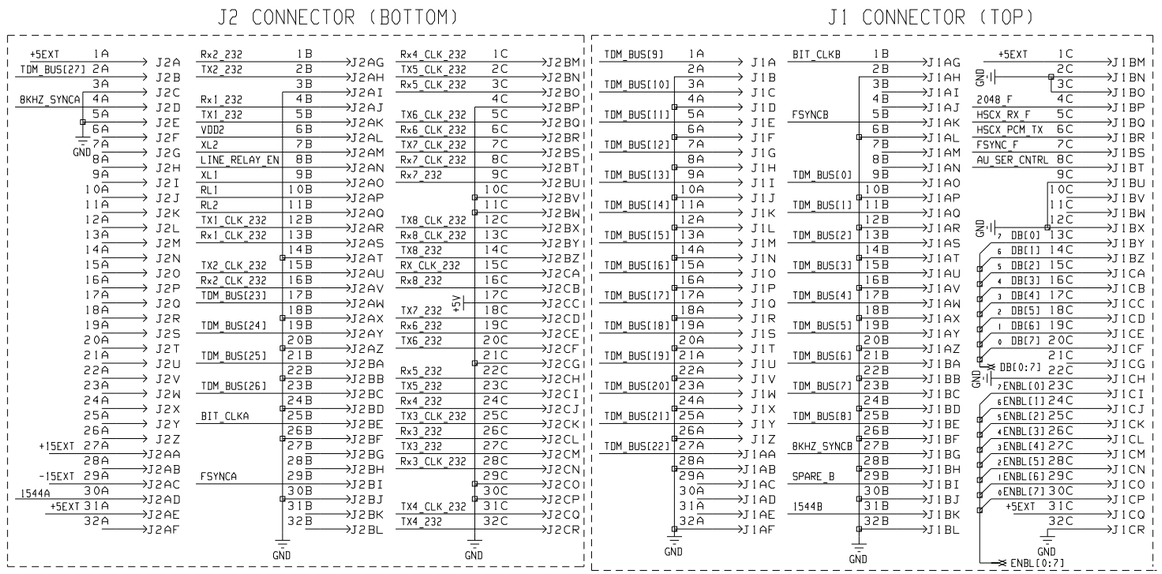

T1/E1 Interface Card
188D5909P1
Sheet 10 of 10

(188D5907 Sh. 10, Rev. 1A)