

MAINTENANCE MANUAL
CONTROL LOGIC/IF BOARD
CMC-855
NOISE BLANKER
CFG-138

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NOTE

Repairs to this equipment should be made only by an authorized service technician or facility designated by the supplier. Any repairs, alterations or substitution of recommended parts made by the user to this equipment not approved by the manufacturer could void the user's authority to operate the equipment in addition to the manufacturer's warranty.

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DESCRIPTION

The System Control Logic/IF circuit board combines functions of the receive circuit 1st IF, 2nd IF, audio detection, audio signal processing and control logic on one circuit board. As an option, an additional circuit board can be plugged into this board to provide **AEGIS** (digital encryption system). Programming and personality information is stored in **FLASH** and **EEPROM** memory on the logic/IF board. The audio speaker amplifier is also part of the same board. Also as an option, an additional circuit board is available to provide noise blanking.

Electrical interfaces are achieved between this board and the Control Unit (LCC), synthesizer, RF PA (APC) and the Option and Remote Control Connector (ORCC) on the rear of the assembled radio.

All radio control signals originate or terminate on the control logic/IF board. Two microcomputers share the processing load. Control signals are connected through a high speed digital link with the control unit, either through the LCC or ORCC connectors, making possible either front or remote control for the radio. The same link also makes possible dual radio or dual control head configuration. An RS-232 compatible digital link is available at the ORCC interface, to facilitate programming or Radio Data Interface to Mobile Digital terminals.

This circuit board also generates Type 99, Channel Guard, GE-Star and DTMF signals if so programmed

The System Control Logic/IF board consists of the following control logic, IF and audio circuits (see figures 1 & 2).

CONTROL LOGIC SECTION (CMC-682)

- CMOS Microprocessor (IC701, IC702)
- Custom CMOS ASIC Chip (IC703)
- Address Decoder (IC704)
- RS-485 (IC705)
- RS-232 (IC706)
- Flash EEPROM (IC707)
- EEPROM (IC708)
- CMOS SRAM (IC709)
- CMOS Inverters (IC711)
- Silicon Serial Number (IC712)
- TTL Inverters (IC713)

IF SECTION (CMF-132)

- Custom CMOS ASP Chip (IC601)
- Operational Amplifier (IC602, IC603)
- Audio Amplifier (IC604)
- 5 Volt Regulator (IC606, IC607)
- 9 Volt Regulator (IC605, IC608, IC609)
- Reset Circuit (IC610)
- Bilateral Switch (IC611, IC612)

CIRCUIT ANALYSIS

CONTROL LOGIC SECTION (CMC-855)

Microcomputer

The main microcomputer circuit in the **ORION** radio consist of microprocessor IC701, EEPROM IC708, Flash EEPROM IC707, RAM IC709 and custom ASIC IC703. This circuitry runs at a 9.8304 MHz rate determined by crystal X701 and controls the radio through a second microprocessor IC702. This second microprocessor runs at a 4.9152 MHz rate. The 4.9152 MHz rate is determined by ASIC IC703.

- Controlling the **ASIC**, **FLASH EEPROM** and **RAM**
- Loading data to the frequency synthesizer
- Fetching and processing the PTT, monitor, channel, selection and volume control
- Controlling the audio circuit (processor)
- Decoding the squelch
- Encoding/Decoding the Channel Guard and Digital Channel Guard
- Controlling the loading interface for the radio data (channel number and signaling)

Flash EEPROM (IC707)

This memory contains the software to control the microprocessor. This Flash EEPROM has a storage capacity of 512k x 8 bits.

CMOS SRAM (IC709)

This SCRATCH RAM has a storage capacity of 32k x 8 bits. The memory is available for variables, buffers, etc.

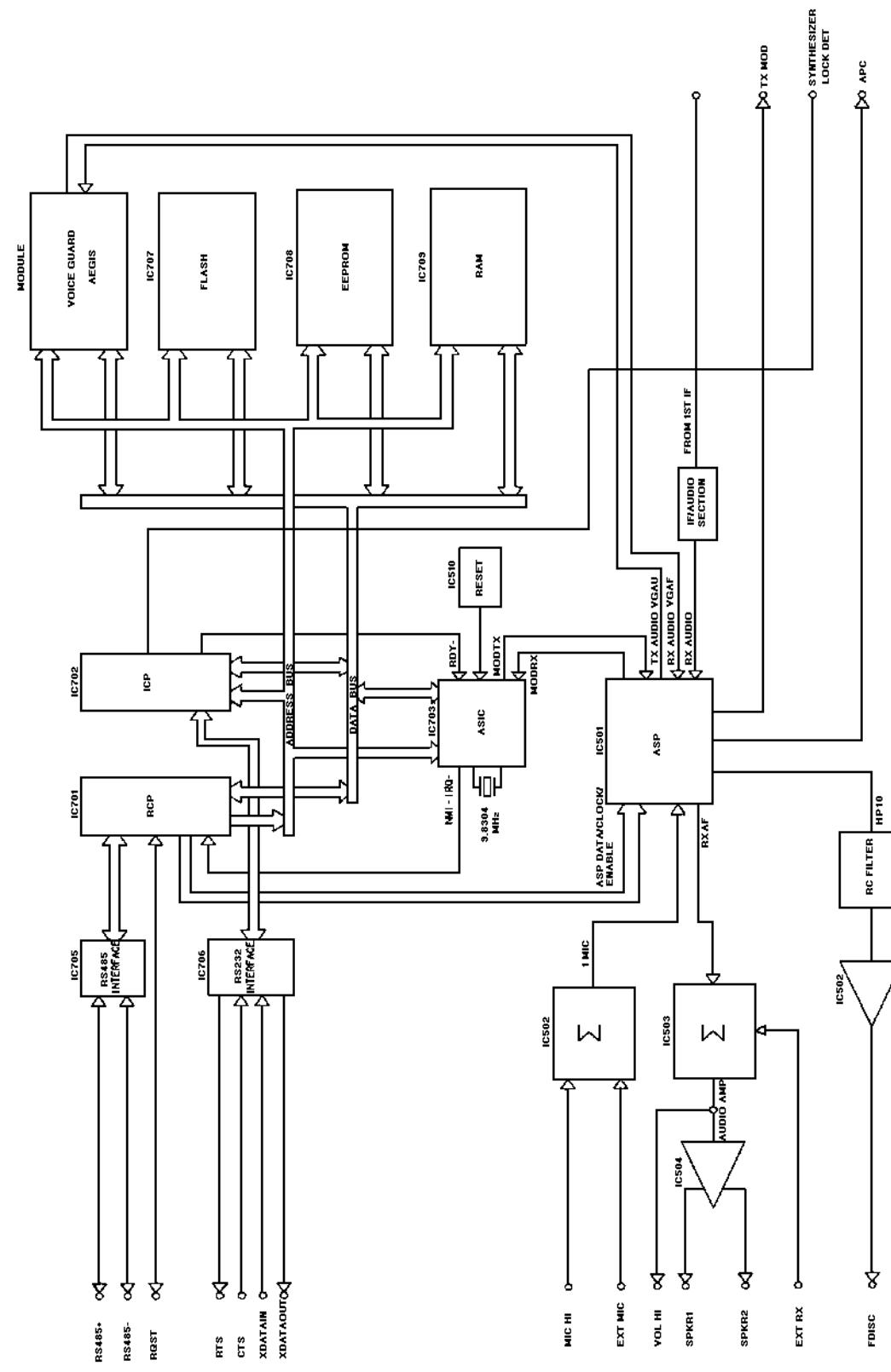


Figure 1 - Control Logic Section Block Diagram

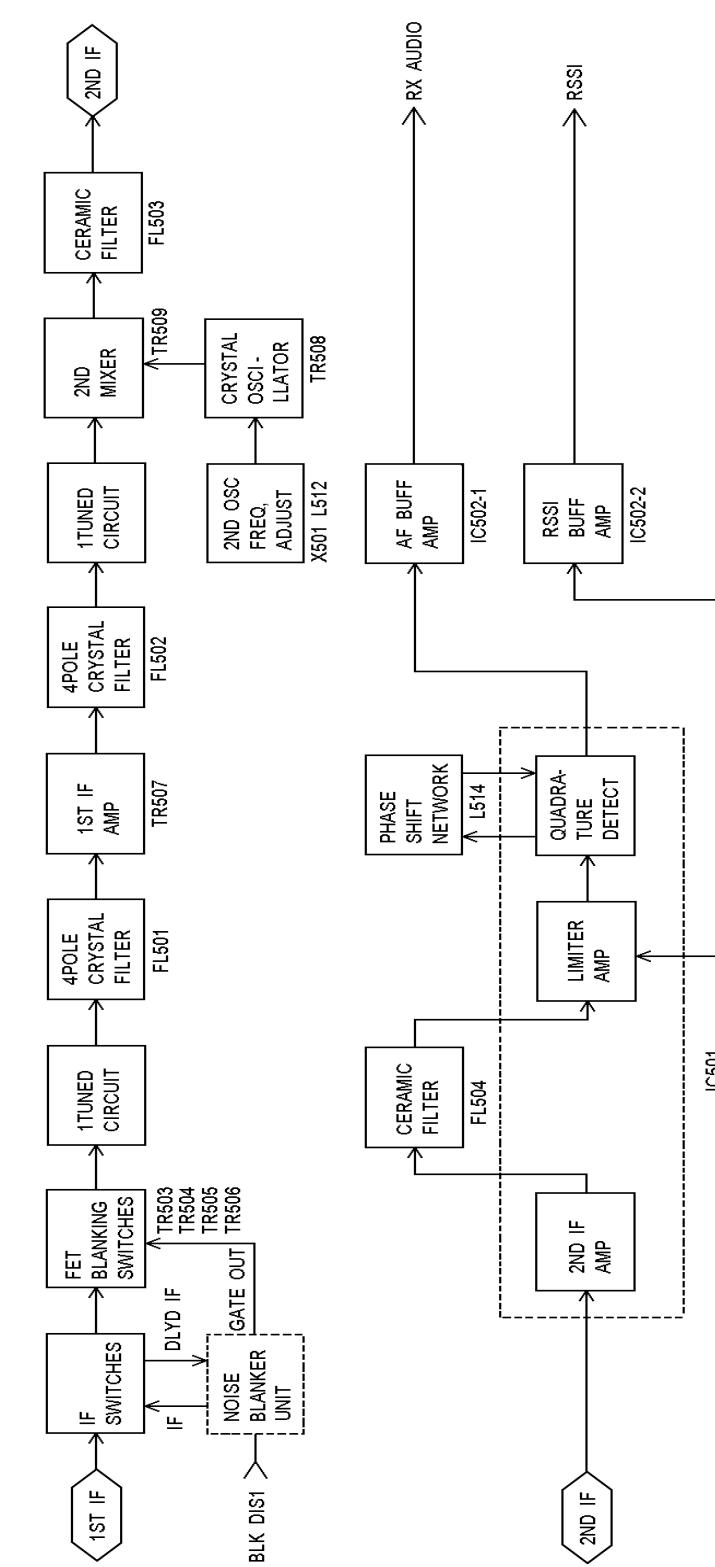


Figure 2 - 20.8 MHz IF Section Block Diagram

EEPROM (IC708)

This EEPROM has a storage capacity of 8k x 8 bits. The memory contains the user configurable parameters that must be maintained through a power cycle. This personality controls various functions of the radio. The personality data is entered from outside the radio through the ORCC connector to the microprocessor and then to the EEPROM.

The data mainly consists of the following:

- Channel Frequency Data
- CG/DCG Data
- Tx Power, Tx Modulation Data
- Squelch Data
- Display Data, etc.

Application Of Specific Integrated Circuits

ASIC (IC703)

The ASIC is basically a chip that integrates many miscellaneous functions. The chip provides functions as follows:

- MODEM
- Watch Dog Timer
- Clock Control
- Interrupt Control
- Address Decode etc.

Voltage Regulators (IC606, IC607) (IC605, IC608, IC609)

Voltage regulators IC606 and IC607 each generate a 5 Vdc for the Control Board. Voltage regulators IC605, IC608 and IC609 each generate a 9 Vdc for the Control Board and Voice Guard Adapter Module.

Audio Amplifier (IC604)

The audio amplifier is located between the audio processor and the speaker. Amplifier IC604 amplifies the output signal of the ASP (IC601) to the level adequate for driving the speaker.

Audio Signal Processor (ASP) (IC601)

The audio process consists of a one-chip IC accommodating almost all of the audio functions. The audio functions are under control of the microcomputer in compliance with the function of the radio unit.

The functions of the audio processor are as follows:

- Rx Audio process with Tone Reject Filter, De-emphasis and Programmable Attenuator.
- CG/DCG filtering and limiting
- Noise Squelch filtering and detecting
- 8 bits D/A Converter with sample and hold
- Tx audio process with microphone amplifier, pre-emphasis, deviation limiter, summing amplifier, post limiter filter and programmable attenuator
- Two 6 bits programmable divider for clock and alert tone

All of these functions are made up of switched capacitor filters, amplifiers and timing logic. The timing for this logic is derived from the 4.9152 MHz clock generator (ASIC).

RS-485 (IC705)

This is a high speed differential TRI-STATE bus/line transceiver designed to meet the requirements of EIA standard RS-485 specification. The IC705 is located between the Radio Unit and the Control Unit, and controls signalling between these points.

RS-232 (IC706)

In Low Band ORION, the RS-232 port is used for programming the radio. This port is controlled by IC706. This IC consists of line drivers/receivers designed to meet the requirements of EIA standard RS -232 specifications. The IC706 is located between the radio unit and the ORCC.

Reset Circuit (IC610)

This is an active low reset IC which includes a delay time generating circuit. Delay time can be set up by externally using a capacitor and a resistor. The function of this IC is to accurately reset the system after detecting voltage at the time of switching power on and instantaneous power off.

Option and Remote Control Connector (ORCC)

The ORCC is located on the rear of the radio and is used for options and accessories when Control Unit and Radio Unit are directly attached and for remote control in all other configurations. The ORCC allows various kinds of external equipment connections to be made. External equipment connecting signals are as follows:

| PIN | SIGNAL | PIN | SIGNAL |
|-----|-----------|-----|-----------|
| 1 | SUP GND | 20 | RTS |
| 2 | XDATA IN | 21 | INP1 |
| 3 | XDATA OUT | 22 | OUT1 |
| 4 | RS485+ | 23 | INP2 |
| 5 | RS485- | 24 | IGN A+ |
| 6 | CTS | 25 | SW + |
| 7 | GND | 26 | HKS W |
| 8 | FPROG | 27 | EXTMIC |
| 9 | OUT2 | 28 | EXTRX |
| 10 | IGN SEN | 29 | FDISC |
| 11 | MIC HI | 30 | EXTALO |
| 12 | ALO | 31 | CUTST |
| 13 | VOL HI | 32 | SPARE |
| 14 | CTL ON | 33 | SPARE |
| 15 | XTONENC | 34 | SPARE |
| 16 | XTONEDEC | 35 | S DATA |
| 17 | RQST | 36 | SONOFF |
| 18 | SPKR1 | 37 | HORN RING |
| 19 | SPKR2 | | |

20.8 MHz IF SECTION (CMF-132)

1st IF

The 20.8 MHz 1st IF output signal is coupled from the output of the first mixer circuit, located on the Synthesizer/Receiver board, through 30-pin connector P501-1 and capacitor C501 to the source input of buffer amplifier Junction Field Effect Transistors (JFET) TR501 and TR502. This input can be monitored at test point TP1. The output of TR501 and TR502 is coupled through capacitor C502 to the input of the optional noise blunker. If the noise blunker is not in the circuit, the input is connected through capacitor C538 to switchable networks through diodes CD501, CD502 and CD503. The output of the switchable networks connects through impedance matching network L504, L506 and associated circuit (by-passing IF blanking FET's TR503 and TR506) to 4-pole crystal band-pass filter FL501. The highly-selective crystal filters FL501-1 and FL502-2 provide the first part of receiver IF selectivity. The output of the filters is coupled through the impedance matching network consisting of inductor L508, capacitors C515 and C516, and resistor R513 to the base of 1st IF amplifier transistor TR507. The amplified signal is taken from the collector of TR507 and connected through an impedance matching network consisting of inductor L509, capacitor C520 and resistor R518 to the input of 4-pole crystal filter FL502. Crystal filters FL502-1

and FL502-2 provide the second part of receiver IF selectivity. The output of the crystal filters is coupled through an impedance-matching network consisting of inductor L511, capacitor C523, resistor R519 and coupling capacitor C523 to the base of 2nd IF amplifier transistor TR509.

2nd Mixer

The 20.8 MHz IF input is applied to the base of transistor TR509 and mixed with a 20.345 MHz frequency supplied by a crystal oscillator circuit consisting of X501 and oscillator transistor TR508. Variable inductor L512 sets the frequency of the oscillator circuit. This signal can be monitored at test point TP5.

2nd IF And Detector

The output of the 2nd mixer is coupled to the input of 4-pole ceramic filter FL503 which provides 455 kHz 2nd IF selectivity. The 455 kHz IF output of ceramic filter FL503 is coupled to Pin 3 of Limiter/FM Detector IC501. The IF signal is amplified internal to IC501 then applied to 4-pole ceramic filter FL504 which provides additional 455 kHz IF selectivity (Refer to **IC DATA** for IC501). The output of the 455 kHz filter is applied to IC501, Pin 7. The 2nd IF signal is amplified and limited internal to IC501. Inductor L514 shifts the IF signal by 90° and applies it to the internal FM detector. The FM detector compares the shifted IF signal to the internal IF signal to recover the audio modulation. The audio output of the operational amplifier internal to IC501 is applied the input of buffer amplifier IC502-2. The **AUDIO** output of IC502-2 is applied to the System Control Logic circuit. This signal can be monitored at test point TP4. The output on Pin 12 of IC501 is applied to the input of amplifier buffer IC502-1. The output of IC502-1 provides a **Receiver Signal Strength Indicator (RSSI)** signal also sent to the System Control Logic circuit. This signal can be monitored at test point TP3.

9 Volt Regulator

The 9-volt regulator circuit powers the IF circuits of CMF-132 and consists of regulator IC503 and filter capacitors C570 ,C571, C572 and C573. An input voltage of +13.8 Vdc is applied to the input of IC503. This input is monitored at test point TP2.

NOISE BLANKER (CFR-138)

The Noise Blanker is a printed wire board subassembly that plugs into the receive circuit through connectors P1/P2/P3 and J501/J502/J503. The noise blunker is designed to improve receiver performance by blanking out impulse noise emanating from the alternator, ignition system, etc. This is accomplished by delaying the IF signal for 200 nanoseconds (**ns**) while generating a blanking gate (pulse) having the

same characteristics as the noise pulses. These blanking pulses are then used to turn off the delayed IF signal precisely where the noise occurs, resulting in noise-free audio reception.

The noise blanker may be disabled, if desired, by software control (by EUS).

The noise blanker consists of a 200 ns fixed delay line, 20.8 MHz rejection filter, three pulse amplifiers, a pulse amplifier/limiter, AGC amplifier, gate driver and blanker disable switch as shown in Figure 3 - Noise Blanker Block Diagram.

The IF signal from JFET buffer transistors TR501 and TR502, on the control logic/IF board, is applied to gate 1 of pulse amplifier transistor TR1 through the 10.8 MHz rejection filter and to delay line Z1. Delay line Z1 delays the IF signal by 200 ns and returns it to the two JFET gating switches on the control logic/IF board. The undelayed IF signal is amplified by pulse amplifier TR1. Transistor TR1 provides approximately 20 dB of amplification. Bias for TR1 is determined by resistors R1 and R2. Transistor TR1 is controlled by Automatic Gain Control (AGC) amplifier IC2, and transistors TR7, TR8 and TR9. The IF output of TR1 is further amplified and limited by pulse amplifier/limiter IC1. IC1 provides approximately 50 dB of amplification.

The output of the limiter is applied to pulse detector transistor TR2. DC bias for TR2 is set at the threshold of conduction so that all noise pulses regardless of magnitude or duration will be detected.

Threshold bias is established by resistors R12 thru R15 and diode CD1. Resistor R13 is a negative temperature compensating resistor where temperature characteristics complement IC1 to adjust the threshold level of TR2 with changes in temperature.

The detected pulse is taken from the collector of TR2 and further amplified by pulse amplifier transistors TR3 and TR5. Capacitor C18 in the emitter circuit of TR3 provides a low frequency bypass to ground and also maintains a full charge to allow TR3 to be switched on and off more rapidly. The output of pulse amplifier TR5 is applied to gate driver transistor TR6. Transistor TR6 provides drive to operate the four JFET switches (TR503 thru TR506) located just ahead of the crystal filters on the synthesizer/Receiver Board. The delayed IF signal from delay line Z1 arrives at TR503 and TR506 at the same time as the gating pulses from the blanker switch. The gating pulse switches TR503 and TR506 coincide with the noise pulses on the IF signal, shunting all noise pulses to ground.

Blanker Disable

The blanker disable inputs are provided to assure complete turn off of the noise blanker function while allowing the delayed IF signal to be processed through the receiver. BLNKR DIS 1 is applied to pulse amplifier TR1, gate 2 and the base of TR4, turning it on. Transistor TR4 shorts the emitter and collector of pulse amplifier TR3, preventing any remaining noise pulses from passing.

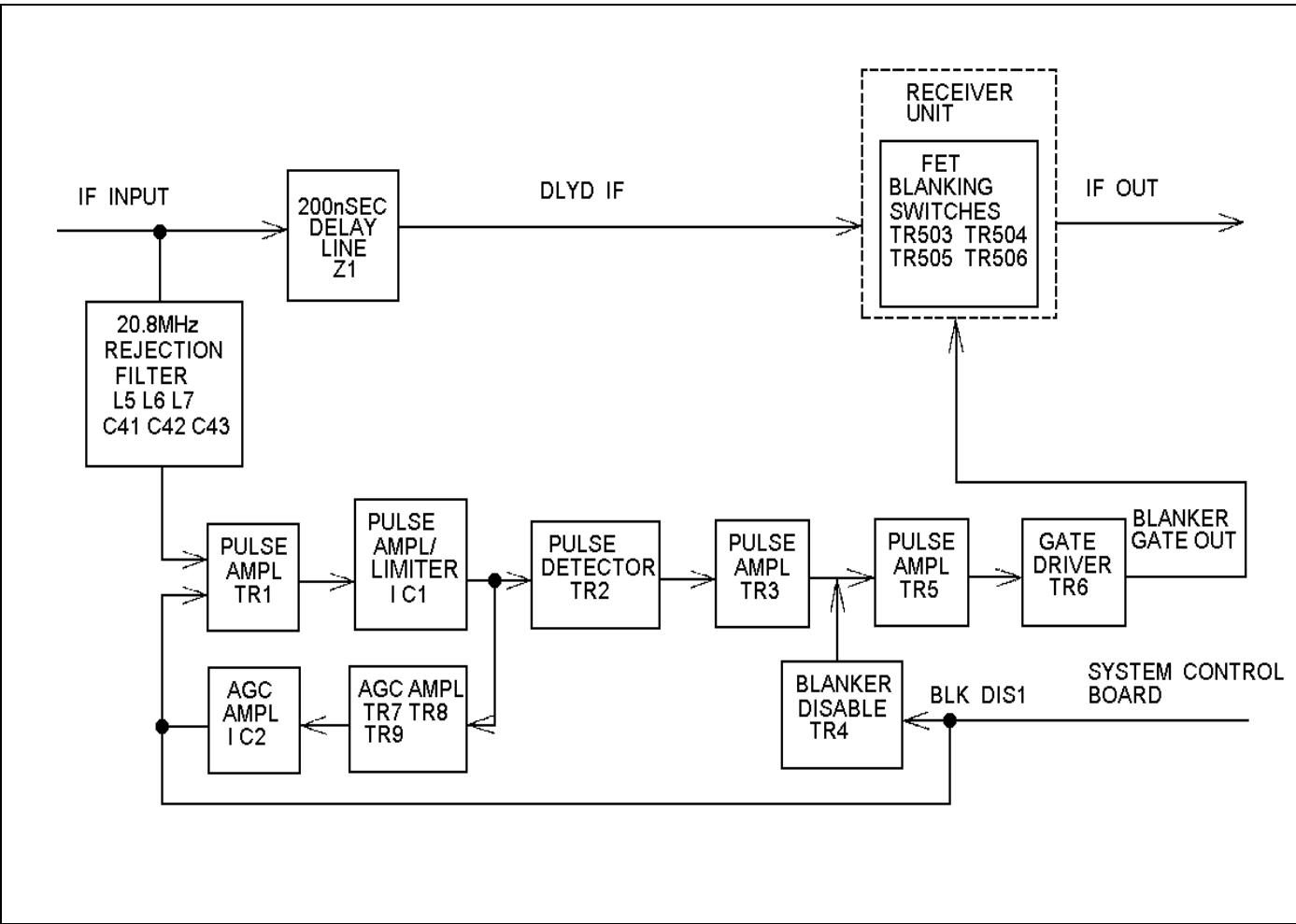
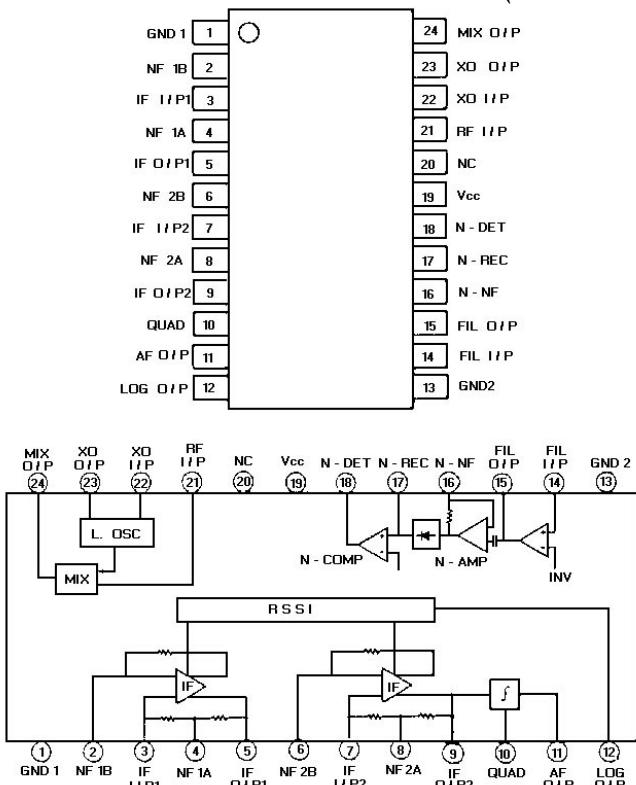
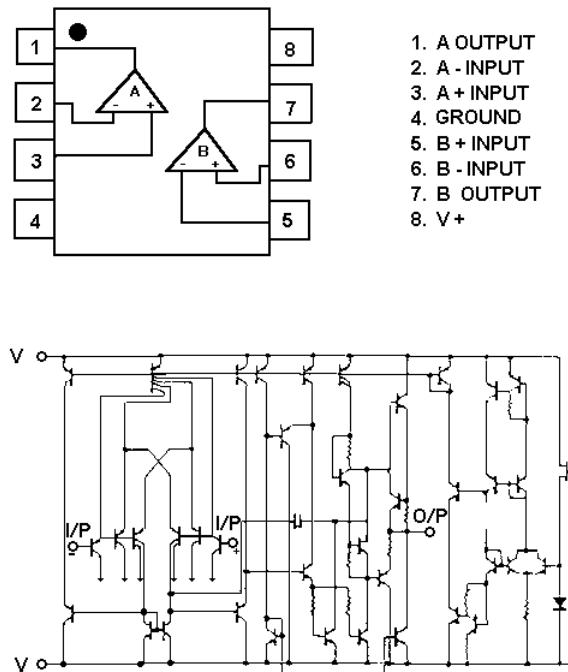
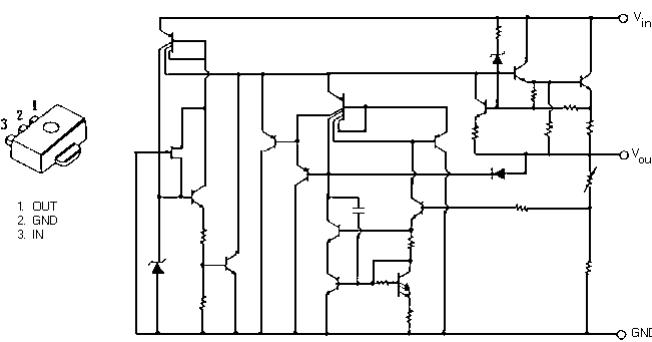
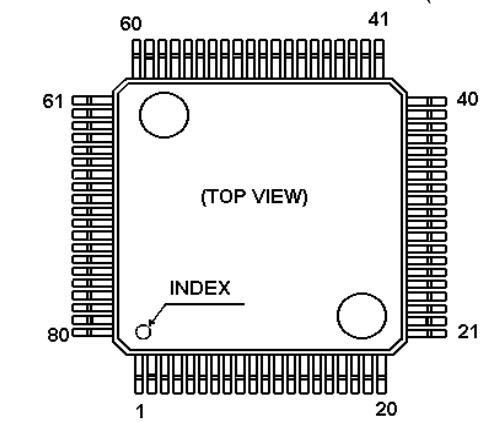


Figure 3 - Noise Blanker Block Diagram

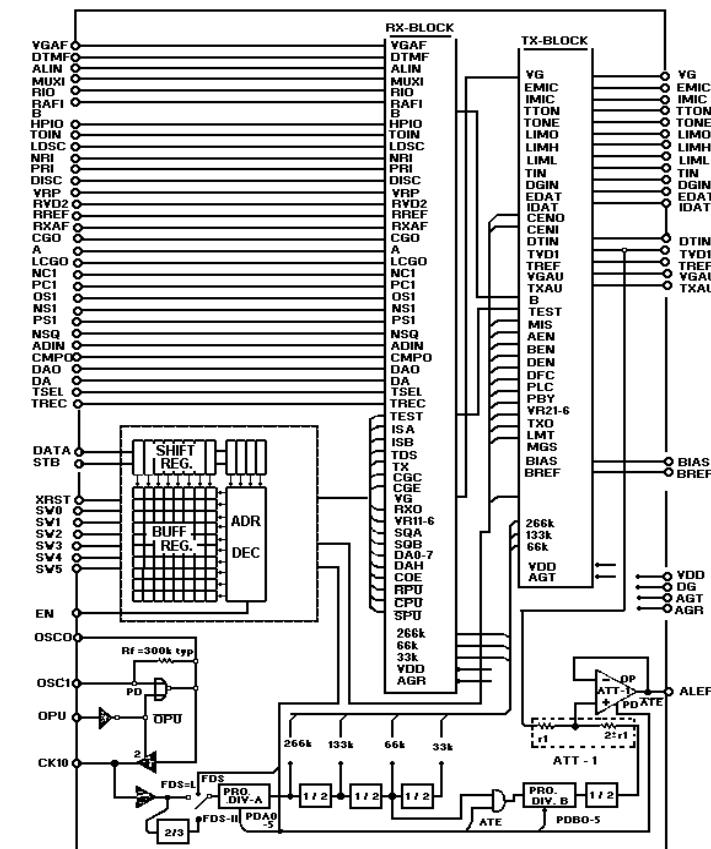
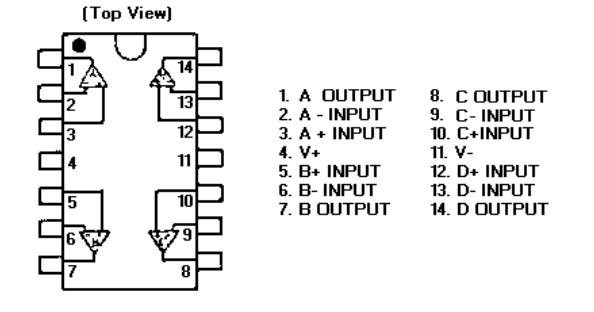
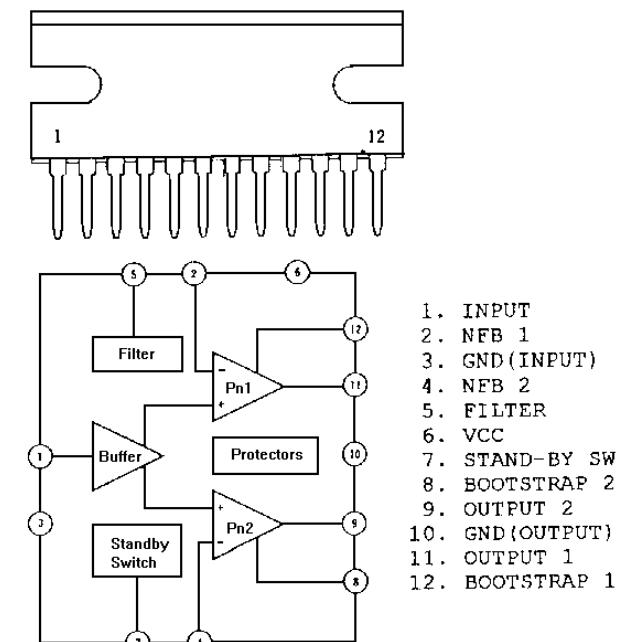
20.8 MHz IF SECTION

Linear, IF Amplifier/Detector IC501
(TA31132F)Linear, Dual Operational Amplifier IC502
(NJM3404)Linear, Positive Voltage Regulator IC503
(NJM78L09UA)

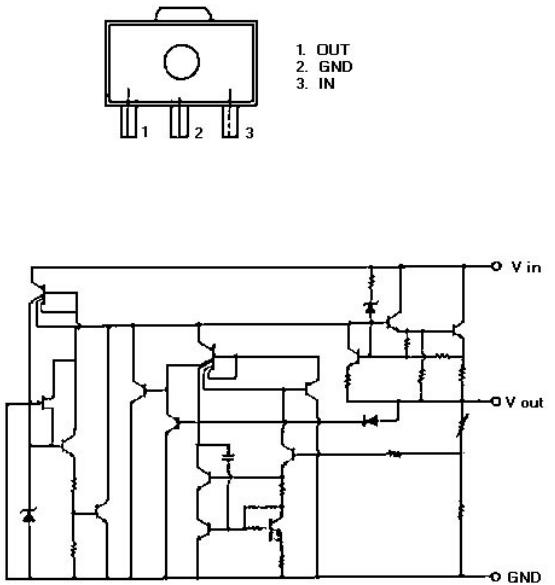
CONTROL LOGIC SECTION

Audio Signal Processor IC601
(SFPM-64V)

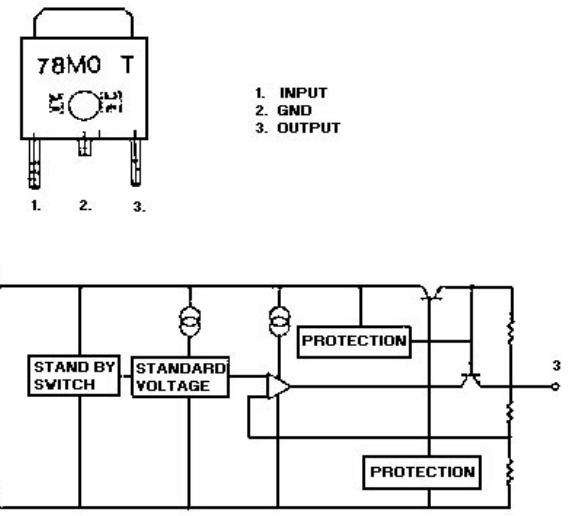
BLOCK DIAGRAM

Linear Audio Amplifier IC602, IC603
(NJRC 3403, PC123D)Audio Frequency Power Amplifier IC604
(UPC2500H)

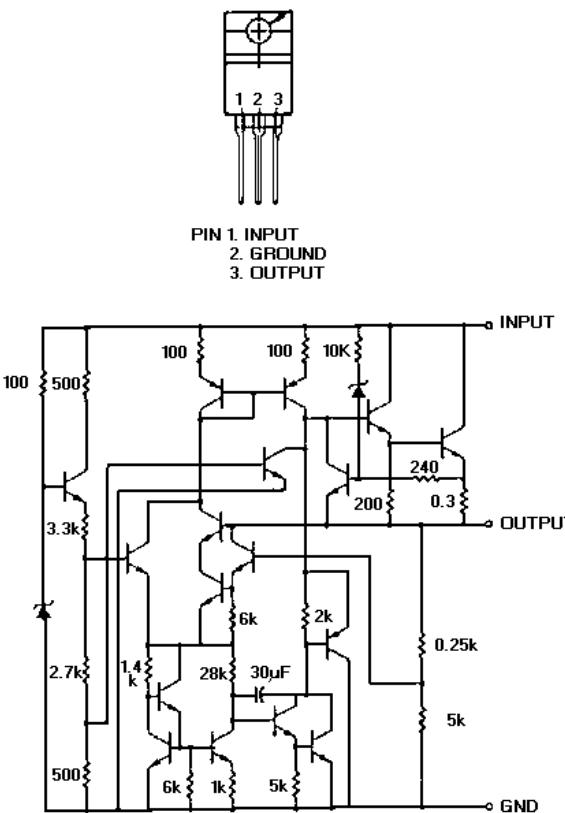
**Linear: Positive Voltage Regulator IC605,
IC609
(NJM78L09UA)**



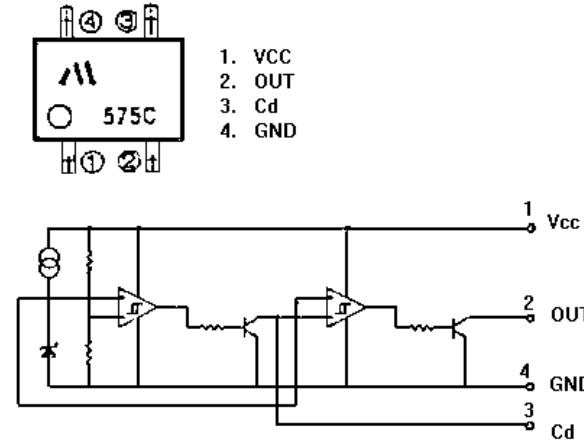
**Linear: Positive Voltage Regulator IC607
(L78M05T)**



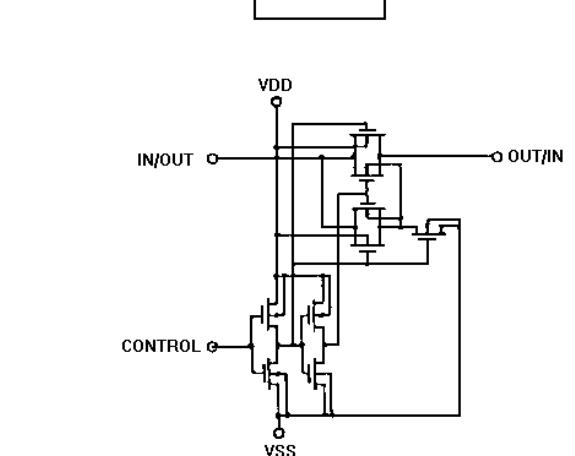
**Linear: Positive Voltage Regulator IC606
(MC7805CT)**



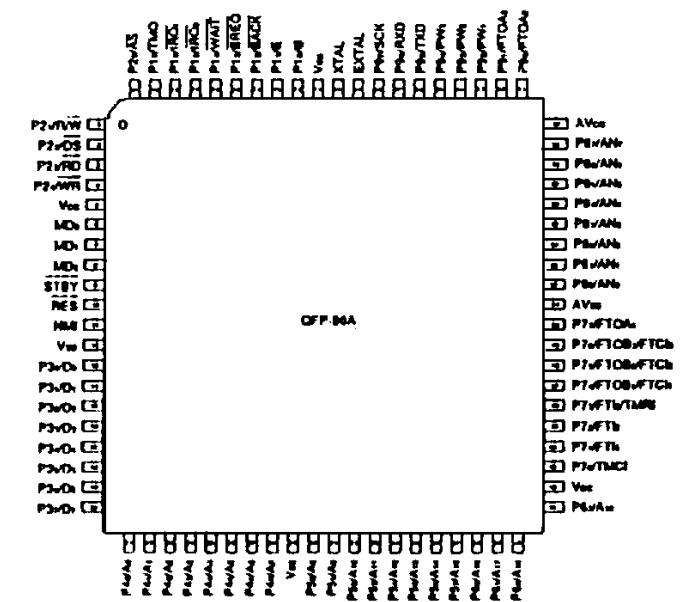
**Linear: Positive Voltage Regulator IC608
(L78M09T)**



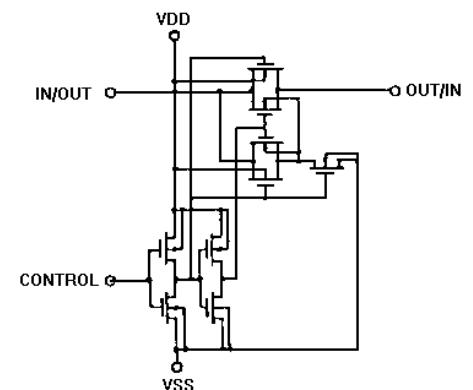
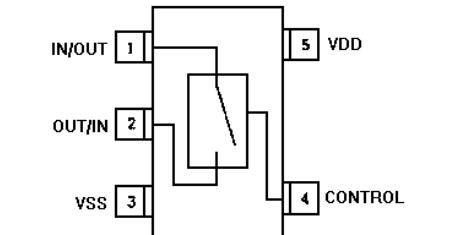
**Audio Amplifier IC610
(NJRC 2903)**



**Central Processing Unit IC701
(HD6435328RC72E)**

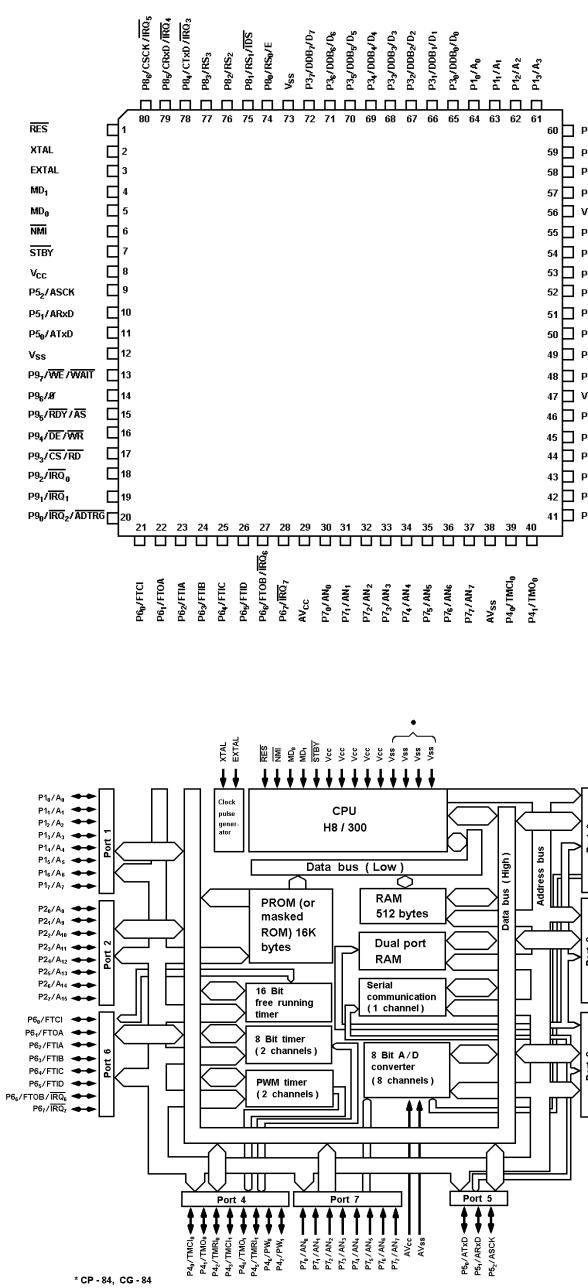


**Bilateral Switch IC611, IC612
(TC4S66F)**

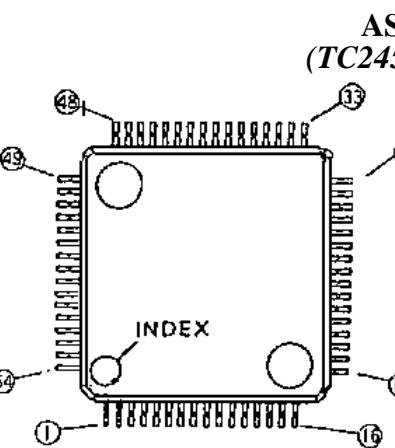


* CP-84 and CO-84 only

Central Processing Unit U702
(HD6433308RR91E)

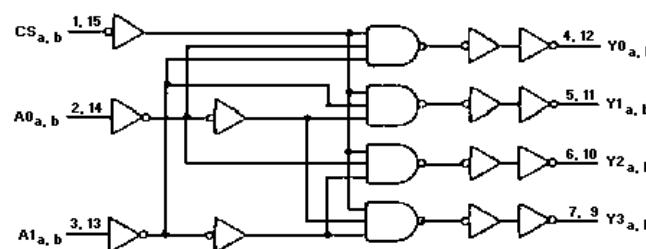


ASIC IC703
(TC245C090AF)

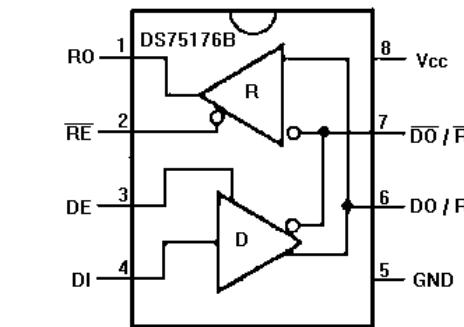
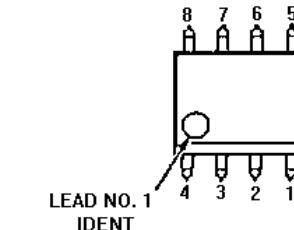


Decoder IC704
(MC74HC139)

| | | | |
|-----------------|---|----|-----------------|
| CS _a | 1 | 16 | Vcc |
| A0 _a | 2 | 15 | CS _b |
| A1 _a | 3 | 14 | A0 _b |
| Y0 _a | 4 | 13 | A1 _b |
| Y1 _a | 5 | 12 | Y0 _b |
| Y2 _a | 6 | 11 | Y1 _b |
| Y3 _a | 7 | 10 | Y2 _b |
| GND | 8 | 9 | Y3 _b |

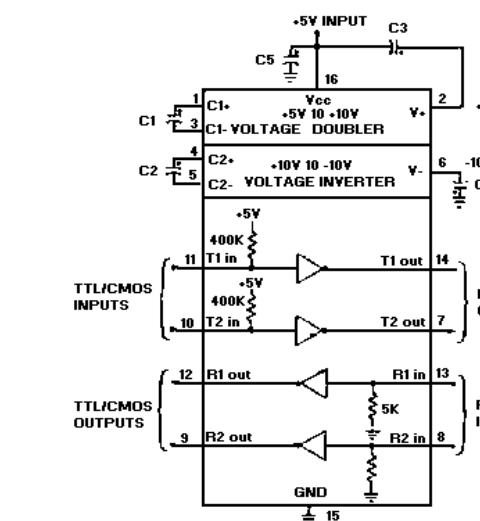


RS-485 Driver/Receiver IC705
(NS AS75176)



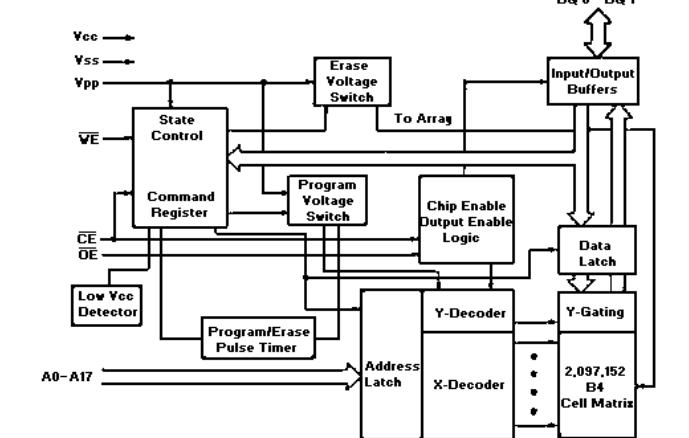
RS-232 Driver/Receiver IC706
(MA232EWE)

| | | | |
|----------|---------|--------|--|
| C1+ | 1 | Vcc | |
| V+ | 2 | GND | |
| C1- 3 | MAX220 | T1 out | |
| C2+ 4 | MAX232 | R1 in | |
| C2- 5 | MAX232A | R1 out | |
| V- 6 | | T1 in | |
| T2 out 7 | | T2 in | |
| R2 in 8 | | R2 out | |



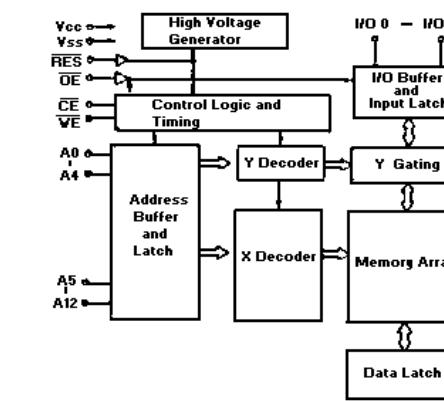
Flash Memory IC707
(N28F020)

| | | | |
|------|----|--------|----|
| A7 | 5 | A12 | 29 |
| A6 | 6 | A13 | 28 |
| A5 | 7 | A8 | 27 |
| A4 | 8 | A9 | 26 |
| A3 | 9 | A11 | 25 |
| A2 | 10 | A10 | 24 |
| A1 | 11 | A11 | 23 |
| A0 | 12 | CE (E) | 22 |
| DQ 0 | 13 | DQ 7 | 21 |

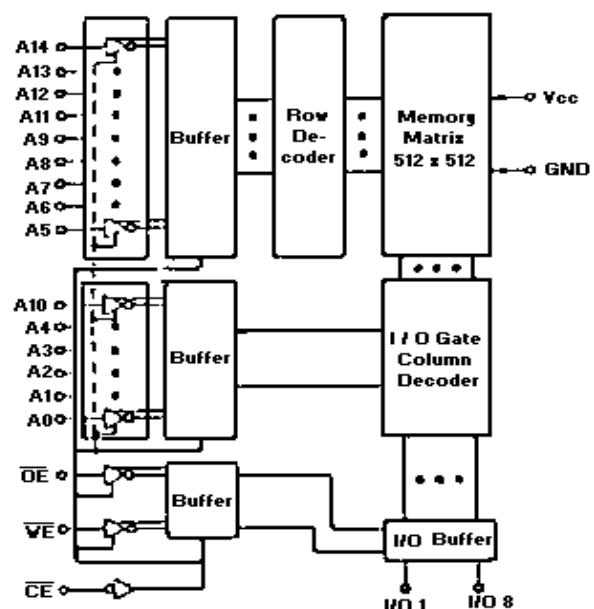
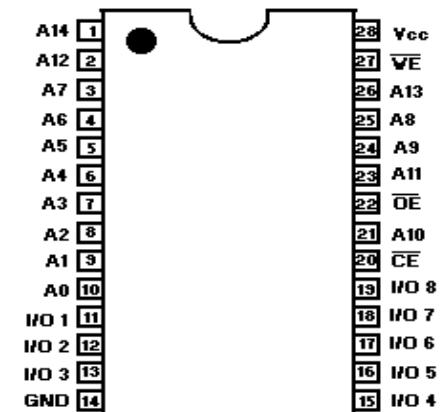


EEPROM IC708
(HN58C66FP)

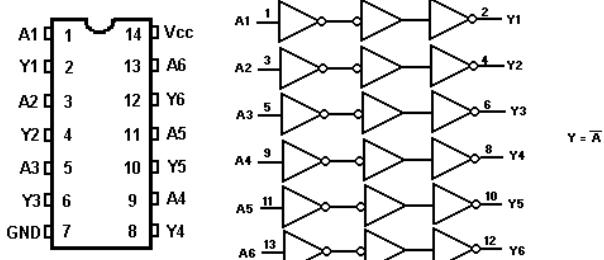
| | | | |
|--------------|----|-------|--|
| RDY / Busg 1 | 23 | Vcc | |
| A12 2 | 27 | VE | |
| A7 3 | 26 | RES | |
| A6 4 | 25 | A8 | |
| A5 5 | 24 | A9 | |
| A4 6 | 23 | A11 | |
| A3 7 | 22 | OE | |
| A2 8 | 21 | A10 | |
| A1 9 | 20 | CE | |
| A0 10 | 19 | I/O 7 | |
| I/O 0 11 | 18 | I/O 6 | |
| I/O 1 12 | 17 | I/O 5 | |
| I/O 2 13 | 16 | I/O 4 | |
| Vss 14 | 15 | I/O 3 | |



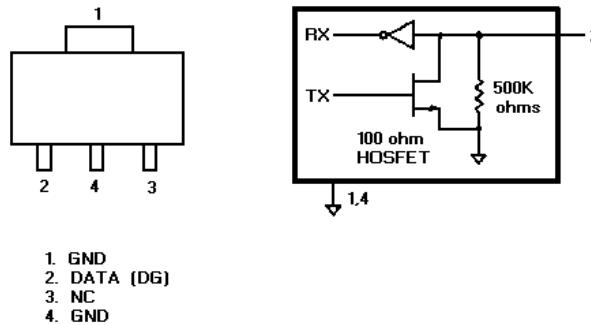
**RAM IC709
(TC55257CFL)**



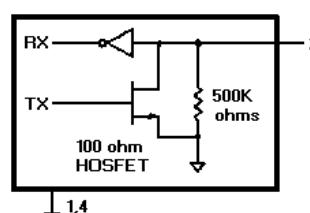
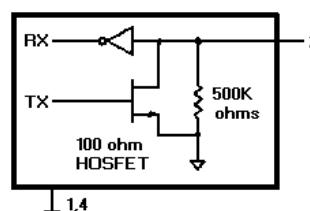
**Inverter IC711
(MC74HC04)**



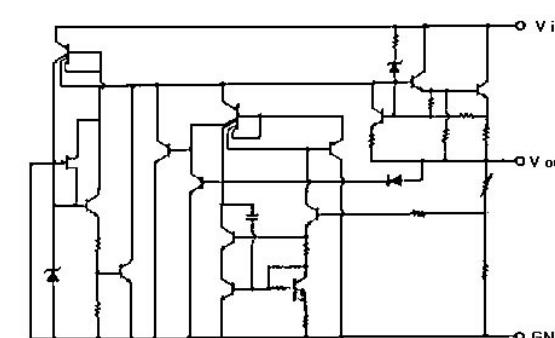
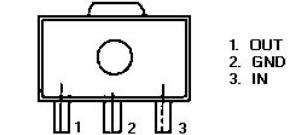
**Silicon Serial Number IC712
(DS2401)**



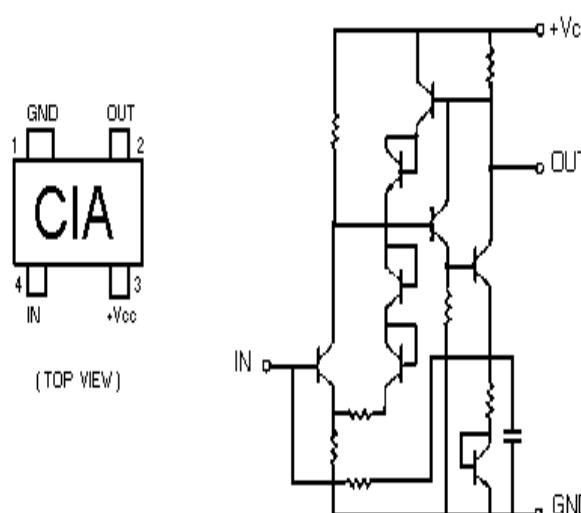
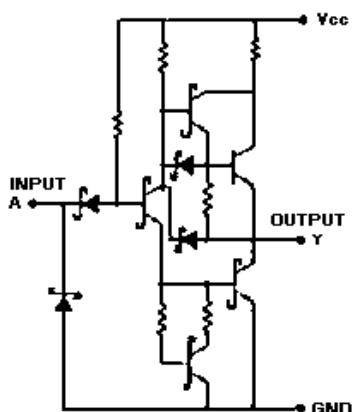
**NOISE BLANKER
Linear, Wide Band Amplifier IC1
(NEC PC1658G)**

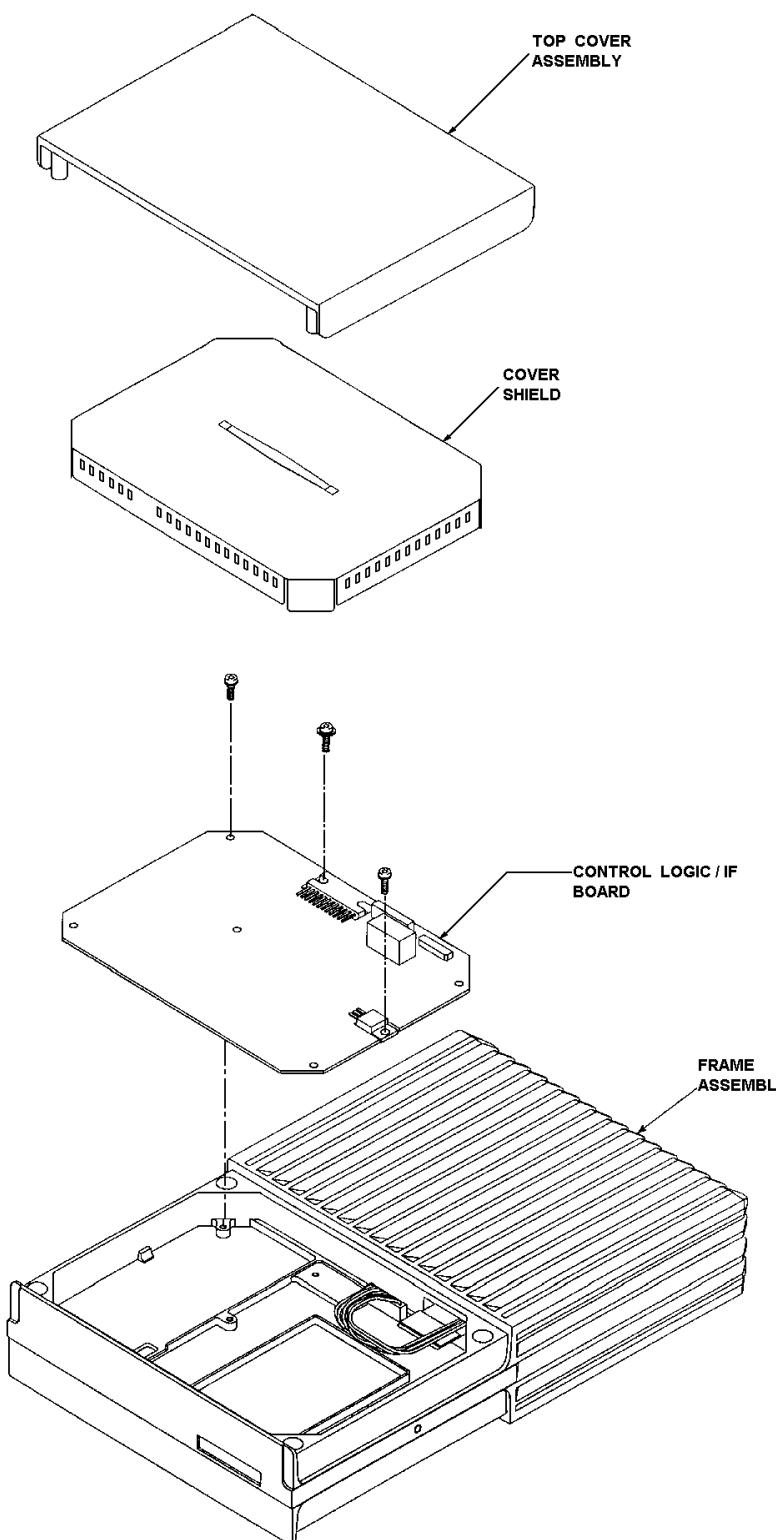


**Linear, Positive Voltage Regulator IC3
(NJRC NJM78L09UA)**

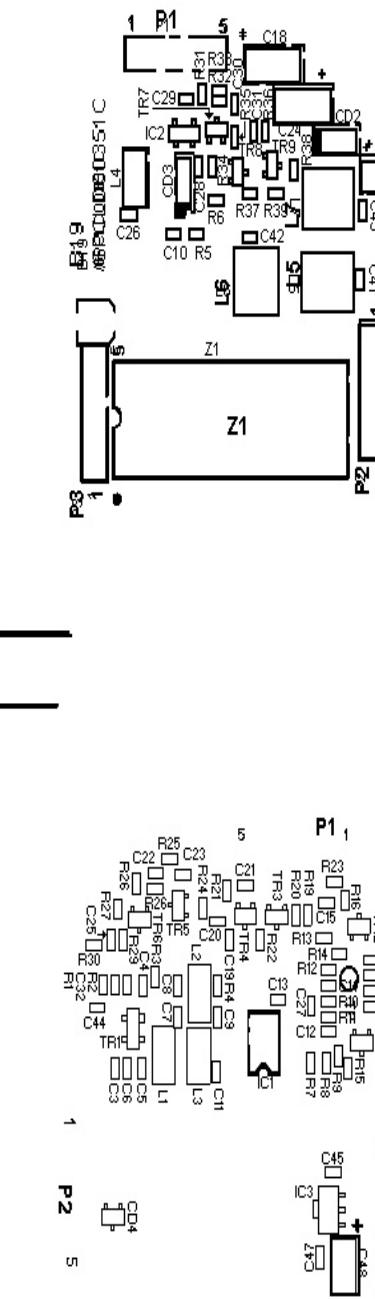


**RF Wide Band Amplifier IC2
(NEC PC1675G)**



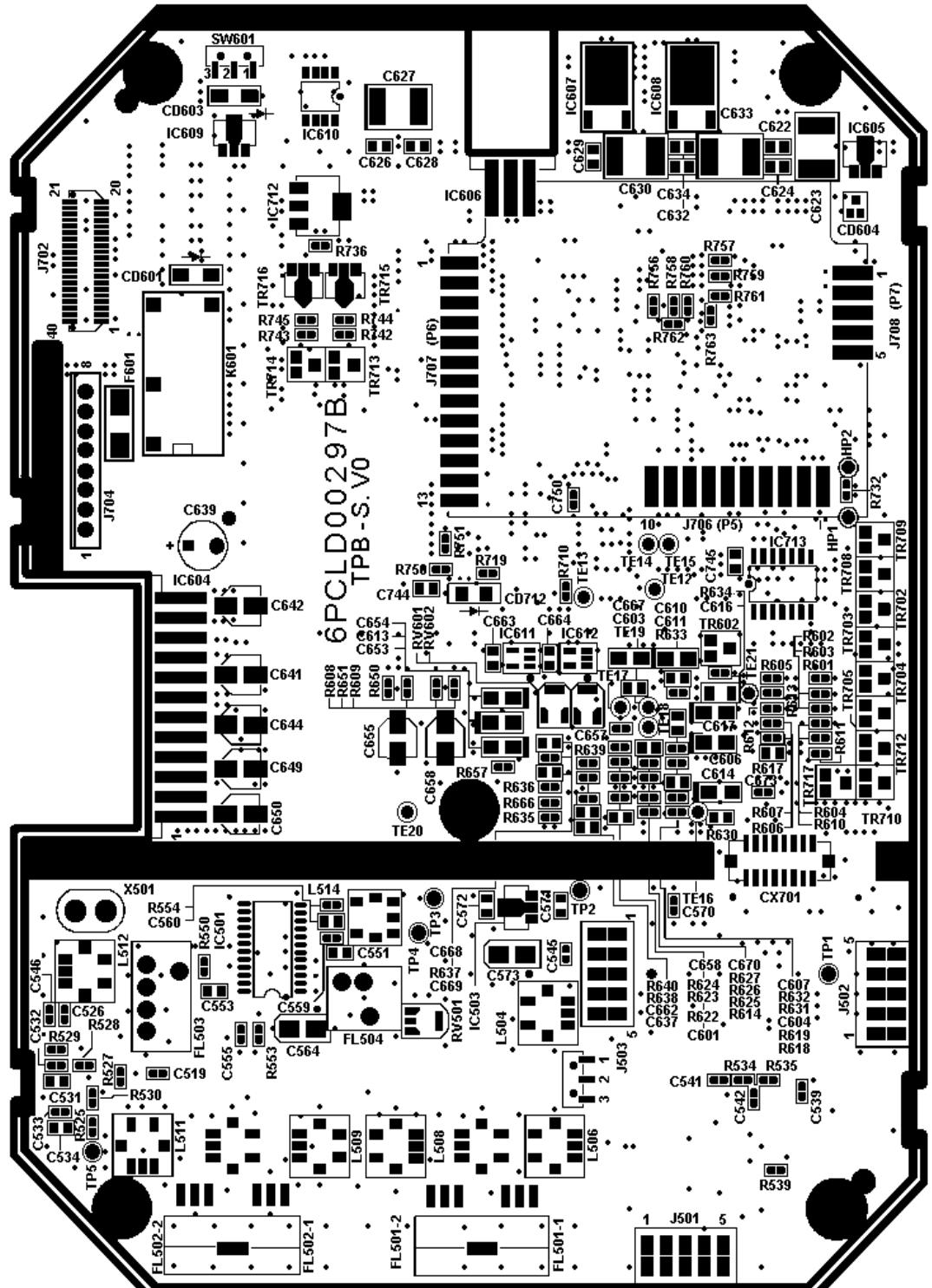


ORION LOW BAND
Control Logic/If Board
With Noise Blanker

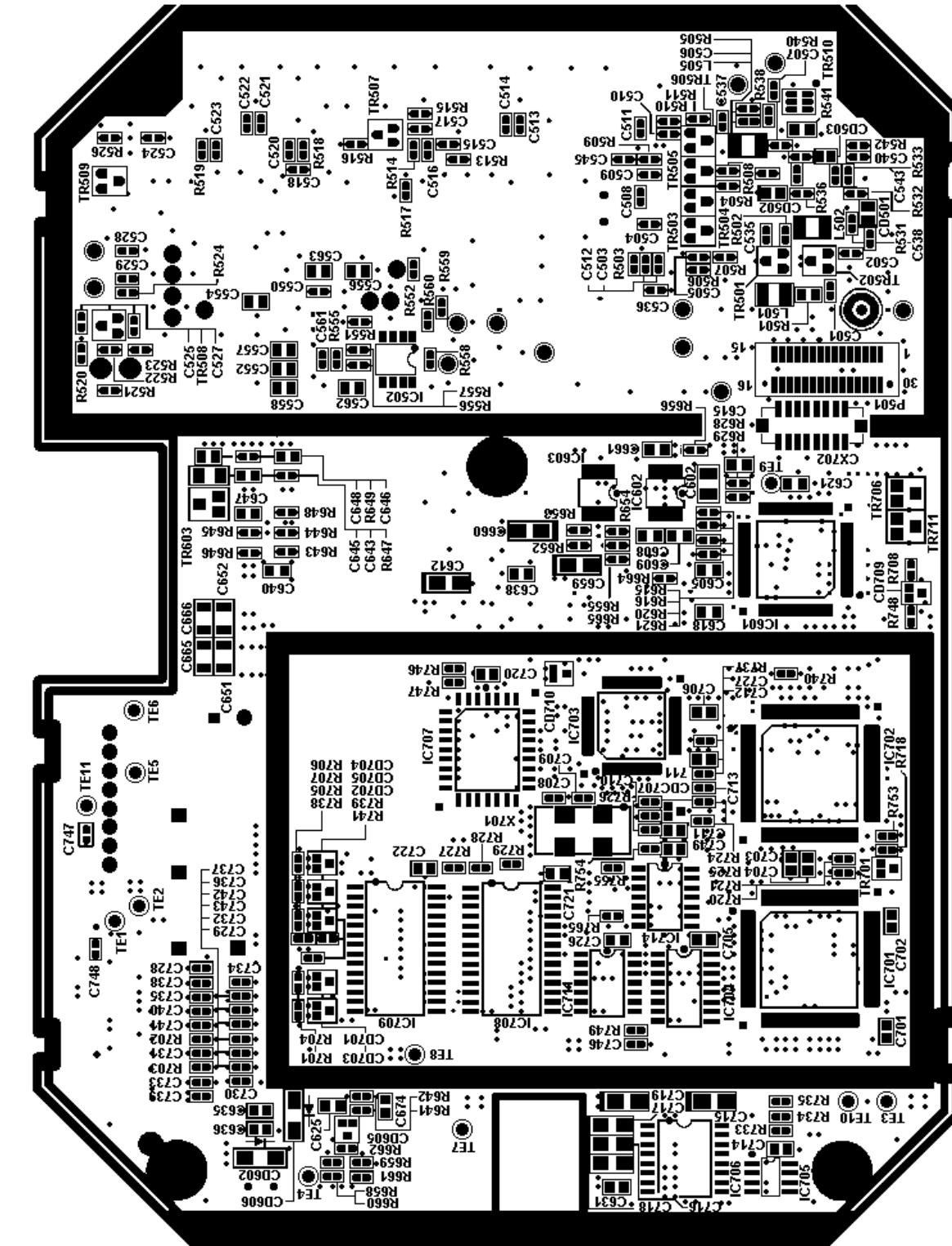


ORION LOW BAND
Noise Blanker
(6PCLD00351C)

COMPONENT SIDE



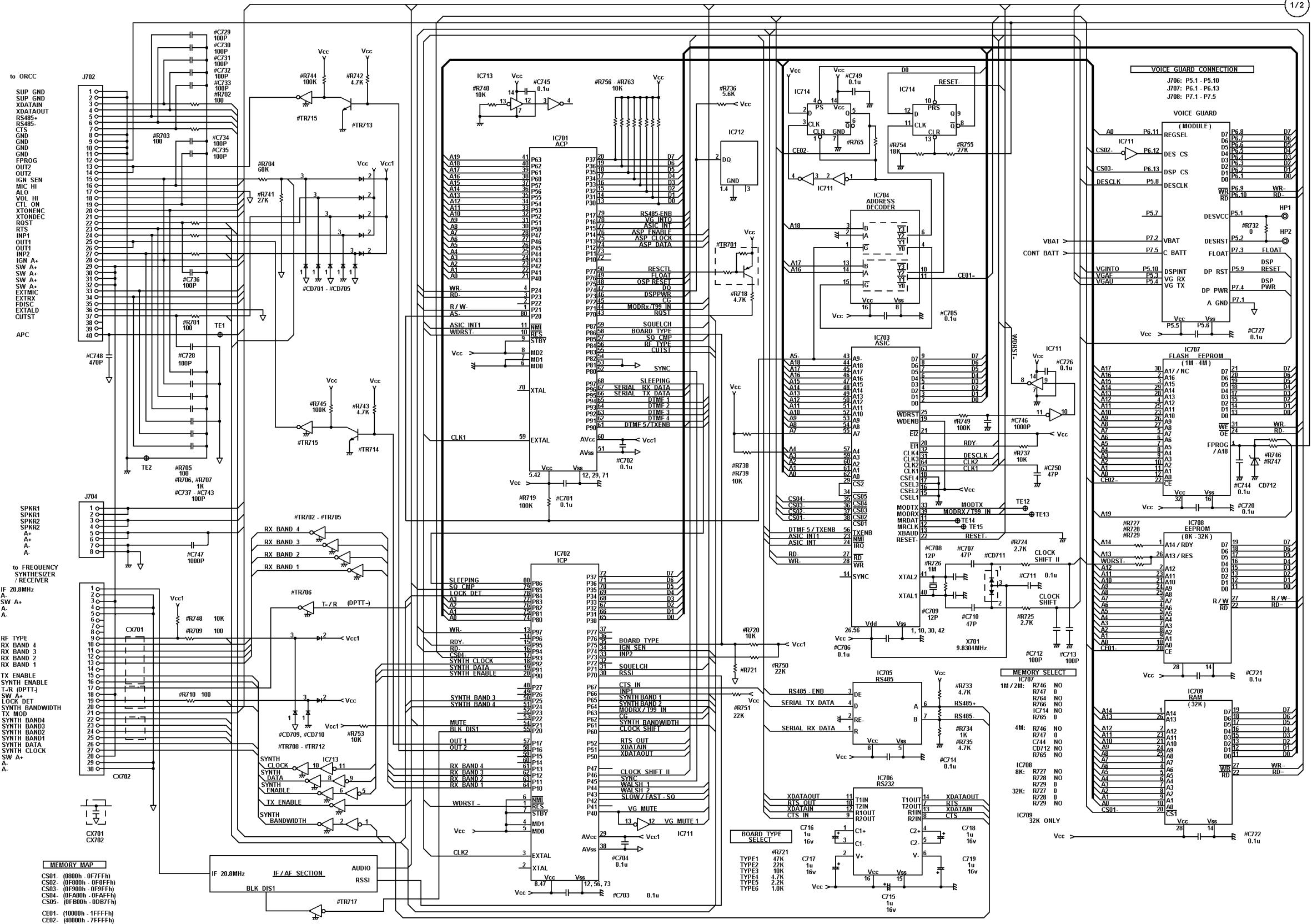
SOLDER SIDE



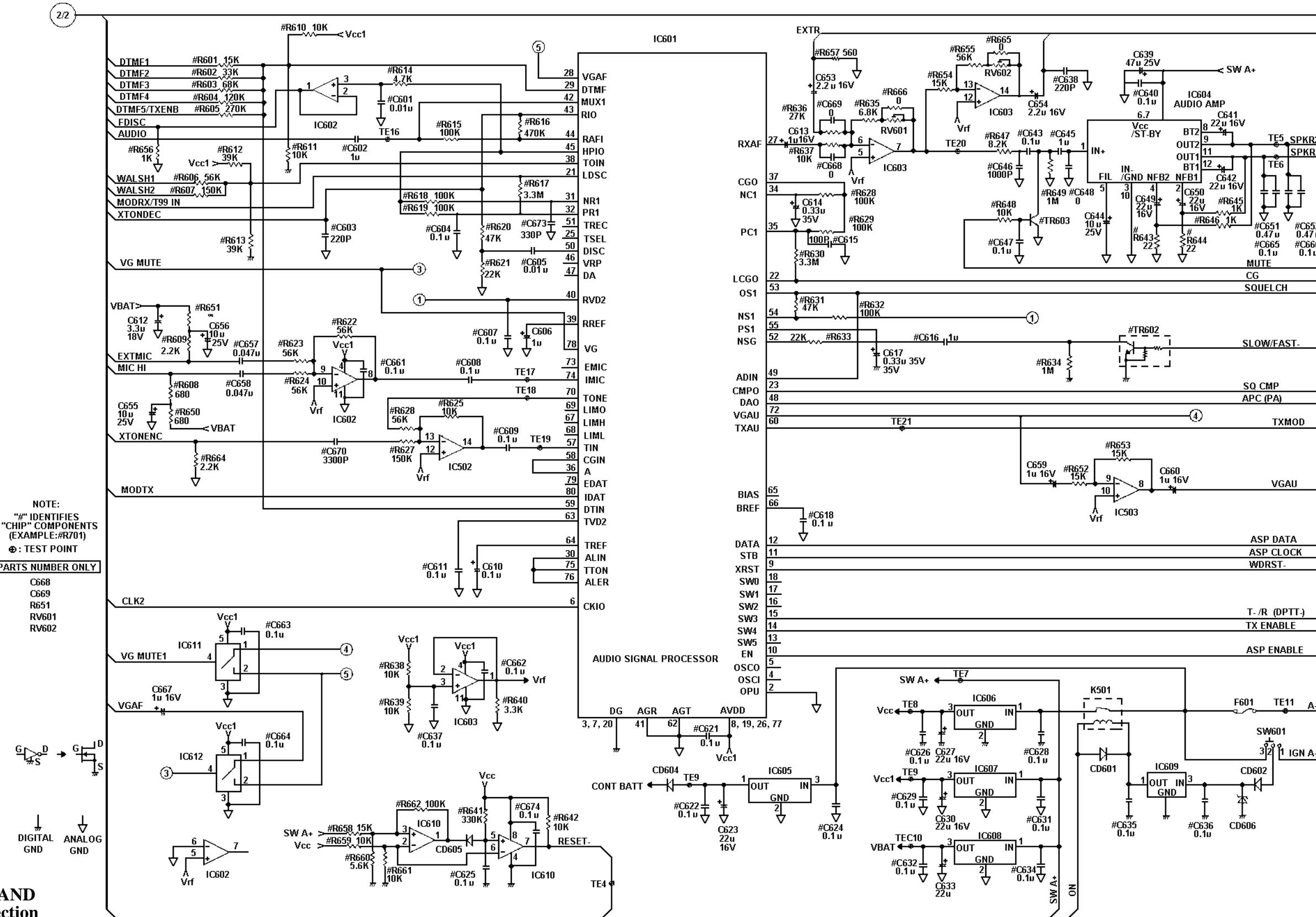
ORION LOW BAND
Control Logic/If Board

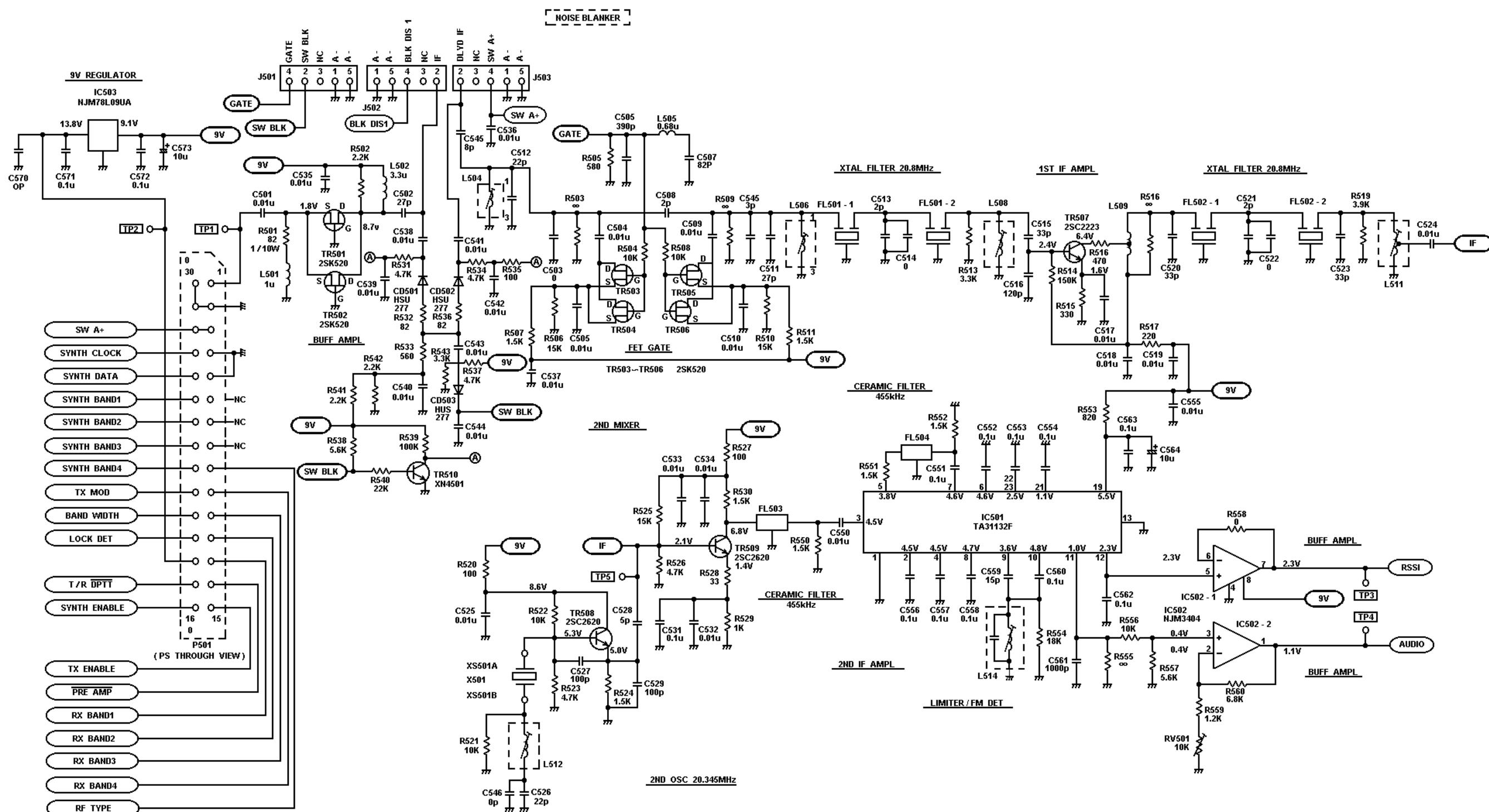
(6PCLD00297B)

1/2

ORION LOW BAND
Control Logic Section

(DD00-CMC-855 1/2)

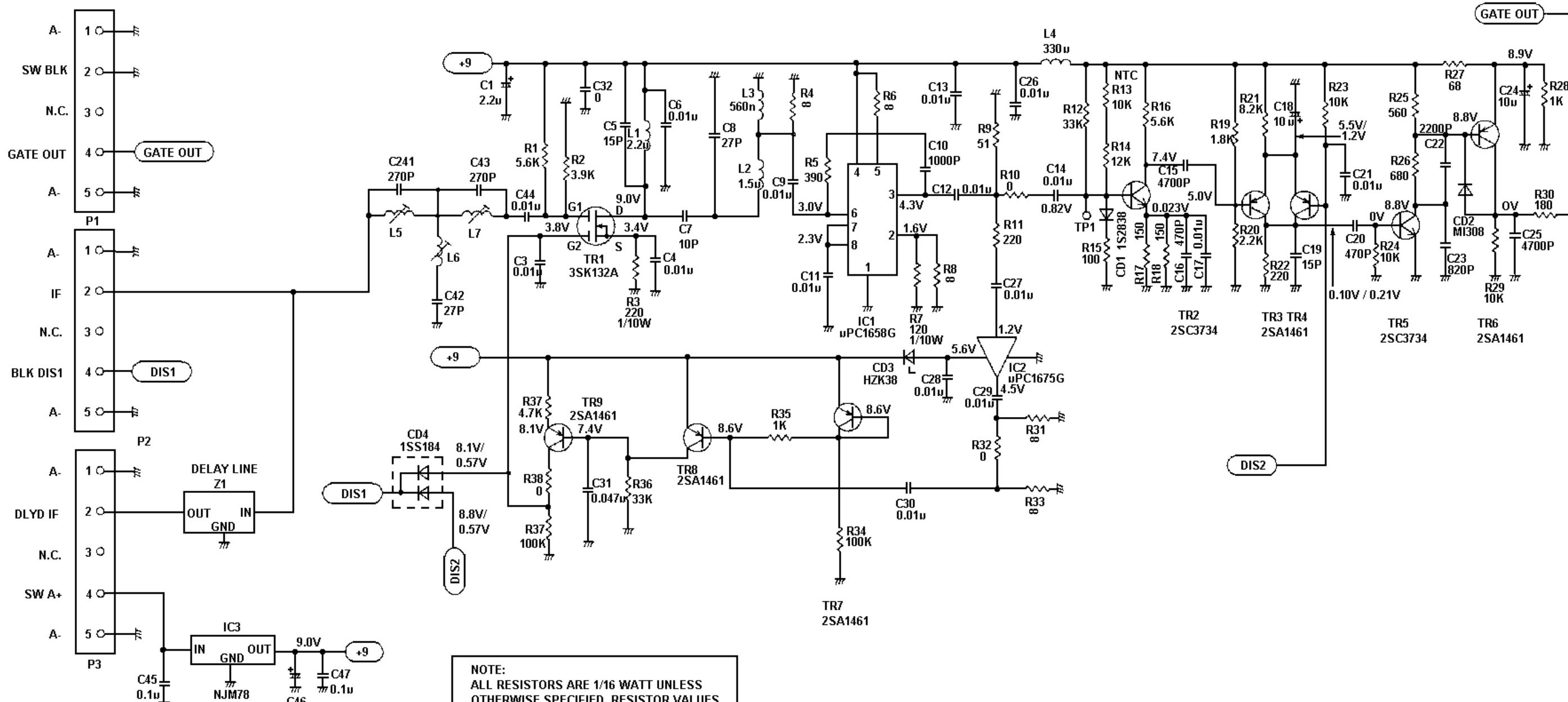




NOTE:
 ALL RESISTORS ARE 1/16 WATT UNLESS OTHERWISE SPECIFIED.
 RESISTOR VALUES IN Ω UNLESS FOLLOWED BY MULTIPLIER K OR M.
 CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER μ OR P.
 INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER μ OR n.

**ORION LOW BAND
20.8 MHz IF Section (CMF-132)**

(DD00-CMF-132)



ORION LOW BAND Noise Blanker

(DD00-CFR-138)

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