MAINTENANCE MANUAL

EDACS® COMPACT VERTICAL VOTER DIGITAL RECEIVER ROA 117 2240/1 & SELECTOR MODULE ROA 117 2040/2

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ERICSSON

FIGURES AND TABLES

SPECIFICATIONS*

ITEM	SPECIFICATION
ROA 117 2240/1 - DIGITAL RECEIVER **ROA 117 2240/2 - SELECTOR**	
DIMENSIONS (H x L)	100 mm x 220 mm
POWER REQUIREMENTS	+5 Vdc ±5% 300 mA typical. +12 Vdc ±5% 30 mA typical. -12 Vdc ±5% 1 mA typical.
CONNECTIONS	96 Pin DIN connector (X1) mating to VME backplane interface. Six pin modular RJ-12 connector (X3).
COMM PORTS	2 synchronous 9600 baud 1 asynchronous - switched for the following purposes: • Backup Serial Link (BSL) • Flash • Site Controller 1 (SC1) • Site Controller 2 (SC2)

* These specifications are intended for use during servicing. Refer to appropriate Specification Sheet for the complete specification.

INTRODUCTION

This manual provides information on the operation, installation, and maintenance of the General Purpose Trunking Card (GPTC) when configured and used in the EDACS Compact Vertical Voter (CV^2) as a Digital Receiver or a Selector.

DESCRIPTION

The Digital Receiver and Selector are the main components of the EDACS Compact Vertical Voter. The voter communicates with a stationary transceiver at the Main Site (or the Control Point in the case of Simulcast Systems) and up to 16 stationary Satellite Receivers or Remote Simulcast Stations (9 max.).

The Digital Receiver processes messages from its corresponding remote receiver and transfers the message to the selector using the Backup Serial Link.

The Selector evaluates the incoming messages and selects or votes for the Digital Receiver with the best digital signal. The selector then relays the voted signals to the Main Site and if present, the Console Switch.

SOFTWARE REQUIREMENTS

The software requirements and hardware compatibility are listed in Table 1. However, over the life of the product, the software may undergo improvements or enhancements. As a result, you should always refer to the Voter's Software Release Notes SRN-1007 to verify software and hardware compatibility.

NOTE

When installing or updating Voter software, ensure all the Digital Receivers and the Selector for a particular channel are using the same software version.

As a general rule, all Digital Receivers and the Selector for a particular EDACS channel should run the same software version. This ensures software compatibility within the same EDACS channel. Since there is no Voter software interaction between EDACS channels, different versions of software may exist on different channels, but it is not recommended.

The Voter Digital Receiver and Selector software is flashed into the Flash PROM U25 using the Flash Loading program stored in the GPTC's Flash Loader PROM U26. The Flash Loader PROM is interchangeable between the Digital Receiver and the Selector.

Once loaded, the application software checks the position of DIP switch S3-7 to determine the hardware configuration. When S3-7 is Closed, the GPTC is configured as a Digital Receiver. When S3-7 is Open, the GPTC is configured as a Selector.

Properly installed Voter Software is verified by observing the front panel LED display. The Digital Receiver and the Selector both have seven front panel LED's. The **RDY** LED, when ON, indicates the correct installation of software and operational readiness of the Digital Receiver or the Selector. The **DR/F** LED, when ON, indicates the GPTC is configured for operation as a Digital Receiver. The **SEL/F** LED, when ON, indicates the GPTC is configured for operation as a Selector. In addition, both the **DR/F** LED and the **SEL/F** LED have a coded blink rate for indicating failure modes. Refer to the LED INDICATORS section of this manual for additional information on the functions of the front panel indicators.

LED INDICATORS

The front panel LED's indicate the Digital Receiver and Selector's current status or state of operation.

NOTE

The numbers shown in parentheses refer to the circuit diagram's reference designator.

DIGITAL RECEIVER

The Digital Receiver front panel indicators, reset switch, and the programming connector shown in Figure 1 are described in detail in the following text.

RDY

The Ready Indicator (V14) is ON during normal operation indicating the code is functioning and the Digital Receiver is ready to send and receive messages. This indicator should be on at all times.

CC

The Control Channel indicator (V11) is ON while the Digital Receiver is operating in the Control Channel Mode. When the **CC** LED is OFF, the receiver is in the Working Channel mode (default mode of operation). The mode is determined by the Main Site and sent to the Voter via the link between the Main Site and the Selector.

However, if the **CC** LED is ON while in the Working Channel mode and one of the BER LEDs (**LBER**, **MBER**, or **HBER**) is ON, then the receiver is receiving Digital Voice data.

XMIT

The transmit indicator (V10) is ON when the Digital Receiver is sending information to the Selector over the

Table 1 - Software Requirements

	Voter Flash PROM (U26) Software	GPTC Hardware Configuration	Voter Operation Software Code	Station GETC software
Digital Receiver	RON 107 756/1 Revision R1A	ROA 117 2240/1 Revision R1A or later	350A1521G1	19A149256G18 or later or 349A9607G1 or later
Selector	RON 107 756/1 Revision R1A	ROA 117 2240/2 Revision R1A or later	350A1521G1	19A149256G18 or later or 349A9607G1 or later

Backup Serial Link (BSL).

Typically, the **XMIT** LED will be off or flashing at a rate of approximately 250 milliseconds (4 Hz).

Depending on the channel activity, one or more Digital Receiver may be transmitting at the same time. Therefore, the **XMIT** LED will not necessarily flash on all Digital Receivers at once. However, at least one Digital Receiver should be transmitting when messages are being sent to the Selector.

DR/F

The Digital Receiver and Fault indicator (V15) is normally ON. The Digital Receiver indicates a communication line failure by flashing the LED. If the **DR/F** LED flashes at a 2 Hz rate, the module is indicating a BSL failure. If it flashes at a 1 Hz rate, a phone line failure is indicated. If both the BSL and the phone line fail, the LED will flash erratically.

LBER, MBER, & HBER

The Bit Error Rate (BER) Indicators (V12, V13, and V16) indicate the calculated Bit Error Rate sent to the Selector during a Digital Voice call. If the BER value is between zero and 3% the **LBER** LED turns ON. **MBER** is ON when the BER is between 3 to 4.5% and **HBER** is ON when the BER is greater than 4.5%.

RST

The Reset Switch (R4) is used to manually generate the reset pulse and initialize the voter software.

PROG

The programming connector (X3) is a six contact modular RJ-12 connector used to flash the voter software from a PC into the Digital Receiver. When PC software "leafoff" runs, it asserts DTR which causes V35 to turn on +12 volts to the flash PROM. When 12 volts appears, a reset pulse is generated by comparator U2 which resets the Digital Receiver and initializes the Flash Loader program. Refer to the Voter Programming and Circuit Analysis sections for complete details.

SELECTOR

The Selector front panel indicators, reset switch, and the programming connector shown in Figure 2 are described in detailed in the following text.

The indicated functions of V13, V15, and V16 are unassigned and will normally be OFF. However, the LEDs being ON does not necessarily indicate a problem. Refer to the Troubleshooting section for additional details.

RDY

The Ready LED (V14) is ON during normal operation indicating the code is functioning properly and the Selector is ready to send and receive messages. This indicator should be on at all times.

CC

The Control Channel indicator (V11) is ON while the Selector is operating in the Control Channel mode. When the Selector is operating in the Working Channel mode (default mode), the **CC** LED is OFF. The operating mode is determined by the Main Site and sent to the Voter via the link between the Main Site and the Selector.

XMIT

The transmit indicator (V10), is ON when the Selector is sending information to the Main Site. During this process, the **XMIT** LED will appear to be flickering or flashing at a 1 Hz rate.

However, during a Digital Voice or Digital Data call, the **XMIT** LED will stay ON for the entire transmission.

SEL/F

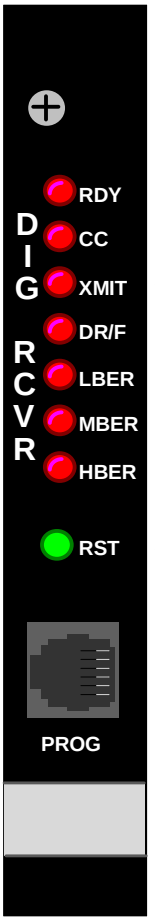
The Selector and Fault indicator (V12) is normally ON. The Selector indicates a communication line failure by flashing the LED. If the **SEL/F** LED flashes at a 2 Hz rate, the module is indicating a BSL failure. If it flashes at a 1 Hz rate, it indicates a phone line failure, and if it flashes erratically, it is indicating both a BSL and phone line failure.

RST

The Reset Switch (R4) is used to manually reinitialize the voter software.

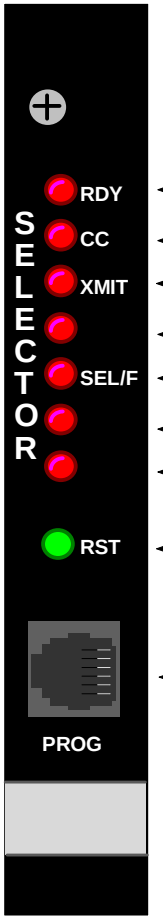
PROG

The programming connector (X3) is used to flash the voter software from the PC into the Selector. When PC software "leafoff" runs, it asserts DTR which causes V35 to turn on +12 volts to the flash PROM. When 12 volts appears, a reset pulse is generated by comparator U2 which resets the Selector and initializes the Flash Loader program. Refer to the Voter Programming and Circuit Analysis sections for complete details.



RDY (V14)	Operationally **Rea**d**y**. ● **ON** indicates the Digital Receiver is ready to send or receive messages.
CC (V11)	**C**ontrol **C**hannel. ● **ON** indicates the Digital Receiver is operating in the Control Channel Mode. ❍ **OFF** indicates the Digital Receiver is operating in the Working Channel Mode.
XMIT (V10)	Transmit. ❇ **FLASHING** indicates the Digital Receiver is sending information to the Selector over the BSL.
DR/F (V15)	**D**igital **R**eceiver/**F**ailure. ● **ON** indicates the unit is configured and operating as a Digital Receiver. ❇ **FLASHING** at a 2 Hz rate indicates a BSL failure, at a 1 Hz rate indicates a phone line failure and flashing erratically indicates both a BSL and a phone line failure.
LBER (V12)	**L**ow **B**it **E**rror **R**ate. ● ON during a Digital Voice Call when the BER is 0 to 3%.
MBER (V13)	**M**edium **B**it **E**rror **R**ate. ● ON during a Digital Voice Call when the BER is 3 to 4.5%.
HBER (V16)	**H**igh **B**it **E**rror **R**ate. ● ON during a Digital Voice Call when BER is greater than 4.5%.
RST (S4)	Manual Reset button.
PROG (X3)	Connector used for flashing software into the Digital Receiver.

Figure 1 - Digital Receiver Front Panel



RDY (V14)	Operationally Ready: ● **ON** indicates the Selector is ready to send or receive messages.
CC (V11)	**C**ontrol **C**hannel: ● **ON** indicates the Selector is operating in the Control Channel Mode. ❍ **OFF** indicates the Selector is operating in the Working Channel Mode.
XMIT (V10)	Transmit: ❇ **FLASHING** indicates the Selector is sending information to the Main Site.
(V15)	Not assigned.
SEL/F (V12)	Selector/Failure: ● **ON** indicates the unit is configured and operating as a Selector. ❇ **FLASHING** at a 2 Hz rate indicates a BSL failure, at a 1 Hz rate indicates a phone line failure and flashing erratically indicates both a BSL and a phone line failure.
(V13)	Not assigned.
(V16)	Not assigned.
RST (S4)	Manual Reset button.
PROG (X3)	Six contact modular connector used for downloading the operating software into the Selector.

Figure 2 - Selector Front Panel

INSTALLATION AND CHECKOUT

Installation or removal of the Receiver or Selector involves sliding the module into or out of the Digital Voter Shelf. The actual slot position is determined by the system's number of channels and sites. However, one selector will always be in slot one and the main site receiver (DR#1) is always in slot three. The modules may be inserted or removed from the shelf with power applied, however, always observe basic safety precautions to prevent injury or equipment damage.

DIP SWITCH SETTINGS

The DIP switches are used to identify the GPTC configuration, Digital Receiver or Selector, and to set the Digital Receiver's time slot number.

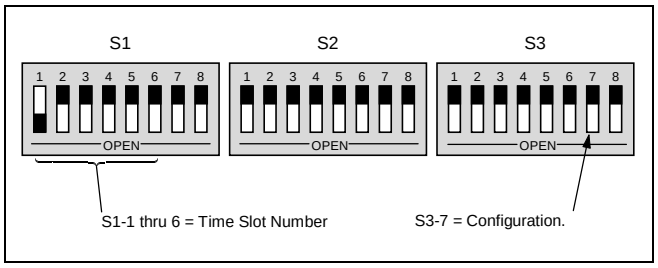


Figure 3 - DIP Switches S1 thru S3

Set the DIP switches S1 thru S3 to the settings corresponding to the Digital Receiver or Selector as follows:

Digital Receiver Switch Settings:

NOTE

Each Digital Receiver in a Voter channel is assigned a time slot number. This number is used to control the sequencing of messages between the Digital Receivers and the Selector.

SWITCH S1

Sections 1-6: Site number/Transmit window. Refer to Table 2 for the switch settings of each time slot number.

Sections 7-8: Closed, not used.

SWITCH S2

Sections 1-8: Closed, not used.

SWITCH S3

Sections 1-6: Closed, not used.

Section 7: Defines the module's operating mode. Closed places the code into the Digital Receiver mode.

Section 8: Closed, not used.

Table 2 - Digital Receiver Time Slot Settings

Site #	DIP Switch S1 Sections					
	1	2	3	4	5	6
1	O	C	C	C	C	C
2	C	O	C	C	C	C
3	O	O	C	C	C	C
4	C	C	O	C	C	C
5	O	C	O	C	C	C
6	C	O	O	C	C	C
7	O	O	O	C	C	C
8	C	C	C	O	C	C
9	O	C	C	O	C	C
10	C	O	C	O	C	C
11	O	O	C	O	C	C
12	C	C	O	O	C	C
13	O	C	O	O	C	C
14	C	O	O	O	C	C
15	O	O	O	O	C	C
16	C	C	C	C	O	C
17	O	C	C	C	O	C
18	C	O	C	C	O	C

Selector Switch Settings:

SWITCH S1

Sections 1-8: Closed, not used.

SWITCH S2

Sections 1-8: Closed, not used.

SWITCH S3

Sections 1-6: Closed, not used.

Section 7: Defines the module's operating mode. Open places the code into the Selector mode.

Section 8: Closed, not used.

CONFIGURATION PLUG INSTALLATION

The configuration plugs are used to physically alter data paths or circuit operation in the GPTC. Both the Digital

Receiver and the Selector have their own configuration plug. For correct operation use the following configuration plugs:

- Digital Receiver ROA 117 2242
- Selector ROA 117 2241

The top of the plug will indicate either Digital Receiver or Selector.

Ensure the configuration plug is correct for the desired operation and that it is properly oriented and installed on connector X2 on the GPTC.

FLASH LOADER PROM INSTALLATION

Ensure the correct version of the Flash Loader PROM is installed in socket XU26. A label on the top of the Prom indicates that the Prom is programmed with Flash Loading software "FLASH BURN" and the software version (for example, RON 117 256/1, version EDACS **01**).

NOTE

Refer to the Software Release Notes SRN-1007 to verify software requirements and hardware compatibility.

VOTER SOFTWARE INSTALLATION

This procedure provides instructions for downloading the Voter software. The Voter software is included in the Voter Media Kit, 350A1521G1. The installation process involves using an IBM compatible personal computer (PC), and interconnecting programming cable (19B804346P111) to download Voter software to the Digital Receivers and Selectors.

Equipment Required

- IBM PC/XT/AT or compatible with at least 640K memory, monitor and keyboard running MS-DOS version 3.0 or higher.
- Hard disk is recommended; but, not required.
- Serial Port configured as COM1.
- Programming Cable 19B804346P111.
- Software Media Kit 350A1521G1 (or later), refer to SRN for software compatibility.

Voter Programming

The loadable Voter software must reside on the PC OR floppy disk as an Intel Hex file. The "leafoff.exe" file is the executable program which loads the Voter hex file into the Digital Receiver or Selector. Both files should be in the same directory.

PC Setup

During first time use it may be necessary to setup the PC. Prepare the PC for programming the Voter GPTC board by performing the following steps:

1. Using standard DOS commands or a software file manager, create a directory named "**VOTER**" on the PC's hard drive (directory name is user selectable). This step is only required for first time use. When upgrading, all existing files should be archived before copying the new files into the directory.
2. Make "**VOTER** " the current directory and copy the following files from the software distribution diskette into the "**VOTER** " directory:
   - leafoff.exe
   - *hexfile*.hex

Programming the Voter

1. Connect the 19B804346P111 programming cable from the PC's Comm Port 1 to the RJ-12 phone jack "**PROG**" on the front of the Digital Receiver or Selector.

NOTE

Power must be applied to the Digital Voter when programming the Digital Receiver or Selector.

2. From the "**VOTER**" directory, run the **leafoff.exe** program by entering the command:

   "**leafoff *hexfile*.hex-1**".

   Replace "*hexfile"* with the Voter software file name.

3. The program will reset the Digital Receiver or Selector and run the Flash Loader program. The program erases the existing Voter software residing in the Flash PROM U25 and writes the new Voter software into the Flash PROM.

   When the program is finished, the PC will display the message "Radio Programmed. Closing down port COM1." Wait a couple of seconds before

disconnecting the programming cable from the "**PROG**" connector. This allows time for the PC to reset the Digital Receiver or Selector and initialize the Voter application program loaded in the Flash PROM.

4. Repeat Steps 2 and 3 to program additional Digital Receivers or Selectors.

NOTE

To save time, it is possible to set up a batch file to run the Flash loading program. The following is an example batch file.

Name the batch, for example, FL.BAT. Names in italics, such as *"voter"* is the name of the directory where the *hexfile* and *leafoff* reside. The file named *"hexfile"* is the file to be loaded and "*leafoff*" is the executable program. Enter the following batch program:

```
cd\voter
leafoff hexfile.hex-1
```

The batch file performs the operations outlined in Step 2. To run the program, type "FL" <enter> to program the Digital Receiver or Selector.

If any difficulty is encountered when loading the program, refer to the Troubleshooting section in this manual.

5. Refer to the Voter System Manual LBI-39149 and check out the Digital Receiver and Selector operation. If any problems are encountered, refer to the troubleshooting procedures in that manual.

   If a problem is traced to an individual GPTC board, refer to the troubleshooting procedures in this manual.

OPERATION

Digital Receivers and Selectors are used in various channel configurations depending on the number of remote Receiver Sites. A channel configuration includes a single Selector with its corresponding Digital Receivers and either a Rockwell Modem Interface Card (RMIC) or RS-232 Interface Card. One Digital Receiver is added for each additional remote Receiver Site. Therefore, the number of Digital Receivers varies according to the number of remote Receiver Sites for the channel.

NOTE

When installing Digital Receivers, Selector(s), and Interface Cards; refer to the Card Configuration Table in LBI-39153 for proper slot locations.

The Voter's first Digital Receiver (DR#1) communicates with the Main Site's receiver and enables voting of the Main Site. Expanded Voter configurations include up to 17 remote Receiver Sites.

The functions of the Digital Receiver and Selector depend on the type of call in progress and the current operating mode. Basically, the Digital Receiver and Selector process information from the remote Receiver Sites and Main Site in the form of digital data. The digital data represents Digital Voice, Data Calls, and internal EDACS system related messages such as Status, keys and unkeys RF, Alarm, Special Key, and Special Call Block messages.

All Digital Receivers and the Selector can function in either the Control Channel or Working Channel operating mode. The Control Channel mode involves processing messages related to channel requests and current status. The Working Channel mode involves processing information which represents digital communication during a call.

In addition, the Digital Receiver controls the squelch of its corresponding Analog Receiver module in the Analog Voter. The Digital Receiver squelches the audio output of its Analog Receiver whenever the remote Receiver Station is idle or not receiving. The Selector performs a similar function by muting the selected audio within the Analog Voter whenever a drop message is processed.

DIGITAL VOTING

Digital voting occurs when the channel is operating as a Working Channel and receiving a Digital Voice (Voice Guard or Aegis) call or the channel is operating as the Control Channel and receiving channel requests.

Both Digital Voice and Data calls are sent to the Digital Receiver from its corresponding remote Receiver Site via an RMIC or RS-232 Interface Card. The Digital Receiver processes the information, maintains sync on the data stream, and performs continuous Bit Error Rate calculations (BER) during a Digital Voice call. During a Data call, an initial BER calculation is performed by the remote Receiver Site. The Digital Receiver then sends a Ready message to the Selector over the BSL.

The Selector continues the digital voting process by simultaneously notifying all the remaining affected Digital Receivers to begin their BER calculations and report the results via the BSL.

The Selector requires a periodic message from the Digital Receivers to obtain information concerning the current status of the remote Receiver Station and the Digital Receiver. A copy of the status buffer is transmitted to the Selector at least every 250 milliseconds. However, RF and Alarm messages have a higher priority than Status messages and are processed first.

During normal operation most of the messages from the Digital Receiver to the Selector are the required 250 millisecond status updates. The Digital Receiver appends the site number to the status update messages sent to the Selector. The Selector echoes the message, including the site number, on the BSL for other Digital Receivers to hear. The appended site number is used by the Digital Receiver to determine if the message on the BSL is their own.

The end result is the Digital Receiver with the lowest BER value relays its data to the Selector over the BSL. In turn, the Selector relays the voted data on to the Main Site. In the event of two or more equal BER values, the Digital Receiver's data with the lowest slot time number is voted.

ANALOG VOTING

The GPTC receives a signal named RCVNG from the Analog Voter. The Analog Voter uses the RCVNG signal to inform the Selector that an Analog Receiver is receiving a signal.

Each Digital Receiver controls an E & M Squelch signal (EM_SQ_TO_AV) to a corresponding Analog Voter Receiver module. After a CV key message is received from its corresponding Satellite receiver, the EM SQ TO AV signal goes low to enable analog voting on that receiver module. The Analog Voter selects the best audio among the enabled receiver modules and routes it to the transmitter.

BSL SYNCHRONIZING

A synchronizing signal, SYNC, is used to arbitrate BSL use to prevent multiple Digital Receivers from trying to transmit messages to the Selector at the same time. Each Digital Receiver must first check the SYNC line before

transmitting on the BSL. The Digital Receiver will wait until the SYNC line is inactive before initiating a message to the Selector.

The SYNC line is present at X1-C29 of the Digital Receiver and routed through the backplane to all the remaining Digital Receivers as shown in the Backplane Interconnection Diagrams in LBI-39150.

The Digital Receiver activates the SYNC line to initiate a message and waits a predetermined period, calculated using the receiver's time slot number, before continuing. This waiting period prevents two Digital Receivers from simultaneously using the SYNC line.

If two Digital Receivers simultaneously activate the SYNC line, the Digital Receiver with the shortest waiting period will gain control of the BSL and will transmit its message to the Selector. The second Digital Receiver, the one with the longer waiting period, sees activity on the BSL, stops its attempt to use the BSL, and restarts the process of checking the SYNC line condition.

CIRCUIT ANALYSIS

The General Purpose Trunking Card (GPTC) is the heart of the Digital Receiver or Selector and contains all the digital circuits required for operation. This section will briefly describe the functionality of the various circuits.

NOTE

Navigation references shown as "≺sh. 1≻" refer to a specific sheet (1 thru 5) of Schematic Diagram 1911-ROA 117 2240 located at the end of this manual.

There are six main circuit groupings. These are the:

- Reset circuit
- Clock circuit
- Microprocessor Logic circuit
- Input and Output circuits
- Serial Ports
- Flash Loading circuits

Input Power

Power for the GPTC is provided by external power supplies supplying +5 Vdc +12 Vdc and -12 Vdc. The +5 Vdc enters at X1 pins A30, A31, B30, and B31 ≺sh. 1≻ and is routed through fuse F1 to the Vcc plane on the 4-layer PCB. The +12 Vdc enters at X1 pin C31 and is routed through fuse F2 to the +12V line, and the -12 Vdc enters at X1 pin C30 and is routed through fuse F3 to the -12V line. Capacitors C1 and C2, C3, and C4 provide additional filtering for the +5 Vdc +12 Vdc and -12 Vdc lines, respectively. Ground connection is made on X1 pins A1, C1, A32, B32, and C32 and connect to a ground plane.

Reset Circuitry

The GPTC contains a Power-on/Manual reset for initializing the programmed code and hardware devices on the board. The heart of the circuit is the microprocessor supervisory circuits contained in U14. These circuits reset the CPU and modems whenever one of the following events occur:

- Power is restored to the board.
- An external momentary active low is applied to X1 pin C23. A one-shot generates a reset pulse when X1-C23 goes low.
- An active low continuous reset is applied to X1 pin C22. Processor is held reset as long as X1-C22 is low.
- The **RESET** switch S4 is pushed and released.
- The Watchdog Timer in U31 times out.
- Flashing is initiated or terminated via the programming cable connected to the **PROG** connector X3.

When power is initially applied to the GPTC or if input power dips below the reset threshold, the microprocessor supervisor IC, U14 ≺sh. 4≻ will initiate a reset pulse. The reset output pulse, RESET, (U14 pin 7) goes low and remains low until the Vcc rises above the reset threshold and the internal timer releases RESET after a preset delay (≈200 ms). The active low reset pulse is applied to NAND gate U33A pin 1 resulting in an active high output at U33A pin 3. This is applied to modem U31 pin 25 (RESIN) . The modem RESOUT (U31 pin 3) is the logical-OR of the RESIN and the internal watchdog-timer pulse (if not serviced by the microcomputer U1). The high output reset pulse (RES) then resets to the microcomputer at U1 pin 10 ≺sh. 3≻ and the Phone Modem at U32 pin 25. It is also applied to inverter U10-4 pin 9 ≺sh. 2≻. The low output signal (pin 8) is then applied to pin 1 on the Output Latches U5, U6, and U7, resetting them.

Reset is also accomplished by pulling NAND Gate U34D pin 13 low. This may be done either externally, by pulling the RESET IN CONT line (X1-C22) low or by pressing the RESET button S4, which grounds pin 13. The resultant output from U34D pin 11 is a high pulse which is inverted by U9-4 and applied to the manual reset (pin 1) input of U14. U14 then generates the reset pulse as described previously.

When the external reset is generated by a pulsed signal, to ensure a permanent reset will not inhibit the GPTC, the RESET IN PULSE line (X1-C23) is used. This momentary active low pulse is applied to the Retriggerable Monostable Multivibrator U8-0 on pin 5 ≺sh. 4≻. The multivibrator generates a negative going pulse with a pulse width of ≈ 50 ms. This pulse is applied to NAND Gate U34D at pin 12. The reset circuit then functions the same as pressing the manual reset.

A reset may occur automatically if the microcomputer fails to service the watchdog timer in modem U32 ≺sh. 4≻. This reset will occur if the microcomputer misses a service for a two-second period .

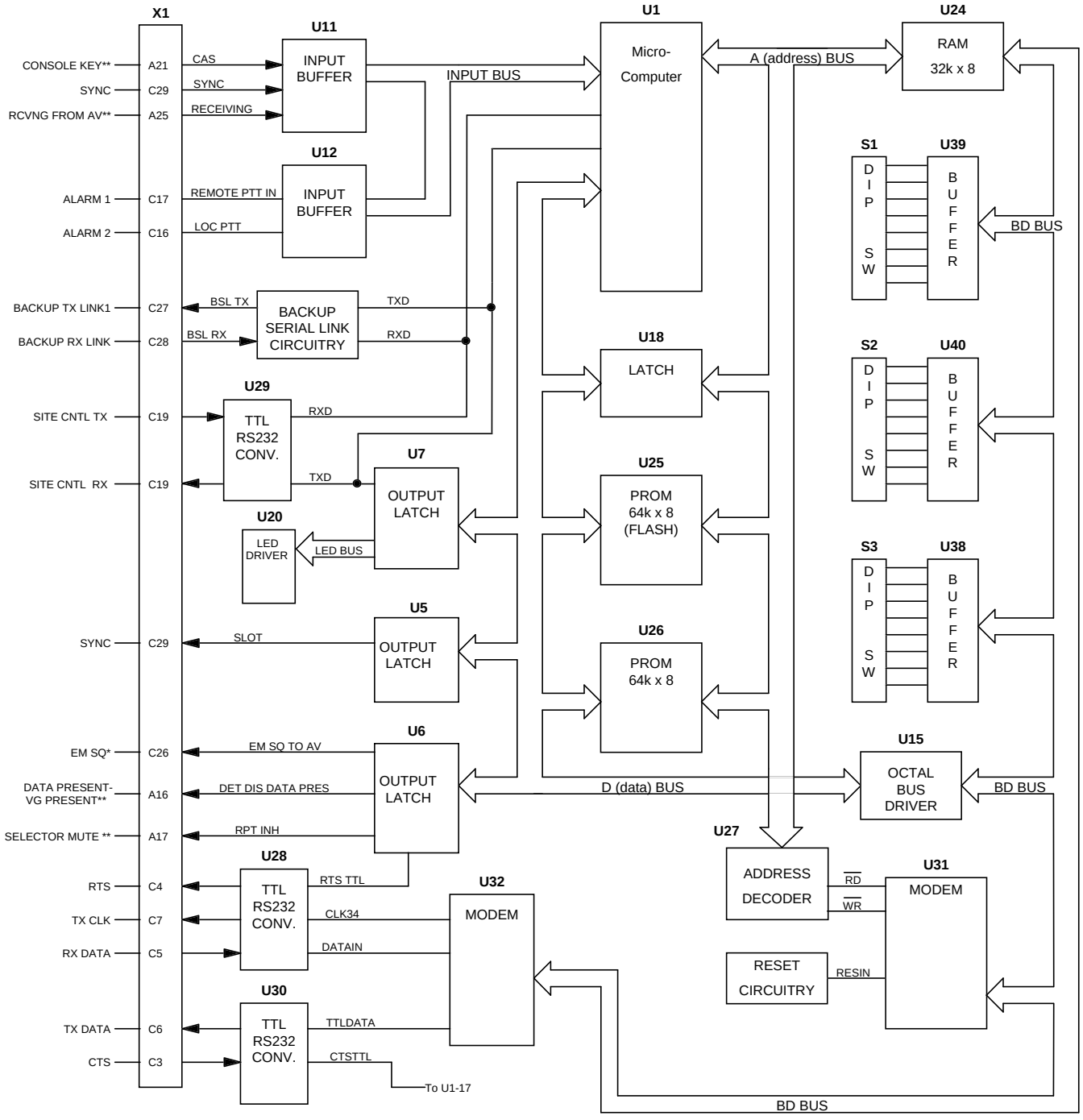


Figure 4 - GPTC Block Diagram

It is also necessary to generate a reset pulse any time the unit initiates the Flash programming or returns to normal operation. When the Flash programming is initiated by the PC though the programming cable plugged into the **PROG** connector X3, the flash circuit consisting of V36, V37, and V35 ⩤sh. 5⩥ causes the FLASH VPP line to go to +12 volts. This transistioning signal is applied the input of a comparator U14 pin 4 ⩤sh. 4⩥. The output of the comparator U14 pin 5 (FLASHING) goes to +5 volts during the flash loading process and returns to zero (0) volts when flashing is complete.

The time constant of R6 and C8 causes a slower rising or falling transition to occur at comparator U2 pins 5 and 6. U2-1 pin 7 is biased at approximately 3.3 volts and U2-2 pin 4 is biased at approximately 1.66 volts.

When the rising or falling FLASHING signal is below 3.3 volts, the output of Comparator U2-1 is high (open collector). When the rising or falling FLASHING signal is above 1.66 volts, the output of Comparator U2-2 is high (open collector). While the signal transitions from 1.66 volts to 3.33 volts or from 3.33 volts to 1.66 volts, the outputs of both comparators are high. Outside 1.66 to 3.33 volt range, one of the comparator outputs will be low keeping V6 cut off and U33A pin 2 high, holding off the reset.

While both comparator outputs are high, V6 turns on and applies a low to NAND Gate U33 pin 2 which outputs an active low signal to the modem U31 pin 25 (RESIN). The modem then resets the microcomputer, Phone Modem, and output latches as previously described.

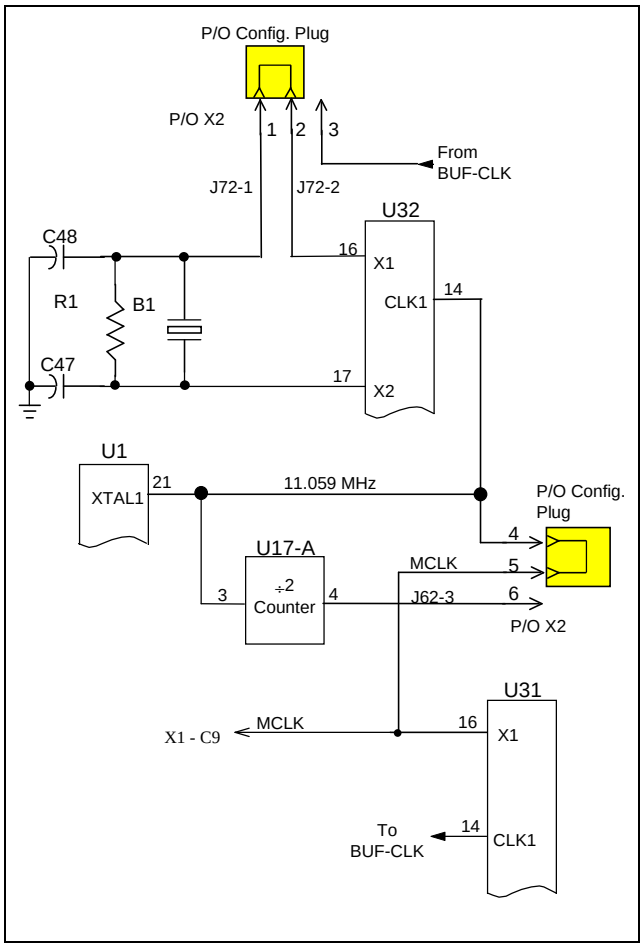


Figure 5 - Clock Circuit

Clock Circuitry

The clock drive for the GPTC originates in modem U32 ⩤sh. 3⩥. The clock oscillator consists of crystal B1, the oscillator amplifier in modem U32, and associated circuitry (see simplified diagram in Figure 5).

The crystal oscillator B1 and associated circuitry is connected to the modem oscillator amplifier U32 pin 16 by installing the Configuration Plug on connector X2 connecting pins 1 and 2 together. The oscillator amplifier circuit runs at 11.059 MHz as determined by crystal B1. The oscillator amplifier output at U32 pin 14 (CLK 1) provides buffered clock signals (11.059 MHz) directly to the microcomputer (U1) and to the RF Data Modem U31 pin 16 (MCLK) via the Configuration Plug and X2 pins 4 and 5.

NOTE

4800 Baud Applications - GPTCs used for 4800 baud applications require a 5.5296 MHz clock signal. This requires a modified Configuration Plug with a jumper from X2 pin 5 to pin 6 instead of pin 4 to pin 5. The X2-5 to 6 jumper routes the 11.059 MHz signal through the divide-by-two counter U17A to generate the 5.5296 MHz clock on the MCLK line.

Microprocessor Logic circuit

The GPTC Logic circuitry ⩤sh. 3⩥ consists of the microcomputer U1, the Flash Prom U25, Flash Controller Prom U26, RAM U24, Address Decoder U27, Bus Transceiver U15, ALE Latch U18, associated latches, DIP switches S1 thru S3 and Bus Drivers U38 thru U40. The microcomputer obtains its instructions from the Voter code loaded into the Flash Prom U25. The upper eight address lines (bits 8 thru 15) of the microcomputer exit port 2, U1

pins 24 (bit 8) to 31 (bit 15) and connect to the Flash PROM U25. The lower address lines (bits 0 thru 7) exit port 0, U1 pins 36 (bit 7) to 43 (bit 0) and are latched into register U18 when ALE (Address Latch Enable) goes high. The output of U18 supplies the lower eight address lines to the Flash PROM. Thus the lower eight address bits are on the address bus during the entire microprocessor cycle. The microcomputer uses the PSEN (Program Store Enable) U1 pin 32 control line to access the data from the Flash PROM U25 pin 24. Address Decoder U27 generates chip enable (CE) signals when RAM U24 or either of the two modems, or any of the three DIP switches, or any of the three output latches are accessed by the software. The address lines to the RAM are identical to those going to the PROM U25.

Microcomputer U1 accesses the Phone Modem (U32) which interfaces externally via TTL/RS-232 Converters U28 and U30 ⋖sh. 5⋗. This provides a 9600 baud synchronous remote data interface. Modem U31 ⋖sh. 4⋗ is used to buffer the system clock. Otherwise, U31 is not used for Voter applications.

The configuration of the GPTC is partly determined by the settings of switches S1 thru S3. Specifically whether the GPTC is operating as a Digital Receiver or Selector and which time slot number the Digital Receiver is set to. The microcomputer reads the switch settings via octal buffers U38 (S3), U39 (S1), and U40 (S2). Resistor pull-ups are provided for each of the switch lines.

The microcomputer accesses data to or from RAM U24, modem U31, modem U32, and octal buffers U38, U39, and U40 via octal bus transceiver U15. The transceiver, when directed by the microcomputer read command (RD at U1 pin 19) transfers the data from the switches and BD (buffered data) Bus to the D (Data) Bus. Data going to or from the PROMs U25 and U26, and Output Latches U5, U6, and U7 is handled by the D (data) bus.

Program memory is selected by the PSEN strobe (U1 pin 32). The ALE addresses the devices on the A (address) Bus by latching the lower eight bits of the address in U18. The upper eight bits of the address are sent directly to the devices. The two-to-four Address Decoder U27 is used to decode the upper address lines (A11 thru A13). When gated by RD (U1 pin 19) or WR (U1 pin 18), the decoder enables the desired device to transmit or receive data. The devices on the microcomputer bus are addressed according to Table 3.

Table 3 - Device Addresses

DEVICE	HEXADECIMAL ADDRESS
U24 - RAM	0000 - 1FFF
U31 - RF Modem	A170 - A172
U38 - S3 Latch	B800
U39 - S1 Latch	B000
U40 - S2 Latch	A800
U32 - Phone Modem	A0F0 - A0F2
U7 - Output Latch	A800
U6 - Output Latch	B000
U5 - Output Latch	B800

Input and Output Circuits

Signals sent to the GPTC from the Analog Voter, other Digital Receivers, and/or the Selector are sent to the microcomputer U1 via the Input Bus. The microcomputer evaluates the input data and depending on programming, outputs the necessary control signals to other elements of the system and turns on or off the front panel LEDs.

Input signals to the GPTC are buffered by U11 and U12 ⋖sh. 2⋗ which interface to the Input Bus. The microcomputer can read the data on the input bus, port 1, at any time.

The microcomputer provides output signals by writing specific logic values into output latches U5, U6, and U7.

The outputs of U7 turn on and off the various LEDs V10 thru V16. These LEDs provide visual front panel indications of the module's operation.

The U6 latch is used to output the Digital Receiver's EM Squelch signal to the Analog Voter (EM SQ TO AV). In a Selector, the U6 latch sends out the Data Present (DATA PRESENT-VG PRESENT) signal and the Selector Mute Signal.

Output latch U5 outputs the SLOT signal. The SLOT signal is applied to U23 ⋖sh. 5⋗ which drives the power FET V33. V33 outputs the SYNC signal to X1-C29 ⋖sh. 1⋗ and the backplane for monitoring by all other Digital Receivers and Selector(s).

Serial Ports

The GPTC contains both synchronous and asynchronous serial communication ports.

Asynchronous

All of the asynchronous signals go in and out of the microcomputer via the RXD (U1 pin 11) and TXD (U1 pin 12) lines. The logic circuits consisting of U9, U13, U33, U35, U36, and U37 ≺sh. 5≻ route these communication signals to the Backup Serial Link (BSL RX and BSL TX), to the PC during flash programming (FLASH RX and FLASH TX), to the RS232/TTL converter U29 via the SITE CNTL RX (X1-C19) and SITE CNTL TX (X1-C20) lines, and to SITE CNTRL 2 under the control of various logic signals 11_73_1SEL, 11_73_2SEL, FLASHING, LED_BUS_2, LED_BUS_5, and J16_2.

The data routed the RXD and TXD lines only flows in one direction at time at the rate of 19.2K Baud.

Synchronous

The 9600 baud synchronous data is received by each Digital Receiver from Satellite Sites or the Main Site. The Selector also transmits 9600 baud synchronous data back to the Main Site. These data paths may be RS-232 or Rockwell Modem (RM).

When the RM is used, the RMIC decodes the data and serially transfers it as an RS-232 signal to the Digital Receiver or Selector at X1-C5 (RX DATA) ≺sh. 1≻. When RS-232 communication is used, data comes directly to X1-C5 and is converted from RS-232 to TTL by the RS232/TTL converter U28 pin 19 ≺sh. 5≻. The output of the converter at pin 20 (DATAIN) is sent to the Phone Modem U32 pin 19 ≺sh. 3≻. When ready, the microcomputer directs the modem (via the ALE and RE signals) to convert the serial data to parallel data and download the data onto the BD Bus (pins 4 thru 11).

NOTE

When the Main Site or Control Point communicates with the Voter via RS-232 link an RS-232 Interface Module is used in place of the RMIC in slot 2.

RS-232 connections are used even when the Voter and site are not collocated if the link is over T1 Mux.

Data to be transmitted by the Selector is latched from the BD Bus into the Phone Modem U32. The modem converts the data from parallel to serial format and outputs the data from U32 pin 21 (TXDAT) on the TTL DATA line to the RS232/TTL converter U30 pin 2 ≺sh. 5≻. U30 converts the data from TTL to RS-232 and routes it to X1-C6 (TX DATA). The data then goes directly to the main site GETC via an RS-232 link or through the RMIC if a RM link is used.

Flash Loading Circuits

Flashing is controlled by the DTR line X3-5 from the PC. When the DTR is low (-12 V) at X3-5, power FET V35 is turned on connecting +12 volts to FLASH_VPP. Applying FLASH_VPP to the Reset Circuit U14 and U2 ≺sh. 4≻, generates a reset and starts the flashing process.

When going in or out of Flash mode, it is necessary to generate a reset pulse so the processor will begin executing the Flash Loader PROM program or the Voter program contained in the Flash PROM (normal operation). This is accomplished by circuitry around U2. When 12 volts is either applied to or removed from the flash, a reset is generated by the dual comparator circuit U2. (Refer to discussion on Reset.)

During flashing, the Voter program data is down loaded from the PC at X3-1 and is converted by the RS232/TTL converter U30. The TTL data (FLASH_RX) is routed to the RXD input of the Microcomputer U1 via the U35 logic circuits. Handshaking from the microcomputer to the PC (FLASH_TX) is routed to the TTL/RS232 converter U30 through logic circuits U13 and U36. Signal lines between the PC and the GPTC **PROG** connector are shown in Figure 6.

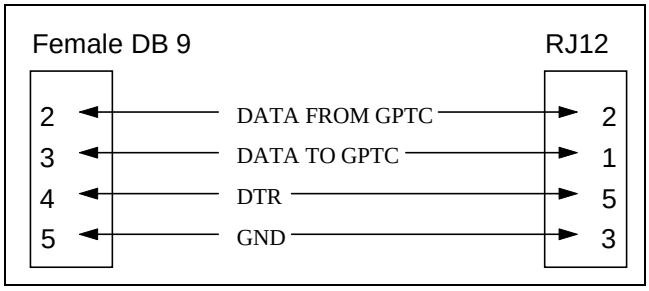


Figure 6 - Programming Cable (19B804346P111)

MAINTENANCE

RECOMMENDED TEST EQUIPMENT

The following equipment is required to test the GPTC:

- Oscilloscope
- Digital Voltmeter with fine tip probes
- Extender Board, ROA 117 2249 (Part of Test Module kit VPTS3X)
- Programming Cable, 19B804346P111 (Part of Test Module kit VPTS3X)

TESTING

An experienced technician can perform limited test and troubleshooting of the GPTC using the extender board to observe signals during operation. Individual resistors and capacitors may be replaced if care is used. The two soldering iron method is recommended. It is not recommended that ICs be replaced in the field.

NOTE

There are no adjustments on the GPTC.

TROUBLESHOOTING

When troubleshooting the GPTC, use the discussion in the Circuit Analysis section to help isolate problems. Use the extender board and the Test Point chart in Table 4 to check signals under operating conditions.

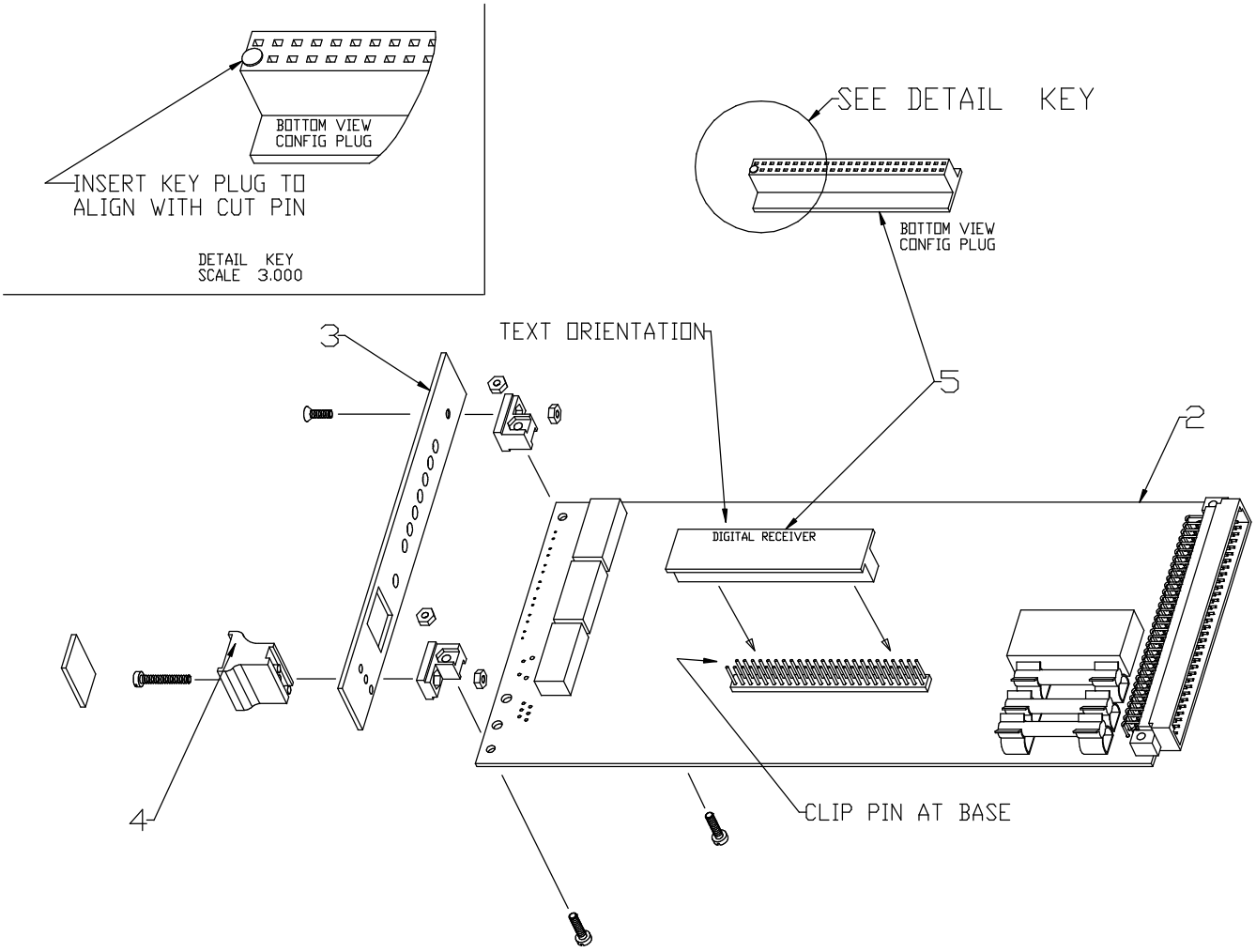
The Troubleshooting Chart provided in Table 5 lists some possible problems and recommended corrective action. Always check for correct configuration plug and proper installation of plug, DIP switch settings, socketted parts properly seated, blown fuses, and broken or missing parts.

Table 4 - Test Point Chart

TEST POINT	FUNCTION
TP30	OSC/2
TP31	GND
TP32	VCC
TP33	WALSH BIT 1
TP34	WALSH BIT 2
TP35	PH RECOVERED DATA
TP36	PH RX CLK
TP37	RF RCV DATA
TP38	RF RX CLK
TP39	PH TX CLK RS232
TP40	SYNC
TP41	BSL TX
TP101	RF TX DATA
TP102	INT0
TP103	VOL/SQ HI (RF DATA IN)
TP104	RF TX CLK
TP105	PH TX DATA
TP106	INT1
TP107	PH RX DATA

Table 5 - Troubleshooting Chart

SYMPTOM	AREA TO CHECK	POSSIBLE PROBLEM
RDY LED OFF after programming Flash PROM.	1. Programming may be corrupted, reprogram Flash PROM. 2. Ensure sufficient decay time is allowed before disconnecting the PC to GPTC programming cable. 3. Program will not load or loads incorrectly, DTR line to PC is not working.	1. The program "leafoff" controls the DTR out of the PC COMM port to turn on and off the +12 Vdc which must be applied to the Flash PROM on the GPTC in order to program it. 2. It is good practice to wait a few seconds after programming is over before unplugging the programming cable. This gives the +12 Vdc time to decay and avoids glitching the DTR while the +12 Vdc is still active. 3. When "leafoff" runs, DTR is at +12 Vdc (inactive state) initially, and FLASH_VPP on the GPTC is at 0V. When directed by the PC program, DTR goes to -12 Vdc causing FLASH_VPP to go to +12 Vdc. This prepares the Flash PROM for reprogramming. DTR is pin 20 on a DB25 connector and pin 4 on a DB-9 connector.
PC displays message "Radio not responding. Please cycle power on the radio."	1. Check voltage and fuses. 2. Check Programming cable. 3. Ensure Configuration plug and U26 are properly installed. 4. Initiate a reset.	1. Voltage at F1 should be +5 Vdc. Voltage at F2 should be +12 Vdc. Voltage at F3 should be -12 Vdc. 2. Disconnect and inspect Programming cable. Whenever cable is connected or disconnected the GPTC should initiate a reset. 3. Observe proper orientation of Configuration plug and U26, refer to GPTC Assembly diagrams for installation information. 4. A reset may be initiated by turning power off, removing and reinserting the GPTC, or by pressing the S4 Reset button on the front panel.



COMPACT VERTICAL VOTER DIGITAL RECEIVER

131 32-ROA 117 2240/1 Rev. B

SYMBOL	PART NUMBER	DESCRIPTION
2	ROA 117 2240, R2A	General Purpose Trunking Card Assembly. See separate Parts List.
3	SXA 120 4174/1	Digital Receiver Front Panel.
4	NTM 201 1079	Hardware Kit.
5	ROA 117 2242, R2A	Digital Receiver Configuration Plug Assembly. See separate Parts List.

PRODUCTION CHANGES

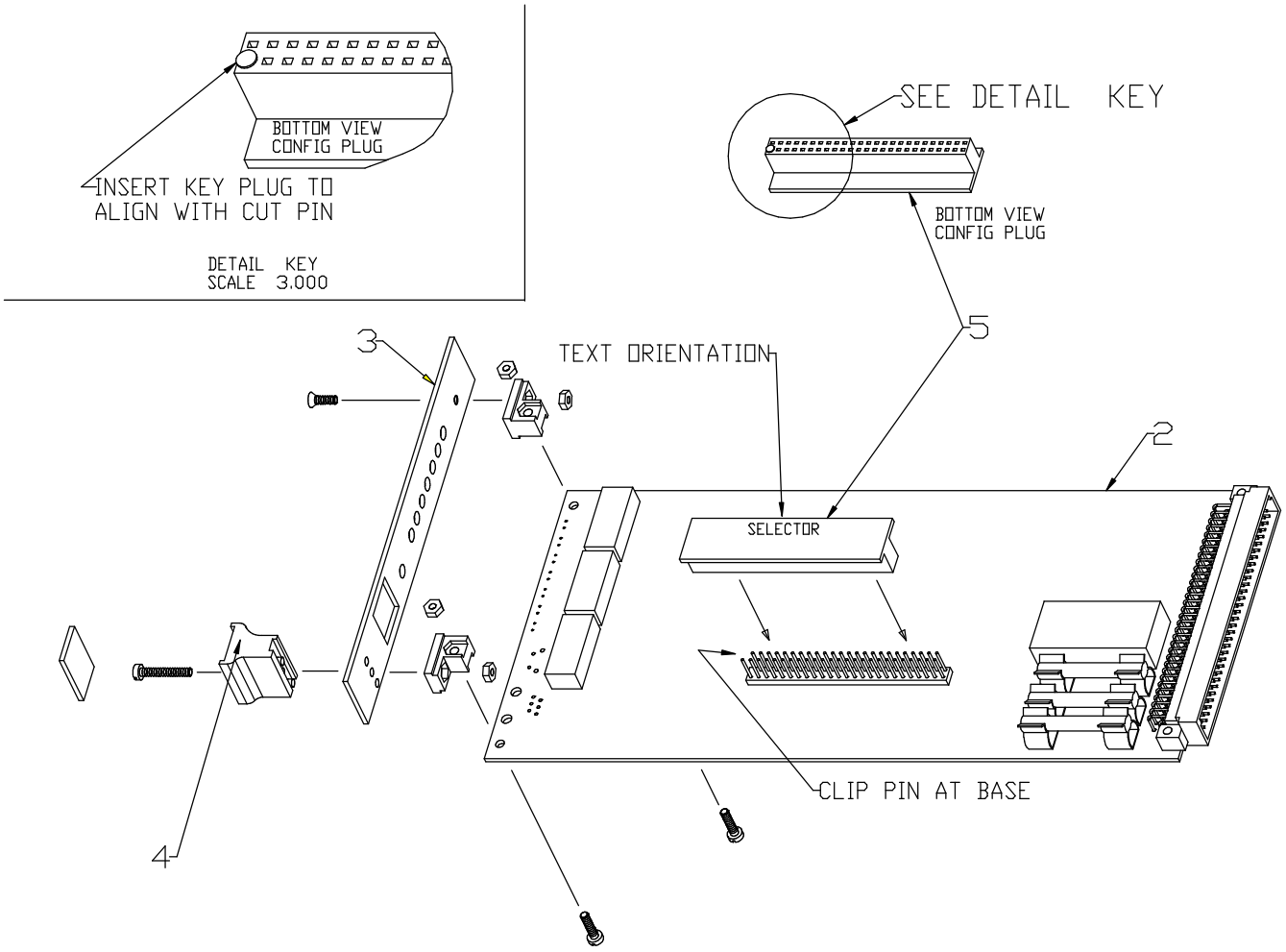
Changes in the equipment to improve performance or simplify circuits are identified by a "Revision Letter," which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the parts list for the descriptions of the parts affected by these revisions.

Rev. R2A - **ROA 117 2240/1**

Changes revision level of GPTC to Rev R2A and Digital Receiver Configuration Plug to Rev. R2A.

VOTER DIGITAL RECEIVER ASSEMBLY ROA 117 2240/1

(1/1078-ROA 117 2240/1, Sh. 1, Rev. A)



COMPACT VERTICAL VOTER SELECTOR

131 32-ROA 117 2240/2 Rev. B

SYMBOL	PART NUMBER	DESCRIPTION
2	ROA 117 2240, R2A	General Purpose Trunking Card Assembly. See separate Parts List.
3	SXA 120 4174/2	Selector Front Panel.
4	NTM 201 1079	Hardware Kit.
5	ROA 117 2241, R2A	Selector Configuration Plug Assembly. See separate Parts List.

PRODUCTION CHANGES

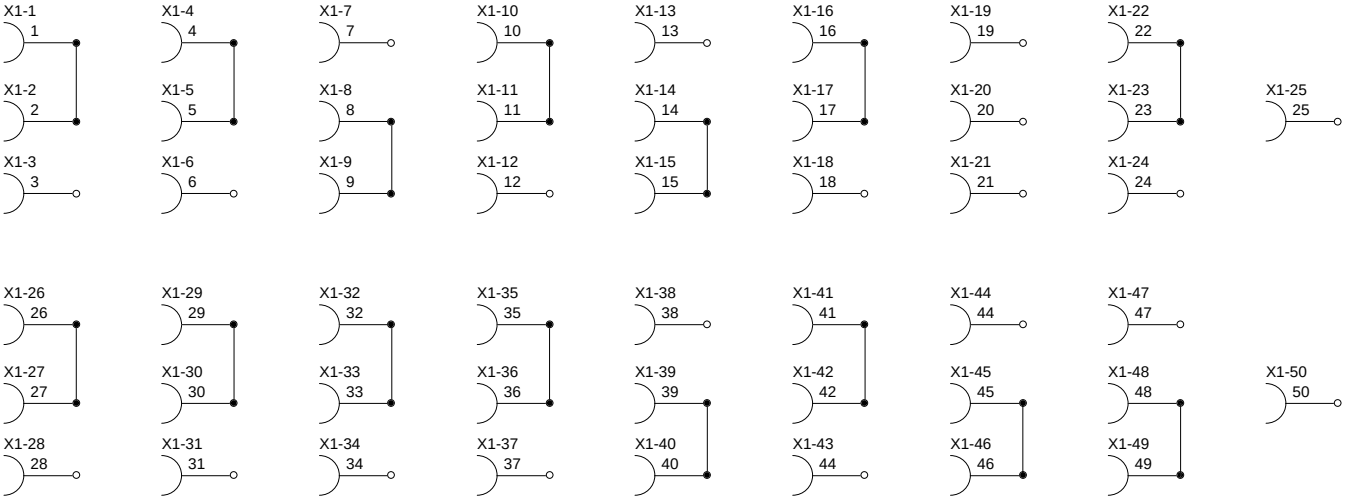
Changes in the equipment to improve performance or simplify circuits are identified by a "Revision Letter," which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the parts list for the descriptions of the parts affected by these revisions.

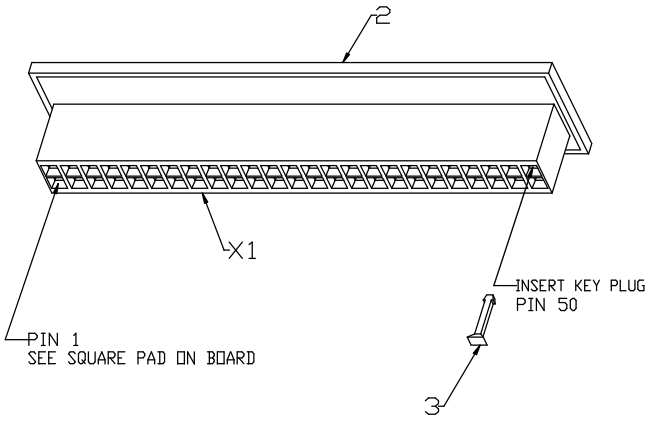
Rev. R2A - ROA 117 2240/2

Changes revision level of GPTC to Rev R2A and Selector Configuration Plug to Rev. R2A.

VOTER SELECTOR ASSEMBLY
ROA 117 2240/2

(1/1078-ROA 117 2240/2, Sh. 1, Rev. A)





DIGITAL RECEIVER CONFIGURATION PLUG

131 32-ROA 117 2242, Rev. B

SYMBOL	PART NUMBER	DESCRIPTION
2	TVA 117 2224, R2	Printed Wiring Board.
3	RNY 101 01/4	Keying plug.
X1	RNV 403 105/225	Connector, Receptacle, PWB mounted.

PRODUCTION CHANGES

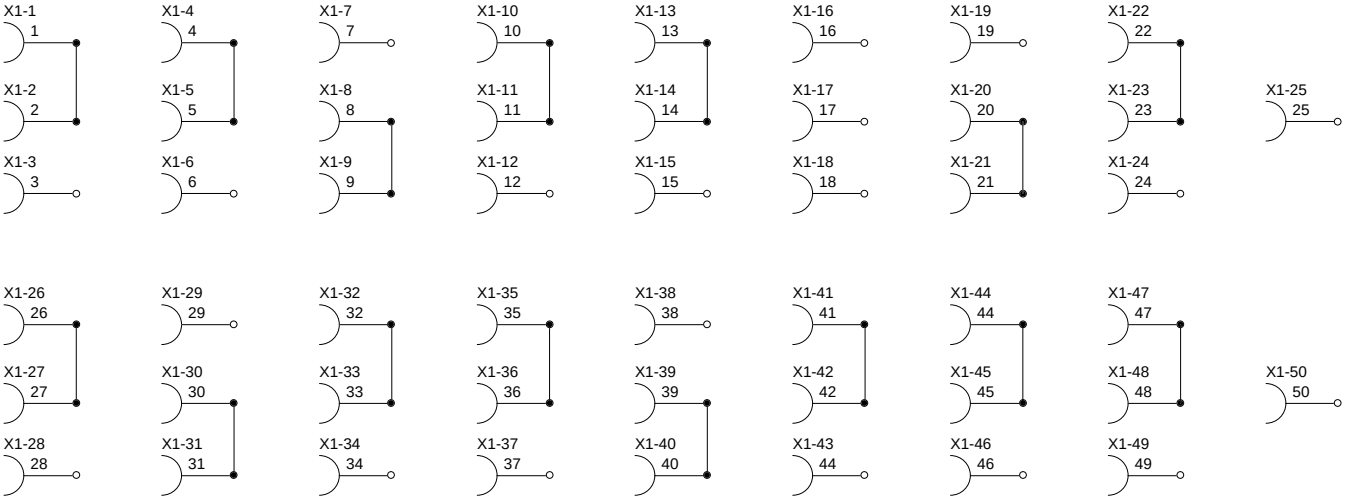
Changes in the equipment to improve performance or simplify circuits are identified by a "Revision Letter," which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the parts list for the descriptions of the parts affected by these revisions.

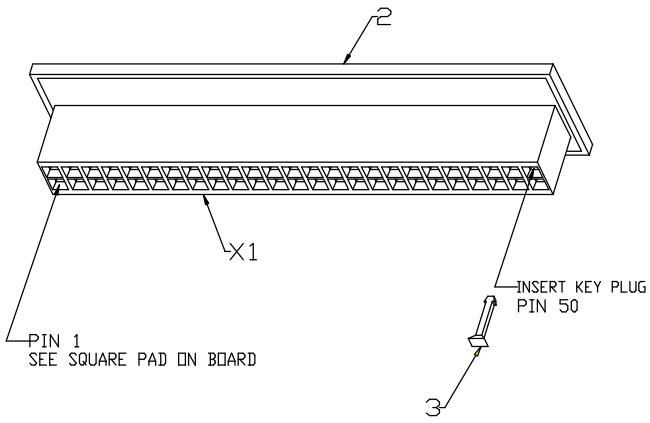
Rev. R2A - ROA 117 2242

Changes revision level of printed wiring board (item 2) from R1 to R2. Rev. R1 and R2 PWBs are functionally equivalent.

DIGITAL RECEIVER CONFIGURATION PLUG ROA 117 2242

(1911-ROA 117 2242 Sh. 1, Rev. A; 1078-ROA 117 2242, Sh. 1, Rev. B)





SELECTOR CONFIGURATION PLUG

131 32-ROA 117 2241, Rev. B

SYMBOL	PART NUMBER	DESCRIPTION
2	TVA 117 2223, R2	Printed Wiring Board.
3	RNY 101 01/4	Keying plug.
X1	RNV 403 105/225	Connector, Receptacle, PWB mounted.

PRODUCTION CHANGES

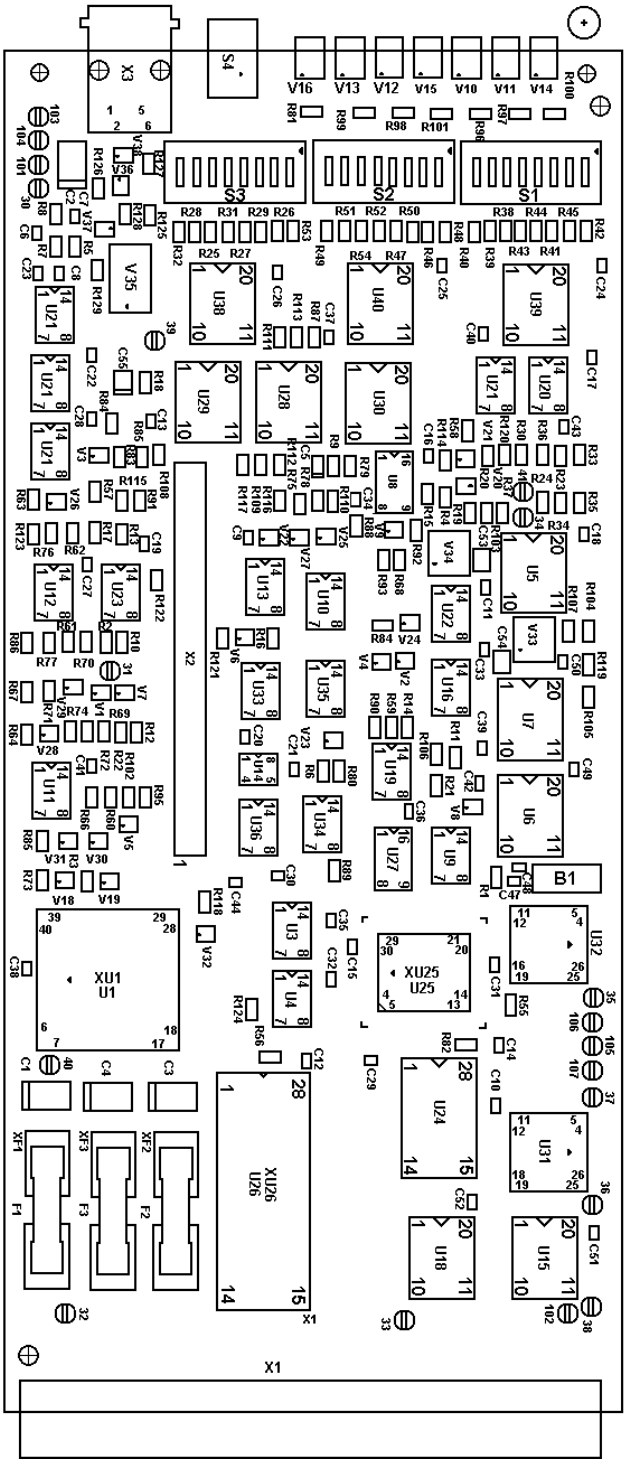
Changes in the equipment to improve performance or simplify circuits are identified by a "Revision Letter," which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the parts list for the descriptions of the parts affected by these revisions.

Rev. R2A - ROA 117 2241

Changes revision level of printed wiring board (item 2) from R1 to R2. Rev. R1 and R2 PWBs are functionally equivalent.

SELECTOR CONFIGURATION PLUG ROA 117 2241

(1911-ROA 117 2241 Sh. 1, Rev. A; 1078-ROA 117 2241, Sh. 1, Rev. B)



GPTC PRINTED WIRING BOARD ASSEMBLY
ROA 117 2240

(1078-ROA 117 2240, Sh. 1, Rev. A)

GENERAL PURPOSE TRUNKING CARD (GPTC)
PRINTED WIRING BOARD ASSEMBLY

131 32-ROA 117 2240, Revision C

SYMBOL	PART NUMBER	DESCRIPTION
		---------- CRYSTALS----------
B1	RTM 501 658/01	Quartz crystal unit; 11.0592 MHz.
		---------- CAPACITORS----------
C1 thru C4	RJE 584 3168/47	Tantalum, electrolytic SMD: 47 µF, ±20%, 16 V.
C5	RJE 584 3107/22	Tantalum, electrolytic SMD: 2.2 µF, ±20%, 10V.
C6 thru C44	RJC 464 3045/1	Monolithic ceramic chip: 10 nF, ±10%, 50V.
C47 and C48	RJC 463 4042/27	Monolithic ceramic chip: 27 pF ±5%, 50V.
C49 thru C52	RJC 464 3045/1	Tantalum, electrolytic SMD: 2.2 µF, ±20%, 10V.
C53 and C54	RJC 463 4074/1	Monolithic ceramic chip: 1.0 nF ±5% 50V.
C55	RJE 584 3167/22	Tantalum, electrolytic SMD: 2.2 µF ±20% 16V.
		---------- FUSES ----------
F1	NGH 241 04/1	FUSE: 1A, slow action 250V, glass 5 x 20mm.
F2	NGH 241 03/25	FUSE: 0.25A, slow action 250V, glass 5 x 20mm.
F3	NGH 241 03/25	FUSE: 0.25A, slow action 250V, glass 5 x 20mm.
		---------- RESISTORS ----------
R1	REP 625 428/1	Ceramic chip: 10 Meg, 5%, 1/8w.
R2 thru R11	REP 625 426/1	Ceramic chip: 100K, 5%, 1/8w.
R12 and R13	REP 625 425/47	Ceramic chip: 47K, 5%, 1/8w.
R14 and R15	REP 625 425/27	Ceramic chip: 27K, 5%, 1/8w.
R16	REP 625 425/22	Ceramic chip: 22K, 5%, 1/8w.
R17	REP 625 425/12	Ceramic chip: 12K, 5%, 1/8w.
R18	REP 625 425/1	Ceramic chip: 10k, 5%, 1/8w.
R19	REP 625 423/1	Ceramic chip: 100 Ohm, 5%, 1/8w.
R20	REP 625 423/51	Ceramic chip: 510 Ohm, 5%, 1/8w.
R21 thru R87	REP 625 425/1	Ceramic chip: 10K, 5%, 1/8w.
R88 and R89	REP 625 424/47	Ceramic chip: 4.7K, 5%, 1/8w.
R90 and R91	REP 625 424/39	Ceramic chip: 3.9K, 5%, 1/8w.
R92 thru R95	REP 625 424/22	Ceramic chip: 2.2K, 5%, 1/8w.
R96 thru R102	REP 625 424/1	Ceramic chip: 1K, 5%, 1/8w.
R103 and R104	REP 625 424/39	Ceramic chip: 3.9K, 5%, 1/8w.
R105	REP 625 423/51	Ceramic chip: 510 Ohm, 5%, 1/8w.
R106	REP 625 423/47	Ceramic chip: 470 Ohm, 5%, 1/8w.
R107 thru R117	REP 625 423/1	Ceramic chip: 100 Ohm, 5%, 1/8w.
R118	REP 625 425/1	Ceramic chip: 10K, 5%, 1/8w.
R119 and R120	REP 625 423/51	Ceramic chip: 510 Ohm, 5%, 1/8w.
R121 thru R123	REP 625 425/1	Ceramic chip: 10K, 5%, 1/8w.
R124	REP 625 424/1	Ceramic chip: 1K, 5%, 1/8w.
R125 and R126	REP 625 426/1	Ceramic chip: 100K, 5%, 1/8w.
R127 thru R129	REP 625 425/1	Ceramic chip: 10K, 5%, 1/8w.
		---------- SWITCHES ----------
S1 thru S3	RMF 356 004/08	Switch, DIP; sim to CTS 206-8.
S4	RMD 955 006/01	Switch, Push Button.
		---------- TEST POINTS ----------
TP30 thru TP107	RPV 380 902/01	Connector, test point 1 pole.

SYMBOL	PART NUMBER	DESCRIPTION
		-------INTEGRATED CIRCUITS -------
U1	RYT 123 6037/C	Digital: 8-bit microcomputer; sim to P80C32.
U2	RYT 101 321/C	Linear: Quad Voltage Comparator; sim to LM339.
U3 and U4	RYT 318 0000/C	Digital: 4x2 In NAND Gate; sim to 74AC00.
U5 thru U7	RYT 306 2031/C	Digital: CMOS 8-Bit Flip-flop; sim to 74HC273.
U8	RYT 306 2024/C	Digital: CMOS 2 x Monostable Multivbrator; sim to 74HC4538.
U9 thru U13	RYT 306 2020/C	Digital: CMOS 6 x Inverter, Schmitt Trigger; sim to 74HC14.
U14	RYT 113 6065/1	Digital: Microprocessor Supervisory Reset Circuit; sim to MAX705CSA.
U15	RYT 306 2013/C	Digital: CMOS Octal Tri-state Transceiver; sim to 74HC245.
U16	RYT 306 2006/C	Digital: CMOS Quad 2-Input NOR Gate; sim to 74HC02.
U17	RYT 306 2003/C	Digital: CMOS Dual Data Flip-flop; sim to 74HC74.
U18	RYT 304 0373/C	Digital: Octal Data Latch; sim to 74HC373.
U19 thru U23	RYT 202 106/C	Digital: Hex Open Collector Inverter; sim to 7406.
U24	RYT 119 6005/4C	Digital: 32K x 8 Static RAM; sim to ECI55257AFL.
U25	RYT 118 6040/C	Digital: CMOS 64K x 8 Flash Memory; sim to 28F512S200.
U26	RON 107 756/1	Preprogrammed 512K byte UV EPROM; part of Media kit 3501521G1.
U27	RYT 116 006/C	Digital: Dual 2-to-1 Decoder/Demultiplexer; sim to 74LS155.
U28 thru U30	RYT 109 082/C	Digital: High-speed RS-232 Driver/Receiver; sim to MAX233.
U31 and U32	ROP 101 688/C	Integrated Circuit, Modem.
U33 thru U37	RYT 306 2001/C	Digital: CMOS QUAD 2-Input NAND Gate; sim to 74HC00.
U38 thru U40	RYT 306 2012/C	Digital: Octal Tri-state Buffer; sim to 74HC244.
		-----DIODES and TRANSISTORS ----
V1 thru V8	RYN 121 675/1	Transistor, Silicon, NPN, low profile; sim to MMBT3904
V9	RYN 120 619/1	Transistor, Silicon, PNP, low profile; sim to MMBT3906
V10 thru V16	RKZ 433 637/1	Light Emitting Diode: 90 degree RED, T1 package.
V18 thru V32	RKZ 123 03/1	Diode, Dual - switching; sim to BAV99, SOT-23.
V33 and V34	RYN 123 621/1	FET, medium power N-channel enhancement mode; sim to BSP29, SOT-223.
V35	RYN 122 623/1	FET, Power P-channel enhancement mode; sim to MTD406.
V36 and V37	RYN 121 675/1	Transistor, Silicon, NPN, low profile; sim to MMBT3904
V38	RKZ 123 03/1	Diode, Dual - switching; sim to BAV99, SOT-23.
		----------CONNECTORS ----------
X1	RPV 403 209/102	Connector, 96 contact.
X2	RPV 380 220/225	Connector, double row pin strip.
X3	RNV 403 19/06	Connector, socket.
		-------- SOCKETS & HOLDERS--------
XF1 thru XF3	NFN 102 04	Holder, fuse.
XU1	RNK 860 12/044	Holder PLCC 44-pole.
XU25	RNK 860 11/1	Holder PLCC 32-pole; sim to AMP 822034-1.
XU26	RNK 841 001/28	Holder DIL 28-pole.

PRODUCTION CHANGES

Changes in the equipment to improve performance or simplify circuits are identified by a "Revision Letter," which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the parts list for the descriptions of the parts affected by these revisions.

Rev. R1B - ROA 117 2240

Change added Crystal B1 to parts list.

Rev. R2A - ROA 117 2240

Changes revision level of printed wiring board (item 2, TVK 117 2217) from R1 to R2. Rev. R1 and R2 PWBs are functionally equivalent.

Changes connector X3 from RNV 256 103 to RNV 403 19/06.

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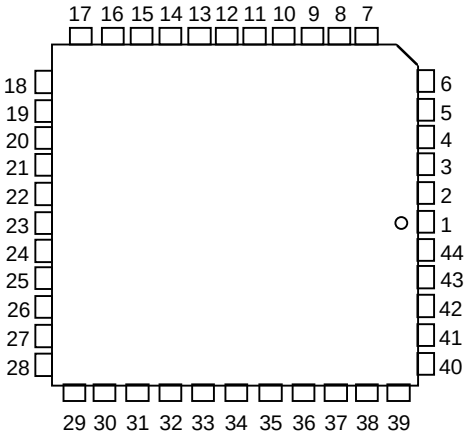
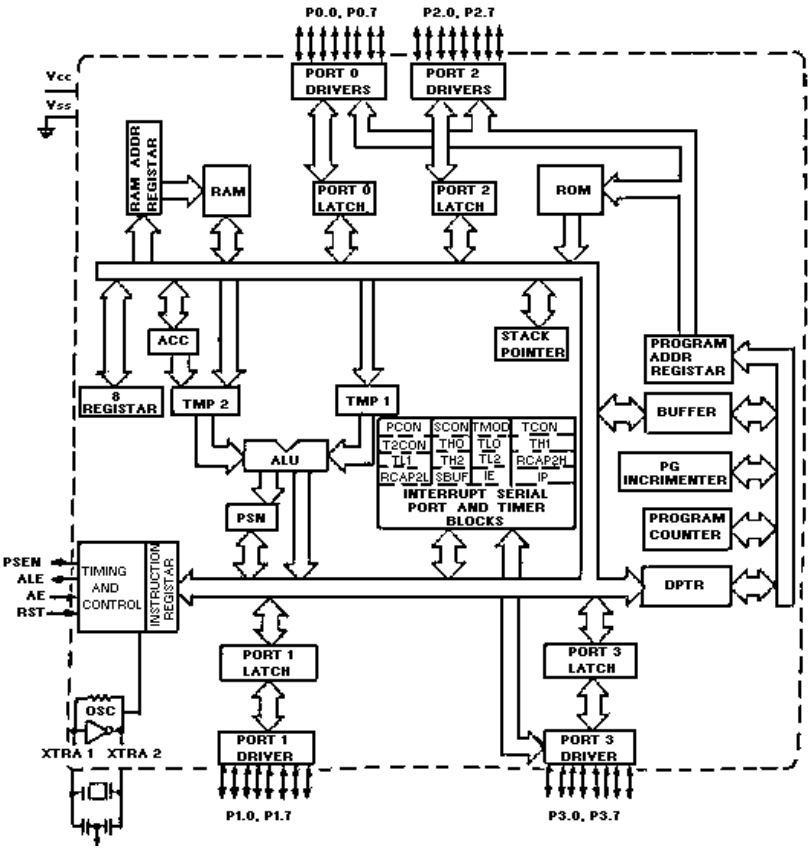
8-BIT MICROPROCESSOR - U1
RYT 123 6037/C (P80C32)



CAUTION
OBSERVE PRECAUTIONS FOR HANDLING **ELECTROSTATIC SENSITIVE DEVICES**

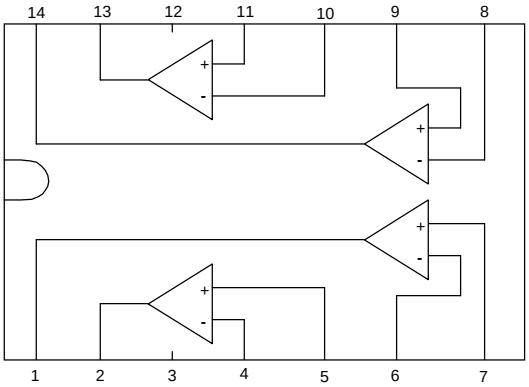
FUNCTION DIAGRAM



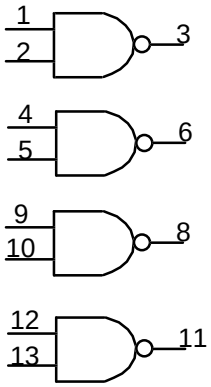
PIN	FUNCTION	PIN	FUNCTION
1	NC	23	NC
2	T2/P1.0	24	P2.0/A8
3	T2EX/P1.1	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6	30	P2.6/A14
9	P1.7	31	P2.7/A15
10	RST	32	$\overline{\text{PSEN}}$
11	RxD/P3.0	33	ALE/$\overline{\text{PROG}}$
12	NC	34	NC
13	TxD/P3.1	35	EA/Vpp
14	$\overline{\text{INT0}}$/P3.2	36	P0.7/AD7
15	$\overline{\text{INT1}}$/P3.3	37	P0.6/AD6
16	T0/P3.4	38	P0.5/AD5
17	$\overline{\text{T1}}$/P3.5	39	P0.4/AD4
18	$\overline{\text{WR}}$/P3.6	40	P0.3/AD3
19	RD/P3.7	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	Vss	44	Vcc

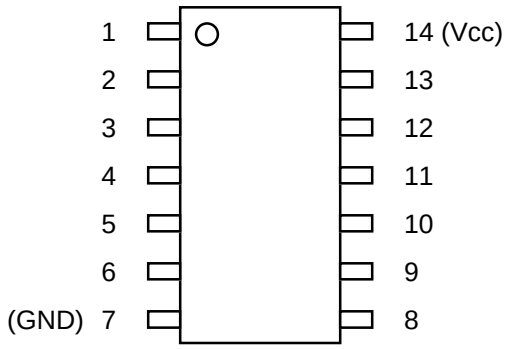
U2 - QUAD VOLTAGE COMPARATOR
RYT 101 321/C (LM339)

TERMINAL	FUNCTION
3	Positive voltage supply
12	Negative voltage supply
	Opamp 1
4	Inverting input (-IN)
5	Noninverting input (+IN)
2	Output
	Opamp 2
6	Inverting input (-IN)
7	Noninverting input (+IN)
1	Output
	Opamp 3
8	Inverting input (-IN)
9	Noninverting input (+IN)
14	Output
	Opamp 4
10	Inverting input (-IN)
11	Noninverting input (+IN)
13	Output



U3 AND U4- NAND GATE
RYT 318 0000/C (74AC00)



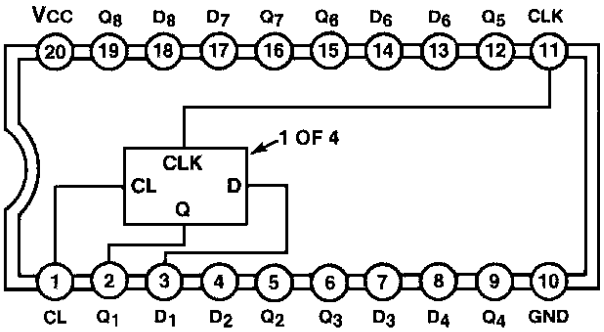


TRUTH TABLE

INPUTS		OUTPUTS
A1 (A2,A3,A4)	B1 (B2,B3,B4)	O1 (O2,O3,O4)
L	L	H
L	H	H
H	L	H
H	H	L

CMOS OCTAL DATA FLIP-FLOP - U5, U6 & U7
RYT 306 2031/C (74HC273)

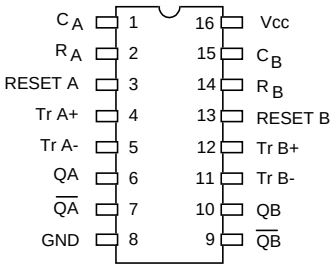
CAUTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES



INPUTS		OUTPUTS	
CLEAR	CLOCK	D	Q
Ø	X	X	Ø
1		1	1
1		Ø	Ø
1	Ø	X	Q_0

X = DON'T CARE Q_0 = Q BEFORE

CMOS 2 X MONOSTABLE MULTIVIBRATOR - U8
RYT 306 2024/C (74HC4538)



FUNCTION TABLE

INPUTS			OUTPUTS	
Reset	+Triggr	- Trigg	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎍
H	↑	H	⎍	⎍

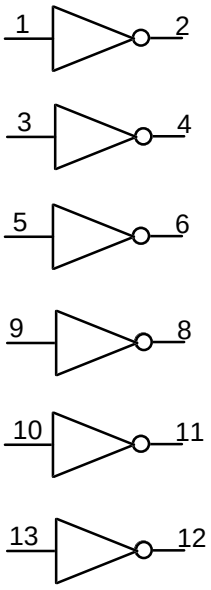
X = H or L

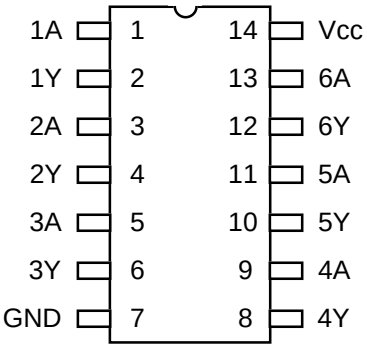
↑ = from L to H

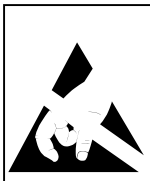
↓ = from H to L

CAUTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

U9 THRU U13 - 6 X INVERTER, SCHMITT TRIGGER
RYT 306 2020/C (74HC14)

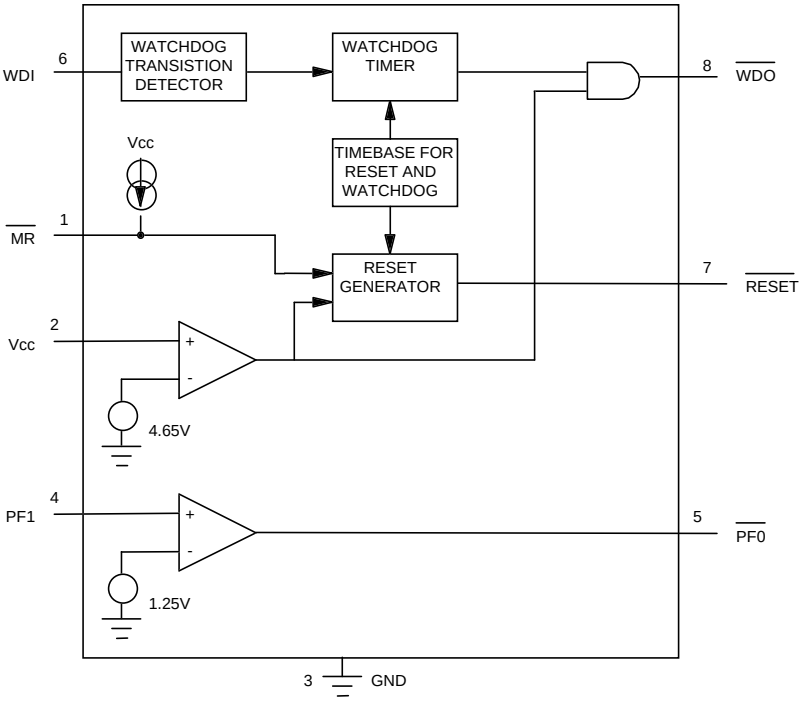


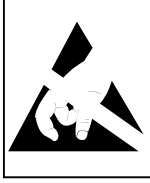




CAUTION
OBSERVE PRECAUTIONS FOR HANDLING **ELECTROSTATIC SENSITIVE DEVICES**

U14 - MICROPROCESSOR SUPERVISORY CIRCUIT
RYT 113 6065/1 (MAX705CSA)

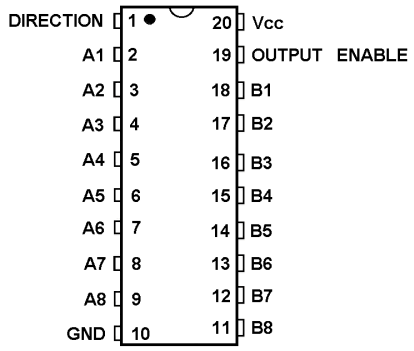




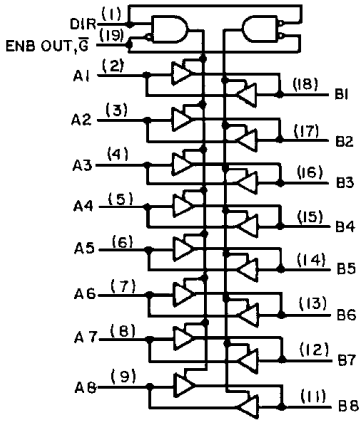
CAUTION
OBSERVE PRECAUTIONS FOR HANDLING **ELECTROSTATIC SENSITIVE DEVICES**

U15 - CMOS OCTAL TRI-STATE TRANSCEIVER
RYT 306 2013/C (74HC245)

PIN ASSIGNMENT



LOGIC DIAGRAM (POSITION LOGIC)



PIN 10 = GND
PIN 20 = Vcc

CAUTION
OBSERVE PRECAUTIONS FOR HANDLING **ELECTROSTATIC SENSITIVE DEVICES**

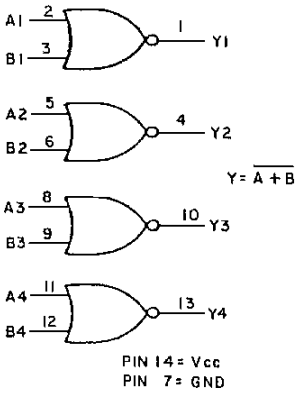
FUNCTION TABLE

CONTROL INPUTS		OPERATION
OUTPUT ENABLE	DIRECTION	
L	L	DATA TRANSMITTED FROM BUS B TO BUS A
L	H	DATA TRANSMITTED FROM BUS A TO BUS B
H	X	BUSES ISOLATOR (HIGH IMPEDANCE STATE)

X=DON'T CARE

U16
CMOS QUAD 2-INPUT NOR GATE
RYT 306 2006/C (74HC02)

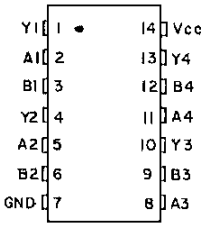
LOGIC DIAGRAM



$Y = \overline{A + B}$

PIN 14 = Vcc
PIN 7 = GND

PIN ASSIGNMENT

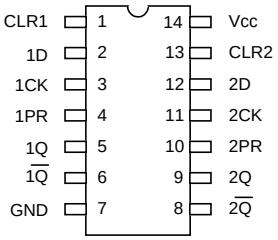


FUNCTION DIAGRAM

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

CAUTION
OBSERVE PRECAUTIONS FOR HANDLING **ELECTROSTATIC SENSITIVE DEVICES**

U17
CMOS DUAL DATA FLIP-FLOP
RYT 306 2003/C (74HC74)



FUNCTION TABLE

INPUTS				OUTPUTS	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	H	L	X	H*	H*
H	L	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

X = Any input, including transistion

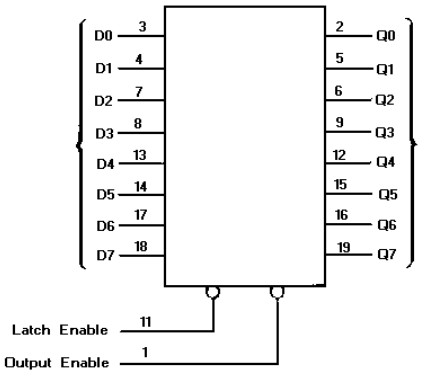
↑ = from L to H

Q_0 = The level of Q after the previous clock pulse

* = Nonstable; don't persist when PR and CLR are set high

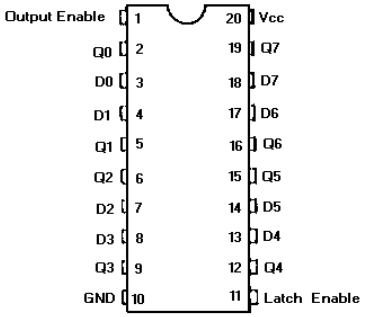
U18 - OCTAL DATA LATCH
RYT 304 0373/C (74HC373)

BLOCK DIAGRAM



Pin 20 = Vcc
Pin 10 = GND

PIN ASSIGNMENT

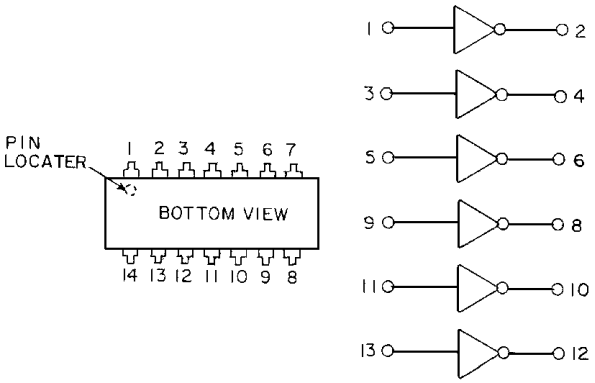


FUNCTION TABLE

Output Enable	Latch Enable	D	Output
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

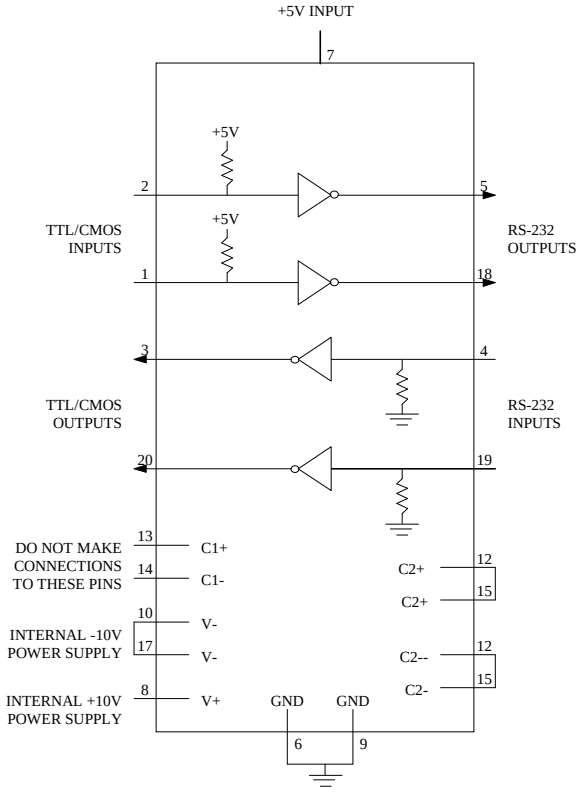
X = don't care
Z = high impedance

U19 THRU U23
HEX OPEN COLLECTOR INVERTER
RYT 202 106/C (7406)

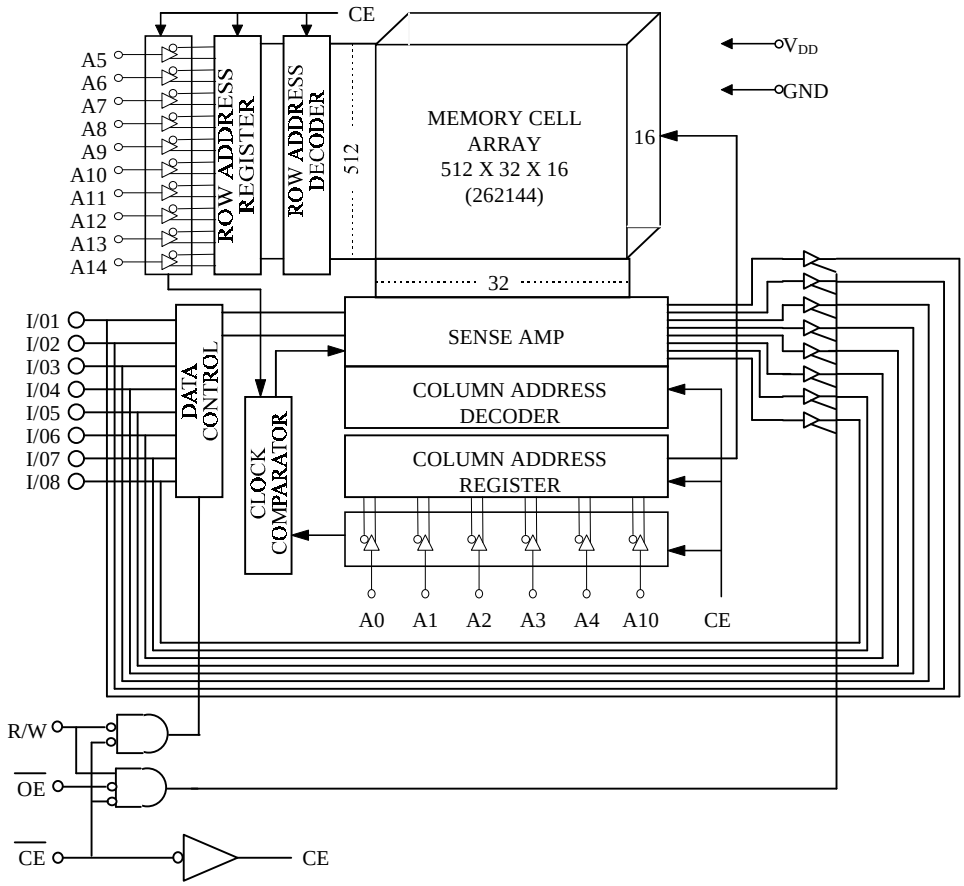


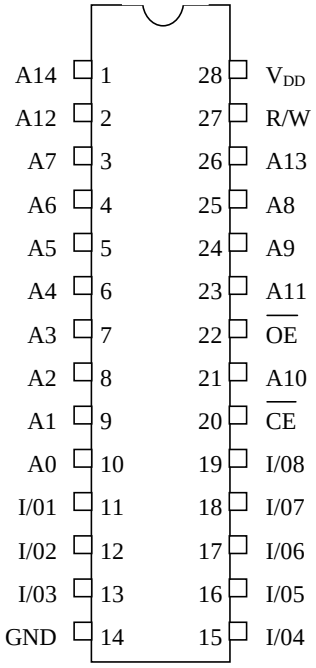
GND = 7
Vcc = 14

U28 THRU U30
RS-232 DRIVER/RECEIVER
RYT 109 082/C (MAX233)



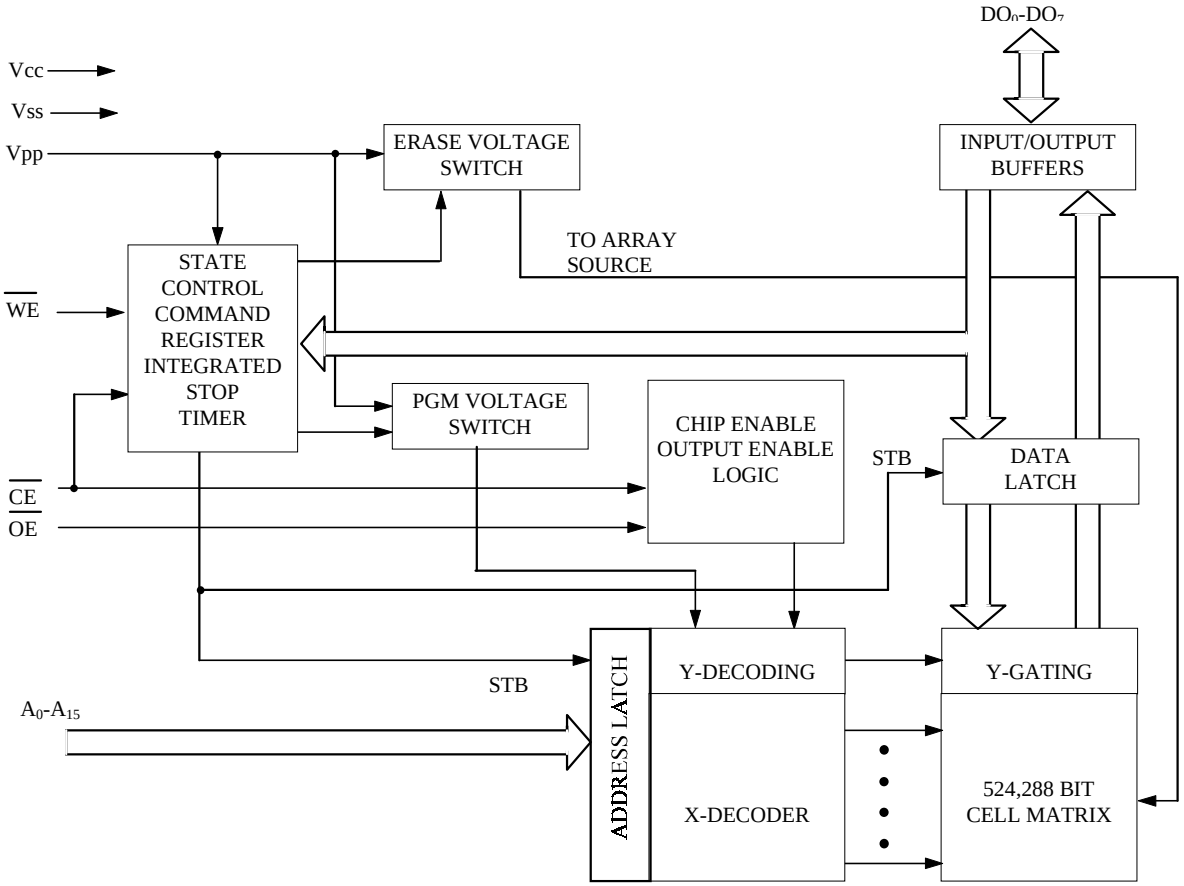
U24
32K X 8 STATIC RAM
RYT 119 6005/4C (EC155257AFL)

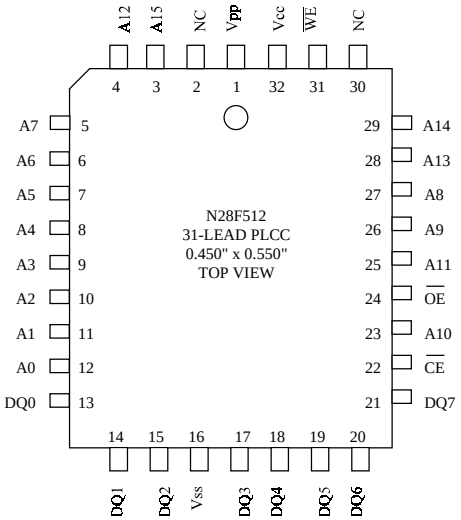




PIN NAMES	FUNCTION
A0 thru A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
I/01 thru I/08	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

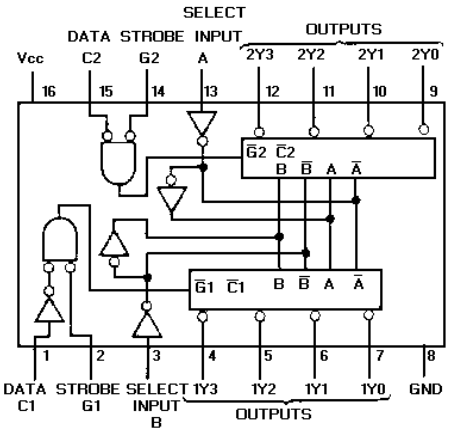
U25
CMOS 64K X 8 FLASH MEMORY
RYT 118 6040/C (28F512S200)





SYMBOL	TYPE	NAME AND FUNCTION
A_0-A_{15}	Input	ADDRESS INPUT for memory address. Addresses are internally latched during a write cycle.
DQ_0-DQ_7	Input/Output	DATA INPUT/OUTPUT: Inputs data during memory write cycles; outputs data during memory read cycles.
$\overline{CE}$	Input	CHIP ENABLE: Activates the device's control logic, input buffers, decoders, and sense amplifiers.
$\overline{OE}$	Input	OUTPUT ENABLE: Gates the devices output through the databuffers during a read cycle.
$\overline{WE}$	Input	WRITE ENABLE: Controls writes to the control register and the array.
Vpp		ERASE/PROGRAM SUPPLY for writing the command register, erasing the entire array, or programming bytes in the array.
Vcc		Device Power Supply. (5V ±10%)
Vss		Ground
NC		No connection to device.

U27 - DUAL 2-TO-1 DECODER/DEMULTIPLEXER
RYT 116 006/C (74LS155)

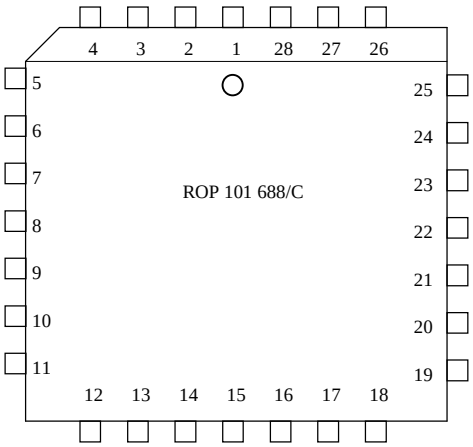


2-Line-to-4-Line Decoder
or 1-Line-to-4-Line Demultiplexer

Inputs			Outputs			
Select	Strobe	Data				
B A	G1	C1	1Y0	1Y1	1Y2	1Y3
X X	H	X	H	H	H	H
L L	L	H	L	H	H	H
L H	L	H	H	L	H	H
H L	L	H	H	H	L	H
H H	L	H	H	H	H	L
X X	X	L	H	H	H	H

Inputs			Outputs			
Select	Strobe	Data				
B A	G2	C2	2Y0	2Y1	2Y2	2Y3
X X	H	X	H	H	H	H
L L	L	L	L	H	H	H
L H	L	L	H	L	H	H
H L	L	L	H	H	L	H
H H	L	L	H	H	H	L
X X	X	H	H	H	H	H

U31 AND U32 - MODEM
ROP 101 688/C

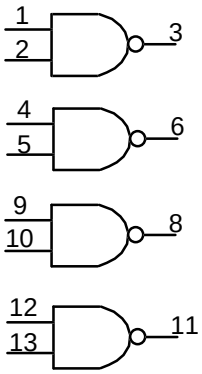


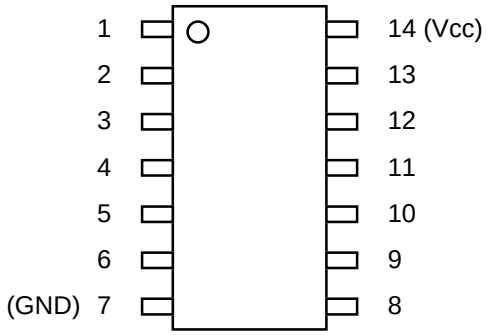
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	RE	Read Enable (active low).
2	EN	Chip Enable (active low).
3	RESOUT	Resout Output (active high).
4	AD0	Bi-directional Address/Data Bus.
5	AD1	Bi-directional Address/Data Bus.
6	AD2	Bi-directional Address/Data Bus.
7	AD3	Bi-directional Address/Data Bus.
8	AD4	Bi-directional Address/Data Bus.
9	AD5	Bi-directional Address/Data Bus.
10	AD6	Bi-directional Address/Data Bus.
11	AD7	Bi-directional Address/Data Bus.
12	ALE	Address Latch Enable (active high).
13	VSS	Ground.
14	CLK1	Buffered Oscillator Output.
15	VDD	Power Supply.
16	XTAL1	Oscillator Input.
17	XTAL2	Oscillator Output.
18	CLK2	640 kHz Output.
19	DATAIN	Received Data Input.
20	SAT/G1	Received SAT Input/G1 EN.HC138 (active high).
21	TXDAT	Transmit Data Output.
22	RCVCLK/ Q2	Recovered Clock Output/Q2 Output for HC138).
23	RCVCLK/ Q0	Recovered Clock Output/Q0 Output for HC138).
24	INT	Interrupt Request (active low O.D.).
25	RESIN	Reset Input (active high).
26	CS	Chip Select (active low).
27	CLK3/4	Transmit Clock Output/CLK1/6 Output.
28	WR	Write Enable (active low).

U33 THRU U37
CMOS QUAD TWO INPUT NAND GATE
RYT 306 2001/C (74HC00)

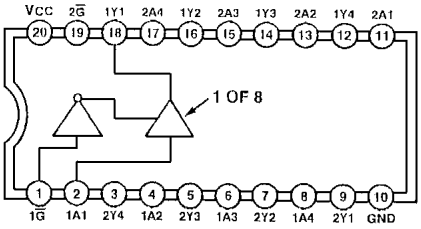
TRUTH TABLE

INPUTS		OUTPUTS
Pin 1 (4, 9, 12)	Pin 2 (5, 10, 13)	Pin 3 (6, 8, 11)
L	L	H
L	H	H
H	L	H
H	H	L





U38 THRU U40
OCTAL TRI-STATE BUFFER
RYT 306 2012/C (74HC244)



$\overline{1G}$	1A	1Y	$\overline{2G}$	2A	2Y
Ø	Ø	Ø	Ø	Ø	Ø
Ø	1	1	Ø	1	1
1	Ø	Z	1	Ø	Z
1	1	Z	1	1	Z

Z = HIGH IMPEDANCE

ADDENDUM NO. 1 TO LBI-39151

PURPOSE

This addendum corrects typographic errors in the manual.

Page 9, Voter Programming

Replace the first paragraph in the "**Voter Programming**" section (right column) as follows:

Currently Reads	Change to Read
Voter Programming The loadable Voter software must reside on the PC OR floppy disk as an Intel Hex file. The "leafoff.exe" file is the executable program which loads the Voter hex file into the Digital Receiver or Selector. Both files should be in the same directory.	**Voter Programming** The loadable Voter software must reside on the PC or floppy disk as an Intel Hex file. The "leafoff.exe" file is the executable program which loads the Voter hex file into the Digital Receiver or Selector. Both files should be in the same directory.

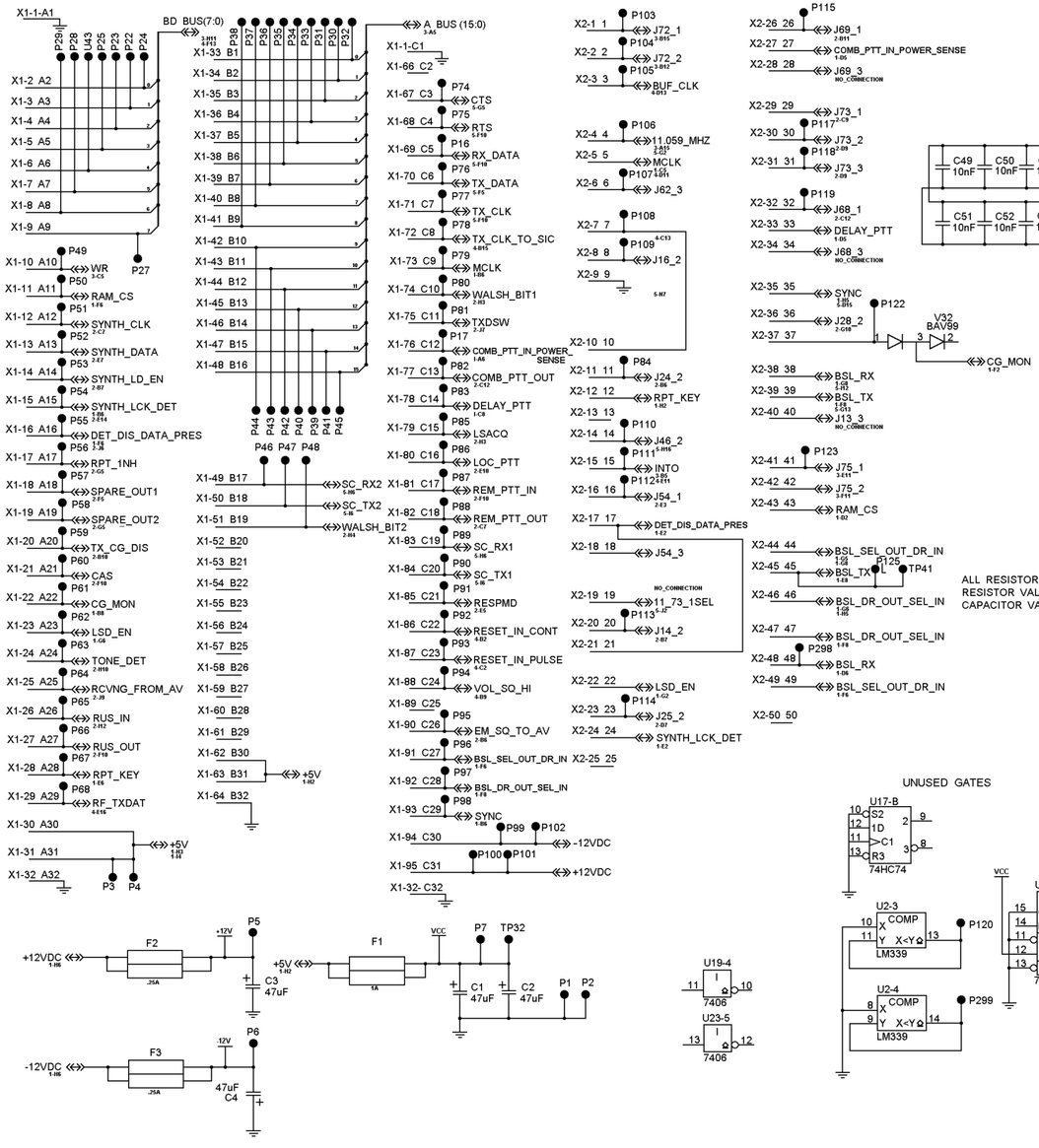
Page 26, Parts List

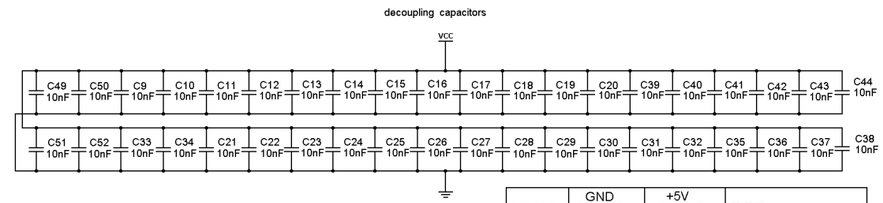
Replace the Description for U26 in the GPTC parts list as follows:

Currently Reads	Change to Read
Preprogrammed 512K byte UV EPROM; part of Media kit 3501521G1.	Preprogrammed 512K byte UV EPROM; part of Media kit 350A1521G1.

Ericsson Inc.
Private Radio Systems
Mountain View Road
Lynchburg, VA 24502
1-800-528-7711 (Outside USA, 804-528-7711)

Printed in U.S.A.



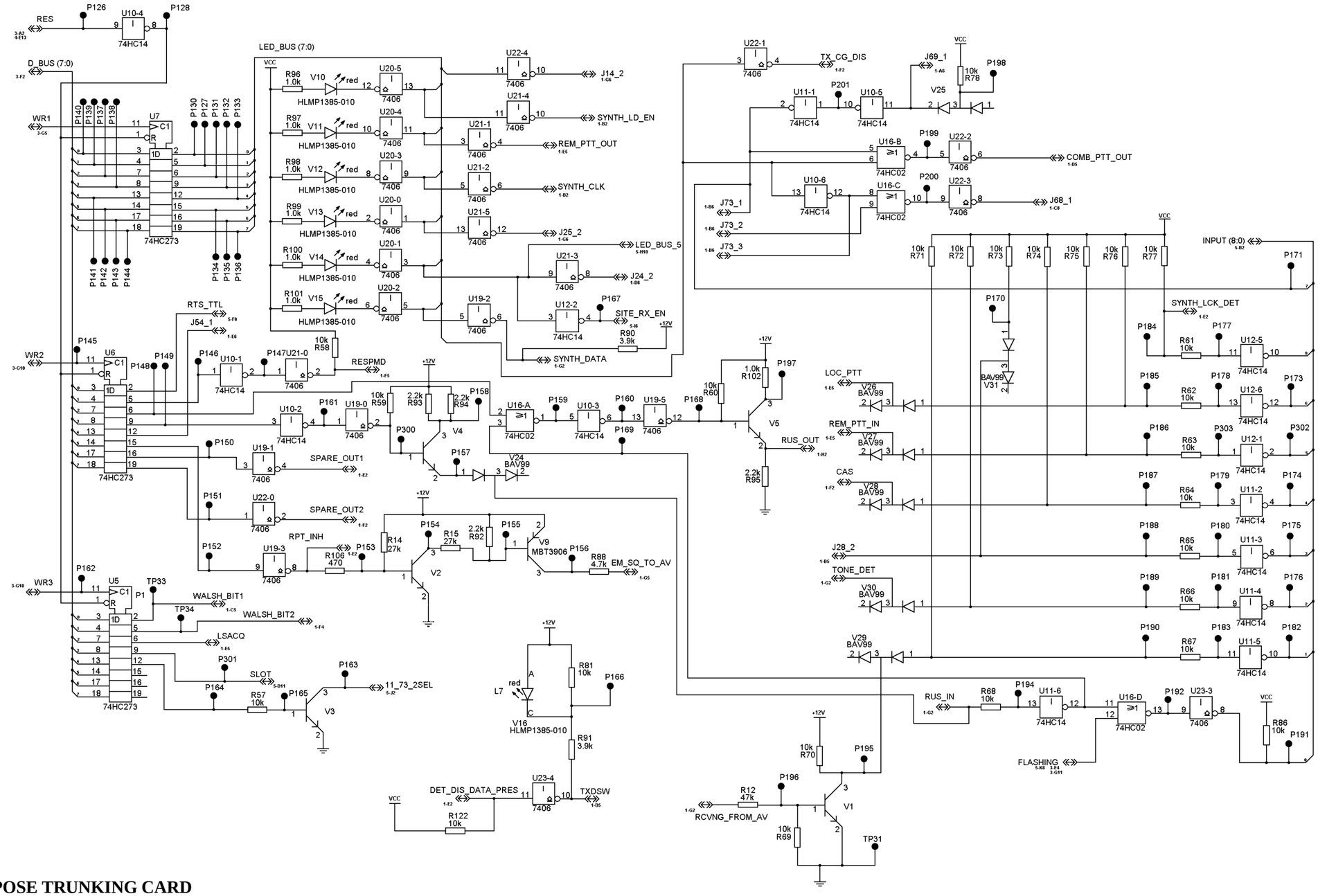


DEVICE	GND PIN NO	+5V PIN NO	TYPE
U1	22,23	44	80C32
U2	12	3	LM339
U3	7	14	74AC00
U4	7	14	74AC00
U5	10	20	74HC273
U6	10	20	74HC273
U7	10	20	74HC273
U8	8	16	74HC4538
U9	7	14	74HC14
U10	7	14	74HC14
U11	7	14	74HC14
U12	7	14	74HC14
U13	7	14	74HC14
U14	3	2	MAX705CSA
U15	10	20	74HC245
U16	7	14	74HC02
U17	7	14	74HC74
U18	10	20	74HC373
U19	7	14	7406
U20	7	14	7406
U21	7	14	7406
U22	7	14	7406
U23	7	14	7406
U24	14	28	TC5527AFL
U25	16	32	28F512S120
U26	14	28	27C512
U27	8	16	74LS155
U28	6,9	7	MAX233A
U29	6,9	7	MAX233A
U30	6,9	7	MAX233A
U31	13	15	MODEM
U32	13	15	MODEM
U33	7	14	74HC00
U34	7	14	74HC00
U35	7	14	74HC00
U36	7	14	74HC00
U37	7	14	74HC00
U38	10	20	74HC244
U39	10	20	74HC244
U40	10	20	74HC244

ALL RESISTORS ARE 1/8 WATT UNLESS OTHERWISE INDICATED
RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY MULTIPLIER K OR M.
CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER U, N OR P.

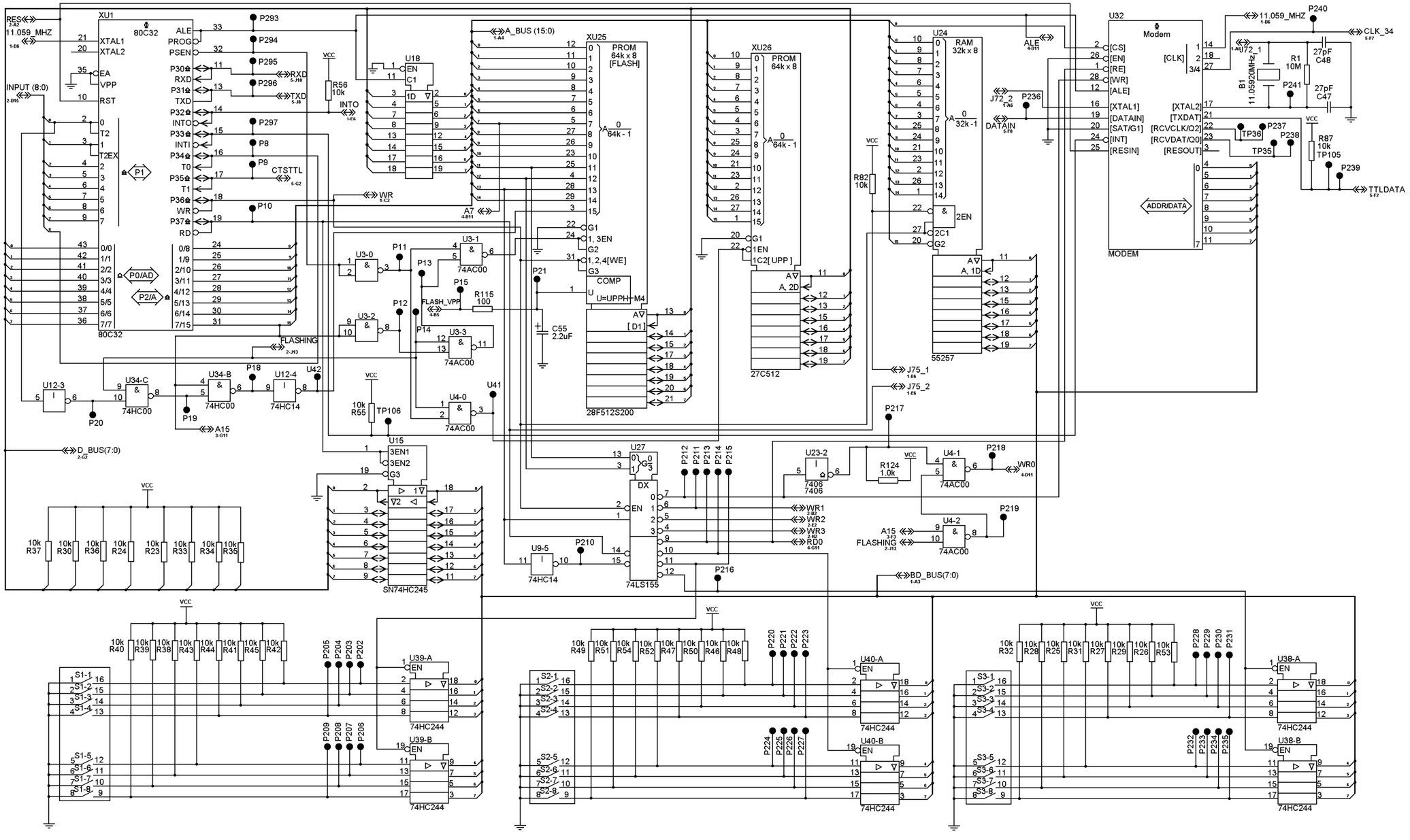
GENERAL PURPOSE TRUNKING CARD
ROA 117 2240

(1911-ROA 117 2240, SH. 1, Rev. A)



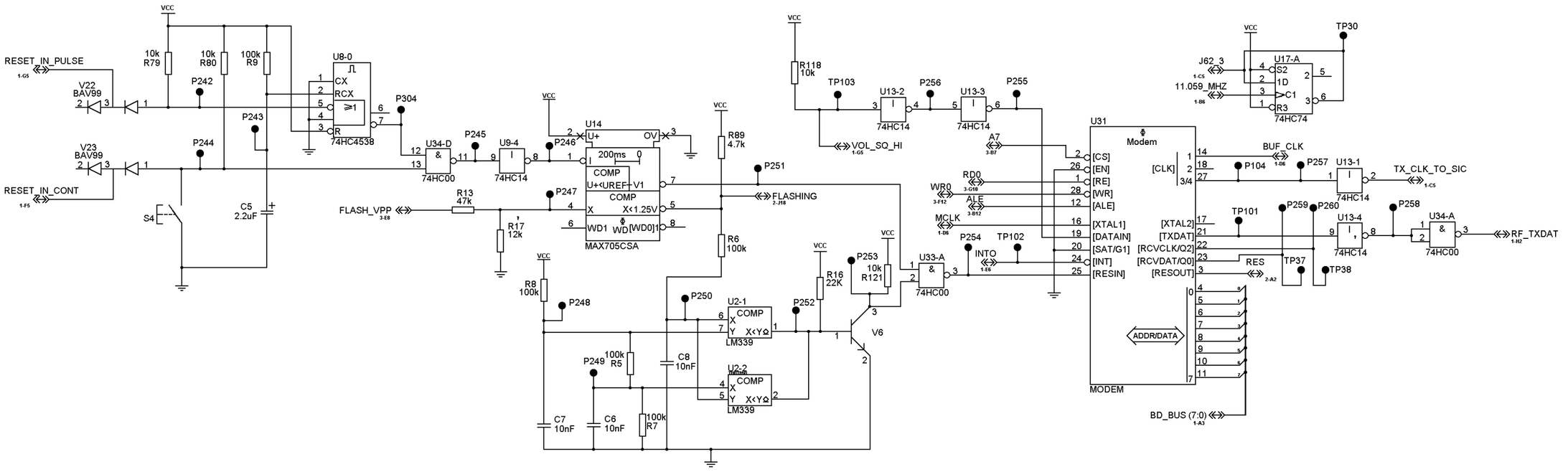
GENERAL PURPOSE TRUNKING CARD
ROA 117 2240

(1911-ROA 117 2240, SH. 2, Rev. A)



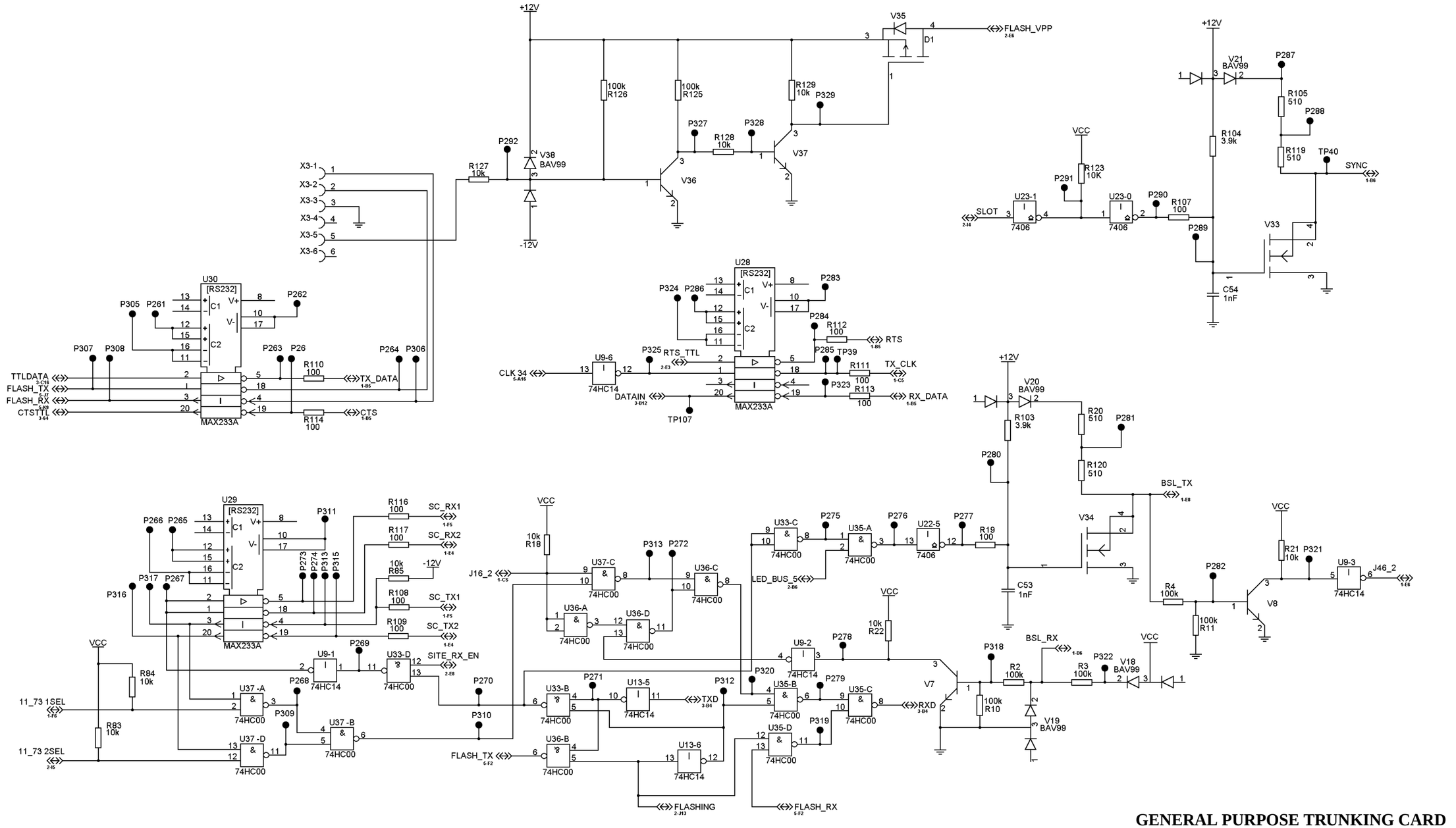
GENERAL PURPOSE TRUNKING CARD
ROA 117 2240

(1911-ROA 117 2240, SH. 3, Rev. A)



GENERAL PURPOSE TRUNKING CARD
ROA 117 2240

(1911-ROA 117 2240, SH. 4, Rev. A)



GENERAL PURPOSE TRUNKING CARD
ROA 117 2240

(1911-ROA 117 2240, SH. 5, Rev. A)

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