MAINTENANCE MANUAL
CONTROL BOARD
188D6149G1

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DESCRIPTION

Aegis™ M-PA™ radios consist of Controller Board 188D6149G1 installed in Front Cover Assembly 19D903620G1 or 19D438676G5. This assembly is joined to the appropriate Rear Cover Assembly to form a complete radio unit.

This manual describes Controller Board 188D6149G1 and how it is interconnected to the Front and Rear Cover Assemblies. Component level troubleshooting information for the controller board is also included.

The Controller Board is the largest and most complex board in the Front Cover Assembly. It contains all microcomputer circuitry that controls the radio. All of the audio circuitry in the radio, except for the microphone, speaker, and volume control, is also located in this board.

Aegis M-PA radios utilize an LCD Board located behind the display bezel. The Controller Board serially communicates with this board to transfer display update information to it. The Keypad Flex is also located in the Front Cover Assembly. This flex circuitry interfaces all operating controls to the Controller Board and the LCD Board. Other assemblies and components in the front cover assembly include the Emergency Button Board, the UDC and Speaker Flex circuits, the speaker, microphone, and Battery Plate.

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CIRCUIT ANALYSIS

CONTROLLER BOARD

The Controller Board is a multi-layered circuit board primarily manufactured using surface mounted components. This board is electrically connected to the Keypad Flex, LCD Board and UDC Flex circuit by two (2) flex connectors at the top of the board, J1 and J4. Single in-line connectors J101/P1 and J102/P2 connect the Controller Board to the RF Board in the Rear Cover Assembly. A 3-pin speaker audio connector, J3, and the battery power connection, H1 and H2, are located at the bottom of the board. The Controller Board is well shielded from the RF portions of the radio and the outside environment by the die-cast aluminum casting and the metallic shield.

On the Controller Board, Microprocessor U701 and Audio Processor U804 communicate by serial data lines. The Microprocessor controls all radio functions and the audio chip is primarily responsible for transmit and receive audio routing and filtering. Factory programmed PROM U703 stores the operating program for U701. RAM U707 provides operating memory. Personality information programmed into the radio from the IBM PC or compatible computer is stored in EEPROM U802. Aegis and VG operations are performed by Digital Signal Processor U705. Support circuitry includes modem U702, voltage regulators, microprocessor reset, and microphone and speaker audio amplifiers.

The schematic diagram for the Controller Board is divided into 4 sheets. The first sheet contains all input/output connections for the board. The LOGIC I/O BUS distributes the signal lines to the logic circuitry on sheet 2. The ASP I/O BUS connects to the audio circuitry on sheet 3.

The second sheet of the schematic contains all of the logic circuitry. Signal lines that leave the board are on the LOGIC I/O BUS to sheet 1. Signal lines to the Audio Signal Processor (ASP) are on the ASP I/O BUS to sheet 3. The last sheet of the schematic contains the Mixed Signal Processor (MSP) U705.

MICROPROCESSOR U701

A single microprocessor U701 controls the operation of the M-PA radio. It is an 80C515 8-bit processor with six I/O ports and one analog or digital input port. All microprocessor lines that connect to the analog portion of the board or connect externally to the board are first RF bypassed by RC circuits. Most of these circuits are shown on other sheets of the schematic but are physically located as close as possible to the digital section of the board.

The microprocessor contains internal “masked” software code to handle the programming of the Flash Memory U703. For normal radio operation, this software code is not needed. The microprocessor normally executes the radio software code in the Flash memory. The external address pin 49 is normally low to address the Flash Memory. The internal memory is only used during Flash programming. See the Flash Memory description below.

To check the operation of the microprocessor, check that the buffered 11.0592 MHz clock from Modem U702 is present on pin 36. The ALE output line (pin 48) should then run at 1.8432 MHz (0.54 ms period on a scope). The PSEN output (pin 47) also runs at the same frequency. This frequency may not be continuous because the microprocessor may have periods of “sleeping”. The PSEN rests at 5 Vdc when the radio is in Flash Programming mode.

FLASH MEMORY U703

The radio operating system software for the microprocessor resides in U703, a 128 Kbytes Flash Memory device. The Flash Memory allows easy reprogramming of the radio software for additional features and software upgrades without opening the radio or removing standard Proms.

The Flash Memory may be reprogrammed through the same PC computer interface that programs the Personality EEPROM. See the section on the personality EEPROM for a description of the PC data interface. When the Flash Memory is programmed, 12.0 +/- 0.5 Vdc is applied to the 12V input at connector J1.10. This voltage is divided down to 5 Vdc by R726 and R727 to feed the external address pin 49 of the microprocessor. With this pin HIGH, the internal “boot code” software masked inside the microprocessor is executed. This “boot code” software handles running the microprocessor to serially communicate with the PC computer to program the Flash Memory.

The radio checks for 12 Vdc within 20 ms after power-up. The Microprocessor initiates U701 pins 73 and 29 HIGH turning ON both Q601 and Q603, which turns ON Q607. With Q607 ON, voltage at J1 pin 10 is passed to the Flash Memory U703 pin 9 and 5 Vdc is input on U701 pin 49. If the 12 Vdc is present on J1 pin 10, the Microprocessor keeps pins 29 and 73 high allowing the radio to Flash Program. If 12 Vdc is not present, the Microprocessor will execute the Flash radio code which never places pins 29 and 73 HIGH simultaneously. This prevents any voltage spikes at the UDC connector from placing the Flash Memory in the program state during radio operation.

PERSONALITY EEPROM U802

An 8k x 8-bit EEPROM U802 stores all customer frequencies, tones and other option information. Tracking data aligned with the RF Board is stored for the transmit high power level, transmit low power level, mic deviation, data deviation, and squelch.

The personality information in the EEPROM matches the unique number in the Serial Number ROM U706. Programming of the EEPROM is accomplished by communicating externally with the microprocessor through the UDC connector.

To PC program the EEPROM, the radio must be placed into PC programming mode before communicating serially on the TX_DATA_OUT (J1 pin 7) and RX_DATA_IN (J1 pin 5) lines. This is done by connecting the PC programming cable on the UDC connector. When the radio is powered up, the Microprocessor will detect the programming cable on the UDC_SENSE line J1.4 and displays that it is in 9600 baud mode on the display.

SERIAL NUMBER ROM U706

The Serial Number ROM (Read Only Memory) U706 contains a unique 48 bit number that is read by the microprocessor at power-up. A single pin on the device provides serial communication with the microprocessor as well as +5 Vdc power through R728.

For proper radio operation, the unique serial number must match the personality information in EEPROM U802. Replacing either device may disable operation on all programmed trunking systems. The radio must be reprogrammed based upon the serial number.

NOTE

If replacement of U706 Serial Number ROM or U802 personality EEPROM is necessary, contact the Technical Assistance Center to obtain programming information.

RAM U707

U707 is a high speed RAM (Random Access Memory) providing 8 Kbytes of temporary data storage for the microprocessor. The RAM receives the lower 8 bits of address (A0 - A7) from the demultiplexer latch inside the modem.

MODEM U702

Modem U702 performs several functions. The modem’s chief function is to perform the serial to parallel and parallel to serial data conversion for receiving and transmitting data respectively. Limited high speed data from ASP U804 (sheet 3) feeds U702 pin 23. Data for transmission on U702 pin 26 is sent to the transmit audio circuits of the ASP on U804 pin 80.

The Modem contains a latch that is used with the microprocessor ALE (address latch enable) line to demultiplex the address/data bus from the microprocessor. Address information (A0 - A7) is separated from the address/data bus and then sent to the Flash Memory, RAM, EEPROM and the MSP. Another function of the Modem is to provide an address decoder for selecting the Modem, Ram, EEPROM, or the MSP. The Microprocessor PSEN line (U701 pin 47) enables the decoder (active high) on U702 pin 24.

The modem also provides the reset signal on U702-43 for the microprocessor and the ASP. The active HIGH reset is inverted by Q703 to be sent to the active LOW reset inputs of the microprocessor (U701 pin 1) and the ASP (U804 pin 9). A second “watch dog timer” inside the modem must be continually reset by the operating software or a 50 ms reset pulse will be sent to the microprocessor if a software failure occurs. Also, the modem receives the reset signal from the 5 volt regulator on U702 pin 33 which is passed to the microprocessor reset.

The 11.0592 MHz clock oscillator is also provided by the modem using Y701. The buffered clock signal (U702 pin 15) is sent to the microprocessor and the ASP. Q702 can provide a clock frequency shift if needed. Normally Q702 is turned off with C735 out of the oscillator circuit (except for the off capacitance of Q702). If a harmonic of the logic circuitry falls on a receiver channel, the clock can be shifted to move the interference.

DTMF ENCODER U803

DTMF (Dual Tone Multi-Frequency) tones are generated by U803. Reference clock oscillator Y801 (3.579545 MHz) only runs while a tone is being generated with the transmitter keyed. The encoder’s oscillator is disabled by software to prevent harmonic and other spurious energy from interfering with the radio receiver. When a software command is sent in transmit to generate a tone, the clock oscillator recovers in 3 ms and enables the DTMF generator.

The Microprocessor serially communicates with the DTMF encoder on the IIC CLK and IIC DATA lines. The generator tones from pin 5 are sent to the RX audio path (for speaker side tone) on ASP U804 pin 29 (sheet 3). They are also sent to the TX audio path to op-amp U304.1 for amplification before entering the TX path on U804 pin 59.

VOLTAGE REGULATORS

There are four (4) regulators on the Controller Board. The 5 volt regulator U801 supplies all the digital circuitry of the board. The regulator receives input voltage from the battery (nominally 7.5 Vdc) on connector H1. A 4 amp fuse in the front cap battery connector plate provides protection from excessive current drain.

The regulator also provides a reset signal if the input voltage falls below 5.2 Vdc. At this point, the regulator will begin to fall out of regulation and pin 5 will switch LOW (to ground). This LOW will discharge capacitor C802 and turn ON Q804. Q804 provides the active HIGH reset signal to modem U702.

When the input voltage to the regulator exceeds 5.2 Vdc (as when the radio is first turned ON), pin 5 switches to a high impedance state. C802 provides a reset pulse delay by charging through R806 and R807. When C802 charges to greater than 4.3 Vdc, Q804 turns OFF to release the reset signal to the Modem U702.

Voltage regulator U704 supplies 5 Vdc to all the analog circuitry on the board. Voltage regulator U805 supplies 5.5 Vdc to front cap keypad and display on connector J4.1 and also supplies the receive circuitry of the RF Board on connector J102/P2.6.

Voltage regulator U806 is used as a switch to supply 5.5 Vdc to the transmit circuitry of the RF Board when the radio is transmitting. When DPTT is pulled LOW, Q802 turns ON providing the active LOW to the input control pin 1 of U806 to turn it ON.

LOW BATTERY SENSE

When the battery voltage drops below approximately 6.3 Vdc, the BAT pixel on the LCD turns on. R801 and R802 divide the battery voltage in half. This low battery sense voltage is sent to the microprocessor U701 pin 8. This pin is an analog input port to the microprocessor that is used to measure the voltage level. D701 protects the microprocessor from over voltage conditions on the battery line.

AUDIO SIGNAL PROCESSOR

The Audio Signal Processor (ASP) U804 handles nearly all audio functions in the M-PA radio. Three (3) I/O lines from the Microprocessor provide serial interfacing with the ASP. The serial bus consists of the clock (ASP_STB U701 pin 79), a data output line (ASP_DATA U701 pin 78), and a chip select output (ASP_EN U701 pin 80). The clock and data lines are shared with the Keypad Flex output shift register IC and the LCD Board controller IC.

Receive Audio Circuits

Trunking Mode RX Audio

Detector audio enters on J101/P1 pin 4. It passes through series switch Q608 and enters ASP pin 44, the (-) input of an op-amp buffer. The gain of this amplifier is selected by ASP pin 16 (SW2). This controls bi-lateral switch U304.4, which changes the feedback resistance by placing R616 and R617 in parallel, changing the gain.

In the ASP, the buffered audio is bandpass filtered (300 to 3000 Hz). The filtered audio is selected by ISA/ISB audio multiplex switch in the ASP and then passes through audio switch VG to the de-emphasis stages. The de-emphasized audio passes through the digital volume control, through audio switch RXO, and then leaves on ASP pin 27. The receive audio path for the trunking mode never loops out and back into the ASP.

Receive audio from ASP pin 27 is attenuated and then enters Audio PA U603-7. U603 amplifies the audio and supplies the internal speaker on differential output pins 1 and 3. For external speakers, the receive audio from ASP pin 27 is sent to AUDIO OUT J1.3 through the Flex circuit to UDC connector J101-3.

High Speed Data Limiter

Buffered, unfiltered detector data in the ASP passes through audio gate TDS to ASP pin 45. The average dc level of the data signal is sent to the limiter (-) input on ASP pin 31 as a reference for the comparator. The output of the limiter ASP pin 21 is inverted by Q602. The data is sent to the modem U702-23 for data decoding and also sent to microprocessor U701-31. This port is normally HIGH. The port is switched LOW during transmit to clamp limited noise to the Modem.

Q705.2 allows the wide band limiter and the low frequency limiter to settle quickly when a RF signal appears that differs from the receiver frequency. Without Q705.2, the long transient that occurs with C609 charging to a new dc level will saturate the limiters momentarily. To reduce this problem, when the channel frequency is changed or when the squelch CAS line goes active, a 5 ms pulse can be sent to Q705.2 before attempting to read any data from the limiters. The 5 ms transient to charge C609 will be absorbed by the dc averaging circuit on the limiters. To prevent this problem during transmit, switch Q608 is opened. This isolates C609 from the discriminator preventing any charge build-up while transmitting.

Noise Squelch

The squelch circuit monitors the level of high frequency noise on the receiver detector audio to determine if a carrier is quieting the receiver. A Digital to Analog converter in the ASP sets the threshold level required to operate the squelch circuit (normally 8 dB SINAD). When the noise falls below the threshold level, the carrier activity sensor (CAS) output switches to 0 Vdc. The CAS signal feeds the microprocessor U701 analog port on pin 43.

Buffered, unfiltered detector audio leaves at ASP pin 43 and feeds ASP pin 50 which is the high pass filter input (7.5 kHz). In the ASP, the high pass filtered audio is rectified and sent out on ASP pin 52. The rectified noise is filtered to provide an average dc level proportional to the noise level. This dc noise level is sent to microprocessor port 6.7 and is applied to a non-inverting dc buffer amp on ASP pin 55. The output of the amp is on ASP pin 53. The gain of the dc amp is set by R620, R622, R623, and thermistor RT601. The thermistor increases in resistance at cold temperatures, causing the dc amp gain to increase. This compensates for the RF Board detector output level dropping at colder temperatures.

The buffered dc noise level output is sent to the (-) comparator input on ASP pin 49. The comparator (+) input receives a reference voltage from the digital to analog converter. When the dc noise level falls below the comparator reference, the comparator output switches high. The comparator output is buffered and inverted and appears at ASP pin 23. This CAS output is normally high (+5 Vdc) and switches low (0 Vdc) when a signal is detected.

To tighten the squelch, the D/A reference voltage is lowered. Hysteresis for the squelch is done in software. When the squelch output switches to indicate a signal is detected, the D/A reference value is increased slightly to loosen the squelch. The hysteresis eliminates "bubbling" or chattering noise in the speaker. The "bubbling" would normally be caused by transitional changes in the dc noise level around the reference point.

Bilateral switch U303.1 is normally turned OFF with DATA_TC (microprocessor P1.5) at 0 Vdc, leaving R624 and C604 in the dc noise averaging circuit. R624 provides a conventional slow (60 ms) squelch operation to prevent chopping the audio with rapid squelch closings in weak signal areas. When U303.1 is turned ON, a 5 ms fast squelch is provided by the parallel combination of R621 and R624.

Alert Tones

Programmable alert tones are generated in the ASP. The ASP uses a 66.6 kHz clock divided by 2 and then divided by a 6 bit divider. Therefore, the lowest alert tone frequency that can be generated is 33.3k / 63 = 528 Hz.

The output of the alert tone divider is on ASP pin 76. The tone output connects to ASP pin 30 to feed the ISA/ISB audio multiplex switch in the receive audio path. The tones then pass through audio switch VG to the de-emphasis stages. The de-emphasized audio passes through the digital volume control, through audio switch RXO, and then leaves on ASP pin 27 which feeds the audio PA.

Table 1 - Audio Signal Processor Switched Outputs

SWITCH	U804 PIN	NAME	USE	OUTPUT HI	OUTPUT LOW
SW0	18	PA_MUTE	Audio Amplifier U603 Switched Power	ON	OFF
SW1	17	DAT_LIM	Data Limiter Read Pulse for discriminator input	OFF	ON
SW2	16	NARROW_BAND	Narrowband switch to select discriminator audio gain	Low gain	High gain
SW3	15	CLK_SHIFT	Shift of the 11.0592 MHz crystal	ON	OFF
SW4	14	MSP_PWD	Power down switch for Mixed Signal Processor U705	MSP ON	MSP OFF
SW5	13	MSP_RESET	Reset switch for the Mixed Signal Processor U705	OFF	RESET

Transmit Audio Paths

Transmit Mic Audio (Non-Aegis Modes - For test Only)

The microphone receives 2.5 Vdc bias through R315. Mic audio is coupled into ASP pin 74. Mic audio passes through audio switch MIS to the mic amplifier. Switch MGS determines the gain of the amplifier. MGS is normally open (MGS = 1) for high gain. A LOW MIC GAIN option in PC programming can lower the gain 10 dB for noisy environments when MGS is closed. The audio from the mic amp is then pre-emphasized and 300 Hz high pass filtered in the ASP. The audio then leaves the ASP on pin 70.

Pre-emphasized mic audio is coupled back into the ASP on pin 57. The audio is passed through muting switch AEN and then feeds the limiter. The limiter threshold can be stepped up by register LMT so that the peak deviation of the mic audio can be increased when no Channel Guard is present.

Limited mic audio then passes through a summing amp in the ASP which sums tones and data. The output of the summing amp feeds switch PBY to allow a choice of passing the audio through the 3 kHz post limiter filter (for limited mic audio) or passing unfiltered audio (for data) directly to the transmit deviation control (TA5 - TA0). The output of the digital deviation control passes through audio switch TXO to ASP pin 60.

The TX audio output from the ASP feeds U301.2. The output of U301.2 is dc coupled to the RF Board to feed the synthesizer.

Transmit RF Output Power:

The D/A converter used to set the squelch threshold in receive, is used to set the power level in transmit. The D/A output is on ASP pin 48. The output voltage level can vary from 0 to 5 Vdc in 256 steps to control the transmit power.

Transmit 9600 Baud Data

Modem data is applied to ASP pin 80. CEN registers select the TX DATA input. The data is passed through a bessel filter in the ASP. The output of the filter is sent to the TX path summing amp. The output of the summing amp feeds audio switch PBY to allow bypassing the 3 kHz post limiter filter for data transmission. The data passes through the digital deviation control and then through audio switch TXO to feed U301.2 and the synthesizer.

During transmit, the modem input from the receive data limiter requires muting to prevent the modem from being disturbed by receive noise. Microprocessor U701 Port 1.0 switches low during transmit to clamp the line to ground.

Transmit DTMF (All Modes)

U803 generates DTMF tones which are amplified by op-amp U304.1 before entering the ASP on pin 59. The tone is passed through muting switch DEN to a summing AMP. It then follows the same path as the mic audio in the ASP (see section on MIC AUDIO).

For receive audio side-tone, the DTMF audio is also fed into ASP pin 29. The side-tone audio is selected by the ISA/ISB receive audio multiplex switch and then passes through audio switch VG to the de-emphasis stages. The de-emphasized audio passes through the digital volume control, through audio switch RXO, and then leaves on ASP pin 27 which feeds the audio PA.

The DTMF encoder uses Y801 3.579545 MHz clock crystal. In receive, the encoder's oscillator is disabled by software to prevent harmonic and other spurious energy from interfering with the radio receiver. When the software command is sent in transmit, the clock oscillator recovers after 3 ms and enables the DTMF generator.

Synthesizer Loading and Lock Monitoring

The loading of frequency data into the synthesizer IC on the RF Board occurs when a new receive frequency is selected, when the radio changes from receive to transmit, or when the radio changes from transmit to receive. This is accomplished by clocked serial lines from the microprocessor. The clock (SYN_CLK U701 pin 28), data (SYN_DATA U701 pin 29), and enable (SYN_EN U701 pin 30) outputs load the synthesizer chip with new frequency data. Data on SYN_DATA is serially clocked into the synthesizer IC by SYN_CLK and latched by SYN_EN.

When the microprocessor wishes to check the lock status of the synthesizer, it monitors the synthesizer's LOCK DETECT output on J102/P2 pin 8. LOCK DETECT goes LOW or pulses when the synthesizer is not locked.

The microprocessor also supplies a band-switch logic line to RF Boards which require this. The BAND_SW output from U701-25 is applied to J102/P2 pin 3. See the appropriate Rear Cover Assembly maintenance manual for details on the logic level verses VCO operating frequency.

AEGIS OPERATION

AEGIS capability is performed by Digital Signal Processor U705. It converts analog speech to and from a compressed digital form.

U705 communicates with the microprocessor and modem through its 8-bit port HDO-HD7, which is on the data bus. The port requires 3 address inputs to select the registers in the port, HAO, HA1 and HA2. The PWD and RESET inputs of U705 are controlled by the audio signal processor switches. PWD is used to power U705 down during standby mode. RESET is used to reset U705 at power up and when changing its parameters such as internal/external mic input. The FLO output provides an active-low interrupt, to the microprocessor U701 when speech data is available in transmit mode or requested in receive mode. Y901, C821 and C822 provide a 9.8304 MHz clock for U705.

U701 must have software loaded into it at power-up. This is performed by the microprocessor U701 each time the radio is powered up and when changing any setup parameters. This software is stored in the Flash EEPROM U703 along with the radio operating software.

Transmit Mode

In the transmit mode, internal microphone audio is amplified and filtered by op-amp U302.2 before entering VINNORM on pin 54 of U705. If an external microphone was attached to the radio at power-up, the audio is amplified and filtered by op-amp U302.1 before entering VINAUX on pin 52 of U705. The DSP converts the input to digital audio, compresses (vocoding) the data and performs optional encryption. The resulting data is passed to the microprocessor and modem where it is formatted and transmitted as 9600 baud data. See **Transmit 9600 Baud Data.**

Receive Mode

In receive mode, data is detected by the high speed data limiter and passes to the modem U702 pin 23. See the **High Speed Data Limiter** section. This data is sent to U705 over the bus where it is optionally decrypted, decompressed, and converted from digital to analog audio. The differential output is present at VOUTP and VOUTN (pins 57 and 58 of U705). Op-amp U301.1 provides differential to single ended conversion of the audio signal. This signal enters pin 28 of the ASP (U804) where it passes through volume control and out pin 27. Note that the de-emphasis stage in the ASP is bypassed when VG is HIGH (U804-78). See **Trunking Mode RX Audio** for remaining audio path.

TROUBLESHOOTING

The following outline will help lead the service technician to a problem with the Controller Board or another associated circuit in the Front Cover Assembly. The Controller Board should be removed and electrically extended for troubleshooting access. Use the adapter board and the extender cable in SPK9011 Front Cover Test Accessory Kit.

CAUTION

ALWAYS remove the battery pack before disassembling the unit to avoid blowing the fuse or causing other component damage.
This radio contains CMOS ICs that can be damaged by static electricity. Observe static handling precautions.

SYMPTOM AND CAUSE OUTLINE

Completely Inoperative Radio

Check Power Supplies

Power supplies should be the first area to check in the event of a completely inoperative unit. The battery fuse is located in the Battery Plate on the bottom of the radio. If the radio is dead, check the fuse.

Power into the radio (7.5 Vdc battery voltage) can be tested by monitoring the input connections H1 and H2 (screw mounting points) located at the bottom of the Controller Board. If dc is not present at this point, suspect the fuse F1 or the battery connection.

Regulated supplies on the Controller Board are the digital 5.0 Vdc (+5V), the analog 5.0 Vdc (+5VA), a 5.5 Vdc (+5.5V) supply for Keypad Flex, LCD Board, and RF Board.

The 5.0 Vdc (+5V) can be checked at Test Point 11 (TP11) and the analog 5.0 Vdc (+5VA) can be checked at TP4. These supplies should be within +/- 0.25 Vdc. Supply failure may indicate a shorted decoupling capacitor on the associated supply rail. The +5.5V can be checked at J4.1 and J102/P2.6. Failure of this supply may indicate a short on the Keypad or LCD Board. Temporarily disconnect the J4/P4 flex connection to verify there is no short on the Keypad Flex or LCD Board.

Check Reset Logic

When the radio is powered up, monitor the reset pulse at U701 pin 1 from the modems reset output U702 pin 43. Trigger the scope on the rising 7.5 Vdc power supply. This pulse should stay LOW 10-30 milliseconds, then transition and stay HIGH. If the reset pin remains LOW, the radio will be inoperative since the microprocessors not released from reset.

If a problem exists with the pulse on U701 pin 1, check reset_in at U702 pin 33. This point should stay HIGH for 10 - 30 ms after turn on. If this signal is good, suspect a problem in the modem IC or a shorted input on U701 pin 1 or U804 pin 9. If the pulse at U702 pin 33 is not good, troubleshoot the reset circuit and the associated RC networks (Q804 and U801).

Slowly lower the battery supply voltage until U702 pin 33 transitions high. This should occur at an approximate battery voltage of 5.7 Vdc. Next, slowly raise the supply voltage and verify the line returns LOW. There should be approximately 0.2 Vdc hysteresis.

Check Clocks

Monitor the buffered 11.0592 MHz clock from the Modem U702 pin 15 at R820 or R752. NOTE: Use an oscilloscope or a frequency counter that has a high input impedance. Suspect Y701 if this clock frequency is in error. Suspect Y701 or U702 if no signal is present.

On digital radios, the Mixed Signal Processor U705 runs off a 9.8304 MHz clock. This clock will run only when the radio is encoding or decoding digital audio. To check this clock, the radio must be either transmit a digital call, or receiving a digital call from another radio. This can be measured at C821. NOTE: This point is unbuffered, so probing this point will slightly shift the frequency.

Check Keypad Scanning

Approximately every 5 milliseconds, pulse activity should be present on the serial lines to and from the Keypad Flex. See Figure 1. These pulses are loading a data byte into shift register U2 and reading U1 on the Keypad Flex. The ASP is also being read and written to with the same clock line. Therefore, other data bursts will appear that are different from Figure 1, but these do not affect keypad scanning or LCD updates. If these signals are not present, microprocessor U701 is suspect.

Synthesizer Not Locking Properly

Each time the channel is changed, the PTT button is pressed, or the PTT button is released, the microprocessor serially loads the synthesizer IC on the RF Board with new TX or RX data. If the synthesizer does not lock or stay locked, the following should be observed:

- the radio continuously or intermittently beeps
- “NO LOCK” flashes in the display
- LOCK DETECT (J102/P2 pin 8) is low or pulsing

If the above condition occurs, the microprocessor should continue to try to reload the synthesizer IC with data until the synthesizer locks.

Synthesizer lock failure can be caused by a problem on the RF Board or Controller Board. If the radio locks only on some frequencies, (for example high-side channels) the problem is most likely on the RF Board (VCO or prescaler circuits for example). The checks below deal with the problems associated with the Controller Board.

1. Read the radio personality with the PC programmer and reprogram to verify that there is good channel data for each channel programmed into the radio. If channels are in error, suspect EEPROM U17 or previous programming.

2. On connectors J101/P1 and J102/P2, verify the 5.5 Vdc supply (RF5.5V) to the RF Board is within +/- 0.2 Vdc, 7.5 Vdc BATT is present, and TX 5.5V is LOW (RX Mode).

3. Monitor the synthesizer load pulses (J102/P2 pins 9, 10 and 11) for pulse activity when a channel is changed. See figure 3. If these signals are not present, suspect a defective microprocessor or an open series resistor. NOTE: Temporarily connect LOCK DETECT (J102/P2 pin 8) to ground to view these waveforms.

4. Verify the bandswitch line, SYN BSW (J102/P2 pin 3), is the correct logic level. See the Rear Cover Assembly maintenance manual for details on the logic level verses VCO output frequency. Suspect the microprocessor if there is a problem. Note that some RF Boards do not use the SYN BSW line.

5. Suspect the RF Board if all the outputs to it are good.

Radio Will Not Program

Check the PC programmer Power

The controller board must first recognize the programming resistor (short to ground at UDC pin 9) with the PC Interface connected. It should then supply 7.5 Vdc (battery power, current limited by Q705.1) to the PC interface via UDC pin 4 (SW BATT).

Figure 1 - Typical Keypad Scanning Waveforms

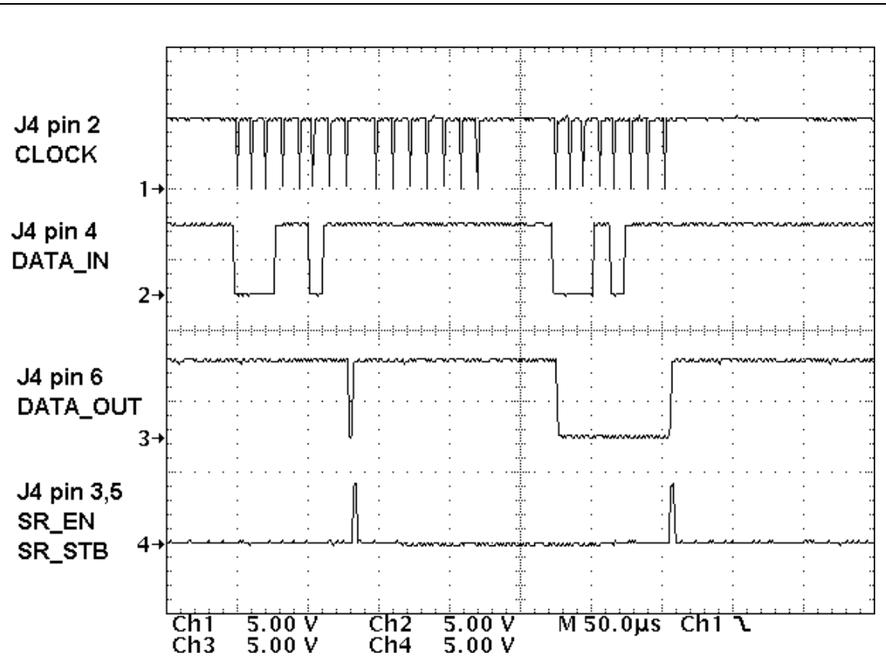
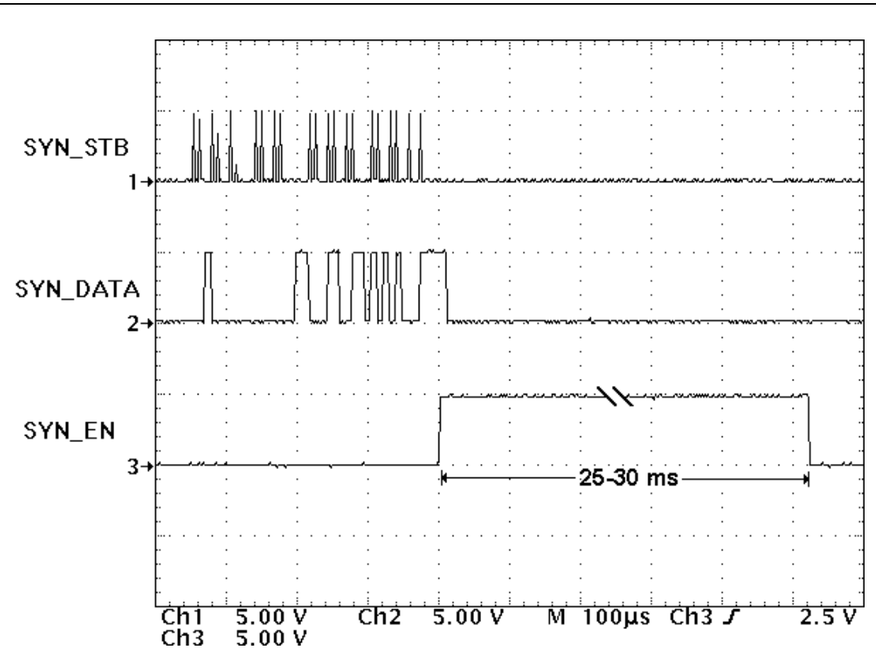


Figure 2 - Synthesizer Load Sequence



1. Attempt to reprogram the unit with the external PC Interface power adapter; if successful, suspect transistors Q706, Q704.

2. Less than 0.6 Vdc should be on U701 pin 12 with the PC interface connected to enable programming mode. If incorrect, suspect R715, R704 or the UDC Flex.

3. Check TX and RX DATA to and from the radio and PC programmer.

Check RX DATA IN

To check the RX DATA input, connect the PC Interface and computer and proceed as follows:

1. Check for logic 0 at J101/P1 pin 5 (RX_DATA_IN). Pulses should be seen here when a radio read is attempted. Suspect the UDC Flex if pulses are not present and the pin is high all the time.

2. Check for logic 1 at U701 pin 15 or Q801 pin 3. Pulses should be seen when the radio read is attempted. Suspect Q801, R718, R709, R705 or D704 if they are not. If pulses are present suspect U701.

Check TX DATA OUT

Attempt to read the radio repeatedly and check for a short serial data burst at the following points:

- U701 pin 16 (signal origin)
- J101/P1 pin 7 (TX_DATA_OUT)

Check the UDC Flex continuity from J101/P1 pin 7 to UDC J101 pin 7. The short burst should be present at the UDC pin. Note that these pulses may be difficult to see on an average oscilloscope because they are at a very low level.

Transmit Audio Problems

No Internal Mic Audio (External Good)

1. Check MIC HI (J101/P1 pin 14) for an internal mic dc bias of approximately 2.5 Vdc. If this bias is incorrect, suspect R315.

2. Average speech into the front cover should produce 10 - 30 mV rms on MIC HI J1 pin 14. If this is not seen, suspect the UDC Flex.

3. Check for audio at U705 pin 54. A 12 Vrms mic input should be amplified to about 100 mVrms at this point. If not, suspect U302.2 and the associated components.

No External Mic Audio (Internal Good)

1. Verify the microprocessor is recognizing the externally connected option. Note that the radio must be turned on after the accessory is attached. The voltage on U701 pin 12 should be approximately 2.5 Vdc with the external mic connected. This voltage is developed from voltage divider R715, R704 and the resistor in the external option.

2. Check for 2.5 Vdc bias at UDC pin 12 and J101/P1 pin 12. If this bias is incorrect, suspect R305.

3. Average speech into the front cover should produce 10-30 mVrms on EXT MIC HI J1-12. If this is not seen suspect the UDC flex.

4. Check for audio at U705-52. A 12 Vrms mic input should be amplified to about 100 mVrms at this point. If not, suspect U302.1 and the associated components.

Complete Mic Audio Failures

1. Verify the radio unit under test and the receive unit have identical outside addresses programmed and the correct data polarity. If the problem is only in private mode, verify the correct cryptographic keys are loaded and the group/channel-to-key selection is correct.

2. Check J102/P2 pin 1 for a modulating signal to the RF Board. If good modulation is present, troubleshoot the RF Board's modulation circuitry.

3. Check for data at U804-80 during transmit. If no data is present, suspect modem U702 or the DSP U705.

4. Check for audio at U804 pin 60. If no audio is present, suspect the ASP.

5. Check op-amp U301.2 pin 7. If audio is present, suspect R314. If not, suspect R306, R309 or C310.

Modem Transmit Data Check

1. Monitor Modem U702 pin 26 (TX DATA) for 9600 baud pulses when a trunked call, Aegis digital or private call is attempted. Signal level should be > 3 Vp-p with rise and fall times < 100 ms. If no pulses are present, there is a communication problem between U701 and U702, or U702 is defective.

2. An internal switched capacitor filter of the ASP filters "rounds" the TX DATA digital pulses to a signal that passes to the FM transmitter. Check U804 pin 60 for a 9600 baud "rounded" signal at 500 mVp-p. If no signal is present, suspect U804.

3. Check J102/P2.1 (TX_MOD) for the 9600 baud signal to the RF Board. The signal should be approximately 800 mVp-p. If no signal is present, suspect U301.2 and the surrounding circuit.

Receive Audio Problems

No Clear Receive Audio (Test Only)

1. Verify audio from the RF Board is present at J101/P1 pin 4. Signal level range from 50 to 150 V rms (» 300 mVp-p) for 1 kHz tone at rated system deviation depending on the radio type. Noise only levels will be near 0.5 Vp-p. Refer to the RF Board maintenance manual for a more accurate level.

2. There should be a dc voltage on U804 pin 49 or thermistor RT601 between 2.5 and 5.0 Vdc. This dc voltage will be proportional to receiver noise.

3. Check the squelch opening tracking data parameters using the PC programmer. Higher numbers should make the squelch open at lower signal levels, and lower numbers should make the squelch open at higher signal levels. Typical squelch opening tracking data is C0 hex. Values below 80 should always squelch the radio and values above E0 should always unsquelch the radio. If the radio does not operate as described, suspect R624, C624 or the ASP.

4. Verify the audio levels in Table 3 following the audio path.

Table 2 - Transmit Audio Signal Levels

TEST LOCATION	LEVEL (typical)	COMMENT
U804 pin 73	12 mVrms	External Mic Amp Input (clear mode path)
U705 pin 52	100 mVrms	External Mic Amp input to Digital Signal Processor
U804 pin 70	270 mVrms	Pre-Amp Output from ASP (Clear mode path)
U804 pin 57	110 mVrms	Limiter Input (Clear mode path)
U804 pin 60	360 mVrms	Transmit Deviation Attenuator Output
J102/P2 pin 1	500 mVrms	Transmit Modulation to the RF Board

Table 3 - Typical Receive Audio Levels at Full Volume

TEST LOCATION	LEVEL (typical)	COMMENT
J101/P1 pin 4	60 mVrms	RX Discriminator Output (RX_DISC)
U804 pin 43	900 mVrms	Buffer Amplifier Output
U804 pin 27	570 mVrms	Volume Attenuator Output
U603 pin 7	100 mVrms	Audio Amplifier Input
U603 pins 1, 3	5000 mVrms	Speaker Audio Amp Output (differential)

No Aegis Digital or Private Mode Receive Audio

1. Verify the radio unit under test and the receive unit have identical outside addresses programmed and the correct data polarity. If the problem is only in private mode, verify the correct cryptographic keys are loaded and the group/channel-to-key selection is correct.

2. Transmit a clear signal to the radio under test and verify the transmission is received, the receiver unsquelches and it is heard in the speaker. If not, troubleshoot the clear mode failure before attempting to troubleshoot an Aegis digital or a private mode failure - there may be a common cause.

3. If the radio does not recognize an Aegis digital or a private signal (observe the "BSY" and "PVT" status flags), suspect modem U702 or the associated circuitry (See **Modem Receive Data Check**). If the radio is equipped with an encrypt/decrypt option, the "PVT" status flag should flash when it receives a valid private signal. If the "PVT" status flag flashes but no audio is heard in the speaker, the cryptographic key, outside address, etc. may be incorrect or there may be an audio problem in the radio.

4. Verify the decoded audio is present on differential outputs of U705-57 & 58. If not, suspect a problem with U705.

5. Verify the decoded audio is present on U804-28. If not, suspect U301.1 and the associated circuitry.

6. With the exception of the de-emphasis characteristics of U804, the audio path from U804 pin 27 to the speaker is identical to the clear mode audio. The de-emphasis response is controlled by the VG line from U701 pin 77 to U804 pin 78. If the radio is unusually low-pitched sounding when in Aegis digital or private modes, Check U804 pin 78. It should be high when a radio is decoding an Aegis digital signal or decrypting a private transmission. This bypasses the pre- and de-emphasis stages.

Modem Receive Data Check

1. Monitor U702 pin 23 (DATAIN) for demodulated data when the radio is receiving 9600 baud data transmission. The signal level should be approximately 5.0 Vp-p. If no pulses are present, suspect Q602, R625, R626 or C603.

2. Modem U702 should interrupt microprocessor U701 when it receives valid data. Check U702 pin 32 for low pulses when the radio is receiving data transmissions. Suspect U702 if the data is present and no interrupt is observed.

If the Microprocessor is being interrupted by the Modem when a valid data transmission is received and the radio does not recognize the transmission, suspect U702 or the radio's personality programming.

Volume Control Problems

The volume control operates by digitizing the dc voltage from the volume potentiometer wiper and varying the digital attenuator in the ASP.

1. Check the dc voltage at J4/P4 pin 9. It should be near 0 Vdc with the volume control fully counterclockwise and near 5.5 Vdc with the control knob fully clockwise. If not, check the volume control knob and Keypad Flex.

2. The volume control wiper voltage minus 1/12 should always be present at U701 pin 7. If not, suspect R821 or R822.

3. If the wiper voltage is present at U701 pin 7, suspect microprocessor U701.

Speaker Amplifier Problems

1. Check the Battery Plate speaker contacts.

2. If the speaker is inoperative and audio is present on UDC pin 3 (or U804 pin 27), check U603 pin 2 for battery power. If it is not present, suspect Q605.

3. Audio should be present on U603's input pin 7. If not, suspect C615, R628 and R629.

4. Check U603's differential outputs on pins 1 and 3. Replace U603 if power and audio inputs are good and the differential outputs are not.

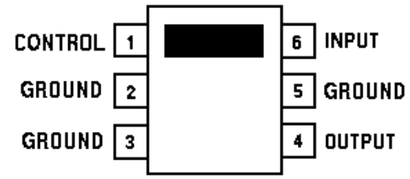
The internal speaker can be quickly tested by applying audio from a signal generator to the appropriate pins on the Battery Plate with the battery removed. With the Front Cover face-down on the bench, apply audio from the signal generator to the second and third pins from the left. The speaker impedance is 24 ohms and it is a 1/2 Watt device.

PARTS LISTS
CONTROL BOARD
PL188D6149G1

SYMBOL	PART NO.	DESCRIPTION
		- - - - - - CAPACITORS - - - - - -
C302 thru C305	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C306	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C307	19A705205P19	Tantalum: 2.2 uF, 10 VDCW; sim to Spargue 293D.
C309	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C310	19A705205P19	Tantalum: 2.2 uF, 10 VDCW; sim to Spargue 293D.
C316	19A702052P5	Ceramic: 1000 pF + or -10%, 50 VDCW.
C340	19A702052P45	Ceramic: 0.22 uF + or -10%, 16 DCWV.
C341	19A149897P47	Ceramic: 220 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C344	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C345	19A702052P34	Ceramic: 0.1 uF + or -10%, 25 VDCW.
C347	19A702052P52	Ceramic: 1.0 uF 16 VDCW + or - 10%.
C348 thru C351	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C352	19A705205P19	Tantalum: 2.2 uF, 10 VDCW; sim to Spargue 293D.
C353	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C360	19A702052P45	Ceramic: 0.22 uF + or -10%, 16 DCWV.
C361	19A149897P47	Ceramic: 220 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C364	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C365	19A702052P34	Ceramic: 0.1 uF + or -10%, 25 VDCW.
C367	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Spragues 293D.
C602	19A149896P121	Ceramic: .01 uF + or -10%, 50 VDCW.
C603	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C607	19A149896P121	Ceramic: .01 uF + or -10%, 50 VDCW.
C609	19A702052P52	Ceramic: 1.0 uF 16 VDCW + or - 10%.
C610	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C611	19A705205P19	Tantalum: 2.2 uF, 10 VDCW; sim to Spargue 293D.
C612	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C613 and C614	19A705205P19	Tantalum: 2.2 uF, 10 VDCW; sim to Spargue 293D.
C615	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C616	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C617	19A149896P121	Ceramic: .01 uF + or -10%, 50 VDCW.
C618	19A702052P52	Ceramic: 1.0 uF 16 VDCW + or - 10%.
C619	19A149896P121	Ceramic: .01 uF + or -10%, 50 VDCW.
C620	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C621 and C622	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C623	19A702052P52	Ceramic: 1.0 uF 16 VDCW + or - 10%.
C624	19A702052P45	Ceramic: 0.22 uF + or -10%, 16 DCWV.
C625	19A705205P19	Tantalum: 2.2 uF, 10 VDCW; sim to Spargue 293D.
C626	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C642	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C644	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C701 thru C718	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C725 and C726	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C727 thru C729	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C730	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 +or -30 PPM
C731	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C732 and C733	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C734	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C735	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0
C737	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C738	19A149897P15	Ceramic: 10 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C739	19A149897P27	Ceramic: 33 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C740 and C741	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C742	19A149897P15	Ceramic: 10 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C743 thru C750	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C751	19A149897P27	Ceramic: 33 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C752 and C753	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C756	19A149897P27	Ceramic: 33 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C757	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C758 thru C763	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C764	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C765 thru C767	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C801	19A702052P52	Ceramic: 1.0 uF 16 VDCW + or - 10%.
C802 and C803	19A702052P45	Ceramic: 0.22 uF + or -10%, 16 DCWV.
C804	19A705205P19	Tantalum: 2.2 uF, 10 VDCW; sim to Spargue 293D.
C805	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C806	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C807	19A705205P19	Tantalum: 2.2 uF, 10 VDCW; sim to Spargue 293D.
C808	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C809	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C810	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C812 thru C818	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C819	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C820	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C821 and C822	19A149897P27	Ceramic: 33 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C823 and C824	19A149897P39	Ceramic: 100 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
		- - - - - - - - - - DIODES - - - - - - - -
D701 thru D709	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99.
D710	19A705377P5	Silicon, Hot Carrier: sim to HSMS-2804.
D711	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99.
		- - - - - - - - - - JACKS - - - - - - - - - -
J1		Part of PWB.
J3	19A702517P5	Contact, Gold Plated, Horizontal Mount; sim to 75121-001.
J4		Part of PWB.
		- - - - - - - - - PLUGS - - - - - - - -
P1	19A704852P202	Connector PWB: 5 circuits, sim to Dupont Berg 65646-105.
P2	19A704852P203	Connector PWB: 11 circuits, sim to Dupont Berg 65646-111.
		- - - - - - - - - - TRANSISTORS - - - - - - - - -
Q601 thru Q604	RYN121649/1	Silicon, NPN: sim to RN1305.

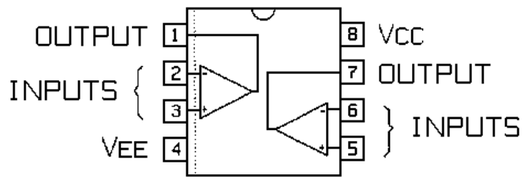
SYMBOL	PART NO.	DESCRIPTION
Q605	19A134577P2	Silicon, PNP: sim to Phillips BCX51-16.
Q606	RYN121649/1	Silicon, NPN: sim to RN1305.
Q607	19A700059P2	Silicon, PNP: sim to MMBT3906, low profile.
Q608	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q701	19A705945P2	Silicon, Dual NPN: sim to R OHM IMX3.
Q702	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q703	RYN121649/1	Silicon, NPN: sim to RN1305.
Q704	19A134577P2	Silicon, PNP: sim to Phillips BCX51-16.
Q705	19A705944P1	Silicon, Dual PNP; sim to ROHM IMT1.
Q706	RYN121649/1	Silicon, NPN: sim to RN1305.
Q801 thru Q803	RYN121649/1	Silicon, NPN: sim to RN1305.
Q804	19A700059P2	Silicon, PNP: sim to MMBT3906, low profile.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R301	19A149818P153	Metal film: 15K ohms + or - 5%, 1/16 w.
R305	19A149818P222	Metal film: 2.2K ohms + or -5%, 1/16 w.
R306	19A149818P683	Metal film: 68K ohms + or -5%, .063 watts.
R309	19A149818P104	Metal film: 100K ohms + or -5%, 1/16 w.
R313	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R314	19A149818P470	Metal film: 47 ohms + or -5%, 1/16 w.
R315	19A149818P222	Metal film: 2.2K ohms + or -5%, 1/16 w.
R316	19B801251P2R2	Metal film: 2.2 ohms + or -5%, 1/10 w.
R317	19A149818P104	Metal film: 100K ohms + or -5%, 1/16 w.
R318	19A149818P222	Metal film: 2.2K ohms + or -5%, 1/16 w.
R340	19A149818P682	Metal film: 6.8K ohms + or -5%, 1/16 w.
R341	19A149818P563	Metal film: 56K ohms + or -5%, 1/16 w.
R343	19A149818P102	Metal film: 1K ohms + or -5%, 1/16 w.
R351 and R352	19A149818P100	Metal film: 10 ohms + or -5%, 1/16 w.
R360	19A149818P682	Metal film: 6.8K ohms + or -5%, 1/16 w.
R361	19A149818P563	Metal film: 56K ohms + or -5%, 1/16 w.
R363	19A149818P102	Metal film: 1K ohms + or -5%, 1/16 w.
R365	19A149818P682	Metal film: 6.8K ohms + or -5%, 1/16 w.
R366	19A149818P472	Metal film: 4.7K ohms + or -5%, 1/16 w.
R370	19A149818P154	Metal film: 150K ohms + or -5%, 1/16 w.
R371	19A149818P334	Metal film: 330K ohms + or -5%, 1/16 w.
R603	19A149818P334	Metal film: 330K ohms + or -5%, 1/16 w.
R604	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R605	19A149818P223	Metal film: 22K ohms + or -5%, 1/16 w.
R607	19A149818P102	Metal film: 1K ohms + or -5%, 1/16 w.
R608	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R609	19A149818P223	Metal film: 22K ohms + or -5%, 1/16 w.
R610	19A149818P104	Metal film: 100K ohms + or -5%, 1/16 w.
R611	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R613	19A149818P473	Metal film: 47K ohms + or -5%, 1/16 w.
R614	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R617	19A149818P334	Metal film: 330K ohms + or -5%, 1/16 w.
R618 and R619	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R620	19A149818P184	Metal film: 180K ohms + or -5%, 1/16 w.
R621	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R622	19A149818P334	Metal film: 330K ohms + or -5%, 1/16 w.
R623 and R624	19A149818P154	Metal film: 150K ohms + or -5%, 1/16 w.
R625	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R626	19A149818P334	Metal film: 330K ohms + or -5%, 1/16 w.
R627	19A149818P222	Metal film: 2.2K ohms + or -5%, 1/16 w.
R628	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R629	19A149818P222	Metal film: 2.2K ohms + or -5%, 1/16 w.
R630 and R631	19A149818P4R7	Metal film: 4.7 ohms + or -5%, .063 watts.
R632	19A149818P473	Metal film: 47K ohms + or -5%, 1/16 w.
R633	19A149818P104	Metal film: 100K ohms + or -5%, 1/16 w.
R637	19A149818P105	Metal film: 1M ohms + or -5%, 1/16 w.
R640 and R641	19A149818P273	Metal film: 27K ohms + or -5%, 1/16 w.
R642 and R643	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R645	19A149818P473	Metal film: 47K ohms + or -5%, 1/16 w.
R646	19A149818P104	Metal film: 100K ohms + or -5%, 1/16 w.
R647 and R648	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R701	19A149818P102	Metal film: 1K ohms + or -5%, 1/16 w.
R702	19A149818P101	Metal film: 100 ohms + or -5%, 1/16 w.
R703	19A149818P470	Metal film: 47 ohms + or -5%, 1/16 w.
R704	19A149818P102	Metal film: 1K ohms + or -5%, 1/16 w.
R705	19A149818P101	Metal film: 100 ohms + or -5%, 1/16 w.
R706	19A149818P102	Metal film: 1K ohms + or -5%, 1/16 w.
R707	19A149818P391	Metal film: 390 ohms + or -5%, 1/16 w.
R708	19A149818P101	Metal film: 100 ohms + or -5%, 1/16 w.
R709 and R710	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R711	19A149818P102	Metal film: 1K ohms + or -5%, 1/16 w.
R712 thru R714	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R715	344A3304P1002	Metal film: 10K ohms + or -1%, 1/10 w.
R716	19A149818P332	Metal film: 3.3K ohms + or -5%, 1/16 w.
R718	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R725	19A149818P100	Metal film: 10 ohms + or -5%, 1/16 w.
R726	19A149818P153	Metal film: 15K ohms + or - 5%, 1/16 w.
R727	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R728	19A149818P472	Metal film: 4.7K ohms + or -5%, 1/16 w.
R732	19A149818P104	Metal film: 100K ohms + or -5%, 1/16 w.
R733 and R734	19A149818P333	Metal film: 33K ohms + or -5%, 1/16 w.
R736 thru R739	19A149818P100	Metal film: 10 ohms + or -5%, 1/16 w.
R740	19A149818P102	Metal film: 1K ohms + or -5%, 1/16 w.
R741	19A149818P333	Metal film: 33K ohms + or -5%, 1/16 w.
R742	19A149818P823	Metal film: 82K ohms + or -5%, 1/16 w.
R743	19A149818P101	Metal film: 100 ohms + or -5%, 1/16 w.
R745 thru R747	19A149818P102	Metal film: 1K ohms + or -5%, 1/16 w.
R748 thru R750	19A149818P101	Metal film: 100 ohms + or -5%, 1/16 w.
R751	19A149818P102	Metal film: 1K ohms + or -5%, 1/16 w.
R752	19A149818P101	Metal film: 100 ohms + or -5%, 1/16 w.
R754	19A149818P100	Metal film: 10 ohms + or -5%, 1/16 w.
R756	19A149818P392	Metal film: 3.9K ohms + or -5%, 1/16 w.
R757	19A149818P102	Metal film: 1K ohms + or -5%, 1/16 w.
R758 thru R760	19A149818P101	Metal film: 100 ohms + or -5%, 1/16 w.
R765	19A149818P101	Metal film: 100 ohms + or -5%, 1/16 w.
R770	19A149818P101	Metal film: 100 ohms + or -5%, 1/16 w.
R772	19A149818P473	Metal film: 47K ohms + or -5%, 1/16 w.
R773	19A149818P104	Metal film: 100K ohms + or -5%, 1/16 w.
R774	19A149818P473	Metal film: 47K ohms + or -5%, 1/16 w.
R775	19A149818P472	Metal film: 4.7K ohms + or -5%, 1/16 w.
R801 and R802	19A149818P473	Metal film: 47K ohms + or -5%, 1/16 w.
R804	19A149818P473	Metal film: 47K ohms + or -5%, 1/16 w.
R805	19A149818P561	Metal film: 560 ohms + or -5%, 1/16 w.
R806 and R807	19A149818P104	Metal film: 100K ohms + or -5%, 1/16 w.
R808	19A149818P102	Metal film: 1K ohms + or -5%, 1/16 w.
R809	19A149818P100	Metal film: 10 ohms + or -5%, 1/16 w.
R810	19A149818P0R0	Jumper.
R811	19A149818P103	Metal film: 10K ohms + or -5%, 1/16 w.
R812	19A149818P101	Metal film: 100 ohms + or -5%, 1/16 w.
R813	19A149818P102	Metal film: 1K ohms + or -5%, 1/16 w.
R814 thru R816	19A149818P101	Metal film: 100 ohms + or -5%, 1/16 w.
R818	19A149818P104	Metal film: 100K ohms + or -5%, 1/16 w.
R819	19A149818P100	Metal film: 10 ohms + or -5%, 1/16 w.
R820	19A149818P101	Metal film: 100 ohms + or -5%, 1/16 w.
R822	19A149818P474	Metal film: 470K ohms + or -5%, 1/16 w.
R823	19A149818P101	Metal film: 100 ohms + or -5%, 1/16 w.
		- - - - - - - - - - THERMISTOR - - - - - - - - -
RT601	19A705813P2	Thermistor: sim to AL03006-58.2K-97-G100.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - -
U301 and U302	19A705798P1	Linear: Dual JFET Op Amp; sim to TLO62CD.
U303	19A702705P4	Digital: Quad Analog Switch,,Multiplexer; sim to 4066 BM.
U304	19A705798P1	Linear: Dual JFET Op Amp; sim to TLO62CD.
U603	19A705452P2	Linear: Audio Amplifier; sim to NJM 2073D.
U701	RYT1236036/2C	Microprocessor, RAM.
U702	19A704727P6	Digital: Modem.
U703	344A4029P201	Digital: 128K x 8-Bit Flash EEPROM; sim to E28F001BX-T120.
U704	RYT1136039/6C	Regulator, voltage w/ON-OFF switch.
U705	349A9662G2	ADI ROM
U706	RYT1186063/1	ROM, 64 bit; sim to DS2401.
U707	RYT1196005/7C	RAM, 32k x 8 bit, CMOS.
U801	344A3202P201	Linear: Voltage Regulator; sim to LP2951ACM.
U802	RYT1186018/2C	EEPROM, 64K, CMOS.
U803	344A3800P102	Linear: Tone Generator; sim to PCD3312C.
U804	344A3291P1	Digital: Audio Signal Processor; sim to MB87780PFV-G-BND.
U805 and U806	344A3303P202	Linear: +5.5 Volt Regulator; sim to TK11455.
		- - - - - - - - - - CRYSTALS - - - - - - - - -
Y701	19A702511G64	Crystal unit, quartz 11.0592 MHz.
Y801	19A702511G65	Crystal unit, quartz: 3.57945 MHz.
Y901	19A702511G70	Crystal unit, 9.8304 MHz.

U805, U806



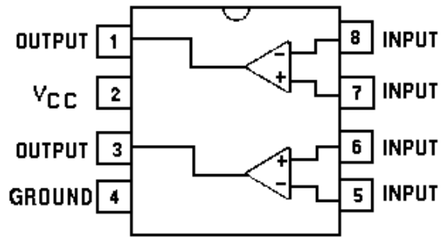
5.5 VOLT REGULATOR
344A3303P202

U301, U302, U304



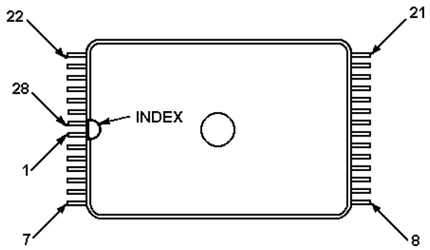
DUAL OP AMP
19A705798P1

U603



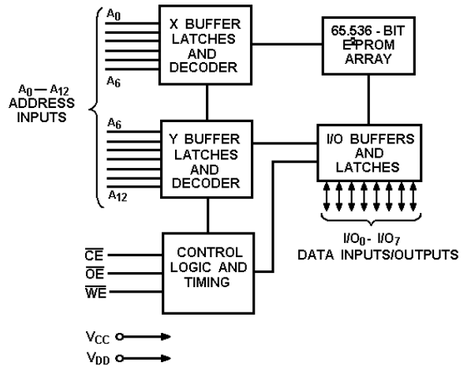
AUDIO AMPLIFIER
19A705452P2

U802



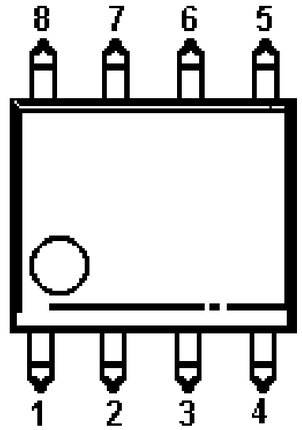
Terminal	Symbol	Function
1	NC	Not connected
2	A12	Address input
3	A7	Address input
4	A6	Address input
5	A5	Address input
6	A4	Address input
7	A3	Address input
8	A2	Address input
9	A1	Address input
10	A0	Address input
11	I/O0	Data input/output
12	I/O1	Data input/output
13	I/O2	Data input/output
14	GND	Ground
15	I/O3	Data input/output
16	I/O4	Data input/output
17	I/O5	Data input/output
18	I/O6	Data input/output
19	I/O7	Data input/output
20	$\overline{CE}$	Chip enable
21	A10	Address input
22	$\overline{OE}$	Output enable
23	A11	Address input
24	A9	Address input
25	A8	Address input
26	NC	Not connected
27	$\overline{WE}$	Write enable
28	Vcc	Supply voltage

BLOCK DIAGRAM



EEPROM
RYT1186018/2C

U801



VOLTAGE REGULATOR
344A3202P201

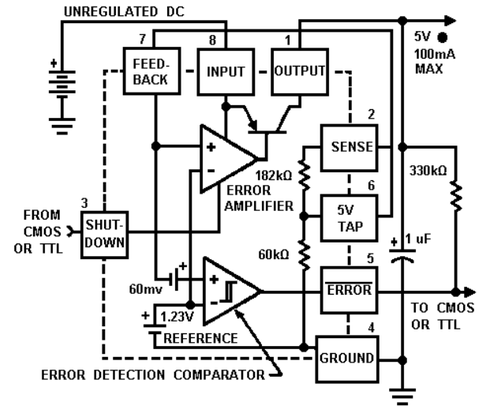
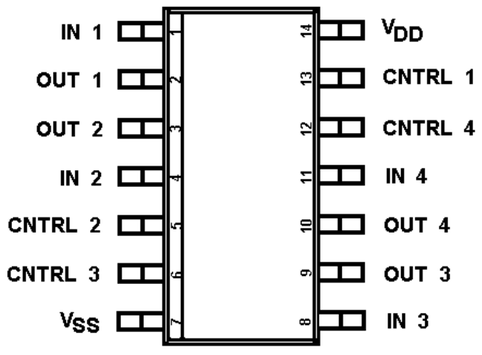


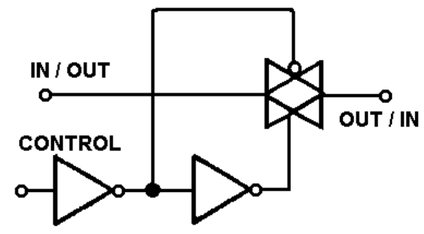
FIG. B FUNCTIONAL DIAGRAM & PINOUT

U303

PIN CONFIGURATION



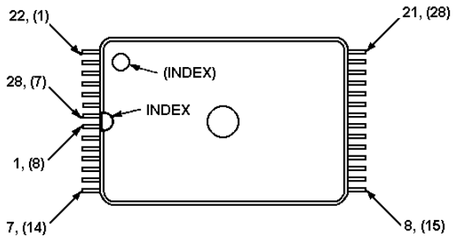
LOGIC DIAGRAM

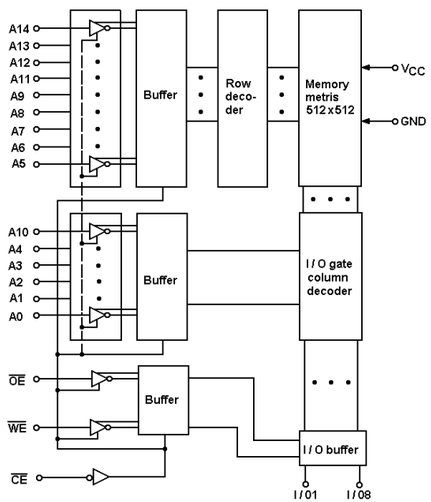


(1/4 OF DEVICE SHOWN)

QUAD ANALOG SWITCH
19A702705P4

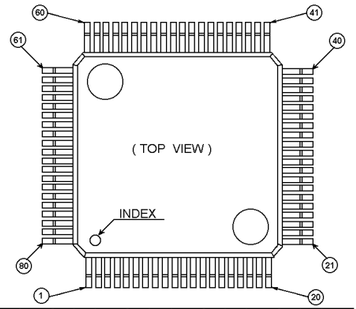
U707





Terminal	Symbol	Function
1,(8)	A14	Address input
2, (9)	A12	Address input
3, (10)	A7	Address input
4, (11)	A6	Address input
5, (12)	A5	Address input
6, (13)	A4	Address input
7, (14)	A3	Address input
8, (15)	A2	Address input
9, (16)	A1	Address input
10, (17)	A0	Address input
11, (18)	I/O1	Data input/output
12, (19)	I/O2	Data input/output
13, (20)	I/O3	Data input/output
14, (21)	GND	Ground
15, (22)	I/O4	Data input/output
16, (23)	I/O5	Data input/output
17, (24)	I/O6	Data input/output
18, (25)	I/O7	Data input/output
19, (26)	I/O8	Data input/output
20, (27)	$\overline{CE}$	Output enable (active low)
21, (28)	A10	Address input
22, (1)	$\overline{OE}$	Output enable (active low)
23, (2)	A11	Address input
24, (3)	A9	Address input
25, (4)	A8	Address input
26, (5)	A13	Address input
27, (6)	$\overline{WE}$	Write enable (active low)
28, (7)	Vcc	Supply voltage

RAM
RYT1196005/7C

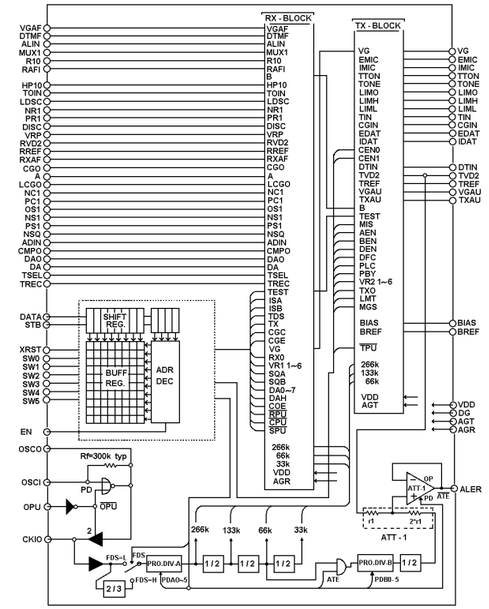


No	IO	name	No	IO	name	No	IO	name	No	IO	name	No	IO	name
1	–	NC	21	O	LDSC	41	G	AGR	61	–	NC			
2	I	OPU	22	O	LCGO	42	AO	MUX1	62	G	AGT			
3	G	DG	23	O	CMPO	43	AO	R10	63	AO	TVD2			
4	I	OSCI	24	–	NC	44	AI	RAFI	64	AO	TREF			
5	O	OSCO	25	I	TSEL	45	AO	HP10	65	AO	BIAS			
6	IO	CKIO	26	VD	VDD	46	AI	VRP	66	AO	BREF			
7	G	DG	27	AO	RXAF	47	AO	DA	67	AO	LIMH			
8	VD	VDD	28	AI	VGAF	48	AO	DAO	68	AO	LIML			
9	I	XRST	29	AI	DTMF	49	AI	ADIN	69	AO	LIMO			
10	I	EN	30	AI	ALIN	50	AI	DISC	70	AO	TONE			
11	I	STB	31	AI	NR1	51	IO	TREC	71	–	NC			
12	I	DATA	32	AI	PR1	52	AO	NSQ	72	AO	VGAU			
13	O	SW5	33	–	NC	53	AO	OS1	73	AI	EMIC			
14	O	SW4	34	AI	NC1	54	AI	NS1	74	AI	IMIC			
15	O	SW3	35	AI	PC1	55	AI	PS1	75	AI	TTON			
16	O	SW2	36	AO	A	56	–	NC	76	AO	ALER			
17	O	SW1	37	AO	CGO	57	AI	TIN	77	VD	VDD			
18	O	SW0	38	AI	TOIN	58	AI	CGIN	78	I	VG			
19	VD	VDD	39	AO	RREF	59	AI	DTIN	79	I	EDAT			
20	G	DG	40	AO	RVD2	60	AO	TXAU	80	I	IDAT			

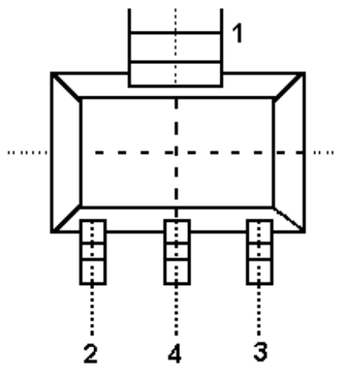
ASP
344A3291P1

Figure 3: Terminal Layout

U804



U706

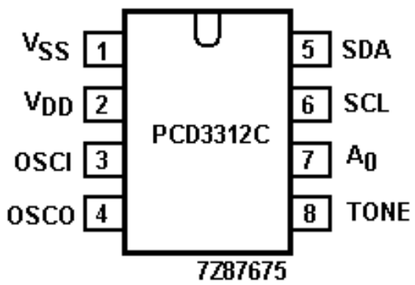


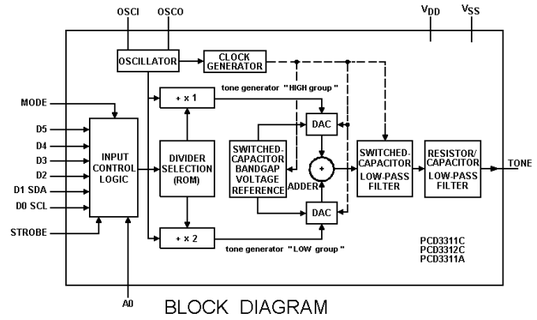
Terminal	Symbol	Function
1	GND	Ground pin
2	DQ	Data pin
3	---	Not connected
4	GND	Ground pin

NOTE: Power is derived from the data line.

ROM
RYT1186063/1

U803

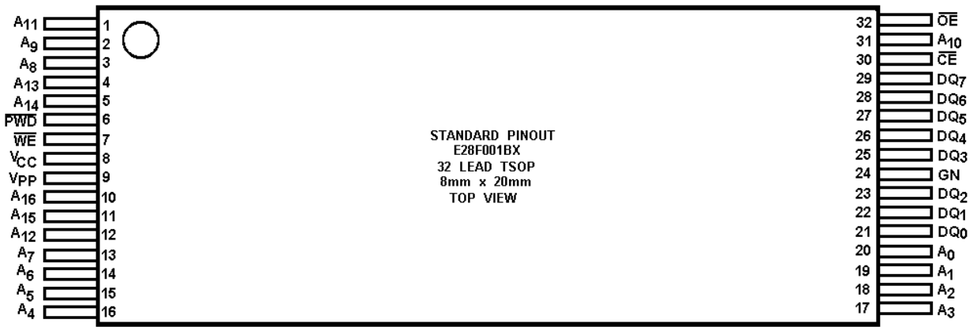




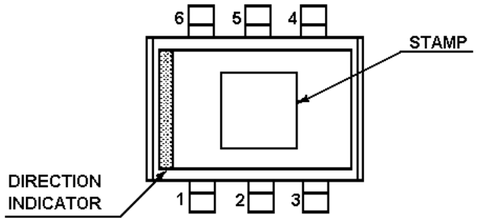
BLOCK DIAGRAM

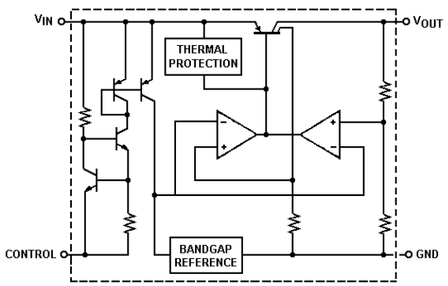
TONE GENERATOR
344A3800P102

U703



U704

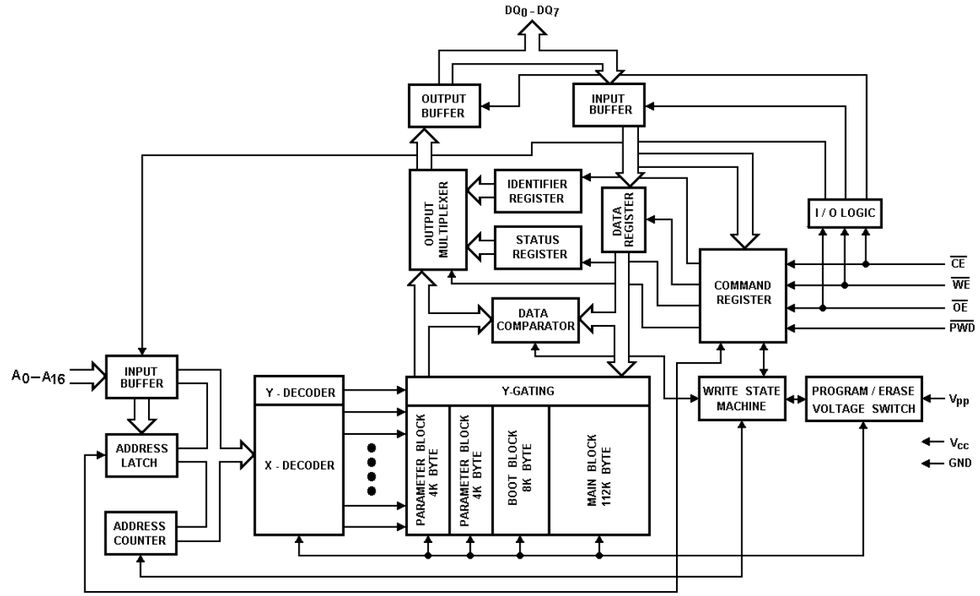




CONNECTIONS

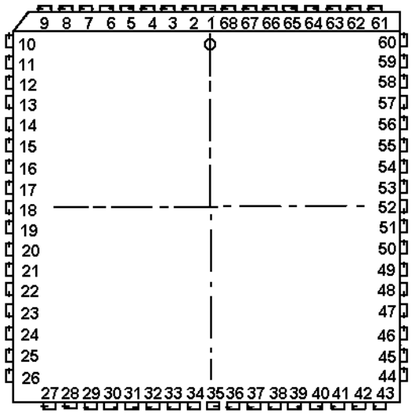
Terminal	Symbol	Function
1	CTRL	Control
2	NC	Not connected
3	GND	Ground
4	Vout	Output voltage
5	NC	Not connected
6	Vin	Input voltage
Note: Connect pin 2 and 5 to GND for maximum heat conduction.		

REGULATOR, VOLTAGE
RYT1136039/6C



EEPROM
344A4029P201

U701



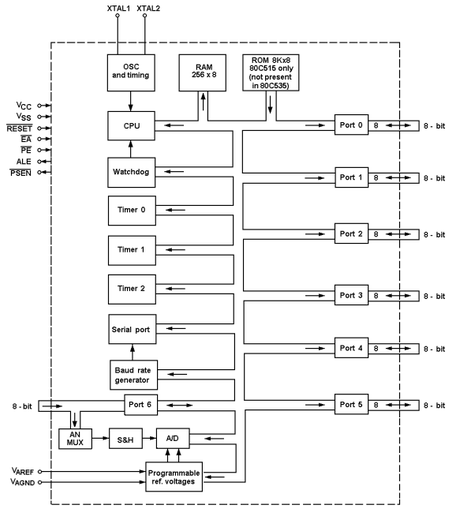
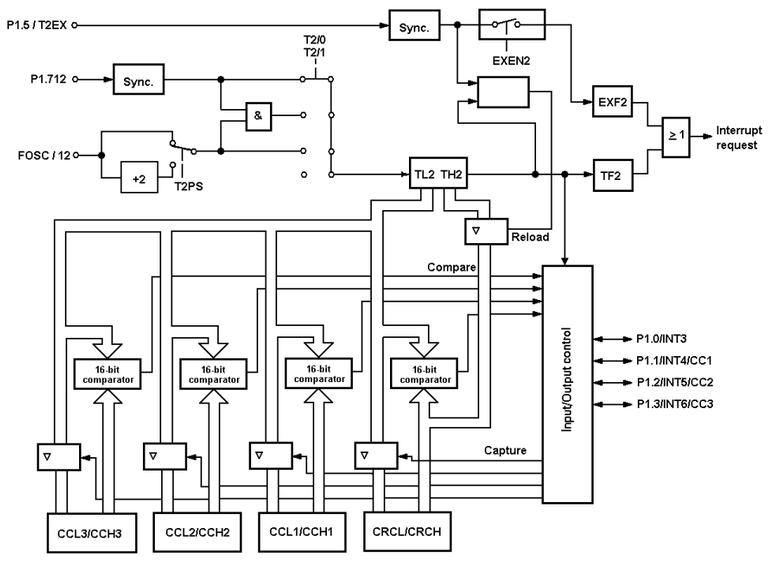


Figure 1



MICROPROCESSOR
RYT1236036/2C

Terminal	Symbol	Function
1	$\overline{\text{RESET}}$	Reset
2,13,14, 23, 32, 35, 46, 50, 51, 68, 70, 71	NC	Not connected
3	V_{AREF}	Reference voltage
4	V_{AGND}	Reference ground
5 - 12	P6.77/AIN7-P6.0/AIN 0	Port 6
15	P3.0/R_XD	Port3/Serial port's receiver data input (asynchronous) or data input/output (synchronous)
16	P3.1/T_XD	Port3/Serial port's transmitter data input (asynchronous) or clock output (synchronous)
17	P3.2/INT0	Port 3/Interrupt 0 input timer 0 gate control input
18	P3.3/INT1	Port 3/Interrupt 1 input timer 0 gate control input
19	P3.4/T0	Port 3/Counter 0 input
20	P3.5/T1	Port 3/Counter 1 input
21	P3.6/WR	Port 3/The write control signal latches the data byte from port 0into the external data memory
22	P3.7/RD	Port 3/The read control signal enables the external data memory to port 0
24	P1.7/T2	Port 1/Counter 2 input
25	P1.6/CLKOUT	Port 1/System clock output
26	P1.5/T2EX	Port 1/Timer 2 external reload trigger input
27	P1.4/INT2	Port 1/Interrupt 2 input
28	P1.3/CC3/INT6	Port 1/Interrupt 6 input/Compare 3 output/Capture 3 input
29	P1.2/CC2/INT5	Port1/Interrupt 5 input/Compare 2 output/capture 2 input

Terminal	Symbol	Function
30	P1.1/CC1/INT4	Port 1/Interrupt 4 input/Compare 1 outpu/Capture 1 input
31	P1.0/CC0/INT3	Port 1/Interrupt 3 input/Compare 0 output/Capture 0 input
33, 69	V_{CC}	Supply power
34	GND	Ground
36	XTAL2	XTAL2
37	XTAL1	XTAL1
38-45	P2.0/A_8-P2.7/A_{15}	Port 2
47	$\overline{\text{PSEN}}$	Program store enable #
48	ALE	Address latch enable
49	$\overline{\text{EA}}$	External access enable #
52-59	P0.0/AD_0-P0.7/AD_7	Port 0
60-67	P5.7-P5.0	Port 5
72-80	P4.0-P4.7	Port 4

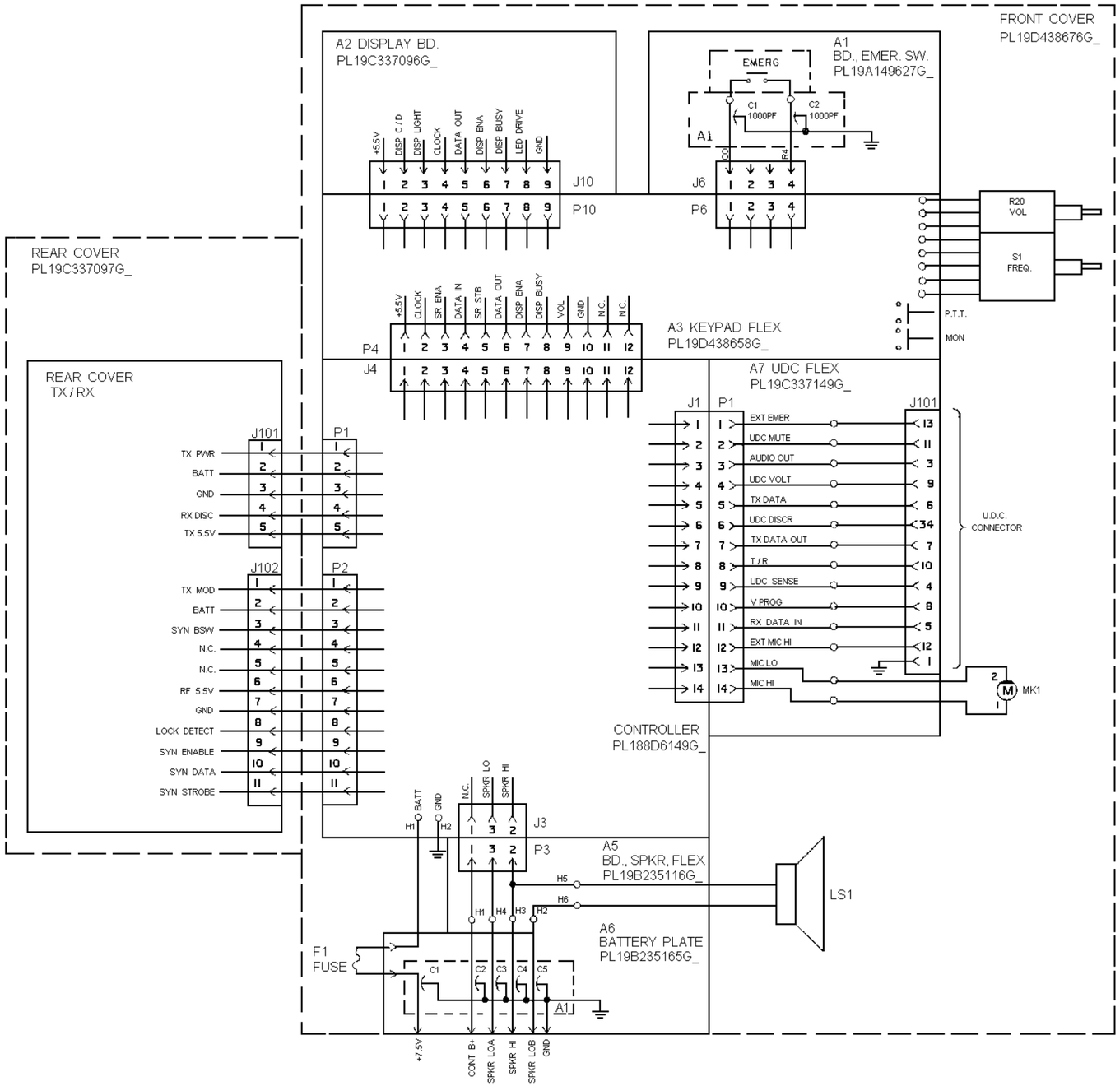
U702

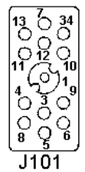
PIN NAME	28PACK PIN	44PACK PIN	DESCRIPTION
RE	1	39	READ ENABLE (ACTIVE LOW)
EN	2	41	CHIP ENABLE (ACTIVE LOW)
RESOUT	3	43	RESET OUTPUT (ACTIVE HIGH)
AD0	4	44	BI-DIRECTIONAL ADDRESS/DATA BUS
AD1	5	1	BI-DIRECTIONAL ADDRESS/DATA BUS
AD2	6	2	BI-DIRECTIONAL ADDRESS/DATA BUS
AD3	7	4	BI-DIRECTIONAL ADDRESS/DATA BUS
AD4	8	6	BI-DIRECTIONAL ADDRESS/DATA BUS
AD5	9	8	BI-DIRECTIONAL ADDRESS/DATA BUS
AD6	10	10	BI-DIRECTIONAL ADDRESS/DATA BUS
AD7	11	11	BI-DIRECTIONAL ADDRESS/DATA BUS
ALE	12	12	ADDRESS LATCH ENABLE (ACTIVE HIGH)
VSS	13	13	GROUND

PIN NAME	28PACK PIN	44PACK PIN	DESCRIPTION
CLK1	14	15	BUFFERED OSCILLATOR OUTPUT
VDD	15	17	POWER SUPPLY
XTAL1	16	19	OSCILLATOR INPUT
XTAL2	17	21	OSCILLATOR INPUT
CLK2	18	22	640 KHZ OUTPUT
DATAIN	19	23	RECEIVED DATA INPUT
SAT/G1	20	24	RECEIVED SAT INPUT/G1 EN. HC138 (ACT.HI)
TXDAT	21	26	TRANSMIT DATA OUTPUT
RCVCLK/Q2	22	28	RECOVERED CLOCK OUTPUT/Q2 OUTPUT FOR HC138
RCVDAT/Q0	23	30	RECOVERED DATA OUTPUT/Q0 OUTPUT FOR HC138
INT	24	32	INTERRUPT REQUEST (ACTIVE LOW O.D.)
RESIN	25	33	RESET INPUT (ACTIVE HIGH)
CS	26	34	CHIP SELECT (ACTIVE LOW)

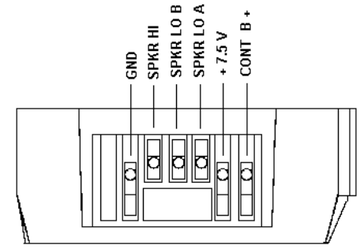
PIN NAME	28PACK PIN	44PACK PIN	DESCRIPTION
CLK3/4	27	35	TRANSMIT CLOCK OUTPUT/CLK1/6 OUTPUT
WR	28	37	WRITE ENABLE (ACTIVE LOW)
MODE	NC	18	Enable 44 pin functions (active low)
A	NC	38	A input for HC138
B	NC	36	B input for HC138
C	NC	31	C input for HC138
G28	NC	20	G2B enable for HC38 (active low)
A0	NC	40	A0 address input
A1	NC	42	A1 address input
A2	NC	3	A2 address input
A3	NC	5	A3 address input
A4	NC	7	A4 address input
A5	NC	9	A5 address input
A6	NC	14	A6 address input
A7	NC	16	A7 address input
Q1	NC	29	Q1 output for HC138
Q3	NC	27	Q3 output for HC138
Q47	NC	25	Q4-Q7 (ored internally) output for HC138

MODEM
19A704727P6





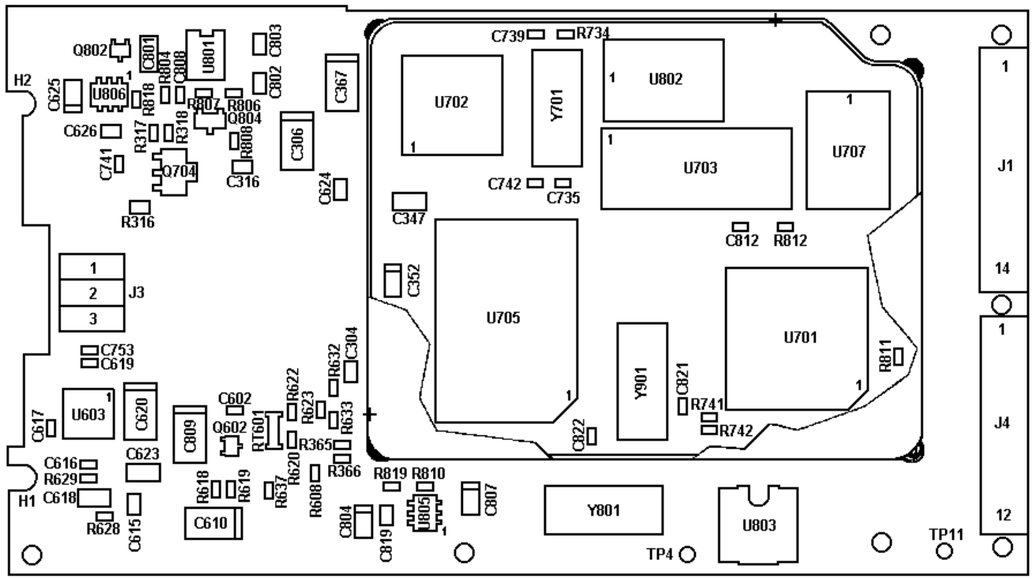
UDC CONTACT IDENTIFICATION
VIEWED FROM OUTSIDE OF CASE



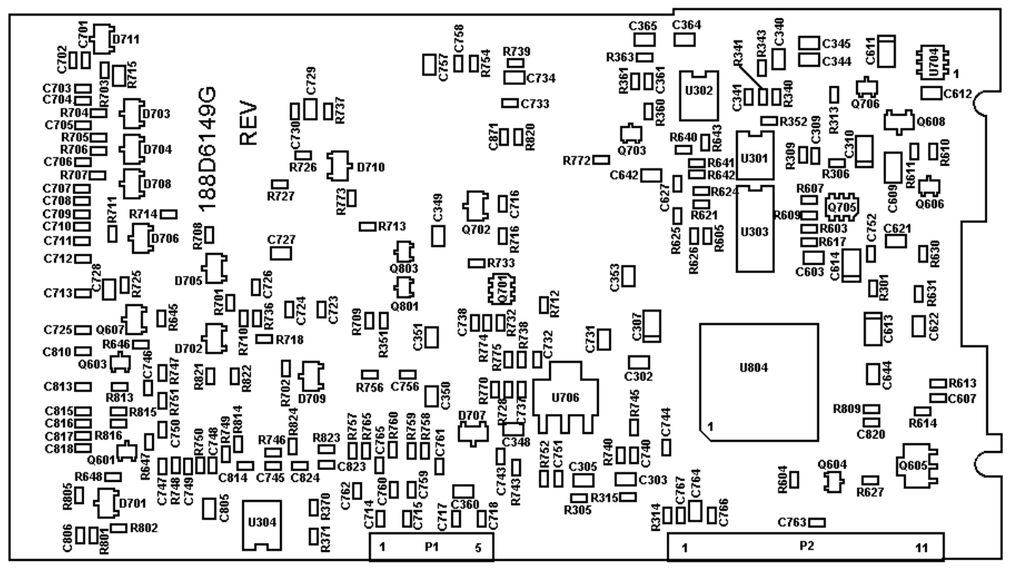
BATTERY CONTACT IDENTIFICATION
VIEWED FROM OUTSIDE OF CASE

COMPLETE RADIO INTERCONNECTION

(Made from 19D902383, Sh. 2, Rev. 1)



VIEW FROM COMPONENT SIDE



VIEW FROM SOLDER SIDE

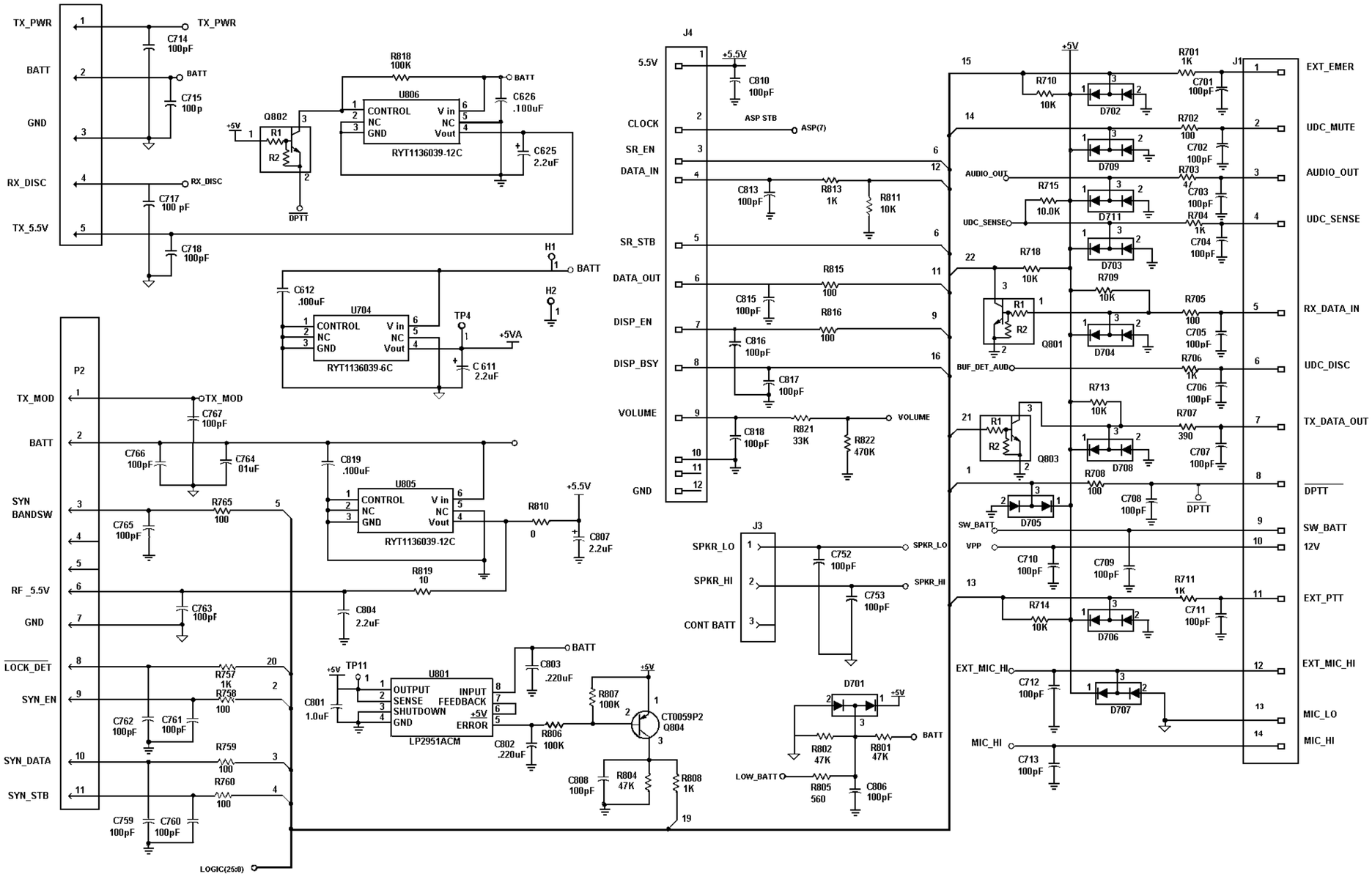
CAUTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES

(1) NOTES:

5. THE FOLLOWING DEVICES ARE ELECTROSTATIC SENSITIVE DEVICES REQUIRING SPECIAL CARE PER 19A701294:
U303, U701, U702, U703, U705, U706, U707, U802, U803, & U804

CONTROL BOARD
188D6149G1

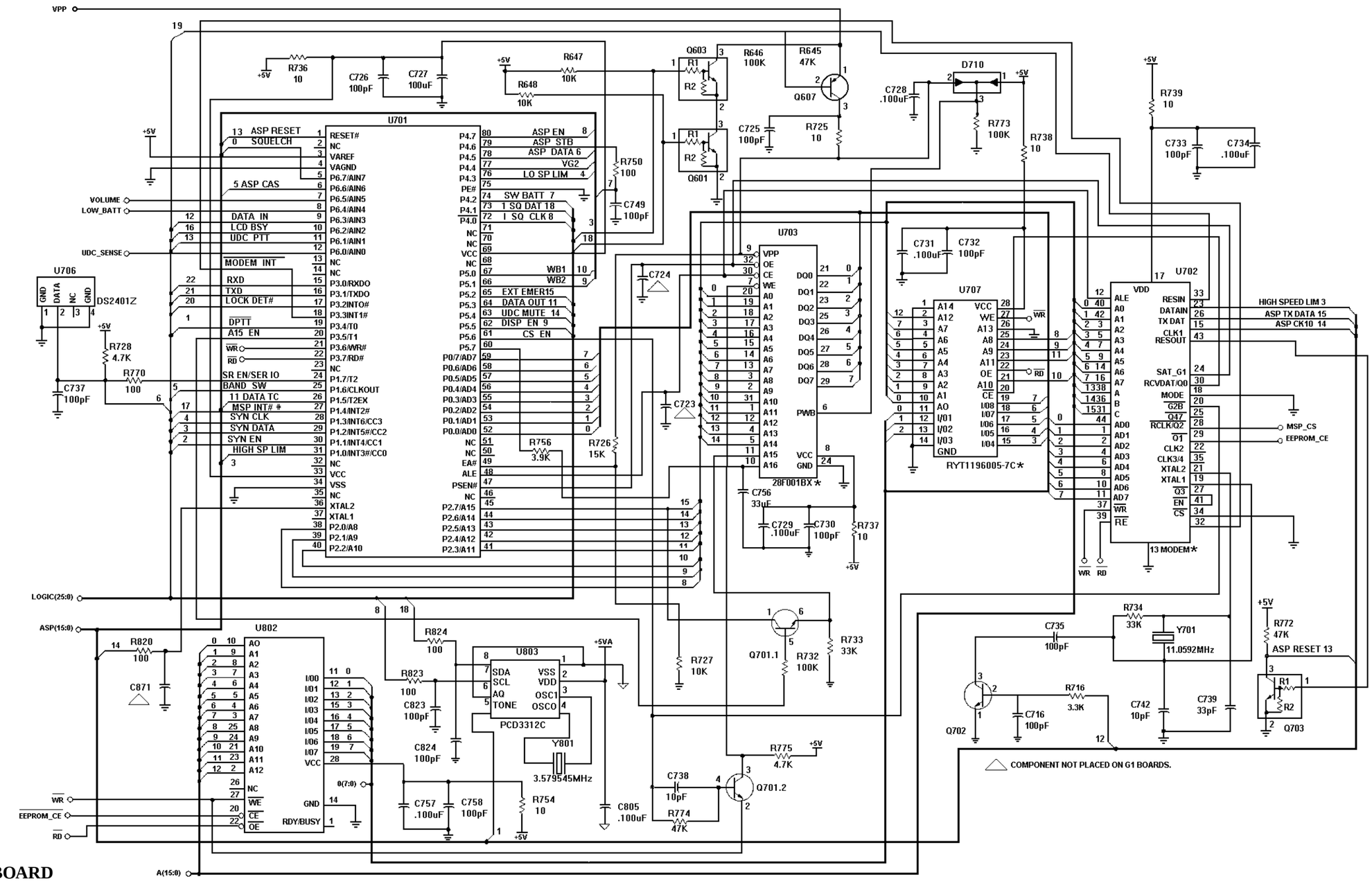
(188D6149 Rev. 2)



THIS SCHEMATIC DIAGRAM APPLIES TO	
MODEL NO.	REV LETTER
188D6149G1	D

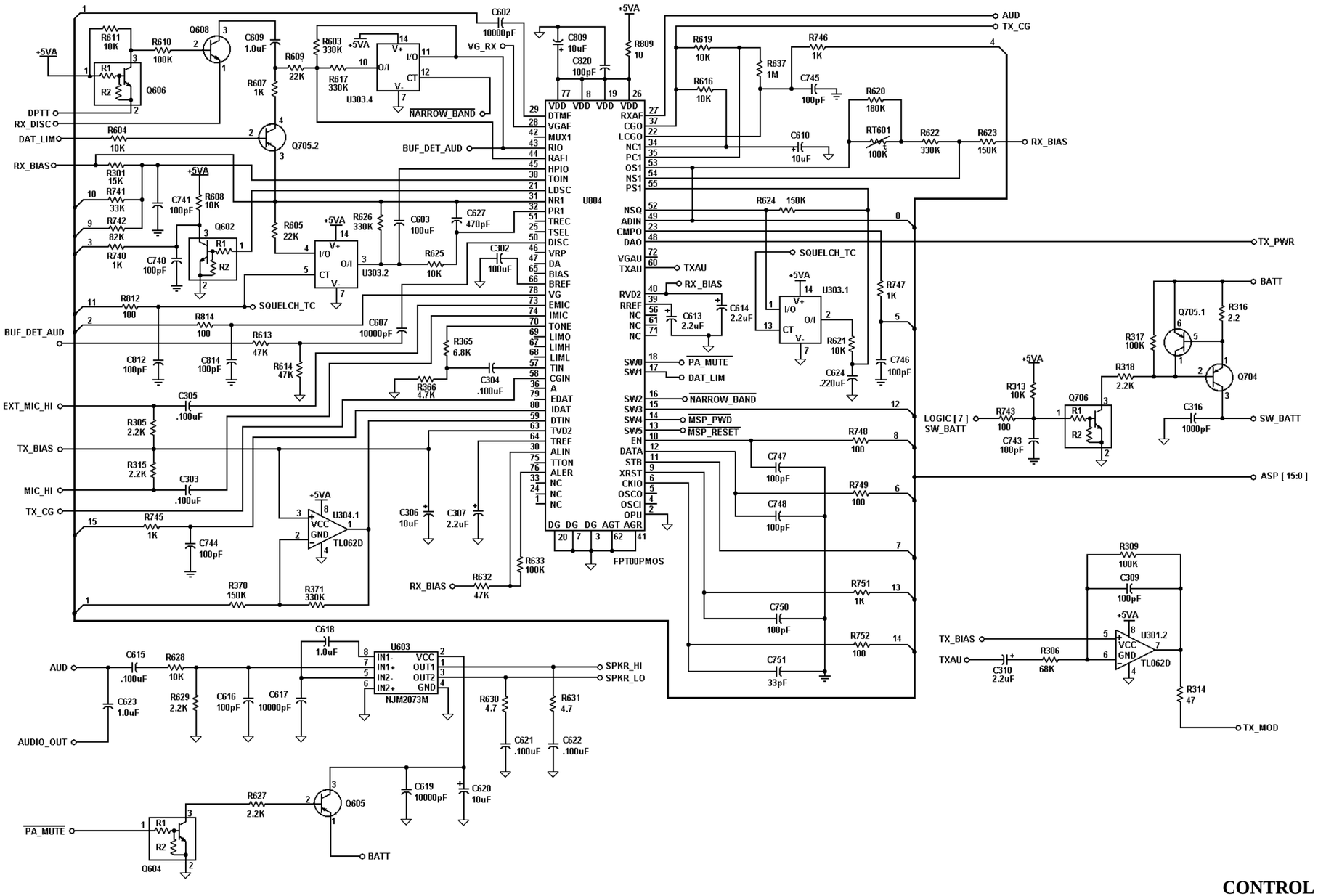
CONTROL BOARD
188D6149G1

(188D6151, Sh. 1, Rev. 5)



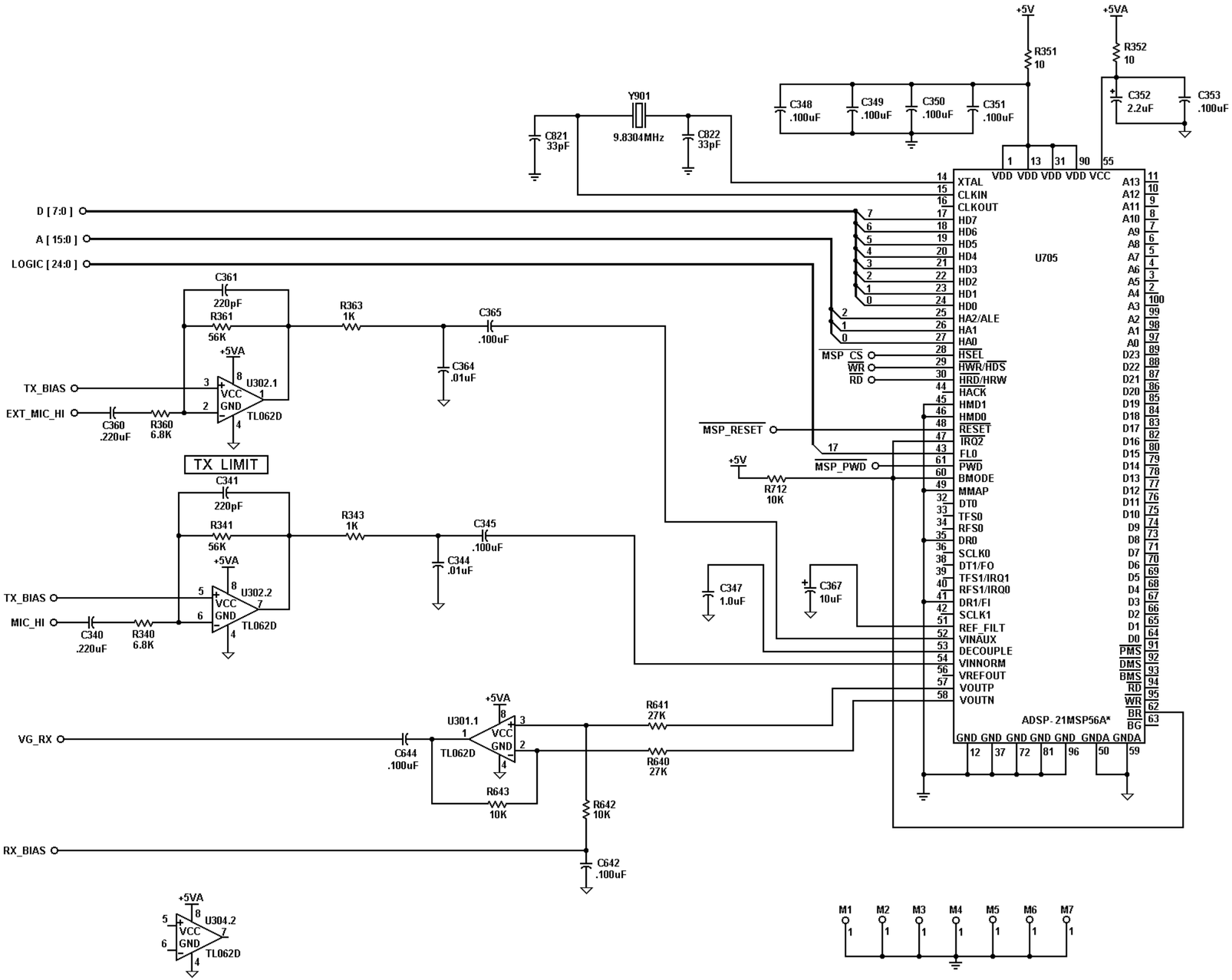
CONTROL BOARD
188D6149G1

(188D6151, Sh. 2, Rev. 5)



CONTROL BOARD
188D6149G1

(188D6151, Sh. 3, Rev. 5)



CONTROL BOARD
188D6149G1

(188D6151, Sh. 4, Rev. 5)

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