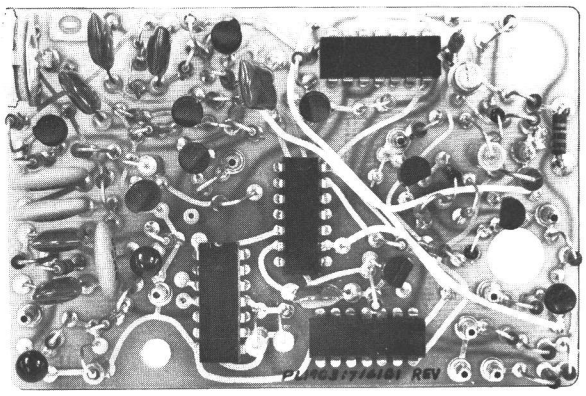
MOBILE RADIO

MASTR® Progress Line

PRIORITY SEARCH-LOCK MONITOR
(Options 7026 thru 7030, 7676 thru 7679, 7458 & 7460)



SPECIFICATIONS *

Priority Search-Lock Monitor	
For Mobile Combinations	19A127557-G1 (Options 7026 thru 7030)
For Station Combinations	19A127679-G1 (Options 7676 thru 7679) (Options 7458 and 7460)
Search Rate (Each Channel)	Four times per second
Sample Time (Each Channel)	125 milliseconds
Priority Channel Search Rate	Four times per second
Priority Channel Sample Time	Six milliseconds
Priority Squelch Sensitivity	20-dB quieting
Input Power	50 milliamperes at +10 volts DC
Silicon Transistors	13
Integrated Circuit Modules	4
Temperature Range	-30°C to +60°C
Dimensions	2-3/8" x 3-3/4"

*These specifications are intended primarily for the use of the serviceman. Refer to the appropriate Specification Sheet for the complete specifications.

PRIORITY SEARCH-LOCK MONITOR

GENERAL ELECTRIC

TABLE OF CONTENTS

WARNING

Under no circumstances should any person be permitted to handle any portion of the equipment that is supplied with high voltage, or to connect any external apparatus to the units while the units are supplied with power. KEEP AWAY FROM LIVE CIRCUITS.

ADDENDUM TO LBI4050

DC/TONE REMOTE CONTROL STATIONS
(Refer to Figure 3A)

In DC/TONE Remote Control Stations three different control currents or Audio Tones on the control line select the receiver frequencies.

When -6 mA's of current for DC Control (or a tone of 1750 Hz for Tone Control) appears on the control line, this current (or tone) is detected and Q21 (or Q4) is turned on. This places +10 Volts on the Rec F1 line to lock the receiver on F1.

When -11 mA's of current for DC Control (or a tone of 1650 Hz for Tone Control) appears on the control line, this current (or tone) is detected and Q19 (or Q8) is turned on. This places +10 Volts on the Rec F2 line to lock the receiver on F2.

When 0 mA's of current for DC Control (or a tone of 1050 Hz for Tone Control) is present on the control line, this current (or tone) is detected and Q16 (or Q11) is turned on. This removes +10 Volts from either receiver oscillator and applies +10 Volts to the F1 priority input on the PSLM. This activates the PSLM which alternately switches +10 Volts to each of the receiver oscillators at a rate of four times per second. If a signal is received on either channel, the PSLM will lock on that channel for the duration of the message, or until a signal is received on the priority channel.

NOTE

The PSLM is normally strapped for F1 priorty. To change or disable the priority function, refer to notes 2 and 3 on the Schematic Diagram for the PSLM.

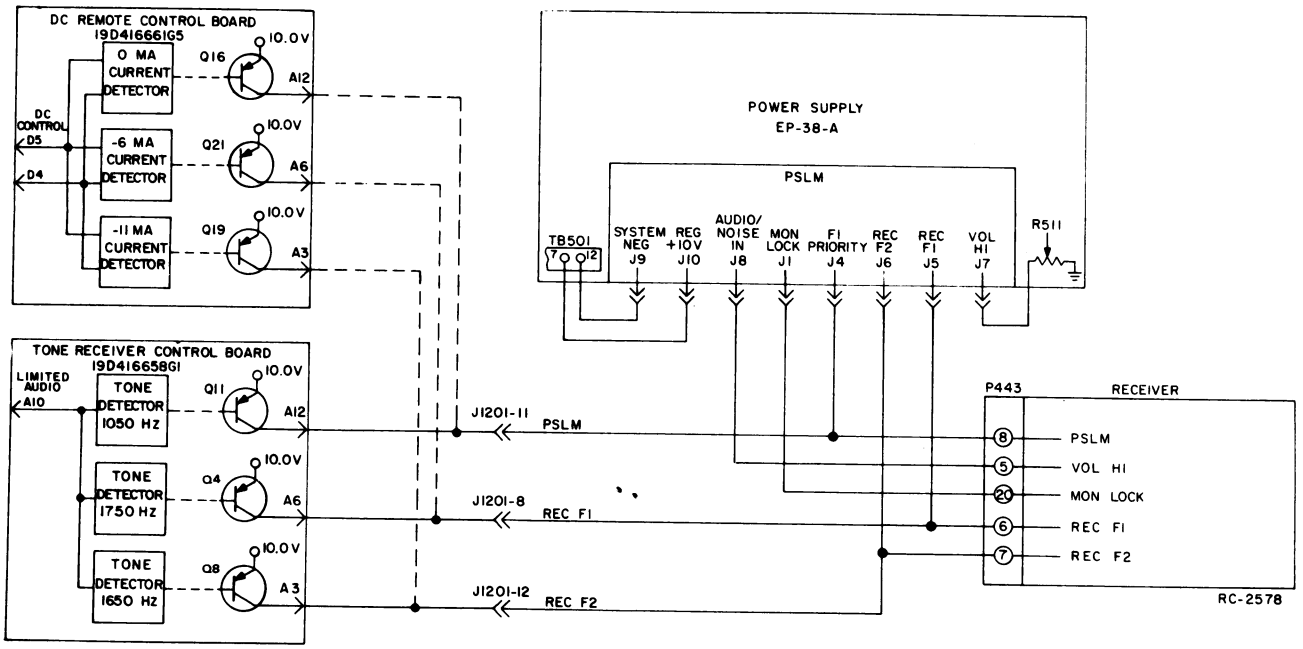


Figure 3A DC/TONE Remote Control Switching Diagram

DESCRIPTION

General Electric Priority Search-Lock Monitor provides two-channel monitoring by alternately searching a priority channel and a non-priority channel. The Priority Search-Lock Monitor (PSLM) assures reception of all signals received on the priority channel regardless of signal strength or which channel receives the first signal.

When a signal is received on the priority channel, the PSLM stops searching and locks on the priority channel for the duration of the message. When a signal is first received on the non-priority channel, the PSLM stops on that channel while monitoring the priority channel. If a signal is received on the priority channel while the PSLM is stopped on the non-priority channel, the PSLM reverts to the priority channel and locks on that channel for the duration of the message.

NOTE

The PSLM will operate only when the receiver is squelched. When the receiver is unsquelched, the PSLM will lock on either the F1 or F2 channel.

Also, operating the PSLM with the control unit squelch set at maximum (fully counterclockwise) may result in a repetitive thumping sound in the speaker. This is caused by a priority channel that is slightly weaker than the receiver maximum squelch sensitivity being rapidly accepted and rejected by the receiver squelch circuit.

In mobile applications, the priority channel is selected by means of the frequency selector switch on the control unit, or is locked on the F1 channel (depending on the option number). In station applications, the priority channel is locked on either the F1 or F2 channel by simply changing a connection on the PSLM board. Instructions for making this change are contained on the Schematic Diagram (see Table of Contents).

In applications where a priority channel is not desired, the priority feature may be disabled by removing capacitor C2 on the PSLM board. When C2 is removed, the PSLM will alternately search both channels and will lock on the channel receiving the first signal.

The mobile and station option numbers and the application of each option are shown in the following chart.

NOTE

Both the control unit and PSLM board are modified for Options 7027 & 7028. Refer to the System Modifications section as listed in the Table of Contents for a description of the modifications.

MOBILE OPTIONS

Option Number	Priority Channel	Number of Frequencies	
		Xmtr	Rcvr
7026	F1 or F2 (selected by operator)	2	2
7027	Locked on F1	1	2
7028	Locked on F1	2	2
7029 and 7030	F1 or F2 (selected by operator)	1	2

STATION OPTIONS

Option Number	Station Control	Number of Frequencies	
		Xmtr	Rcvr
7676	Local & Local/Remote	1	2
7677	Local & Local/Remote	2	2
7678	Remote	1	2
7679	Remote	2	2
7458	DC Remote	1 or 2	2
7460	Tone Remote	1 or 2	2

MOBILE AND STATION SWITCHING

MOBILE COMBINATIONS

In mobile combinations, the operation of the PSLM is controlled by the SEARCH-OFF switch and the frequency selector switch on the control unit. The SEARCH-OFF switch controls the operation of the PSLM. The frequency selector switch (marked F1 and F2) selects the priority channel, or the operating channel when the PSLM is disabled (see Figure 1).

With the SEARCH-OFF switch in the SEARCH position, +10 Volts is connected through the frequency selector switch to the F1 or F2 Priority input on the PSLM board to determine the priority channel. The PSLM alternately switches +10 Volts to each receiver oscillator at a rate of four times

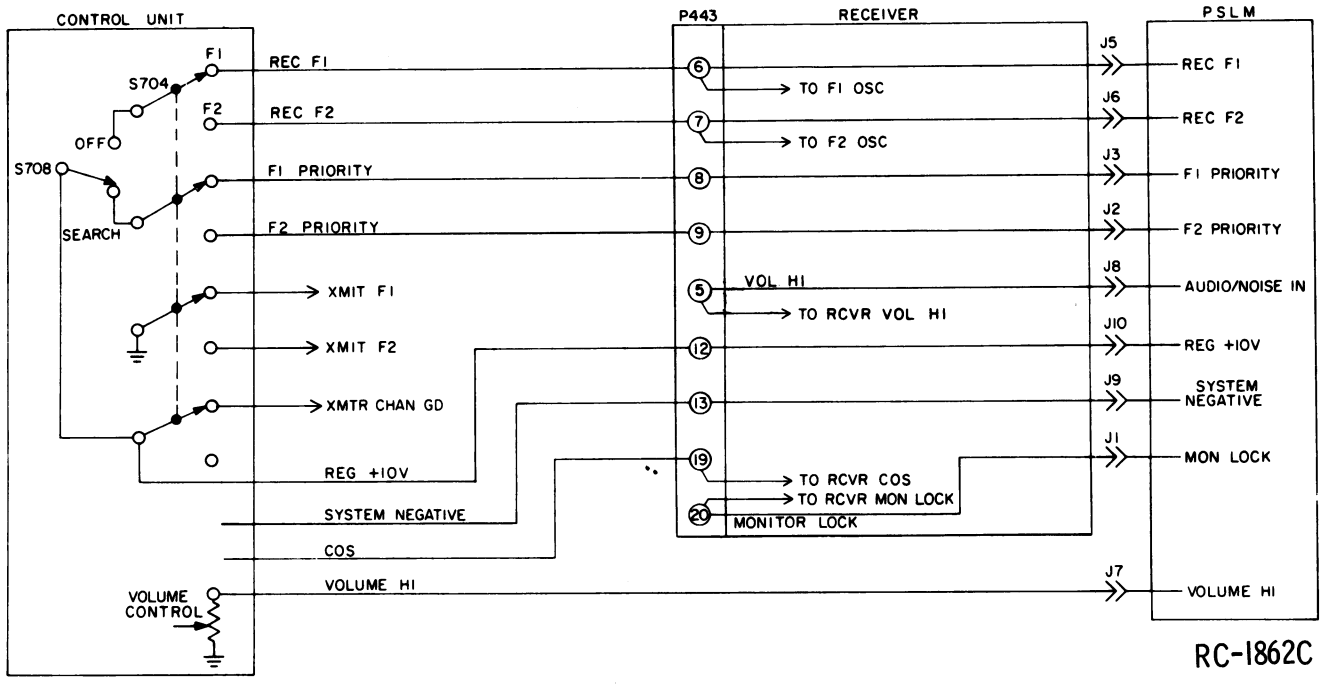


Figure 1 - Mobile Switching Diagram

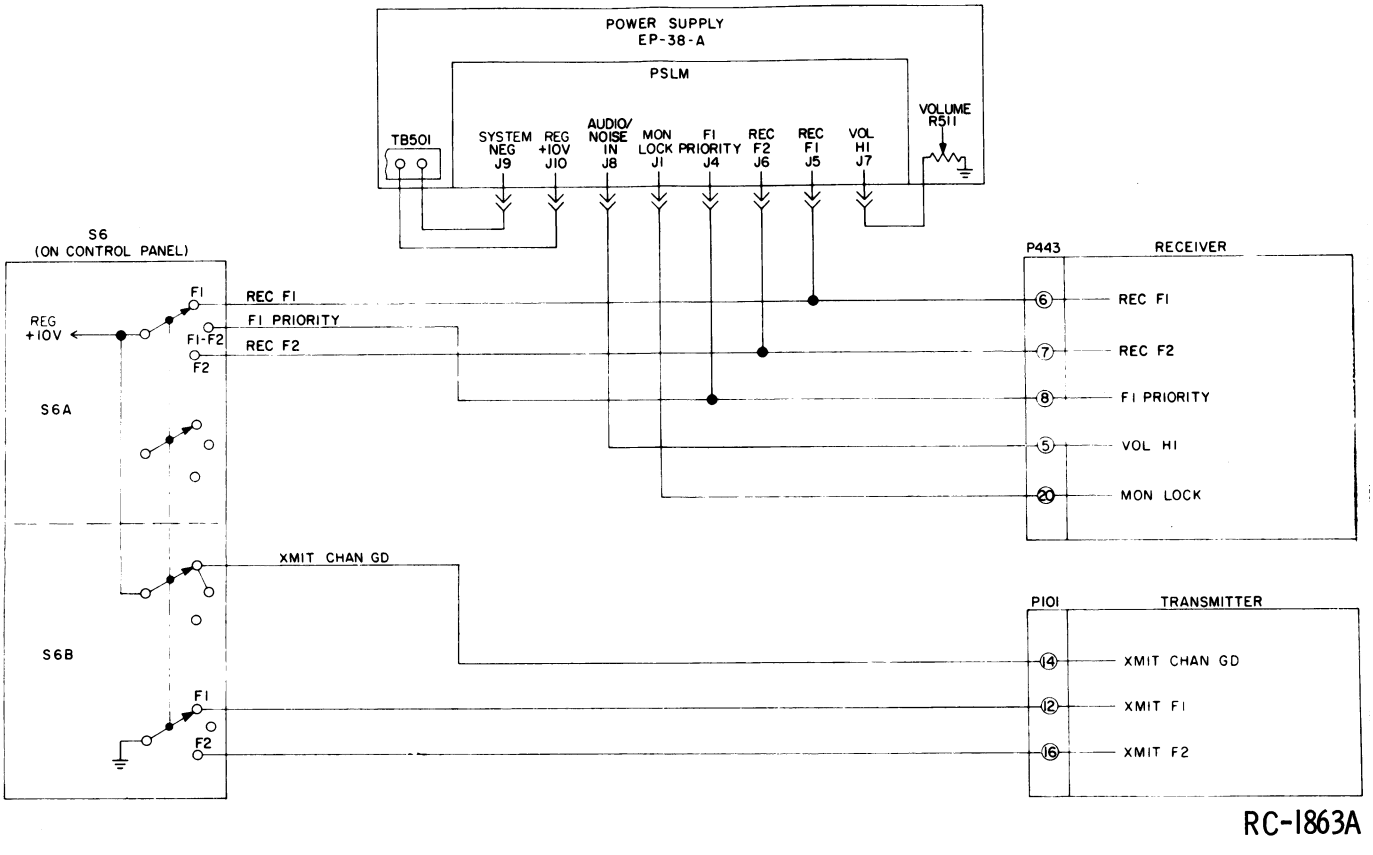


Figure 2 - Local and Local/Remote Switching Diagram

per second. When a signal is received on either channel, the PSLM will lock on that channel for the duration of the message, or until a signal is received on the priority channel.

The frequency selector switch also selects the transmitter oscillator.

With the SEARCH-OFF switch in the OFF position, the +10 Volts is removed from the F1 or F2 Priority input on the PSLM, and is connected directly to the receiver oscillator, overriding the PSLM. Now, only the channel selected by the frequency selector switch will be monitored.

If operator selection of the priority channel is not desired, the priority channel may be locked on the F1 or F2 channel by simply changing a connection to the PSLM F1 or F2 Priority input. Instructions for making this change are contained on the PSLM Schematic Diagram (see Table of Contents).

NOTE

In radios equipped with transmitter Channel Guard encoders, the encoder will operate when the frequency selector switch is in the F1 position only.

LOCAL & LOCAL/REMOTE STATIONS

In local and local/remote stations, the PSLM is controlled by a three-position switch on the station control panel marked F1, F1-F2 and F2 (see Figure 2).

Turning the switch to the F1-F2 position removes the +10 Volts from either receiver oscillator, and applies +10 Volts to the F1 priority input on the PSLM. This activates the PSLM which alternately switches +10 Volts to each of the receiver oscillators at a rate of four times per second. If a signal is received on either channel, the PSLM will lock on that channel for the duration of the message, or until a signal is received on the priority channel.

When the switch is in the F1-F2 position, the transmitter will operate on F1 frequency only.

NOTE

In radios equipped with transmitter Channel Guard encoders, the encoder will operate only when the frequency selector switch is in the F1 or F1-F2 position.

Turning the switch to the F1 or F2 position applies +10 Volts to the selected receiver oscillator, and overrides the PSLM. Now, only the channel selected will be monitored. Switching to the F1 or F2 position also selects the transmitter oscillator.

REMOTE CONTROL STATIONS

In remote control stations, two pushbuttons (R-F1 and R-F2) on the Transistorized Control Console activate relays K1 and K2 on the remote control panel to switch receiver frequencies (see Figure 3).

When R-F1 and R-F2 pushbuttons are both pressed in (or both are out), neither of the relays is energized. No voltage is

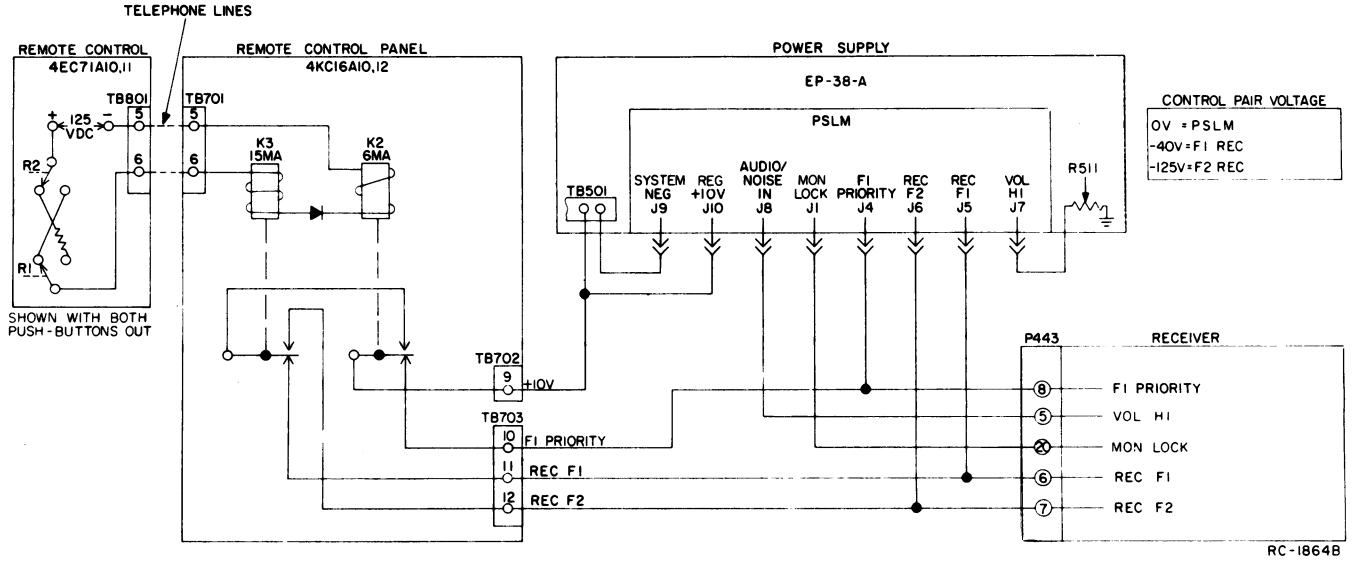


Figure 3 - Remote Control Switching Diagram

connected through the relays to the receiver oscillator, and +10 Volts is connected through the normally-closed contacts of K2 to the F1 Priority input of the PSLM. The PSLM alternately switches +10 Volts to each receiver oscillator four times per second. When a signal is received on either channel, the PSLM will lock on that channel for the duration of the message, or until a signal is received on the priority channel (F1).

Pressing in the R-F1 pushbutton applies 40 Volts to the relays on the remote control panel, energizing relay K2 and applying +10 Volts to the F1 receiver oscillator. The +10 Volts overrides the PSLM and turns on the F1 receiver oscillator.

Pressing in the R-F2 pushbutton applies 125 Volts to the remote control panel, energizing relays K1 and K2 and applying +10 Volts to the F2 receiver oscillator. The +10 Volts overrides the PSLM and turns on the F2 oscillator.

The transmitter frequencies are selected by the T-F1 and T-F2 pushbuttons on the Transistorized Control Console.

LOGIC CIRCUITS

This section contains a detailed description of all of the logic circuits used in the PSLM board. It is suggested that the serviceman study the following information carefully, as a good understanding of basic logic circuitry is essential for servicing the PSLM.

SOLID STATE SWITCHES

An ideal switch has infinite resistance when open and zero resistance when closed. The transistor and semiconductor diode can be made to approach these conditions while operating at a much higher rate than conventional switches. Logic circuits are primarily switching devices which are either in a state of full conduction (saturated) or turned off. These devices can be switched from one state to the other as rapidly as required by the circuit function.

DIODE SWITCH

A semiconductor diode presents maximum resistance to the circuit when the diode is reversed biased or there is no difference of potential between the cathode or anode (see Figure 4). Applying a negative potential to the cathode of the diode (with respect to the anode), or a positive potential (with respect to the cathode) to the anode of sufficient amplitude to overcome the series resistance of the diode, forward biases the diode causing it to conduct. The diode now switches from maximum to minimum resistance.

The resulting current flow in the diode circuit increases from near zero to the maximum value allowed by the amplitude of the switching voltage and the series resistance of the circuit.

TRANSISTOR SWITCH & INVERTER

The high value of "off" resistance and the low value of "on" resistance make the

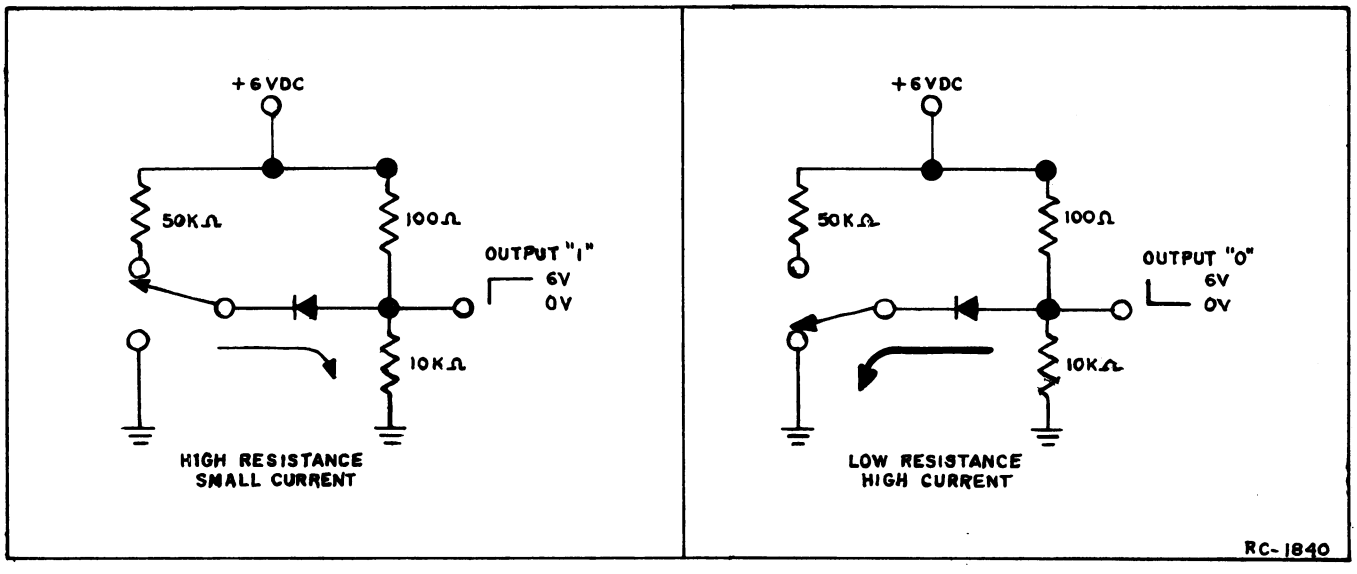


Figure 4 - Diode Switching Circuit

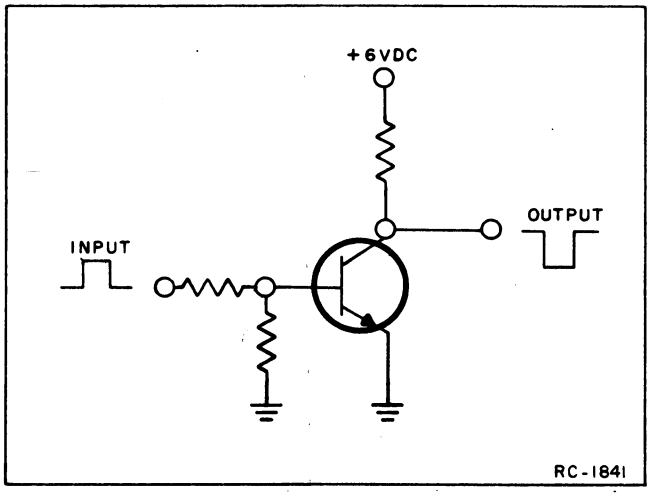


Figure 5 - Transistor Switch & Inverter

transistor invaluable for switching applications. When no base current is applied to the transistor switch shown in Figure 5, and the collector has the proper voltage applied, the open circuit resistance of the transistor approaches several megohms. If sufficient base current is suddenly applied to drive the transistor into saturation (turned ON), the collector-emitter resistance will drop to as low as 1.0 ohm. Voltage across the transistor under these conditions may be only a few tenths of a Volt.

The transistor stage shown in Figure 5 can also be used as an inverter for reversing the polarity of the input signal. A positive signal applied to the base-emitter junction will cause the collector voltage to drop from +6 Volts to near ground potential.

GATING CIRCUITS

Formal logic requires that a statement be either true or false; no other condition can exist for the statement. A logic circuit is basically a switch or gate that is either closed or open; no other condition can exist for the circuit. By logical arrangement of these gating circuits, electrical functions can be performed in a predetermined sequence by opening or closing the gates at the proper time.

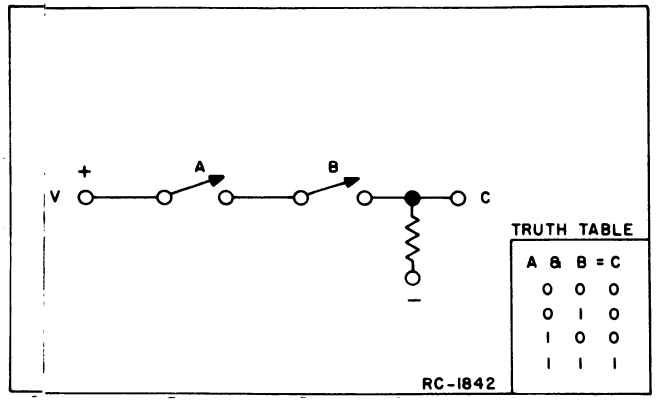


Figure 6 - Simple AND Gate

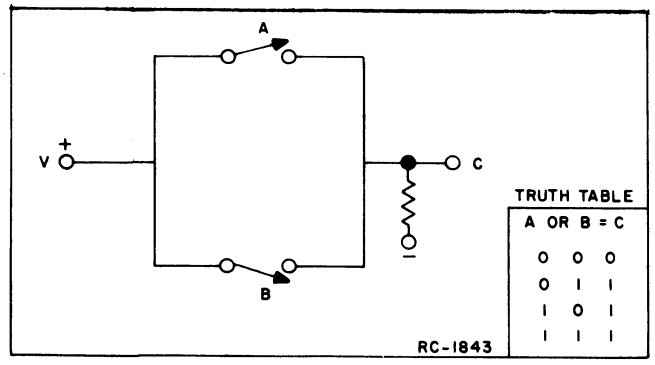


Figure 7 - Simple OR Gate

A single-pole, single-throw switch is equivalent to a binary device with only two possible operating conditions: either open or closed. If point "C" of Figure 6 is to be made equal to potential V, switches A and B must be closed. It can then be said that A AND B = C. If switches A and B are considered as gates, then potential V is said to be gated to "C" when both gates are closed. By representing the closed state of a switch or gate as "1" and the open state of a switch or gate as "0", then all possible conditions for the AND gate are shown in the Truth Table in Figure 6.

In Figure 7, if point "C" is to be made equal to potential V, either switch A or B (or both) may be closed. It can then be said A OR B = C. All possible conditions for the OR gate are shown in the Truth Table in Figure 7.

DIODE GATING CIRCUITS

In gating circuits, the desired state of the gate may be represented by either "0"

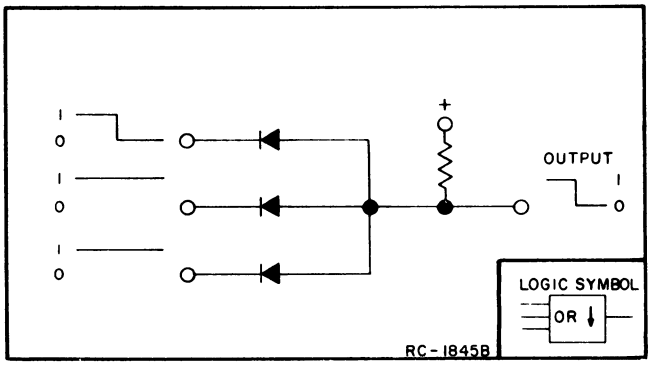


Figure 8 - Diode OR Gate

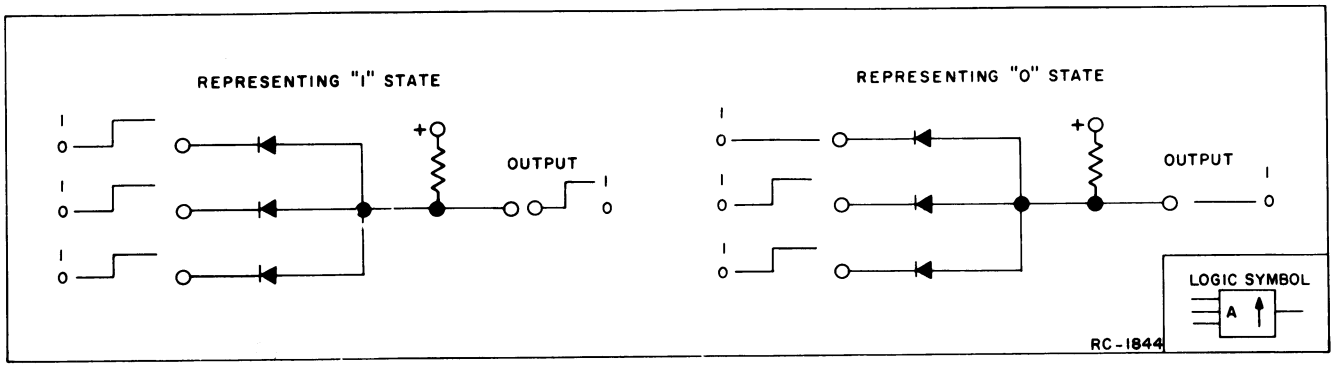


Figure 9 - Diode AND Gate

or "1". In this section, "1" will be used to represent a positive potential (approximately +6 Volts) and "0" will be used to represent a low potential (near zero Volts).

Logic Symbols

The use of logic symbols in this manual provides a simple method of showing the function of complicated logic circuits without drawing each diode, resistor and transistor in the circuit. The individual symbols can be tied together to form a logic diagram of a complete unit. Logic symbols of circuits used in the PSLM are shown in the following simplified diagrams.

OR Gate

A simple diode OR gate is shown in Figure 8. The same conditions exist in this circuit as the switch gate of Figure 7. Application of a positive potential at any of the inputs will result in an output of the same polarity, representing the "1" state.

AND Gate

A simple diode AND gate is shown in Figure 9. The same conditions exist in this circuit as in the switch gate of Figure 6. Application of a positive potential to the diodes at all inputs will result in a positive potential at the output. This represents the "1" state of the gate. Application of a positive potential to one or two terminals will result in no potential developed, representing the "0" state of the gate.

NAND Gate

The basic logic circuitry used in the PSLM is the NAND gate (NOT-AND). A NAND gate is simply an AND gate with a transistor inverter (NOT) stage added (see Figure 10). Applyinga positive potential to inputs A and B back biases diodes CR1 and CR2, permitting inverter Q1 to conduct. When conducting, the collector of Q1 drops to near ground potential.

Additional buffer or amplifier stages are usually added to the NAND gate to provide better isolation and increased gain. These additional stages are connected so that the logical output of the inverter is not changed.

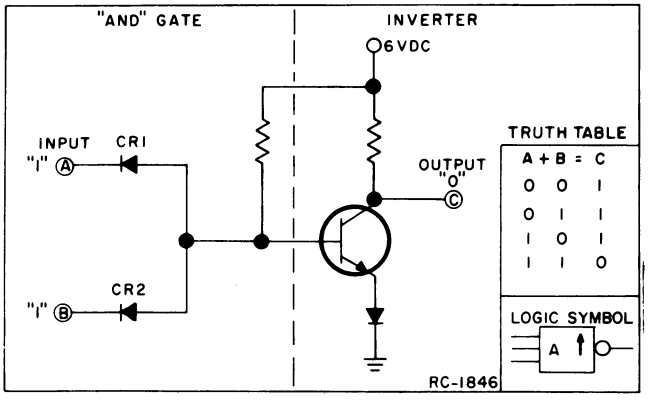


Figure 10 - Simplified NAND Gate

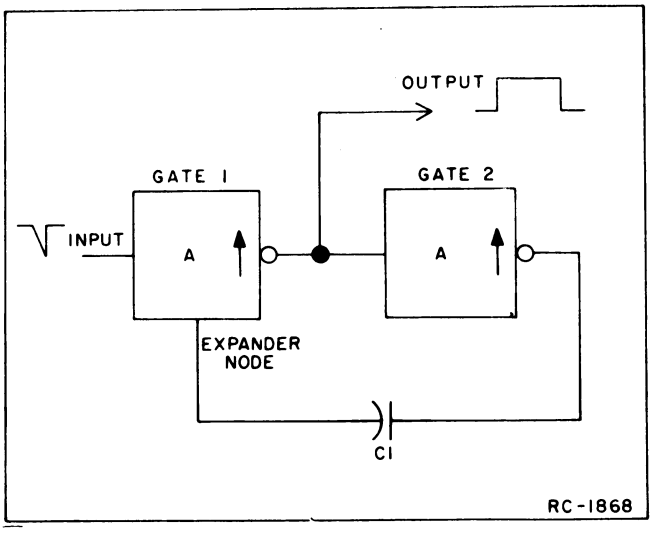


Figure 11 - NAND Gate One-Shot

NAND Gate One-Shot

Two NAND gates may be connected as shown in Figure 11 to provide virtually the same function as a conventional "one-shot" multivibrator. One of the NAND gates is required to have a direct input (called an expander node).

Assume that the inputs to Gate 1 are positive, making the output near ground potential. This ground is applied to the input of Gate 2, making its output positive so that C1 charges. Applying a negative-going pulse to the input of Gate 1 causes its output to go positive. This positive output is applied to the input of Gate 2, causing its output to drop to ground, discharging capacitor C1. C1 starts charging through the circuitry in Gate 1, keeping the output of Gate 1 positive until the capacitor charges. When C1 is charged, both inputs to Gate 1 are positive, and the output drops to near ground potential. The output of the "one-shot" is a square wave whose pulse width is determined by the value of C1 and the resistance in NAND gate 1.

FLIP-FLOPS

Two NAND gates connected as shown in Figure 12 will provide the same logic functions as the conventional flip-flop (bistable multivibrator).

Assume that a positive potential is applied to all inputs. Momentarily grounding the cathode of CR4 turns off Q2, causing its collector voltage to rise to approximately +6 Volts. This turns on Q1, causing its collector voltage to drop to near ground potential, keeping Q2 turned off. The flip-flop will remain in this state until CR1 is grounded.

Usually, two or more of the flip-flops are connected in a "master-slave" configuration (one flip-flop driving the other) for additional flexibility. Terminal identification for the flip-flop is shown in Figure 13A. However, the flip-flops used in the PSLM are actually connected as shown in Figure 13B, with external connections from input terminal 3 to output terminal 5, and from input terminal 2 to input terminal 6. This leaves terminal 1 as the input terminal or "Trigger". A flip-flop connected in this manner (J-K connected) will change state each time a pulse is applied to the trigger (terminal 1).

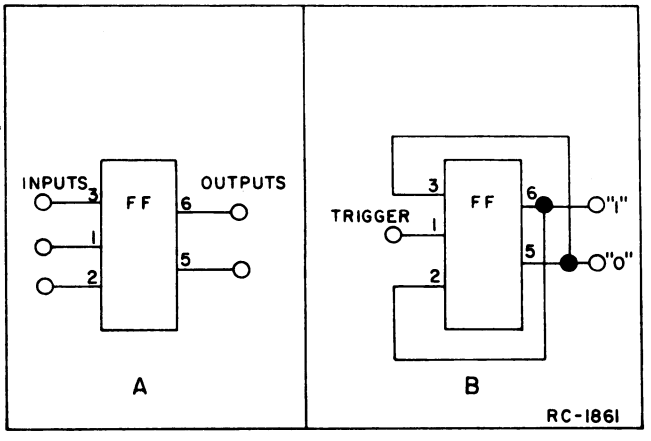


Figure 13 - Flip-Flop Terminal Identification

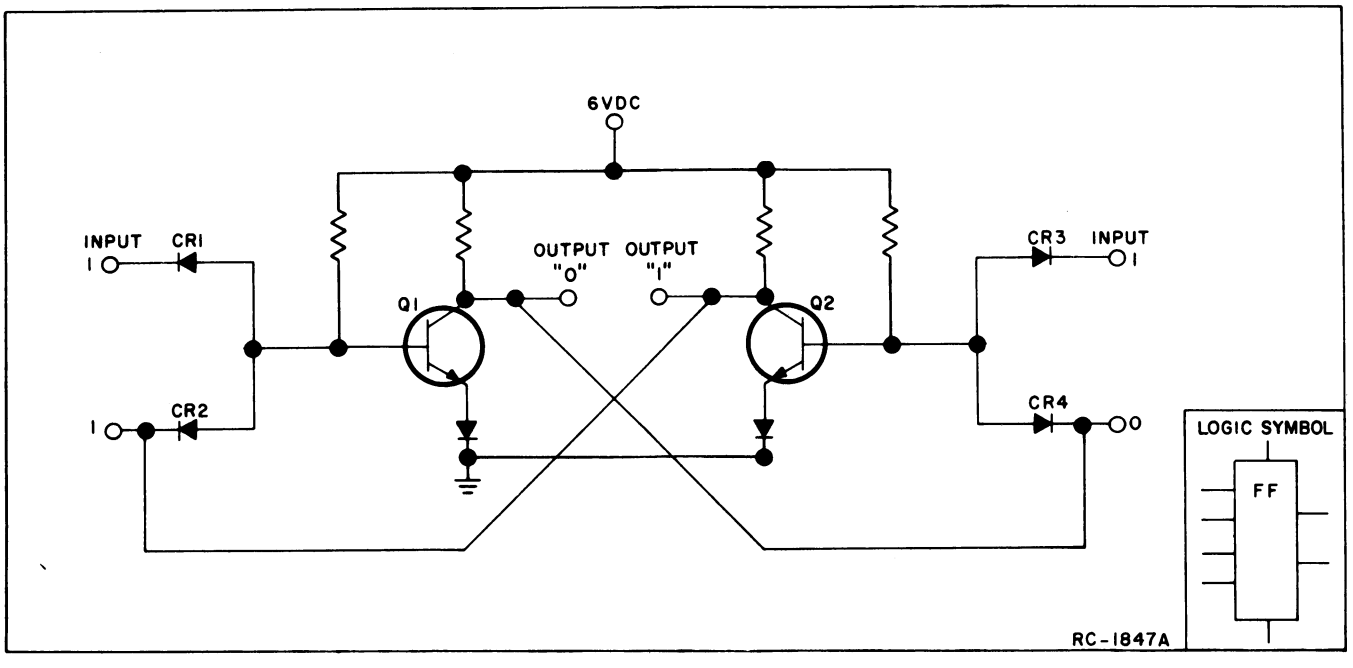


Figure 12 - NAND Gate Flip-Flop

For purposes of simplicity, supply and ground terminals (as well as any unused terminal) are not shown in the logic diagrams.

CIRCUIT ANALYSIS

The Priority Search-Lock Monitor is fully transistorized, using both discrete components and Integrated Circuit modules (IC's). Discrete components are used in the pulse generator, differentiator, driver, audio muting and squelch circuits. The IC's are used in the logic circuitry. Typical schematic and logic diagrams for the IC's are listed in the Table of Contents.

References to symbol numbers mentioned in the following texy may be found on the Outline Diagram, Schematic Diagram and Parts List (see Table of Contents).

Supply voltage for the PSLM is provided by the mobile or station 10-Volt regulator. +10 Volts is required for operating the discrete transistor stages. The IC's are supplied by the output of the 5.4-Volt regulator circuit composed of C4, CR2, and R7.

MASTER PULSE GENERATOR

The heart of the PSLM is the Master Pulse Generator. The pulse generator consists of unijunction transistor Q1, resistors R1 through R4 and capacitor C1. When power is applied to the circuit, C1 charges up and causes Q1 to conduct (emitter to base-1). This quickly discharges C1, causing Q1 to stop conducting until C1 charges up again through R1 and R2. This cycle is repeated as long as power is applied to the circuit, and provides a positive output pulse every 125 milliseconds (8 Hz). This output is applied to two different IC's to provide the timing pulses required for the different modes of operation. The PSLM sample rates and times discussed in the different modes of operation were selected to assure the reception of the first syllable of a message received on either channel, and to assure full intelligibility of messages received on the non-priority channel.

MODES OF OPERATION

Operation of the PSLM can be divided into three different modes. The three modes are:

- Received squelched
- Receiving priority channel
- Receiving non-priority channel

RECEIVER SQUELCHED

When the receiver is squelched (no signal applied), the PSLM alternately monitors each channel four times per second for a duration of 125 milliseconds. IC output timing waveforms for this mode of operation are shown in Figure 14.

The base of Inverter Q14 is tied to the Mon-Lock input (collector of DC amplifier Q9 in the MASTR Receiver). When the receiver is squelched, approximately 8.5 Volts are applied to the base of Q14, keeping the transistor turned off. When turned off, the emitter of Q14 is at a positive potential (or "1") which is continuously applied to terminal 9 of NAND Gate 1.

When a positive pulse from Master Pulse Generator Q1 is applied to terminal 10, the "1" at both inputs causes output terminal 8 to drop to "0", triggering the Channel Flip-Flop. The flip-flop is triggered every 125 milliseconds by the pulse generator, which alternately turns on the F1 and F2 Drivers, applying +10 Volts to the receiver oscillators. The PSLM will continue switching until a signal unsquelches the receiver.

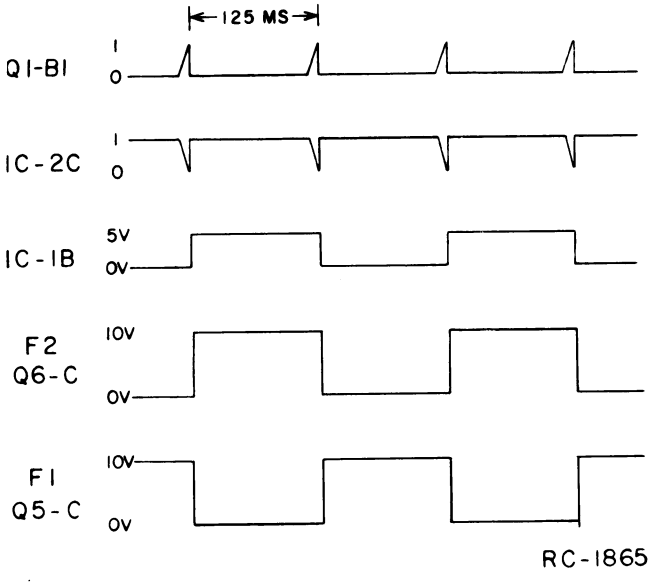


Figure 14 - Receiver Squelched Waveforms

RECEIVING PRIORITY CHANNEL

When a signal is received on the priority channel, the PSLM locks on that channel for the duration of the message. IC output timing waveforms for this mode of operation are shown in Figure 15

Assume that F1 is the priority channel. Receiving a signal on the F1 channel unsquelches the receiver and grounds the base of Inverter Q14, turning it on. When turned

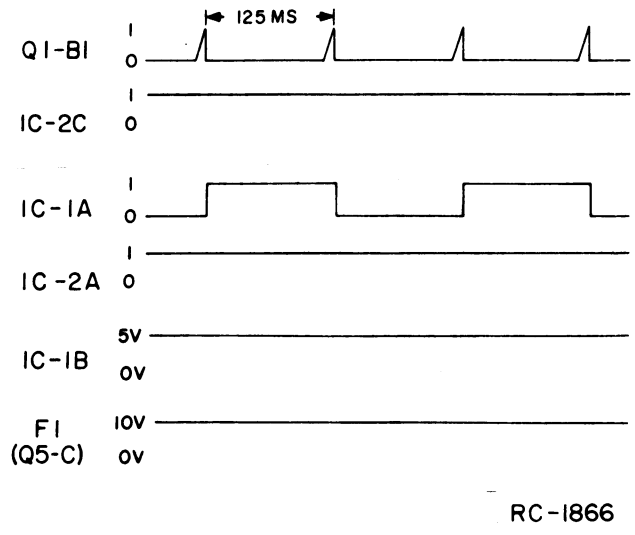


Figure 15 - Priority Channel Waveforms

on, the emitter of Q14 drops to ground potential, applying a "0" to terminal 9 of Gate 1, resulting in a "1" at output terminal 8. The output will remain a "1" as long as a "0" is applied to the input. This blocks the Master Pulse Generator output and prevents the Channel Flip-Flop from being triggered.

The "0" at terminal 6 of the Channel Flip-Flop keeps F1 Driver Q5 turned on, applying +10 Volts to the F1 receiver oscillator.

The Master Pulse Generator output also drives the Divider Flip-Flop, whose output is applied to the input of Gate 2. When a signal is received on the priority channel, the output of the Priority Selector/Identifier Gates (gates 4, 5 and 6) blocks Gate 2, preventing the timing pulses from being applied to the IC's and triggering the Channel Flip-Flop.

When F1 is the priority channel, +10 Volts is continuously applied to F1 Priority Jack J3. This results in a "1" at terminal 2 of Gate 4. The "0" at terminal 6 of the Channel Flip-Flop is applied to terminal 1 of Gate 4, resulting in a "1" output to Gate 6.

Applying a "1" to both inputs of Gate 6 results in a "0" at the output. This "0" is applied to the input of Gate 2, blocking the gate.

With Gates 1 and 2 blocked, the PSLM remains locked on the F1 channel until the message is completed (receiver squelches).

RECEIVING NON-PRIORITY CHANNEL

When a signal is received on the non-priority channel, the PSLM stops on that

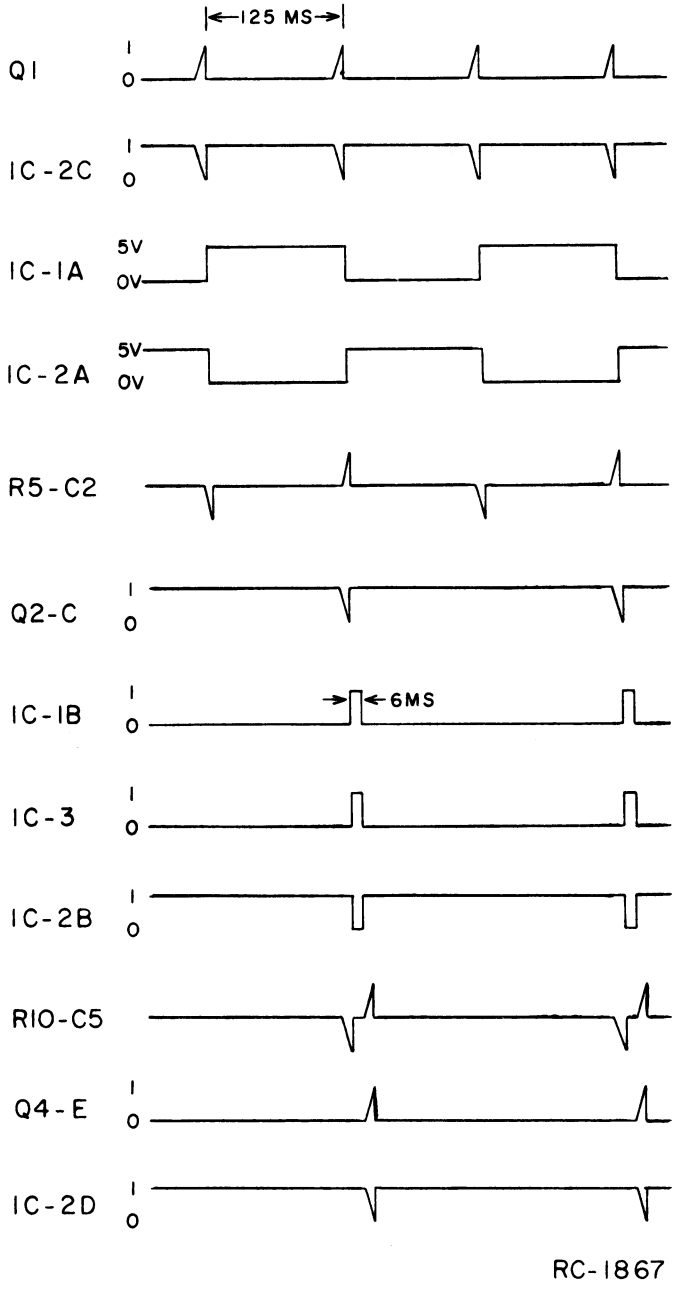


Figure 16 - Non-Priority Channel Waveforms

channel while monitoring the priority channel four times per second for a duration of six milliseconds. If a signal is received on the priority channel while receiving the non-priority channel, the PSLM will revert from the non-priority channel and lock on the priority channel for the duration of the message. IC output timing waveforms for this mode of operation are shown in Figure 16.

Assume that F2 is the non-priority channel. Receiving a signal on the F2 channel turns on Inverter Q14. This blocks Gate 1 and the Channel Flip-Flop turns on

the F2 Driver, applying +10 Volts to the F2 receiver oscillator.

On the non-priority channel, +10 Volts is not applied to the F2 Priority jack (J2) so that both inputs to Gate 5 are "0", resulting in a "1" output to Gate 6. With the Channel Flip-Flop stopped on the F2 channel, both inputs to Gate 4 are "1"s, resulting in a "0" output to Gate 6.

Applying a "1" and a "0" to the inputs of Gate 6 results in a "1" at the output. The "1" output does not disable Gate 2, so that the timing pulses from the Master Pulse Generator are passed to Differentiator Q2.

The output of Gate 2 is differentiated by C2 and R5 (see Figure 16), and the pulses are applied to the base of Q2. As Q2 is an NPN transistor, only the positive pulses (applied every 250 milliseconds) causes the transistor to conduct. When Q2 conducts, the negative-going output pulse at its collector forward biases CR1 and switches the Channel Flip-Flop to the priority channel. The output of Q2 also activates One-Shot Time Delay IC3, which provides a six-millisecond positive output pulse. The output pulse is simultaneously applied to the audio muting circuit and to Inverter IC-2B.

In the audio muting circuit, audio and noise from the emitter of audio-noise amplifier Q5 on the MASTR receiver is connected to J8 on the PSLM board. The audio is normally coupled through C8, R20, C7 and Emitter-Follower Q9, and then connected from J7 to volume high in the mobile or station combination.

The positive pulse from the One-Shot turns on Q7 and then Q8 for a total time of eight milliseconds. When turned on, the collectors of Q7 and Q8 drop to ground potential, shunting the receiver audio path. This prevents an objectionable noise burst from being heard at the speaker each time the priority channel is monitored (every 250 milliseconds).

At the same time the audio is muted, the output of the One-Shot is inverted and applied to the Squelch Muting Transistor Q10 and to Differentiator Q4.

The fast squelch circuit consists of Q10 through Q13. When the priority channel is not being monitored, audio and noise applied to the fast squelch circuit is shunted to ground by normally-on transistor Q10. When the Channel Flip-Flop is switched to the priority channel, the negative-going six millisecond inverter output is applied to the base of Q10, turning the transistor off. While Q10 is turned off, the noise output of the active high-pass noise filter is applied to the base of Noise Amplifier Q12. The filter consists of C9, C10, C12, R25, R26, Squelch Adjust potentiometer R29, and Q11. Instructions for setting R29 are listed in the Table of Contents.

The output of Q12 is rectified by CR7 and CR8, and the resultant negative voltage turns off DC Switch Q13. Turning off Q13 removes the "0" at the input of Gate 3, unlocking the gate.

While Q13 is turned off, the output of Inverter IC-2B is differentiated by C5 and R10 (see Figure 16), and the positive-going pulse turns off PNP transistor Q4. Turning off Q4 applied a "1" to the remaining input of Gate 3, switching the output to a "0". The "0" triggers the Channel Flip-Flop, causing it to switch back to the non-priority channel. The entire cycle is repeated every 250 milliseconds until a signal is received on the priority channel.

If a signal is received on the priority channel during the six millisecond monitor period, the signal quiets the receiver. With the receiver quieted, there is insufficient noise to operate the fast squelch circuit so that Q13 remains on (its collector at ground potential). The "0" at the collector of Q13 blocks Gate 3, while the output of the Priority Selector/Identifier Gates blocks Gate 2. With both gates blocked, the Channel Flip-Flop remains locked on the priority channel for the duration of the signal.

MAINTENANCE

DISASSEMBLY

To gain access to the PSLM board in mobile combinations, remove the four screws in the back cover and remove the cover.

In station combinations, the PSLM board is mounted on the rear of transmitter-receiver power supply Type EP-38-A, adjacent to power transformer T501.

TROUBLESHOOTING

Procedures for troubleshooting the PSLM include DC voltage readings and waveforms. Refer to the Troubleshooting Procedure as listed in the Table of Contents.

SYSTEM MODIFICATION

The following modifications are required in MASTR mobile and station combinations when the Priority Search-Lock Monitor options are installed. The modifications include changes in the system wiring, and changes to receivers equipped with standard crystal oscillators (non-ICOM) to reduce the oscillator starting time. For mobile options 7027 and 7028, additional changes to the control units and PSLM board are required to bypass the frequency selector switch and lock the priority on the F1 channel.

MOBILE SYSTEM CHANGES

1. Removed the White-Orange-Brown wire connected from P703-16 to P443-5 (Volume Hi).

2. Removed the jumper connected from TB901-1 to TB901-4.

3. When using Control Unit Models 4EC59A80 and 4EC59A82:

Added White COS lead from J443-19 to P703-3.

When using Control Unit Models 4EC59A99 through 4EC59A102:

Added White MON-LOCK lead from J443-20 to P703-3.

STATION SYSTEM CHANGES

In stations, disconnect the Red wire from R511-3 on power supply EP-38-A, and connect the Red wire to the W-BK-R wire going to J8 of the PSLM board. Make other cable connections as directed on the Outline Diagram.

For station power supplies EP-38-A equipped with line amplifier models 4EA24A12 & 13, replace R4 on the line amplifier board with a 510-ohm, ±5%, 1/2-watt resistor (GE Part No. 3R77P511J).

For stations with a Pro 72 base station control shelf, replace R10/R72 on remote audio board 19D416667G3 & 4 with R1701, a 200-ohm, 5%,1/4-watt resistor (GE Part No. 3R152P201J).

RECEIVER CHANGES

1. On all receiver and Dual Front End oscillator boards: removed C5 (and C6 on two-frequency oscillators), and replaced C17 (and C18 on two-frequency oscillators) with 7 pF, NPO ceramic capacitors (GE Part No. 19C300685-P95).

2. On 450-470 MHz receivers and DFE's, also removed RT9 and C43.

OPTION 7027 & 7028 CHANGES

1. On the mobile control unit, removed the White-Yellow-Red wire from frequency selector switch S704-2S, and added a jumper from S704-1S to -2S.

2. On the PSLM board, moved the White-Yellow-Green wire from J2 to J4.

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WORLD HEADQUARTERS • LYNCHBURG, VIRGINIA 24502 U.S.A.

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PRIORITY SQUELCH ADJUSTMENT

Priority Squelch Adjust R29 was set at the factory for 20-dB quieting sensitivity on the priority channel, and will normally require no further adjustment. If it should become necessary to set R29, use one of the following procedures. Each procedure requires a signal generator (M560 or equivalent) with a 6-dB pad.

PROCEDURE A

Before starting Procedure A, make sure that the receiver is properly aligned with the PSLM disabled (SEARCH-OFF switch in the OFF position). Then measure and record the F1 20-dB quieting sensitivity.

1. In mobile combinations, place the frequency selector switch in the F1 (priority) position, and the SEARCH-OFF switch in the SEARCH position.

In local and local/remote stations, place the frequency selector switch in the F1-F2 position.

In remote control stations, make sure that the R-F1 and R-F2 pushbuttons at the remote control console are both pressed in (or both are out).

2. Alternately squelch and unsquelch the receiver until the PSLM stops on the F2 (or non-priority) channel. The PSLM searches when the receiver is squelched, and may lock on either channel when the receiver is unsquelched. Therefore, several attempts may be required to stop the PSLM on the F2 channel. Make sure that the PSLM is stopped on the F2 channel by checking the light on the mobile control unit, or by checking for +10 volts across J6 (Rec F2) and J9 (system negative) on the PSLM board.

3. Next, apply a signal on the F1 (or priority) channel from the signal generator. Then slowly increase the signal generator output until the receiver switches to the F1 channel. This should be at the 20-dB quieting level as measured previously.

4. If necessary, adjust Priority Squelch Control R29 until the PSLM switches channels at the 20-dB level.

PROCEDURE B

1. In mobile combinations, place the frequency selector switch in the F1 (priority) position, and the SEARCH-OFF switch in the SEARCH position.

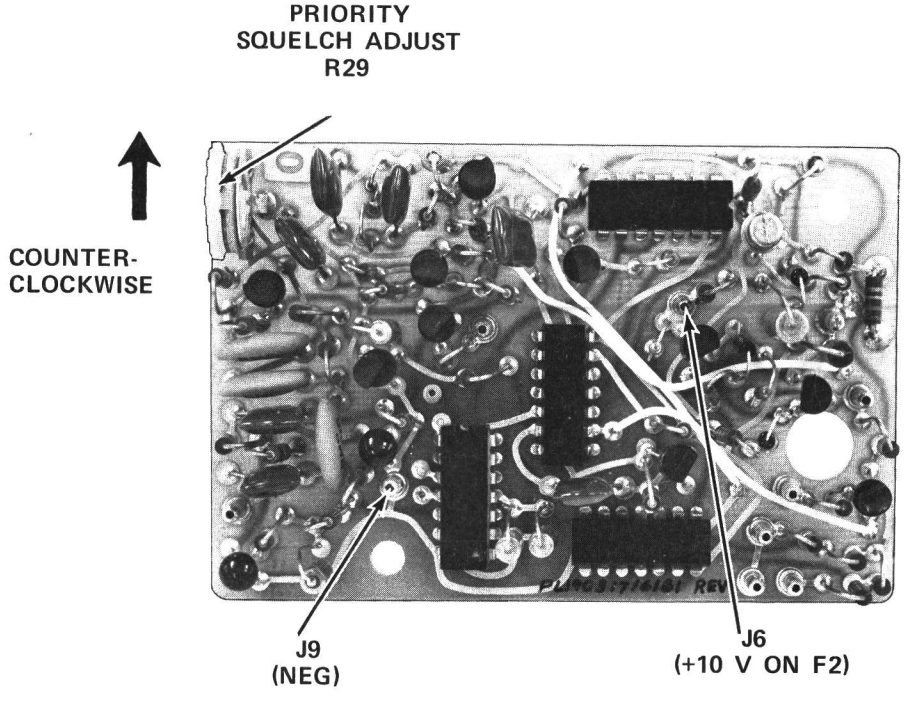
In local and local/remote stations, place the frequency selector switch in the F1-F2 position.

In remote control stations, make sure that the R-F1 and R-F2 pushbuttons at the remote control console are both pressed in (or both are out).

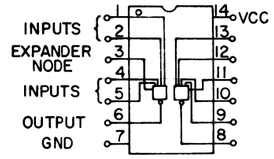
2. With the receiver squelched, apply a 100-microvolt signal on the F2 (non-priority) channel.

3. Turn R29 fully counterclockwise, causing the receiver to false (a repeated thumping noise is heard in the speaker).

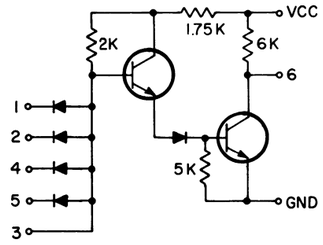
4. Carefully turn R29 clockwise until falsing stops. Then continue turning R29 clockwise for an additional 15 to 20% of rotation.



DUAL 4-INPUT GATES
19A115913-P1

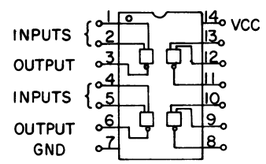


LOGIC DIAGRAM

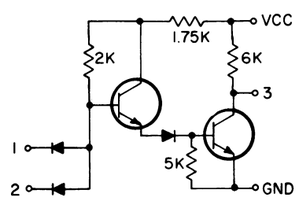


TYPICAL SCHEMATIC DIAGRAM
(ONE GATE ONLY)

QUADRUPLE 2-INPUT GATES
19A115913-P7



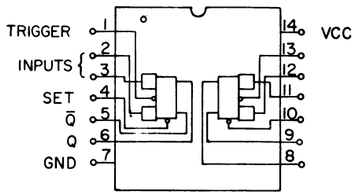
LOGIC DIAGRAM



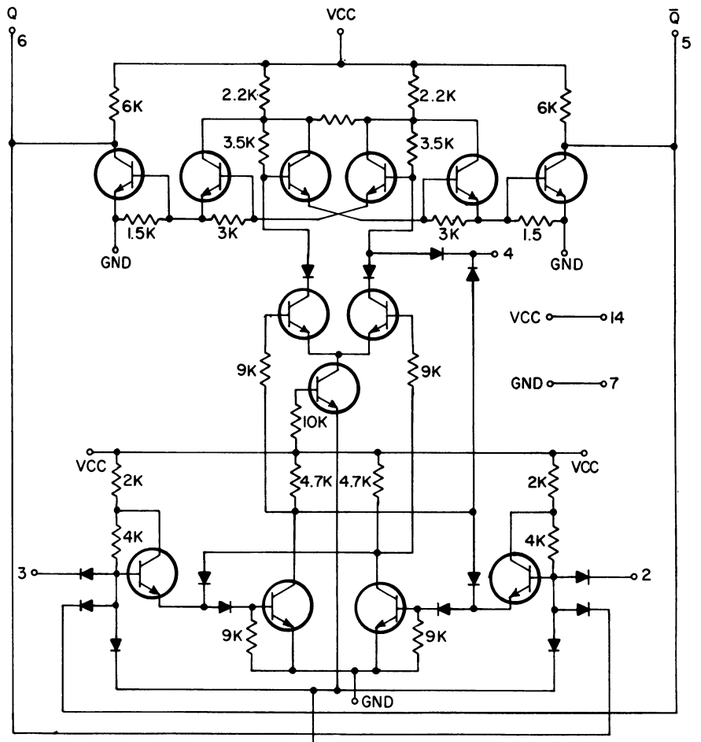
TYPICAL SCHEMATIC DIAGRAM
(ONE GATE ONLY)

RC-1873

MASTER-SLAVE FLIP-FLOP
19A115913-P10



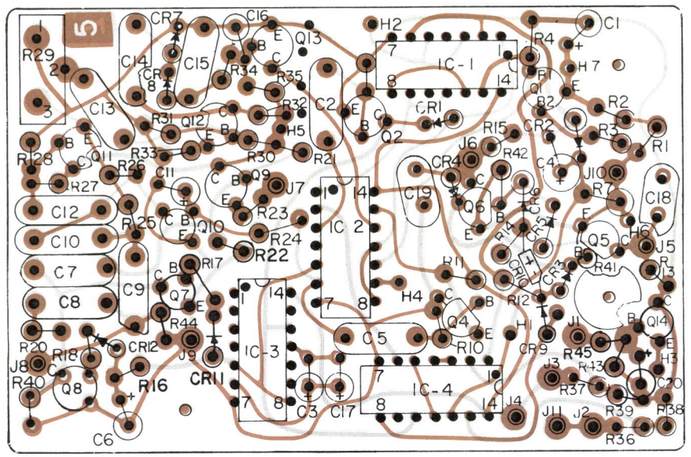
LOGIC DIAGRAM



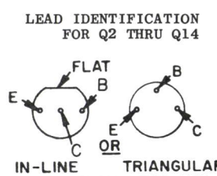
TYPICAL SCHEMATIC DIAGRAM
(ONE FLIP-FLOP ONLY)

LOGIC & SCHEMATIC DIAGRAMS

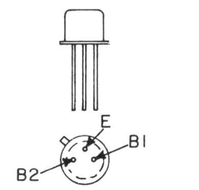
FOR INTERGRATED CIRCUIT MODULES
PRIORITY SEARCH-LOCK MONITOR



LEAD IDENTIFICATION
FOR Q2 THRU Q14

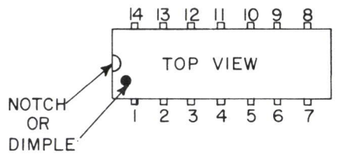


NOTE: LEAD ARRANGEMENT, AND NOT CASE SHAPE, IS DETERMINING FACTOR FOR LEAD IDENTIFICATION.

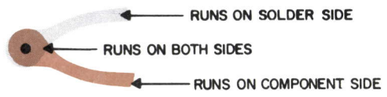


LEAD IDENTIFICATION
FOR Q1

INTEGRATED CIRCUIT
LEAD IDENTIFICATION



(19C317320, Rev. 4)
(19B216562, Sh. 1, Rev. 5)
(19B216562, Sh. 2, Rev. 7)



OUTLINE DIAGRAM

PRIORITY SEARCH-LOCK MONITOR

CONNECTIONS CHART

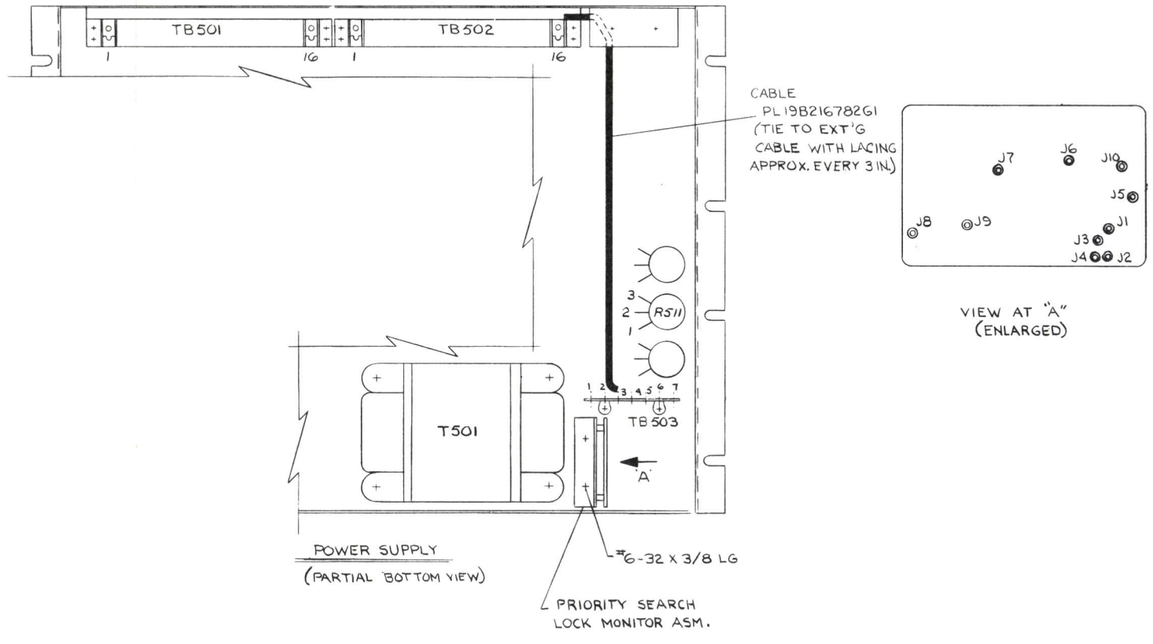
MOBILE			STATIONS			
FROM PSLM BOARD	WIRE COLOR	CONNECT TO	FROM PSLM BOARD	WIRE COLOR	CONNECT TO 4EP38A10,11	CONNECT TO 4EP38A12
J1	W-O-R	P443-20	J1	W-G-BL	TB8-2	TB503-4
J2	W-Y-G	P443-9	J4	W-BL-O	TB502-7	TB502-7
J3	W-Y-O	P443-8	J5	W-O-R	TB502-9	TB502-9
J4	(SEE NOTE 1)		J6	W-G-O	TB502-8	TB502-8
J5	W-Y-BR	P443-6	J7	W	TB502-2	TB502-2
J6	W-Y-R	P443-7	J8	W-BK-R	P443-5 *	P443-5 *
J7	W-O-BR	P703-16	J9	BK-W	TB501-11	TB501-11
J8	W-R-BL	P443-5	J10	BL	TB501-7	TB501-7
J9	W-O	P443-13	J11	(SEE NOTE 2)		
J10	W-R	P443-12				
J11	(SEE NOTE 1)					

RC-1871B

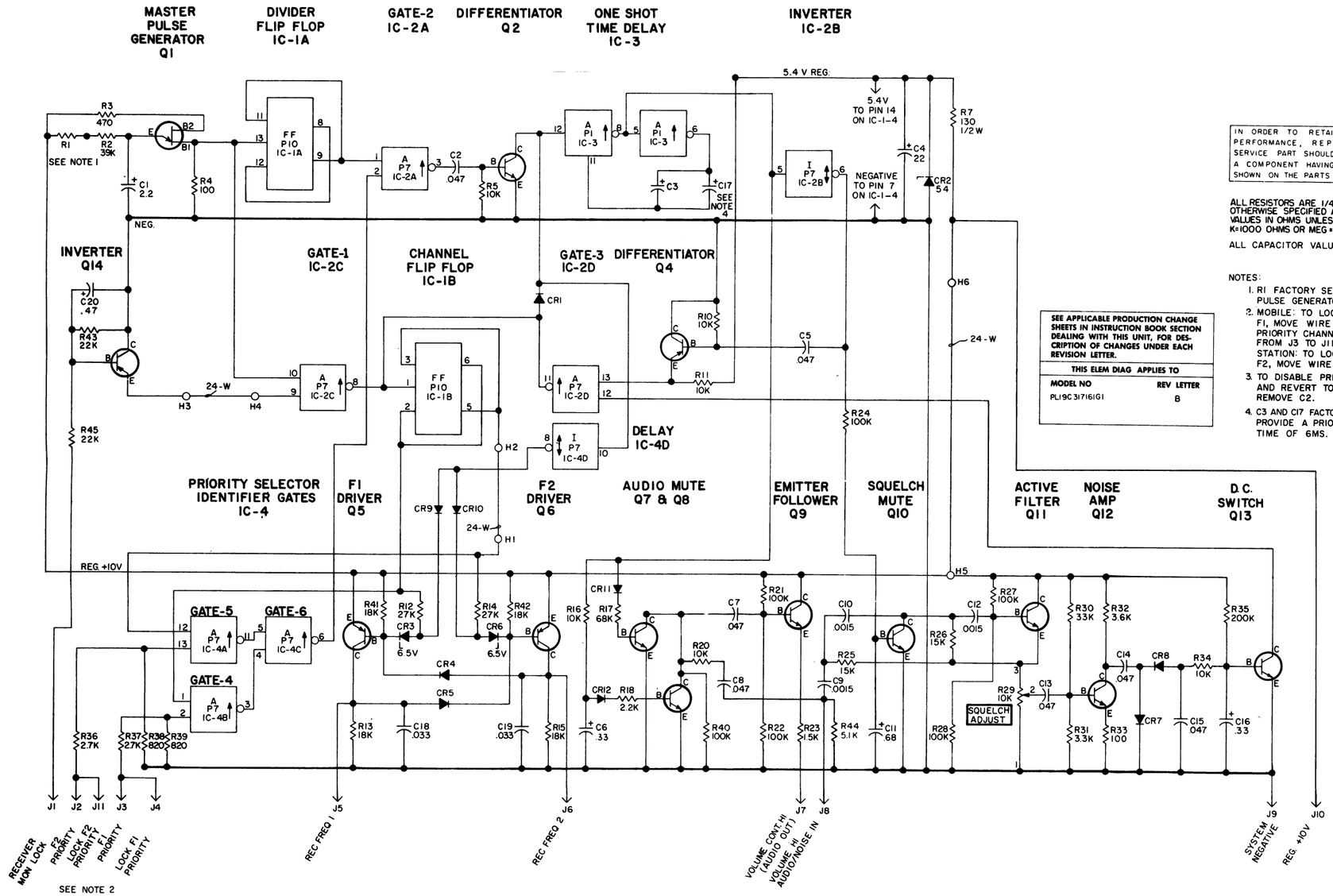
NOTE 1. TO LOCK PRIORITY CHANNEL ON F1, MOVE W-Y-G WIRE FROM J2 TO J4. TO LOCK PRIORITY CHANNEL ON F2, MOVE W-Y-O WIRE FROM J3 TO J11.

NOTE 2. TO LOCK PRIORITY CHANNEL ON F2, MOVE W-BL-O WIRE FROM J4 TO J11.

* W-BK-R WIRE CONNECTS TO RED WIRE REMOVED FROM R511-3.



(19C317305, Sh. 2, Rev. 3)



IN ORDER TO RETAIN RATED EQUIPMENT PERFORMANCE, REPLACEMENT OF ANY SERVICE PART SHOULD BE MADE ONLY WITH A COMPONENT HAVING THE SPECIFICATIONS SHOWN ON THE PARTS LIST FOR THAT PART.

ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY K=1000 OHMS OR MEG=1,000,000 OHMS.

ALL CAPACITOR VALUES IN UF

NOTES:

1. R1 FACTORY SELECTED TO SET MASTER PULSE GENERATOR OUTPUT RATE AT 8HZ.
2. MOBILE: TO LOCK PRIORITY CHANNEL ON F1, MOVE WIRE FROM J2 TO J4. TO LOCK PRIORITY CHANNEL ON F2 MOVE WIRE FROM J3 TO J11.
   STATION: TO LOCK PRIORITY CHANNEL ON F2, MOVE WIRE FROM J4 TO J11.
3. TO DISABLE PRIORITY FUNCTION OF PSLM AND REVERT TO SEARCH LOCK MONITOR, REMOVE C2.
4. C3 AND C17 FACTORY SELECTED (IF REQUIRED) TO PROVIDE A PRIORITY CHANNEL SAMPLE TIME OF 6MS.

SEE APPLICABLE PRODUCTION CHANGE SHEETS IN INSTRUCTION BOOK SECTION DEALING WITH THIS UNIT, FOR DESCRIPTION OF CHANGES UNDER EACH REVISION LETTER.

THIS ELEM DIAG APPLIES TO	
MODEL NO	REV LETTER
PLI9C317161G1	B

(19D413287, Rev. 8)

SCHEMATIC DIAGRAM

PRIORITY SEARCH-LOCK MONITOR

PARTS LIST

LBI-4055E

PRIORITY SEARCH LOCK MONITOR
19A127557G1 (MOBILE)
19A127679G1 (STATION)

SYMBOL	GE PART NO.	DESCRIPTION
		COMPONENT BOARD 19C317161G1 REV B
		- - - - - - - - - CAPACITORS - - - - - - - - -
C1	5496267P213	Tantalum: 2.2 µf ±10%, 20 VDCW; sim to Sprague Type 150D.
C2	19A116080P5	Polyester: 0.047 µf ±20%, 50 VDCW.
C3A	5496267P417	Tantalum: 1.0 µf ±5%, 35 VDCW; sim to Sprague Type 150D.
C3B	19B200240P15	Tantalum: 1.8 µf ±5%, 20 VDCW.
C3C	5496267P413	Tantalum: 2.2 µf ±5%, 20 VDCW; sim to Sprague Type 150D.
C4	5496267P10	Tantalum: 22 µf ±20%, 15 VDCW; sim to Sprague Type 150D.
C5	19A116080P5	Polyester: 0.047 µf ±20%, 50 VDCW.
C6*	5496267P227	Tantalum: 0.33 µf ±10%, 35 VDCW; sim to Sprague Type 150D.
		In REV A and earlier:
	5496267P228	Tantalum: 0.47 µf ±10%, 35 VDCW; sim to Sprague Type 150D.
C7 and C8	19A116080P5	Polyester: 0.047 µf ±20%, 50 VDCW.
C9 and C10	5494481P124	Ceramic disc: 1500 pf ±10%, 1000 VDCW; sim to RMC Type JF Discap.
C11	5496267P29	Tantalum: 0.68 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C12	5494481P124	Ceramic disc: 1500 pf ±10%, 1000 VDCW; sim to RMC Type JF Discap.
C13 thru C15	19A116080P5	Polyester: 0.047 µf ±20%, 50 VDCW.
C16	5496267P27	Tantalum: 0.33 µf ±20%, 35 VDCW; sim to Sprague Type 150D. NOTE: The value of C17 (if required) is selected to provide a priority channel sample time of 6 milliseconds.
C17A	5496267P227	Tantalum: 0.33 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C17B	5496267P228	Tantalum: 0.47 µf ±10%, 35 VDCW; sim to Sprague Type 150D.
C17C	5496267P229	Tantalum: 0.68 µf ±10%, 35 VDCW; sim to Sprague Type 150D.
C17D	5496267P230	Tantalum: 0.82 µf ±10%, 35 VDCW; sim to Sprague Type 150D.
C17E	5496267P217	Tantalum: 1.0 µf ±10%, 35 VDCW; sim to Sprague Type 150D.
C17F	5496267P226	Tantalum: 0.22 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C17G	5496267P224	Tantalum: 0.1 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C18 and C19	19A116080P4	Polyester: 0.033 µf ±20%, 50 VDCW.
C20*	5496267P228	Tantalum: 0.47 µf ±10%, 35 VDCW; sim to Sprague Type 150D. Added by REV A.
		- - - - - - - DIODES AND RECTIFIERS - - - - - -
CR1	4038056P1	Germanium.
CR2	4036887P5	Silicon, Zener.
CR3*	4036887P48	Silicon, Zener.
		Earlier than REV A:
	4036887P6	Silicon, Zener.
CR4 and CR5	19A115250P1	Silicon.
CR6*	4036887P48	Silicon, Zener.
		Earlier than REV A:
	4036887P6	Silicon, Zener.
CR7 thru CR12	19A115250P1	Silicon.
		- - - - - - - INTEGRATED CIRCUITS - - - - - -
IC1	19A115913P10	Monolithic, Dual 945 Flip-Flop; sim to Fairchild DTL 093.
IC2	19A115913P7	Monolithic, Quad 2-Input Gate; sim to Fairchild DTL 946.
IC3	19A115913P1	Monolithic, Dual 4-Input Gate; sim to Fairchild DTL 930.
IC4	19A115913P7	Monolithic, Quad 2-Input Gate; sim to Fairchild DTL 946.
		- - - - - - - JACKS AND RECEPTACLES - - - - - -
J1 thru J11	4033513P4	Contact, electrical: sim to Bead Chain L93-3.
		- - - - - - - - - TRANSISTORS - - - - - - - - -
Q1	19A115364P1	Unijunction: N Type, sim to 2N2656.
Q2	19A115123P1	Silicon, NPN.
Q3*	19A115123P1	Silicon, NPN. Deleted by REV A.
Q4 thru Q6	19A115768P1	Silicon, PNP; sim to Type 2N3702.
Q7 and Q8	19A115362P1	Silicon, NPN; sim to Type 2N2925.
Q9 thru Q11	19A115123P1	Silicon, NPN.
Q12*	19A115362P1	Silicon, NPN; sim to Type 2N2925.
		In REV A and earlier:
	19A115123P1	Silicon, NPN.
Q13	19A115123P1	Silicon, NPN.
Q14*	19A115768P1	Silcion, PNP; sim to Type 2N3702. Added by REV A.
		NOTE: The value of R1 is selected to provide a Master Pulse Generator output of 8 Hz.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1A	3R152P432J	Composition: 4300 ohms ±5%, 1/4 w.
R1B	3R152P822J	Composition: 8200 ohms ±5%, 1/4 w.
R1C	3R152P123J	Composition: 12,000 ohms ±5%, 1/4 w.
R1D	3R152P163J	Composition: 16,000 ohms ±5%, 1/4 w.
R1E	3R152P203J	Composition: 20,000 ohms ±5%, 1/4 w.
R1F	3R152P243J	Composition: 24,000 ohms ±5%, 1/4 w.
R1G	3R152P273J	Composition: 27,000 ohms ±5%, 1/4 w.
R1H	3R152P303J	Composition: 30,000 ohms ±5%, 1/4 w.
R1I	3R152P333J	Composition: 33,000 ohms ±5%, 1/4 w.
R1J	3R152P363J	Composition: 36,000 ohms ±5%, 1/4 w.
R1K	3R152P393J	Composition: 39,000 ohms ±5%, 1/4 w.
R1L	3R152P433J	Composition: 43,000 ohms ±5%, 1/4 w.
R2	3R152P393J	Composition: 39,000 ohms ±5%, 1/4 w.
R3	3R152P471K	Composition: 470 ohms ±10%, 1/4 w.
R4	3R152P101K	Composition: 100 ohms ±10%, 1/4 w.
R5	3R152P103K	Composition: 10,000 ohms ±10%, 1/4 w.
R7	3R77P131J	Composition: 130 ohms ±5%, 1/2 w.
R8*	3R152P473K	Composition: 47,000 ohms ±10%, 1/4 w. Deleted by REV A.
R10 and R11	3R152P103K	Composition: 10,000 ohms ±10%, 1/4 w.
R12	3R152P273K	Composition: 27,000 ohms ±10%, 1/4 w.
R13	3R152P183K	Composition: 18,000 ohms ±10%, 1/4 w.
R14	3R152P273K	Composition: 27,000 ohms ±10%, 1/4 w.
R15	3R152P183K	Composition: 18,000 ohms ±10%, 1/4 w.
R16	3R152P103K	Composition: 10,000 ohms ±10%, 1/4 w.
R17	3R152P683K	Composition: 68,000 ohms ±10%, 1/4 w.
R18	3R152P222K	Composition: 2200 ohms ±10%, 1/4 w.
R20	3R152P103K	Composition: 10,000 ohms ±10%, 1/4 w.
R21 and R22	3R152P104K	Composition: 100,000 ohms ±10%, 1/4 w.
R23	3R152P152K	Composition: 1500 ohms ±10%, 1/4 w.
R24	3R152P104K	Composition: 100,000 ohms ±10%, 1/4 w.
R25 and R26	3R152P153K	Composition: 15,000 ohms ±10%, 1/4 w.
R27 and R28	3R152P104K	Composition: 100,000 ohms ±10%, 1/4 w.
R29	19B209358P106	Variable, carbon film: approx 75 to 10,000 ohms ±10%, 0.25 w; sim to CTS Type X-201.
R30	3R152333K	Composition: 33,000 ohms ±10%, 1/4 w.
R31	3R152P332K	Composition: 3300 ohms ±10%, 1/4 w.
R32	3R152P362J	Composition: 3600 ohms ±5%, 1/4 w.
R33*	3R152P101K	Composition: 100 ohms ±10%, 1/4 w.
		Earlier than REV A:
	3R152P271K	Composition: 270 ohms ±10%, 1/4 w.
R34	3R152P103K	Composition: 10,000 ohms ±10%, 1/4 w.
R35	3R152P204K	Composition: 200,000 ohms ±10%, 1/4 w.
R36 and R37	3R152P272J	Composition: 2700 ohms ±5%, 1/4 w.
R38 and R39	3R152P821J	Composition: 820 ohms ±5%, 1/4 w.
R40	3R152P104K	Composition: 100,000 ohms ±10%, 1/4 w.
R41 and R42	3R152P183K	Composition: 18,000 ohms ±10%, 1/4 w.
R43*	3R152P223K	Composition: 22,000 ohms ±10%, 1/4 w. Added by REV A.
R44*	3R152P512K	Composition: 5100 ohms ±10%, 1/4 w. Added by REV A.
R45*	3R152P223K	Composition: 22,000 ohms ±10%, 1/4 w. Added by REV A.
		MOBILE WIRING HARNESS 19C317190G1
		- - - - - - - - - MISCELLANEOUS - - - - - - -
	4029840P2	Contact, electrical: sim to Amphenol 42827-2.
		STATION WIRING HARNESS 19B216782G1
		- - - - - - - - - MISCELLANEOUS - - - - - - -
	4029840P2	Contact, electrical: sim to Amphenol 42827-2.
	19B209260P103	Terminal.
		RECEIVER OSCILLATOR MODIFICATION 19B216671G1
		- - - - - - - - - CAPACITORS - - - - - - - - -
C1 and C2	19C300685P95	Ceramic disc: 7 pf ±2%, 500 VDCW, temp coef 0 PPM.

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by these revisions.

REV. A - To make the PSLM compatible with Channel Guard:
Deleted Q3; changed R33 and CR6; and added C20, R43, R44, R45 and Q14. Also changed the control voltage at J1 from COS to MON-LOCK.

REV. B - To reduce the audio mute time.
Changed C6 and Q12.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

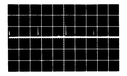
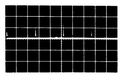
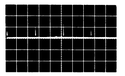
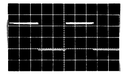
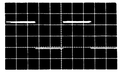
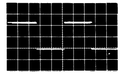
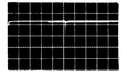
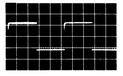
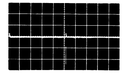
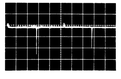
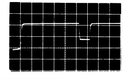
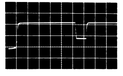
WAVEFORMS

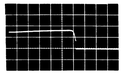
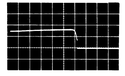
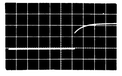
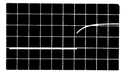
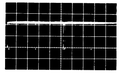
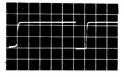
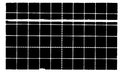
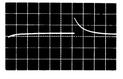
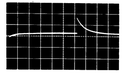
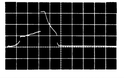
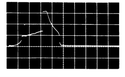
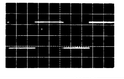
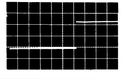
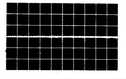
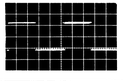
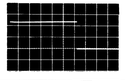
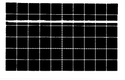
All waveforms are taken at Test Points (A) thru (T) as shown in Figures A and B, and are taken with the PSLM board connected for F1 priority (see note 2 of the Schematic Diagram). When applicable, the waveforms are shown for three different modes of operations as follows:

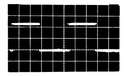
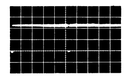
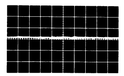
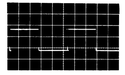
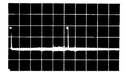
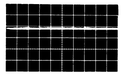
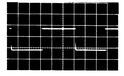
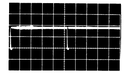
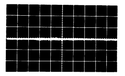
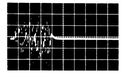
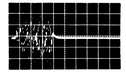
1. Receiver Squelched (PSLM Searching)
2. Receiver Unsquelched (Receiving Non-Priority Channel)
3. Receiver Unsquelched (Receiving Priority Channel)

NOTE

All waveforms are taken using Test Point E as the SYNC SOURCE (Trigger Pulse) except where NOTED.

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL	RECEIVING PRIORITY CHANNEL
(A)	 50ms/Div. 4V/Div. NOTE: INTERNAL SYNC	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC
(B)	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC
(C)	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC	 50ms/Div. 2V/Div.	
(D)	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div.	
(E)	 1ms/Div. 2V/Div.	 1ms/Div. 2V/Div.	

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL	RECEIVING PRIORITY CHANNEL
(F)	 1ms/Div. 2V/Div.	 1ms/Div. 2V/Div.	
(G)	 1ms/Div. 2V/Div.	 1ms/Div. 2V/Div.	
(H)	 50ms/Div. 2V/Div.	 1ms/Div. 2V/Div.	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC
(I)	 1ms/Div. 2V/Div.	 1ms/Div. 2V/Div.	
(J)	 2ms/Div. 0.5V/Div.	 2ms/Div. 0.5V/Div.	
(L)	 50ms/Div. 2V/Div.	 1ms/Div. 2V/Div.	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC
(M)	 50ms/Div. 2V/Div.	 1ms/Div. 2V/Div.	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL	RECEIVING PRIORITY CHANNEL
(N)	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC
(O)	 50ms/Div. 5V/Div.	 50ms/Div. 5V/Div.	 50ms/Div. 5V/Div. NOTE: INTERNAL SYNC
(P)	 50ms/Div. 5V/Div.	 50ms/Div. 5V/Div.	 50ms/Div. 5V/Div. NOTE: INTERNAL SYNC
(Q)	 2ms/Div. 0.2V/Div.	 2ms/Div. 0.2V/Div.	
(R)	2ms/Div. 0.2V/Div.	2ms/Div. 0.2V/Div.	
(S)	2ms/Div. 0.5V/Div.	2ms/Div. 0.5V/Div.	2ms/Div. 0.5V/Div. NOTE: INTERNAL SYNC
(T)	2ms/Div. 1V/Div.	2ms/Div. 1V/Div.	2ms/Div. 1V/Div. NOTE: INTERNAL SYNC