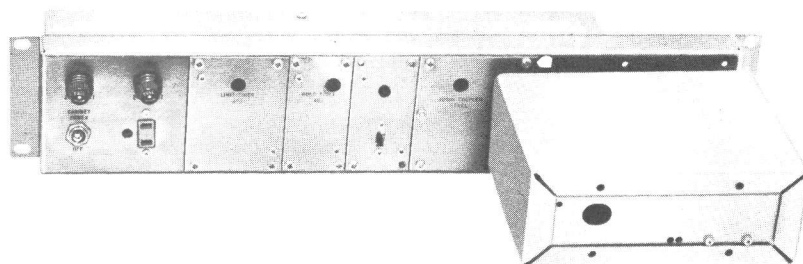


MASTR PROGRESS LINE

REPEATER CONTROL DIGITAL DECODER

MODELS 4EJ18D10-12 (Options 7736, 7737 & 7738)



SPECIFICATIONS *

<u>Model Number</u>	<u>Tone Input</u>	<u>MASTR Professional Option Number</u>
4EJ18D10	590 Hz	7736
4EJ18D11	1500 Hz	7737
4EJ18D12	2805 Hz	7738
Pulsing Speed	8 to 16 PPS (10 PPS Nominal)	
Input Impedance	3000 ohms minimum	
Audio Sensitivity		
590 & 1500 Hz	.02 to 6.0 volts at 10 dB SINAD	
2805 Hz	.02 to 6.0 volts at 14 dB SINAD	
Input Power	12.6 volts at 160 milliamperes (add 20 milliamperes for relay)	
Temperature Range	-30°C to +60°C	

*These specifications are intended primarily for the use of the serviceman. Refer to the appropriate Specification Sheet for the complete specifications.

TABLE OF CONTENTS

SPECIFICATIONS	Cover
DESCRIPTION	1
PRELIMINARY ADJUSTMENTS	1
LOGIC CIRCUITS	1
Solid State Switches	1
Gating Circuits	2
CIRCUIT ANALYSIS	7
Tone Receiver	7
Pulse Routing Board	9
External Control Relay	12
Counter Board	12
MAINTENANCE	13
Disassembly	13
Troubleshooting	13
Timer Control Modification	13
Tone Receiver Adjustment	13
CODE SETTING PROCEDURE	15
Four-Digit Codes	15
Three-Digit Codes	15
One-Digit Drop-Out	16
LOGIC & SCHEMATIC DIAGRAMS FOR INTEGRATED CIRCUITS	17
OUTLINE DIAGRAM	18
SCHEMATIC DIAGRAM	19
PARTS LIST	20
PRODUCTION CHANGES	20
TROUBLESHOOTING PROCEDURE	21
INTERCONNECTION DIAGRAM	22

WARNING

No one should be permitted to handle any portion of the equipment that is supplied with voltage; or to connect any external apparatus to the units while the units are supplied with power. KEEP AWAY FROM LIVE CIRCUITS.

DESCRIPTION

General Electric Digital Decoder Models 4EJ18D10-12 are transistorized, single-tone decoders for controlling the operation of MASTR repeater stations. The decoder assembly mounts on the front of the repeater panel in the option mounting area.

The decoder responds to a tone that is interrupted by a telephone-type dial to form a series of pulses corresponding to the digit dialed. The standard decoder is connected for Repeater Control. In this type of operation, dialing the "Repeater On" code enables the repeater (all timers operative). The repeater remains enabled until the "Repeater Off" code is dialed.

If desired, the decoder may be connected for Timer Control operation. In this type of operation dialing the "Repeater On" code enables the repeater. However, when the Drop-Out Delay Timer or 3-Minute Limit timer on the repeater panel cuts off the transmitter, it automatically disables the repeater. The "Repeater On" code must be dialed each time the repeater is enabled. Dialing the "Repeater Off" code overrides the Drop-Out Delay Timer and disables the repeater.

A relay may be added to the decoder assembly whenever additional external control functions are desired.

PRELIMINARY ADJUSTMENTS

The decoder is normally shipped from the factory set to operate on the following codes:

- Repeater On: 5-9-5-5
- Repeater Off: 5-9-5-6

Before placing the decoder into operation, new code assignments and new code settings are normally required. Complete instructions for setting three- and four-digit codes, as well as a one-digit repeater drop-out code are contained in the Code Setting Procedure. Instructions are also provided for connecting the decoder for Timer Control operation (see Table of Contents).

LOGIC CIRCUITS

This section contains a detailed description of all of the logic circuits used

in the decoder. It is suggested that the serviceman study the following information carefully, as a good understanding of the basic decoder circuitry is essential for servicing the decoder.

SOLID STATE SWITCHES

An ideal switch has infinite resistance when open and zero resistance when closed. The transistor and semiconductor diode can be made to approach these conditions while operating at a much higher rate than conventional switches. Logic circuits are primarily switching devices which are either in a state of full conduction (saturated) or turned off. These devices can be switched from one state to the other as rapidly as required by the circuit function.

DIODE SWITCH (Figure 1)

A semiconductor diode presents maximum resistance to the circuit when the diode is reversed biased or there is no difference of potential between the cathode or anode. Applying a negative potential to the cathode of the diode (with respect to the anode), or a positive potential (with respect to the cathode) to the anode of sufficient amplitude to overcome the series resistance of the diode, forward biases the diode causing it to conduct. The diode now switches from maximum to minimum resistance.

The resulting current flow in the diode circuit increases from near zero to the maximum value allowed by the amplitude of the switching voltage and the series resistance of the circuit.

TRANSISTOR SWITCH & INVERTER (Figure 2)

The high value of "off" resistance and the low value of "on" resistance make the transistor invaluable for switching applications. When no base current is applied to the transistor switch shown in Figure 2, and the collector has the proper voltage applied, the open-circuit resistance of the transistor approaches several megohms. If sufficient base current is suddenly applied to drive the transistor into saturation (turned ON), the collector-emitter resistance will drop to as low as 1.0 ohm. Voltage across the transistor under these conditions may be only a few tenths of a volt.

The transistor stage shown in Figure 2 can also be used as an inverter for reversing the polarity of the input signal. A positive signal applied to the base-emitter junction will cause the collector voltage to drop from +6 volts to near ground potential.

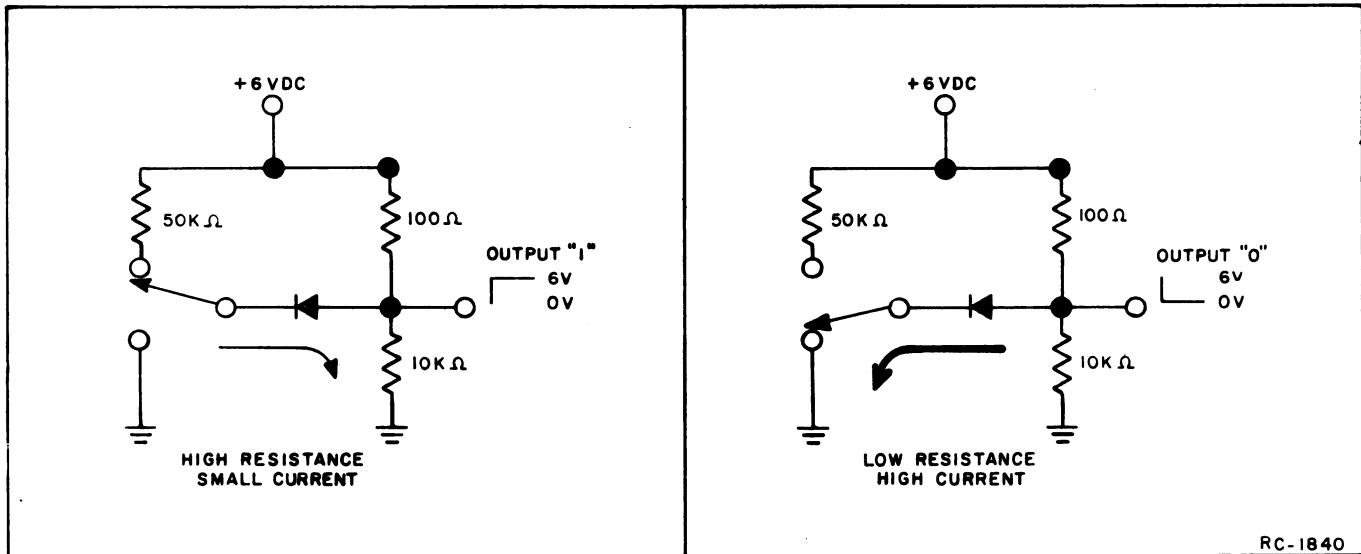


Figure 1 - Diode Switching Circuit

closed. By representing the closed state of a switch or gate as "1" and the open state of a switch or gate as "0", then all possible conditions for the AND gate are shown in the Truth Table in Figure 3.

In Figure 4, if point "C" is to be made equal to potential V, either switch

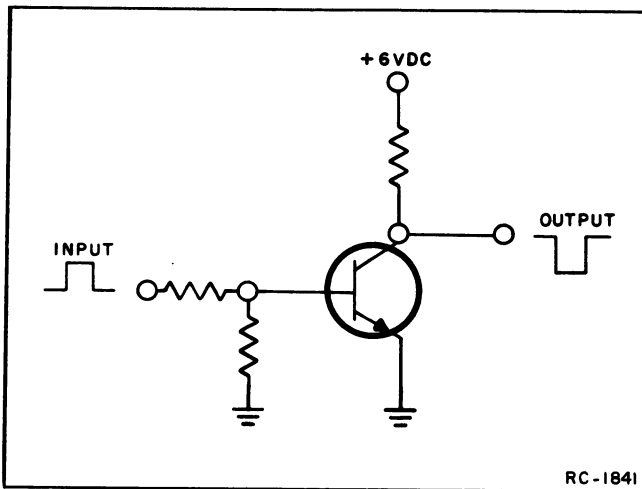


Figure 2 - Transistor Switching Circuit

GATING CIRCUITS

Formal logic requires that a statement be either true or false; no other condition can exist for the statement. A logic circuit is basically a switch or gate that is either closed or open; no other condition can exist for the circuit. By logical arrangement of these gating circuits, electrical functions can be performed in a pre-determined sequence by opening or closing the gates at the proper time.

A single-pole, single-throw switch is equivalent to a binary device with only two possible operating conditions: either open or closed. If point "C" of Figure 3 is to be made equal to potential V, switches A and B must be closed. It can then be said that $A \text{ AND } B = C$. If switches A and B are considered as gates, then potential V is said to be gated to "C" when both gates are

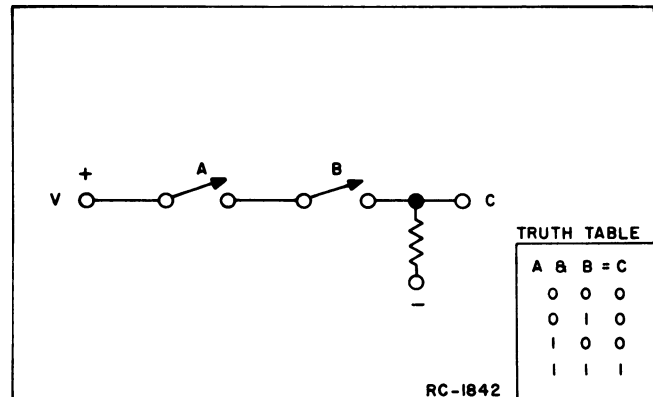


Figure 3 - Simple AND Gate

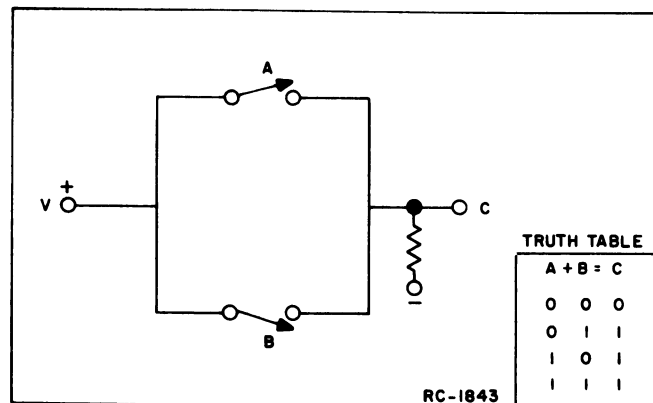


Figure 4 - Simple OR Gate

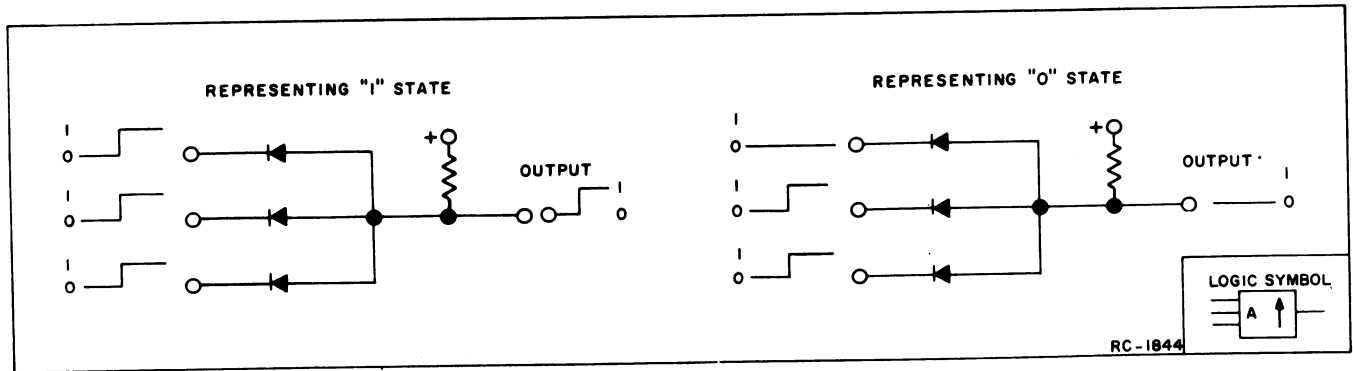


Figure 5 - Diode AND Gate

A or B (or both) may be closed. It can then be said $A \text{ OR } B = C$. All possible conditions for the OR gate are shown in the Truth Table in Figure 4.

DIODE GATING CIRCUITS

In gating circuits, the desired state of the gate may be represented by either "0" or "1". In this section, "1" will be used to represent a positive potential (approximately +6 volts) and "0" will be used to represent a low potential (near zero volts).

Logic Symbols

The use of logic symbols in this manual provides a simple method of showing the function of complicated logic circuits without drawing each diode, resistor and transistor in the circuit. The individual symbols can be tied together to form a logic diagram of a complete unit (decoder, encoder, etc.). Logic symbols of circuits used in the decoder are shown in the following simplified diagrams.

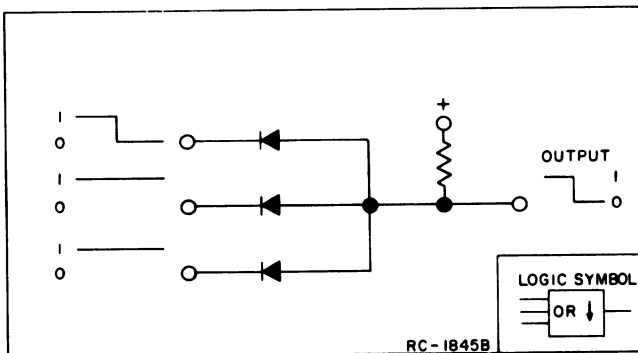


Figure 6 - Diode OR Gate

AND Gate

A simple diode AND gate is shown in Figure 5. The same conditions exist in this circuit as in the switch gate of Figure 3. Application of a positive potential to the diodes at all inputs will result in a positive potential at the output. This represents the "1" state of the gate. Application of a positive potential to one or two terminals will result in no potential developed, representing the "0" state of the gate.

OR Gate

A simple diode OR gate is shown in Figure 6. The same conditions exist in this circuit as the switch gate of Figure 4. Application of a positive potential at any of the inputs will result in an output of the same polarity, representing the "1" state.

NAND Gate

The basic logic circuitry used in the decoder is the NAND gate (NOT-AND). A NAND gate is simply an AND gate with a transistor inverter (NOT) stage added (see Figure 7).

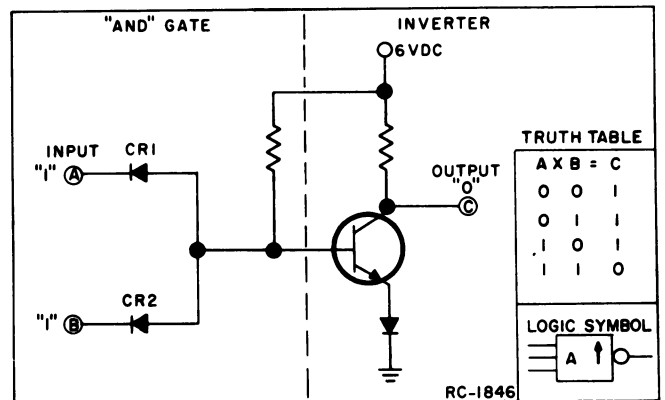


Figure 7 - Simplified NAND Gate

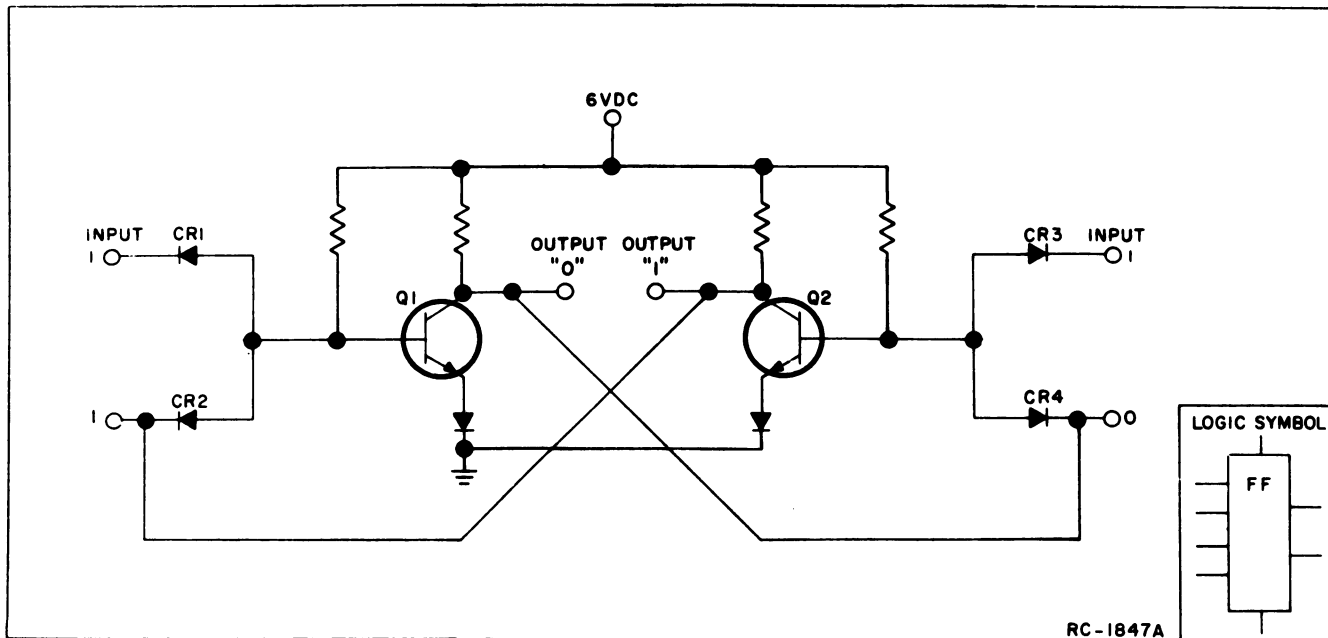


Figure 8 - NAND Gate Flip-Flop

Applying a positive potential to inputs A and B back biases diodes CR1 and CR2, permitting inverter Q1 to conduct. When conducting, the collector of Q1 drops to near ground potential.

Additional buffer or amplifier stages are usually added to the NAND gate to provide better isolation and increased gain. These additional stages are connected so that the logical output of the inverter is not changed.

NAND gates may also be used to provide the OR function. Assume that inputs A and B are all at a positive potential. Grounding either A or B turns off the inverter, so that the output (C) rises to approximately 6 volts.

Flip-Flops

Two NAND gates connected as shown in Figure 8 will provide the same logic functions as the conventional flip-flop (bistable multivibrator).

Assume that a positive potential is applied to all inputs. Momentarily grounding the cathode of CR3 or CR4 turns off Q2, causing its collector voltage to rise to approximately +6 volts. This turns on Q1, causing its collector voltage to drop to near ground potential, keeping Q2 turned off. The flip-flop will remain in this state until either CR1 or CR2 are grounded.

Usually, two or more of the flip-flops are connected in a "master-slave" configura-

tion (one flip-flop driving the other) for additional flexibility. Terminal identification for the flip-flop is shown in Figure 9A. However, the flip-flops used in the decoder are actually connected as shown in Figure 9B, with external connections from input terminal 3 to output terminal 9, and from input terminal 12 to output terminal 6. This leaves terminal 2 as the input terminal or "trigger". A flip-flop connected in this manner (J-K connected) will change state each time a negative-going pulse is applied to the trigger (terminal 2).

Terminal 10 of the flip-flop is the reset terminal. Applying a negative-going pulse to the reset terminal shifts the output of the flip-flop to a "1" at terminal 6

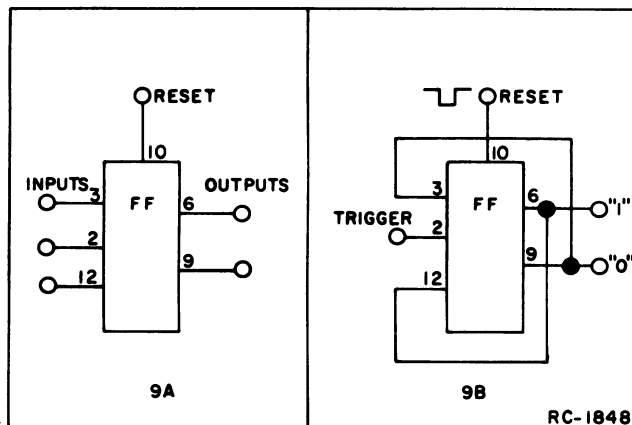


Figure 9 - Flip-Flop Terminal Identification

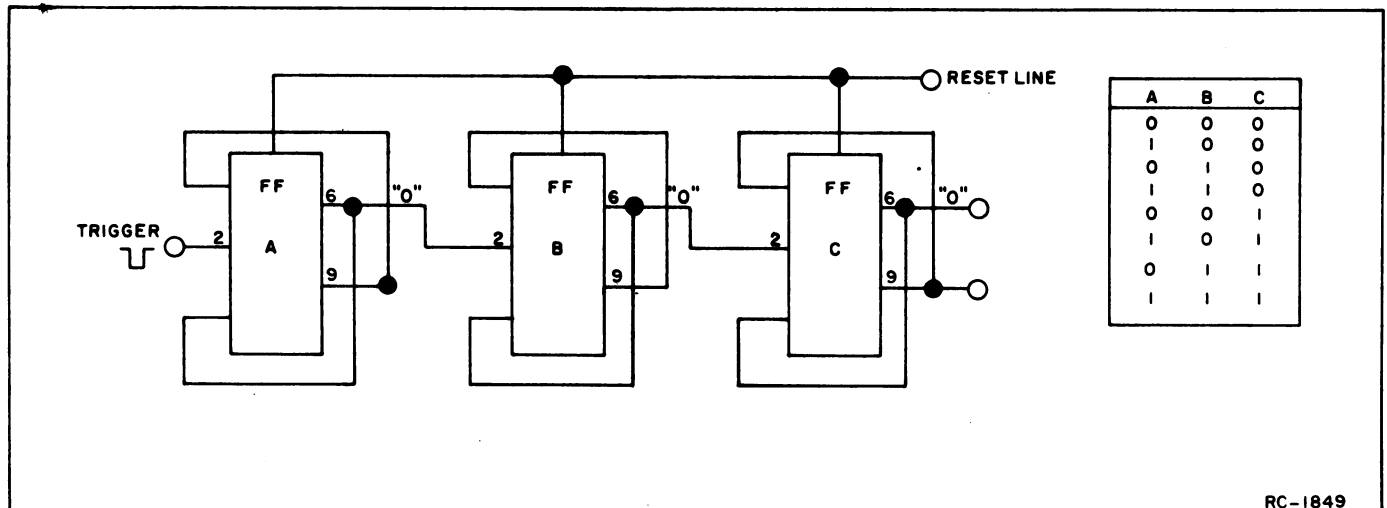


Figure 10 - Simplified Counter

and a "0" at terminal 9, even when a pulse is being applied to the trigger.

Counters

Two or more flip-flops may be connected to form a counter. The counter circuit in Figure 10 uses three flip-flops for counting up to eight pulses.

A reset pulse switches all three flip-flops to a "1" at terminal 6 (and a "0" at terminal 9). The first negative-going pulse applied to the trigger of A switches all of the flip-flops to the "0" state at terminal 6. The second pulse switches A back to the "1" state at terminal 6 while B and C do not change state.

Applying the third pulse switches terminal 6 of A back to a "0". This switches terminal 6 of B to a "1", which does not change the state of C. The application of four more pulses to the trigger of A will shift the outputs at terminal 6 of A, B and C as shown in the truth table in Figure 10. Note that each flip-flop changes state only when the preceding flip-flop goes from a "1" to a "0".

A NAND gate diode matrix connected to the outputs of the counter flip-flops is used to detect a unique set of outputs. In effect, the counter and matrix provides a simple method of recognizing (decoding) a correctly coded input signal. A simplified bit counter and digit counter with a decode matrix are shown in Figure 11.

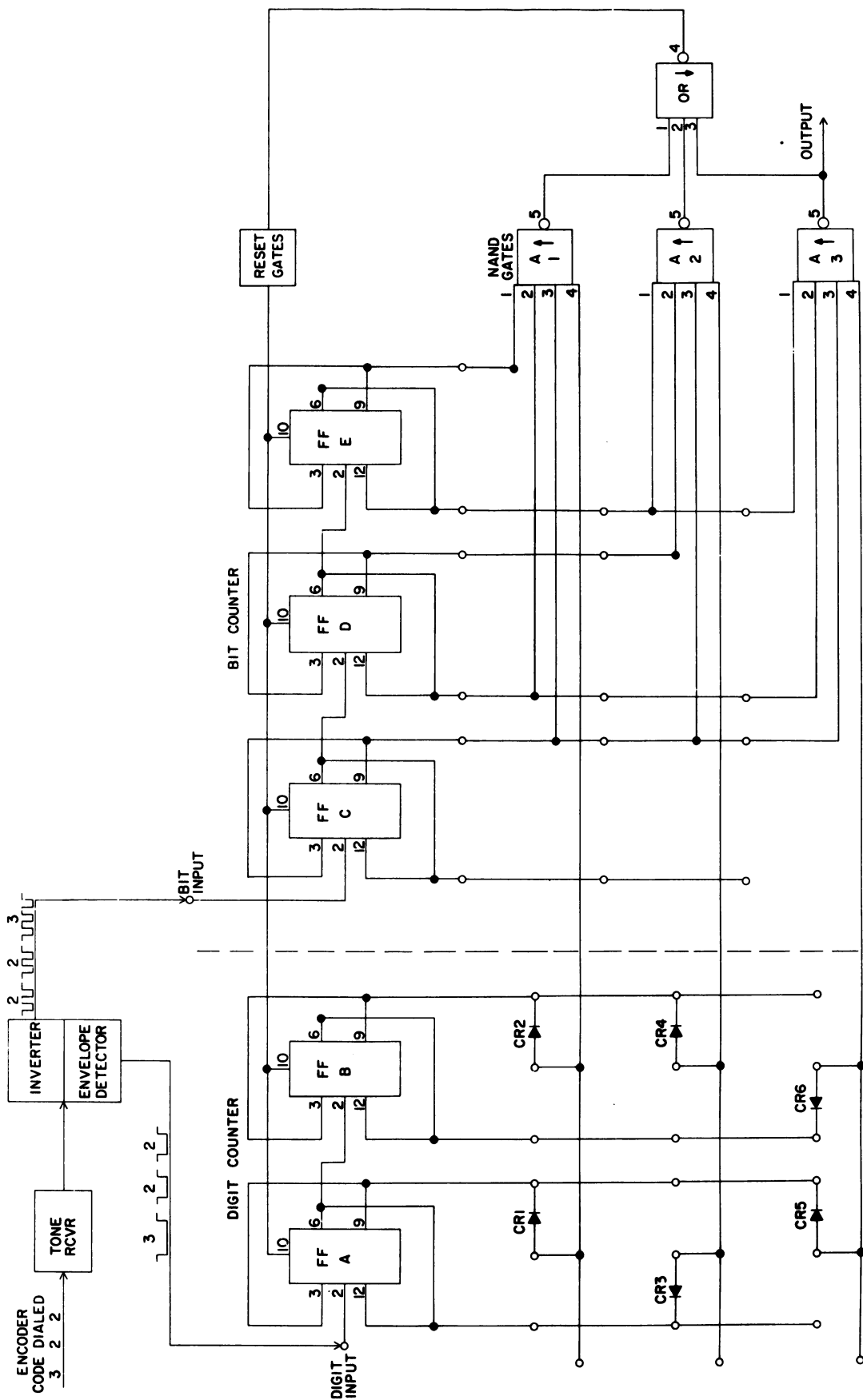
The digit counter is triggered by a pulse for each digit dialed, while the bit counter is triggered by a pulse for each interruption in the coded tone. The matrix is shown connected for a code of 3 - 2 - 2.

Assume that this code is being dialed at the encoder. Tone applied to the decoder at the start of dialing resets all of the flip-flops to a "1" at terminal 6. The first pulse at the dialed code applied to the counters switches all of the flip-flops to "0" at terminal 6.

In the digit counter, terminal 9 of flip-flops A and B are now positive. This back biases diodes CR1 and CR2, removing the ground on input 4 of NAND gate 1. As terminal 6 of A and B is "0", CR3 and CR6 are forward biased, grounding input 4 of NAND gates 2 and 3. This disables gates 2 and 3 while the first digit is counted.

In the bit counter, the second and third pulses switch terminal 6 of flip-flop C to a "1" and back to a "0". The "0" at the trigger of D switches its output to a 1, while E remains an "0". Terminal 9 of C and E are now positive, removing the ground on inputs 1 and 3 of NAND gate 1. Terminal 6 of D is positive, removing the ground on input 2 of NAND gate 1. All positive inputs activates the NAND gate and its output goes negative. This negative output activates the OR gate and its output goes positive. The positive OR gate output prevents the reset circuit from resetting the counters so that they remain ready for the next digit in the code.

In the digit counter, applying the second digit of the code switches flip-flop A to a "1" at terminal 6 while B remains a "0". This reverse biases CR3 and CR4, removing the ground to input 4 of NAND gate 2. The two pulses applied to the bit counter switch flip-flop C from "0" to "1", and from "1" to "0". The "0" at the trigger of D switches its output from "1" to "0", which switches E to "1". Now all of the inputs to NAND gate 2 are positive, activating the gate. This again activates the OR



RC-1936

Figure 11 - Simplified Counter and Matrix

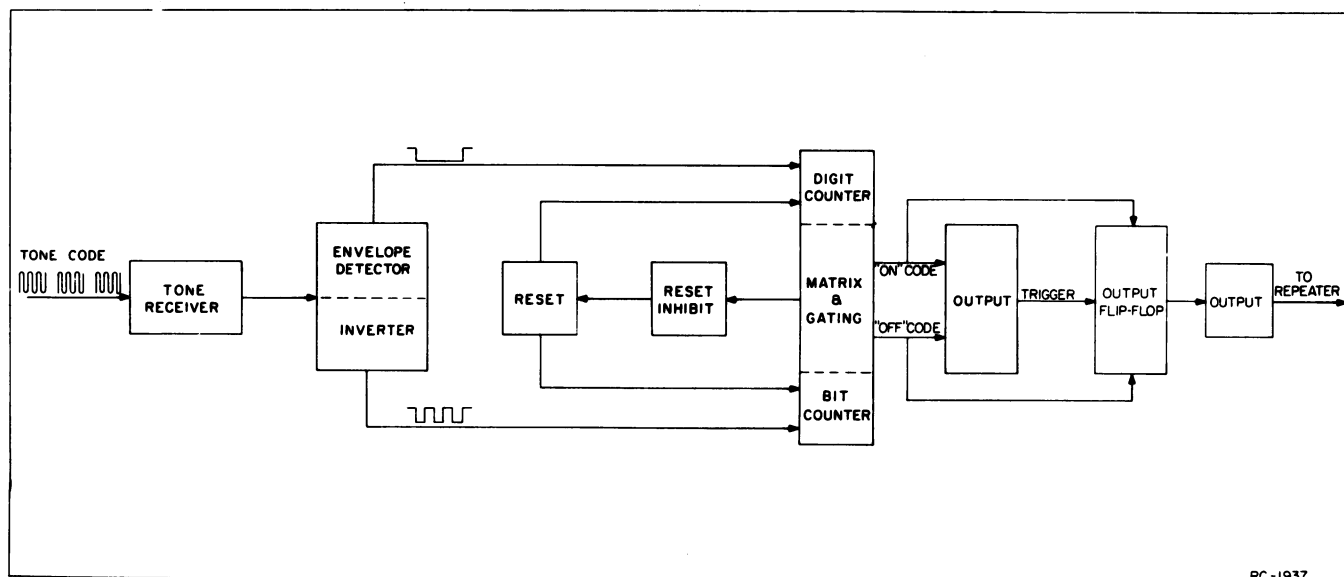


Figure 12 - Decoder Block Diagram

gate, so that its output goes positive to prevent resetting.

Applying the last digit of the code switches digit counter flip-flop A to "0" and B to "1". This reverse biases CR5 and CR6, removing the ground to input 4 of NAND gate 3. The two pulses applied to the bit counter shifts terminal 6 of flip-flop C from "0" to "1" and from "1" to "0". The "0" output switches D from "0" to "1", and output of E remains a "1". This activates NAND gate 3 and the OR gate to prevent resetting. The negative-going output of the NAND gate also is applied to the output circuitry for enabling or disabling the repeater functions.

When the tone is removed from the decoder for over 150 milliseconds, the counters reset and remain in the reset condition until tone is again applied to the decoder.

CIRCUIT ANALYSIS

The basic decoder consists of a tone receiver board, a pulse routing board and a counter board.

The decoder is fully transistorized, using both discrete components and Integrated Circuit Modules (IC's) for increased reliability. Typical schematic and logic diagrams of the IC's used in the decoder are listed in the Table of Contents.

References to symbol numbers mentioned in the following test may be found on the applicable Schematic Diagram, Outline Diagram and Parts List (see Table of Contents).

TONE RECEIVER

Three different tone receiver boards are available for use in the decoder, depending on the system frequency. The operating frequency of each board is as follows:

- A1701-590 Hz
- A1702-1500 Hz
- A1703-2805 Hz

Each tone receiver board consists of an amplifier-limiter, a tuned circuit, a detector and regulator, and an output switch.

A coded tone from the mobile or station receiver is coupled through DC blocking capacitor C12 to amplifier-limiters Q1 and Q2. A negative feedback path from the collector of Q1 to diode limiters CR3 and CR4 limits the signal applied to the base of Q2. Diodes CR1 and CR2 provide large-signal protection for Q1. The output of Q2 is applied to a tuned circuit consisting of C5/C6, C7/C8/C9 and L1/L2.

When an incorrect tone (or no tone) is applied to the tuned circuit, diode CR5 is forward biased by current through L1/L2. With CR5 conducting, detector Q3 is turned off. This allows diode CR6 to conduct, keeping output switch Q5 turned off.

Applying the correct tone to the tuned circuit increases the impedance of L1/L2, removing the bias on CR5. The diode now conducts only on the positive half-cycles of tone, and is cut off (reverse biased) on the negative half cycles. When a negative half cycle turns CR5 off, Q3 turns on. Turning on Q3 turns off CR6, which forward biases CR7 and CR8 and turns on output switch Q5. When a positive half cycle turns CR5

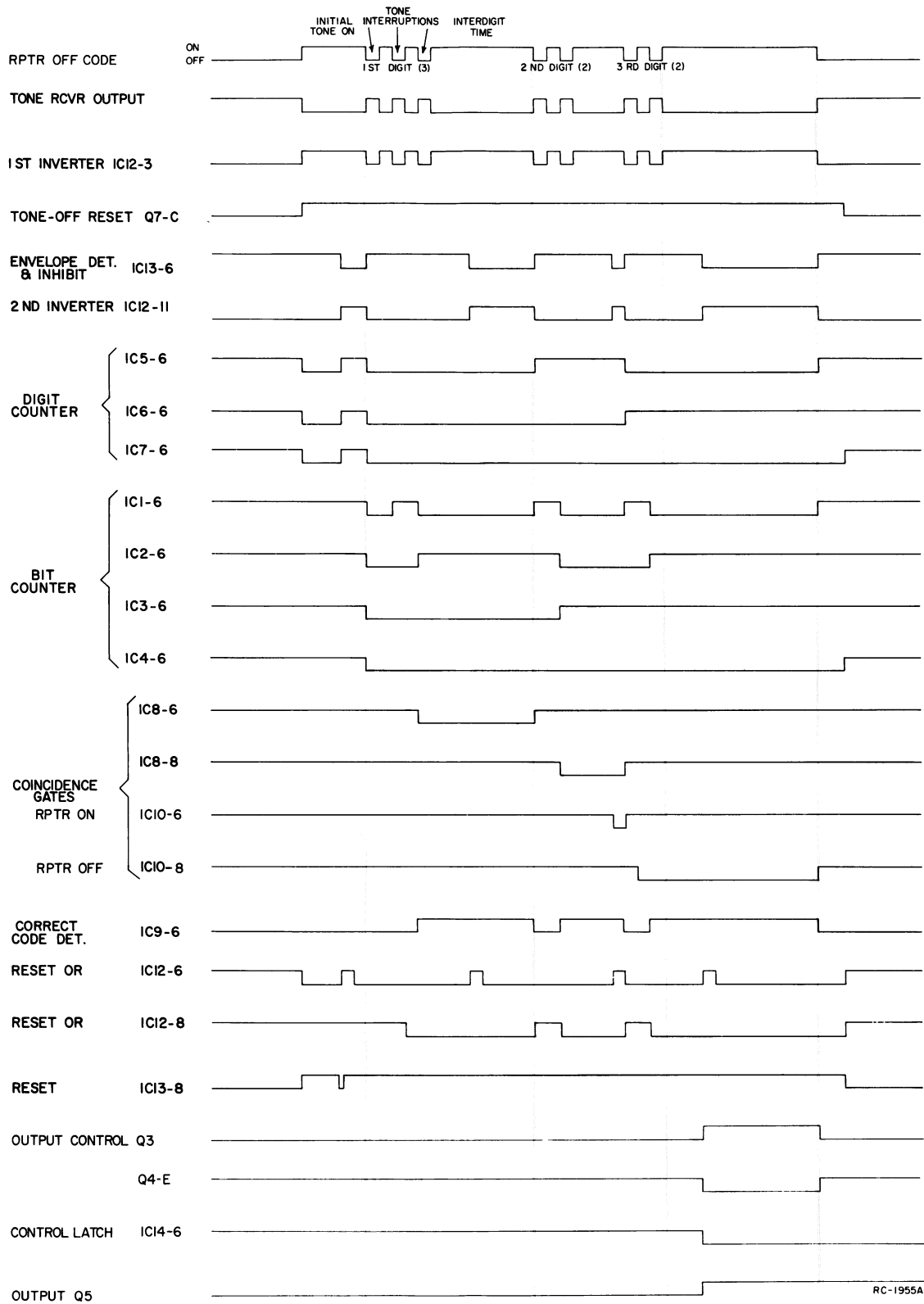


Figure 13 - Decoder Timing Waveforms

on (and Q3 off), C10 starts discharging through R17 and R18, keeping CR6 off and Q5 on. The output of Q5 is a positive pulse for each interruption in the tone code. Q4 acts as a regulator, keeping the emitter voltage of Q3 constant over the temperature range.

PULSE ROUTING BOARD

The pulse routing board contains the 6-volt regulator, inverters, envelope detector, tone-off reset, reset, and output stages. Multiple-input Integrated Circuits, (IC's) are used for the inverters, envelope detectors control latch flip-flop and reset circuits. Discrete transistors are used for the regulator, tone-off reset and output stages, and in the envelope detector.

Figure 13 contains a complete set of decoder timing waveforms. It is recommended that these waveforms be used in conjunction with the circuit analysis for a better understanding of the decoder circuitry.

6-VOLT REGULATOR

Operating voltage for the decoder is supplied by the 6-volt regulator. +13 volts from the vehicle battery or station power supply is applied to the zener diode-emitter follower regulator (CR8 and Q2). The +6-volt, 250-milliamp output is taken from the emitter of Q2.

1ST INVERTER

The output of the tone receiver board is connected to input terminal 1 of the 1st inverter (IC12).

When no tone is applied to the decoder, the output of the tone receiver board is high (positive) and the output of the inverter is low (zero). When tone is first applied the inverter output goes positive. The positive-going pulses (one for each interruption in the tone) from the tone receiver are changed to negative-going pulses by the inverter. These negative-going pulses are applied to the trigger of the first flip-flop in the bit counter.

The inverter output is also applied to the input of the envelope detector and the tone-off reset circuits.

ENVELOPE DETECTOR

With no tone applied, the zero inverter output is applied to terminal 1 of the envelope detector OR gate, resulting in a positive output.

When tone is first applied to the decoder, the inverter output goes positive. This positive potential is applied to terminal 1 of the OR gate, and also turns on Q1 so that its collector drops to zero. This keeps the OR gate output positive for as long as Q1 conducts. Q1 conducts until C1 is fully charged, and then turns off. This causes the OR gate output to drop to zero.

The first negative-going pulse in the pulse train from the inverter switches the OR gate output to positive, and also causes C1 to rapidly discharge through CR1 and CR2. The trailing edge of the first pulse (now positive-going) turns on Q1, keeping the OR gate output positive. This cycle is repeated until the end of the digit pulse train and results in a positive pulse envelope for the digit pulses. The pulse envelope is inverted by IC13 and the negative-going pulse triggers the first flip-flop in the digit counter.

TONE-OFF RESET

When tone is first applied, the positive inverter output of the first inverter turns on Q6, and also charges C9 through CR14. Turning on Q6 turns off normally-on transistor Q7 so that its collector goes positive.

The negative-going digit pulses applied to the tone-off reset circuit causes C9 to discharge through R20 and the base-emitter junction of Q6, which keeps Q6 on. The output of Q7 remains positive until tone is removed from the decoder and C9 discharges. The output of Q7 is applied to the reset circuit.

RESET

The reset circuit consists of two NAND gates utilized as negative OR gates (IC12) driving a NAND gate (IC13). A simplified reset circuit and the truth table for all of the gates is shown in Figure 14. When both OR gate outputs are positive, the NAND gate output goes negative, resetting the counter flip-flops.

With no tone applied to the decoder, input A to each OR gate is at zero, holding the NAND gate in the reset condition.

When tone is applied, the positive output of Q7 keeps terminal A of both OR gates positive. Terminal B of the first OR gate is kept positive through R4, and the output of OR gate is "0". In the second OR gate, terminal A is positive and terminal B is held at "0" by the correct code detector so that the second OR gate output is positive. The zero and positive inputs to the NAND gate keep its output high, preventing the counters from resetting.

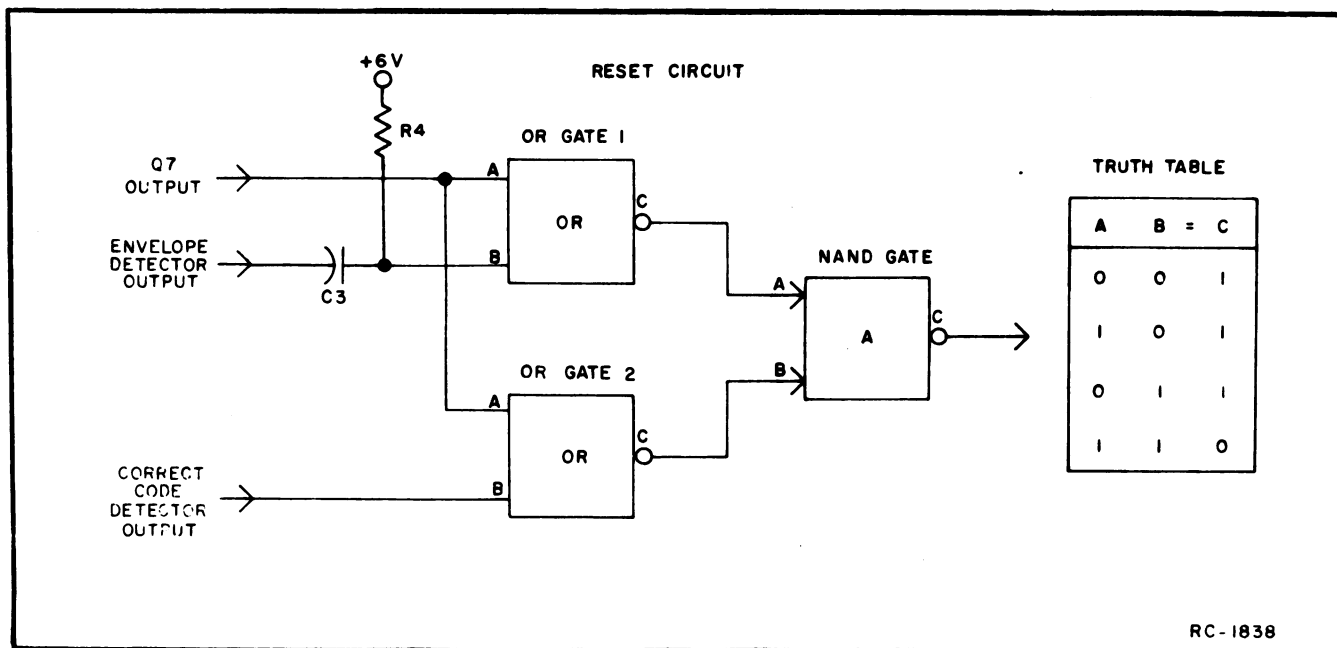


Figure 14 - Reset Circuit

At the end of the first digit, a negative pulse from the envelope detector is coupled through C3 to terminal 4 of the OR gate, causing its output to go positive momentarily. At the same time, if a correct code has been applied to the counters, the output of correct code detector (OR gate) goes positive and is applied to terminal B of the second OR gate. Now, the output of the first reset OR gate is positive, and the second OR gate is zero, keeping the NAND gate output positive (no reset).

If an incorrect code is dialed, the correct code detector output remains at zero and both OR gate outputs go positive at the end of the incorrect digit. This switches the NAND gate output to zero, resetting the counters.

OUTPUT

The decoder output can be connected for either Repeater Control or Timer Control applications. In Repeater Control applications, dialing a "Repeater On" code enables the repeater function, and dialing a "Repeater Off" code disables the repeater function. The decoder is normally shipped from the factory connected for Repeater Control.

In Timer Control applications, dialing a "Repeater On" code enables the repeater function. The repeater function is disabled when the Drop Out Delay Timer operates. The repeater can also be disabled by dialing the "Repeater Off" code.

Repeater Control

When no code is applied to the decoder, the positive output of coincidence gates "D" and "E" on the counter board is connected through R6 and R7 to the base of output transistor Q3, keeping the transistor turned off. Dialing the "Repeater On" code switches the output of coincidence gate "D" to ground potential. This causes current to flow in emitter-base junction of Q3, turning it on (see Figure 15). The ground from gate "D" is also applied to terminal 12 of the control-latch flip-flop. When Q3 is turned on, the positive voltage on its collector causes current to flow in the base-emitter junction of Q4, turning it on. With terminal 3 of the flip-flop at a positive potential and terminal 12 at ground, turning on Q4 grounds terminal 2, triggering the flip-flop. Triggering the flip-flop causes terminal 6 to go positive, back biasing diode CR8. Back biasing CR8 removes the shunt on the base current of Q5, permitting current to flow in the base-emitter junction of the transistor, turning it on. When turned on, Q5 completes a current path to the emitter of A703-Q1 on the Delay Timer board, enabling the repeater function.

With the emitter of A703-Q1 grounded, unsquelching the receiver applies 13 volts to the base of Q1, turning it on. This switches the flip-flop on the Delay Timer board, turning on A703-Q4. The +10 volts on the collector A703-Q4 turns on A702-Q4 on the Carrier-Operated Switch, lighting the TRANSMIT light and keying the station transmitter. The transmitter remains keyed

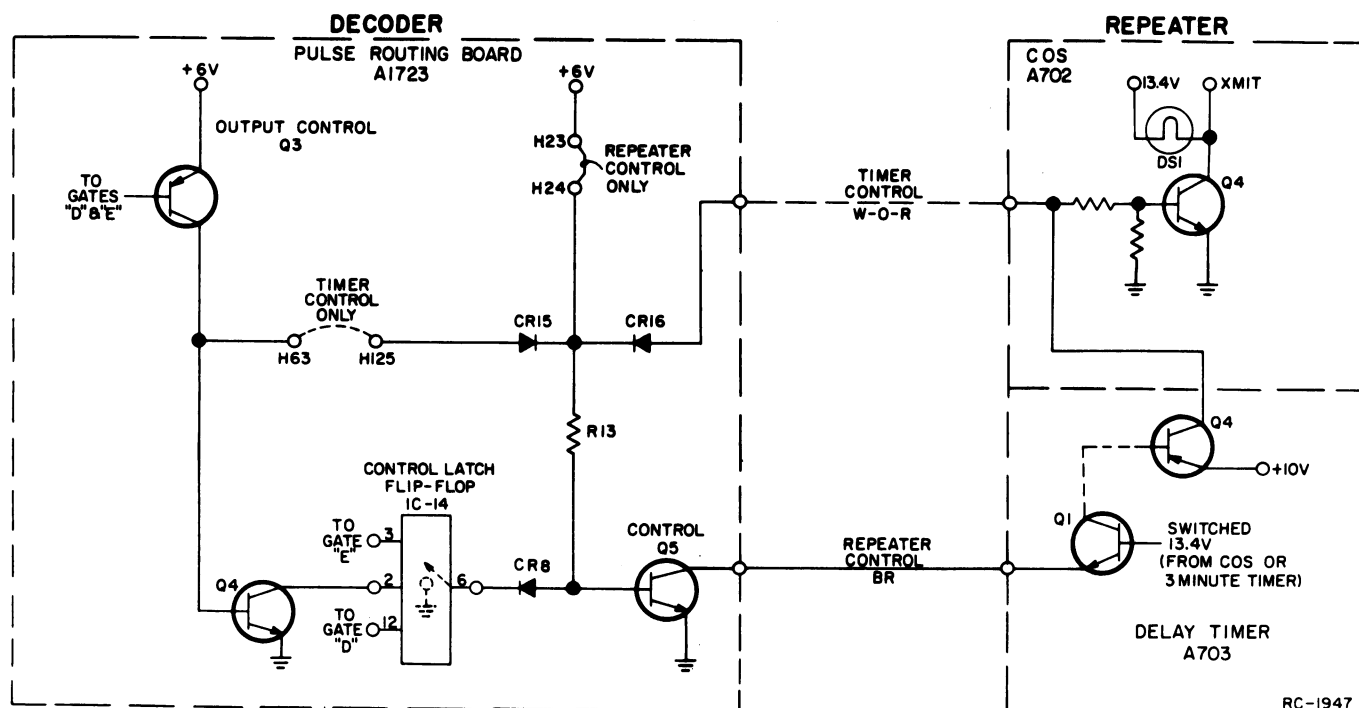


Figure 15 - Output Control Circuits

until the Delay Timer or 3-Minute Limit Timer operates. The repeater function remains enabled (Q5 on) until the "Repeater Off" code is dialed.

Dialing the "Repeater Off" code switches the output of coincidence gate "E" to ground, turning on Q3. The ground is also applied to terminal 3 of the control latch flip-flop. When turned on, the positive voltage on the collector of Q3 causes current to flow in the emitter junction of Q4, turning it on. With terminal 3 of the flip-flop at ground potential and terminal 12 at a positive potential, turning on Q4 triggers the flip-flop, causing output terminal 6 to drop to ground potential. This forward biases CR8 and shunts the base current to Q5, turning it off. Turning off Q5 removes the current path to the emitter of A703-Q1, disabling the repeater function. The repeater remains disabled until the "Repeater On" code is dialed.

Timer Control

In Timer Control applications, the output of Q3 is connected to the base circuit of Q5 by a jumper from H63 to H125. The 6-volt supply jumper from H23 to H24 is removed.

When no code is applied to the decoder, the positive output of coincidence gates "D" and "E" on the counter board is connected through R6 and R7 to the base of output control transistor Q3 keeping the transistor turned off. Dialing the "Repeater On"

code switches the output of coincidence gate "D" to ground potential. This causes current to flow in emitter-base junction of Q3, turning it on (see Figure 15). The ground from gate "D" is also applied to terminal 12 of the control-latch flip-flop. When Q3 is turned on, the positive voltage on its collector causes current to flow in the base-emitter junction of Q4, turning it on. With terminal 3 of the flip-flop at a positive potential and terminal 12 at ground, turning on Q4 grounds terminal 2, triggering and flip-flop. Triggering the flip-flop causes terminal 6 to go positive, back biasing diode CR8. Back biasing CR8 removes the shunt on the base current of Q5, permitting current to flow in the base-emitter junction of the transistor, turning it on. When turned on, Q5 completes a current path to the emitter of A703-Q1 on the Delay Timer board, enabling the repeater function.

With the emitter of A703-Q1 grounded, unsquelching the receiver applies 13 volts to the base of Q1, turning it on. This switches the flip-flop on the Delay Timer board, turning on A703-Q4. The +10 volts on the collector of A703-Q4 turns on Q4 on Carrier-Operated Switch A702, lighting the TRANSMIT light and keying the station transmitter.

The +10 volts at the base of A702-Q4 is also connected to the base of control transistor Q5, keeping Q5 locked on for the duration of the transmission. The transmitter remains keyed until the Delay Timer or optional 3-Minute Limit Timer operates.

When either timer operates, the +10 volts is removed from the base of Q5, turning it off. This disables the repeater function until the "Repeater On" code is dialed.

In the case of interference keying (noise unquenching the receiver), dialing the "Repeater Off" code overrides the Delay Timer, turning the transmitter off.

Dialing the "Repeater Off" code switches the output of coincidence gate "E" to ground, turning on Q3. The ground is also applied to terminal 3 of the control latch flip-flop. When turned on, the positive voltage on the collector of Q3 causes current to flow in the emitter junction of Q4, turning it on. With terminal 3 of the flip-flop at ground potential and terminal 12 at a positive potential, turning on Q4 triggers the flip-flop, causing output terminal 6 to drop to ground potential. This forward biases CR8 and shunts the base current at Q5, turning it off. Turning off Q5 removes the current path to the emitter of A703-Q1, disabling the repeater function. The repeater remains disabled until the "Repeater On" code is dialed.

EXTERNAL CONTROL RELAY

A relay and spike suppressor diode may be mounted on the decoder Pulse Routing Board whenever external control functions are required. The relay provides two form-C contacts for the desired switching functions, and may be dialed on (energized) and dialed off (de-energized).

Mounting locations and connections for the relay and diode are shown on the decoder Outline Diagram (see Table of Contents).

COUNTER BOARD

The counter board consists of 11 IC's in the counters and gating circuits. The digit counter consists of three master-slave flip-flops (IC5, IC6 and IC7) whose outputs are connected to the coincidence gates through a discrete diode matrix. The bit counter consists of four master-slave flip-flops (IC1, IC2, IC3 and IC4) whose outputs are connected to the coincidence gate inputs by screws located in the various holes in the counter board. The screws are positioned in holes 1 through 8 on lines A through G according to the code setting information as listed in the Table of Contents.

The decoder Schematic Diagram is shown strapped (by dotted lines in the matrix) for a "Repeater On" code of 5-9-5-5 and a "Repeater Off" code of 5-9-5-6. The Truth Table on the Schematic Diagram shows all possible states of the flip-flop outputs (at terminal 6) while counting.

Assume that the "Repeater On" code (5-9-5-5) is dialed at the encoder. When

the first digit is received at the decoder, one pulse is applied to the digit counter and five pulses are applied to the bit counter.

The pulse applied to the digit counter switches all of the flip-flops from the reset condition (all "1"s at terminal 6) to a "0" at terminal 6 and a "1" at terminal 9. This back biases diodes CR1, CR2 and CR3, removing the ground on terminal 3 of NAND coincidence gate "A".

The five pulses applied to the bit counter sequentially switches the flip-flop outputs at terminal 6 from the reset condition (all "1"s at terminal 6) to a "0" - "0" - "1" - "0" as shown on line 5 of the Truth Table. Now all of the inputs to coincidence gate "A" are positive, and its output goes to ground. The ground activates the correct code detector OR gate, and its output goes positive. The positive output (reset inhibit) is applied to the reset circuit to prevent the counters from resetting.

When the second digit (9) is applied to the decoder, another pulse is applied to the digit counter and nine pulses are applied to the bit counter.

The pulse applied to the digit counter switches the flip-flops to a "1" - "0" - "1" at terminal 6. This back biases CR4, CR5 and CR6, removing the ground on terminal 11 of coincidence gate "B".

The nine pulses applied to the bit counter switches the flip-flop outputs at terminal 6 to a "1" - "0" - "1" - "1" as shown on line 14 of the Truth Table. Now all of the inputs to coincidence gate "B" are positive, and its output goes to ground. This activates the correct code detector and its output goes positive. The positive reset inhibit is applied to the reset circuit to prevent the counters from resetting.

Applying the third digit (5) to the decoder applies one more pulse to the digit counter and 5 more pulses to the bit counter.

The pulse applied to the digit counter switches the flip-flops to "0" - "1" - "0" at terminal 6. This back biases CR7, CR8 and CR9, removing the ground on terminal 11 of coincidence gate "C".

The five pulses applied to the bit counter switches the flip-flops to "0" - "1" - "0" - "0" at terminal 6 as shown on line 3 of the Truth Table. Note that after the counter counts 16 bits, it recycles (i.e., starts counting over again from the first line on the Truth Table). Now all of the inputs to coincidence gate "C" are positive. The output of the coincidence gate goes to ground, activating the correct code detector.

The fourth digit applies one more pulse to the digit counter and five more pulses to the bit counter. The pulse applied to the digit counter switches the flip-flops to "1" - "1" - "0" at terminal 6. This back biases diodes CR10, CR11 and CR12, removing the ground on terminal 3 of coincidence gate "D".

The five pulses applied to the bit counter switch the bit counter outputs at terminal 6 to "1" - "1" - "0" as shown on line eight of the Truth Table. Now all of the inputs to coincidence gate "D" are positive, causing its output at terminal 6 to drop to ground potential to activate the correct code detector. The ground is also applied to the base of output control transistor and to terminal 12 of the control latch flip-flop. This activates the output stages and enables the repeater.

After the code is completed, the counters reset so that the decoder is ready for another code.

Dialing the "Repeater OFF" code activates coincidence gates "A", "B", "C" and "E" in that order. This activates the output stages and disables the repeater function.

MAINTENANCE

DISASSEMBLY

To gain access to the decoder assembly, remove the four #6 screws in the back of the decoder and slide the housing. The counter board is at the top of the decoder for ease of code strapping.

To gain access to the tone receiver and pulse routing boards, remove the single screw on one end of the hinged tone receiver board, and swing the board up.

TROUBLESHOOTING

Procedures for troubleshooting the decoder include DC readings and waveforms for the tone receiver, pulse routing and counter boards. Refer to the Troubleshooting Procedure as listed in the Table of Contents.

TIMER CONTROL MODIFICATION

For Timer Control operation, modify the pulse routing board as follows:

1. Remove the decoder cover and gain access to the pulse routing board as directed in the Disassembly Procedure.
2. Remove the jumper between H23 and H24 (refer to the Outline Diagram for location of Holes).
3. Connect a jumper between H63 and H125.
4. Connect the White-Orange-Red wire (at H26) to TB701-5 on the repeater panel.

ADJUSTMENT

Coil L1/L2 on the tone receiver board is the only adjustment on the decoder. This coils is set at the factory and will normally require no further adjustment unless it is necessary to replace L1/L2, C5/C6 or C7/C8/C9. If any of these components are replaced, adjust L1/L2 as follows:

1. Connect a VTVM across C5/C6 or C7/C8/C9.
2. Apply a continuous tone to the decoder at the proper operating frequency (590 Hz, 1500 Hz or 2805 Hz).
3. Tune L1/L2 for maximum meter reading.

CODE SETTING

3-DIGIT INDIVIDUAL CALL CODES

For three-digit operation, modify the counter board and set the codes according to the following procedure:

1. Move the White-Black-Brown wire from H9 to H17 (see Figure 16).
2. Move diode CR10 to the dotted position (see Figure 16).
3. Connect a jumper from H11 to H12 (see Figure 16).
4. The codes used as examples are:

Repeater On - 5-9-5
Repeater Off -5-9-6

5. Write complete three-digit codes in the box below:

Function	Number
Repeater On	
Repeater Off	

EXAMPLE:

Function	Number
Repeater On	5-9-5
Repeater Off	5-9-6

6. Place the first digit of the code beside the letter A in the column of letters below. Next add second digit to the first and put this sum beside B. Add the third digit to figure placed at B and place this sum at C (Repeater Off) or D (Repeater On). NOTE: Zero on the telephone dial actually provides 10 pulses. When a zero is used in a code number, it must be added as a 10.

EXAMPLE:

REPEATER ON

A First Digit
+ Second Digit
B Subtotal
+ Third Digit
D Total

REPEATER ON 5 9 5

A 5
+ 9
B 14
+ 5
D 19

First Digit
Second Digit
Subtotal
Third Digit
Total

REPEATER OFF

A First Digit
+ Second Digit
B Subtotal
+ Third Digit
C Total

REPEATER OFF 5 9 6

A 5
+ 9
B 14
+ 6
C 20

First Digit
Second Digit
Subtotal
Third Digit
Total

7. Write each letter beside its corresponding subtotal in the following columns.
8. Read the screw positions for each subtotal and move the four screws for each letter to their proper positions on the Counter Board.

LETTERS SUBTOTALS SCREW POSITIONS

	1	2 4 6 8
	2	1 4 6 8
	3	2 3 6 8
A	(5)	(2 4 5 8)
	6	1 4 5 8
	7	2 3 5 8
	8	1 3 5 8
	9	2 4 6 7
	10	1 4 6 7
	11	2 3 6 7
	12	1 3 6 7
B	(14)	(1 4 5 7)
	15	2 3 5 7
	16	1 3 5 7
	17	2 4 6 8
Repeater On--D	(18)	(1 4 6 8)
Repeater Off-C	(19)	(2 3 6 8)
	20	1 3 6 8
	21	2 4 5 8
	22	1 4 5 8
	23	2 3 5 8
	24	1 3 5 8
	25	2 4 6 7
	26	1 4 6 7
	27	2 3 6 7
	28	1 3 6 7
	29	2 4 5 7
	30	1 4 5 7
	31	2 3 5 7
	32	1 3 5 7

The decoder is normally shipped from the factory set for the codes used in the examples below. Set the new codes assembly to the following procedure. The codes used are:

REPEATER ON - 5-9-5-5
REPEATER OFF - 5-9-5-6

1. Write the complete four-digit code in the box below:

EXAMPLE:

Function	Number
Repeater On	
Repeater Off	

Function	Number
Repeater On	5955
Repeater Off	5956

2. Place the first digit of the code beside the letters below. Next, add the second digit to the first and put this sum beside B. Add the third digit to figure placed at B and place this sum at C. NOTE: Zero on the telephone dial actually provides 10 pulses. When a zero is used in a code number, it must be added as a 10.

EXAMPLE:

REPEATER ON

A First Digit
+ Second Digit
B Subtotal
+ Third Digit
C Subtotal
+ Fourth Digit
D Total

REPEATER ON 5 9 5 5

A 5
+ 9
B 14
+ 5
C 19
+ 5
D 24

First Digit
Second Digit
Subtotal
Third Digit
Subtotal
Fourth Digit
Total

REPEATER OFF

A First Digit
+ Second Digit
B Subtotal
+ Third Digit
C Subtotal
+ Fourth Digit
E Total

REPEATER OFF 5 9 5 6

A 5
+ 9
B 14
+ 5
C 19
+ 6
E 25

First Digit
Second Digit
Subtotal
Third Digit
Subtotal
Fourth Digit
Total

3. Write each letter beside its corresponding subtotal in the columns at right.
4. Read the screw positions for each subtotal and move the four screws for each letter to their proper positions on the counter board (See Figure 16).

4-DIGIT INDIVIDUAL CALL CODES

LETTERS	SUBTOTALS	SCREW POSITIONS
	1	2 4 6 8
	2	1 4 6 8
	3	2 3 6 8
	4	1 3 6 8
A	(5)	(2 4 5 8)
	6	1 4 5 8
	7	2 3 5 8
	8	1 3 5 8
	9	2 4 6 7
	10	1 4 6 7
	11	2 3 6 7
	12	1 3 6 7
	13	2 4 5 7
B	(14)	(1 4 5 7)
	15	2 3 5 7
	16	1 3 5 7
	17	2 4 6 8
	18	1 4 6 8
C	(19)	(2 3 6 8)
	20	1 3 6 8
	21	2 4 5 8
	22	1 4 5 8
	23	2 3 5 8
D	(24)	(1 3 5 8)
E	(25)	(2 4 6 7)
	26	1 4 6 7
	27	2 3 6 7
	28	1 3 6 7
	29	2 4 5 7
	30	1 4 5 7
	31	2 3 5 7
	32	1 3 5 7
	33	2 4 6 8
	34	1 4 6 8
	35	2 3 6 8
	36	1 3 6 8
	37	2 4 5 8
	38	1 4 5 8
	39	2 3 5 8
	40	1 3 5 8

NOTE

The letters A through G used in the Code Setting Procedure correspond to a line of screw positions on The Counter Board. The numerals 1 through 8 represent the position of each screw in the selected screw line.

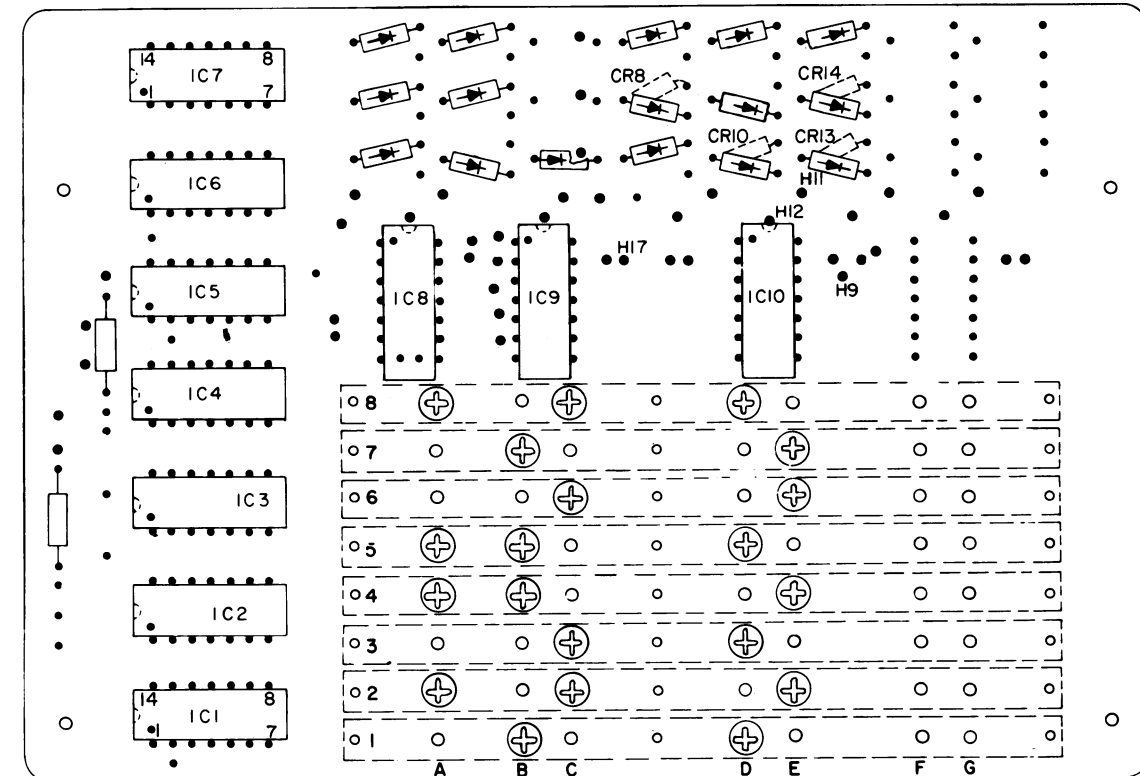


Figure 16 - Counter Board

RC-1956

CODE SETTING PROCEDURE

REPEATER CONTROL DIGITAL DECODER
MODELS 4EJ18D10-12

CODE SETTING

1-DIGIT DROP-OUT

The counter board may be modified for one-digit drop-out, so that dialing a single number disable the repeater. It is recommended that a higher number be used to minimize falsing (i.e., 7, 8, 9 or 0).

NOTE

The number used for the one-digit drop-out code cannot be used in any other code.

With a 4-Digit Code:

1. If the decoder is strapped for a four-digit "Repeater On" code, move CR13 and CR14 to the dotted position as shown in Figure 16.
2. Write an "E" beside the number selected in the column below. The number used in the example is a 0 (must be counted as a 10).
3. Read the screw positions for the selected number, and move the four screws to their proper position in line E.

CODE NUMBER	SCREW POSITIONS
1	2 4 6 8
2	1 4 6 8
3	2 3 6 8
4	1 3 6 8
5	2 4 5 8
6	1 4 5 8
7	2 3 5 8
8	1 3 5 8
9	2 4 6 7

EXAMPLE: E--(10)----- (1 4 6 7)

With a 3-Digit Code:

1. If the decoder is strapped for a three-digit "Repeater On" code, move CR8 to the dotted position as shown in Figure 16.
2. Write a "C" beside the number selected in the column below. The number used in the example is a 0 (must be counted as a 10).
3. Read the screw positions for the selected number, and move the four screws to their proper position in line C.

CODE NUMBER	SCREW POSITIONS
1	2 4 6 8
2	1 4 6 8
3	2 3 6 8
4	1 3 6 8
5	2 4 5 8
6	1 4 5 8
7	2 3 5 8
8	1 3 5 8
9	2 4 6 7

EXAMPLE: C--(10)----- (1 4 6 7)

NOTE

The letters A through G used in the Code Setting Procedure correspond to a line of screw positions on The Counter Board. The numerals 1 through 8 represent the position of each screw in the selected screw line.

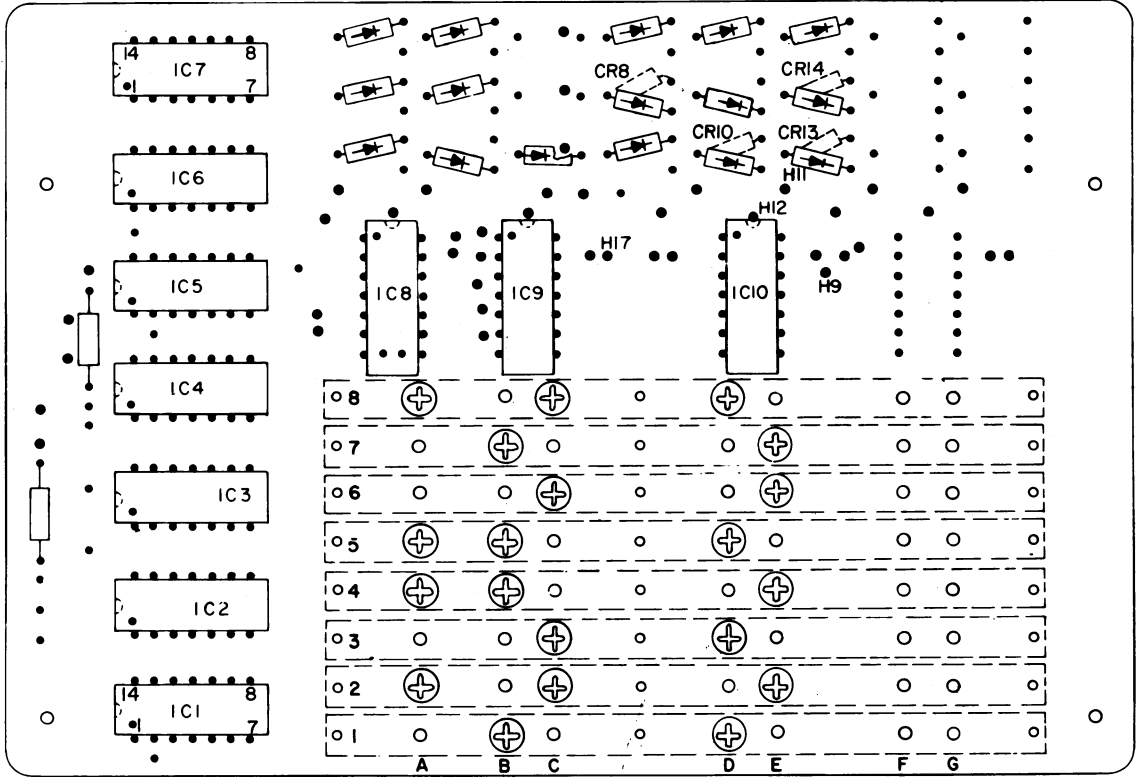
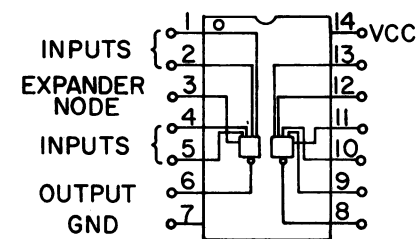


Figure 16 - Counter Board RC-1956

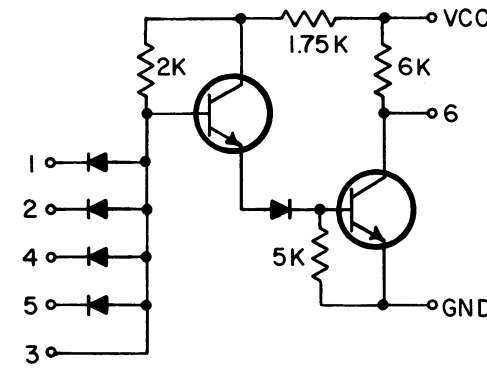
CODE SETTING PROCEDURE

REPEATER CONTROL DIGITAL DECODER
MODELS 4EJ18D10-12

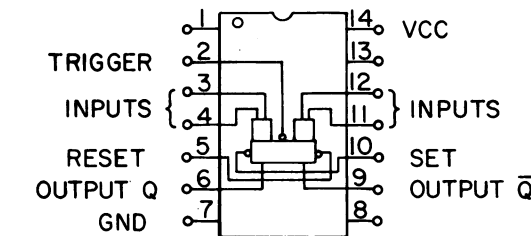
DUAL 4-INPUT GATES 19AI15913-P1



LOGIC DIAGRAM

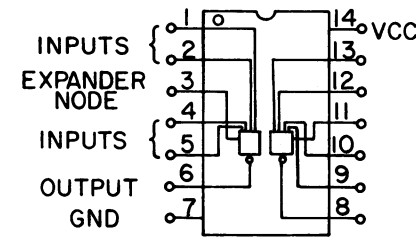
TYPICAL SCHEMATIC DIAGRAM
(ONE GATE ONLY)

MASTER-SLAVE FLIP-FLOP 19AI15913-P6

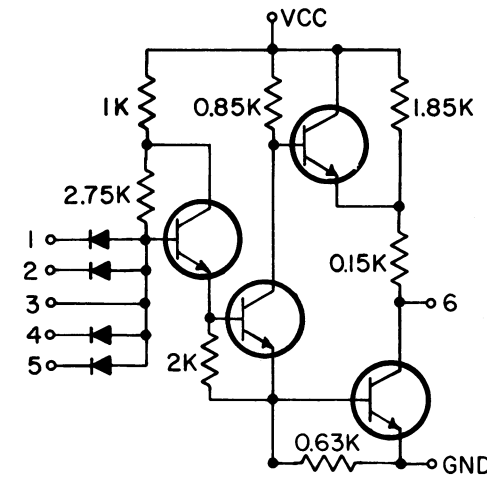


LOGIC DIAGRAM

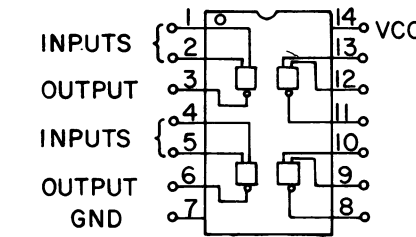
DUAL 4-INPUT BUFFERED GATES 19AI15913-P3



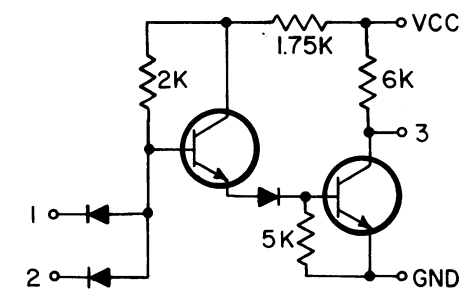
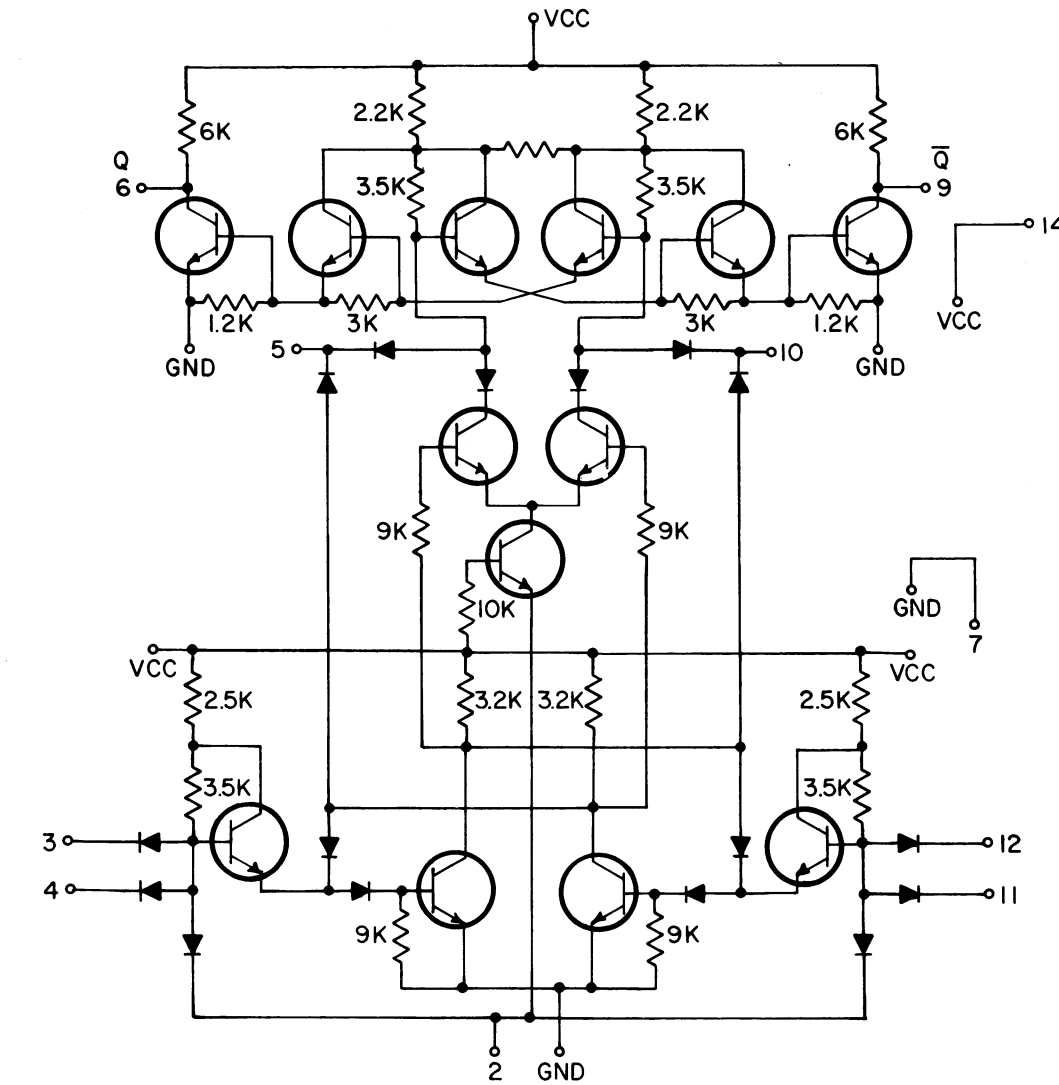
LOGIC DIAGRAM

TYPICAL SCHEMATIC DIAGRAM
(ONE GATE ONLY)

QUADRUPLE 2-INPUT GATES 19AI15913-P7



LOGIC DIAGRAM

TYPICAL SCHEMATIC DIAGRAM
(ONE GATE ONLY)

RC-1837

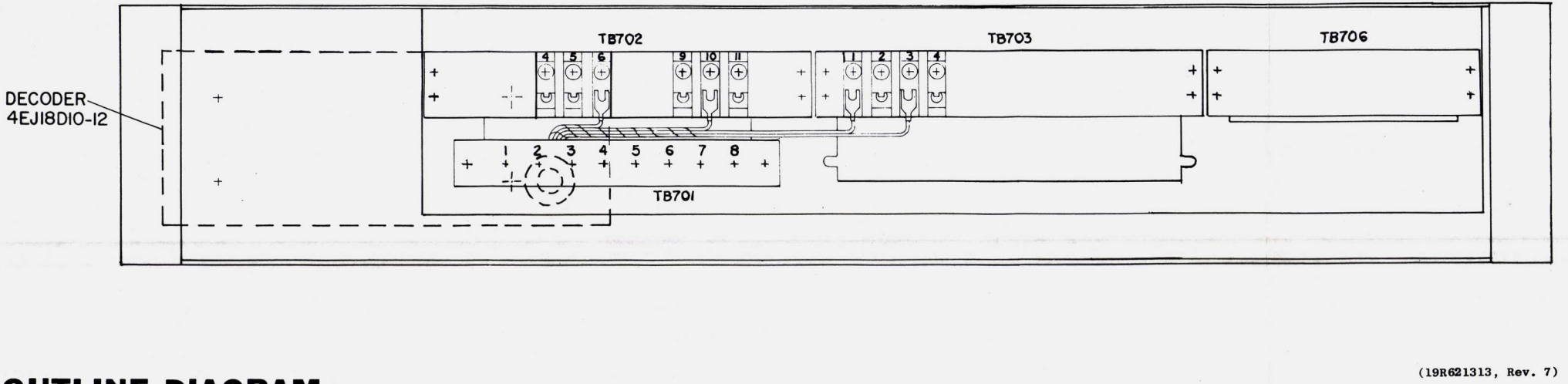
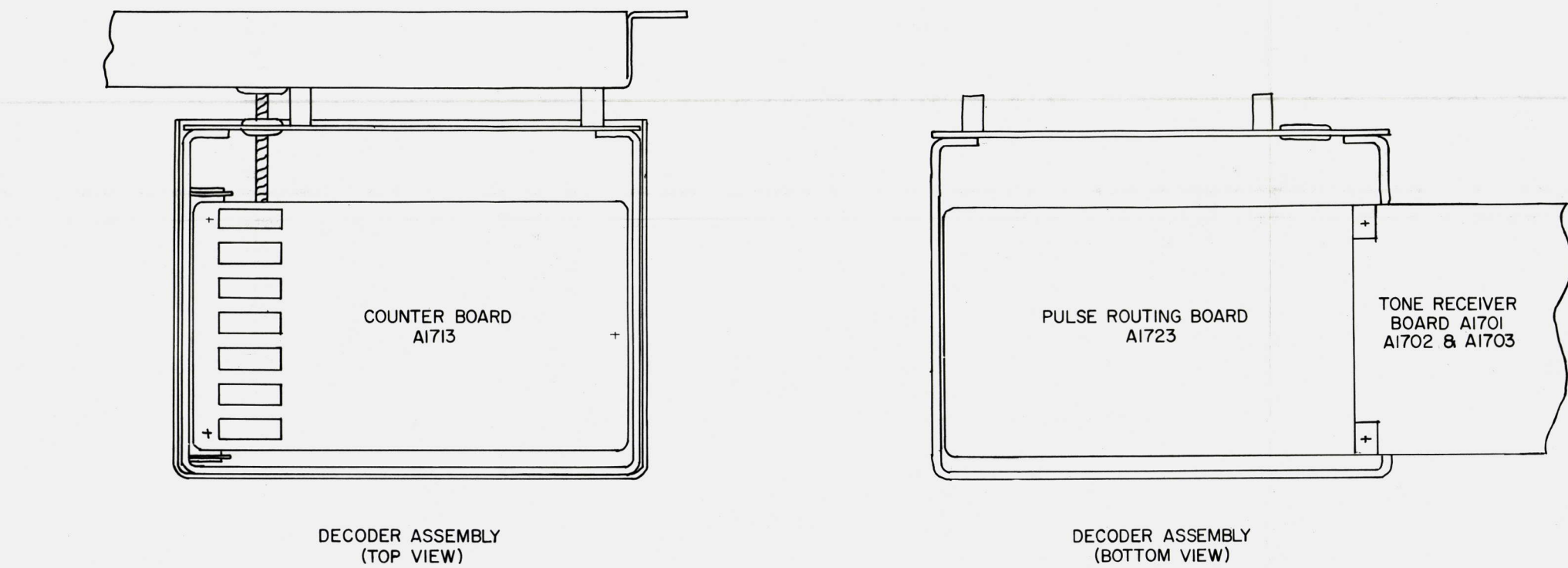
TYPICAL SCHEMATIC DIAGRAM

TYPICAL LOGIC & SCHEMATIC DIAGRAMS

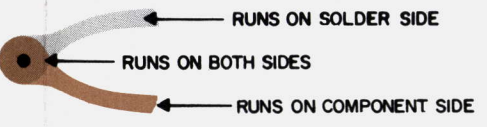
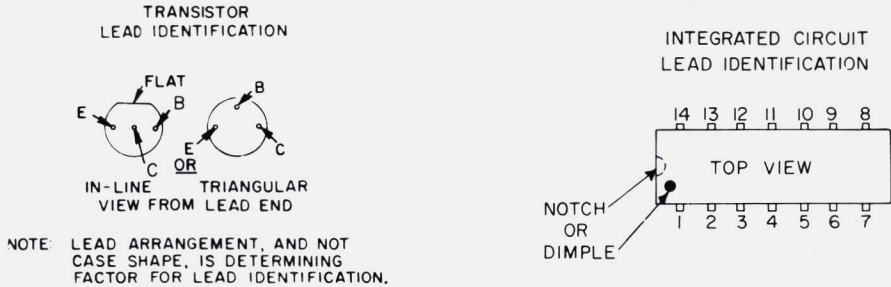
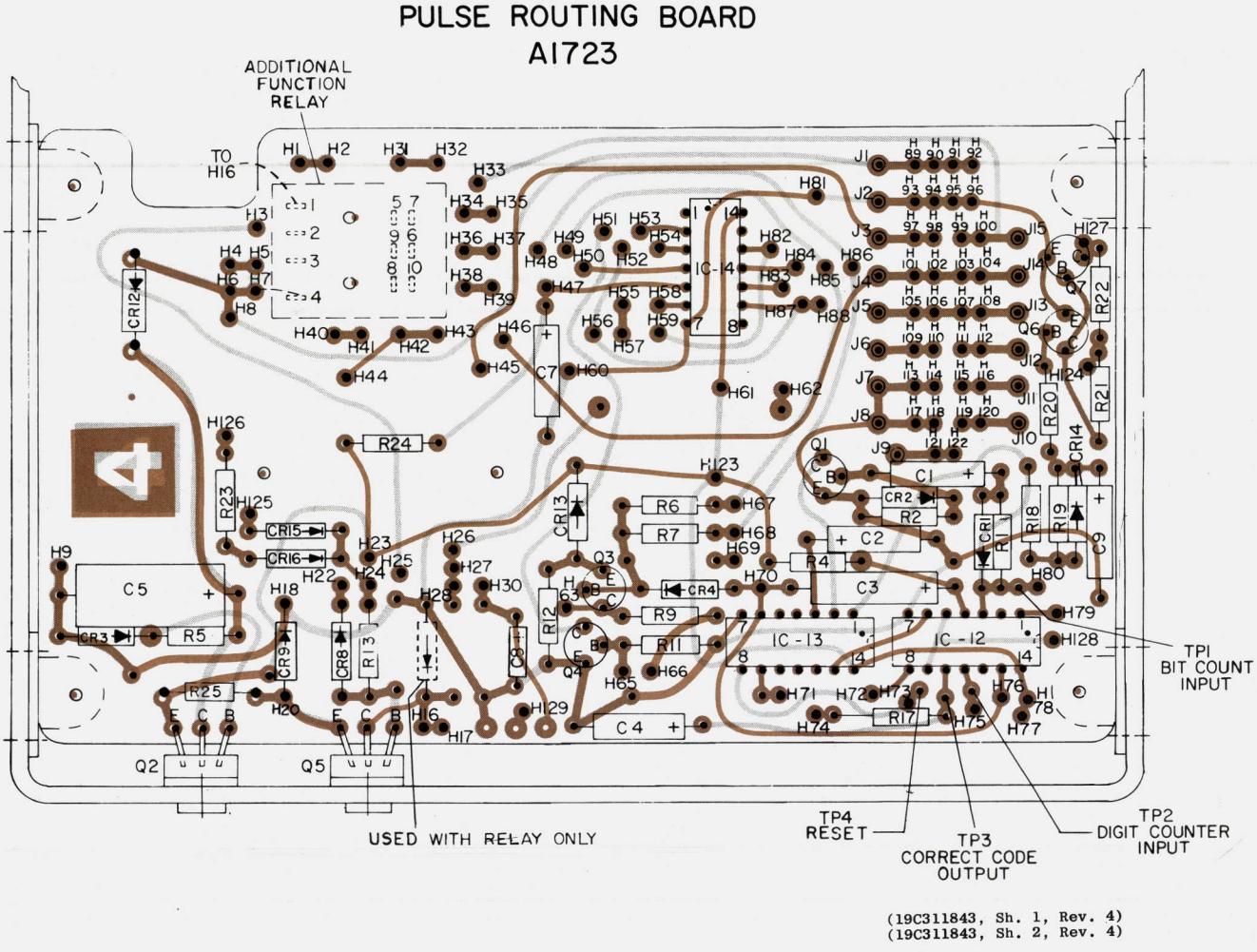
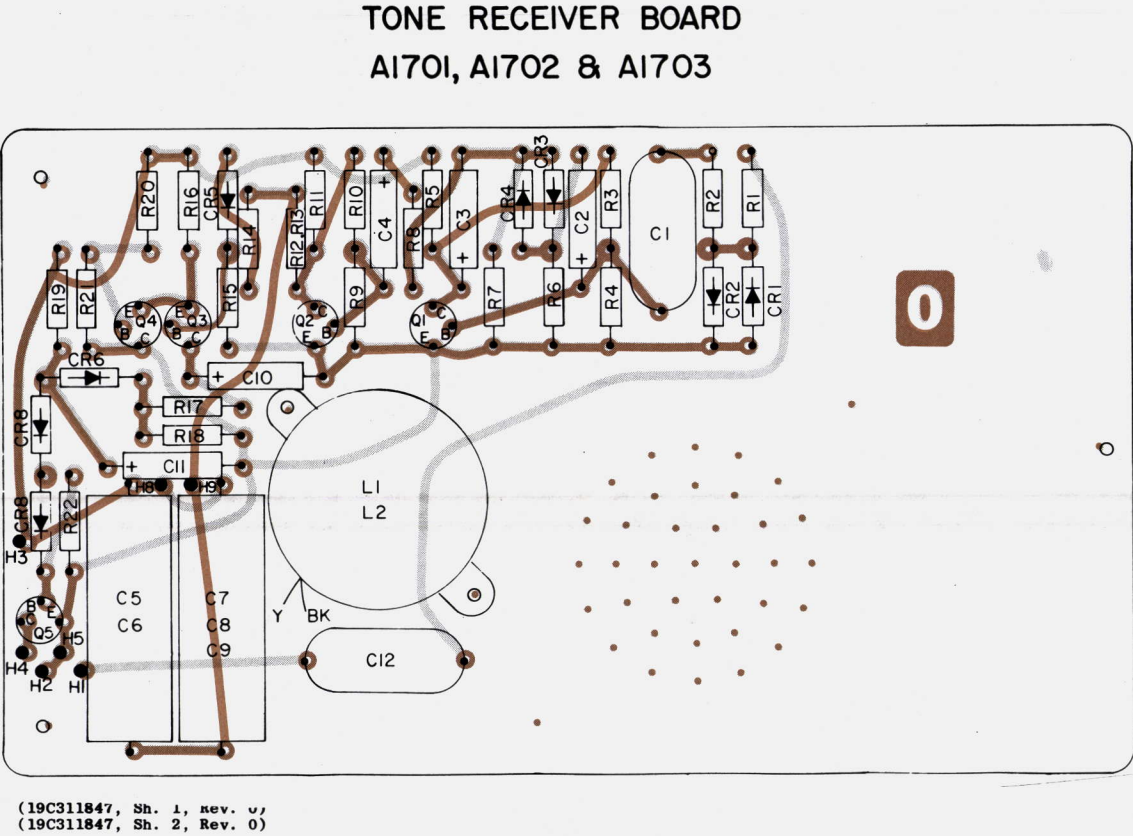
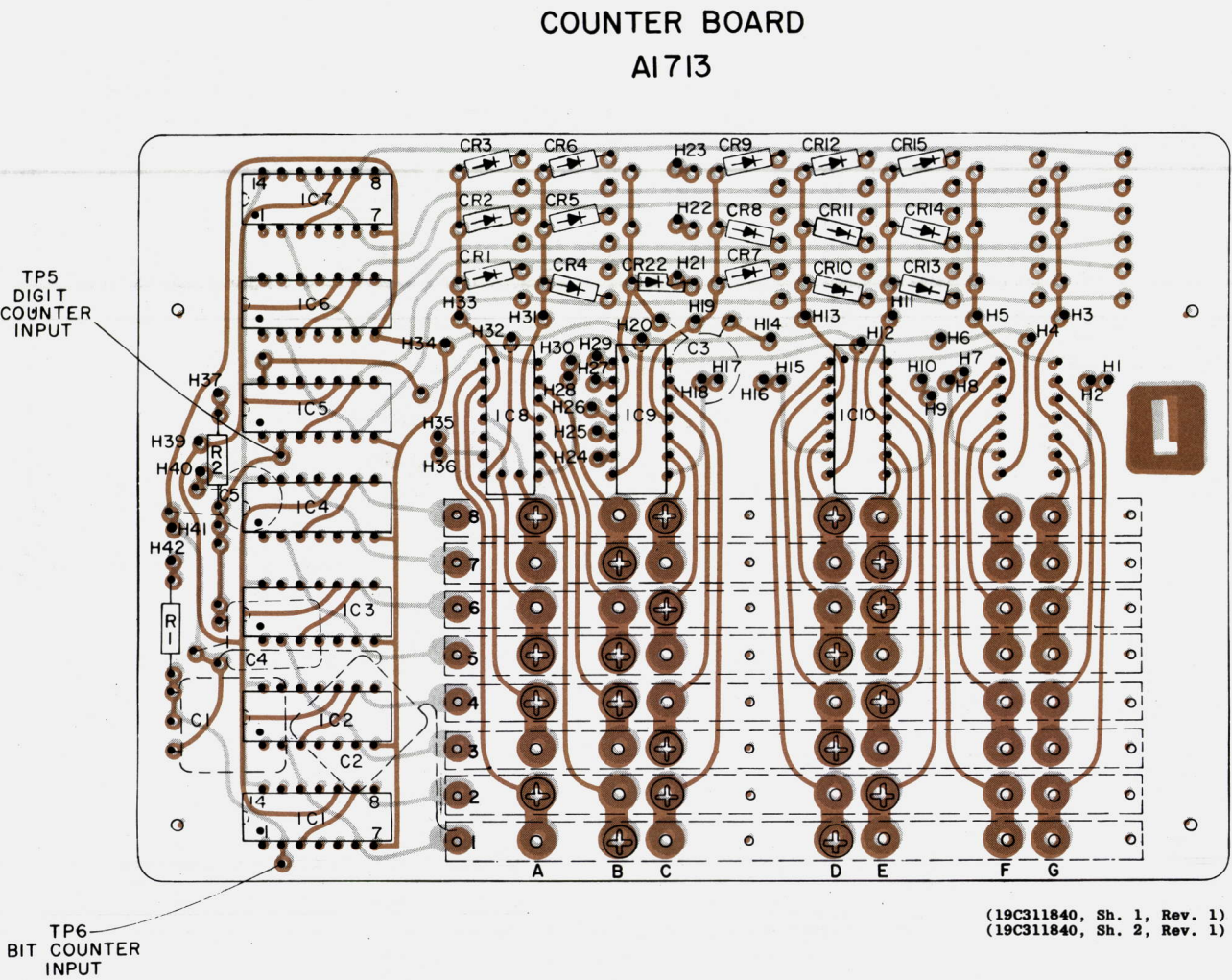
FOR INTEGRATED CIRCUIT MODULES
REPEATER CONTROL DIGITAL DECODER MODELS 4EJ18D10-12

OUTLINE DIAGRAM

REPEATER CONTROL DIGITAL DECODER
MODELS 4EJ18D10-12



(19R621313, Rev. 7)





PARTS LIST

LBI-4038B

REPEATER DECODER PANEL

MODELS 4EJ18D10-12

SYMBOL	GE PART NO.	DESCRIPTION
A1701 thru A1703		TONE RECEIVER A1701 19C311852G1 590 Hz A1702 19C311852G2 1500 Hz A1703 19C311852G3 2805 Hz
----- CAPACITORS -----		
C1	19B209243P14	Polyester: 0.33 μ f \pm 20%, 250 VDCW.
C2 and C3	5496267P1	Tantalum: 6.8 μ f \pm 20%, 6 VDCW; sim to Sprague Type 150D.
C4	5496267P17	Tantalum: 1.0 μ f \pm 20%, 35 VDCW; sim to Sprague Type 150D.
C5	19C300075P 47001G	Polyester: 47,000 pf \pm 2%, 100 VDCW; sim to GE Type 61F.
C6	5496249P25000G	Polystyrene: 25,000 pf \pm 2-1/2%, 125 VDCW.
C7	19C300075P 22002G	Polyester: 220,000 pf \pm 2%, 100 VDCW; sim to GE Type 61F.
C8	5496249P16000G	Polystyrene: 16,000 pf \pm 2-1/2%, 125 VDCW.
C9	5496249P20000G	Polystyrene: 20,000 pf \pm 2-1/2%, 125 VDCW.
C10	5496267P17	Tantalum: 1.0 μ f \pm 20%, 35 VDCW; sim to Sprague Type 150D.
C11	5496267P13	Tantalum: 2.2 μ f \pm 20%, 20 VDCW; sim to Sprague Type 150D.
C12	19B209243P14	Polyester: 0.33 μ f \pm 20%, 250 VDCW.
----- DIODES AND RECTIFIERS -----		
CR1 thru CR8	19A115250P1	Silicon.
----- INDUCTORS -----		
L1	19B205354G2	Coil.
L2	19B205354G3	Coil.
----- TRANSISTORS -----		
Q1	19A115362P1	Silicon, NPN; sim to Type 2N2925.
Q2	19A115123P1	Silicon, NPN; sim to Type 2N2712.
Q3 and Q4	19A115768P1	Silicon, PNP; sim to Type 2N3702.
Q5	19A115123P1	Silicon, NPN; sim to Type 2N2712.
----- RESISTORS -----		
R1 and R2	3R152P302J	Composition: 3000 ohms \pm 5%, 1/4 w.
R3	3R152P513J	Composition: 51,000 ohms \pm 5%, 1/4 w.
R4	3R152P123J	Composition: 12,000 ohms \pm 5%, 1/4 w.
R5	3R152P242J	Composition: 2400 ohms \pm 5%, 1/4 w.
R6 and R7	3R152P223J	Composition: 22,000 ohms \pm 5%, 1/4 w.
R8	3R152P102J	Composition: 1000 ohms \pm 5%, 1/4 w.
R9	3R152P103J	Composition: 10,000 ohms \pm 5%, 1/4 w.
R10	3R152P473J	Composition: 47,000 ohms \pm 5%, 1/4 w.
R11	3R152P103J	Composition: 10,000 ohms \pm 5%, 1/4 w.
R12	3R152P243J	Composition: 24,000 ohms \pm 5%, 1/4 w.
R13	3R152P513J	Composition: 51,000 ohms \pm 5%, 1/4 w.

SYMBOL	GE PART NO.	DESCRIPTION
R14	3R152P103J	Composition: 10,000 ohms \pm 5%, 1/4 w.
R15	3R152P204J	Composition: 200,000 ohms \pm 5%, 1/4 w.
R16	3R152P221J	Composition: 220 ohms \pm 5%, 1/4 w.
R17 and R18	3R152P822J	Composition: 8200 ohms \pm 5%, 1/4 w.
R19	3R152P753J	Composition: 75,000 ohms \pm 5%, 1/4 w.
R20	3R152P242J	Composition: 2400 ohms \pm 5%, 1/4 w.
R21	3R152P622J	Composition: 6200 ohms \pm 5%, 1/4 w.
R22	3R152P104J	Composition: 100,000 ohms \pm 5%, 1/4 w.
DECODER 19D413162G3		
A1713		COUNTER BOARD 19D413160G3
----- CAPACITORS -----		
C1	19A116080P7	Polyester: 0.1 μ f \pm 20%, 50 VDCW.
C2*	19A116080P7	Polyester: 0.1 μ f \pm 20%, 50 VDCW.
Earlier than REV A:		
	19B209243P7	Polyester: 0.1 μ f \pm 20%, 50 VDCW.
C3	5494481P11	Ceramic disc: 1000 pf \pm 20%, 1000 VDCW; sim to RMC Type JF Discap.
C4*	19A116080P103	Polyester: 0.022 μ f \pm 10%, 50 VDCW. Added by REV B.
C5*	5494481P11	Ceramic disc: 1000 pf \pm 20%, 1000 VDCW; sim to RMC Type JF Discap. Added by REV B.
----- DIODES AND RECTIFIERS -----		
CR1 thru CR15	19A115250P1	Silicon.
CR22	19A115250P1	Silicon.
----- INTEGRATED CIRCUITS -----		
IC1 thru IC7	19A115913P6	Digital, Clocked Flip-Flop; sim to Fairchild DTL 945.
IC8 thru IC10	19A115913P1	Digital, Dual 4-Input Gate; sim to Fairchild DTL 930.
----- RESISTORS -----		
R1 and R2	3R152P510J	Composition: 51 ohms \pm 5%, 1/4 w.
----- TEST POINTS -----		
TP5 and TP6	N503P304C13	Cotter Pin.
A1723		PULSE ROUTING BOARD 19D413158G3
----- CAPACITORS -----		
C1	5496267P17	Tantalum: 1.0 μ f \pm 20%, 35 VDCW; sim to Sprague Type 150D.
C2	5496267P1	Tantalum: 6.8 μ f \pm 20%, 6 VDCW; sim to Sprague Type 150D.
C3	5496267P10	Tantalum: 22 μ f \pm 20%, 15 VDCW; sim to Sprague Type 150D.
C4	5496267P17	Tantalum: 1.0 μ f \pm 20%, 35 VDCW; sim to Sprague Type 150D.
C5	5496267P15	Tantalum: 47 μ f \pm 20%, 20 VDCW; sim to Sprague Type 150D.
C7	5496267P1	Tantalum: 6.8 μ f \pm 20%, 6 VDCW; sim to Sprague Type 150D.
C8*	5496267P17	Tantalum: 1.0 μ f \pm 20%, 35 VDCW; sim to Sprague Type 150D. Added by REV A.

SYMBOL	GE PART NO.	DESCRIPTION
C9	5496267P13	Tantalum: 2.2 μ f \pm 20%, 20 VDCW; sim to Sprague Type 150D.
----- DIODES AND RECTIFIERS -----		
CR1 and CR2	19A115250P1	Silicon.
CR3	4036887P6	Silicon, Zener.
CR4	19A115250P1	Silicon.
CR8	19A115250P1	Silicon.
CR9	4037822P1	Silicon.
CR12	4037822P1	Silicon.
CR13	4036887P1	Silicon, Zener.
CR14 thru CR16	19A115250P1	Silicon.
CR17*	4037822P1	Silicon. Added by REV C. Deleted by REV D.
----- INTEGRATED CIRCUITS -----		
IC12	19A115913P7	Digital, Quad 2-Input Gate; sim to Fairchild DTL 946.
IC13	19A115913P3	Digital, Dual Buffer; sim to Fairchild DTL 932.
IC14	19A115913P6	Digital, Clocked Flip-Flop; sim to Fairchild DTL 945.
----- JACKS AND RECEPTACLES -----		
J1 thru J15	4033513P15	Contact, electrical: sim to Bead Chain R40-1A.
----- TRANSISTORS -----		
Q1	19A115362P1	Silicon, NPN; sim to Type 2N2925.
Q2	19A116118P1	Silicon, NPN.
Q3	19A115768P1	Silicon, PNP; sim to Type 2N3702.
Q4	19A115123P1	Silicon, NPN; sim to Type 2N2712.
Q5	19A116118P1	Silicon, NPN.
Q6	19A115889P1	Silicon, NPN; sim to Type 2N2712.
Q7	19A115123P1	Silicon, NPN; sim to Type 2N2712.
----- RESISTORS -----		
R1	3R152P333J	Composition: 33,000 ohms \pm 5%, 1/4 w.
R2	3R152P623J	Composition: 62,000 ohms \pm 5%, 1/4 w.
R4	3R152P202J	Composition: 2000 ohms \pm 5%, 1/4 w.
R5	3R152P561J	Composition: 560 ohms \pm 5%, 1/4 w.
R6 and R7	3R152P302J	Composition: 3000 ohms \pm 5%, 1/4 w.
R9	3R152P302J	Composition: 3000 ohms \pm 5%, 1/4 w.
R11*	3R152P513J	Composition: 51,000 ohms \pm 5%, 1/4 w.
Earlier than REV A:		
	3R152P512J	Composition: 5100 ohms \pm 5%, 1/4 w.
R12	3R152P202J	Composition: 2000 ohms \pm 5%, 1/4 w.
R13*	3R152P202J	Composition: 2000 ohms \pm 5%, 1/4 w.
In REV D and earlier:		
	3R152P221J	Composition: 220 ohms \pm 5%, 1/4 w.
R15*	3R152P21J	Composition: 620 ohms \pm 5%, 1/4 w. Added by REV A. Deleted by REV E.
R17	3R152P240J	Composition: 24 ohms \pm 5%, 1/4 w.
R18	3R152P332J	Composition: 3300 ohms \pm 5%, 1/4 w.
R19	3R152P393J	Composition: 39,000 ohms \pm 5%, 1/4 w.
R20	3R152P104J	Composition: 100,000 ohms \pm 5%, 1/4 w.
R21	3R152P303J	Composition: 30,000 ohms \pm 5%, 1/4 w.
R22	3R152P103J	Composition: 10,000 ohms \pm 5%, 1/4 w.
R23	3R152P102J	Composition: 1000 ohms \pm 5%, 1/4 w.

SYMBOL	GE PART NO.	DESCRIPTION
R24	3R152P513J	Composition: 51,000 ohms \pm 5%, 1/4 w.
R25*	3R152P102J	Composition: 1000 ohms \pm 5%, 1/4 w. Added by REV B.
----- TEST POINTS -----		
TP1 thru TP4	N503P304C13	Cotter Pin.
ADDED FUNCTION RELAY AND DIODE		
	19A115250P1	Diode, silicon.
	5491595P12	Relay, armature: 1.5 w operating, 520 ohms \pm 15% coil res, 2 form C contacts; sim to Allied Control T154-X-186.

PRODUCTION CHANGES

Changes in equipment to improve performance or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by these revisions.

Pulse Routing Board, 19D413158G3

REV. A - To improve operation of control-latch flip-flop on Pulse Routing Board. Added C8, R15 and jumper from R30 to H66. Changed R11.

REV. B - To insure operation of the optional added-function relay on Pulse Routing Board. Added R25.

REV. C - To optimize the control transistor emitter bias. Added CR17.

Decoder, 19D413162G3

REV. A - To improve the threshold of the input stages of the bit and digital counters. Deleted C2. Added C2 between code setting strip 1 and the hole nearest IC2 terminal 2.

REV. B - To prevent operation due to ignition noise and other stray pulses. Added C4 and C5.

Pulse Routing Board, 19D413158G3

REV. D - To improve reliability. Deleted CR17.

REV. E - To improve keying reliability. Changed R13. Deleted R15.

TROUBLESHOOTING PROCEDURE

EQUIPMENT REQUIRED

- DC-triggered oscilloscope
- AC and DC VTVM
- A tone generator of the proper frequency and a telephone-type dial, or a TGS-735 or TGS-740 encoder on the proper frequency
- A 12-volt, DC power supply

PRELIMINARY INSTRUCTIONS

1. All waveforms shown are with the proper tone applied and the digit 5 dialed. Note: the digit 6 was dialed for the incorrect code reset waveform shown in Figure 17.
2. The oscilloscope setting for all waveforms is 5 volts/division vertical and 100 milliseconds/division horizontal except where noted.
3. Before starting the procedure, check for +6 volts DC at the emitter of regulator transistor Q2 (see Fig. 17). Then check for +6 volts on the Counter and Tone Receiver Boards (see Figs. 18 and 19).

SYMPTOM	PROCEDURE
PULSE ROUTING AND COUNTER BOARDS	
Decoder responds to a wrong code	<ol style="list-style-type: none"> 1. Check the screw placement on the counter board (refer to the Code Setting Procedures as listed in the Table of Contents). 2. Check to see that no screws are missing (one screw in each pad). 3. Check to see that all screws are firmly seated. 4. Check diode CR4 (see Fig. 17).
Decoder doesn't respond to correct codes	<ol style="list-style-type: none"> 1. Check the screw placement on the counter board (refer to the Code Setting Procedure as listed in the Table of Contents). At no time should two screws be located in any one screw pad (see Figure 18). 2. Dial a "5" and check the waveforms at TP1 and TP2 (see Fig. 17). If the proper waveforms are not present, refer to Tone Receiver Board Checks. If proper waveforms are present, continue with Step 3. 3. Dial a correct first digit and keep the tone on after dialing. All of the screw heads in row A should measure approximately +6 volts DC, which indicates that the first digit was counted correctly. <p>Dial a correct second digit and keep the tone on after dialing. All of the screw heads in Row B should be at +6 volts, indicating the second digit was counted correctly.</p> <p>Dial a correct third digit and keep the tone on after dialing. All of the screw heads in row C should measure +6 volts, indicating that the third digit was counted correctly.</p> <p>Dial a correct fourth digit (Repeater on Code), and keep the tone on after dialing. All of the screw heads in row D should measure +6 volts, indicating that the fourth digit was counted correctly.</p> <p>If all of the digits are counted correctly, check the alarm output of Q3 at H63 (see Fig. 17) and check the output circuit (Q3, Q5, CR15, etc.). If the screw heads do not go to +6 volts during the digit checks, continue with Step 4.</p>

SYMPTOM	PROCEDURE
Decoder doesn't respond to correct codes (cont'd)	<ol style="list-style-type: none"> 4. Connect the reset disable jumper to battery negative to prevent re-setting while dialing (see Fig. 17). Dial the correct first digit again, keeping the tone on after dialing. Check the screw heads in row A again for +6 volts. If all of the screw heads are at +6 volts, check for a positive voltage at the cathode of CR1, CR2 and CR3. If the screw heads or cathodes are not positive, check the flip-flops as instructed in Step 5. <p>If the screw heads and cathodes are positive (indicating a correct count), dial the second, third and fourth correct digits to check the screw heads in rows B, C, and D, and the cathode of diodes CR4 through CR12. If all codes are counted correctly and the cathode of the diodes are positive, this indicates a fault in the reset circuit. Check the correct code, incorrect code reset and reset inhibit waveforms shown in Figure 17, and refer to the circuit analysis section for detailed operation and Truth Table for the reset circuitry.</p> <ol style="list-style-type: none"> 5. With the reset disable jumper connected, dial a "5" and check the input waveforms at TP5 and TP6 (see Fig. 18). If the waveforms are not correct, check the Tone Receiver Board or the envelope detector circuitry. <p>If the waveforms are correct, check to see if the flip-flops are switching (one output terminal at +6 volts ("1") and the other at zero ("0")). Refer to the circuit analysis of the Counter Board and the Truth Table on the Schematic Diagram (see Table of Contents).</p> <ol style="list-style-type: none"> 6. If the flip-flops are not switching properly (both output terminals at zero volts or both at +6 volts), remove all of the screws in the bit counter flip-flop or unsolder all of the diodes in the output of the digit counter and re-check the flip-flop output. If the flip-flop does not switch correctly, replace the IC module. <p style="text-align: center;">NOTE</p> <p>To remove an IC module, clip off all of the leads as close as possible to the body of the module. Then unsolder and remove one lead at a time, being careful not to pull the printed wiring away from the board.</p>
No tone output	<ol style="list-style-type: none"> 1. While applying 100 millivolts of on-frequency tone, dial a "5" and check the waveform at C3 (see Fig. 19). If the proper waveform is not present, check the Tone Receiver input circuitry. 2. With tone applied, dial a "5" and check the waveform at C10 (see Fig. 19). If the proper waveform is present, check CR6, CR7, CR8 and Q5. If the waveform is not correct, check for a sine wave across L1/L2. 3. If the sine wave is present across L1/L2, connect a jumper across L1/L2 and check for a near zero reading at the positive end of C10. If the reading is not near zero, check CR5, Q3 and Q4.
No tone output at high input levels, but operates normally at low input levels	Check C2, C3, CR3, CR4, R6 and R7 in the limiter circuitry.

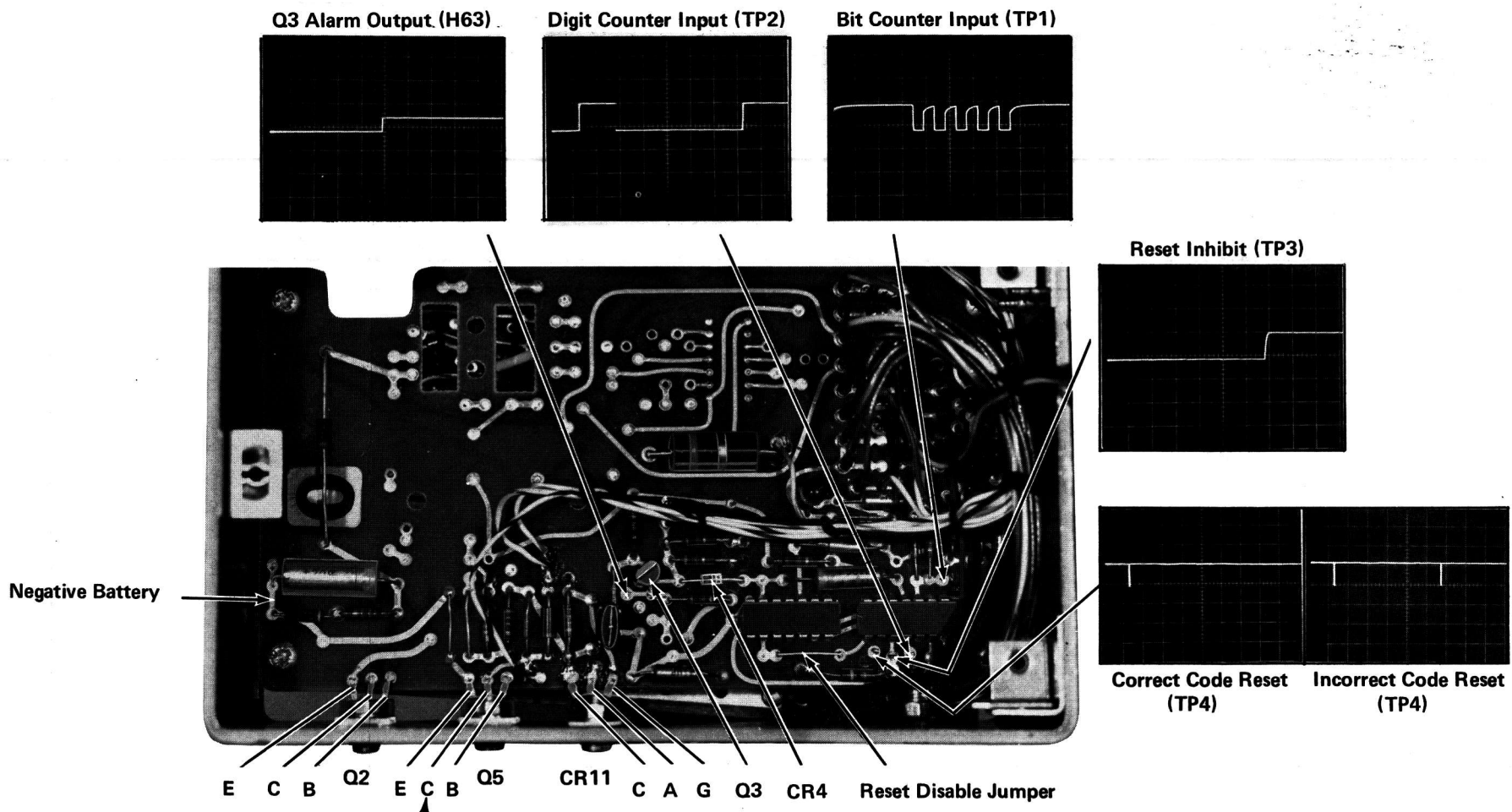
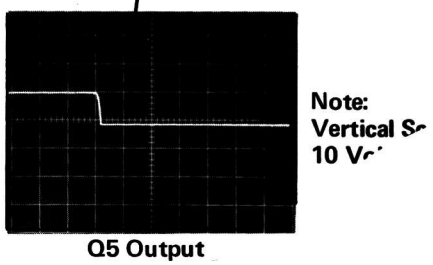


Figure 17 - Pulse Routing Board



Note: Vertical Scope Setting of 0.1 Volt/Div

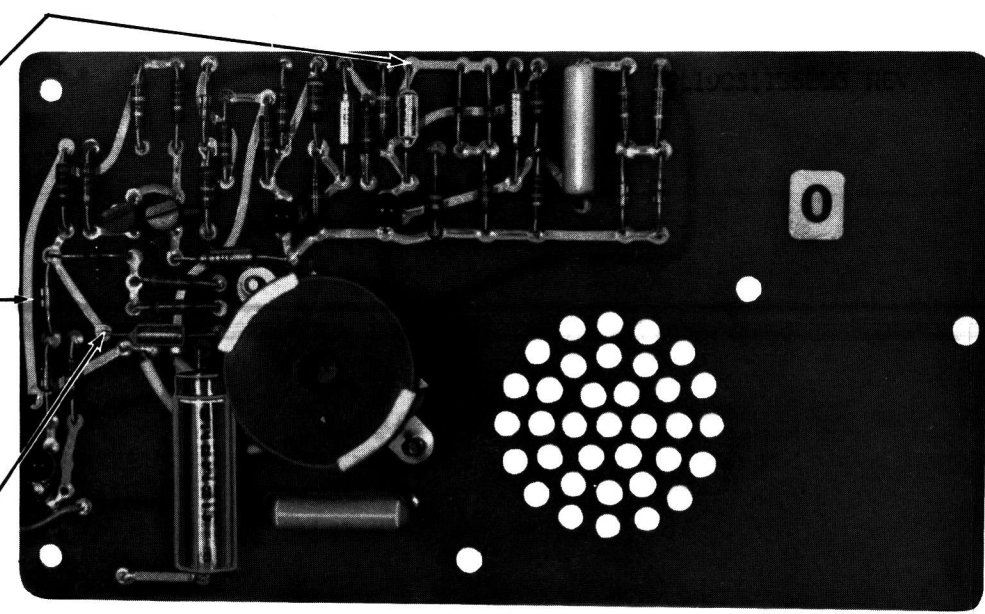
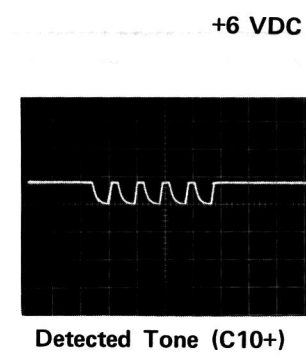
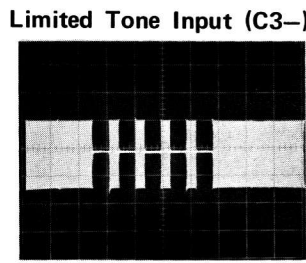


Figure 19 - Tone Receiver Board

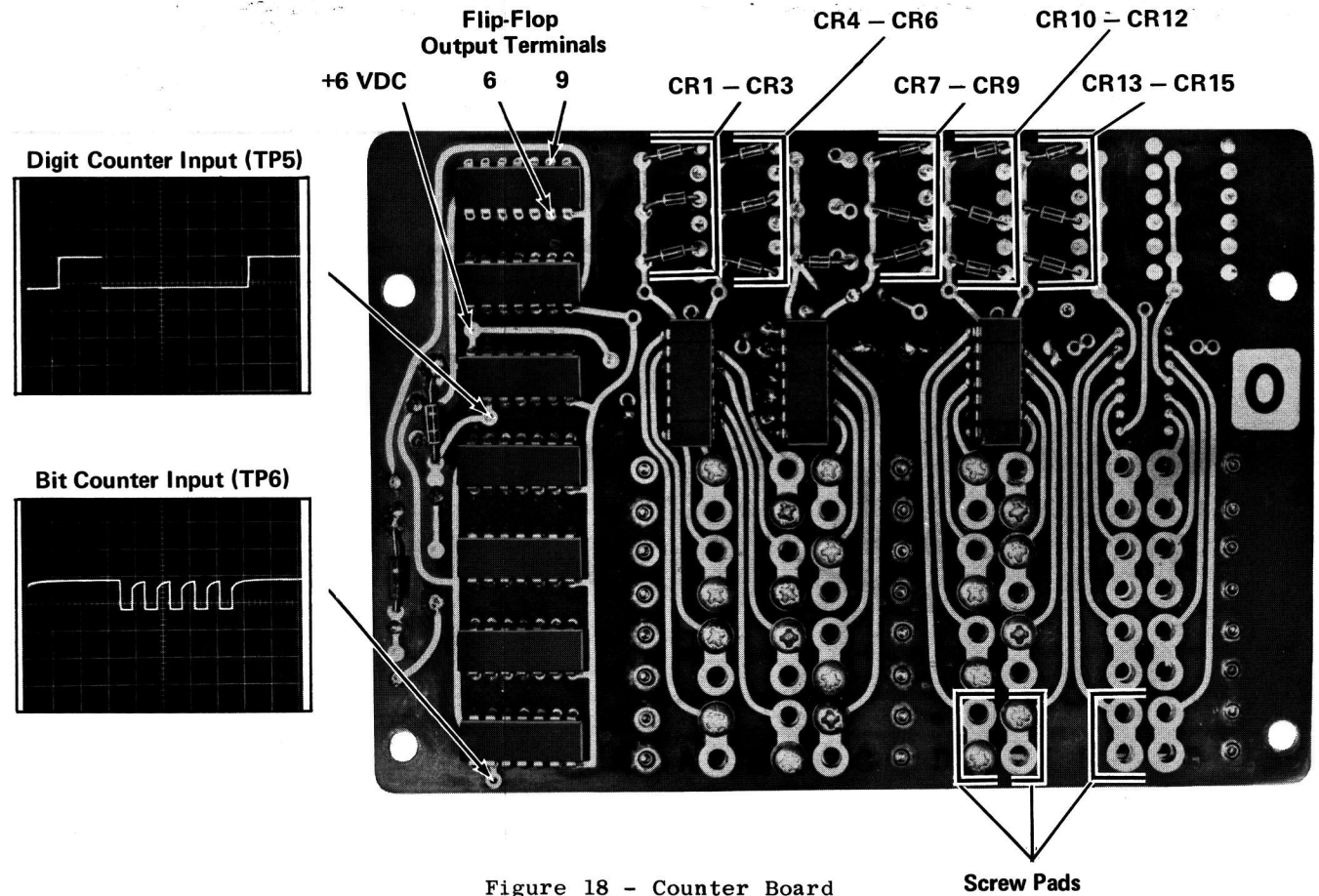
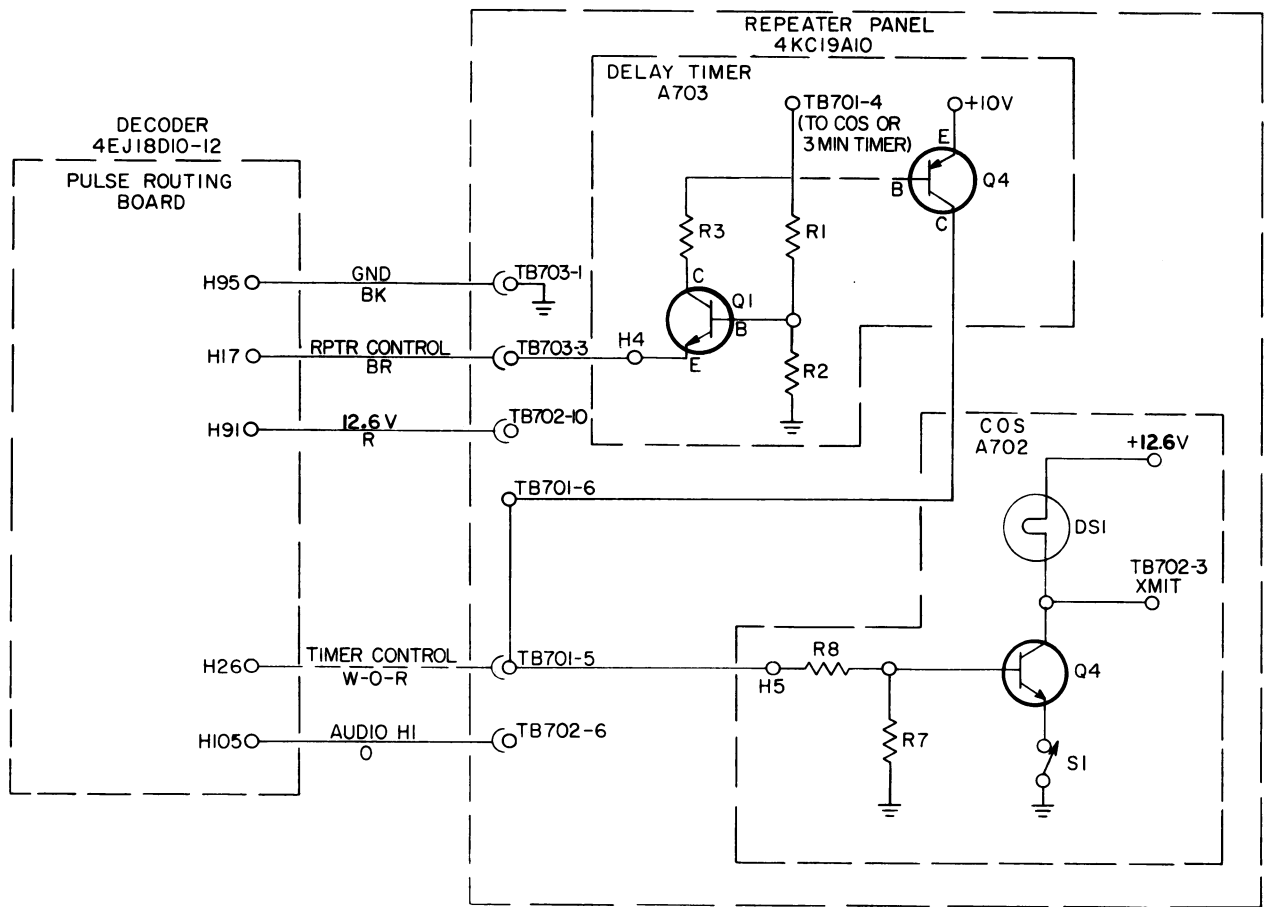
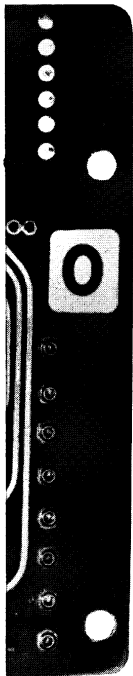


Figure 18 - Counter Board

TROUBLESHOOTING PROCEDURE

REPEATER CONTROL DIGITAL DECODER
MODELS 4EJ18D10-12

R13 R15



(19D413172, Rev. 3)

TROUBLESHOOTING PROCEDURE

REPEATER CONTROL DIGITAL DECODER
MODELS 4EJ18D10-12

DURE

TAT ECODER
D10-12

ORDERING SERVICE PARTS

Each component appearing on the schematic diagram is identified by a symbol number, to simplify locating it in the parts list. Each component is listed by symbol number, followed by its description and GE Part Number.

Service Parts may be obtained from Authorized GE Communication Equipment Service Stations or through any GE Radio Communication Equipment Sales Office. When ordering a part, be sure to give:

1. GE Part Number for component
2. Description of part
3. Model number of equipment
4. Revision letter stamped on unit

These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance.

Should further information be desired, or should particular problems arise which are not covered sufficiently for the purchaser's purposes, contact the nearest Radio Communication Equipment Sales Office of the General Electric Company.

MAINTENANCE MANUAL

LBI-4080

MOBILE RADIO DEPARTMENT
GENERAL ELECTRIC COMPANY • LYNCHBURG, VIRGINIA 24502

GENERAL  **ELECTRIC**

PRINTED IN U.S.A.

DF-5036