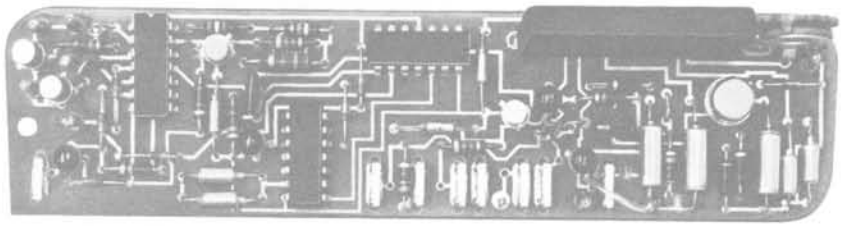
MOBILE RADIO

MAINTENANCE MANUAL

TWO FREQUENCY PRIORITY SEARCH LOCK MONITOR

Maintenance Manual LBI 4680 E
DATEFILE FOLDER - DF 8410

PRIORITY SEARCH LOCK MONITOR



SPECIFICATIONS *

Controls	Priority Squelch Adjust Search (ON-OFF)
Channel Search Rate	Four Times Per Second
Priority Sample Rate	6-7 Milliseconds
Priority Signal Override	20 dB quieting
Temperature Range	-40°C to 70°C (-40°F to +158°F)
Current Drain	45 mA maximum @ 13.8 VDC

*These specifications are intended primarily for the use of the serviceman. Refer to the appropriate Specification Sheet for the complete specifications.

GENERAL ELECTRIC

TABLE OF CONTENTS

WARNING

Although the highest DC voltage in the radio is supplied by the vehicle battery, high current may be drawn under short circuit conditions. These currents can possibly heat metal objects such as tools, rings, watchbands, etc., enough to cause burns. Be careful when working near energized circuits!

High-level RF energy in the transmitter Power Amplifier assembly can cause RF burns. KEEP AWAY FROM THESE CIRCUITS WHEN THE TRANSMITTER IS ENERGIZED!

Copyright © 1975, General Electric Company

DESCRIPTION

The General Electric Two Frequency Priority Search Lock Monitor Option consists of Option Kit 19A129567G5. (Variations in strapping of the Option Kit provide the three modes of operation.

The Option Kit (see Figure 1) is made up of the following components and is supplied factory installed, or may be field installed at a later date.

- Priority Search Lock Monitor Board 19C320453.
- Control Unit Nameplate NP270753P5.
- Option Switch with mounting hardware.
- Option Indicator (LED) and retainer clip.

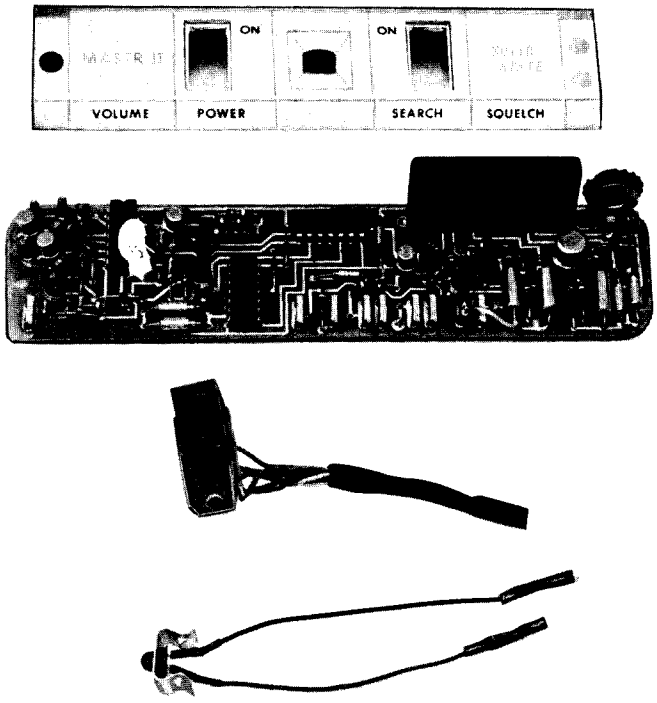


Figure 1

The PSLM board plugs into designated pins on the Control Unit printed wire board and contains the necessary circuitry to continuously and sequentially monitor any two channels of a multi-frequency receiver.

The two-frequency PSLM allows the user to select two of up to eight receive channels to be searched. Depending on the option employed either channel can be designated as the priority channel or when only two channels comprise a system the priority channel may be selected by the Frequency Selector Switch on the Control Unit.

The locked priority channel is selected by means of interconnecting straps in accordance with Table 1 of the Installation Instructions.

The PSLM assures reception of all signals on the priority channel regardless of the signal strength of the first signal received.

The three modes of operation are:

- Two Frequency Search-Selectable Priority
- Multi-Frequency Locked Priority-Selectable Non-Priority.
- Multi-Frequency Locked Non-Priority-Selectable Priority

When a signal is received on the priority channel, the PSLM stops searching and locks on the priority channel for the duration of the message. When a signal is received on the non-priority channel, the PSLM stops on that channel but continues to monitor the priority channel. If a signal is then received on the priority channel whose signal strength equals or exceeds 20 dB quieting, the PSLM reverts to the priority channel and locks for the duration of the priority message.

NOTE

The PSLM operates only when the receiver is squelched. When the receiver is unsquelched the PSLM will lock onto the active channel. If this should be the non-priority channel and a second signal is received the PSLM will revert to priority (locked) channel operation.

Channel Busy Indicator

The Channel Busy Indicator is a light emitting diode (LED) that turns on when a message is being received on the priority channel and flashes when a message is recevied on the non-priority channel.

Search Switch (S1701)

When the SEARCH Switch is in the On position, the PSLM alternately monitors the priority and non-priority channels and selects the appropriate channel when a message is received.

When the SEARCH Switch is on the "Off" position, the PSLM circuitry is disabled and messages are received and transmitted on the channel indicated by the Frequency Selector Switch on the Control Unit.

Operating the push-to-talk (PTT) Switch disables the PSLM circuitry and permits message transmissions on the frequency indicated by the Frequency Selector Switch. The Channel Busy Indicator is out when transmitting.

CIRCUIT ANALYSIS

The Priority Search Lock Monitor is fully transistorized using both discrete components and integrated circuits (IC's) to achieve maximum reliability. Discrete components are used in the Master Pulse Generator, Inverter, Channel Drivers, Transmit Revert, Lamp Driver, and Voltage Regulator circuits. IC's are used in the logic circuitry while hybrid circuits are employed for audio muting and squelch control.

References to symbol numbers mentioned in the following text may be found on the Block Diagram, Schematic Diagram, Outline Diagram or Parts List (see Table of Contents).

Supply voltage for the PSLM is provided from the vehicle ignition switch through Jack 701-11 and the power ON-OFF Switch. A voltage regulator on the PSLM board provides +9.5 V to the PSLM muting and squelch circuit hybrid U1704 and to the Master Pulse Generator. Regulated +5 V is supplied to the logic circuits.

MASTER PULSE GENERATOR

The Master Pulse Generator generates the timing pulses required to permit searching the selected channels and to permit monitoring the priority channel while receiving on the non-priority channel. The Master Pulse Generator consists of unijunction transistor Q1701, resistors R1701-R1704 and capacitor C1701.

When power is applied to the circuit C1701 charges up and causes Q1701 to conduct (emitter to base 1). This quickly discharges C1701 causing Q1701 to stop conducting until C1701 again charges up through R1701 and R1702. This cycle is repeated as long as power is applied. The value of R1701 is selected to provide a frequency of 8 Hz. (A pulse every 125 milliseconds).

The output of the Master Pulse Generator is applied to two IC's (U1701-A and U1702-C) to provide timing pulses required for different modes of operation. The PSLM sample rates and times discussed in the different modes of operation assures the reception of the first syllable of a message received on either channel, and to assure full intelligibility of messages received on the non-priority channel. Figure 2 is a Functional Block Diagram of the PSLM and also shows the primary signal interconnections required for normal operation.

TWO FREQUENCY SEARCH, SELECTABLE PRIORITY

Operation of the PSLM can be divided into three modes:

- Receiver Squelched
- Receiving Priority Channel
- Receiving Non-Priority Channel

Receiver Squelched

When the receiver is squelched (no signal applied), the PSLM alternately monitors each channel four times per second for a duration of 125 milliseconds. A typical Timing Diagram for this mode of operation is shown in Figure 3.

The base of Inverter Q1703 is connected to the CAS Buffer Switch in the receiver. When the receiver is squelched the base of Q1703 is near ground potential keeping the transistor turned off. When turned off the collector of Q1703 is high permitting the Search Control Gate (U1702-G) to trigger the Channel FF under control of the Master Pulse Generator. The Channel FF is triggered every 125 milliseconds and alternately turns on the F1 and F2 drivers. The drivers are turned on when their base voltage is positive and turned off when the base voltage approaches zero. When turned on, the driver applies A- to the associated receiver ICOM to monitor that channel during the time it is being searched.

A- is also applied to the set direct (SD) input of FF U1701-A causing it to remain in the true state (pin 8 high, pin 9 low) until a signal is received. So long as the SD input is held low the output of Priority Sample Control GATE 2 remains high. Since the Priority Sample Pulse Generator operates only when GATE 2 changes state, it is disabled when the receiver is squelched.

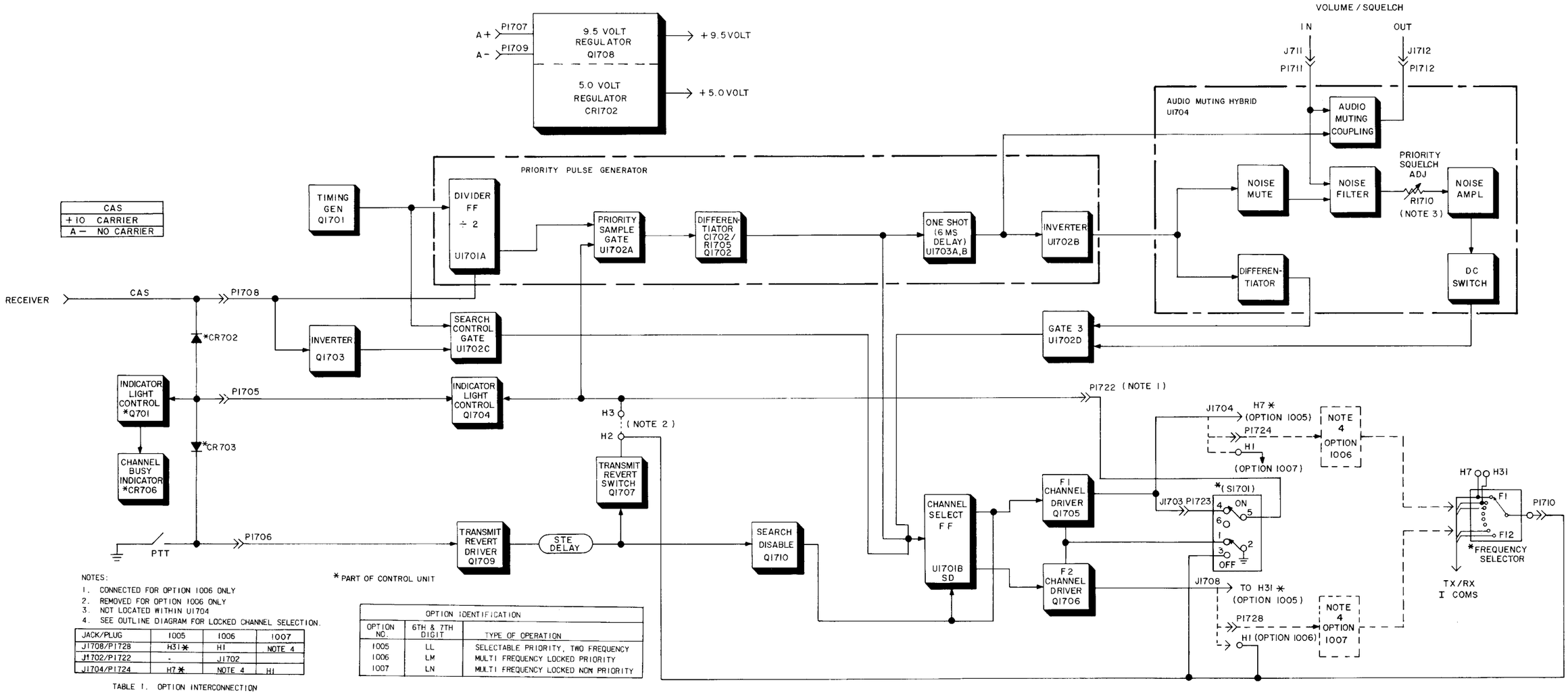
The Channel Busy Indicator is biased off during this mode of operation due to A- being applied from the carrier activity sensor line (CAS) to the base of Q701. A- is present on the CAS line when a carrier signal is not being received.

Receiving Priority Channel

This mode of operation allows the user to select the priority channel via the Frequency Selector Switch on the Control Unit. The circuit description below assumes F1 as the priority channel.

When a carrier signal is received on the priority channel, the PSLM locks on that channel for the duration of the message. A typical Timing Diagram for this mode of operation is shown in Figure 4.

Receiving a carrier signal on the F1 Channel unsquelches the receiver and applies +10 V to the base of Inverter Q1703, turning it on. When turned on, the collector of



NOTES:
1. CONNECTED FOR OPTION 1006 ONLY
2. REMOVED FOR OPTION 1006 ONLY
3. NOT LOCATED WITHIN U1704
4. SEE OUTLINE DIAGRAM FOR LOCKED CHANNEL SELECTION.

JACK/PLUG	1005	1006	1007
J1708/P1728	H31*	H1	NOTE 4
J1702/P1722	-	J1702	
J1704/P1724	H7*	NOTE 4	H1

TABLE 1. OPTION INTERCONNECTION

* PART OF CONTROL UNIT

OPTION IDENTIFICATION		
OPTION NO.	6TH & 7TH DIGIT	TYPE OF OPERATION
1005	LL	SELECTABLE PRIORITY, TWO FREQUENCY
1006	LM	MULTI FREQUENCY LOCKED PRIORITY
1007	LN	MULTI FREQUENCY LOCKED NON PRIORITY

Figure 2 - PSLM Block Diagram

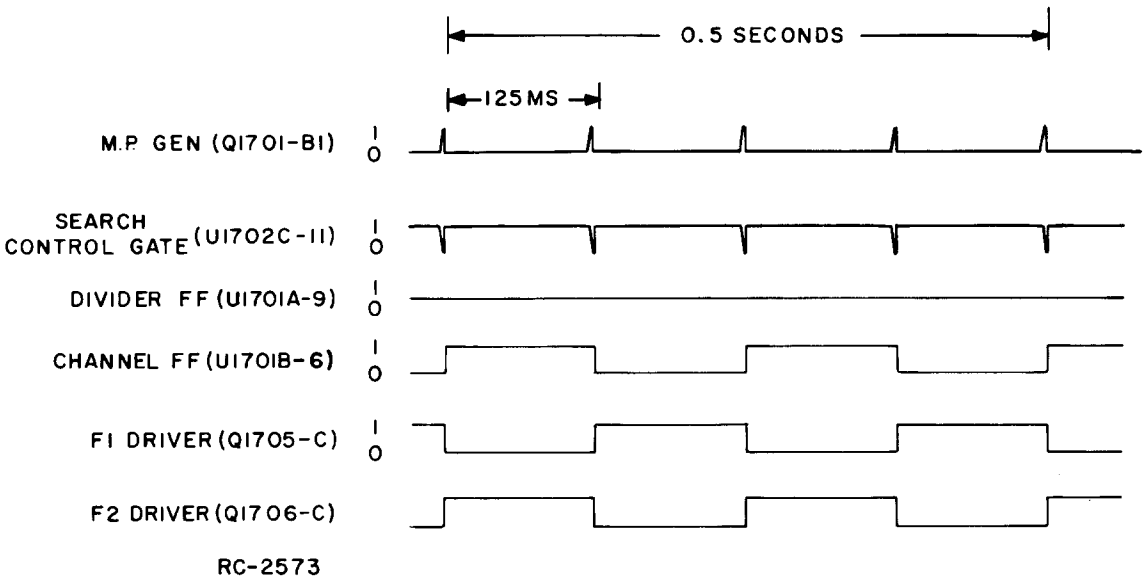


Figure 3 - Receiver Squelched

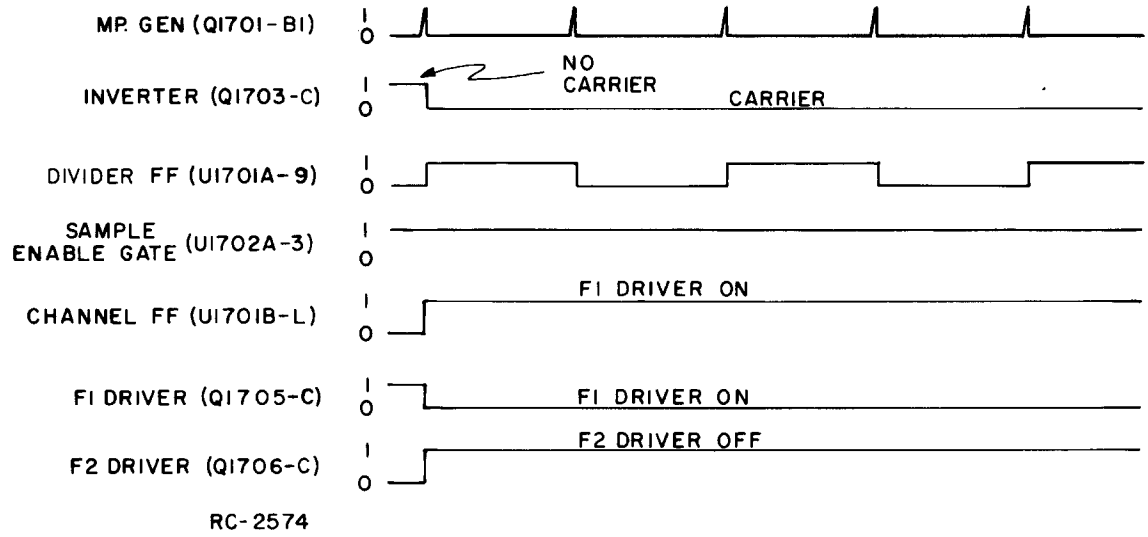


Figure 4 - Receiving Priority Channel

Inverter Q1703 drops to ground potential and disables the Search Control Gate (Gate 1) thereby preventing the Master Pulse Generator from triggering the Channel Select FF. The output of Search Control Gate 1 remains high as long as a carrier signal is received. Additionally the "0" level applied to the SD output of divider FF U1701A is removed and a 250 millisecond square wave is applied to Priority Sample Control Gate 2. Gate 2, however, is disabled by A- applied through the Frequency Select Switch from Channel Driver F1 (1705-C). This disables the Priority Sample Pulse Generator and prevents it from triggering the Channel FF.

The Channel Busy Indicator is turned on when receiving the priority channel. During this time A- is applied to the base of Q1704 turning it off and removing A- from the base of Q701 allowing the base of Q701 to go positive, turning it and the Channel Busy Indicator "on".

Receiving Non-Priority Channel

When a signal is received on the non-priority channel, the PSLM stops on that channel while monitoring the priority channel. The priority channel is monitored for 6-7 milliseconds at approximately 250 millisecond intervals (four times per second). If a signal is received on the priority channel while receiving the non-priority channel, the PSLM will transfer operation from the non-priority channel to the priority channel for the duration of the message. A typical

Timing Diagram for this mode of operation is shown in Figure 5.

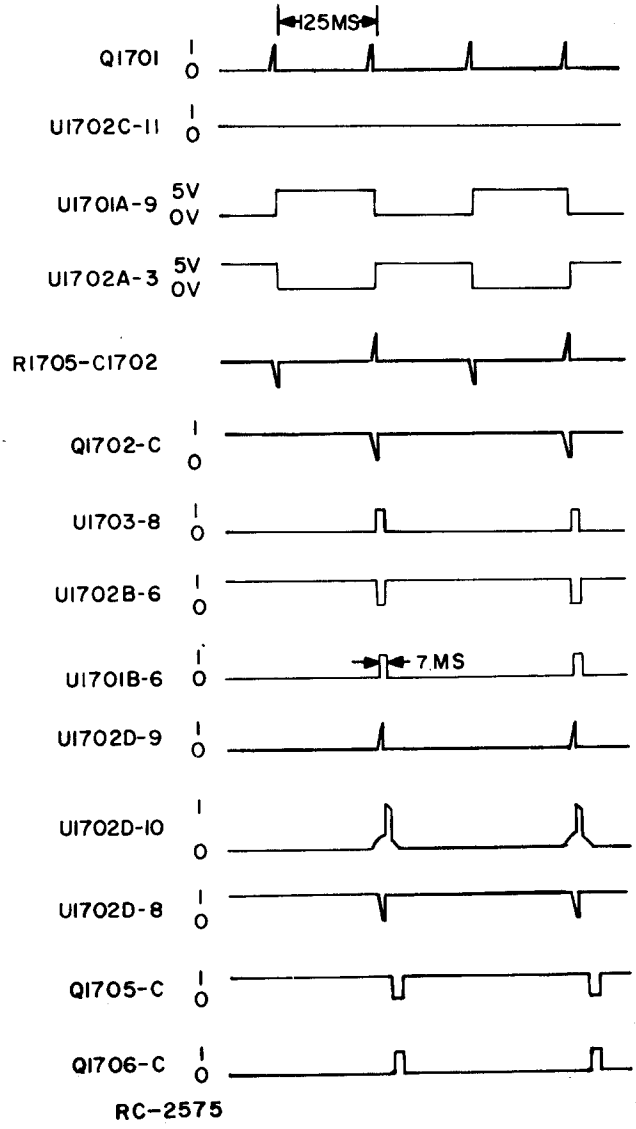


Figure 5 - Receiving Non-Priority Channel

Assume that F2 is the non-priority channel. Receiving a signal on the F2 channel turns on Inverter Q1703. The collector of Q1703 goes low, disabling Search Control Gate 1. The output of the Search Control Gate goes high locking the Channel FF to Channel Driver F2 for the duration of the message or until a 20 dB quieting signal is received on the priority channel. The F2 driver, Q1706, stays on and applies a constant ground to the associated receiver ICOM, to assure continuous reception of the message. Channel Driver F1 is turned off during this time. In addition, Divider FF U1701A is enabled and applies a 250 millisecond square wave to Priority Sample Control Gate 2.

In this mode of operation A- from the F2 Driver is not returned through the Frequency Selector Switch to the input of Priority Sample Control Gate. Gate 2 therefore is enabled allowing the Priority Sample Pulse Generator to generate a seven millisecond pulse four times a second. The Priority Sample Pulse Generator consists of U1701A, U1702A & B, Q1702, U1703A & B, C1703, C1708 and differentiator C1702 and R1705. C1703 and C1708 determine the width of the priority pulse. The values of C1703 and C1708 are selected to provide a sample time of seven milliseconds. The priority sample pulse is generated coincident with the normal turn on time of the F1 Channel Driver when the PSLM is searching both channels. This enables the PSLM to monitor the priority channel while receiving on the non-priority channel.

The output of Gate 2 is differentiated by C1702 and R1705 (see Figure 5) and the pulses are applied to the base of Q1702. As Q1702 is an NPN transistor, only the positive pulses (applied every 250 milliseconds) cause the transistor to conduct. When it conducts, the negative-going output pulse at its collector forward biases CR1701 and switches the Channel FF to the priority channel. The output of Q1702 also activates One-Shot Time Delay U1703 which provides a seven millisecond positive output pulse. The output pulse is simultaneously applied to the audio muting circuit in U1704 and to Inverter U1702B.

In the audio muting circuit, audio and noise from the emitter of audio-noise amplifier in the receiver is connected to P1711 on the PSLM board. The audio is normally coupled through Pin 3 on U1704. C3, R4, C2 and Emitter Follower Q4, and then connected from Pin 4 on U1704 to P1712 on the PSLM board. Refer to Figure 6 for a Simplified Diagram of PSLM Audio Mute Hybrid U1704.

The positive pulse from the One-Shot turns on Q2 and then Q3 for a total time of eight milliseconds. When turned on, the collectors of Q2 and Q3 drop to A-, shunting the receiver audio path. This prevents objectionable noise bursts from being heard at the speaker each time the priority channel is monitored.

At the same time the audio is muted, the output of the One-Shot is inverted and applied to Squelch Muting Transistor Q5 and to Differentiator Q1.

The fast squelch circuit consists of Q5 through Q8. When the priority channel is not being monitored, audio and noise applied to the fast squelch circuit is shunted to ground by normally-on transistor Q5. When the Channel FF is switched to the priority channel, the negative-going output of the seven millisecond One-Shot is applied

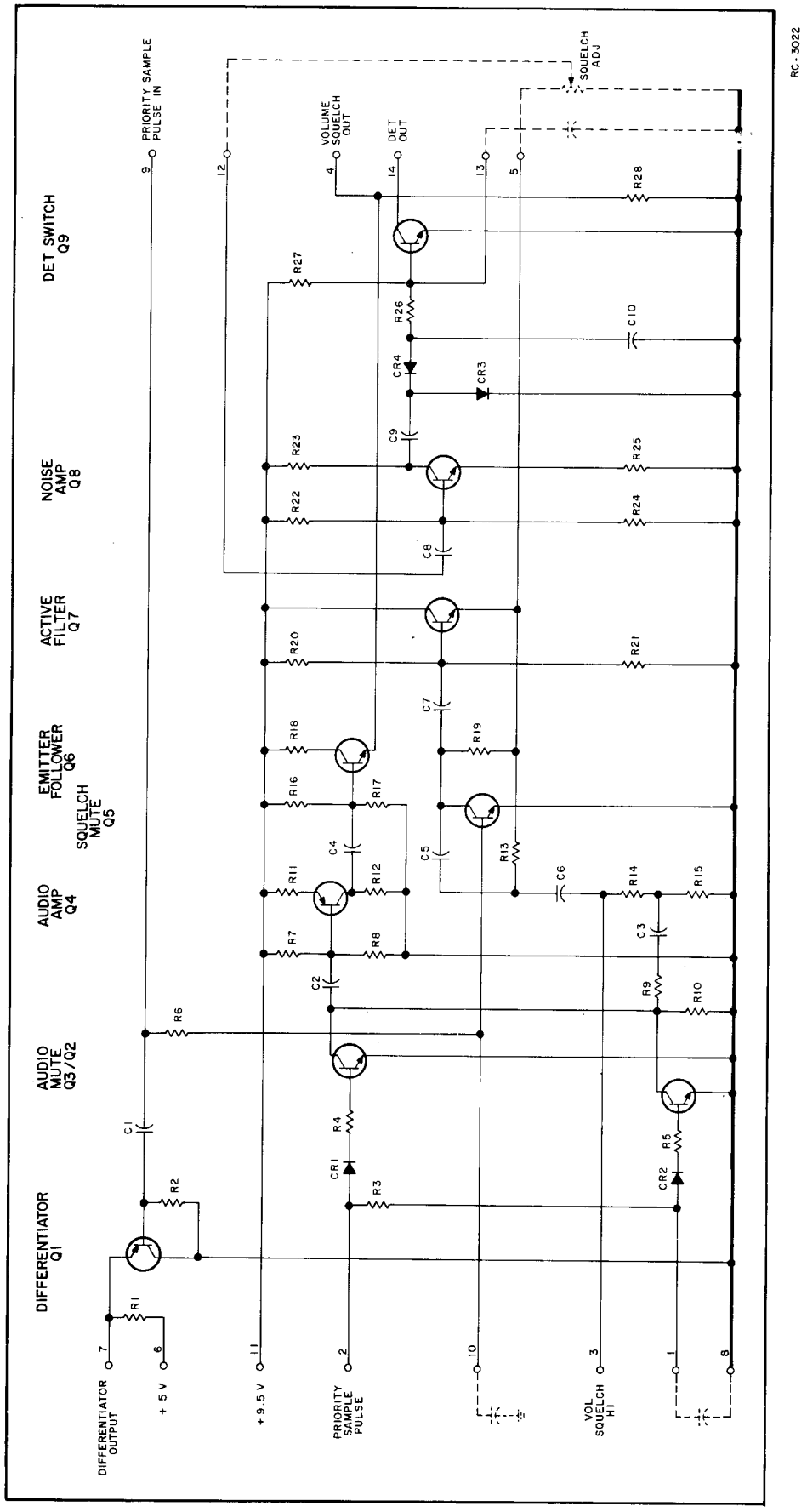


Figure 6 - Typical PSLM Mute Hybrid U1704

to the base of Q5 turning the transistor off. While Q5 is turned off, the noise output of the active high-pass noise filter is applied to the base of Noise Amplifier Q7. The filter consists of C4, C5, C6, R9 and R10, Squelch Adjust potentiometer R1710 and Q11. Instructions for setting R1710 are listed in the Table of Contents.

The output of Q7 is rectified by CR3 and CR4 and the resultant negative voltage turns off DC Switch Q8. Turning off Q8 removes the ground at the input of Gate 3 (U1702D) thereby allowing it to pass the priority pulse.

While Q8 is turned off, the output of the Inverter UC1702B is differentiated by C1 and R21 (see Figure 6), and the positive-going pulse turns off PNP Transistor Q1. Turning off Q1 applies a "1" to the remaining input of Gate 3, switching the output to a "0". The "0" triggers the Channel FF, causing it to switch back to the non-priority channel. The entire cycle is repeated every 250 milliseconds until a carrier signal with a strength of 20 dB quieting or more is received on the Priority Channel or for the duration of the message.

If a signal is received on the priority channel during the seven millisecond monitor period, the signal quiets the receiver.

With the receiver quieted, there is insufficient noise to operate the fast squelch circuit so that Q6 remains on (its collector at ground potential). A- at the collector of Q8 blocks Gate 3, while A- from Q1705 collector is applied back through the Frequency Selector Switch to disable Priority Sample Control Gate 2. With both gates 2 and 3 disabled, the Channel FF remains locked on the priority channel for the duration of the message.

The Channel Busy Indicator will flash on when receiving messages on the non-priority channel. Since messages are now being received on the non-priority channel, A- is removed from the base of Indicator Light Control Transistor Q1704, allowing Q1704 to turn on. Q1704 then applies A- to the base of Q701 which turns off and keeps the Channel Busy Indicator off. However, when the priority sample pulse is generated and the priority channel sampled, A- is applied to the base of Indicator Light Control Transistor Q1704 turning it off for the duration of the priority sample pulse (7 milliseconds). During this time A- is removed from the base of Q701 which allows it to turn on and to turn on the Channel Busy Indicator.

PRIORITY DISABLE

The PSLM can also be modified to operate without priority for any channel. To disable the priority function of the PSLM and revert to Search Lock Monitor operation remove C1702 in the PSLM Priority Sample Pulse Generator.

TRANSMIT REVERT MODE

When operating in the Transmit Revert Mode (PTT switch depressed) the Transmit Revert circuits within the PSLM disable the Priority Pulse Generator, the F1 and F2 Channel Drivers and turn off the Indicator Light Control. Messages are transmitted on the channel selected by the Frequency Selector Switch.

Operating the PTT switch pulls the base of Transmit Revert Driver Q1709 low, turning it on. Q1709 in turn applies A+ to Transmit Revert Switch Q1707 and DC Switch Q1710, turning both transistors on.

The Transmit Revert Switch applies A- to Indicator Light Control Q1704, Priority Sample Control Gate 2 U1702A and the Frequency Select Switch common lead, turning off the Indicator Light Control, disabling the Priority Sample Pulse Generator. The transmit frequency is determined by the Frequency Selector Switch.

DC switch Q1710 applies A- to the set direct (SD) input of the Channel FF and to the base of Channel Driver F1. When A- is applied to the SD input of the Channel FF the Q and $\overline{Q}$ outputs are "1" and "0" respectively. This, then, turns off the F2 Channel Driver. Under this condition, when the PTT switch is operated, both channel drivers are off and the PSLM is disabled.

When the PTT switch is released a delay of approximately 250 milliseconds, due to the discharge of C1711 through R1715 and the base emitter junction of Q1710 and through R1702 and the base emitter junction of Q1707 allows the Transmit Revert Driver Q1709 to keep the transmit frequency selected. This is required to allow for the Squelch Tail Elimination delay, when Channel Guard is used. To eliminate the delay when Channel Guard is not used remove the DA wire between H4 and H5.

VOLTAGE REGULATOR

The Voltage Regulator, consisting of Q1708 and associated circuitry, provides +9.5 V and +5.0 V to the PSLM circuits. Transistor Q1708 is a series regulator whose base emitter voltage is held constant by zener diode CR1704. Q1708 can be considered as a voltage controlled variable resistor whose resistance varies with a change in collector voltage.

With the base emitter voltage constant, a drop in collector voltage will cause Q1708 to conduct harder thereby reducing the voltage drop across the emitter and maintain a constant +9.5 V at collector. Conversely, an increase in collector voltage will decrease conduction of Q1708 which effectively increases the series resistance and prevents the emitter voltage from rising.

Zener diode CR1702 connected across the +9.5 V regulator through a series resistor provides a regulated +5 V output to the various logic circuits in the PSLM.

Two Frequency Selectable Priority was discussed above; therefore, the following description is limited to the circuit differences for option 1006 and 1007.

MULTI FREQUENCY LOCKED

This mode of operation permits the user to designate any one of eight channels as the locked priority channel and to select, at will, any of the remaining channels as the non-priority channel to be searched by setting the Frequency Selector Switch to the desired channel.

NOTE

Only two channels may be searched-- the priority and non-priority.

Locked priority is achieved by strapping the collector of Channel Driver (F1) to the Frequency Selector Switch in accordance with Table 1 on the Schematic Diagram.

Channel Driver F2 is connected via H1 to the wiper (common) of the Frequency Selector Switch to permit selection of the non-priority channel.

When a message is received on the priority channel the collector of F1 Channel Driver goes low and applies A- to the Priority Sample Control Gate and to Indicator Light Control Q1704. This inhibits operation of the Priority Pulse Generator and turns on the Channel Busy Indicator. The SEARCH Control Gate is disabled by the CAS signal applied to Inverter Q1703. Disabling these two gates, inhibits operation of the Channel FF and causes the Channel FF to lock on to the priority channel.

When a message is received on the non-priority channel (selected by the Frequency Selector Switch) A- is applied from the collector of Channel Driver F2 to the selected non-priority receiver ICOM through the Frequency Selector Switch. The Search Control Gate is disabled by the CAS signal, however, the Priority Sample Gate is enabled due to the absence of A- from the F1 Channel Driver. Under these conditions, a priority sample pulse is generated four times per second and applied to the Channel FF to permit monitoring the priority channel.

When the priority channel is monitored, F1 Channel Driver Q1705 turns on for six milliseconds and applies A- to the Indicator Light Control via contacts 4 and 5 of S1701 causing the Channel Busy Indicator to flash. Additionally A- is applied to the Priority Sample Control Gate to disable it during the monitor period.

If a message is received on the priority channel while receiving on the non-priority channel, the Priority Sample Gate remains disabled preventing the Channel FF from reverting back to the non-priority channel.

NOTE

If the Frequency Selector Switch is set to the Priority Channel, the PSLM will appear not to search. Under these conditions the collectors of both Channel Drivers are connected together through the Frequency Selector Switch, thus the Priority Channel is monitored as if manually selected.

MULTI FREQUENCY LOCKED NON-PRIORITY

This mode of operation is similar to the locked priority mode except that the locked non-priority channel is assigned by strapping the collector of non-priority Channel Driver F2 instead of Channel Driver F1 to the Frequency Selector Switch in accordance with Table 1 on the Schematic Diagram. The priority channel is then selected by setting the Frequency Selector Switch to one of the remaining channels as desired. Again, only two channels may be searched -- the priority and the non-priority.

Channel Driver F1 is connected via H1 to the wiper (common) of Frequency Selector Switch to permit selection of the priority channel. Channel Driver F2 is connected to the desired non-priority channel in accordance with Table 1.

When a message is received on the priority channel, Q1705 turns on and its collector goes low, applying A- to the Priority Sample Control Gate and to Indicator Light Control Q1704. This inhibits operation of the Priority Pulse Generator and turns on the Channel Busy Indicator. The Search Control Gate is disabled by the CAS signal. Disabling these two gates inhibits operation of the Channel FF causing it to lock onto the selected priority channel.

When a message is received on the locked non-priority channel, A- is applied from the collector of Channel Driver F2 directly to the receiver ICOM. The search Control Gate is disabled by the CAS signal; however, due to the absence of A- from Channel Driver F1 the Priority Sample Control Gate is enabled. Under these conditions the priority sample pulse is generated four times a second to permit monitoring the priority channel.

When the priority channel is monitored, F1 Channel Driver Q1705 turns on for six milliseconds and applies A- to the Indicator Light Control causing the Channel Busy Indicator to flash.

If a message is received on the priority channel while receiving on the non-priority channel, the Priority Sample Control Gate remains disabled, preventing the Channel FF

from reverting operation to the non-priority channel.

NOTE

If the Frequency Selector Switch is set to the locked non-priority channel the PSLM will appear not to search. Under these conditions the collectors of both Channel Drivers are connected together through the Frequency Selector Switch, thus, the Priority Channel is monitored as if manually selected.

FIELD INSTALLATION

The following instructions can be used to install the PSLM board in a multi-frequency Control Unit that is not equipped with any other option boards.

Control Unit Models:

19A129576G1 (Common Kit)
19A129578G1 (1-thru 8-Frequency Kit)
19A129578G2 (1-thru 12-Frequency Kit)

Installation of the PSLM Option Kit in this model requires that the Control Unit printed wiring board (PWB) be removed from the Control Unit. This is necessary in order to cut the applicable points on the Control Unit PWB. Proceed as follows:

a. Remove the two screws on the bottom of the front edge of the Control Unit and lift off the top cover.

b. Remove the two screws securing the microphone jack.

c. Remove the screw between J701 and J702, and the screw between J702 and J703.

d. Remove the screw at each end of the switch and control mounting bracket.

e. Remove the screw securing the Power-On switch (S701) to the Control Unit housing, then swing the board up from the front and lift out.

f. Remove the printed wiring board from the Control Unit and cut the printed wiring run at Points F and G. Refer to the Control Unit Maintenance Manual for the location of the specified points.

g. Re-install the board assembly in the Control Unit, but do not replace the top cover at this time.

h. Follow Step 1 through Step 6 to complete the installation.

Control Unit Models:

19D423590G3, 4 & 5

Installation of the PSLM Option Kit in this Control Unit model requires the following:

a. Remove the two screws on the bottom of the front edge of the Control Unit and lift off the top cover.

b. On the Control Unit printed wire board, cut DA jumpers "F" (H55 to H56) and "G" (H53 to H54). Refer to the Control Unit Maintenance Manual for the location of specified jumpers.

c. Follow Step 1 through Step 6 to complete the installation.

STEP 1: Position the PSLM component board assembly in the guide slots located inside the sides of the Control Unit housing. Gently insert the board assembly into the Control Unit, making sure that the connectors on the board assembly mate correctly with the square pins of the Control Unit printed wire board.

STEP 2: Mount the SEARCH Switch (S1701) in the space provided in the Control Unit. Orient the switch as shown on the Outline Diagram. Secure the switch to the control mounting bracket with the 4-40 x 1/4 inch Phillips head POZIDRIV® tap screw provided. Secure the other end of the switch to the Control Unit housing with the 4-40 1/4 inch Phillips head tap screw provided.

STEP 3: Position the LED (CR706) in the front indicator slot of the Control Unit housing and secure in place with the spring clip provided.

STEP 4: Make LED and switch connections as indicated in the connection chart on the outline diagram.

STEP 5: Remove the existing nameplate from the Control Unit top cover and install new Nameplate (NP270753P5) as follows:

a. Viewing the Control Unit from the front, note that there are only three of the plastic Nameplate tabs which lock in place. These are the top left hand tab, the top right hand tab and the bottom center tab. The remaining tabs function only as guide tabs.

b. Release the locking action of the tabs, starting with the top right hand tab, then the top left hand tab. Apply pressure with fingers or use a small flat blade screwdriver to release tabs. Push released tabs up through slots to prevent relocking of tabs.

c. Release the locking action of the bottom center tab and pry the nameplate loose from the top cover. The old nameplate will not be used with the PSLM Option.

d. Install the new nameplate.

STEP 6: Replace the Control Unit top cover and secure in position with the two screws previously removed.

MAINTENANCE

PRIORITY SQUELCH ADJUSTMENT

Priority Squelch Adjust R1710 was set at the factory for 20 dB quieting sensitivity on the priority channel, and will normally require no further adjustment. If it should become necessary to set R1710, use the following procedure. A signal generator (M560 or equivalent) with a 6 dB pad is required.

1. Set the Frequency Selector Switch to a non-locked frequency position and the SEARCH-OFF switch to the SEARCH position.

2. Alternately squelch and unsquelch the receiver until the PSLM stops on the non-priority channel. The PSLM searches when the receiver is squelched and may lock on either the priority or non-priority channel when the receiver is unsquelched. Therefore, several attempts may be required to stop the PSLM on the non-priority channel. Make sure that the PSLM is stopped on the non-priority channel by verifying that the Channel Busy Light on the Control Unit flashes.

3. Next apply a signal on the priority channel from the signal generator. Increase the signal generator output until the receiver switches to the priority channel. This should be at the 20 dB quieting level as measured previously.

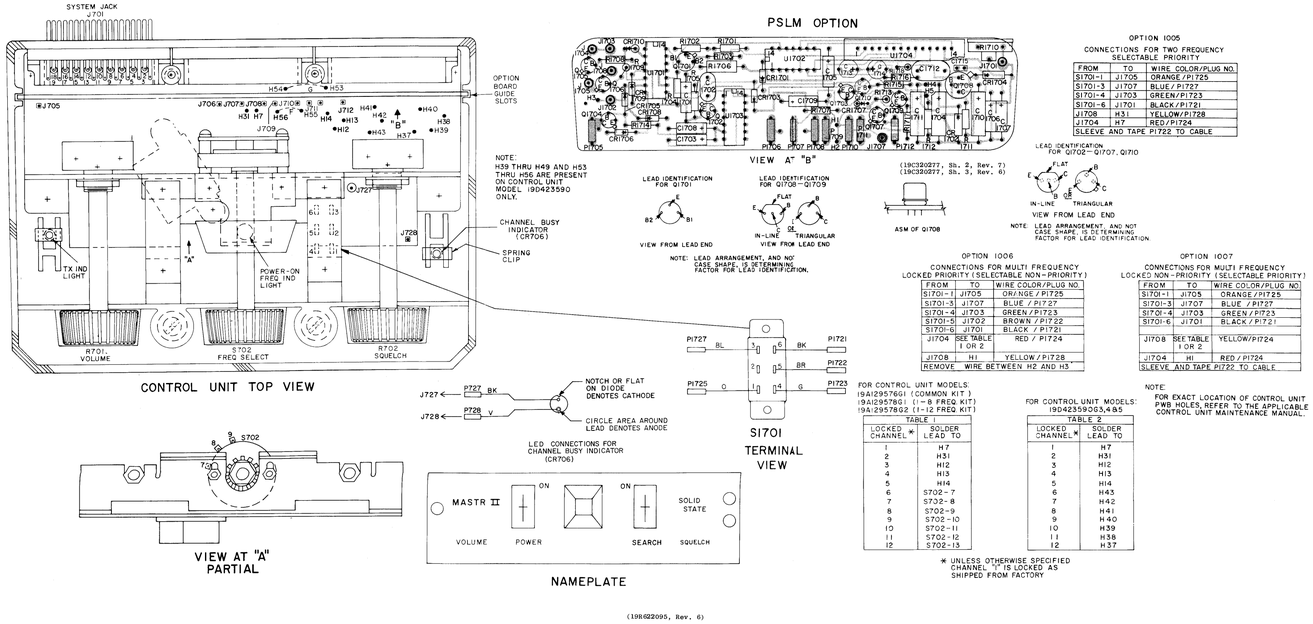
4. If necessary, adjust the Priority Squelch Control R1710 until the PSLM switches channels at the 20 dB level. Check all channels for this same function.

GENERAL ELECTRIC COMPANY • MOBILE COMMUNICATIONS DIVISION
WORLD HEADQUARTERS • LYNCHBURG, VIRGINIA 24502 U.S.A.

GENERAL ELECTRIC* U.S.A.

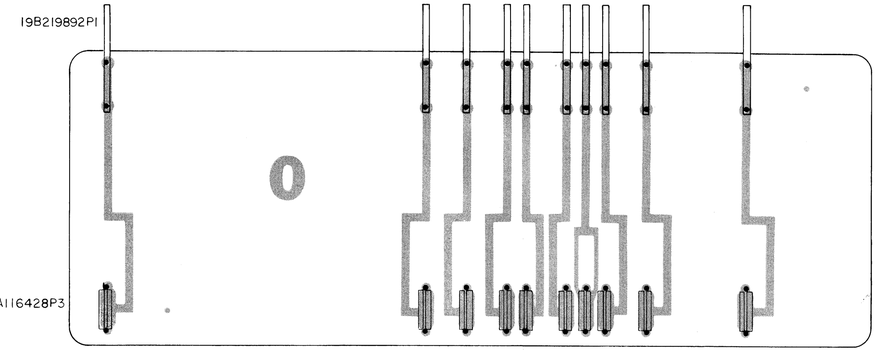
 (Page 11 is blank)

* Trademark of General Electric Company U.S.A.
Printed in U.S.A.

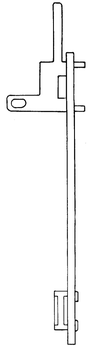


OUTLINE DIAGRAM

TWO FREQUENCY PRIORITY
SEARCH LOCK MONITOR



(19C321356, Rev. 1)
(19C320590, Sh. 2, Rev. 0)
(19C320590, Sh. 3, Rev. 0)



OUTLINE DIAGRAM

EXTENDER BOARD 19C320588G1

PARTS LIST

LBI4676C

TWO FREQ PRIORITY SEARCH LOCK MONITOR

SYMBOL	GE PART NO.	DESCRIPTION
		CONTROL UNIT MODIFICATION KIT 19A129567G5
		- - - - - - - DIODES AND RECTIFIERS - - - - - -
CR706	19B219800G2	Diode assembly: light emitting, red.
		SWITCH ASSEMBLY 19B219956G1
		- - - - - - - - - - PLUGS - - - - - - - - - -
P1721 thru P1723	4029840P2	Contact, electrical: sim to Amp 42827-2.
P1725	4029840P2	Contact, electrical: sim to Amp 42827-2.
P1727	4029840P2	Contact, electrical: sim to Amp 42827-2.
		- - - - - - - - - - SWITCHES - - - - - - - - - -
S1701	19A116622P4	Push: DPDT, 2 position, .5 amp at 125 VDC, 3 amps at 125 VAC; sim to Switchcraft 11K187.
		- - - - - - - - - - MISCELLANEOUS - - - - - - - -
	19B201074P204	Tap screw, Phillips POZIDRIV®: No. 4-40 x 1/4.
	N117P9004C6	Tap screw, phillips: No. 4-40 x 1/4.
	19A116807P1	Clip, spring tension.
	NP270753P5	Nameplate.
		COMPONENT BOARD 19C320453G1
		- - - - - - - - - - CAPACITORS - - - - - - - - - -
C1701	5496267P213	Tantalum: 2.2 µf ±10%, 20 VDCW; sim to Sprague Type 150D.
C1702	19A116080P5	Polyester: 0.047 µf ±20%, 50 VDCW.
		NOTE: The value of C1703 (if required) is selected to provide a priority channel sample time of 6 milliseconds.
C1703A	5496267P417	Tantalum: 1.0 µf ±5%, 35 VDCW; sim to Sprague Type 150D.
C1703B	19B200240P15	Tantalum: 1.8 µf ±5%, 20 VDCW.
C1703C	5496267P413	Tantalum: 2.2 µf ±5%, 20 VDCW; sim to Sprague Type 150D.
C1704	5496267P10	Tantalum: 22 µf ±20%, 15 VDCW; sim to Sprague Type 150D.
C1705*	5496267P229	Tantalum: 0.68 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
		In REV A & earlier:
	5496267P228	Tantalum: 0.47 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C1706	5496267P29	Tantalum: 0.68 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C1707	5496267P27	Tantalum: 0.33 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
		NOTE: The value of C1708 (if required) is selected to provide a priority channel sample time of 6 milliseconds.
C1708A	5496267P227	Tantalum: 0.33 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C1708B	5496267P228	Tantalum: 0.47 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C1708C	5496267P229	Tantalum: 0.68 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C1708D	5496267P230	Tantalum: 0.82 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C1708E	5496267P217	Tantalum: 1.0 µf ±10%, 35 VDCW; sim to Sprague Type 150D.
C1708F	5496267P226	Tantalum: 0.22 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C1708G	5496267P224	Tantalum: 0.1 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C1709	5496267P228	Tantalum: 0.47 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C1710	5496267P10	Tantalum: 22 µf ±20%, 15 VDCW; sim to Sprague Type 150D.
C1711	5496267P218	Tantalum: 6.8 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C1712*	19A116080P7	Polyester: 0.1 µf ±20%, 50 VDCW. Added by REV A.
C1713* and C1714*	19A134202P6	Tantalum: 22 µf ±20%, 15 VDCW. Added by REV E.
C1715*	19A116192P2	Ceramic: 470 pf ±20%, 50 VDCW; sim to Erie 8111-A050-W5R-471M. Added by REV E.
		- - - - - - - DIODES AND RECTIFIERS - - - - - -
CR1701	19A115250P1	Silicon, fast recovery, 225 mA, 50 PIV.
CR1702	4036887P56	Silicon, Zener: 500 mW, 5.0 v. nominal.
CR1703	19A115250P1	Silicon, fast recovery, 225 mA, 50 PIV.
CR1704	4036887P11	Silicon, Zener: 500 mW, 10.0 v. nominal.
CR1705 and CR1706	19A115250P1	Silicon, fast recovery, 225 mA, 50 PIV.
CR1707	4036887P7	Silicon, Zener: 500 mW, 9.0 v. nominal.
CR1708 thru CR1710	19A115250P1	Silicon, fast recovery, 225 mA, 50 PIV.
		- - - - - - - JACKS AND RECEPTACLES - - - - - -
J1701 thru J1705	4033513P4	Contact, electrical: sim to Bead Chain L93-3.
J1707 and J1708	4033513P4	Contact, electrical: sim to Bead Chain L93-3.
		- - - - - - - - - - PLUGS - - - - - - - - - -
P1705 thru P1711	19A116428P3	Contact, electrical: sim to AMP 85487-3 (Strip Form).
		- - - - - - - - - - TRANSISTORS - - - - - - - -
Q1701	19A115364P1	Unijunction: N Type; sim to 2N2646.
Q1702 thru Q1707	19A115910P1	Silicon, NPN; sim to Type 2N3904.
Q1708	19A115300P2	Silicon, NPN; sim to Type 2N3053.
Q1709	19A115768P1	Silicon, PNP; sim to Type 2N3702.
Q1710	19A115910P1	Silicon, NPN; sim to Type 2N3904.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
		NOTE: The value of R1701 is selected to provide a Master Pulse Generator output of 8 Hz.
R1701A	3R152P432J	Composition: 4.3K ohms ±5%, 1/4 w.
R1701B	19A700106P85	Composition: 8.2K ohms ±5%, 1/4 w.
R1701C	3R152P912J	Composition: 9.1K ohms ±5%, 1/4 w.
R1701D	19A700106P87	Composition: 10K ohms ±5%, 1/4 w.
R1701E	3R152P113J	Composition: 11K ohms ±5%, 1/4 w.
R1701F	19A700106P89	Composition: 12K ohms ±5%, 1/4 w.
R1701G	3R152P133J	Composition: 13K ohms ±5%, 1/4 w.
R1701H	19A700106P91	Composition: 15K ohms ±5%, 1/4 w.
R1701J	3R152P163J	Composition: 16K ohms ±5%, 1/4 w.
R1701K	19A700106P93	Composition: 18K ohms ±5%, 1/4 w.
R1701L	3R152P203J	Composition: 20K ohms ±5%, 1/4 w.
R1701M	19A700106P95	Composition: 22K ohms ±5%, 1/4 w.
R1701N	3R152P243J	Composition: 24K ohms ±5%, 1/4 w.
R1701P	19A700106P97	Composition: 27K ohms ±5%, 1/4 w.
R1701Q	3R152P303J	Composition: 30K ohms ±5%, 1/4 w.
R1701R	19A700106P99	Composition: 33K ohms ±5%, 1/4 w.
R1701S	3R152P363J	Composition: 36K ohms ±5%, 1/4 w.
R1701T	19A700106P101	Composition: 39K ohms ±5%, 1/4 w.
R1701U	3R152P433J	Composition: 43K ohms ±5%, 1/4 w.
R1702	19A700106P101	Composition: 39K ohms ±5%, 1/4 w.
R1703	19A700106P55	Composition: 470 ohms ±5%, 1/4 w.
R1704	19A700106P39	Composition: 100 ohms ±5%, 1/4 w.
R1705	19A700106P87	Composition: 10K ohms ±5%, 1/4 w.
R1706	3R77P131J	Composition: 130 ohms ±5%, 1/2 w.
R1707	19A700106P103	Composition: 47K ohms ±5%, 1/4 w.
R1708	3R152P123K	Composition: 12K ohms ±10%, 1/4 w.
R1709	19A700106P91	Composition: 15K ohms ±5%, 1/4 w.
R1710	19B209358P106	Variable, carbon film: approx 300 to 10,000 ohms ±10%, 0.25 w; sim to CTS Type X-201.
R1711	19A700106P63	Composition: 1K ohms ±5%, 1/4 w.
R1712	19A700106P95	Composition: 22K ohms ±5%, 1/4 w.
R1713	19A700106P87	Composition: 10K ohms ±5%, 1/4 w.
R1714 and R1715	19A700106P95	Composition: 22K ohms ±5%, 1/4 w.
R1716	19A700106P63	Composition: 1K ohms ±5%, 1/4 w.
R1717	3R152P332K	Composition: 3.3K ohms ±10%, 1/4 w.
R1718*	19A700106P39	Composition: 100 ohms ±5%, 1/4 w. Added by REV E.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - - -
U1701	19A115913P10	Digital, Dual J-K Flip-Flop: Identification No. 093.
U1702	19A115913P7	Digital, Quad 2-Input Nand Gate: Identification No. 946.
U1703	19A115913P1	Digital, Expandable Dual 4-Input Nand Gate: Identification No. 930.
U1704	19D424078G1	Audio Mute Hybrid.
		- - - - - - - - - MISCELLANEOUS - - - - - - - - -
	4036555P1	Insulator, washer: nylon. (Used with Q1708).

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

PRODUCTION CHANGES

LBI4680

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter," which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by these revisions.

REV. A - Incorporated in initial shipment.

REV. B - To reduce audio thump when receiving non-priority channel. Changed C1705.

REV. C - To resume search after transmitting when used with Channel Guard. Relocated R1717.

REV. D - To improve operation. Changed U1704.

REV. E - To improve operation in Monitor Receiver Applications. Added R1718, C1713, C1714 and C1715.

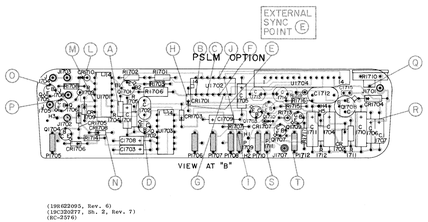


Figure A - Chassis Test Points

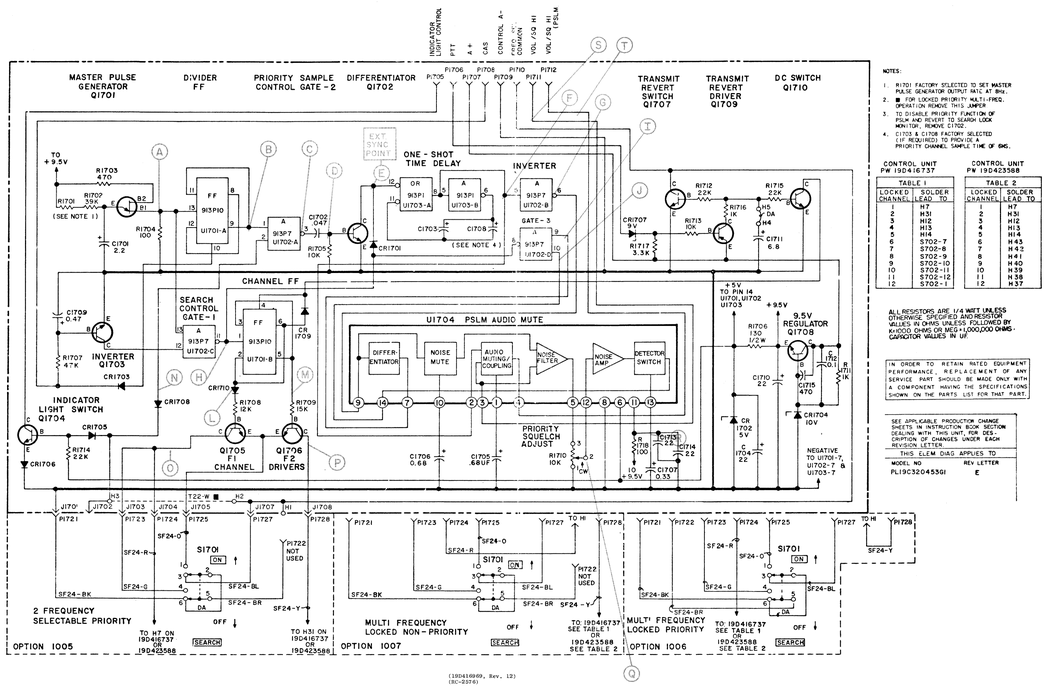


Figure B - Schematic Test Points

NOTES:
1. R1701 FACTORY SELECTED TO SET MASTER PULSE GENERATOR OUTPUT RATE AT 8Hz.
2. ■ FOR LOCKED PRIORITY MULTI-FREQ. OPERATION REMOVE THIS JUMPER.
3. TO DISABLE PRIORITY FUNCTION OF PSLM AND REVERT TO SEARCH LOCK MONITOR, REMOVE C1702.
4. C1703 & C1708 FACTORY SELECTED (IF REQUIRED) TO PROVIDE A PRIORITY CHANNEL SAMPLE TIME OF 6MS.

CONTROL UNIT PN 190416737

TABLE 1

LOCKED CHANNEL	SOLDER LEAD TO
1	H1
2	H3I
3	H1S
4	H1A
5	H14
6	S702-7
7	S702-8
8	S702-9
9	S702-10
10	S702-11
11	S702-12
12	S702-1

CONTROL UNIT PN 190423588

TABLE 2

LOCKED CHANNEL	SOLDER LEAD TO
1	H7
2	H3I
3	H12
4	H1A
5	H14
6	H43
7	H42
8	H41
9	H40
10	H39
11	H38
12	H37

ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY K=1000 OHMS OR MEG=1,000,000 OHMS. CAPACITOR VALUES IN UF.

IN ORDER TO RETAIN RATED EQUIPMENT PERFORMANCE, REPLACEMENT OF ANY SERVICE PART SHOULD BE MADE ONLY WITH A COMPONENT HAVING THE SPECIFICATIONS SHOWN ON THE PARTS LIST FOR THAT PART.

SEE APPLICABLE PRODUCTION CHANGE SHEETS IN INSTRUCTION BOOK SECTION DEALING WITH THIS UNIT, FOR DESCRIPTION OF CHANGES UNDER EACH REVISION LETTER.

THIS ELEM DIAG APPLIES TO

MODEL NO	REV LETTER
PLI9C320455G1	E

TROUBLESHOOTING PROCEDURE

NOTE

The audio quality of the Non-Priority channel can best be checked with an unmodulated carrier or voice modulation. When the PSLM is on the Non-Priority channel, applying a constant tone to the receiver will result in a pulsed sound.

Preliminary checks

NOTE - Voltages are nominal.

1. Check for a regulated +9.5 volts at C1710 (+)
2. Check for +5 volts at C1704 (+)
3. Check for +5 volts at Pin 14 of all IC's.
4. Check for ground (A-) at Pin 7 of all IC's.

SYMPTOM	PROCEDURE
No receiver audio	1. Check the receiver in a different system (with or without PSLM.) 2. Check waveforms at Test Points (S) and (A).
No 1st oscillator activity	Check waveforms at Test Points (O) and (P) with search mode disabled.
Receiver rapidly alternates between F1 and F2 while trying to receive the Non-Priority channel. - - - - OR - - - Obnoxious white noise received on the Non-Priority channel	1. Check the setting of Priority Squelch Adjust R1710 (see Table of Contents) 2. Check waveforms at Test Points (S) and (T). 3. Check system interconnections (refer to Interconnection Diagram in the Maintenance Manual for the Control Unit).
Fails to receive Priority Channel	1. Check setting of Priority Squelch Adjust R1710 (See Table of Contents). 2. Check Voltage readings and waveforms at Test Points (F), (M), (N), (O), and (P).
Incorrect Priority channel	1. Verify correct strapping for selected option. Refer to Installation and Outline Diagram in this manual. 2. Check voltage readings and waveforms at Test Points (M), (N), (O), and (P).
Missed syllables on the first part of transmissions	Check waveform at Test Point (A) for incorrect sample rate. Resistor R1 is selected at the factory for an output of 8 Hz (±5%). See Parts List for values of R1.
PSLM Continues searching when PTT switch depressed	1. Verify A- at junction of CR17C5 and CR1708 and the cathode side of CR1709. 2. Verify proper operation of Q1707-Q1710. 3. Check microphone.

VOLTAGE READINGS

All voltage readings are DC readings measured with a 20,000 ohm-per-volt VOM with reference to system negative. The readings are taken with the PSLM board connected for F1 priority.

NOTE

Readings followed by a (P) are averages of pulsating meter deflections. These readings may vary widely due to the differences in meter ballistics, but may be used to determine that the circuit is operative (or switching) and not at a DC or ground potential.

Preliminary Checks

NOTE - Voltages are nominal

1. Check for +9.5 volts at C1710 (+)
2. Check for +5 volts at C1704 (+)
3. Check for +5 volts at Pin 14 of all IC's.
4. Check for ground (A-) at Pin 7 of all IC's.

Test Point	Reading with Receiver Squelched	Reading with Receiver Unsquelched (on Non-Priority Channel)	Reading with Receiver Unsquelched (on Priority Channel)
A	.42 V	.4 V	.4 V
B	.15 V	2.4 V (P)	2.4 V (P)
C	4.9 V	2.4 V (P)	5 V
D	0 V	0 V	0 V
E	4.6 V	4.6 V (P)	4.6 V
F	.1 V	.25 V (P)	.2 V
G	4.7 V	4.7 V (P)	4.7 V
H	5.0 V	5.0 V (P)	5.0 V
I	.7 V	.75 V (P)	.7 V
J	.1 V	.25 V (P)	.2 V
K	0.5 V	.2 V	.2 V
L	2 V (P)	3.8 V (P)	.2 V
M	2 V (P)	.2 V (P)	3.9 V
N	.7 V	.8 V	.75 V
O (J5)	2 V (P)	.3 V (P)	3.8 V
P (J6)	2 V (P)	3.9 V	.2 V
Q	1.7 V	1.75 V	1.75 V
R	.7 V	0.65 V (P)	.75 V
S (J7)	4.2 V	4.2 V	4.2 V
T (J8)	4.3 V	4.3 V	4.3 V

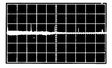
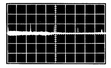
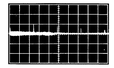
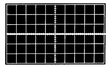
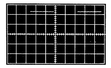
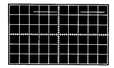
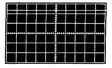
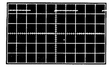
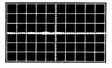
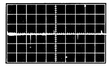
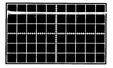
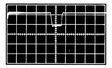
WAVEFORMS

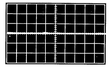
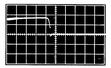
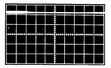
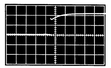
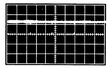
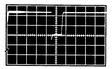
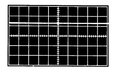
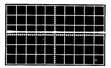
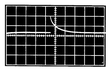
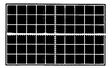
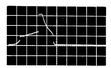
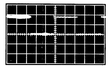
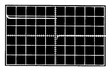
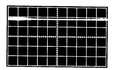
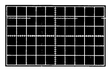
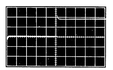
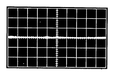
All waveforms are taken at Test Points (A) thru (T) as shown in Figures A and B, and are taken with the PSLM board connected for F1 priority. When applicable, the waveforms are shown for three different modes of operation as follows:

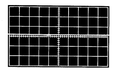
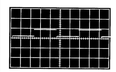
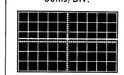
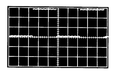
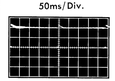
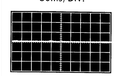
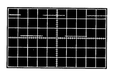
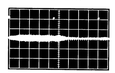
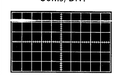
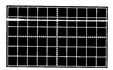
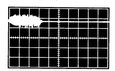
1. Receiver Squelched (PSLM Searching)
2. Receiver Unsquelched (Receiving Non-Priority Channel)
3. Receiver Unsquelched (Receiving Priority Channel)

NOTE

All waveforms are taken using Test Point E as the SYNC SOURCE (Trigger Pulse) except where NOTED.

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL	RECEIVING PRIORITY CHANNEL
A	 50ms/Div. 2V/Div. NOTE INTERNAL SYNC	 50ms/Div. 2V/Div. NOTE INTERNAL SYNC	 50ms/Div. 2V/Div. NOTE INTERNAL SYNC
B	 50ms/Div. 2V/Div. NOTE INTERNAL SYNC	 50ms/Div. 2V/Div. NOTE INTERNAL SYNC	 50ms/Div. 2V/Div. NOTE INTERNAL SYNC
C	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC	 50ms/Div. 2V/Div.	
D	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div.	
E	 1ms/Div. 2V/Div.	 1ms/Div. 2V/Div.	

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL	RECEIVING PRIORITY CHANNEL
F	 1ms/Div. 2V/Div.	 1ms/Div. 2V/Div.	
G	 1ms/Div. 2V/Div.	 1ms/Div. 2V/Div.	
H	 50ms/Div. 2V/Div.	 1ms/Div. 2V/Div.	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC
I	 1ms/Div. 2V/Div.	 1ms/Div. 2V/Div.	
J	 2ms/Div. 0.5V/Div.	 5ms/Div. 1V/Div	
L	 50ms/Div. 2V/Div. INTERNAL SYNC	 1ms/Div. 2V/Div. INTERNAL SYNC	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC
M	 50ms/Div. 2V/Div. INTERNAL SYNC	 1ms/Div. 2V/Div. INTERNAL SYNC	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL	RECEIVING PRIORITY CHANNEL
N	 50ms/Div. 2V/Div. INTERNAL SYNC	 50ms/Div. 2V/Div. INTERNAL SYNC	 50ms/Div. 2V/Div.
O	 50ms/Div. 2V/Div. INTERNAL SYNC	 50ms/Div. 2V/Div. CR1710 + SYNC	 50ms/Div. 2V/Div.
P	 50ms/Div. 2V/Div.	 50ms/Div. 5V/Div. CR1710 + SYNC	 50ms/Div. 5V/Div. NOTE: INTERNAL SYNC
Q	 2ms/Div. 0.2V/Div.	 2ms/Div. 1Volt/Div.	
R	2ms/Div. 0.2V/Div.	2ms/Div. 0.2V/Div.	
S	2ms/Div. 0.2V/Div.	2ms/Div. 2V/Div.	2ms/Div. 0.5V/Div. NOTE: INTERNAL SYNC
T	2ms/Div. 1V/Div.	2ms/Div. 2V/Div.	2ms/Div. 1V/Div. NOTE: INTERNAL SYNC