ICOM UX Module Design Guide

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The ICOM UX module series consists of at least 9 different modules covering 7 frequency ranges. Most of the modules were designed for the IC-900 Multi-band Transceiver, while some were designed specifically for the IC-901 Transceiver. The modules feature a simple daisy-chain control bus architecture which allows multiple modules to be assembled (also referred to as "stacked") to cover a wide variety of frequency bands and modulation modes.

Figure 1 illustrates the IC-901 Transceiver architecture. The IC-900 block diagram is similar except that the 2M and 440MHz transceivers are not built into the base unit, and there is no expansion bus. The interface to the modules is accomplished using two, 15-pin daisy-chain connectors. Digital and analog signals are conveyed along the daisy-chain bus as a series of short-stub taps. 13.8Vdc Power and RF connections are at the back side of the modules, and the daisy-chain busses are at the front of the modules.

With a microprocessor and some relatively simple interface circuitry, one can design a control unit that eliminates the need for the base unit and remote controller. This has been done by several companies to produce frequency agile, multi-band remote base interfaces for repeaters. I have personally created a very efficient APRS radio as well as frequency agile remote-base systems using the FC-900/UX modules and the IC-901/UX modules. Their modest size and lack of display (a source of increased current draw for many radios) make them very attractive for a variety of applications.

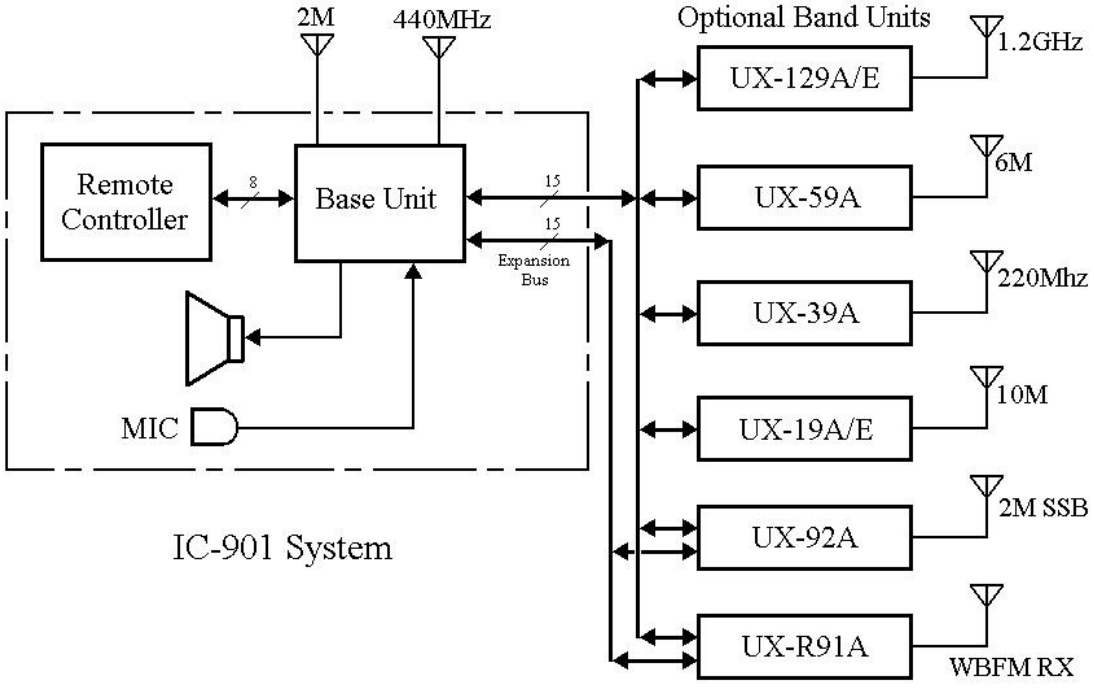


Figure 1. Simplified block diagram for the IC-901.

This document represents a collection of technical data needed to control the ICOM UX modules and is the culmination of many years of effort spent reverse engineering the modules behavior and refining the resulting interface. All of the information contained herein has either been collected by monitoring module signals that are easily accessible, or by analyzing published schematics and component datasheets.

The ICOM UX Module

Figure 2 illustrates a typical UX module with the covers removed. The ICOM modules are generally divided into two circuit cards, identified by ICOM as the Main Unit and the Front Unit. The Front Unit is a small circuit card located at the front of the module. It performs the base unit bus-interface and module address selection functions via a pair of 15 pin, daisy-chain "joint" cables (the "expansion" modules have two pair of these connectors). The Front Unit is essentially identical for all of the original IC-900 series modules (differing only in that there are a series of solder-jumpers used to program the module address ID). The Front Units for the "expansion" modules are not interchangeable, but perform the same functions. The Main Unit holds all of the transmitter and receiver circuits. Some of the Main Unit circuit cards are similar from one module to another (the 10M and 6M modules are an example), but even those are not readily swap-able from one band to another because of component differences.

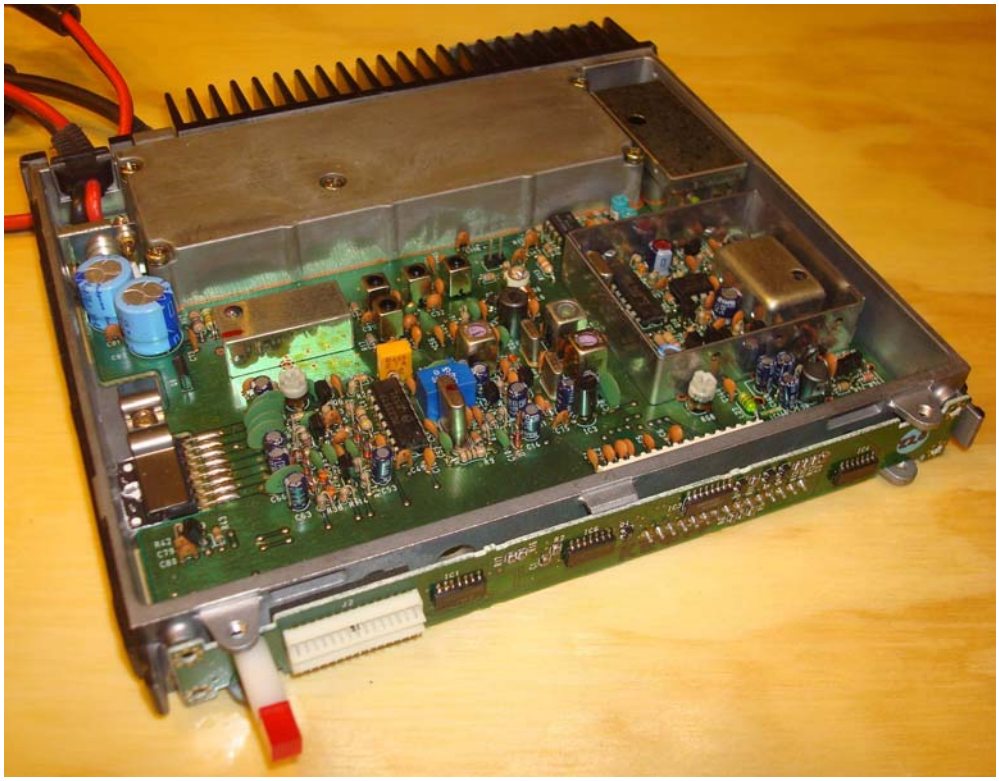


Figure 2. An ICOM UX module with covers removed.

Of particular interest for any given module is the PLL circuit as this is the primary means for controlling the transmit and receive frequencies. The following table describes the modules that are discussed in this document:

UX Module	band/mode	RF Out (hi/lo)	Compatibility	#daisy-chains
UX-19	10M (FM)	10W/1W	IC-900/901	1
UX-59	6M (FM)	10W/1W	IC-900/901	1
UX-29A	2M (FM)	25W/5W	IC-900	1
UX-29H	2M (FM)	45W/5W	IC-900	1
UX-39	220 (FM)	25W/5W	IC-900/901	1
UX-49	440 (FM)	25W/5W	IC-900	1
UX-129	1.2GHz (FM)	10W/1W	IC-900/901	1
UX-92A	2M (SSB)	25W/5W (PEP)	IC-901	2
UX-R91	Wide-band RX (AM/FM)	N/A	IC-901	2

Based on the schematics for the IC-901, provision was made for several other expansion modules, but I have never seen anything available, nor heard any rumor of any other modules. The Front Units on the expansion modules are not interchangeable as they feature circuitry that is dedicated to the respective module.

UX Module Interface Specification

This section describes the connectors, pinouts, and circuits needed to interface with the UX modules. A daisy-chain connector system connects each module to the base unit. These connectors (one for the "controller side" and one for the "module side") are located at the front of the module. The daisy-chain connectors (designated as OPC-179 by ICOM, and sometimes referred to as "ribbon" cables) are 15 pin single row connectors with a 1.5mm contact pitch. The Front Unit section covers the construction of these cables in more detail. Since the OPC-179 is symmetrical, either end may be used interchangeably.

Primary daisy-chain bus (J1 is lower, J2 is upper):

Pin#		Signal Name	Type	Description
J1-1	(J2-15)	E (GND)	Power	Signal common
J1-2	(J2-14)	+5V	Power (in)	+5V to operate the Front Unit circuits
J1-3	(J2-13)	MOD	Analog (in)	Modulation signal, pre-emphasized
J1-4	(J2-12)	STB	Digital (in)	Serial strobe signal (+5V CMOS logic levels)
J1-5	(J2-11)	DATA	Digital (in)	Serial data signal (+5V CMOS logic levels)
J1-6	(J2-10)	CK	Digital (in)	Serial clock signal (+5V CMOS logic levels)
J1-7	(J2-9)	BUSY	Digital (out)	Open-collector signal to indicate module is accessed
J1-8	(J2-8)	SRFB	Analog (out)	Sub-band S-meter and relative TX power for
J1-9	(J2-7)	SRFA	Analog (out)	Main-band S-meter and relative TX power for
J1-10	(J2-6)	DETB	Analog (out)	Sub-band RX audio (no de-emphasis)
J1-11	(J2-5)	DETA	Analog (out)	Main-band RX audio (no de-emphasis)
J1-12	(J2-4)	SQ2B	Analog (out)	Sub-band squelch adjust (via 5K pot to GND)
J1-13	(J2-3)	SQ2A	Analog (out)	Main-band squelch adjust (via 5K pot to GND)
J1-14	(J2-2)	SQSB	Digital (out)	Sub-band squelch gate (>4V = open, <1V = closed)
J1-15	(J2-1)	SQSA	Digital (out)	Main-band squelch gate (>4V = open, <1V = closed)

Note: all digital signals are +5V CMOS logic.

Table 1. Front Unit J1/2 daisy-chain connector pinouts. Signal directions (in or out) are from the standpoint of the UX module.

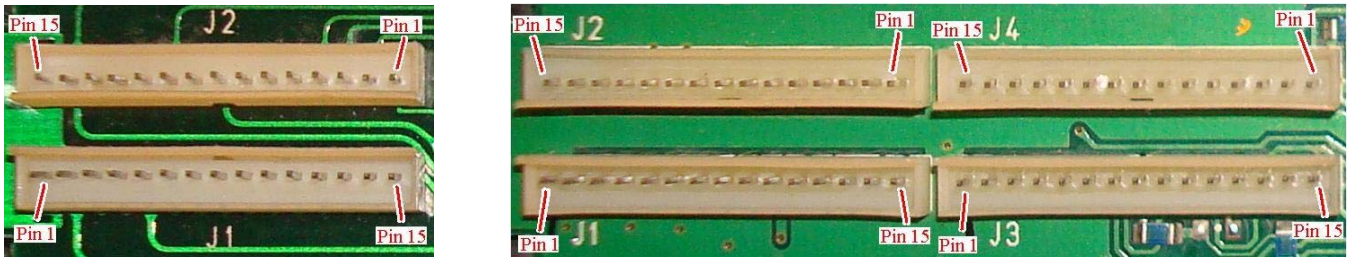
Expansion daisy-chain bus (J3 is lower, J4 is upper):

Pin#		Signal Name	Type	Description
J3-1	(J4-15)	PTT	Digital (out)	PTT engaged when <1V
J3-2	(J4-14)	TMUTE	Digital (out)	>2V when UX-92 PLL unlocked
J3-3	(J4-13)	KEY	Digital (in)	Base controller TX key signal (+5V keys 2M SSB)
J3-4	(J4-12)	BAND6	Digital (in)	Band 6 select signal (UX-R91, WBFM Receiver)
J3-5	(J4-11)	BAND5	Digital (in)	Band 5 select signal (module association unknown)
J3-6	(J4-10)	BAND4	Digital (in)	Band 4 select signal (UX-92, 2M SSB)
J3-7	(J4-9)	BAND3	Digital (in)	Band 3 select signal (module association unknown)
J3-8	(J4-8)	BAND1	Digital (in)	Band 1 select signal (module association unknown)
J3-9	(J4-7)	UNLKV	Digital (out)	UX-92 PLL Unlock when >2V
J3-10	(J4-6)	UNLKU	Digital (out)	UHF PLL unlock signal (module unknown)
J3-11	(J4-5)	UNLK12	Digital (out)	1.2GHz PLL unlock signal (module unknown)
J3-12	(J4-4)	RITST	Digital (in)	RIT strobe (see text)
J3-13	(J4-3)	SSBST	Digital (in)	SSB strobe (see text)
J3-14	(J4-2)	PLST	Digital (in)	PLL strobe (see text)
J3-15	(J4-1)	CTRST	Digital (in)	Control strobe (see text)

Note: all digital signals are +5V CMOS logic.

Table 2. Front Unit expansion connector pinouts. Signal directions (in or out) are from the standpoint of the UX module.

Tables 1 & 2 list the signals that are available on the Front Unit daisy-chain connectors. A close-up view of the connectors for the FM and expansion modules is shown in Figures 3a and 3b. The pin numbering reversal depicted in Table 1 occurs because ICOM rotated the top connector (J2 or J4) 180 degrees from the orientation of the bottom connector (J1 or J3) while connecting the pins directly between the pair of connectors on the bottom of the PWB. This rotation can cause no small degree of confusion if one is trying to design a custom Base Unit controller.



(a) (b)

Figure 3. Close-up views of the daisy-chain connectors, (a) is the layout of an FM-only module, (b) is the layout of the UX-91/92. When stacked vertically, J1/2 of the FM-only modules will line up with J1/2 of the UX-91/92 modules

The answer to "Which pin-1 to use?" depends entirely on where the Base Unit is to be located. A base unit on the bottom of a UX module stack would orient pin 1 of the corresponding connectors to match that of the top connector of the Front Unit (J2 or J4). A top-mounted control unit with UX modules underneath would orient pin 1 to match that of the bottom connector of the Front Unit (J1 or J3). A controller in the middle (not recommended) would need two connectors oriented in the same fashion as the Front Unit.

A common issue with the UX modules is that the OPC-179 cable is missing or damaged. A close mate to the module male housings is the Molex 87439-1500 female housing and the 87421-0000 crimp pins. Using the Molex parts and suitable wire (26 or 28 AWG stranded) replacement cables can be fabricated by cutting 15, 1.875" long wire pieces, strip at each end (0.06"), and apply female crimp pins to each wire end (sounds easy enough, except that the crimp pins are extremely small, and the approved crimp tool is very expensive). These 15 wires are then inserted into the two female housings to create the UX daisy-chain cable as shown in Figure 4. The trick is to get the housings oriented properly. I've always considered these little cables as 1:1 cables, but the truth is that they are crossover cables because the wires do not connect to the same pins on the two housings. The wire map is pin 1 of housing A (A1) connects to pin 15 of housing B (B15), pin A2 connects to B14, A3 to B13, etc…. When you lay the OPC-179 out flat, it appears to be wired "1:1" but you have to look closely to notice the crossover effect. Because the top and bottom connectors on the Front Unit are reversed from one-another, the cables end up connecting the signals from one module to the next in "straight-through" fashion.

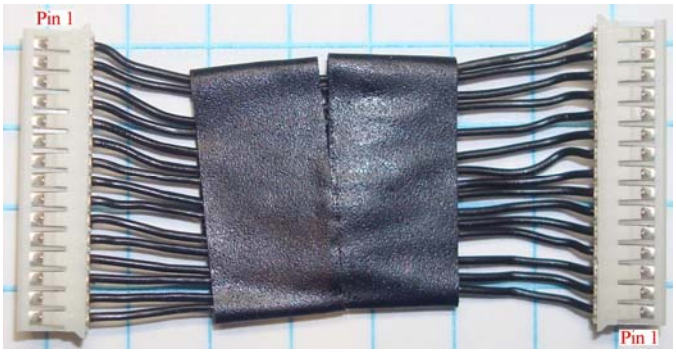


Figure 4. OPC-179 "joint" cable

The J1 through J4 digital signals require +5V CMOS logic. There are no bi-directional signals, so this simplifies the microcontroller interface. A controller that is designed for FM only UX modules is much simpler since the additional control signals of the expansion bus are not required. Figures 5a and 5b illustrate simplified block diagrams for an FM-only, and a full-featured UX module controller. The microcontroller is typically a single-chip device which contains all of the I/O and internal peripherals needed to provide the signals and timing needed to access the UX modules. However, any microprocessor based computer will work if it has sufficient I/O signals available and enough processing power to handle the serial data transfers.

The command port is depicted as a serial connection, but this could be a direct user interface if the microcontroller has enough additional I/O to drive a key-matrix and display. The UX module operates with 5V logic levels, so modern 3.3V (or lower) microcontrollers will likely require level shifting circuits (not shown). A simple level shifter for 3.3V to 5V logic is the 74HCTxx family with a 5V supply (the 74HCT1G08 is a good choice for a non-inverting level shifter). These devices operate on TTL voltage levels inputs, which are approximately equal to 3.3V CMOS levels, but output 5V CMOS levels (which are compatible with the UX module logic circuits) and therefore offer a simple level translation option for 3.3V processors.

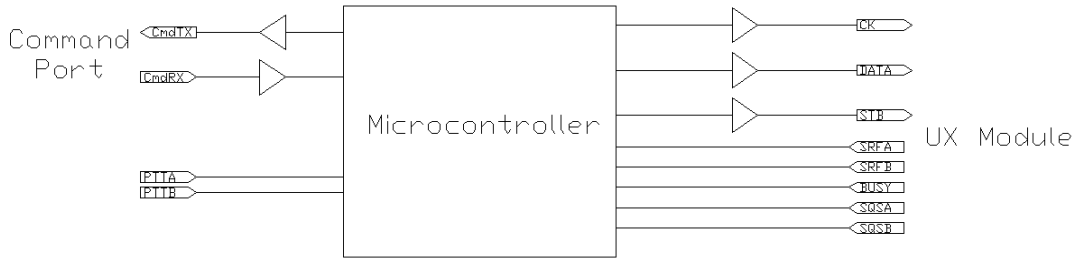


Figure 5a. Block diagram of an FM-only controller

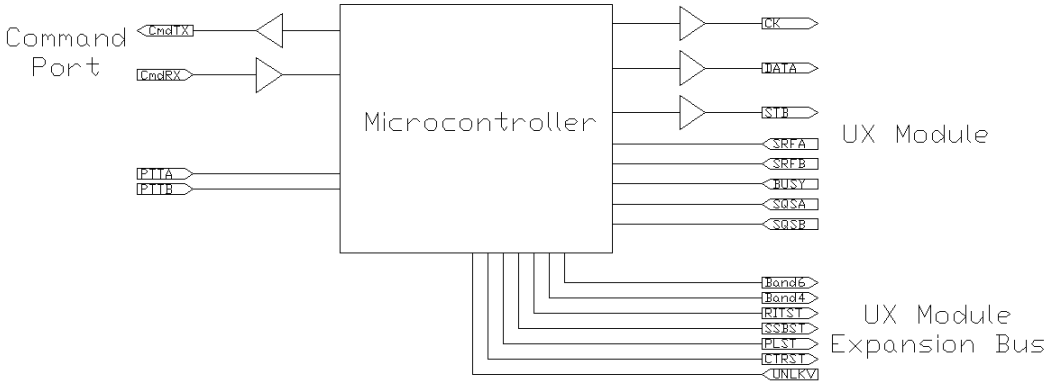


Figure 5b. Block diagram of a full-featured controller

The controller is highly software dependant and this document does not directly address the software needed to control the UX modules. The programming language and processor type would be determined by the designer and a discussion of those choices is beyond the scope of this document. From a software requirement standpoint, the microcontroller should be able to transmit the serial data with timings that approximate the ICOM implementation, with enough I/O to drive all of the relevant control signals. Also, the controller software must be capable of handling the transitions from receive to transmit and vis-à-vis, so it would need a PTT input signal (two if separate sub-band transmit control is desired). Also, if the controller is to access the SRF signals, an analog to digital converter is required (two if main/sub band architecture is implemented). The speed of the A/D conversion is not terribly critical for most applications, and suitable performance possible with as little as 8 bits of resolution (if the A/D span closely matches the desired input range of about 2.0 V).

The UX module analog signals require some attention to detail, but need not be terribly complicated. At the bare minimum, the modulation audio provided to the modules on the MOD pin must be pre-emphasized (a response slope of +6 dB/octave across the voice band) and band limited to 3 KHz. Amplitude limiting (i.e., clipping) is recommended to prevent the module(s) from over-deviating on signal peaks. Limiting may be omitted if the source audio is already amplitude limited (such as a PC audio or modem source). High-pass filtering of the CTCSS band (with an F_c of around 300Hz) is also recommended for applications where CTCSS encode features are implemented.

A diode limiter for a 0Vdc offset pre-emph signal is shown in Figure 6. The diodes are offset, or biased, such that the limit levels are about 5.8 Vpp. The reason for this is that the diode limiter response is generally "mushy" in that there isn't a hard limit at 0.7V – this makes it difficult to get a good deviation limit since the deviation can continue to increase long after severe distortion is realized. By applying

bias, the limit level is expanded, but the diode response remains the same. Following the modified limiter with a voltage divider reduces the degree of the "mushy" diode response by an amount that is proportional to the voltage division ratio. Another option for this circuit is to utilize an op-amp with a power supply voltage that is selected so that the maximum output swing of the op-amp defines the limiter range (generally, this op-amp is given a separate power supply that is designed to match up with a particular op-amp performance specification). The output of the op-amp is then fed to a resistive voltage divider to reduce the peak-to-peak amplitude of the signal.

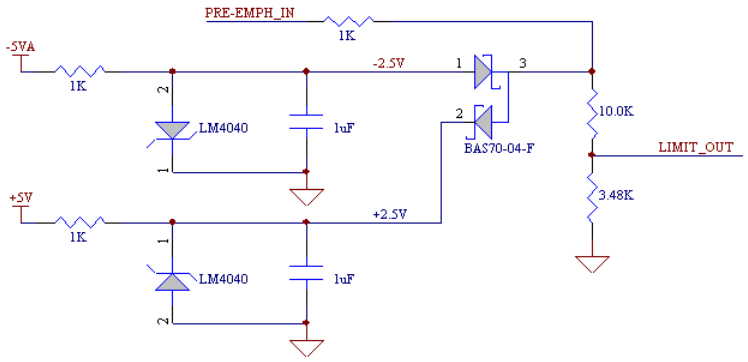


Figure 6. Modified diode limiter schematic

A properly aligned UX module will need 352 mVpp (125 mVrms) at the MOD pin for 5 KHz of deviation. Consequently, a CTCSS tone would need to be 50 mVpp (18 mVrms) to provide 0.75 KHz of deviation. The controller should provide a deviation control that can vary the modulation output from about 750 mVpp down to zero. This would put the nominal adjustment point at the mid-range of the pot swing. Figure 7 summarizes the necessary building blocks for a complete modulation shaping circuit for the FM modules.

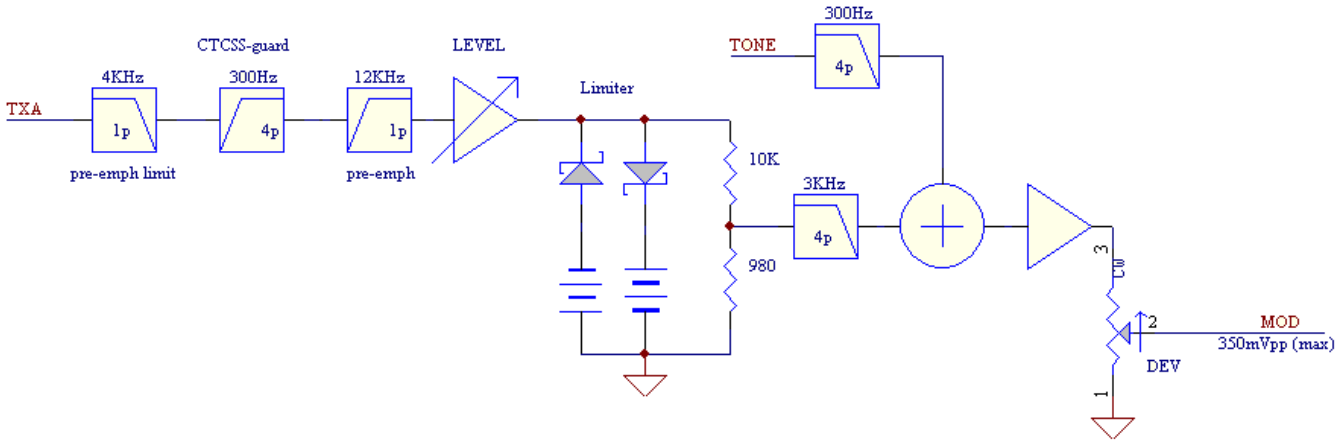


Figure 7. Block diagram for the FM MOD filter chain of an ICOM UX module

When including the UX-92 module in the modulator design, one must take into account the fact that the SSB shaping requirements are completely different than those of the FM modules. The pre-emphasis

and CTCSS guard blocks are not required and the limiter is also not required (but could be used to add a compressor if desired). Generally, it is easier to produce two modulation shaping circuits, and switch between them at the MOD pin node. This makes it easier to address the widely different modulation requirements that exist between FM and SSB.

For reception, the DETA/B signals provide raw audio from the demodulator. De-emphasis is needed and can be provided by a simple RC low-pass filter with an Fc of 150Hz or less, as shown in Figure 8. A properly aligned UX module will produce 0.255 Vpp (riding on a 3.5 Vdc offset) at the DET pin when receiving a 1 KHz tone with 3 KHz deviation (full quieting). In addition, the squelch threshold circuit must be satisfied with an adjustable resistance of 0 to 5 KΩ which sets the squelch level threshold. This resistance may be in the form of a traditional pot, or may be implemented with a digitally adjustable pot with a maximum allowed voltage of at least 5V. The squelch output (SQ2) is a COS (carrier-operated-squelch) indicator only, the DET output is not muted when the squelch is "closed" which implies that a mute circuit for each DET signal is also needed for general purpose applications. Either the CD4066 or CD4053 analog switch ICs are two device choices that can be easily implemented as audio squelch gates.

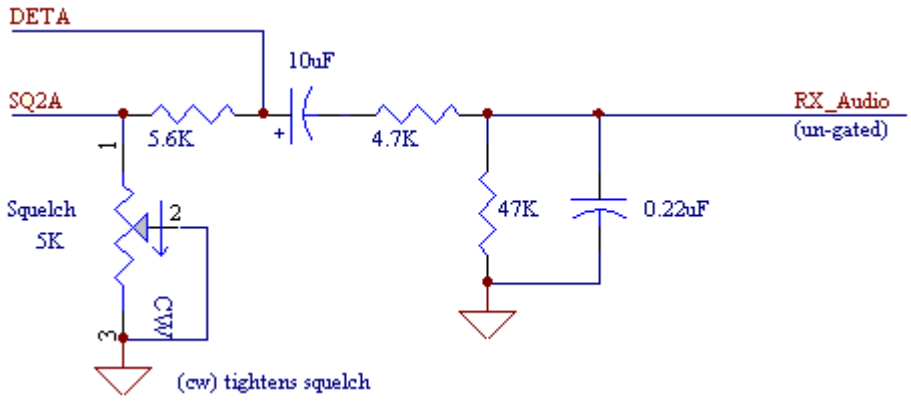


Figure 8. Simple RX Audio & squelch interface

The last analog signal to be addressed is the SRFA/B signal. This signal is used to indicate S-meter reading when receiving, and RF power output when transmitting. If the SRF features are not desired, these pins may be left un-terminated. During receive, the voltage for SRF varies from approx. 0.02 V for no-signal, to approximately 1.5 V for a full-strength signal (however, the exact maximum value will vary somewhat between modules).

After observing the behavior of the SRF signal during transmit and carefully analyzing the circuit that generates this signal, I have concluded that this signal is simply an indicator that the module is producing measurable power. The op-amp stage that drives the SRF signal generally has better than 30 dB of excess gain which results in saturation of the op-amp, and no real indication of the relative power except that it is at above some minimum level (my analysis indicates that this power threshold could be as low as 10mW). One might challenge this observation by noting that the ICOM control head indicates different SRF meter readings at low power vs. high power. However, this is simply a vestige of the controller software distinguishing between the high and low power setting and adjusting the display accordingly. I was able to prove this postulation by placing a variable resistor from SRFA to ground on

a UX module. This resistance modified the SRFA voltage by reducing it as the shunt-resistance was reduced. When the SRFA voltage reached about 0.32V, the SRF indication on the IC-901 control head would disappear entirely, without any gradual transition. The module was still producing rated power, but there was no indication on the display.

It is possible to modify each module by removing a resistor (the feedback resistor of the op-amp, e.g., R132 in the UX-19) and replacing it with a different value (or a pot) to reduce the gain of the SRF op-amp to the point that the SRF signal will provide a meaningful indication of the RF output power. This would require each module to be modified, and would likely affect the operation of the transmit indicator if the module were to be used with the IC-900 or IC-901 radio systems. However, the change would be relatively easy to accomplish and would not affect any of the other module systems. The aim is to reduce the gain of the SRF op-amp to a value of about 4 (for most of the modules the gain of this stage is in the range of 67 or higher). The exact values might require some experimentation to get the gain to the point where it is useable, providing an SRF voltage of about 1.5V for full power. A pot adjustment would be advisable to allow multiple modules to be calibrated against each other. The reading would still need to be taken with a grain of salt since it will depend on the RF power produced by the module as well as the antenna match, but might prove to be a simple and helpful tool for remote installations.

The SRF signal for the UX-92 is different from that of the FM modules in that it produces an SRF signal that is proportional to the instantaneous power which varies from 0V to 1.2V (matched load, high power – to be safe, one should assume that this voltage could vary to as much as 2.5V for full power into an infinite SWR). However, the proportionality constant is not linear, it is square-law. This is because of how the module produces the SRF voltage. RF is sampled from the final transmit matching chain and rectified, then it is filtered and buffered. By ohms law, $V^2/R = P$ and thus, $V(SRF) \propto \sqrt{P}$ and, assuming that the antenna match is near perfect, the proportionality constant can be calculated by measuring V(SRF) for several (at least two) power output levels. Using the UX-92 module I had available, the following equation was determined by measuring V(SRF) at two different (and measured) RF power levels and averaging the result. Thus, $Pout = (V(SRF)/0.225)^2$. The proportionality constant is likely to vary somewhat from one module to the next and, in this case, is only valid for $R_L \approx 50\ \Omega$.

The FM-Only Front Unit

The FM-only version of the ICOM Front Unit is shown in Figure 10. The expansion Front Units are discussed separately later in this document. The Front Unit serves two basic functions: First, it serves as an electronic, two position switch for the receiver signals to be selected as either the main or sub band connection to the base unit. Second, it holds address decode and steering logic for the PLL serial connections. The address decoding also captures several control signals to set the module's receiver switch (to select main or sub) and any logic signals that are particular to the module at hand.

Figure 10. ICOM UX module "Front Unit" (FM modules)

The receiver switching is handled by a series of CD4066 analog switches that are wired as four SPDT switches that connect the receive signals to either the "main" or "sub" busses that run via the 15 pin OPC-179 cables. There are four pairs of signals that are switched: SQ2A/SQ2B, SQSA/SQSB, DETA/DETB, and SRFA/SRFB. Logic signals from the address decode logic select the A (main) or B (sub) for connection to the receiver circuits. Because the UX stacking protocol only features a single MOD signal, there is no switching involved with the transmit signals. If one implements a system whereby the main and sub units can both transmit, they must transmit the same audio unless significant modifications are made to the Front Unit daisy-chain scheme.

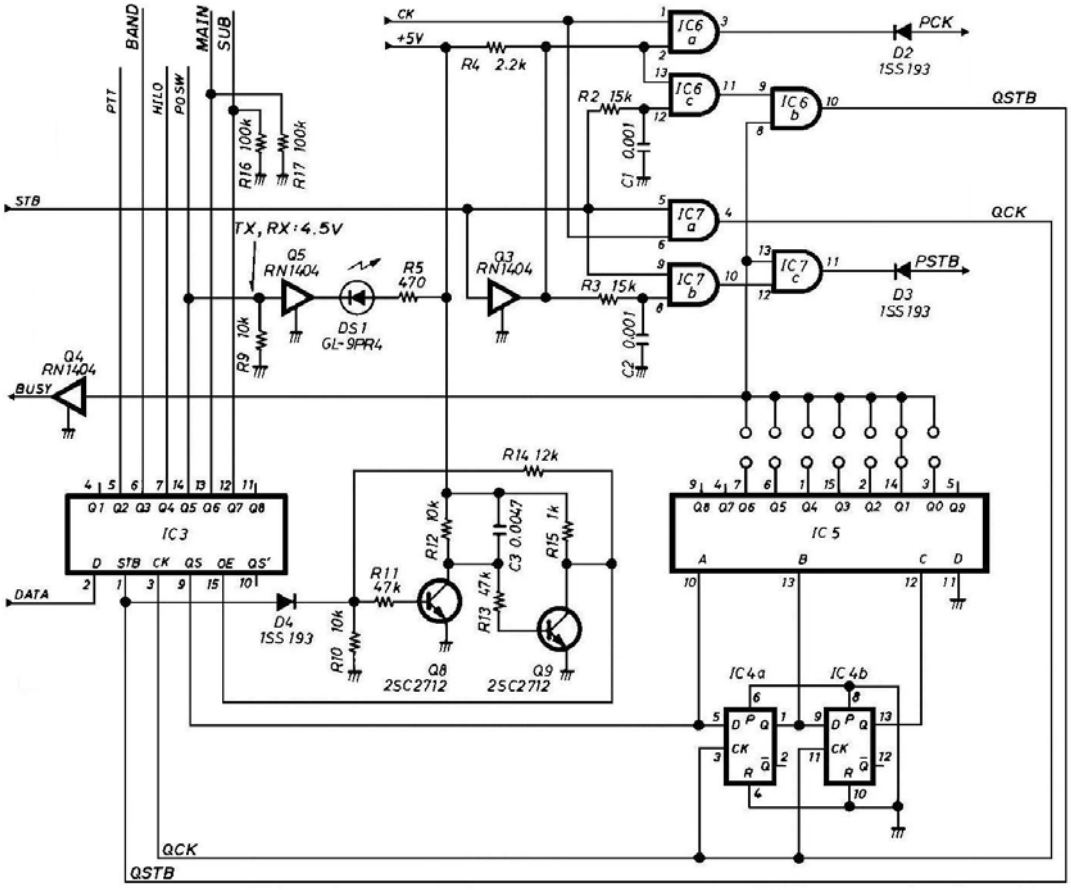


Figure 11. ICOM UX address decoding and steering logic circuit.

Figure 11 depicts the decoding and clock steering logic of the FM-only Front Unit. The steering logic is accomplished by a combination of a 10 bit shift register (comprised of a CD4094 8-bit SR, IC3, a CD4013 dual D flip-flop, IC4, and a CD4028 one-of-8 decoder, IC5) and a series of logic gates. A simple edge detector constructed from an RC network and an AND gate is used to produce pulses at the rising or falling edge (depending on the configuration of the gate and RC combination) of the strobe (STB) pulse. In this manner, the PSTB and QSTB signals are produced. PSTB drives the PLL strobe, while QSTB drives the IC3 strobe to latch the module control signals.

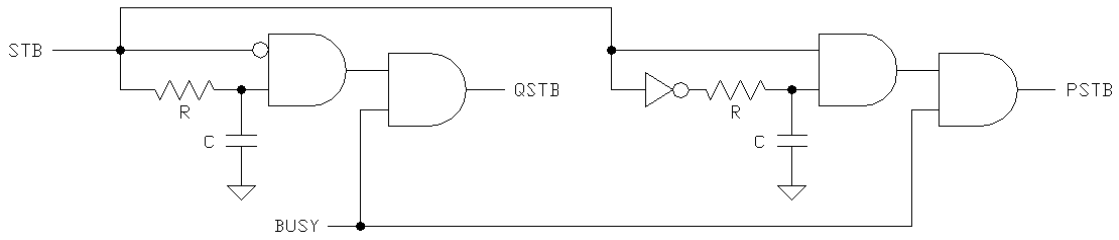


Figure 12. Simplified QSTB & PSTB edge detector circuits

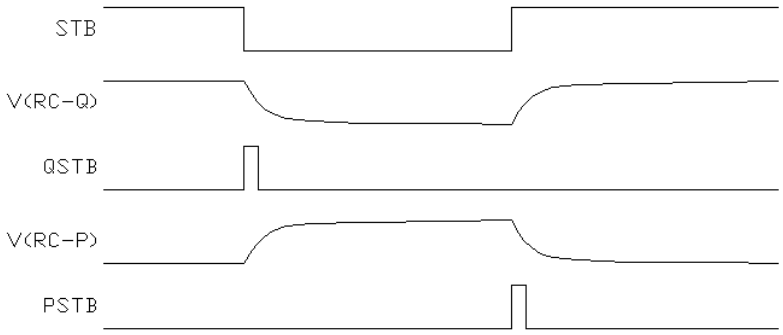


Figure 13. QSTB & PSTB circuit waveforms.

Figures 12 and 13 depict the operation of the QSTB and PSTB edge detector circuits. The QSTB pulse is produced by delaying an inverted version of the input signal (using an RC time constant) and feeding both signals through an AND gate. The width of the pulse is proportional to the value of RC (15 KΩ and 0.001 µF) and the switching threshold of the AND gate. Using the equation for RC decay (where V(RC) is normalized), $V(RC) = 1 - e^{-t/RC}$, and solving for t gives $t = -RC\ln(V(RC))$. If one assumes a 50% gate switching threshold for V(RC), the values of R and C used in the UX modules result in a pulse width of about 10µs.

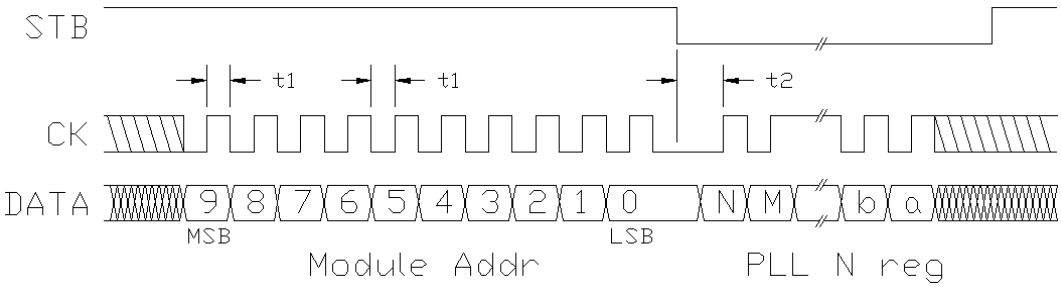
The switching threshold of the logic gate is the most nebulous of values in the above equation, varying with the IC processes and temperature. At the low extreme of 80% for the switching threshold (a typical datasheet minimum), t = 3.3µs which is actually a bit low for some of the PLL devices. Room temperature measurements of PSTB give a value of 10.3 µs (down to 9.8 µs when the AND gate was exposed to a blast of freeze spray). The following table summarizes some of the specifications of the PLL devices used in the UX modules:

Part#	**UX Module**	**T_{low} (°C)**	**T_{high} (°C)**	**t_{PSTB} (min)**	**Bit Order**
PLL2001	UX-19, UX-59	-30	+80	2.7µs	msb first
MB87001A	UX-29, UX-39	-40	+85	1µs	msb first
µPD2834C	UX-49	-40	+85	5µs	msb first
TC9181P	UX-129	-30	+85	2.7µs	lsb first

Figure 14 illustrates the bit-fields and critical timing to send data to a UX module. IC3 is a buffered shift register – the shift register section is always active and data clocked through the register is shifted back out on pin 9. This output of IC3 and the two flip-flops of IC4 form a 3 bit shift register (un-

buffered) that captures the module address bits, while the remaining 7 bits of IC3 capture control data. When the address bits (IC4 pins 5, 1, and 13) match the device address that is selected by the solder jumper adjacent to IC5 (only one of the 7 jumpers may be soldered at a time), the BUSY output is activated which enables the PSTB and QSTB signals. The BUSY signal is also connected to the base unit and allows the controller to determine if an addressed module is installed.

STB is normally high and is brought low at the end of the 10 bit module control/address frame. This readies the steering logic for PLL data and clock and pulses the QSTB line to latch the module control signals. When the QSTB goes high, the IC3 shift register bits are transferred to the IC3 output pins and these pins retain their value when QSTB goes low again which latches the module control signals. I apply an "edge delay" of at least 150µs after the STB edge to make sure that the steering logic has been properly engaged, but any delay longer than 20 or 30 µs should be sufficient. Next, PLL data can be sent. The ICOM IC-900/901 sends PLL frames as fixed 20 bit wide values, but each PLL type has different register widths and so the fixed 20 bit width is not necessary (ICOM likely sends a fixed 20 bit frame to simplify the control software). In addition, the shift order of the PLL data is not the same for all modules. Most of the modules shift msb first, but the UX-129 shifts lsb first. The module control/address data is always shifted msb first. Once the PLL clocking is finished, the controller raises STB high and the next transaction can occur (after waiting the edge delay).



t1	clock half-period duration, 104 us (min)	t2	strobe settling time, 150 us (min)
D[9:7]	module address (bit 9 = first bit to shift, msb)		
Module Control Signals, D[6:0]:			
D6	main bus select	D3	RF power ("1" = high, "0" = low)
D5	sub bus select (D[6:5] = "11" is not allowed)	D2	BAND signal
D4	module power on	D1	TX enable (PTT3)
		D0	not used
PLL Data:			
D[N:a]	PLL data (20 bits, typ. "N" = first bit to shift, msb for all except UX-129)		

Figure 14. UX Module serial data diagram.

Serial data to be sent to the module is clocked at the rising edge of CK which should have an edge-to-edge half-cycle period of no less than 104µs to match the ICOM timing (this is very conservative compared with the device specifications, but is necessary due to the ICOM circuitry and physical layout of the module stack). To gain the maximum noise margin, data should transition at or near the falling edge of the clock to allow the signal to settle at the far-end of the signal path before asserting the rising edge of the clock. The ACC controller used open drain/collector style drivers to clock data into the band modules, but push-pull drivers are a better choice, especially if they are bus-driver devices (like the 'HC244). Push-pull devices actively assert the signals in both the high and low states giving rise and

fall times that are more consistent and faster than open drain/collector devices. Open drain/collector drivers are actively asserted only in the "0" state. In the "1" state, the signal level is established with a pull-up resistor. The rise time of the signal is then determined by the value of the pull-up resistor, and the stray capacitance from the signal to ground, while the fall time is determined by the R-on of the driver and that same line capacitance (R-on is generally many orders of magnitude smaller than R pull-up).

The PLL data varies depending on the PLL chip and module architecture. These differences are covered in the Main Unit section below. In addition, the BAND signal is not used except on the 2M and 6M FM modules, and it is also covered in the Main Unit section.

There is an aspect of the PLL data transfer that I have not explored as yet. It would greatly reduce the amount of time required to configure some of the PLL devices. For those PLL devices that require initialization frames, STB can be pulsed high for, say, 50 µs in between each PLL register. This would reduce the number of bits (by a factor of 10 bits per register, since the control/address bit frame would not need to be re-sent) that were required under the ICOM method. This is especially attractive for the UX-129 since there are 4 different registers that must be configured for the TC9181P PLL. As long as CK is low, STB can be pulsed to trigger PSTB. The STB pulse should be no less than 10 µs, and there should be at least 50 µs between STB pulses.

The Main Unit

The Main Unit contains all of the receiver, transmitter, and power supply circuits. The discussion here focuses on the behavior of the interface signals. These are divided between the serial data signals, and the analog TX/RX signals. All of the modules use a common interface for these signals with the primary difference between modules being the format of the PLL serial data. The analog signals have been covered in the previous sections.

Three signals are provided to the Main Unit for the serial data interface to the PLL: DATA, CKD, and PSTB. In addition, the POSW, PTT3, and BAND signals are provided to control the Main Unit circuits. POSW is set to 1 to enable the Main Unit power supply and thus turns on the UX module. When PTT3 is set to logic 1, the TX circuits are enabled which puts the module in transmit mode. *Note: The PLL must first be configured for the desired TX frequency before PTT3 is activated or the module will produce RF output on an out-of-band frequency.*

BAND is used by the UX-59 and UX-29 modules to bypass the receiver front-end bandpass filter. This increases the receiver sensitivity outside the specified (Ham band) frequency range to allow reception of out-of-band signals. Of course, this increase in sensitivity comes at the cost of selectivity, so the user must be aware that they may have to tolerate an increased level of co-channel or IMD interference when receiving signals in this configuration. BAND is normally set to 0 for ham-band coverage, and is set to 1 to enable out-of-band coverage. The out-of band sensitivity generally leaves something to be desired (the 12dB SINAD sensitivity can be as much as 5 or 10 µV or higher) but it is much better than with the in-band filtering enabled and can still be useful for receiving fixed service stations such as NOAA weather broadcasts.

It should be noted that the ICOM UX modules all feature a single PLL that serves double duty as transmit and receive LO (most modules operate their VCO at the TX operating frequency). The receiver IF sets the VCO frequency difference between RX/TX and this is generally different for each module type. This means that the control system must send PLL data at least twice for every transmit/receive cycle (once to set the TX frequency on initial transmit, and again to set the receive frequency when the PTT is released).

PLL Basics

There are a number of factors that go into the design of a PLL system and a full discussion of these factors is beyond the scope of this document. Because of this, only the factors that relate to operating frequency are discussed here (and even at that, the discussion is very light). Even though some of the UX modules share the same PLL device, the architecture of the receivers is such that none of the modules share the same exact PLL-N and ref-divider code conversion algorithms. Knowing something about how the PLL works and how the module architecture is arranged can greatly simplify the understanding of the PLL control algorithms. However, this understanding is not necessary to make use of the information. Some of these architecture and circuit specifics are discussed below, but in the end, one only needs to know a base PLL pattern, base operating frequency for RX and TX, and bit shift order in order to configure the module's PLL (these items are all tabulated below).

The simplest PLL is nothing more than a programmable digital divider/counter chain that accepts the output of a VCO (voltage controlled oscillator). The final carry output of the PLL divider/counter is fed to a phase comparator (a basic phase comparator is nothing more than a two-input exclusive-OR gate). The other input to the phase comparator comes from a reference oscillator. The output of the phase comparator is filtered and fed back to the VCO input. If the divided VCO signal and reference oscillator are exactly in-phase and on-frequency, the output of the phase comparator will be zero (or some base-bias value, depending on the design of the phase comparator). Any phase difference will result in a non-zero phase comparator output which, once filtered, becomes an error voltage that drives the VCO to return the system to a zero phase error.

Some PLL devices have built-in reference oscillators, while others require an external reference oscillator. Additionally, some reference inputs have a separate reference divider that is programmable. Most PLL devices also have provisions for dual-modulus prescaler devices that divide-down the VCO output so that the PLL logic can process the signal (most PLL devices can only accept VCO inputs up to a couple of hundred MHz). The dual-modulus architecture basically allows fractional division of the VCO to allow small frequency steps (e.g., 5 KHz) to be programmed. These prescaler/PLL combinations can cause the PLL divider to be split into two dividers, which must sometimes be dealt with in the PLL register conversion logic when calculating a PLL register setting from a desired operating frequency value.

Finally, some PLLs feature still other configuration registers which can affect the configuration of the phase comparator or allow control of general purpose I/O signals (as is the case with the PLL used on the UX-129).

The reference oscillator is one of the controlling factors in the determination of minimum frequency step in the VCO output. Typically, the ICOM PLLs operate off of a 5 KHz base reference which is derived

from a 5.12 to 12.8 MHz oscillator (depending on the particular module) and a reference divider that is configured to produce a 5 KHz reference. If the PLL has a reference divider, this must be configured before PLL data can be sent.

All of the PLL devices used in the UX modules can be configured once at power-up and those configurations will be retained until later modified, or power is removed. However, the ICOM protocol is to set all of the configurations every time the PLL "N" divider is modified. This is a fail-safe method which ensures that the PLL will at least recover to normal operation on the next frequency change if its configuration is corrupted. The overhead for configuration is not excessive if the ICOM clock timings are used so I haven't tried to investigate how the modules might perform otherwise.

PLL Calculations

From my earliest investigations into the IC-901 behavior, I developed a means of calculating PLL values based on the empirical bit patterns that I had observed. Now that I've studied the actual PLL device datasheets and have a greater understanding of the PLL bit definitions, little has changed regarding how the bits are calculated. Basically, one starts with a base PLL value (a 20 bit HEX value) that corresponds to a specific RX frequency (the base frequency) which is used to calculate the frequency difference between the desired frequency and the base RX frequency. Since the PLLs all operate with 5 KHz channel steps (the UX-129 PLL has 5 KHz steps, but the VCO is doubled for transmit and receive so the module operates on a 10 KHz minimum step), the frequency difference is then divided by 5 KHz and the result is added to the base PLL value. If the desired frequency is for transmit, then a TX offset is added or subtracted, which is a fixed value for each band module that relates to the receiver IF frequency. The resulting value is then sent to the PLL "N" divider register to set the PLL operating point. The following table lists the values needed for each of the UX modules:

UX Module	Base Freq.	Base PLL (hex)	TX offs (hex)	Mod bit	PLL Init	Bit Order
UX-19	28.000 MHz	0x01e3b	0x085b (-)	7 *	0x1325	msb first
UX-59	40.000 MHz	0x02a2e	0x0aee (-)	7 *	0x1325	msb first
UX-29	136.000 MHz	0x05cd0	0x0d70 (+)	none	none	msb first
UX-39	220.000 MHz	0x11e70	0x0d70 (+)	none	none	msb first
UX-49	400.000 MHz	0x1266a	0x1216 (+)	none	none	msb first
UX-129	1240.000 MHz	0x1af04	0x355c (+)	7	see notes	lsb first

UX-129 has several initialization frames:

Ref osc init:	0x88500	
"HL" init:	0x00	(only 4 bits sent)
"GPIO" init1:	0x0c	(only 4 bits sent)
"GPIO" init2:	0x0f	(only 4 bits sent)

** The UX-19 and UX59 PLL register is left shifted one bit to align with the divider bits after all PLL calculations have been performed*

PLL_N (RX) = $((F_{op} - F_{base})/5\ KHz) + Base\_PLL$

PLL_N (TX) = $((F_{op} - F_{base})/5\ KHz) + Base\_PLL + TXoffs$

The "Mod bit" column indicates if (and where) a '0' bit must be inserted into the PLL-N code to adjust the PLL divide code to account for a dual-modulus divider. For example, if bit 7 is the modulus bit, a zero must be inserted into the bit pattern by shifting the PLL-N bits [20:7] one bit toward the msb, leaving bits [6:0] unchanged and bit 7 = 0. The PLL bits are arranged as 20 bit fields, but the various PLL devices actually use different register widths. The extra bits are simply shifted out of the PLL register. Note that the UX-129 requires the lsb be shifted first. This means that the application software must either bit reverse the value at run time (as would be needed if a microcontroller SPI interface were

used), or a separate set of clocking functions would be needed for the UX-129 to clock the PLL data lsb first. The latter is how I implemented the UX-129 interface.

As an example, the PLL code for 52.525 MHz (UX-59) TX would be calculated as:

((52,525,000 – 40,000,000)/5000) + `0x02a2e` – `0x0aee` = `0x2909`

Before sending to the PLL resister, a zero must be inserted into bit 7 yielding `0x05209` as the PLL divide register. The UX-59 further requires that the PLL be left shifted one bit, which gives the final PLL-N code of `0x0a412` to transmitting on 52.525 MHz.

The Mechanics of PLL Updates

Just sending a single set of PLL updates isn't enough to properly operate the UX module unless it is only required to receive on a single frequency. Since the PLL must be adjusted for every TX/RX cycle, the system controller must be able to send the relevant PLL data whenever a transition is needed between RX and TX. Further, the operation of the PLL and VCO must be considered during these transitions. The main issue regards the step performance of the VCO/PLL combination. Since the VCO/PLL form a feedback control loop, step changes require some minimum settling time. During this time, the VCO frequency is rapidly changing and may experience over/under-shoot as the loop settles. This can be extremely undesirable in transmit mode, so steps need to be taken to prevent transmitting at an unknown frequency.

The best approach would be to monitor a lock signal from the PLL and engage the TX amplifiers (via the PTT3 bit in the module control field) after the PLL is in-lock. While the expansion modules (the 2M SSB module in particular) offer an un-lock signal that can be monitored by the control processor, the FM modules do not have the lock-status available. The only other alternative is to wait-in-the-blind for some period of time for the PLL to settle before activating the module PTT3 signal. Thus the protocol is to send the PLL data for TX with the PTT3 = 0, wait a certain amount of time for the VCO to settle, then send the PLL data again, with PTT3 = 1. The trick is in determining the settling time for the VCO. From empirical measurements of the IC-901, 10ms seems to be what ICOM uses as a reasonable settling time.

One must be aware that there is a latency involved in the process of shifting from receive to transmit and vis-à-vis. Generally speaking, a minimum delay of 60 bit clocks plus 10ms to go from RX to TX (about 22ms), or about 12ms to go from TX to RX (this doesn't include any delay introduced by the processor in recognizing the transition between TX/RX). These latencies would be difficult to notice in an analog transceiver application, but might require some attention for digital modes.

UX-92 Module Overview

The UX-92 "expansion" module is fundamentally different from the FM-only modules. Aside from the differences in the modulation, there are many different configuration registers for the UX-92 vs. the two basic register types of the FM-only modules. The Front Unit for this module (shown in Figure 15) has a total of four OPC-179 cable connections to accommodate the additional interface signals required to facilitate the features offered by the UX-92. While the basic serial transfers are similar to those of the FM-only modules, there are some important differences, as discussed below.

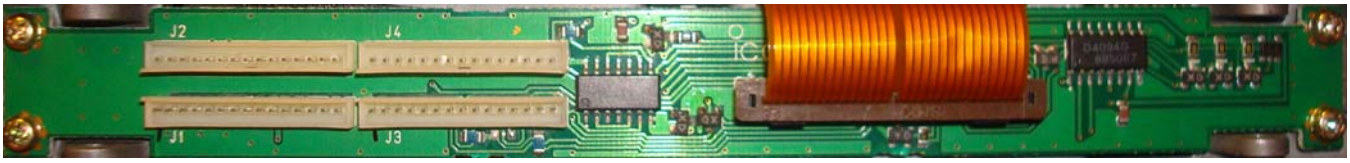
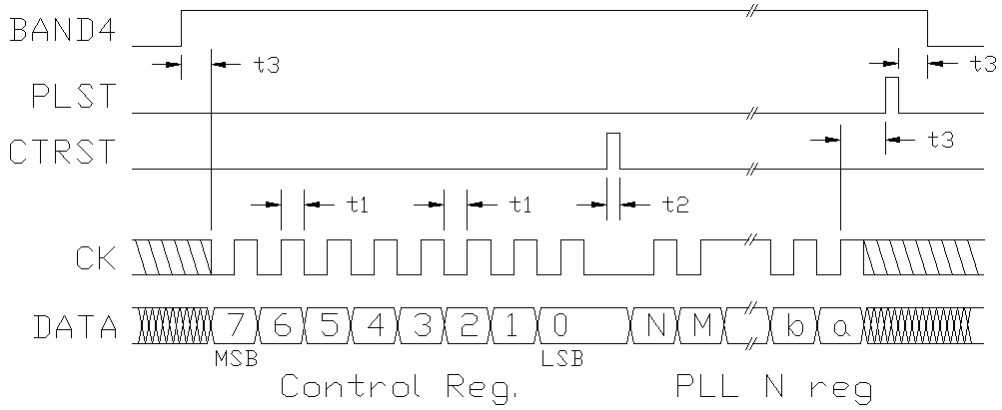


Figure 15. ICOM UX-92 module "Front Unit"

The ICOM UX-92 is a 2M SSB transceiver module and as such, there are several aspects of the module controls that are non-existent for an FM-only module. In addition, the modulation input to the UX-92 is different from the FM-only modules (e.g., no pre-emphasis for SSB modulation) as was mentioned previously in this document.

For the UX-92, the CK and DATA signals operate in a similar fashion as with the FM-only modules, however STB is not used. Instead, various strobe signals (CTRST, SSBST, PLST, and RITST) found on the expansion bus are used to strobe the various serial data formats. Figure 16 illustrates the serial transfer model for the expansion modules.



t1	clock half-period duration, 104µs (min)	t2	strobe width, 10µs (min)
D[7:0]	Control data (see text)	t3	clock setup/hold time, 104µs (min)
PLL Data:			
D[N:a]	PLL data (20 bits, typ. "N" = msb (first bit to shift)		

Figure 16. Expansion Module serial data diagram.

These transfers require the microcontroller to activate the appropriate band signal (BAND4 = 1 for the UX-92) during data transfers and pulse the various strobe signals depending on the Main Unit device

that is to be accessed (the pulses follow the last data bit transferred). The following table lists all of the controllable circuits that make up the UX-92:

Control Description	Data Format (see text)	Strobe
Control data (CDAT)	8 bits, MSB first	CTRST
SSB control data (SDAT)	8 bits, MSB first	SSBST
PLL (coarse frequency control)	15 bits, MSB first	PLST (CDAT[1] = 0)
FDA (fine frequency control)	8 bits, MSB first	PLST (CDAT[1] = 1)
SDA (squelch)	8 bits	RITST (SDAT[7:6] = 01)
RDA (RIT/XIT)	8 bits	RITST (SDAT[7:6] = 10)

As shown above, PLST and RITST perform double-duty acting as the strobe signal for one of two different registers based on the status of control data bits. This indicates that the control data transfers must be completed prior to loading these other resources. The control data registers produce logic signals that are used to control the SSB features and strobe steering.

Because this unit is AM based, the tuning is much more critical than for FM. This necessitates a much finer tuning step to than is available on the FM-only modules. Because of the difficulties in producing PLL circuit with increasingly smaller minimum steps, the UX-92 adopted a multifaceted approach to managing the tuning step size. First, the PLL was designed to produce 5 KHz steps, and is controlled in much the same fashion as the PLLs used in the FM-only modules.

The architecture of the UX-92 PLL is quite different, however, and features a reference oscillator and a down-conversion oscillator. The Reference oscillator establishes the 5 KHz frequency step, while the down-conversion oscillator is applied to the VCO output via a mixer and filter to produce the PLL-N divider input. The 5 KHz steps are then subdivided by tuning the down-conversion oscillator to produce an approximate minimum step of about 15 HZ using two separate analog tuning voltages produced by the FDA and RDA D/A converters.

The FDA converter is configured to produce 100, 50 Hz tuning steps to form the base minimum tuning step. The FDA is an 8-bit shift register that drives a simple R-2R ladder D/A that feeds the reference oscillator tuning circuit. Further refinement of the operating frequency comes from the RDA register. RDA is another simple 8-bit D/A circuit that also drives the PLL reference oscillator over a range of ±63 steps. However, the RDA adjustments result in RIT/XIT tuning steps of approximately 15 Hz increments due to the different scaling applied to the RDA signal applied to the down-conversion oscillator. Of course, the RIT tuning range overlaps the FDA range by a considerable degree, spanning almost 2 KHz.

The SDA is yet another simple D/A converter that sets the squelch threshold in 32 steps (as implemented in the IC-901). Even though this register has 8 bits, only the most significant 5 bits are used (except for step setting #32, which uses all 8 bits).

UX-92 Control Protocols

There are several registers that require attention on the UX-92 making it much more complicated to control than any of the FM-only UX modules. Some of these differences are obvious, while others can

be more difficult to discern. However, the controls can be broken down into three distinct categories to simplify the control process: First, the module control registers must be asserted. Next, the operating frequency is adjusted, with the squelch control being last on the list.

UX-92 Control Registers

The UX-92 features two 8-bit control registers:

Bit#	CTRST (CDAT)	SSBST (SDAT)
7	mode1 (mode[1:0] = 00 is n/a, 11 is CW)	not used
6	mode0 (01 is LSB, and 10 is USB)	RIT select _____ Steers RTIST to RDA or SDA
5	If 1, main, else sub	SQU select __/ (these bits can not both = 1)
4	If 1, module power on, else off	If 1, slow AGC, else fast
3	If 1, RF power = high, else low	RFGa: if 1, RF atten = med. RFG[b:a] = 11 prohibited
2	not used	RFGb: if 1, RF atten = high. RFG[b:a] = 00, atten off
1	If 1, TX mode, else RX	If 1, Noise blanker on
0	If 1, steers PLST to FDA, else to PLL	If 1, RIT else RIT/XIT

Aside from the direct controls present in these registers, they each feature steering bits to control the routing of some of the strobe lines. In particular, the RITST strobe accesses the RIT D/A register (RDA) or the squelch D/A register (SDA) depending on the status of bits 5 and 6 of the SDAT register. Also, the PLST strobe accesses either the PLL (if CDAT[0] = 0) or the fine tuning D/A register (FDA) if CDAT[0] = 1.

The bit functions are relatively straightforward for most of the control bits. With the exception of the steering bits, the remaining controls are direct-action which is to say that the action of the bits is immediate and no other serial data transfers are required.

UX-92 Operating Frequency

The operating frequency of the UX-92 is more difficult to calculate because of the increased tuning resolution and the complicated nature of the tuning circuits. There are three separate register systems that each influence the operating frequency as previously discussed. Of course, the main influence is from the PLL registers, with the FDA and RDA registers offering decreasing levels of influence. The separated control of the operating frequency requires the controller software to break out the frequency calculations into 3 distinct results. It must calculate the 5 KHz PLL register values, followed by the 50 Hz step FDA register value, and finally, the 15 Hz step RDA register values. Other complications to these calculations derive from how to implement the RIT feature, and the fact that the modulation mode influences the frequency calculations.

The basic algorithm I have constructed starts with the operating frequency and adds an offset based on the modulation mode. Next, the 5 KHz PLL values are calculated. Finally, the remainder of the 5 KHz calculation is divided into 50 Hz and 15 Hz steps to arrive at the FDA and RDA register values. Once all of the calculations are made, these values are all sent to the module.

The UX-92 PLL, when considered alone, operates much the same as the FM-only modules. It consists of a PLL chip and a VCO which establish the module operating frequency to a resolution of 5 KHz. The PLL chip, MC14515, features reference divider and N divider registers that are each 14 bits wide plus an

additional bit (at the lsb position) to select the reference register, lsb = 1, or the PLL N register, lsb = 0. Adding the register select bit brings the PLL register transfers to 15 bits total and it uses an msb-first shift protocol.

The easiest way to handle the PLL is to use a 16 bit, unsigned integer to hold the binary value of the PLL register. When the PLL calculations are completed, shift the 16 bit register left one bit leaving the lsb = "0" for PLL N data, or set the lsb to "1" for reference (PLL init) data. Then shift the entire 16 bits, msb first, to the PLL device. The following table illustrates the values used to control the PLL (Base PLL and PLL init are not right shifted 1 bit):

					MOD_offset (LSB = 0)	
UX Module	**Base Freq.**	**Base PLL (hex)**	**PLL Init**	**Bit Order**	**USB**	**CW**
UX-92	139.9965 MHz	0x00d5	0x0400	msb first	+3 KHz	+2.2 KHz

The PLL-N register formula is: PLL_N = INT((F_{op} + MOD_offset – F_{base})/5 KHz) + Base_PLL. To calculate The FDA value, use this formula: FDA = ((F_{op} + MOD_offset – F_{base})/5 KHz) - INT((F_{op} + MOD_offset – F_{base})/5 KHz)) * 100. This is simply the fractional part of the 5 KHz remainder times 100. Finally, if one desires to calculate the nearest 15 Hz step, take the fractional part of the FDA result, and multiply by 50/15, the integer portion of which which becomes the RDA value (RIT or XIT must be enabled for RDA to be active).

My interface applications tend to utilize a VFO register that holds the operating frequency as packed BCD values or a long (32 bit) integer value. This drives my algorithms to work against the minimum frequency step resolution of the system with the RIT/XIT feature handled as a modifier to the VFO setting (i.e., the RIT/XIT is a separate register that is added or subtracted with the VFO when calculating the module register values). The IC-901, on the other hand, operates on a 50 Hz step, and the RIT/XIT feature is handled separately. In my opinion, which implementation to use is purely an esoteric issue.

UX-92 Squelch

The squelch register shares the RITST with the RDA register. It is an 8-bit register that encodes the squelch value as a number between 0 and 32. The squelch value is encoded as 5 bits (0-31) and it is left shifted 3 bits so that the msb of the squelch value aligns with the msb of the register – the value for squelch position "32" is encoded as "1"s in all 8 bits of the register (0xff). Squelch values 0 – 31 have "0"s in bit positions 2:0 of the squelch register. The progression of squelch settings is thus 0x00, 0x08, 0x10, 0x18, 0x20, … , 0xf0, 0xf8, 0xff. A squelch value of 0x00 corresponds to fully open, while 0xff is fully closed.

UX-92 Summary

The ICOM protocol generally sends PLL data first, followed by other control register data fields. Of course, the CTRST field is needed to send PLL data. The easiest way to approach controlling the UX-92 is to group the control fields by function. The basic functions are Control Bits, Frequency, RIT/XIT value, and Squelch. Control bits are those bits contained in the CDAT and SDAT registers and include AGC, RF gain, noise blanker, RIT/XIT mode, modulation mode, module power, RF power, TX enable, and strobe steering.

The initialization frames for initial power would be as follows:

- Send CDAT with all zero bits.
- Send PLL N register data of all zero bits.
- Send CDAT with PLL steering selected and all other bits set as desired (including module power on).
- Send PLL init frame.
- Repeat CDAT and PLL init frames.
- Send CDAT with PLL steering selected and all other bits set as desired.
- Send PLL N-register frame for operating frequency.
- Send CDAT with FDA steering selected and all other bits set as desired.
- Send FDA register frame.
- Enable RDA steering in SDAT frame.
- Send RDA value frame.
- Enable SDA steering in SDAT frame.
- Send SDA value frame.

To change frequency:

- Send CDAT with PLL steering selected and all other bits set as desired (including module power on).
- Send PLL init frame.
- Send CDAT with PLL steering selected and all other bits set as desired.
- Send PLL N-register frame for operating frequency.
- Send CDAT with FDA steering selected and all other bits set as desired.
- Send FDA register frame.
- Enable RDA steering in SDAT frame.
- Send RDA value frame.

To change from RX to TX or TX to RX:

- Send CDAT with PLL steering selected and all other bits set as desired (including CDAT[1] set to the new TX status).
- Send PLL init frame.
- Send CDAT with PLL steering selected and all other bits set as in previous frame.
- Send PLL N-register frame for operating frequency.
- Send CDAT with FDA steering selected and all other bits set as in previous frame.
- Send FDA register frame.
- Enable RDA steering in SDAT frame.
- Send RDA value frame.

To change one of the radio controls (RF gain, AGC, etc…) simply send the SDAT or CDAT register as appropriate.

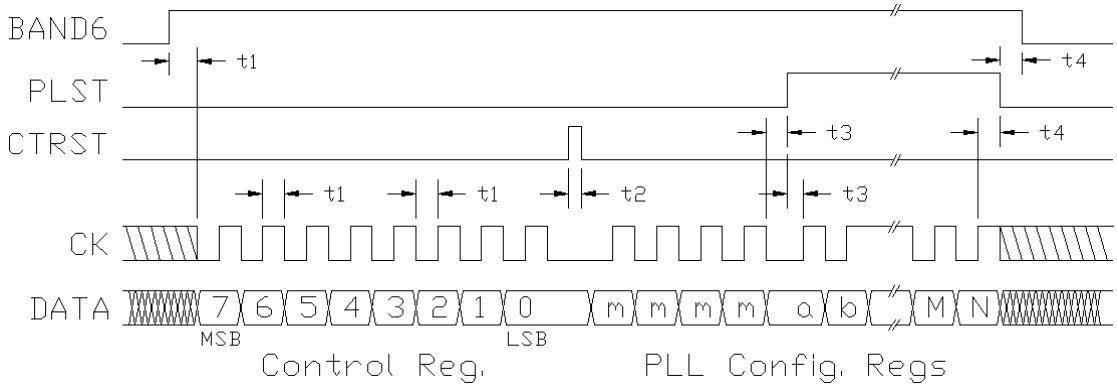
UX-R91 Module Overview

The UX-R91 "expansion" module is fundamentally different from all of the other IC-900/901 modules. Even though it is receive only, the PLL architecture is much more complicated due to the wide bandwidth it must cover (there are different combinations of three VCOs and two doublers needed to cover all of the frequency ranges of the UX-R91). The Front Unit for this module has a total of four OPC-179 cable connections to accommodate the additional interface signals required to facilitate the features offered by the UX-R91 (as is the case for the UX-92). While the basic serial transfers are similar to those of the FM-only modules, there are some important differences, as discussed below.

The UX-R91 covers six frequency bands: the AM broadcast band (0.5 to 1.6 MHz), the FM broadcast band (WBFM, 76 – 108 MHz), the aircraft band (AM, 108 – 137 MHz), the 2M band (NBFM, 137 – 200 MHz), the 220 band (NBFM, 200 – 236 MHz), the 440 band (NBFM, 300 – 500 MHz), and the 800 band (NBFM, 800 – 950 MHz). The following table lists all of the controllable circuits that make up the UX-R91:

Control Description	Data Format (see text)	Strobe
Control data (CDAT)	8 bits, MSB first	CTRST
PLL (coarse frequency control)	60 bits, LSB first	PLST (CDAT[1] = 0)
VOL (stereo output volume)	18 bits, LSB first	PLST (CDAT[1] = 1)

The serial data protocols are described in Figure 17. Since the module can not transmit, there is no provision for it to be connected as a main band, and therefore only sub-band interface signals are used. In addition to the power and antenna connections, the module features connections for right and left audio outputs from the WBFM demodulator. These outputs (as well as DETB, a mix of the right and left channel audio) are controlled by the volume (VOL) serial data register.



t1	clock half-period duration, 104µs (min)	t3	PLST setup/hold time, 10µs (min)
t2	strobe width, 10 µs (min)	t4	BAND6 hold time, 10µs (min)
D[mmmm]	PLL mode bits ("1000" typ.)	D[7:0]	Control data (see text)
D[N:a]	PLL data (56 bits, typ. "a" = lsb (first bit to shift)		

Figure 17. UX-R91 expansion module serial data diagram.

As shown above, PLST performs double-duty acting as the strobe signal for one of two resources based on the status of a control data bit. This indicates that the control data transfers must be completed prior

to loading these other resources. The control data registers produce logic signals that are used to control the module features and strobe steering.

As mentioned previously, the architecture of the UX-R91 PLL is quite different from any other UX module and features a reference oscillator input, multiple VCO sources, and several general purpose outputs. The reference oscillator/divider establishes the frequency step (which is generally different for each band), while the GP outputs select the VCO/front-end path for a given band.

UX-R91 Control Registers

The UX-R91 features one 8-bit control register:

Bit#	CTRST (CDAT)
7	not used
6	mode (0 is FM, and 1 is AM)
5	not used
4	If 1, module power on, else off
3	not used
2	not used
1	If 1, select VOLST, else select PLLST
0	not used

UX-R91 Volume (WBFM Only)

The UX-R91 features a line-level, stereo output for the WBFM (76 – 108 MHz) band. A volume/balance control is implemented using a dual, digital level control I.C., the TC9154. This IC allows 35 distinct amplitude settings that are calibrated in dB. The attenuation step is 2dB and the range is 0dB to -68dB (which is essentially muted). The device features an 18 bit control register which holds all of the control bits. This register is loaded by setting CDAT[1] = 1, shifting the 18 control bits, then pulsing PLST high then low. Figure 18 details the bitmapped field formats for the volume device.

```
VolHi  VolL
/     \/   \
h     lh   l
VVVVVVVvvvvv0LR000
^           ^^    ^
|_ bit 0     ||    |_ PLST = pulse high
             ||_ Right select
             |_ Left select
```

Figure 18. UX-R91 VOL frame field definitions.

The volume register implements the desired level setting as a “high” order and “low” order setting. The low order setting selects 0 to -8 dB in 5 steps, while the high-order setting selects 0 to -60 dB in 7 steps. The two level values add to produce the overall level. The steps are implemented as a “1 of 7” binary code for the high-order value, and a “1 of 5” binary code for the low-order value. For example, the bit-pattern for a few level settings are as follows:

```
0 dB, Right:            -24 dB Right:           -68 dB Right:
VVVVVVVvvvvv0LR000      VVVVVVVvvvvv0LR000      VVVVVVVvvvvv0LR000
100000010000001000      001000000100001000      000000100001001000
```

Balance is implemented by applying a differential level setting to the right and left channels. The IC-901 implements these controls as step increments or decrements based on a button press on the control unit. Thus, there aren't really any calculations to make, just increment/decrement one or the other (for balance) or increment/decrement both together (volume). If one implements level and balance registers to control this feature, then it would be necessary to convert those microcontroller registers to the "1 of N" code format for each of the channels.

The UX-R91 provides a mix of the right and left channel output jacks for the DETB audio that is available at the Front Unit connector, so the volume and balance will affect this audio source even if the jacks are not used (DETB is, of course, a monaural mix of the right and left channels).

UX-R91 Operating Frequency

Even though the UX-R91 PLL/VCO sub-system is rather complicated, the frequency controls are relatively straightforward. All of the possible PLL configurations are transferred in a single 60 bit frame (even though the LM7005 PLL chip supports other frame lengths, this is the only one used for this application). There are a lot of bit-fields in the 60-bit frame, but they are reasonably straightforward to assemble.

Because of the multiple bands supported by this module, the PLL equation is best handled by sorting the calculation into one of 7 cases, based on the operating frequency (F_{op}). The other fields that are dependent on F_{op} are the R_{div} register, and the GP output register. Finally, the CDAT register has the modulation mode bit and the VOL/PLL steering bit that must be configured.

The PLL update stream consists of a CDAT transfer followed by a PLL frame (as depicted in Figure 17). The bit field diagram of Figure 19 illustrates the fields that are transferred with the PLL frame.

```
mmmm D0-------------D17 **vVs* R0---------R13 tT GP outs *lLeEpPzZ
     /                \        /             \    /     \
1000 abcdefghijklmnopqr 001010 ABCDEFGHIJKLMN 00 0123456 000000000
^   ^                                                          ^^
|   |____ PLST = "1"                                    bit 59 _||
|                                                              |
|_ bit 0                                             PLST = "0" __|
```

Figure 19. UX-R91 PLL frame field definitions. Gaps between bit-fields are added for clarity.

Note that the LM7005 requires that the shift order be lsb first, so the bits illustrated in Figure 19 would be shifted first from the left side of the figure (bit 0 first), progressing to the right (bit 59 last). The D[r:a] bits are the PLL N-divisor value (r = msb, a = lsb), the D[N:A] bits are the reference divisor value (N = msb, A = lsb), and the D[6:0] bits are the GP outputs (which are used to switch between the different VCO and front end circuits). All other bits hold the values shown for all frequencies.

The PLL calculation is similar to the FM-only modules except that there are 5 different equations that are differentiated based on the desired F_{op}. Furthermore, the GP Outputs and reference divider value are other variables which all fold into the 7 different combinations needed to control the UX-R91 across its design frequency ranges. The PLL-N value (D[r:a]) equation follows the form of:

$D[r:a] = ((F_{op} - F_{base})/F_{step}) + PLL_{BASE}$

Where F_{base}, F_{step}, and PLL_{base} are determined by the value of F_{op}.

The following table lists the equation parameters for the seven band ranges of the UX-R91:

Freq. Range & Mod.		F_{base} (MHz)	F_{step} (KHz)	(18 bits) PLL_{base} (hex)	(14 bits) Ref (D[N:A])	(7 bits) GP out (hex)	Modulation CDAT[6]
0.5 – 1.7	AM	0.500	1.00	0x003bb	0x1900	0x7e	1
76 – 107.9	WBFM	76.000	5.00	0x03304	0x0500	0x7d	0
108 – 136.9	AM	108.000	12.50	0x0345c	0x0400	0x7b	1
137 – 199.995	NBFM	137.000	5.00	0x03c82	0x0500	0x7b	0
200 – 236.0	NBFM	137.000	5.00	0x03c82	0x0500	0x77	0
300 – 500.0	NBFM	137.000	5.00	0x03c82	0x0500	0x6f	0
800 – 950.0	NBFM	800.000	12.50	0x0e764	0x0400	0x5f	0

Note: CDAT[4] = 1 (module on) and CDAT[1] = 0 for the PLL frame (all other CDAT bits = 0)

As a software note, the easiest way to handle the PLL frame is to construct a serial driver function that shifts a long-integer (32 bits) by a variable number of bits (up to 18) via the data and clock pins of the processor. This one function could then be used to send each of the fields defined in Figure 19 making it a relatively simple task to make sure that the bit alignment and bit count are correct.

Closing Remarks

This document is a work in progress. I have made every effort to verify the integrity of the information presented, but it is inevitable that an error or two yet linger herein. As well, I am still developing applications for the UX modules and am finding that there are still details to learn, even though I have been studying them for many years.

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