1. ATTACHMENTS

-- QRN4506A Station Control Module	31-SP5253003
•Circuit Board Detail (Component Side)	(Sheet 1 of 3)
•Circuit Board Detail (Solder Side)	(Sheet 2 of 3)
•Schematic Diagram	(Sheet 3 of 3)
•Parts List	31PL-SP5253003

2. DESCRIPTION

The QRN4506A Station Control Module is a Motorola MICOR™ Base/Repeater remote control chassis support module. The module provides the following major functions.

- •Amplifies station receiver discriminator signal for use by other modules.
- •Buffers line audio for application to the station transmitter.
- •Sets audio paths according to the mode selected.
- •Integrates control functions from other modules for control of station transmitter keying.
- •Delays Line PTT functions (delay period is selectable) for compatibility with line modems and SECURENET XL™ equipment.
- •Provides front panel controls for local operation.

3. THEORY OF OPERATION

3.1 DISCRIMINATOR AMPLIFIER AND LINE AUDIO BUFFER

3.1.1 The receiver discriminator output is applied to pin 7 of the station control module. Operational amplifier U1A amplifies the received signal by 6.5 dB. The output signal of U1A is also dc offset to half the A+ supply

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voltage. This amplified signal is output, via module pin 8, to the squelch gate module.

3.1.2 The line audio input from the line driver module is applied as MIC HI at pin 2 of the station control module. This audio signal bypasses gate U2A through jumper J19 and is applied to operational amplifier U1B. U1B buffers the line audio signal. The buffered line audio signal is applied to gate U2C. If the station is in clear mode (DVP CONTROL module pin 9 is logic high) and repeater PTT is inactive (RPTR PTT module pin 11 is logic high) and no data is detected (DATA DETECT module pin 10 is logic low), U6B-9 is high causing U2C to gate the buffered audio signal out to module pin 6 where it is routed to the station exciter. For special applications, U2B gates a second audio line which is routed to the station exciter.

3.2 TRANSMITTER KEYING

3.2.1 An active logic low at module pin 11 (RPTR PTT) or module pin 3 (LINE PTT) or module pin 14 (LOCAL PTT) activates module outputs at pin 19 (KEYED A+), pin 21 (DELAYED KEYED A+), and pin 17 (KEYED A-). These three outputs are required to key the station transmitter.

3.2.2 If any of the PTT input signals are active (logic low), U6C-10 is low. The signal at U6C-10 is inverted by U7D, and inverted again by U9A. U9A drives Q1 on which provides KEYED A+ output. KEYED A+ is also applied to U13B-8 and U10B-11. The high-level KEYED A+ signal sets U13B-12 low. This low turns on Q2 which produces DELAYED KEYED A+ output. With module pin 16 (PL ENABLE) active logic low, U5B-11 output is high impedance which allows DELAYED KEYED A+ to turn Q3 on, producing KEYED A- output. When PTT becomes inactive, KEYED A+ goes low causing U10B-11 to go low causing a low level 150 millisecond pulse at U13B-11. When the 150 millisecond pulse elapses, U13B-11 goes high causing U13B-12 to go high which turns off Q2, disabling DELAYED KEYED A+.

3.2.3 The three PTT input signals also control the PTT CONTROL output at module pin 13. An active LOCAL PTT or RPTR PTT causes U9C-10 to output a logic high to gate U2D-10. If LINE PTT is inactive, U2D-11 drives U5C-5 high. U5C-12 output goes low providing an active PTT CONTROL output. This output is routed to the F1-PL module. The F1-PL module outputs an active PL ENABLE signal which is applied as an input to the station control module to enable KEYED A-. If LINE PTT is active, U2D opens the path between U9C and U5C causing a high PTT CONTROL output. For Line PTT function, PL ENABLE is driven active low by a function tone decoder module.

3.3 ANTENNA SWITCH CONTROL

3.3.1 The antenna switch control signal (ANT SW module pin 15) is active during one of the following conditions:

- LINE PTT (module pin 3) or LOCAL PTT (module pin 14) is active low.
- KEYED A- (module pin 17) is low and RPTR PTT (module pin 11) is high.

3.3.2 An active LINE PTT or LOCAL PTT causes a high at U7F-13. This high causes a low U4A-3, which causes a high at U7E-11, which causes U5E-14 to output an active ANT SWITCH output signal.

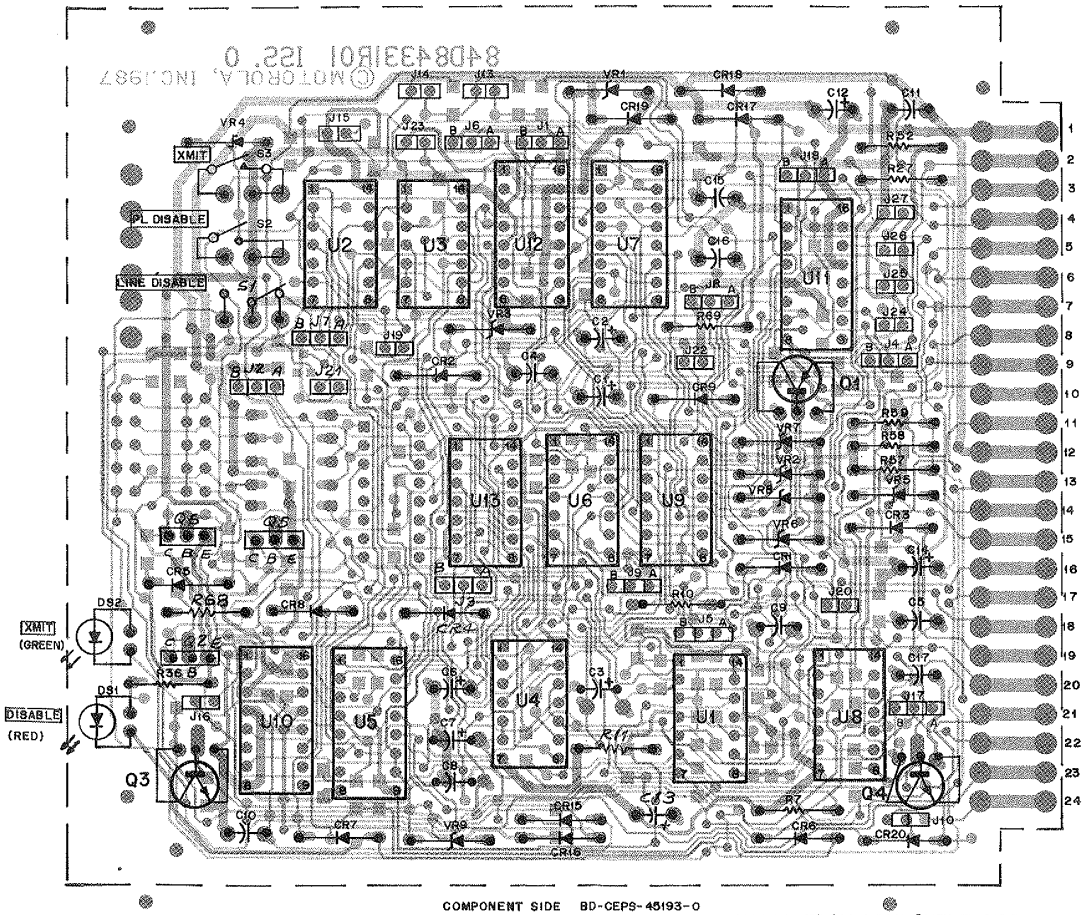
3.3.3 An active KEYED A- causes a low at U3D-12. If RPTR PTT is inactive, U13A-1 applies a low to U3D-13. Two low inputs to U3D cause a low at U3D-11, which is gated through U4A, U7E, and U5C producing an active ANT SW output. This KEYED A-/ANT SW logic sequence can be overridden by a Repeater PTT (or a Delayed Repeater PTT) function. The purpose of this override is to disable the antenna switch during Repeater PTT. During a Repeater PTT, RPTR PTT is active causing a high at U13A-6. Because U13A-6 is high, U13A-1 is high, which makes U3D-13 high, thus overriding the low input at U3D-12 and causing a high ANT SW output. When RPTR PTT goes from low to high, monostable U10A-7 outputs 270 millisecond low-level pulse to U13A-3. Immediately after the 270 millisecond pulse elapses, U13A-3 goes high causing U13A-1 to go low, which removes the override condition.

3.4 MODEM COMPATIBLE AND DELAYED LINE PTT

3.4.1 When Line PTT is activated, the station control module momentarily disables the station transmitter to avoid transmission of the fast train signaling produced by the line modem upon code detect.

3.4.2 A high to low LINE PTT signal causes a trigger pulse at monostable U12A-4. U12A-6 outputs a 50 millisecond high level pulse to monostable U12B-11. After 50 milliseconds, U12B-11 goes low triggering U12B which outputs a 240 millisecond high level pulse to U5A-7. U5A-10 is low which turns off Q3 disabling KEYED A-, and consequently turning off the station transmitter for the duration of the 240 millisecond pulse. The 240 millisecond pulse is required for 1 modem application. The pulse width can be adjusted, via jumpers J13 through J15, to 400 milliseconds for applications using two modems in tandem and to 180 milliseconds for XL stations.

3.4.3 If a Line PTT interruption occurs during coded repeater operation, the LINE PTT signal causes a trigger pulse at U12A-4. U12A-7 outputs a 50 millisecond low-level pulse. This output pulse turns Q4 off, making DELAYED LINE PTT inactive for the duration of the pulse. This signal is output at module pin 22 and is routed, as an input, to the F1-PL and squelch gate modules which delays a signal to turn off the transmitter for 50 milliseconds to allow transmission of EOM. (Note that jumper J17 is in position B when Delayed Line PTT function is used. Therefore, Line Disable function is not available.)



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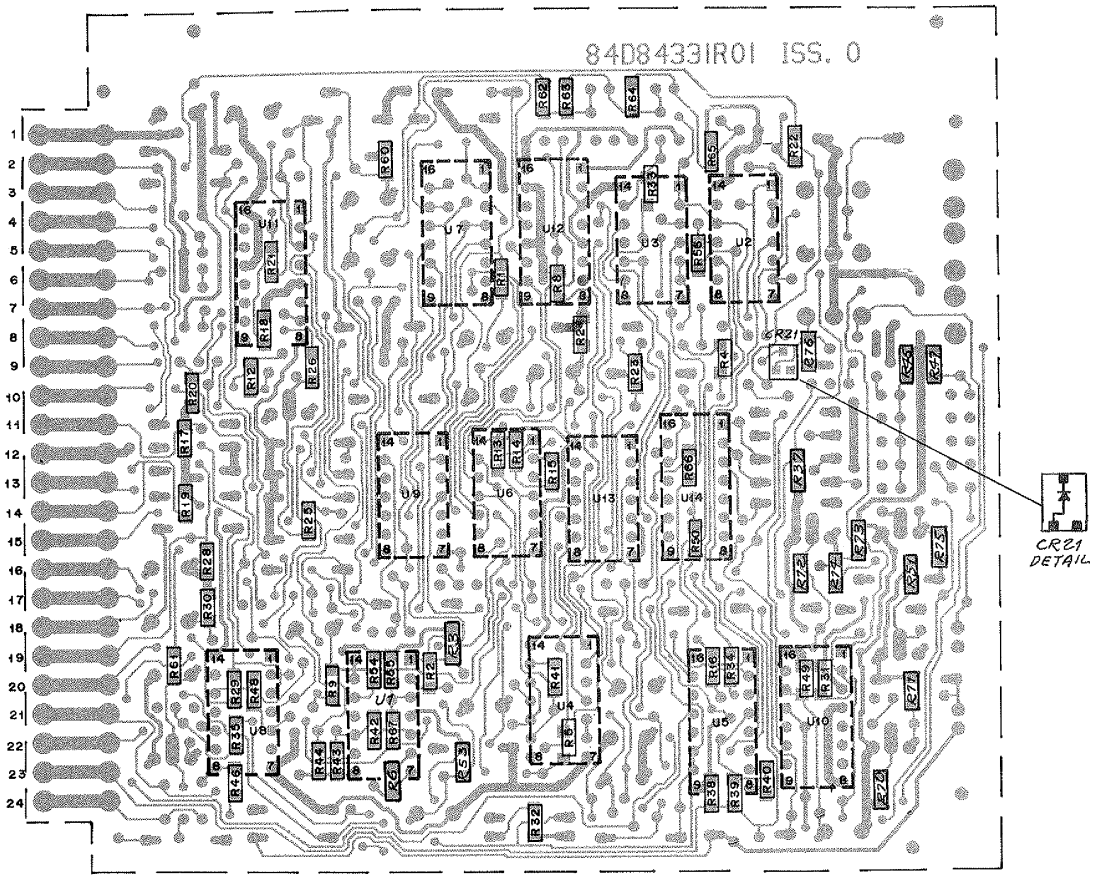

QRN4506A Station Control Module
Circuit Board Details and
Schematic Diagram
Motorola No. 31–SP5253003–2
(Sheet 2 of 3)
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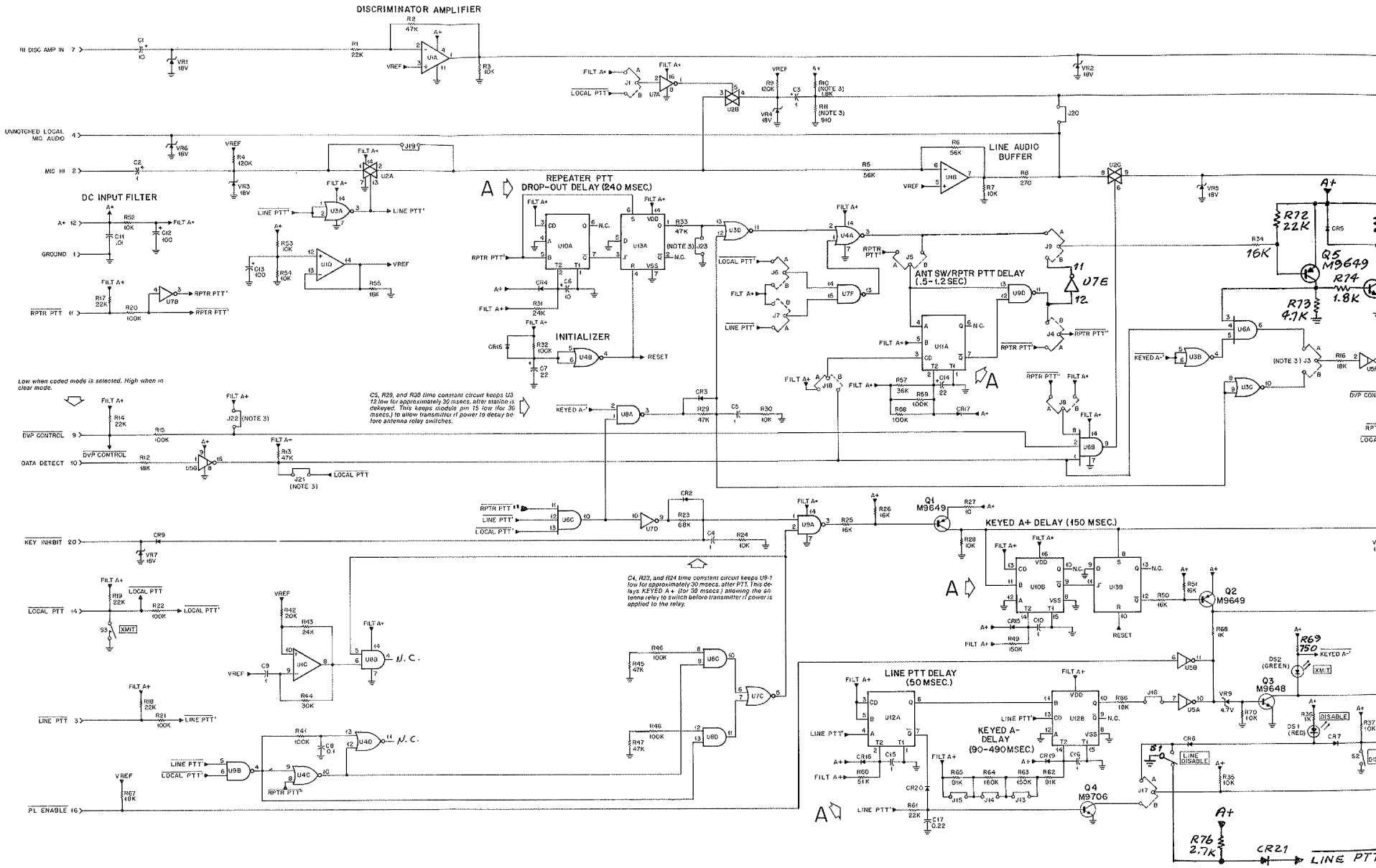
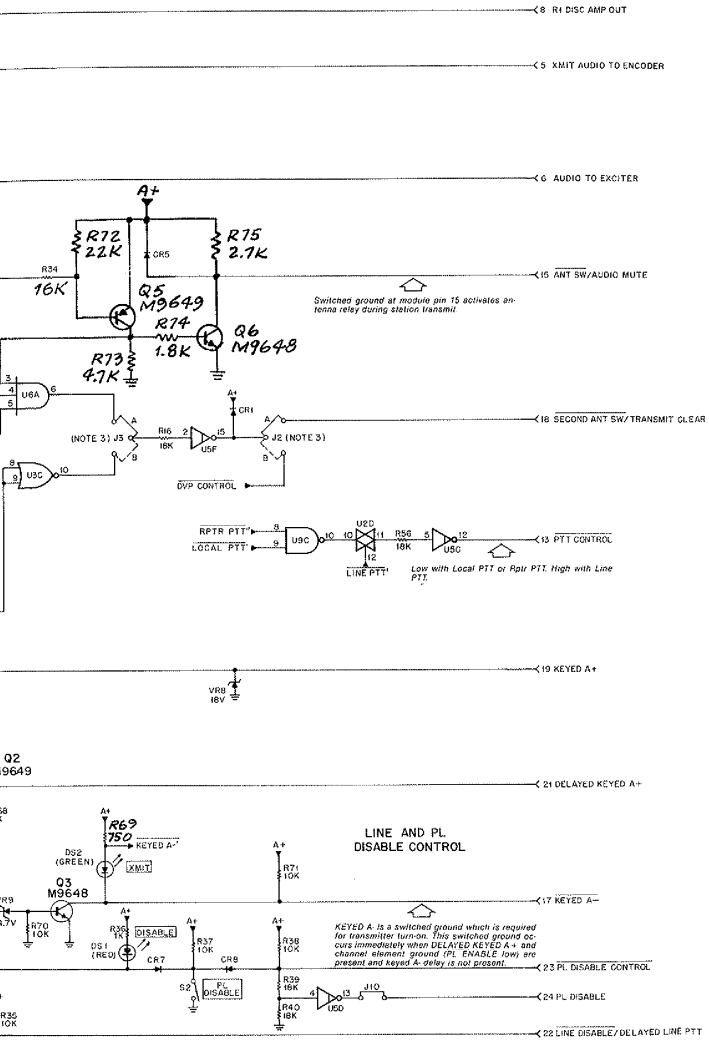
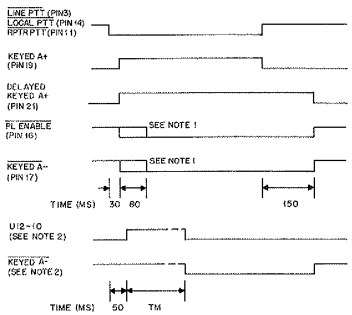

DISCRIMINATOR AMPLIFIER
RI DISC AMP IN 7
UNMOTCHED LOCAL MIC AUDIO 4
MIC HI 2
DC INPUT FILTER
A+ 12
GROUND 1
RPTR PTT 11
REPEATER PTT DROP-OUT DELAY (240 MSEC.)
RPTR PTT'
LOCAL PTT'
LINE PTT'
ANT SW/RPTR PTT DELAY (.5-1.2 SEC)
INITIALIZER
RESET
LINE AUDIO BUFFER
KEYED A+ DELAY (150 MSEC.)
LINE PTT DELAY (50 MSEC.)
KEYED A- DELAY (90-490 MSEC.)
DVP CONTROL 9
DATA DETECT 10
KEY INHIBIT 20
LOCAL PTT 14
LINE PTT 3
PL ENABLE 16
XMIT
DISABLE
LINE DISABLE
N.C.
Low when coded mode is selected. High when in clear mode.
C5, R29, and R30 time constant circuit keeps U3-12 low for approximately 30 msecs. after station is dekeyed. This keeps module pin 15 low (for 30 msecs.) to allow transmitter rf power to decay before antenna relay switches.
C4, R23, and R24 time constant circuit keeps U9-1 low for approximately 30 msecs. after PTT. This delays KEYED A+ (for 30 msecs.) allowing the antenna relay to switch before transmitter rf power is applied to the relay.

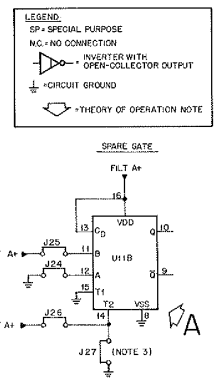


KEYED A- TIMING DIAGRAM



NOTE 1: KEYED A- IS ENABLED 30 MILLISECONDS AFTER THE REPEATER PTT OR LOCAL PTT IS ASSERTED OR 110 MILLISECONDS AFTER THE LINE PTT IS ASSERTED DUE TO PL ENABLE.
NOTE 2: KEYED A- IS DELAYED FOR TM MILLISECONDS AFTER A LINE PTT IS ASSERTED WHEN MODULE IS JUMPERED FOR MODEM INTERFACE OR XL ENCRYPTION (J16 IN).

TM = 180MS AS JUMPERED FOR XL (J13 & J14 IN; J15 OUT).
TM = 240MS AS JUMPERED FOR ONE MODEM (J13 OUT; J14 & J15 IN).
TM = 420MS AS JUMPERED FOR TWO MODEMS (J13 & J14 OUT; J15 IN).



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U10, U11, and U12 are dual retriggerable resettable monostable multivibrators. The output pulse duration of each monostable is determined by the external RC components connected to T1 and T2 inputs.

TRIGGER — Before an input trigger occurs, the Q output is low and the external timing capacitor is fully charged. When trigger input A goes low to high (while inputs B and C_D are held high) or trigger input B goes high to low (while input A is held low and C_D is held high), the monostable circuit rapidly discharges the external capacitor and sets the Q output high. The capacitor now begins charging through the external resistor. After one RC time constant, the capacitor is charged enough to trigger the Q output low.

RETRIGGER — If a trigger input occurs before the Q output returns low, the Q output remains high for a time constant period after the last retrigger.

RESET — A high to low on C_D causes the monostable to rapidly charge the external capacitor. The Q output is reset low (pulse shortened). If C_D is held low, trigger inputs at A and B are inhibited.

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NOTES:

1. Unless otherwise indicated: resistor values are in ohms; capacitor values are in microfarads.
2. This diagram shows positive logic:
   Logic "1" ≥ 11 V dc
   Logic "0" <2.5 V dc
3. Resistors R10 and R11 are removed when QRN4530A INTERCONNECT BOARD IS NOT used. Jumpers J2, J3, J21, J22, J23 and J27 are not used.
4. Refer to Table 1 for Integrated Circuit types and power connections for this board.
5. Refer to Table 2 for jumper usage details.

Table 1. Integrated Circuits Power Connections, Motorola Type Numbers, and Descriptions

Ref. Symbol	Total Pins	A+	FILT A+	GND	Motorola Type No.	Description
U1	14	4		11	21K32	Quad Differential Input Operational Amplifier
U2	14		14	7	84L48	Quad Analog Switch
U3, 4	14		14	7	87K09	Quad 2-Input NOR Gate
U5	16	9		8	22M75	Peripheral Hex Driver Array (Open Collector Outputs)
U6	14		14	7	84L60	Triple 3-Input AND Gate
U7	16		16	8	84L61	Hex Gate
U8	14		14	7	84L51	Quad 2-Input AND Gate
U9	14		14	7	84K08	Quad 2-Input NAND Gate
U10-12	16		16	8	87K53	Dual Precision Monostable Multivibrator
U13	14		14	7	87K13	Dual D Flip-Flop

Table 2. Jumper Usage

Ref. Symbol	Status
J1	Normally position A; position B for SP application.
J2, 3	NOT USED
J4, 5	Normally position A; position B for SP application.
J6, 7	Normally position A; position B for Repeater PTT priority.
J8	Normally position A; position B enables line audio to exciter during clear mode Repeater PTT.
J9	Normally position A; position B for SP application.
J10	IN for PL Squelch; OUT for Carrier Squelch.
J11, 12	NOT USED
J13	Normally IN; OUT when one or two modems are used on line.
J14	Normally IN; OUT when two modems are used on line.
J15	Normally IN; OUT for XL station.
J16	Normally IN; OUT for no modem on line and non-XL station.
J17	Position B FOR XL REPEATERS; POSITION A ALL OTHERS.
J18	Normally position A; position B for SP application.
J19	Normally IN; OUT for SP application.
J20	Normally OUT; IN when QRN4530A INTERCONNECT BOARD IS NOT USED.
J21-23	NOT USED.
J24-26	Normally IN; OUT for SP application.
J27	NOT USED.

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PARTS LIST

REF SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, fixed: uF +-5% unless otherwise stated
C1	2311019A21	10 +-20% 35V
C2,3	2311019A09	1 +-20% 50V
C4,5	0811044A33	1 50/63V
C6	2311054F06	10 +-10% 15V
C7	2311054F10	22 +-10% 15V
C8	0811044A15	0.1 63V
C9,10	0811044A33	1 50/63V
C11	0811044A24	.01 63V
C12,13	2311019A46	100 +-20% 25V
C14	2311019A28	22 +-20% 35V
C15,16	0811044A33	50/63V
C17	0811044A29	0.22 50/63V
		DIODE: (SEE NOTE)
CR1 thru 9	4883654H01	silicon
CR10 thru 14		NOT USED
CR15 thru 20	4883654H01	silicon
CR21	4811058C11	silicon
		LIGHT EMITTING DIODE:
DS1	4888245C24	red
DS2	4888245C22	green
		CONNECTOR, male:
J1	2884318M07	3-contact
J2,3		NOT USED
J4 thru 9	2884318M07	3-contact
J10	2884318M06	2-contact
J11,12		NOT USED
J13 thru 16	2884318M06	2-contact
J17,18	2884318M07	3-contact
J19,20	2884318M06	2-contact
J21,22,23		NOT USED
J24,25,26	2884318M06	2-contact
J27		NOT USED
		TRANSISTOR: (SEE NOTE)
Q1,2	4800869649	PNP type M9649
Q3	4800869648	NPN type M9648
Q4	4800869706	NPN type M9706
Q5	4800869649	PNP type M9649
Q6	4800869648	NPN type M9648

PARTS LIST

REF SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		RESISTOR, FIXED: +-5% 1/8W; unless other stated
R1	0611024A81	22k
R2	0611024A89	47k
R3	0611024A73	10k
R4	0611024A99	120k
R5,6	0611024A91	56k
R7	0611009A73	10k 1/4W
R8	0611024A35	270
R9	0611024A99	120k
R10	0611009A55	1.8k 1/4W
R11	0611009A98	910 1/4W
R12	0611024A79	18k
R13	0611024A89	47k
R14	0611024A81	22k
R15	0611024A97	100k
R16	0611024A79	18k
R17,18,19	0611024A81	22k
R20,21,22	0611024A97	100k
R23	0611024A93	68k
R24	0611024A73	10k
R25,26	0611024A78	16k
R27	0611009A01	10 1/4W
R28	0611024A73	10k
R29	0611024A89	47k
R30	0611024A73	10k
R31	0611024A82	24k
R32	0611024A97	100k
R33	0611024A89	47k
R34	0611024A78	16k
R35	0611024A73	10k
R36	0611009A49	1k 1/4W
R37,38	0611024A73	10k
R39,40	0611024A79	18k
R41	0611024A97	100k
R42	0611024A80	20k
R43	0611024A82	24k
R44	0611024A84	30k
R45	0611024A89	47k
R46	0611024A97	100K
R47	0611024A89	47k
R48	0611024A97	100k
R49	0611024B02	150k
R50,51	0611024A78	16k
R52	0611009A01	10 1/4W
R53,54,55	0611024A73	10k
R56	0611024A79	18k

PARTS LIST

REF SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R57	0611009A86	36k 1/4W
R58,59	0611009A97	100k 1/4W
R60	0611024A90	51k
R61	0611024A81	22k
R62	0611024A96	91k
R63	0611024B02	150k
R64	0611024B03	160k
R65	0611024A96	91k
R66,67	0611024A79	18k
R68	0611009A49	1k 1/4W
R69	0611009A46	750 1/4 W
R70,71	0611024A73	10k
R72	0611024A81	22k
R73	0611024A65	4.7k
R74	0611024A55	1.8k
R75, 76	0611024A59	2.7k
		SWITCH, toggle:
S1,2	4083249K14	spdt
S3	4083249K16	spdt momentary
		INTEGRATED CIRCUIT: (SEE NOTE)
U1	5184621K32	quad operational amplifier
U2	5184887K73	quad bilateral switch
U3,4	5184887K09	quad 2-input NOR gate
U5	5183222M75	5V log to LED display interface
U6	5184887K28	triple 3-input AND gate
U7	5184887K82	functional hex gate
U8	5184887K75	quad 2-input AND gate
U9	5184887K08	quad 2-input NAND gate
U10,11,12	5184887K53	dual monostable multivibrator
U13	5184887K13	dual D-type flip-flop
U14		NOT USED
		VOLTAGE REGULATOR: (SEE NOTE)
VR1 thru 8	4883461E18	18V
VR9	4882256C03	4.7V
		NON-REFERENCED ITEMS:
	0983697M01	CONTACT, female; 24 used
	5483865R01	LABEL
	4583914G01	GUIDE, card; 2 used
	6484237R04	PANEL, front
	0310943J09	SCREW, locking: 4-40 x 5/16''; 2 used
	0984728L01	JUMPER, connector; 19 used