STATION CONTROL MODULE
MODEL TLN2423A

1. GENERAL DESCRIPTION

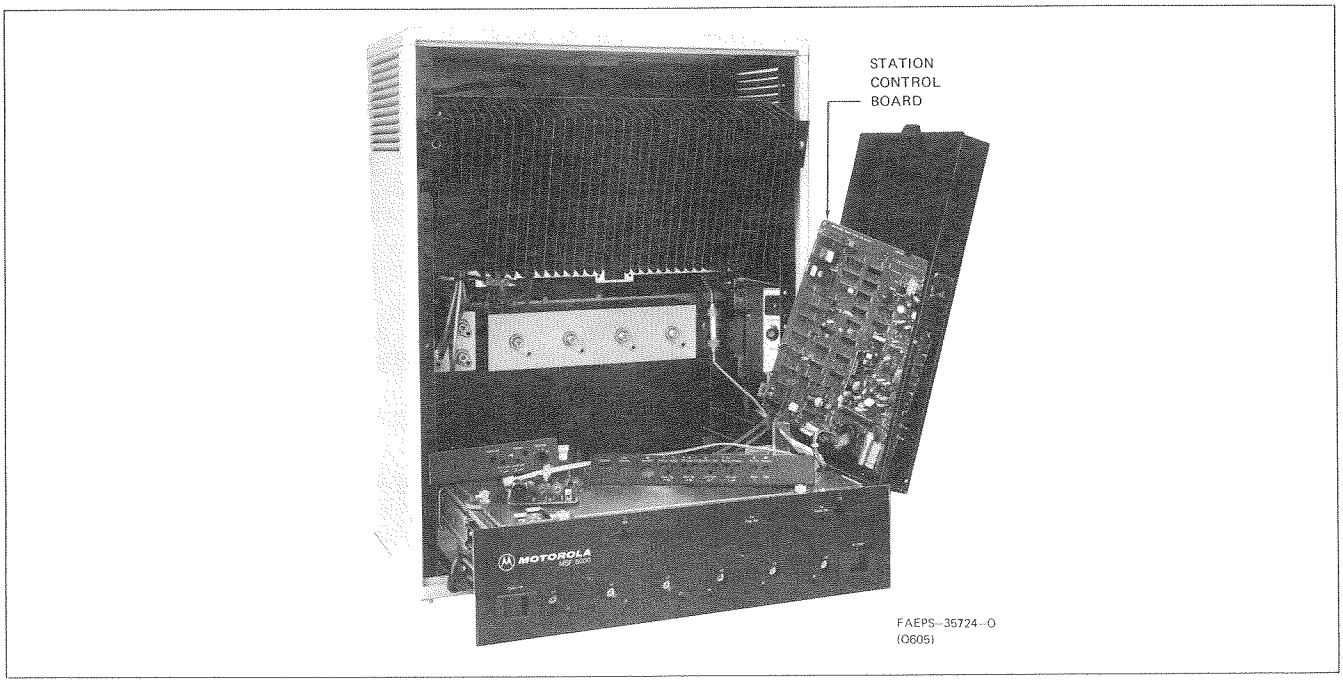
The TLN2423A Station Control Module directly controls most major functional blocks of the station. The module consists of the following items:

- TFN6045A PL Filter Hybrid
- TRN4372A Analog-to-Digital Hybrid
- TRN5195A PL/DPL Station Control Board
- TRN5196A PL/DPL Station Program EPROM

The station control board (see overall block diagram at end of this section) can be functionally divided into four sections:

- DC-DC Converter section.
- Processor section.
- Receiver Audio, PL/DPL, and Squelch section.
- Audio Routing/Control section.

The dc-dc converter section essentially functions alone. That is, it is the source of the regulated +5 V used within the station plus the bias voltages required by the audio/squelch circuits. Other than these voltages, its only functional operation is to provide the power-up RESET signal, which is used to initialize the entire station during initial turn-on, or during a reset turn-on after loss of any of the three station operating voltages (+5 V, +9.6 V, or A+). The receiver audio, PL/DPL, and squelch section together with the audio/routing control section process all audio and provide all squelching used within the station. The processor section controls operation of the complete station, properly sequencing operations in a timely manner so that both transmission and reception is performed with the specified parameters. As shown in Figure 1, the station control board is located within (fastened to the underside of) the Control Tray which is mounted above the RF Tray.



Figuere 1. Location of TRN5195A Station Control Board

1.1 DC-DC CONVERTER SECTION

The dc-dc converter section (see block diagram at the end of this section) of the station control board provides the bias voltages for the various audio and squelch circuits on the station control module, and produces the filtered and regulated +5 V used within the station. The dc-dc converter also provides routing, fusing, and some filtering for the A+ from the power supply, internally routing A+ to the processor section and the audio and squelch control sections and externally routing A+ to the remote control board and expansion connector. The dc-dc converter additionally contains a power-up RESET circuit that provides a system initialization reset signal to the station.

1.2 PROCESSOR SECTION

The processor section (see block diagram at the end of this section) of the station control board controls all major radio functions of a station on a per-channel basis, including transmit and receive frequencies and switching, PL/DPL encode and decode, time-out timers, dropout and push-to-talk delays, automatic station identification (auto ID), alarm monitoring and generating, and squelch gating/repeater key-up conditions. The heart of the control function is a Motorola MC6803 Microprocessor Unit (MPU) that uses a preprogrammed erasable, programmable read-only memory (EPROM) and a personality code plug, both of which combine to provide the exact operating program and parameters for a particular station. Proper sequencing of the various controlling operations from the MPU is supervised by the watchdog timer circuitry, which resets the MPU if its timing should falter (either too early or too late). The various latches and buffers within the processor section route status and control signals to the MPU, and command and control signals to the other portions of the station, or to external optional equipment.

1.3 RECEIVER AUDIO, PL/DPL, AND SQUELCH SECTION

The Receiver Audio, *Private-Line/Digital Private-Line* (PL/DPL), and Squelch section (see block diagram at the end of this section) of the station control board processes the detected raw receiver audio from the i-f amplifier section of the uniboard. The processing includes separation and detection of received PL-DPL data, filtering and de-emphasis of receiver audio, and detection of both repeater (if used) and receiver 1 squelch. When used, the remote squelch control option is also located in this section. The PL-DPL portion of this section is also capable of accepting commands from the processor section to produce PL or DPL encoding tones (or codes) for encryption of the selected *Private-Line* tone (or code) during transmission.

1.4 AUDIO ROUTING/CONTROL SECTION

The audio routing/control section (see block diagram at the end of this section) of the station control board provides routing for all audio within a station. This includes pre-emphasis and deviation control limitation for transmitter modulation audio, summing and amplification for local speaker audio (including a 1/2 watt audio driver), and summing and amplification for line audio. Summation of audio inputs for the three audio outputs is controlled via analog gate switches, except for the second receiver audio (if used) from the expansion connector.

2. DC-DC CONVERTER SECTION THEORY OF OPERATION

2.1 GENERAL

The dc-dc converter section (see schematic at the end of this section) converts the auxiliary 13.8 V input into the filtered and regulated +5 V required by the station by using a controlled pulse-width modulator (PWM). The bias voltages used by the audio/squelch circuits and by the dc-dc converter are produced through a resistive divider network and through an operational amplifier used as a voltage follower. The circuits of the dc-dc converter section are generally grouped into one area of the station control module and may be located by referring to the circuit board detail at the end of this section.

2.2 BIAS VOLTAGE GENERATION DESCRIPTION

The five bias voltages (V_A through V_E) are produced by three circuits shown on the left side of the schematic at the end of this section. The 5.1-volt V_E is derived from Zener VR701 and resistor R739 connected to the +9.6 V input regulator. The 4.8-volt V_B is developed from the +9.6 V input to divider network R838-R839 used as the (+) input to operational amplifier U835B, which is configured as a voltage follower circuit. A divider network, comprised of R1538-R1539 and R1541-R1542, is used to produce the 5.1-volt V_A, 4.8-volt V_C, and 4.1-volt V_D. Bias voltage V_E is used in the dc-dc converter circuits while V_A through V_D are used in the audio and squelch circuits.

2.3 +5 V POWER SUPPLY CIRCUIT

2.3.1 The majority of the dc-dc converter section comprises the +5 V power supply, as shown on the schematic diagram at the end of this section. Further details of operation are also included on the schematic diagram.

2.3.2 When the auxiliary 13.8 V supply comes up, the +9.6 V regulator also begins operation. Bias voltage V_E provides a reference voltage to shutdown comparator U701A. Thus, when A+ rises above 12 V, U701A output goes high and turns on oscillator U701C, allowing the station to begin operation after the +5 V supply stablizes. The station is kept in a reset condition, for at least 100 milliseconds after the +5 V output

comes on, by the $\overline{\text{RESET}}$ signal generated from U701B and Q705. This provides sufficient time for all transients to settle out before the MPU in the processor section begins its initialization/turn-on routine. The +5 V supply includes a current limiting circuit, consisting of Q704 and R731-R734, which reduces the +5 V supply output voltage if the output current exceeds approximately 2 amperes. The +5 V supply also includes an over-voltage protection circuit to prevent damage to the digital integrated circuits. If the +5 V supply output exceeds approximately 6 V, Q706 turns on causing the A+ fuse, F701, to blow.

3. PROCESSOR SECTION THEORY OF OPERATION

3.1 MC6803 MPU DESCRIPTION

3.1.1 The control center for the processor section is a Motorola MC6803 MPU, programmed to operate in Mode 2, which has multiplexed data/addresses (lower order), external interrupt vectors, internal random-access memory (RAM), and a 4.9068 MHz crystal-controlled clock source, but no internal read-only memory (ROM). The MPU operating mode is determined by the inputs at ports P20 through P22 (pins 8 through 10 of U801). With a diode in the circuit for a particular port, its input bit is configured as a logic 0 on the trailing edge of the RESET pulse at U801-6. Without a diode and by using a pull-up resistor to +5 V, a mode input bit is figured as a logic 1 by the $\overline{\text{RESET}}$ pulse trailing edge. Therefore, with diodes in for P22 and P20, but out for P21, the MPU is configured for mode 2 operation. Refer to MC6801 8-Bit Single-Chip Microcomputer Reference Manual MC6801RM(AD) for more detailed information.

3.1.2 Ports 1 and 2 of the MPU are used for various input and output (I/O) signals. Port 3 is dedicated to multiplexed data and low-order address bits. Port 4 is dedicated to the high-order address bits. All I/O, control signals, and power/ground input pins are shown in Figure 2. Key control signals are described in the following paragraphs. The particular applications of the MPU's I/O lines are shown on the schematic diagrams at the end of this section. More detailed electrical specifications for these lines are available in the MC6801 Microcomputer Reference Manual MC6801RM(AD).

3.1.2.1 Control Input/Output Pins

3.1.2.1.1 READ/$\overline{\text{WRITE}}$ (R/$\overline{\text{W}}$), pin 38

The R/$\overline{\text{W}}$ output strobe is an active low pulse that is generated for an MPU read or write to the

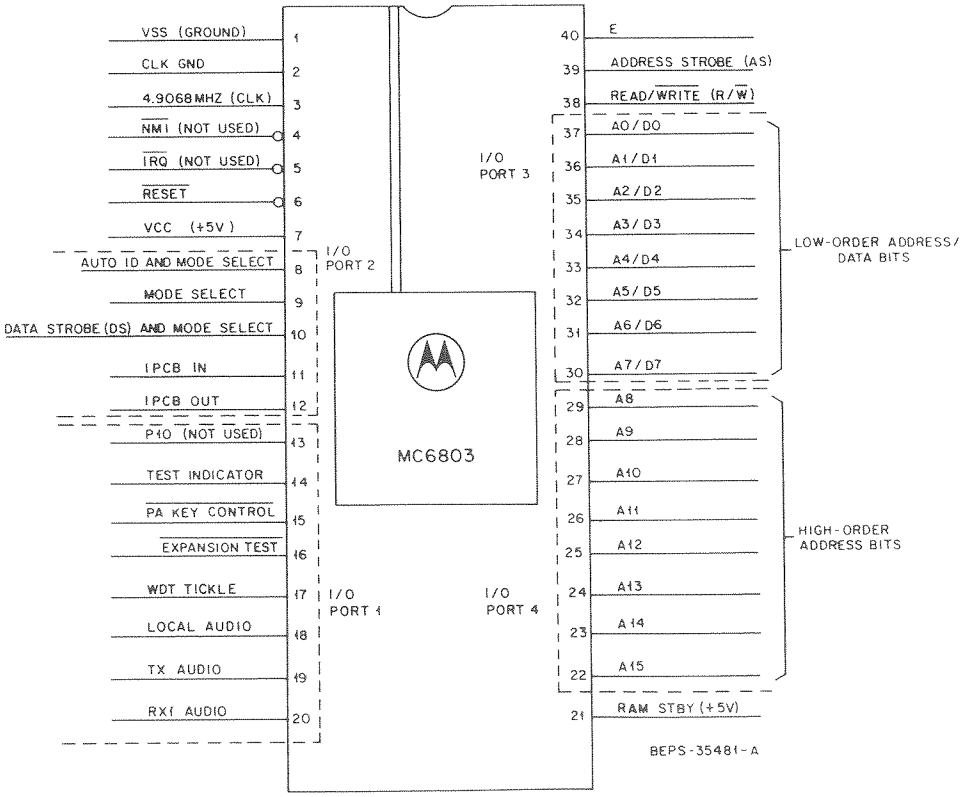


Figure 2.
Motorola MC6803 MPU Pin Configuration

Port 3 data register in the MPU, depending upon the MPU's control configuration. The R/$\overline{W}$ pulse, approximately one E-cycle wide (that cannot be varied), is used for memory map decoding and as a strobe input to the code plug.

3.1.2.1.2 ADDRESS STROBE (AS), pin 39

The AS output strobe is used as a Latch Enable (LE) input for Address Latch (Low-Order) U802. It latches the addresses on its falling edge.

3.1.2.1.3 ENABLE (E), pin 40

The E signal is the primary MPU system timing signal and synchronizes all DATA bus transfers. An MPU E-cycle (or bus cycle) consists of a negative half-cycle of E followed by a positive half-cycle. The data bus is active only while E is high or, equivalently, "during E".

3.1.2.1.4 $\overline{\text{PA Key}}$, pin 15

Port 12 (pin 15) outputs $\overline{\text{PA Key}}$, a control signal that is gated to the station transmitter power control circuit.

3.1.2.1.5 DATA STROBE (DS), pin 10

The DS signal is used to strobe multiplexed address and data (MUXBUS signals) to EXPANSION connector J800 for intermodule operations. The signal is buffered and inverted by U822B and U827B before it is applied to the EXPANSION connector as $\overline{\text{DS}}$. The signal edges indicate the status of the address and data on the MUXBUS lines. The falling edge of $\overline{\text{DS}}$indicates that the station control MPU has written a new address to the MUXBUS. The rising edge of $\overline{\text{DS}}$ indicates that all modules have written the appropriate data to the MUXBUS.

3.1.2.1.6 IPCB Out, pin 12, IPCB In, Pin 11

These pins provide the serial communication transmit and receive lines of the MPU. They are connected to the bidirectional Interprocessor Communications Bus (IPCB), on EXPANSION connector J800, via buffer/invertes U826F, U827A, U826E, and U822F.

3.1.2.2 Microprocessor Control Bus Signals

Port 3 consists of P30 through P37 (pins 37 to 30 of U801) and is used for the multiplexed low-order address bits/data. Thus, depending upon the internal MPU programming control, port 3 will output the eight low-order address bits or port 3 will provide or accept eight bits of data via the DATA bus. Port 4 consists of P40 through P47 (pins 29 to 22 of U801) and is dedicated to the high-order address bits. That is, port 4 will not accept inputs, being used only to output the eight higher order bits of any particular address.

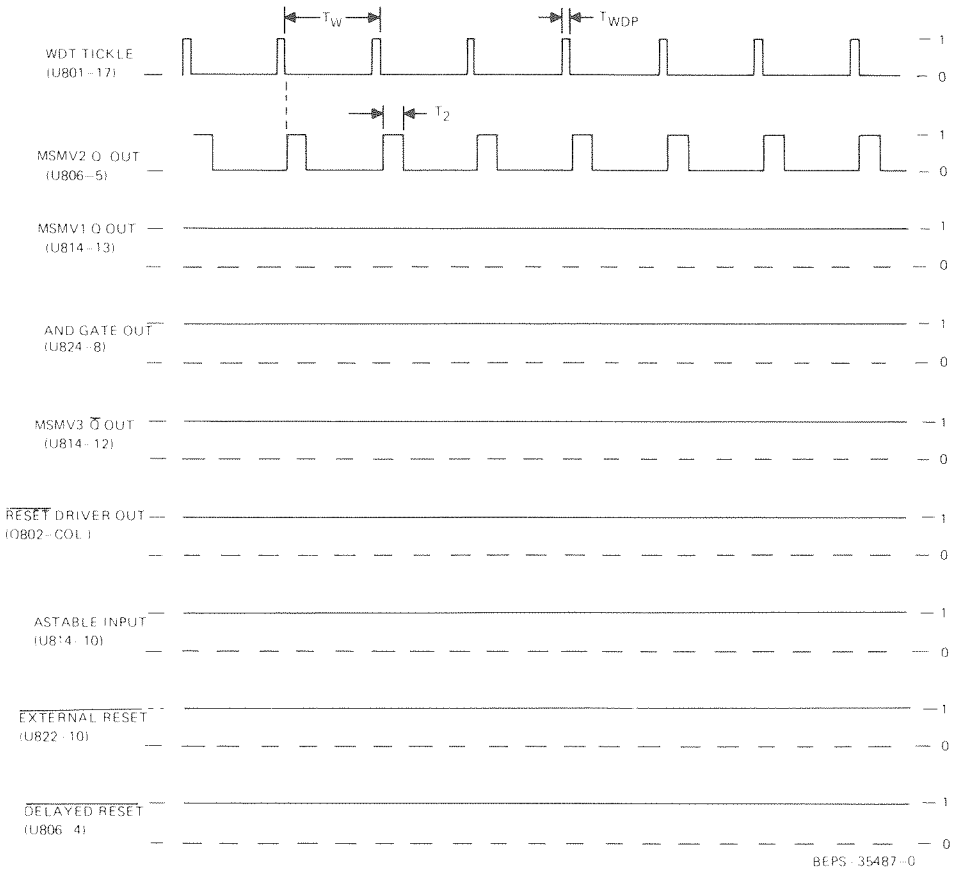
3.1.3 Watchdog Timer Description

3.1.3.1 When the MPU is operating properly, it outputs the WDT TICKLE pulses (on U801-17) that are characterized by a given periodicity, as shown on the timing diagram for normal operation in Figure 3 and listed in Table 1. The watchdog timer circuit monitors this period and, if the pulses are not within a predetermined range (i.e., timing "window"), the watchdog timer circuit resets the MPU. At the same time, it prevents other circuits from experiencing any ill effects of a MPU control section malfunction by holding them reset until the MPU is again operating properly.

3.1.3.2 Monostable multivibrators (MSMV) U814A and U806B are used to set the tickle-pulse period range by forming a window in which the pulse must occur. In normal operation, U814A is kept retriggered by the negative-going edge of the MPU tickle pulse (Figure 3). The U814A time constant determines the maximum allowable tickle period. If tickle pulses occur too far apart, U814A times out, and generates a reset pulse through U814B and Q802. The U806B time constant determines the minimum allowable tickle period. If tickle pulses occur too close together, the normal output from U806B allows the "too-early" tickle pulse through NAND gate U823D to clear MSMV U814A, which again causes a reset pulse to be generated by U814B and Q802.

Table 1. Timing Parameter Chart

Parameter	Description	Timing Range	Average	Units
t_W	Watchdog Timer Tickle Period	35-71	53	ms
t_{WDP}	Watchdog Timer Tickle Pulse Width	40-300	170	uS
t1	MSMV U814A Time Constant	89-214	151	ms
t2	MSMV U806B Time Constant	9-21	15	ms
t_{WND}	Window Width (t1-t2)	68-205	136	ms
t3	MSMV U814B Time Constant	2.5-4.5	3.5	ms
t4	MSMV U806A Time Constant	490-1389	935	ms
t5	Astable Time Constant (C807, R823)	14-230	122	ms

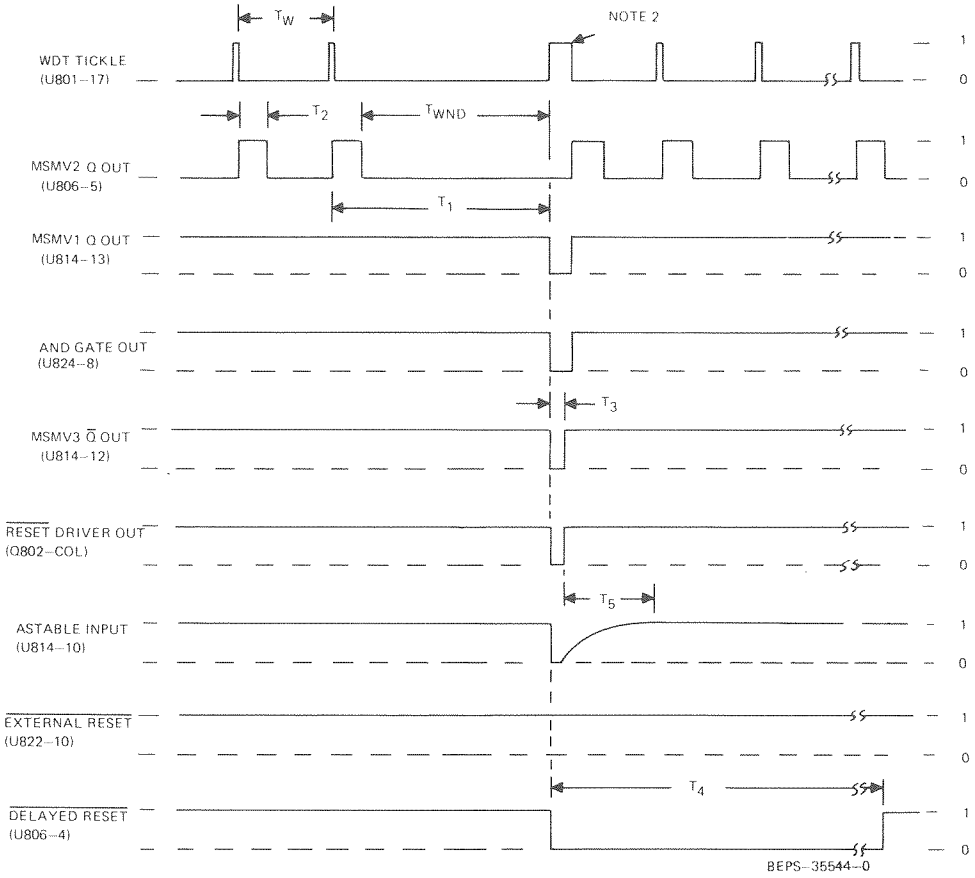


1. All timing is approximate, due to component variation.

Figure 3.
Normal Operation Timing Diagram

3.1.3.3 The MPU reset occurs in the following manner. Retriggerable MSMV U814B generates a reset pulse whose duration is determined by its time constant (established by C805 and R820). This occurs when the $\overline{A}$ input at pin U814-9 goes active (low) as a result of improper tickling (see timing diagrams for abnormal operations as shown in Figures 4 and 5). As part of the reset procedure, the B input (pin 10) of U814B goes inactive (low) through the action of Q803 being turned on by the Q output from U814B. With the B input of U814 inactive, the MPU has time to go through its startup routines and begin outputting tickle pulses; the first tickle pulse should occur about six milliseconds after the trailing edge of the $\overline{RESET}$ pulse (see Figure 4 and 5). However, if no tickle pulse occurs, the $\overline{A}$ input remains active and another $\overline{RESET}$ pulse is generated when the charging circuit C807-R823 reaches the MSMV triggering level at the B input of U814B. This astable operation will continuously attempt to reset the MPU as long as improper tickling occurs, as shown in Figure 7 for a MPU malfunction. When the MPU properly outputs a tickle pulse after being reset, the $\overline{A}$ input for U814B goes inactive (high) and prevents any additional $\overline{RESET}$ pulses from occuring due to the astable operation of U814B.

3.1.3.4 An external reset function for the Watchdog timer circuit is incorporated in the following manner. As long as the $\overline{EXPANSION\ RESET}$ signal is held active (low), U814B will astable as described previously. Furthermore, the MPU will be held in reset by the action of NAND gate U823C (see timing diagram for an external reset, as shown in Figure 6). In this case, the astable operation is not needed to reset the MPU, but instead is used to retrigger Delayed Reset MSMV U806A. The $\overline{EXPANSION\ RESET}$ signal is also used to clear MSMV U806B, so that when the WDT tickle signal is pulled high as a result of a reset, another reset does not occur due to a low output from U823D.



NOTES:

1. All timing is approximate, due to component variation.
2. The Watchdog Timer (WDT) tickle signal is pulled low approximately 6 ms after the $\overline{\text{RESET}}$ signal to the processor goes inactive (high).

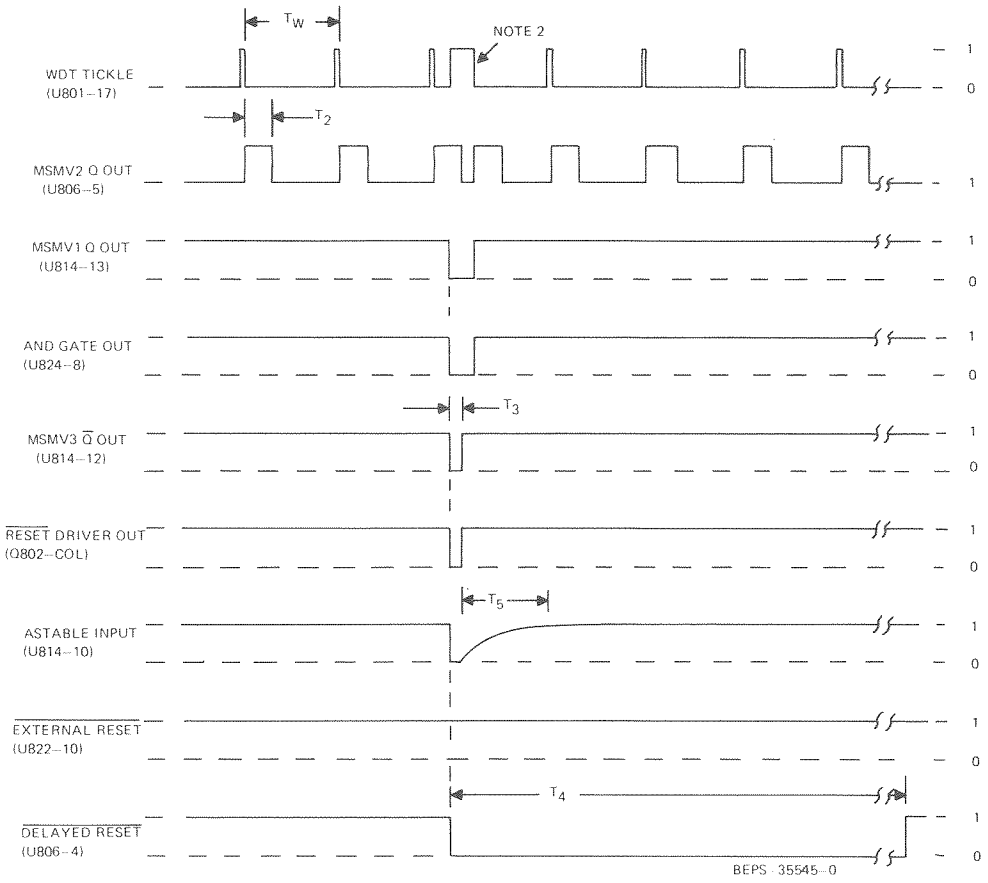
Figure 4.
Abnormal Operation Timing Diagram
(Tickle Pulse Late or Missing)

3.1.3.5 The $\overline{\text{DELAYED RESET}}$ output from U806A is used to hold other circuits of the processor section (e.g., $\overline{\text{PA Key}}$, $\overline{\text{DS}}$, $\overline{\text{IOR}}$, and $\overline{\text{IOW}}$) inactive until the MPU properly tickles the WDT circuit and astable operation has ceased. The time constant for U806A is such that the $\overline{\text{DELAYED RESET}}$ signal is active long enough to guarantee that two proper tickle pulses will occur after the final reset to the MPU (a single tickle pulse could be the result of a MPU malfunction). During an external reset, the astable operation of U814B keeps U806A retriggered so that it cannot time out early (as shown in Figure 6).

3.1.4 Test/Reset Arbiter Description

The Test/Reset Arbiter circuit performs two functions. First, the MPU can generate an $\overline{\text{EXPANSION TEST}}$ signal without resetting itself. When the $\overline{\text{EXPANSION TEST}}$ signal at U801-16 switches low, the low is applied directly to U823B-4 before a high signal propagates to U823B-5 via U822C, U826B, and U822D. Therefore, U823B-6 remains high and no $\overline{\text{EXPANSION RESET}}$ signal occurs. When the $\overline{\text{EXPANSION TEST}}$ signal switches high, U823B-6 switches momentarily low until a low signal propagates to U823B-5. This low signal is short enough, however, that capacitor C879 cannot charge up to a logic high level and therefore, no $\overline{\text{EXPANSION RESET}}$ signal occurs. Second, when a reset command, generated externally to the station control board, is received, the Test/Reset Arbiter circuit produces an MPU reset. This is accomplished since the inactive state of the $\overline{\text{EXPANSION TEST}}$ signal allows the $\overline{\text{EXPANSION RESET}}$ signal through NAND gate U823B to become the $\overline{\text{EXTERNAL RESET}}$ signal. The $\overline{\text{EXTERNAL RESET}}$ generates a MPU reset as described previously, and can occur due to:

- $\overline{\text{RESET}}$ from the expansion bus connector
- $\overline{\text{RESET}}$ from the DC-DC converter section
- $\overline{\text{RESET}}$ from the remote control connector



NOTES:

1. All timing is approximate, due to component variation.
2. The Watchdog Timer (WDT) tickle signal is pulled low approximately 6 ms after the $\overline{\text{RESET}}$ signal to the processor goes inactive (high).

Figure 5.
Abnormal Operation Timing Diagram
(Tickle Pulse Early)

NOTE

Switch S801, when put to the TEST position, can also generate an external reset via the DC-DC Converter section.

3.1.5 Memory Devices Description

3.1.5.1 The main executable code for the processor section is stored in station program EPROM U804, (an 8k × 8 EPROM). U804 contains the operating program for the station. It, interacts with the personality data stored in code plug U803, and the changing parameters of the station itself, to control station operation. The station program EPROM shipped in any station contains unique information which makes it compatible with that station hardware and code plug. Extreme care must be exercised when exchanging station program EPROM's between stations, or when replacing damaged parts. If a malfunction should be localized to U804, the device must be exchanged for an operational device with the same Motorola part number.

3.1.5.2 The other memory device for the processor section is code plug U803, which stores the station configuration ("personality") data. It is a 4k × 8 EPROM device. Table 2 gives the memory locations of these devices and provides a memory map of all other station control functions. Table 3 gives proper jumper usage for the various operational characteristics.

Table 2. MSF 5000 Station Control Memory Map

Name	Type	Software Address Used	Comments
Internal Registers	R/W	$0000-$001F	—
External Memory	—	$0020-$007F	Unused — See Code Plug
Internal RAM	R/W	$0080-$00FF	—
External Memory	—	$0100-$1FFF	Unused — See Code Plug
Code Plug	R	$2000-$2FFF	Hardware Allows Use of $0000-$3FFF
I/O Devices*	R/W	Defined as Follows	Hardware Allows Use of $4000-$7FFF
Bus Read Data Buffer	R	$59FF	$\overline{A13} \bullet \overline{IOR}$ (Note 2)
MUX bus Latch	W	$69FF	$\overline{A12} \bullet \overline{IOW}$ (Note 3)
Synthesizer Latch	W	$71FF	$\overline{A11} \bullet \overline{IOW}$
TX Synth Strobe	W	$7DFF	$A10 \bullet \overline{IOW}$
RX Synth Strobe	W	$7BFF	$A9 \bullet \overline{IOW}$
PL/DPL DAC Latch	W	$78FF	$\overline{A8} \bullet \overline{IOW}$
TX/RX Status Buffer	R	$797F	$\overline{A7} \bullet \overline{IOR}$
Options Latch	W	$79BF	$\overline{A6} \bullet \overline{IOW}$
Options Buffer	R	$79DF	$\overline{A5} \bullet \overline{IOR}$
Command/Service Buffer	R	$79EF	$\overline{A4} \bullet \overline{IOR}$ (Note 2)
System ROM	R	$C000-$DFFF	Hardware Allows Use of $8000-$FFFF
Internal ROM Space	—	$F800-$FFEF	Unused
External Vectors	R	$FFF0-$FFFF	$DFF0-$DFFF Used to Read Software $FFFF-$FFFF
*Undefined I/O Devices	R/W	$79F0-$79FF	Address, as shown will not select a device

NOTES:
1. The symbol "$" preceding any alphanumeric character(s) means that the character(s) are HEX coded.
2. $\overline{IOR} = E \bullet R / \overline{W}$ (DEL RS) (A14 • $\overline{A15}$), where DEL RS = Delayed Reset, and is High.
3. $\overline{IOW} = E \bullet R/W$ (DEL RS) (A14 • $\overline{A15}$).

Table 3. Diode and Jumper Usage

Ref. Design	Normally	Description
CR801	IN	Out for MPU operation mode where program code (PC) Ø = 1
CR802	OUT	In for MPU operation mode where program code (PC) 1 = Ø
CR803	IN	Out for MPU operation mode where program code (PC) 2 = 1
JU1	OUT	In to disable software power control and enable PA fail alarm
JU2	OUT	In for 8k × 8 EPROM
JU3	IN	Out for 8k × 8 EPROM
JU4	OUT	In for 2k × 8 RAM
JU5	IN	Out for 2k × 8 EPROM; out for 2k × 8 RAM
JU6	OUT	In for 2k × 8 EPROM
JU9	IN	Out for 2k × 8 RAM
JU10	OUT	In for 2k × 8 RAM
JU11	IN	Out for 2-RCVR station

3.1.6 Address Latch Description

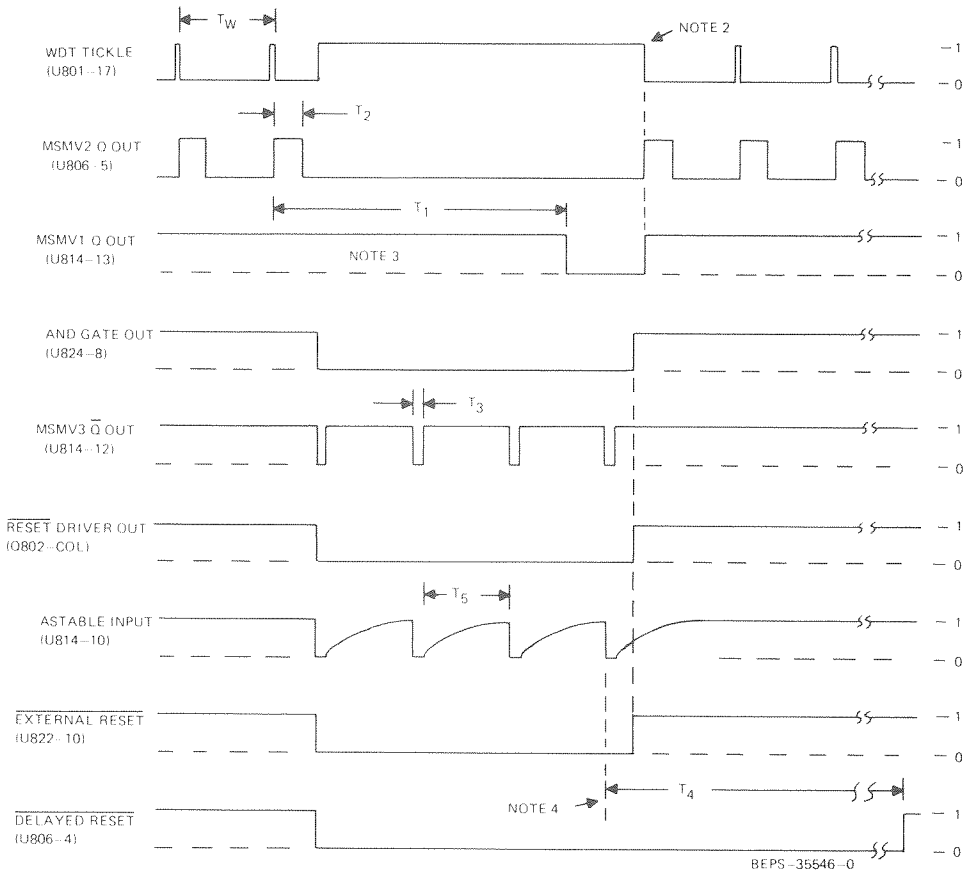
The address latch (U802) is used to hold the low-order address bits from the multiplexed address/data lines output at port 3 of the MPU. Latch U802 is transparent (i.e., passes a signal as if it were not there) while the Latch Enable (LE) input is high. The LE signal is the ADDRESS STROBE (AS) signal from the MPU, and when the AS signal goes low (inactive), the address bits are latched into U802. The address lines of U802 are output to the ADDRESS/CONTROL bus, forming part of the total address used to control the various parts of the processor section.

3.1.7 Memory Map Decoder Description

The Input/Output Read (IOR) and input/output write ($\overline{IOW}$) are two control signals that are generated by the memory map decoder circuits to allow selection of I/O devices in the processor section. The $\overline{IOR}$ signal provides an enable for the group of I/O devices that the processor reads (i.e., obtains data from), while the $\overline{IOW}$ signal provides an enable for the group of I/O devices to which the processor writes (i.e., passes data to). For both groups, the control signal provides only one enable to the device. The second enable signal needed is an address line. Both types of enable or gating signals are carried on the CONTROL SIGNALS TRUNK (see schematic at the end of this section) to each device controlled by the processor section for input and output functions. The control signals and addresses used for I/O device selection are listed in the station control board memory map chart of Table 2.

3.1.8 Synthesizer Latch Description

The data that the processor writes to the synthesizer latch (U805) are used to program the transmit and receive frequencies for the station. This information is configured as four data bits and three address bits for use by the synthesizers (one output is not used).



NOTES:

1. All timing is approximate, due to component variations.
2. The Watchdog Timer (WDT) tickle pulse is pulled low approximately 6 ms after the $\overline{\text{RESET}}$ signal to the processor goes inactive (high).
3. The MSMV1 Q Output will not change state (High to Low) if the $\overline{\text{EXTERNAL RESET}}$ signal is held active (low) for less than the remaining T_1 time.
4. Since MSMV4 (U806A) is kept retriggered, the $\overline{\text{DELAYED RESET}}$ time T_4 begins with the falling edge of the last output from U814B-12.

Figure 6.
Timing Diagram Showing Effects of External Reset Signal

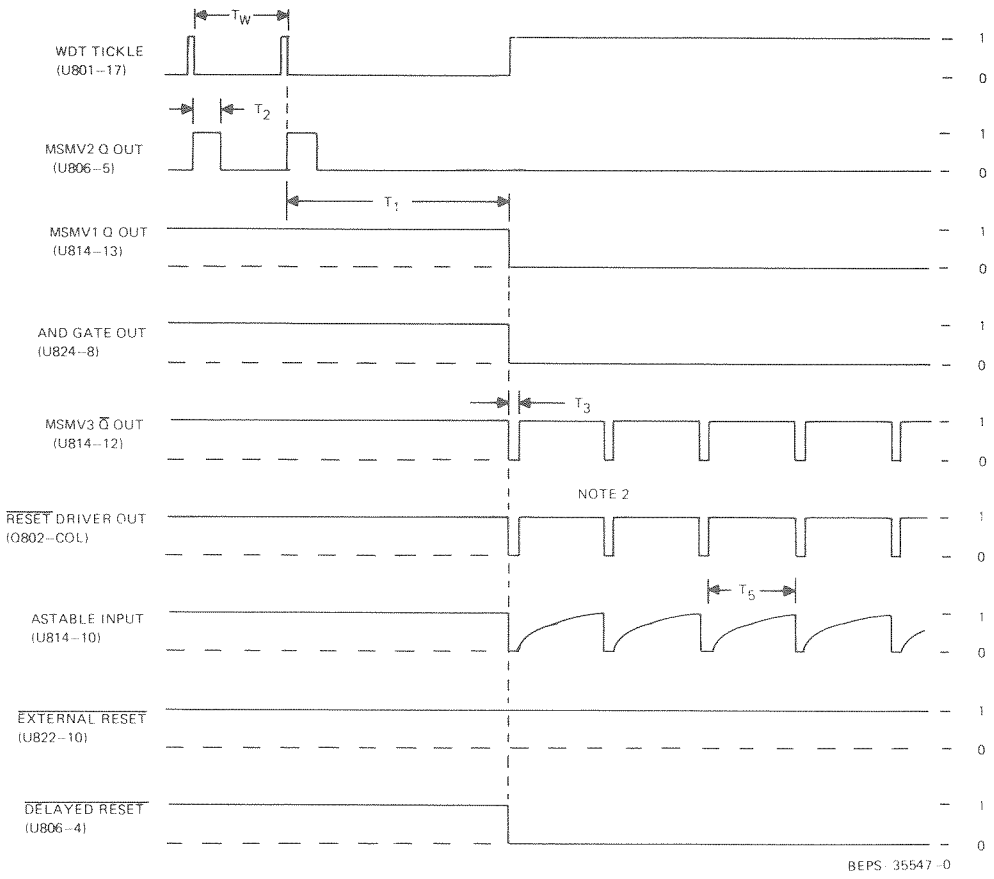
In order to program the synthesizers, seven sets of data are written to the latch for each synthesizer. This information is then strobed to the appropriate transmit or receive synthesizer circuits by means of the logic gates generating the transmit strobe (TX STROBE) and receive strobe (RX STROBE) signals.

3.1.9 PL/DPL DAC Latch Description

The *Private-Line/Digital Private-Line* (PL/DPL) digital-to-analog converter (DAC) latch (U808) supplies the five bits necessary to encode PL or DPL control information. The outputs from U808 are routed to the DAC circuit in the audio section where they are used to generate the proper code for the transmit audio signal. The DPL rotate bit, another output of the latch, is routed to the options buffer and used to signal the processor to rotate the DPL encode word by one bit. This rotation occurs every 7440 microseconds in order to supply a new encode bit to the DAC circuit. The remaining two latch outputs are unused.

3.1.10 Options Latch Description

The MPU writes eight different control signals to the options latch (U807). The PL/DPL bit controls the configuration of the decode filters used to decode either PL or DPL in the receive audio signal. The deviation control bit allows reduction in the deviation of the transmit modulated audio signal. The PA power adjust signal is gated to the power control section and controls reduction in the PA power. The antenna switch output of latch U807 is gated to the interconnect board and controls switching of the antenna switch. The alarm audio control and repeater audio control bits control



NOTES:

1. All timing is approximate, due to component variation.
2. The astable operation of MSMV3 (U814B) generates pulses in an attempt to reset the processor.

Figure 7.
Timing Diagram Showing Effects of MPU Malfunction

gating in the audio circuits area. The alarm audio control allows the auto ID signal (and alarm tones) to be mixed onto the line audio signal. The repeater audio control bit controls mixing of the RX1 Audio signal with the TX Audio signal. The squelch level bit is used for remote control of receiver 1 squelch level, and the adapt bit allows the squelch circuit to clear its detect indication quickly for use with channel scan operation.

3.1.11 TX/RX Status Buffer Description

Two inputs to buffer U809 are controlled by the power control circuit and are used as status signals. These signals, PA On and PA Full Power indicate whether the PA is on and whether it is operating under full power. Partial power (or power cutback) capabilities may be used with options (such as battery backup) and for minimizing damage in case of a PA or related failure. The following four signals are inputs to the buffer from the transmitter and receiver circuits. The Tx Lock and Rx Lock signals specify whether the transmitter and receiver are locked on a frequency while Tx Loop and Rx Loop are synchronizing signals used to indicate when the processor can output new transmitter and receiver frequency data to the synthesizers. The loop signals are ignored during normal station operation but are available for synchronous synthesizer loading for special products such as channel scan stations that require fast synthesizer locking. The remaining two signals, RX1 Unsquelch and Repeater Unsquelch, indicate when the receiver 1 audio (RX Audio) is at a quieting level sufficient to activate the receiver 1 and repeater squelch circuits.

3.1.12 Options Buffer Description

All eight inputs of buffer U810 are used for distinct functions. The PL/DPL Decode Data signal is the low-pass filtered and limited PL or DPL data to be decoded by the processor. The DPL Rotate bit signals the processor to rotate the DPL code. The Battery Revert and Overvoltage Alarm signals are inputs to the processor from the dc-dc converter circuits. These two

signals originate from the battery charger board of the power supply. The Battery Revert signal indicates that the station is operating under battery power. The Overvoltage Alarm bit signals that a charging circuit malfunction has occurred (such that the batteries are being overcharged). This results in the charging circuit being disabled and in the station operating on batteries (servicing is required to resume non-battery operation). The DC/TRC signal specifies which module type (tone or dc control) is in the remote control slot. The Intercom bit is activated by a dc remote or a tone remote control front panel switch and is used when servicing the station. This bit, along with a MIC PTT, results in gating the local or service audio signal outbound on the wireline and prevents the PA from keying. If the Intercom bit is active without a MIC PTT signal, the TX audio signal is gated to the local speaker. In both cases, the receiver audio is allowed to mix with the given signal. Note that these intercom functions are disabled if a RPTR PTT or a LINE PTT occurs. Channel Activity is a signal from the receiver 1 squelch circuit similar to RX1 Unsquelch and is to be used for special applications such as channel scan operation, resulting in a faster unsquelch. The Service input indicates that the service jumper is in place, causing software power control to be inhibited and a PA FAIL alarm to be activated.

3.1.13 Command Service Buffer Description

Four inputs to buffer U813 are configured as a 4-bit word from the remote control connector. When a tone remote control board is used, this word consists of the current status of the channel select switch on the tone remote control board. When the dc remote control board is used, without the access disable switch activated, the word consists of the dc current information. When the dc remote control board is used, with the access disable switch activated, the word consists of the status of the channel select switch on the front panel of dc remote control. The MIC PTT input indicates that a Push-To-Talk (local) was generated by means of the CONTROL connector J812. The three remaining buffer connections are used to read three switch inputs, Access Disable, Transmit, and PL Disable. The Access Disable position of S801 (ACC DIS) inhibits several functions: auto ID, alarm tones, time-out timer, repeater PTT from the receiver, and some wireline commands including line PTT. The Transmit position of S802 (XMIT) results in a PA key without audio or the encoding of PL or DPL. This position of S802 also acts to strip PL or DPL from any signal currently being transmitted (i.e., carrier squelch operation). The PL Disable position of S802 (PL DIS) is used to locally monitor all receiver activity, regardless of the PL or DPL code. This position of S802 allows the opening of the receiver audio gate with only receiver activity (i.e., carrier squelch operation).

3.1.14 MUX Bus Write Latch Description

This latch (U811) holds information that will be written to the EXPANSION connector (J800) by the processor section. Four bits (BA0 through BA3) are configured as the address and the four remaining bits (WD0 through WD3) are routed through open-collector inverter buffers as the multiplexed "write-data" corresponding to that address.

3.1.15 MUX Bus Read Data Buffer Description

Four inputs to buffer U812 are unused while the remaining four are used to read the multiplexed "bus-data" bits (BD0 through BD3) that are present at the EXPANSION connector. The data at J800 is inverted from that written to expansion bus latch U811.

3.1.16 Synthesizer Failsafe Circuit Description

If the transmit synthesizer is not locked onto the selected frequency, the synthesizer failsafe circuit prevents or aborts power amplifier (PA) keying. Flip-flop U818A is a D-type whose output (pin 5) is a logic high while the TRANSMIT SYNTHESIZER LOCK signal is inactive (high). After the transmit synthesizer locks onto its selected frequency, the TX LOCK signal is active (low), is inverted by U822A, and enables flip-flop U818A to output a low signal. This occurs when the MPU outputs a PA key control signal and DELAYED RESET is inactive. The low Q-output from U818A is inverted by U826D to turn on transistor Q804, whose output is the PA KEY signal to the radio interface J801.

3.1.17 Front Panel Indicators Description

3.1.17.1 The light-emitting diodes (LED's), used as indicators on the front panel of the station control board, are color-coded according to their function. The red LED's indicate a failure or servicing status.

IMPORTANT

Stations should not normally be returned to operation after service while any red LED is on.

3.1.17.2 The green LED's indicate active operation of the named signal. The yellow LED's indicate a request for action or a warning status. The functions of these front panel indicators are fully described in the Operation section of this manual.

4. RECEIVER AUDIO, PL/DPL, AND SQUELCH SECTION THEORY OF OPERATION

4.1 GENERAL

The receiver audio, PL/DPL, and squelch section of the station control board (see schematic diagram)

provides the primary processing for the receiver audio and squelch portions of the station. Raw receiver audio is split into two paths, one is used for squelch control and the other is used for audio processing. Audio from the Quad Audio Buffer (U835A) is routed through a PL/DPL low-pass filter (U833B, C, and D) to the PL/DPL Digital-to-Analog Converter (DAC) hybrid (HY802) for decoding of PL and DPL data. Quad audio is also routed to EXPANSION connector J800-39.

4.2 RECEIVER AUDIO CIRCUITS DESCRIPTION

Receiver audio to be routed to the local speaker and wireline, or routed to the transmitter, is processed by this section of the station control board. Raw receiver audio is buffered by U835A, whose output (Quad audio) is supplied to PL/DPL high pass filter hybrid HY803 and through jumper JU7 to the PL/DPL decode low pass filter. Filter HY803 removes the coded squelch tones from the received audio and passes the filtered receiver audio to the RX LEV control R841, a front panel accessible potentiometer, which adjusts the internal system-level setting for audio (available at TP1, at U834B-7). The system level adjusted audio is de-emphasized by amplifier stage U833A, whose output is then routed to the RX1 audio gate (U823A) in the audio routing/control section of the station control board. RX1 audio is also routed to EXPANSION connector J800-38.

NOTE

A plated through pad on the printed circuit board has been provided at HY803-15 for applications that require receiver audio with PL/DPL codes removed, but not de-emphasized.

4.3 PL/DPL CIRCUITS DESCRIPTION

4.3.1 Receiver quad audio from U835A is routed to a 5-pole, low-pass filter consisting of amplifiers U833B and U833C. The filter separates the PL and DPL tones from voice audio and higher frequency noise signals that may be present in the received audio. When DPL tones are being decoded, FET switch Q807 is turned on, changing the filter to optimize DPL decoding. A low signal on the PL/$\overline{\text{DPL}}$ control line from the processor section turns FET Q807 on.

4.3.2 The filtered PL/DPL audio is applied to limiter stage U833D, which produces the zero-crossing data used for decoding purposes. The limiter is also optimized for DPL decoding by FET switch Q808 that is turned on by the same PL/$\overline{\text{DPL}}$ control line from the processor section that controls Q807. The zero-crossing data is buffered to TTL-voltage levels (i.e., HI greater than or equal to 2 V, and LO less than or equal to 0.8 V) by DAC/low-pass filter HY802. Hybrid HY802 then routes the PL/DPL decode data to options buffer U810 in the processor section of the station control board.

4.3.3 Hybrid HY802 also produces the PL/DPL encode tones. This is accomplished by using the data bits sent by PL/DPL DAC latch U808 in the processor section. The filtered tones for either PL or DPL are routed to the instantaneous deviation control (IDC) R889 adjustment circuit in the audio routing/control section of the station control board.

4.4 SQUELCH CONTROL CIRCUITS DESCRIPTION

4.4.1 Squelch Input

The input to amplifier U1550A is a noise pre-emphasis network that boosts the noise content of the input signals above 5 kHz. For squelch processing, the first amplifier/limiter is driven into limiting to prevent audio signals from squelching the receiver. Amplifier/limiter U1550B again amplifies the noise signal and relimits audio signals to provide further protection against audio signals squelching the receiver. The output signal of U1550B is then used to drive both the audio and repeater squelch circuits.

4.4.2 Audio Squelch Detector and Switching Circuits

4.4.2.1 The amplified noise output signal level is adjusted by SQUELCH control R1531 and sent to the noise detector (U1550D) via audio squelch buffer U1550C. The input network to the detector provides further attenuation of audio and any harmonics generated by audio limiting at the output of U1550B. Noise detector U1550D is a half-wave rectifier amplifier that produces negative going spikes at its output. The average dc value of these spikes is a function of received signal strength. The lowest average dc output voltage corresponds to a no-signal input (maximum noise) condition. As the received signal strength increases, the noise level decreases, and the average dc output voltage increases.

4.4.2.2 The squelch switching circuit operates in two modes. With a receive signal just above the opening sensitivity, squelch closing is slow (approximately 150 ms), which produces the squelch tail heard at the end of a received message. The 150 ms delay is present to prevent the received message from being chopped during a weak fluttering signal. With a strong signal (approximately 10 dB above opening sensitivity), squelch closing occurs immediately after the end of a received signal. This prevents the squelch tail from being heard.

4.4.2.3 Active integrator U1552D provides squelch opening and slow squelch closing. Comparator U1552B compares the detector's average dc output voltage with a reference voltage to determine the level for squelch opening and closing.

4.4.2.4 Fast squelch closing is provided by U1552C. A strong signal charges C1553 through R1545, driving U1552C low. At the end of a strong signal, any noise spikes from the detector are captured by CR1523. This immediately discharges C1553 and forces U1552C high. Then, capacitor C1552 forces U1552B to close the squelch.

4.4.3 Remote Squelch Control

Remote squelch switch Q1506 is remotely signaled to switch REM SQ control R1529 in parallel with R1531. This reduces the noise level input to the audio squelch circuit. It serves to provide a remotely controlled second squelch level that is lower than that of the primary audio squelch control setting.

4.4.4 Squelch Adapt Control Switch

Squelch Adapt Control Switch Q1507 is turned off when the synthesizers are in the "adapt" mode. When off, the collector of Q1507 goes to 9.6 V, forcing U1552C low and U1552D high. This causes the squelch to be in a fast detect mode.

4.4.5 Channel Activity Switch

The output of U1552D is used to control Q1508. This provides a fast responding open collector output signal to the processor section. This signal is used in channel-scan operation.

4.4.6 Repeater Squelch Detector and Switching Circuits

4.4.6.1 The repeater squelch circuits are very similar to the audio squelch circuits. They provide a separate adjustable squelch level for controlling the repeater function. The amplified noise output signal level is adjusted by RPTR SQ control R1558 and sent to noise detector U1551B via RPTR squelch buffer U1551A. The input network to the detector provides further attenuation of audio and any harmonics generated by audio limiting at the output of U1550B.

4.4.6.2 Noise detector U1551B is a half-wave rectifier amplifier that produces negative-going spikes at its output. The average dc value of these spikes is a function of received signal strength. The lowest average dc output voltage corresponds to a no-signal input (maximum noise) condition. As the received signal strength increases, the noise level decreases, and the average dc output voltage increases.

4.4.6.3 Active integrator U1551C provides squelch opening and slow squelch closing. Comparator U1551D compares the voltage to determine squelch opening and closing. The tight squelch level for the repeater squelch is typically 2 dB greater than the audio squelch. Squelch closing time is typically 200 ms.

5. AUDIO ROUTING/CONTROL SECTION THEORY OF OPERATION

5.1 GENERAL

5.1.1 The major audio routing for proper base station/repeater operation is accomplished by the circuits in this section of the station control board. There are five audio control gates (refer to schematic diagram), as follows:

- RX1 Audio Gate (U832A)
- TX Audio Gate (U832B)
- Local Audio Gate (U832C)
- Repeater Audio Gate (U831A)
- Alarm Audio Gate (U831B)

The five gates control four major audio signals, as follows:

- Local audio
- Transmitter audio
- Receiver 1 audio
- Alarm tones

The gates route the various audio signals to the proper summing amplifiers as required to produce the desired audio outputs as determined by the PTT signal and the control program.

5.1.2 When more than one type of PTT command occurs simultaneously, then the station control module operating program chooses the PTT with the highest priority. The PTT priority is determined by the code plug programming and can be varied on a per-channel basis. For example, channel 1 may be programmed with line PTT having priority over repeater PTT, and channel 2 may be programmed oppositely, in the same station.

5.1.3 Unless specified to be different, the stations are normally programmed with line PTT having priority over repeater PTT and *both* having priority over local PTT. Only those control functions associated with the priority PTT will occur. For example: if a line PTT and local PTT occur together, and if line PTT has priority, then the TX audio gate will open, routing remote wire line audio to the transmitter; while the local audio gate will be closed, preventing local microphone audio from reaching the transmitter.

5.1.4 Any PTT command has priority over the XMIT position of S802 on the front panel of the station control module. However, the activation of S802 to the XMIT position will cause transmit PL or DPL to be stripped from any other PTT transmit signal. Additional details for gate timing and routing are included in the theory notes given on the schematic diagram for the audio routing/control section.

5.2 SUMMING NETWORK/AMPLIFIERS

5.2.1 The three summing network/amplifiers (U834B, C, and D) combine and amplify the selected audio signals for output from the station control board.

5.2.1.1 The transmit audio summing amplifier (U834D) buffers:

- local audio (either from the microphone, via CONTROL connector J812-4, or the local audio, from EXPANSION connector J800-33)
- transmit audio from remote control connector J804-5
- RX1 (receiver 1) audio via repeater audio gate U831A, from the audio control and squelch section of the station control board.

The buffered TX audio signal modulates the selected transmit frequency for the base station.

5.2.1.2 The select audio summing amplifier (U834B) buffers:

- transmit (TX) audio
- received (RX1) audio
- automatic station identification and alarm tones (AUTO ID/ALARM)
- RX2 audio (from a second receiver via J800-35).

The buffered select audio signals provide an output to the local speaker at J812-2, via the 1/2 watt audio circuits, or to other local speakers, via J800-32.

5.2.1.3 The line audio summing amplifier (U834C) buffers:

- local audio
- RX1 audio
- RX2 audio and
- AUTO ID/ALARM audio.

The buffered line audio signals provide an output to the remote control board, via J804-4, where it is amplified for outbound wireline transmission.

5.2.2 For dual receiver stations, second receiver audio is filtered for PL/DPL tones, then de-emphasized and gated on the control board of the second receiver. The filtered and gated RX2 audio is then routed to the station control board via J800-35. When a second receiver is used, jumper JU11 is removed (see diode/jumper usage in Table 3).

5.3 AUTO ID LOW-PASS FILTER

Under program control, the MPU generates a square wave signal at an 800 Hz rate (at U801-8) for the automatic station identification code and at a 1600 Hz rate for alarms. The automatic ID low-pass filter circuit (U835C) removes most of the harmonics of the tones, attenuating the alarm tones relative to the automatic ID tones. The alarm tones produce about ±1.5 kHz deviation upon transmission and the ID tones about ±2 kHz deviation. The ID and alarm tones are routed through the splatter filter circuit to the IDC summing amplifier, bypassing the preemphasis circuit of C835 and R8132. Both types of tones are also routed to the local speaker amplifier and outbound wireline circuits.

5.4 TRANSMIT AUDIO CIRCUIT

5.4.1 The buffered transmit audio signal is routed from the TX Audio Summing Amplifier (U8340) to amplifier circuit U838B, which provides preemphasis (via C835 and R8132) and serves as a limiter before the IDC summing amplifier. The preemphasis circuit, enhances the audio frequencies toward the high end of the transmit audio frequency range (300 to 3000 Hz). Limiter amplifier U838B clips the audio at about 5.8 volts, peak-to-peak (2.1 VRMS), to prevent excessive audio modulation of the transmitted signal (with low-voltage audio inputs, the amplifier acts as a linear gain stage).

5.4.2 The preemphasized, limited audio is resistance coupled to splatter filter U838A, a 3 kHz low-pass filter that removes the high order harmonics from the audio signal. Having a unity gain, the amplifier is used to attenuate the high-frequency harmonics that are present in the clipped audio signal from the preemphasis/limiter circuit. The splatter filter output, which contains voice audio and automatic ID/alarm tones, is then combined with the PL/DPL encode tones at IDC summing amplifier U835D. The audio level presented to the amplifier input is controlled by IDC/DEV control R889, which can be accessed from the front of the control tray.

5.5 DEVIATION CONTROL CIRCUIT

5.5.1 The deviation bias gate (U831C) is used for applications where a temporary reduction in transmitter frequency deviation is required to optimize the system. When gate U831C is on, the audio from the splatter filter circuit is shunted by R884, which reduces the maximum deviation from ±4.6 kHz (the normal setting for deviation adjusted through IDC/DEV control R889) to ±3 kHz. The deviation bias gate can also be used as an audio boost circuit in paging or similar applications.

5.5.2 In paging or similar applications, deviation bias gate U831C is off when transmitting without PL/DPL tone encoding, allowing maximum deviation of ±4.6 kHz from voice alone. The gate is on when transmitting with PL/DPL, which reduces the voice audio level, and again allows ±4.6 kHz maximum deviation with both voice and PL/DPL. Shunt resistor

R884 must be changed for this application, and maximum deviation must be adjusted for transmission with or without PL/DPL, whichever is greater. Both changes are used only in custom applications.

5.6 LOCAL SPEAKER AUDIO CIRCUIT DESCRIPTION

The buffered select audio from Select Audio Summing Amplifier U834B is applied directly to VOLUME control R876, which is accessible from the front of the control tray. The control adjusts the audio level for all local speakers connected to the base station. Select audio is also routed from the VOLUME control wiper to J800-32. The output from the VOLUME control wiper is coupled to 1/2 W Audio Buffer U834A for buffering and amplification, then to 1/2 W Speaker Audio Amplifier U836 for final amplification. A local speaker connection rated for 1/2 W into a 3.2 ohm impedance speaker is available, via tapped transformer T801, at CONTROL connector J812-2.

6. EXPANSION CONNECTOR

6.1 GENERAL

The station control tray EXPANSION connector, J800, provides interface lines which connect power, audio and digital signals between the station control board and other control modules within the station and external equipment. The connector is a 40 pin flat ribbon cable header and is accessed through the top of the control tray. There are five types of signal lines provided, as follows:

- audio lines
- dedicated logic lines
- multiplexed logic (MUX bus) lines
- power lines
- spares.

6.2 AUDIO LINES

6.2.1 Quad Audio (Pin 39)

The Quad Audio signal, originating on the station control module, is buffered, raw audio from the receiver quadrature detector. All receiver audio, coded squelch or other signaling tones, and receiver noise are available on this signal line. The signal is not muted by the receiver squelch circuitry. The signal line is driven by a low impedance op-amp, biased at 4.8 V dc, and the ac signal level is nominally 400 mVrms.

6.2.2 RX1 Audio, (Pin 38)

The RX1 Audio signal, originating on the station control module, is receiver audio that has been deemphasized and filtered to remove coded squelch signaling tones. The audio signal is not muted by the receiver squelch circuitry. The signal line is driven by a low impedance op-amp driver biased at 4.8 V dc, and the ac signal level is nominally 325 mVrms.

6.2.3 Select Audio (Pin 32)

The Select Audio signal, originating on the station control module, is the audio input for the local speaker amplifier circuit in the Diagnostic Metering Panel option. Any of these audio signals will be present on the select audio line when it is gated on by the control circuits in the station: primary receiver audio, secondary receiver audio, transmit audio from the remote wire line, and automatic station I.D. and alarm tone audio. The signal line is connected to the wiper of the VOLUME control on the control tray front panel. The dc bias level and ac level are variable depending on the VOLUME control setting.

6.2.4 Local Audio (Pin 33)

The local audio signal line is an alternate input for microphone audio to the station. It should not be used when a service microphone or handset is used for local keying. The audio on this signal line is gated to the transmit audio circuits and to the remote control module line driver circuits when a local PTT occurs. The signal line provides a signal pull-up to 9.6 V and a 560 ohm input impedance.

6.2.5 TX Audio (Pin 36)

The TX audio signal, originating on the remote control module, is the inbound transmit audio from the remote control wire line. It is gated to the transmit audio circuits and the local speaker when a line PTT occurs. The signal line is driven by a low impedance op-amp driver, biased at 4.8 V dc, and the ac signal level is nominally 200 mVrms.

6.2.6 TX Data Audio (Pin 34)

The TX Data Audio signal is an input to the station control module which is used (in special applications) to modulate the transmitter, bypassing the control circuits, pre-emphasis, and IDC circuits. This input is dc coupled to the modulator and must be biased to 4.8 V dc. The level of the input signal must be adjusted at the signal source to assure proper transmitter deviation. When this input is used, a resistor must be added to the station control module at the circuit point labeled R898 on the schematic and overlay. When the input is not used, R898 should be omitted. Since this input bypasses the control and IDC circuits, a special FCC filing is required when it is used.

6.2.7 RX2 Audio (Pin 35)

The RX2 Audio signal is an input to the station control module for audio from a second receiver. The

audio must be de-emphasized, filtered to remove coded squelch tones, and switched on and off by the second receiver squelch circuits, before being applied to the RX2 Audio line. The station control module input is ac coupled with an input impedance greater than 13k ohms. When a second receiver is used, JU11 is removed from the station control module. When the input is not used, JU11 is installed.

6.3 DEDICATED LOGIC LINES

6.3.1 Expansion Reset (Pin 12)

The Expansion Reset signal is a shared logic line which allows a clean, coordinated start up of the station control module and any other interconnected modules or external equipment. The Expansion Reset signal is active low at power-up, or S801 is put into the TEST position, or when activated, or when the watchdog timer resets the station control module's or when the remote control module receives a command to reset the station. Also, normal MUX bus (multiplex logic lines, described in subsequent paragraphs) operation is suspended while RESET is active low. The data strobe line, $\overline{DS}$, is held inactive and the address and data lines do not follow their normal patterns.

IMPORTANT

While the Expansion Reset line is active low, no module except the station control module should write to the MUX bus data lines. Otherwise, the station control module may fail its self diagnostic tests, and remain reset indefinitely.

6.3.2 IPCB (Pin 11)

The interprocessor communications bus (IPCB) signal line has the following characteristics:

- Single "party" line
- Half duplex
- 5 V
- Open collector
- Non-return to zero (NRZ) format
- 1200 baud serial port

Single "party" line means that only one module can transmit at a time. All modules will receive (including the one transmitting) unless the MPU "wake- up" serial port feature is used. Refer to the MC6801 8-Bit Single Chip Microcomputer Reference Manual MC6801RM(AD) for further details concerning the IPCB. Open collector drivers allow nondestructive contention.

6.3.3 Shutdown (Pin 23)

The Shutdown signal line is an enable line for any auxiliary 5 V supplies connected to EXPANSION connector J800. Its purpose is to prevent the auxiliary 5 V supplies from turning on, and enabling any controlled expansion modules microprocessor to operate, unless the station control module 5 V supply comes on. This prevention is done so that the station control module MPU is allowed to control the start-up sequence.

6.4 MULTIPLEXED LOGIC (MUX bus) LINES

6.4.1 The multiplexed logic (MUX bus) lines consist of the following lines:

- 4 Address lines (BA0-BA3)
- 4 Data lines ($\overline{BD0}$-$\overline{BD3}$)
- Data strobe ($\overline{DS}$).

All MUX bus lines are referenced to logic ground. The 4 address and 4 data lines define 16 words of 4 bits each, or 64 total bits as shown in Table 4. These bits form a multi-directional digital communications path. The bus is multiplexed to conserve interconnections (64 connections reduced to 9) and to increase future expansion capability. The data strobe and the 4 address lines are driven by the station control module. The data lines are inverted and open collector driven. This allows multiple hardware modules (and the optional diagnostic metering panel) to drive the same bit in a nondestructive, wired "OR" fashion.

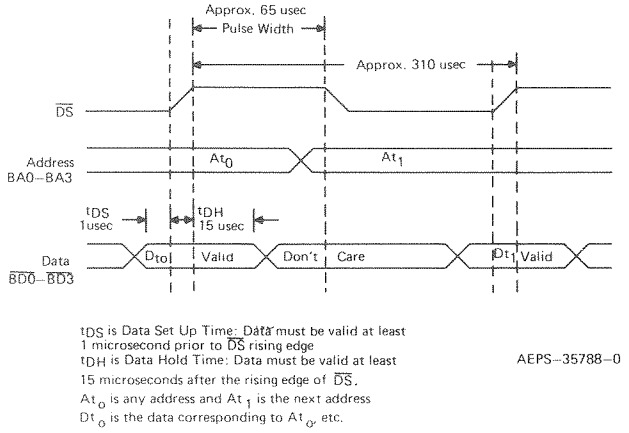


Figure 8. MUX Bus Timing Diagram

6.4.2 The MUX bus timing diagram is shown in Figure 8. The address lines are incremented once, approximately every 310 microseconds. The address changes when data strobe is inactive ($\overline{DS} = 1$). The data must be valid for 1 microsecond before the rising edge of $\overline{DS}$. The data must be valid for 15 microseconds after the rising edge of $\overline{DS}$. At certain times, the MUX bus may be momentarily halted, for instance, during channel scan. The halt is in effect an extended period of inactive data strobe. The address lines will be driven, but will remain the address of the MUX bus cycle just prior to the halt. The data lines are in a "don't care" state during a halt and may be random. Any MUX bus bit which, when activated by any module other than the station control module, does not change the state of the station is called a "status only" bit. As an example of a "status only" bit, "Transmitter Activity" (TX ACT) is activated by the station control module whenever the transmitter has successfully keyed. But, if another module activates TX ACT, the transmitter will not key. Thus, TX ACT is a "status only" MUX bus bit. All "status only" MUX bus bits are signified in Table 4 by a double asterisk (**).

Table 4. MUX Bus Bit Map

Address On BAØ-BA3	BD3	BD2	BD1	BD0
0	SP XMT	SCAN	T ALM DS	S ALM DS
1	RPT PTT	LIN PTT	LOC PTT	INTCOM
2	TX PL DS	TX ACT**	RX2 ACT	RX1 ACT
3	RX PL DS	R1 PL DT	R1 SQ LV	R1 UN SQ**
4	R2 MUTE	R2 PL DT	R2 SQ LV	R2 UN SQ**
5	GD TN DT	AUX DET	RPT KD	RPT USQ**
6	ACC DIS**	EX DA DT	DVP SEL	DVP C/C
7	*	*	*	*
8	TX RX C8	TX RX C4	RX C2	TX RX C1
9	AUX C8	AUX C4	AUX C2	AUX C1
10	*	*	*	*
11	*	*	*	*
12	RW4 OVG	RW3 SYN	RW2 PA	RW1 BAT
13	RWC8	RWC7	RWC6	RWC5
14	FWC4	FWC3	FWC2	FWC1
15	FWC8	FWC7	FWC6	FWC5

* currently unassigned
** status only bits

7. MAINTENANCE AND TROUBLESHOOTING

7.1 SELF DIAGNOSTIC ROUTINES

7.1.1 General

7.1.1.1 The station control board features self-diagnostic routines that make it possible to troubleshoot the digital circuits with standard bench test equipment (e.g., oscilloscope) in most cases. The board is equipped with a self-diagnostic routine that it performs when the station is first powered up, or whenever S801 (on the front panel) is put into the TEST position. The routine checks the integrity of MPU U801, program EPROM U804, Code Plug U803, the MUX bus read/write circuits, and the serial port (IPCB) read/write circuits, in that order. If any of these basic blocks fail the self test, the MPU flashes the TEST LED repeatedly, as specified number of times (one, two, three, or four times), to indicate the failure that was discovered. It then waits about 1.5 seconds and resets the board by failing to tickle the watchdog circuits. Refer to the Watchdog Timer paragraphs in this section of the manual. When the watchdog circuit resets the board, the TEST LED flashes once, with a flash that is shorter than the failure indication flashes. After the watchdog circuit resets the board, the diagnostic routine is repeated. If the board fault remains unchanged, the routine locates it again, flashes the TEST LED, and resets the board again. The result is that the board sends a sequence of flashes, a short flash, another sequence of flashes, a short flash, etc. The interpretation of the TEST LED indications is given in the Self-Diagnosed Failures paragraphs in this section of the manual.

7.1.1.2 The station control board may fail in such a way that the program routines cannot be run, including the power-up self diagnostic routine described previously. This indicates a major digital circuit failure. The watchdog circuits aid in determining these failures, yet keeps the station in a benign state until the program routines are again running correctly. When this type of failure occurs, the TEST LED is on steadily, or else flashing at a rapid rate (many times per second). Troubleshooting this type of failure is described in the Watchdog Reset Failure paragraph in this section of the manual.

7.1.1.3 Another possible failure is associated with EXPANSION connector J800, termed Expansion Reset failure. The expansion drive circuits on the station control board work with a limited total length of flat cable and a limited number of external modules (including any remote control board). If a capacitive load in excess of 288 picofarads, including the capacitance of the flat cable and all integrated circuit loads, is attached to the Expansion Reset line, the board may reset at the end of the power-up self-diagnostic routine. At the end of the routine, the MPU (U801-16) Expansion Test signal switches from low to high and the Expansion Reset line also switches from low to high. The low-to-high transition of the Expansion Reset line is slowed down by excessive capacitance on the line, allowing C879 in the Reset Arbiter circuit to charge up and reset the MPU U801. If the MPU is reset in this manner, then the power-up self-diagnostic routine is repeated and the Expansion Reset failure is also repeated. Indication of this failure is a series of short flashes on the TEST LED, spaced about 2 seconds apart. Excessive loading of the EXPANSION connector J800 should be carefully avoided when adding expansion modules to the control circuits.

7.1.2 Watchdog Reset Failure

This type of board failure is indicated when the TEST LED is on steadily, or else flashing at a rapid rate (many times per second). When this major digital circuit failure indication is seen, the following procedure should aid in finding the failed circuit.

Step 1. Use an oscilloscope in the dc coupled mode of operation, to look at the signal at the reset (RES) pin of the MPU, U801-6. The normal signal at this pin is always high. A series of low pulses, of 2 milliseconds duration, approximately, occurring every 10 milliseconds to 250 milliseconds, indicates a type of reset caused by the MPU watchdog circuit when it finds a fault in the series of MPU tickle pulses. If this type of signal is present at U801-6, proceed to Step 2. If the signal at U801-6 is always low, the fault is probably in the reset arbiter circuits, proceed to the Reset Arbiter paragraphs in this section of the manual.

Step 2. Look at the signal at the watchdog tickle (WDT Tickle) pin of the MPU, U801-17. The signal should be high during the short reset pulse. The signal should switch low within 10 seconds of the time that

reset pin (U801-6) switches high. After this point, a high pulse should occur approximately every 53 milliseconds. If the WDT Tickle signal does not switch low after the reset pulse, this indicates that the board is failing at the beginning of the self-diagnostic routine. The board fault is probably in one of four areas: either MPU U801 is faulty, program EPROM U804 is faulty, Address Latch U802 is faulty, or there is a short circuit on one of the MPU address or data lines. Proceed to Step 6. If the WDT Tickle signal does go low after the reset signal, then either the WDT Tickle signal pulses are not spaced properly (approximately 53 milliseconds apart), or there is a failure in the watchdog timer circuitry. To troubleshoot this type of failure, proceed to Step 3.

Step 3. When WDT Tickle pin U801-17 goes low, U814-13 should switch high, making U824-10, -8, and U814-9 all high. Look for these signals to occur before proceeding. If they do not, look for some fault causing this malfunction.

Step 4. Check the signal at U806-5. It should go high when WDT Tickle pin U801-17 goes low, and stay high for approximately 9 to 21 milliseconds, and then switch low until the WDT Tickle signal switches from high to low again. If the WDT Tickle signal goes high sometime before U806-5 goes low, then both pins U823-13 and U823-12 are high making U823-11 low. This will reset the MPU via U814A and U814B. This action indicates that the self-diagnostic routines are not running properly. Proceed to Step 7.

Step 5. Check U814-13 again. If this pin is staying high for more than 80 milliseconds before switching low, this indicates that the self-diagnostic routines are not running properly. Proceed to Step 7.

Step 6. Look at the E (Enable) pin U801-40. The signal on this pin should be a square wave that is low for 408 nanoseconds and high for 408 nanoseconds. If this signal is not present, or has the wrong duty-cycle, check the supply lines to the MPU and the connections to crystal Y801 and capacitors C801 and C802. If all these connections are correct and the proper signal is not present, replace MPU U801.

Step 7. Look at Address Stobe (AS) pin U801-39. The signal on this pin should be a square wave that is high for 200 nanoseconds and low for 600 nanoseconds. If this pin is not changing, or has the wrong duty-cycle look for a short circuit on the line. If there is no short, either MPU U801 or Address Latch U802 is defective.

Step 8. Look at: the High-Order Address pins U801-22 through -29; the Low-Order Address pins U802-2, -5, -6, -9, -12, -15, -16, and -19; and the data pins at U801-30 through -37. If any of these pins are not changing state (are either always high or always low) look for a short circuit on that line.

Step 9. Look at MPU programming pins U801-8 and U801-10. When U801-6 goes low, these pins should also be low. When U801-6 switches high, the pins also switch high, momentarily. If these pins do not go low, check programming diodes CR801 and CR803. MPU U801-6 can be forced low by putting S801 to the TEST position on the front panel.

Step 10. If none of the previous steps reveals a fault, then probably either Program EPROM U804 or MPU U801 is damaged and should be replaced. Return to Step 1.

7.1.3 Self-Diagnosed Failures

Certain station control board faults are indicated by a series of 1, 2, 3, or 4 flashes of TEST LED DS807, followed in about 1.5 seconds by a short flash (the MPU resetting itself), followed about 4 seconds later by another series of 1 through 4 flashes, etc. This recurring pattern indicates that the self-diagnostic routine is running and is detecting a fault in the station control board circuits. The meaning of the different sets of flashes is as follows:

- One Flash —

  This indicates that either MPU U801 or Program EPROM U804 is defective and should be replaced.

- Two Flashes —

  This indicates that Code Plug U803 is defective and should be replaced.

- Three Flashes —

  This indicates that the MUX bus is not operating properly. The self-diagnostic routine determines this by writing a certain address anr data pattern to the MUX bus and reading the same data back. If the read or write circuits on the station control board fail, the routine indicates the failure. If one of the MUX bus lines on J800 is shorted, or if another module connected to the MUX bus lines fails and shorts one of these lines, then the routine indicates this fault also. Note that during the self-diagnostic routine, MPU Expansion Test pin U801-16 is low, which causes the Expansion Reset signal on J800-12 to be low. This low should disable all modules that are connected to J800 from writing outputs to the MUX bus lines, since writing to the lines would cause a fault condition during the self-diagnostic routine.

  The self-diagnostic routine has an added feature to aid in troubleshooting the MUX bus lines when a MUX bus fault is indicated. If the collector of Q803 is shorted to ground with a jumper, the watchdog timer is disabled, preventing a watchdog reset to the MPU. When this is done, the self-diagnostic routine writes a fixed pattern of data to the address and data lines of the MUX bus via MUX bus Write Latch U811. The BAØ output at U811-2 should be a square wave that is

low for 45 microseconds then high for 45 microseconds, then low again. Address line BA1 at U811-5 is also a square wave signal changing at half the rate of BAØ (i.e., high for 90 microseconds then low for 90 microseconds). Each subsequent address or data line on U811 is a square wave at half the rate of the previous line (i.e., BA2 is 180 microseconds; BA3 is 360 microseconds; WDØ is 720 microseconds; etc.). With this fixed pattern, the MUX bus read and write circuits and the MUX bus lines on J800 can be checked with an oscilloscope.

- Four Flashes —

  This indicates that interprocessor communication bus (IPCB) J800-11, J804-14, or J812-1 is not operating properly. The self-diagnostic routine determines this by writing a string of high and low levels to the IPCB and reading the string back. If the read and write circuits fail or if the IPCB line on J800-11 is shorted, the self-diagnostic routine indicates a failure.

  The self-diagnostic routine has another added feature to aid in troubleshooting the IPCB circuits when a fault is indicated. If the collector of Q803 is shorted to ground with a jumper, as described previously, the self-diagnostic routine writes a series of alternating high and low levels to the IPCB line via IPCB Out pin of the MPU, U801-12. The line continues to switch from high to low indefinitely until the MPU is again reset. With this continuous signal coming from the MPU, the IPCB read and write circuits can be checked with an oscilloscope.

7.1.4 Reset Arbiter

The following procedure describes and examines faults that are indicated when reset pin U801-6 of the MPU is always low.

Step 1. Look at the Expansion Reset signal on U826B-4 or J800-12. If this signal is always low, disconnect any external connection to J800, and remote control connector J804. If this removes the fault, and the station control board comes out of reset, then check for a short on the disconnected items.

Step 2. If Step 1 does not solve the problem, or no short is found, check the Expansion Test signal at U801-16. This signal should always be high if the MPU is always reset. Also check that U826C-6 is low, and that pull-up resistor R882C (by Q705 collector) on the Expansion Reset line is connected.

Step 3. If the Expansion Reset signal is high, but the MPU Reset pin U801-6 is low, then look for a fault in the logic circuitry between those points: U822D, U823B, U826C, U822E, U823C, and Q802.

7.2 STATION CONTROL INPUT/OUTPUT (RADIO INTERFACE J801) SIGNALS

7.2.1 General

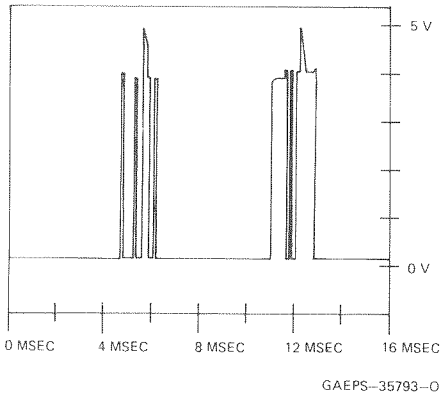
7.2.1.1 The MPU communicates with the RF Tray via radio interface connector J801, to the remote control board via remote control connector J804, and to any expansion modules via EXPANSION connector J800. The MUX bus address and data lines, the IPCB line, and the EXPANSION RESET line are located on J800 and J804. Troubleshooting procedures for these lines are explained in the preceeding paragraphs. Signals for the INTERCOM and ACCESS DISABLE function and the remote control Command lines are located on J804.

7.2.1.2 The radio interface connector J801 routes signals used for loading the transmit and receive synthesizers, the PA Key command, the Antenna Relay, and command, and the PA Power cutback command. Troubleshooting procedures for these signals are explained in the following paragraphs. There are also signals on J801 that indicate that the synthesizers are locked and that the PA is on and at full power. These functions are displayed on the LED's located on the front panel of the Control Tray. Although these function displays are located on the control tray, the actual circuits represented are located on the Uniboard in the RF Tray. If a failure of one of these functions is indicated by the LED's, consult the troubleshooting procedure for the Uniboard. For example, if the RX LOCK LED is off, this indicates that the receiver synthesizer, located on the Uniboard, is out of lock.

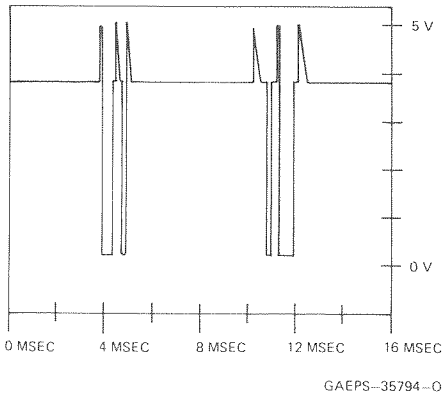
7.2.2 Synthesizer Loading Lines

7.2.2.1 The synthesizers are loaded with data sent from the station control board via J801. The data is sent in packets, of approximately 2 milliseconds duration, with the packets spaced from 5 to 10 milliseconds apart on the SAØ, SA1, SA2, SDØ, SD1, SD2, and SD3 pins. While the packets are being sent, each line exhibits a number of transitions between high and low logic levels. Between the packets, the lines hold one state (either high or low). Figures 9a and 9b are representative of the type of signals to expect.

7.2.2.2 The synthesizer data is actually loaded when the transmit and receive strobe pulses, TX Strobe and RX Strobe, are sent by the station control board, via J801, to the appropriate synthesizer. Seven pulses occur on each strobe line during each packet of synthesizer data. The strobe pulse duration is very short, from about 450 nanoseconds to 1 microsecond long. Figures 10a and 10b are representative of the packets of strobe pulses and of one strobe pulse on an expanded scale.

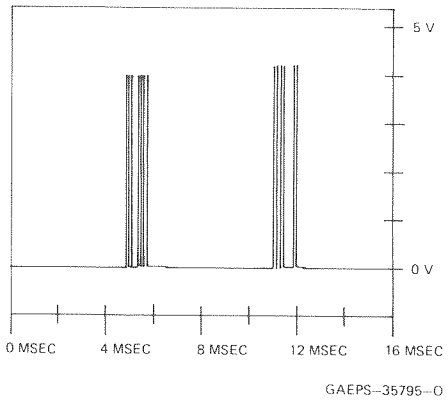


a. Normally Low

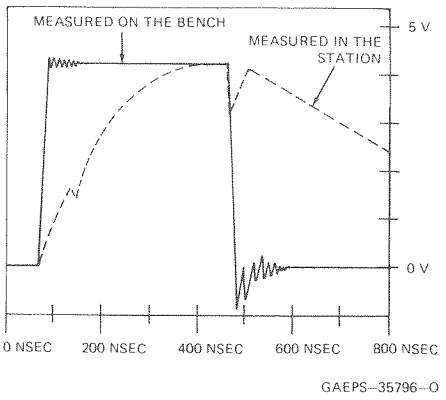


b. Normally High

Figure 9.
Typical Waveforms for Synthesizer Loading Lines



a. Strobe Pulses



b. One Strobe Pulse

Figure 10.
Typical Waveforms for Synthesizer Strobe Lines

7.2.2.3 To assure that the station control board is loading the synthesizers properly, it is only necessary to assure that the synthesizer address and data lines are changing state and that the synthesizer strobe pulses are occurring. It is not necessary to check that the data itself is correct. The data is located in the code plug and the validity of code plug data is assured by the self-diagnostic routine that the station control board performs when the station is powered up or when S801 is put into the TEST position.

7.2.3 PA Key Signal

The PA Key Control signal is generated by the MPU at pin U801-15, and is controlled by two failsafe circuits. The first failsafe circuit is U824B. If the MPU watchdog circuit detects a failure, the Delayed Reset signal from U806A-4 prevents a PA Key signal by applying a low signal to U824B-5. The second failsafe circuit is Synthesizer Failsafe U818A. If the transmit synthesizer comes out-of-lock anytime during a PA key operation (TX Lock line switches high), the Synthesizer Failsafe circuit prevents a PA Key signal until the end of all current push-to-talk commands, and until the synthesizer locks again. When the TX Lock line is high, U818A-4 is low, which causes U818A-5 to switch high. This causes U826D-8 to switch low and turns Q804 off, ending the PA Key signal. Pin U826D-8 remains low until the next time the MPU issues a new PA Key Control command, which causes U818A-3 to switch from a low to a high state.

7.2.4 Antenna Relay Signal

The Antenna Relay control signal is generated by Options Latch U807, and is buffered by Q806 to drive the antenna switch, via W900.

7.2.5 Remote Control Connector

The four remote control command lines (CMD Ø, CMD 1, CMD 2, and CMD 3) provide data from the current detector circuits, and data from the CHANNEL select switch S901, on the remote control board to the station control board, via J804. These lines provide open collector outputs, and their pull-up resistors are located on the station control board.

7.3 STATION CONTROL BOARD BENCH TEST CONNECTIONS

7.3.1 DC Power Connections

The station control board requires two dc supplies to operate: A+ (approx. 13.8 V dc) and 9.6 V dc. The A+ supply is attached at pin 1 (positive terminal) and pin 5 (negative terminal) of power connector J701. The A+ supply should be capable of at least 2 amperes at 13.8 V dc. The 9.6 V supply is connected to the test pin marked +9.6 V (positive terminal) and the negative terminal to either J701-5 or one of the test pins marked A.G. (Audio Ground). The board itself generates the required 5 V supply for the digital circuits. When troubleshooting the 5 V dc-dc converter, the digital circuits can be disconnected from the 5 V supply by removing jumper JU8. Both dc supplies must be connected before the 5 V dc-dc converter will operate. When the dc-dc converter is operating, the small green LED (DS710) in the converter section will light.

7.3.2 Radio Interface Lines

In order to test the control and audio circuits, four control signals from the RF Tray to the station control board (via J801-8, -10, -12, and -15) must be simulated on the bench. The four signals are RX Lock, TX Lock, PA On, PA Full Power. To provide the correct simulation, the four control lines must be shorted to ground.

7.3.3 Audio Connections

7.3.3.1 Receiver audio can be simulated by connecting an audio signal generator to TP3 (by J801-5) via a dc blocking capacitor. The ac levels shown on the schematic for the receiver audio assume a 650 mV rms signal at TP3.

7.3.3.2 Mic audio can be connected to the board by plugging a test palm microphone or handset into J812, or by attaching simulated signal generator to an audio TP8 (by J812-4), and to A.G. The ac levels on the schematic assume a 120 mV rms signal at TP8. The microphone PTT button causes a MIC PTT, as does grounding TP9 (by J812-3).

7.3.3.3 Inbound audio, that would have come over the wireline via the remote control board, can be simulated by attaching an audio signal generator to J804-5 and to A.G. The ac levels on the schematic assume a 200 mV rms level at J804-5.

7.3.3.4 The TEK5 metering kit can be connected to CONTROL connector J812 (with the appropriate adapter plug) to provide speaker audio and microphone input when testing on the bench.

7.3.4 Other Connections

7.3.4.1 The optional Diagnostic Metering Panel will work with the station control board when operated on the bench. Connect the panel to the station control board by using the ribbon cable provided with the panel.

7.3.4.2 The remote control board will operate, if connected to the station control board before power up, as described previously. This means that the entire Control Tray can be removed from a station and tested on a bench with two power supplies and a few jumpers connected to RF Tray radio interface connector J801.

7.4 CHECKING THE STATION CONTROL BOARD IN THE STATION

The ac levels shown on the receiver audio circuits schematic represent typical levels when an on-frequency carrier, modulated with ±3 kHz deviation of a 1 kHz tone, is connected to the receiver rf input, J11. When a microphone is not available at the station, microphone audio can be simulated by connecting an audio signal generator to TP8 and to an audio ground pin (A.G.). A MIC PTT can be be generated by grounding TP9.

7.5 STATION CONTROL BOARD TESTS

7.5.1 Using Switch S802

7.5.1.1 Switch S802, located on the front panel of the Control Tray, has two positions, XMIT and PL DISable. In the XMIT position, it performs two functions. When used alone, it keys the transmitter without modulation (neither audio, nor PL or DPL signals). This feature can be useful when checking the transmit frequency of a transmitter that uses coded squelch. When used in conjunction with another push-to-talk signal, it strips the encoded PL or DPL signals from transmit audio, but otherwise has no effect. For example, if the transmitter was locally keyed with a microphone, and then S802 was held in the XMIT position, the serviceman could transmit normally, but the station would not be encoding PL or DPL signals.

7.5.1.2 In the PL DISable position, S802 defeats receiver coded squelch operation. This results in the receiver reverting to carrier squelch operation.

NOTE

The PL DISable position does not affect repeater operation, which still would require the proper coded squelch signals.

7.5.2 Audio Circuits

7.5.2.1 DC Bias Levels

The dc bias level at the output of all op-amps, except those in the squelch circuits, should be at V_B (about 4.8 V dc) when the circuits are operating properly. The dc bias level of the 1/2 Watt Amplifier, at U836-4, should be about 1/2 of the A+ supply level. U836 generates its bias level internally.

7.5.2.2 Receiver Audio Path Circuits

7.5.2.2.1 If the station receiver has the requirement of PL or DPL decode for squelch operation, then S802 should be put to the PL DISable position for these tests.

NOTE

The op-amps are high gain devices. Thus, very little or no audio should be seen at their input pins when they are operating properly.

7.5.2.2.2 Receiver quadrature audio, either noise or audio, should always be present at the outputs of the first three stages of the receiver audio path: Quad Audio Buffer U835A-1, PL/DPL High-Pass Filter hybrid HY803-15, and receiver audio adjust (RX LEV) and de-emphasis circuit at TP5 (also U833A-1). The level at TP5, and the subsequent circuitry is controlled by setting RX LEV control R841. Receiver audio is gated to the local speaker and remote control board by RX1 Audio Gate U832A. This gate is controlled by the MPU via level shifter U829F. The gate should be on when the audio squelch circuit indicates an unsquelch condition (this condition can be checked by measuring the output of the audio squelch circuit at TP7, which should be greater than 2.5 V. The gate is turned on by a high signal (about 9.6 V dc) at U832A-11. The PL DISable, S802 switch position removes any requirement for PL/DPL detection (or any auxilliary detection) to turn the gate on.

7.5.2.2.3 Receiver audio routed to the remote control board (inbound audio) can be measured at TP2. Receiver audio that drives the local speaker, via the 1/2 W audio amplifier, can be measured at TP1. The audio level at the Local Speaker is controlled by VOLUME control R876. By adjusting R876, the 1/2 W amplifier circuit should have an output greater than 1.25 V rms (1/2 W into 3.2 ohms) at CONTROL connector J812, between J812-2 and -5.

7.5.2.2.4 The gain of 1/2 W amplifier U836 is controlled by resistor divider R877 and R878, and fed back to U836-2. This feedback must be connected for stable amplifier operation (otherwise, it tends to oscillate at frequencies greater than 200 kHz). The amplifier also has a tendency to be unstable when driving a highly inductive load. High- frequency shunt circuit R879 and C839 compensates for this tendency. Output transformer T801 provides impedance matching for optimum operating efficiency in the amplifier. The voltage transfer ratio for the transformer is that the voltage at T801-3 is the voltage at T801-5, divided by the square root of 5 (about 2.24).

7.5.2.3 Transmit Audio Path Circuits

7.5.2.3.1 Outbound wireline audio from a remote control console enters the station control board from the remote control board via J804-5. This audio is gated to the transmit audio circuits and the local speaker by TX Audio Gate U832B. This gate is controlled by the MPU via level shifter U829A. The gate is on during a Line PTT or when INTERCOM switch S902 on the remote control board is in the INTERCOM position. The gate is turned on by a high signal (about 9.6 V dc) at U832B-10.

7.5.2.3.2 Local audio coming from a microphone connected to CONTROL connector J812 or coming from EXPANSION connector J800-33 is gated to the transmit audio circuits and the remote control board by Local Audio Gate U832C. This gate is controlled by the MPU via level shifter U829B. The gate is on during a local PTT. The gate is turned on by a high signal (about 9.6 V dc) at U832C-9.

7.5.2.3.3 In repeater stations, receiver audio is gated to the transmit audio circuits by Repeater Audio Gate U831A. This gate is controlled by Options Latch U807, via level shifter U829D. The gate is on during a Repeater PTT. The gate is turned on by a high signal (about 9.6 V dc) at U831A-13.

7.5.2.3.4 TX Audio Summing Amplifier U834D buffers the audio to the pre-emphasis and IDC circuit. The pre-emphasis circuit (R8132 and C835) to IDC limiter amplifier U838B causes a 6 dB/octave pre-emphasis in the 300 to 3000 Hz band. The voltages shown on the schematic at U834D-14, U838B-7, and U838A-1 represent typical ac voltages that cause ±3 kHz transmitter deviation for a 1 kHz audio tone. The waveforms shown at U838B-7 and U838A-1 represent the output of the limiter and splatter filter, respectively, at maximum system deviation.

7.5.2.3.5 Audio and PL/DPL tones are combined in the IDC adjustment circuit. The combined audio can be measured at TP4. With the IDC limiter in "hard limit," it should always be possible to adjust the signal level at TP4 to at least 4 V peak-to-peak by using IDC/DEV control R889. Refer to the Installation section of this manual for proper IDC setting.

7.5.2.4 Automatic Station Identifier Circuit

The network from C834 to U835C-8 is a low-pass filter that removes harmonic frequencies from the Auto I.D. and Alarm tone signals generated by the MPU. These tones are routed to the local speaker circuits and to the transmit audio circuits (bypassing the pre-emphasis to reduce distortion). The tones are gated to the remote control board by Alarms Audio Gate U831B. This gate is controlled by Options Latch U807 via level shifter U829E. The gate is on during alarm tones transmissions.

7.5.2.5 PL/DPL Decode Filter Circuit

The network from JU7 to U833C-8 is a low-pass filter with nearly unity gain below 200 Hz and falling rapidly above 200 Hz. U833D is used as a limiter that converts the PL or DPL signal at U833C-8 to a sharp square wave signal. This square wave signal passes through a logic gate on hybrid HY802 to convert the square wave to TTL logic levels. Transistors Q807 and Q808 are used to adapt the filter for optimum DPL filtering. When the PLDPL signal is low, Q807 and Q808 are on, and the filter is operating as a DPL filter.

7.5.2.6 PL/DPL Encode Digital-to-Analog Converter (DAC) and Filter Circuit

The circuits on hybrid HY802 convert data inputs from PL/DPL DAC Latch U808 into PL or DPL signals for transmission. The PL/DPL Encode Tones at output HY802-17 have only about 1% distortion and need no further filtering. The PL/DPL signal level is about 3.1 V peak-to-peak.

7.5.3 Digital Circuits

When performing maintenance on or troubleshooting the digital circuit portions of the station control board, the service technician should make use of the information presented on the schematic diagrams at the end of this section.

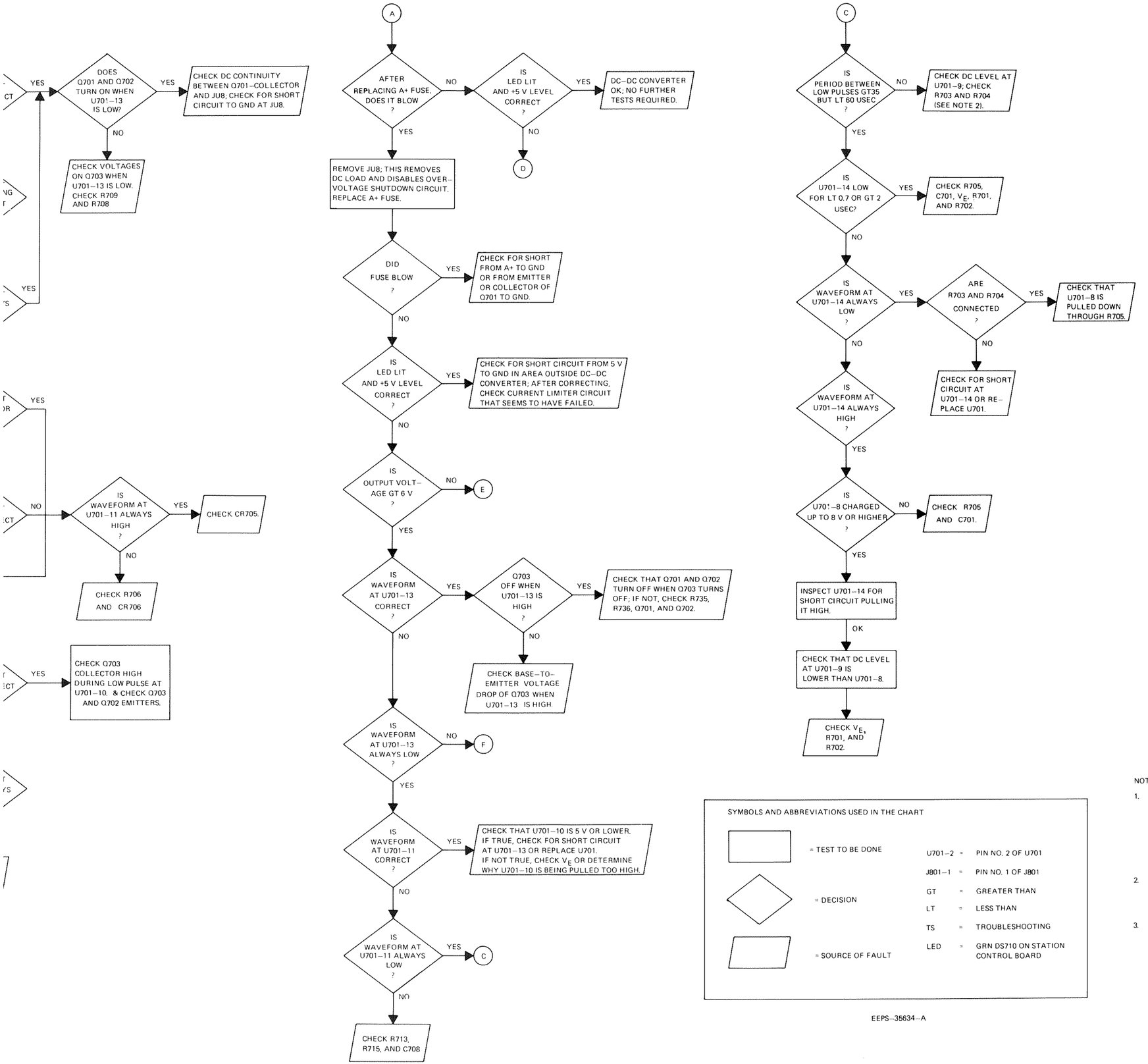
7.6 STATION CONTROL CODE PLUG

If a replacement station control module is ordered, the program EPROM in the new station control module will contain the latest version software which has been updated to accommodate various new *MSF 5000* station options. The new program EPROM software and the old code plug may not be compatible if the program EPROM, and the code plug are not of the same version. If they are incompatible, the test LED will flash twice (indicates bad code plug) and the station will not operate.

Code plug and EPROM compatibility can be determined by comparing the code plug version number with the EPROM version number as shown in the following chart. (The code plug version number is printed in the parameter booklet supplied with the station.)

EPROM Kit No.	Motorola Part No.	Code Plug Version Compatibility	Label No.
TRN5196A	51-90006C04	1, 2, 3	54-84691N02
TRN9261A	51-90006C24	3	54-84691N09

DC-DC CONVERTER
TROUBLESHOOTING CHART



SYMBOLS AND ABBREVIATIONS USED IN THE CHART

= TEST TO BE DONE

= DECISION

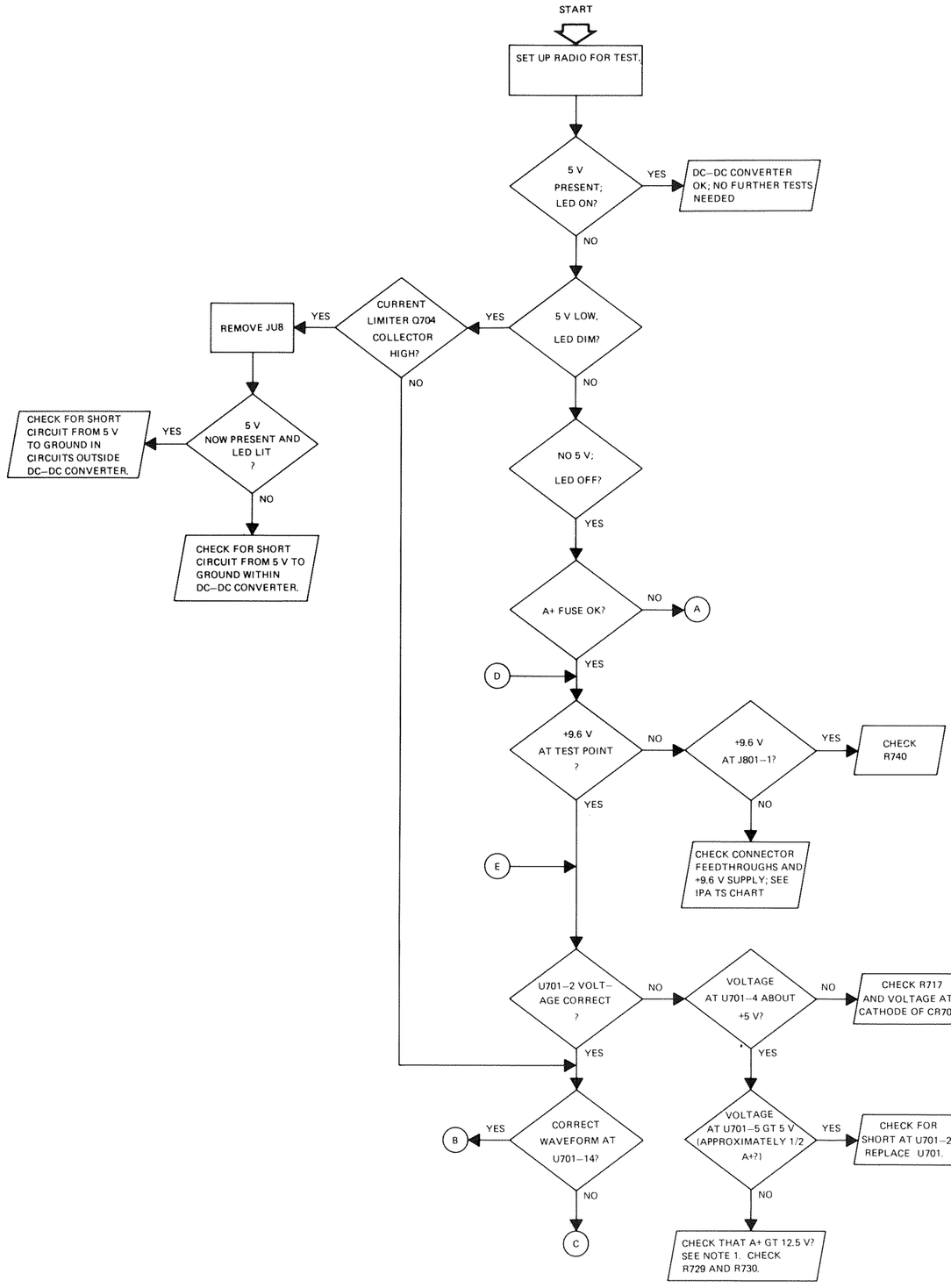
= SOURCE OF FAULT

U701–2	=	PIN NO. 2 OF U701	
J801–1	=	PIN NO. 1 OF J801	
GT	=	GREATER THAN	
LT	=	LESS THAN	
TS	=	TROUBLESHOOTING	
LED	=	GRN DS710 ON STATION CONTROL BOARD	

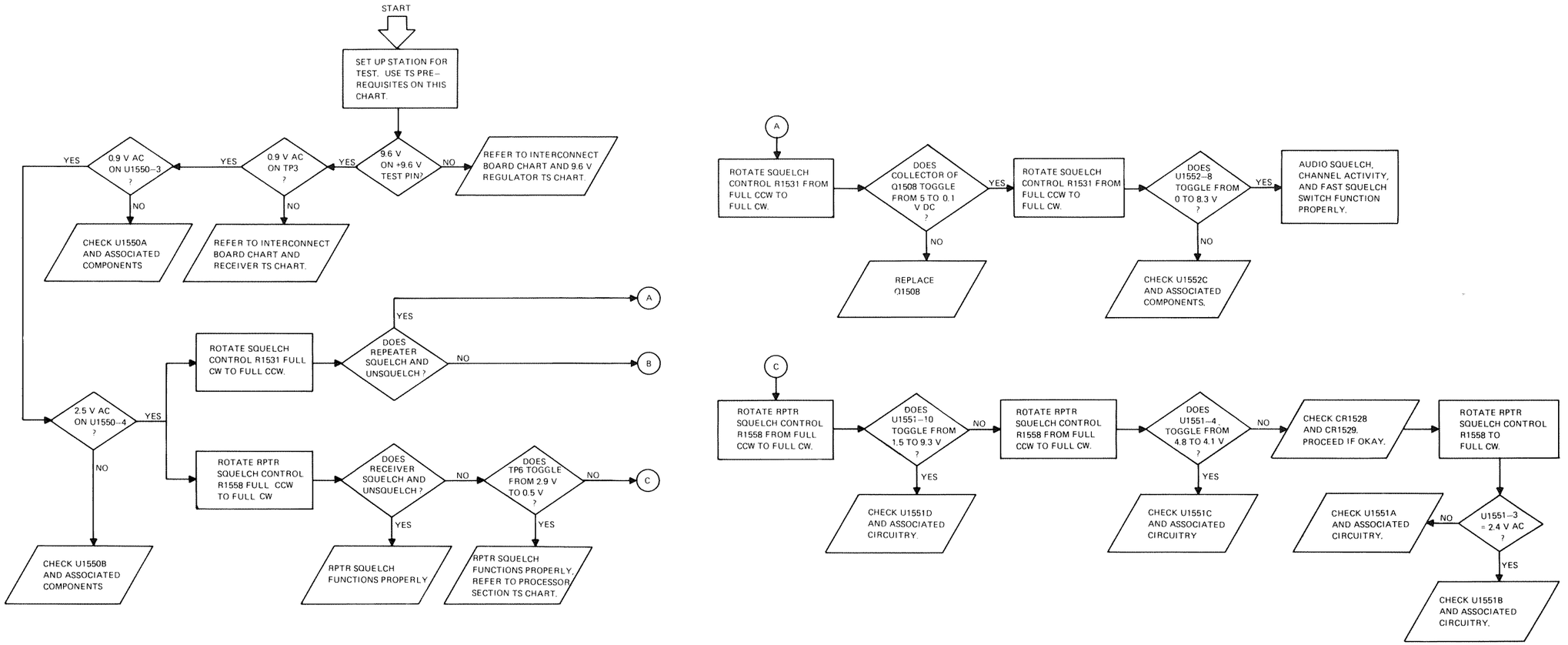
EEPS–35634–A

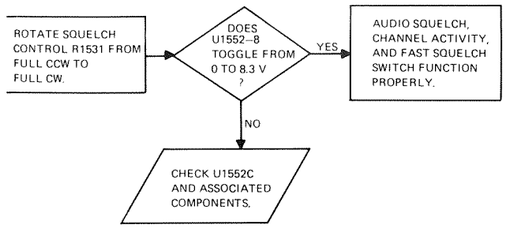
NOTES:

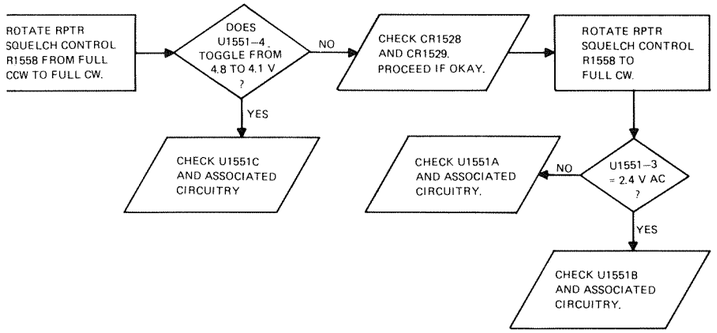
1. WHEN OPERATING FROM BATTERY–SUPPLIED POWER, A+ MAY BE LESS THAN 12.5 V AND SHUTDOWN COMPARATOR MAY HOLD DC–DC CONVERTER IN SHUTDOWN MODE (I.E. U701–2 IS LOW). IF THIS HAPPENS, MOMENTARILY PLACE ACC DIS/TEST SWITCH TO TEST POSITION. IF A+ SUPPLIED BY BATTERY IS LESS THAN 10.5 V, DC–DC CONVERTER WILL NOT ENERGIZE.
2. WHEN CHECKING DC LEVEL AT U701–9, OPERATION OF OSCILLATOR CIRCUIT IS ALWAYS DISTURBED. IGNORE ANYTHING ELSE THAT HAPPENS WHEN PROBING U701–9 SINCE DC LEVEL CAN BE RELIABLY CHECKED.
3. REFER TO SCHEMATIC DIAGRAMS IN THIS MANUAL FOR VARIOUS CIRCUITS REFERENCED IN CHART.

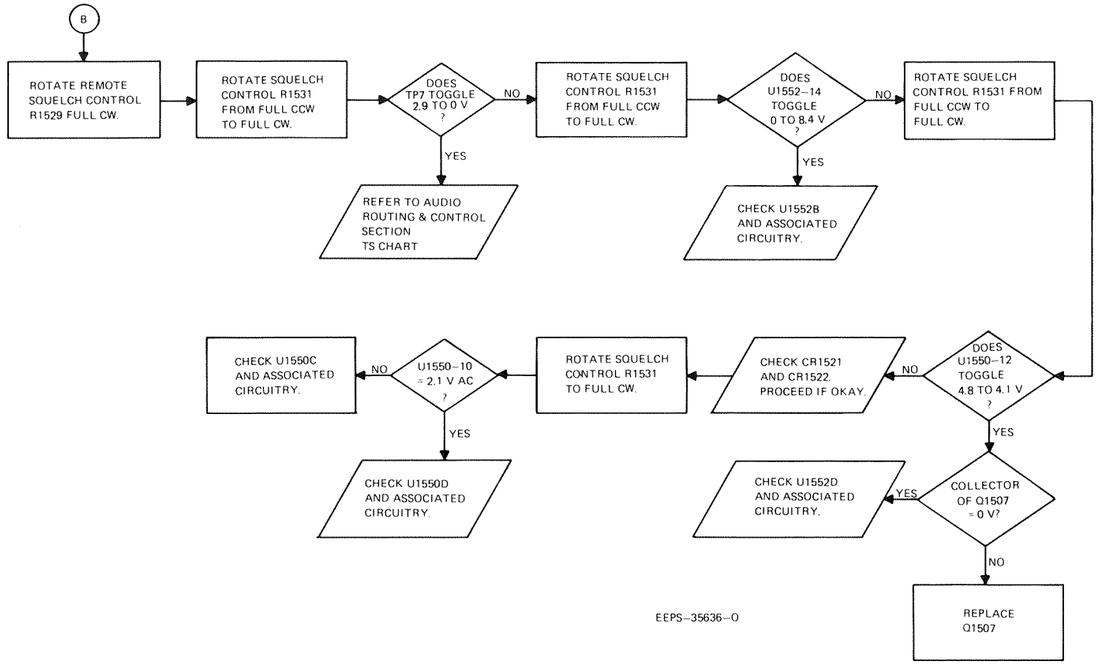

START
SET UP RADIO FOR TEST.
5 V PRESENT; LED ON?
YES
DC–DC CONVERTER OK; NO FURTHER TESTS NEEDED
NO
5 V LOW, LED DIM?
YES
CURRENT LIMITER Q704 COLLECTOR HIGH?
YES
REMOVE JU8
YES
5 V NOW PRESENT AND LED LIT ?
YES
CHECK FOR SHORT CIRCUIT FROM 5 V TO GROUND IN CIRCUITS OUTSIDE DC–DC CONVERTER.
NO
CHECK FOR SHORT CIRCUIT FROM 5 V TO GROUND WITHIN DC–DC CONVERTER.
NO
NO 5 V; LED OFF?
YES
A+ FUSE OK?
NO
A
YES
D
+9.6 V AT TEST POINT ?
NO
+9.6 V AT J801–1?
YES
CHECK R740
NO
CHECK CONNECTOR FEEDTHROUGHS AND +9.6 V SUPPLY; SEE IPA TS CHART
YES
E
U701–2 VOLTAGE CORRECT ?
NO
VOLTAGE AT U701–4 ABOUT +5 V?
NO
CHECK R717 AND VOLTAGE AT CATHODE OF CR709.
YES
YES
B
YES
CORRECT WAVEFORM AT U701–14?
NO
C
VOLTAGE AT U701–5 GT 5 V (APPROXIMATELY 1/2 A+?)
YES
CHECK FOR SHORT AT U701–2; REPLACE U701.
NO
CHECK THAT A+ GT 12.5 V? SEE NOTE 1. CHECK R729 AND R730.
B
IS WAVEFORM AT U701–13 CORRECT ?
YES
DOES Q701 AND Q702 TURN ON WHEN U701–13 IS LOW?
YES
CHECK DC CONTINUITY BETWEEN Q701–COLLECTOR AND JU8; CHECK FOR SHORT CIRCUIT TO GND AT JU8.
NO
CHECK VOLTAGES ON Q703 WHEN U701–13 IS LOW. CHECK R709 AND R708
NO
IS WAVEFORM AT U701–13 CHANGING STATE BUT NOT CORRECT ?
YES
CHECK R713, R715, AND C708
NO
IS WAVEFORM AT U701–13 ALWAYS LOW ?
YES
NO
IS WAVEFORM AT U701–13 LOW FOR VERY SHORT SPIKES ?
YES
NO
F
IS WAVEFORM AT U701–11 CORRECT ?
NO
IS WAVEFORM AT U701–11 ALWAYS HIGH ?
YES
CHECK CR705.
NO
CHECK R706 AND CR706
YES
IS WAVEFORM AT U701–10 CORRECT ?
YES
CHECK Q703 COLLECTOR HIGH DURING LOW PULSE AT U701–10. & CHECK Q703 AND Q702 EMITTERS.
NO
IS WAVEFORM AT U701–10 ALWAYS LOW ?
NO
CHECK CR703
YES
CHECK R711
A
AFTER REPLACING A+ FUSE, DOES IT BLOW ?
NO
IS LED LIT AND +5 V LEVEL CORRECT ?
YES
NO
D
YES
REMOVE JU8; THIS REMOVES DC LOAD AND DISABLES OVER–VOLTAGE SHUTDOWN CIRCUIT. REPLACE A+ FUSE.
DID FUSE BLOW ?
YES
CHECK FOR SHORT FROM A+ TO GND OR FROM EMITTER OR COLLECTOR OF Q701 TO GND.
NO
IS LED LIT AND +5 V LEVEL CORRECT ?
YES
CHECK FOR SHORT CIRCUIT F
TO GND IN AREA OUTSIDE DC
CONVERTER; AFTER CORREC
CHECK CURRENT LIMITER CI
THAT SEEMS TO HAVE FAILE
NO
IS OUTPUT VOLTAGE GT 6 V ?
NO
E
YES
IS WAVEFORM AT U701–13 CORRECT ?
YES
Q703 OFF WHEN U701–13 IS HIGH ?
YES
NO
CHECK BASE–TO–EMITTER VOLTAGE DROP OF Q703 WHEN U701–13 IS HIGH.
NO
IS WAVEFORM AT U701–13 ALWAYS LOW ?
NO
F
YES
IS WAVEFORM AT U701–11 CORRECT ?
YES
CHECK THAT U701–10 IS 5 V
IF TRUE, CHECK FOR SHORT
AT U701–13 OR REPLACE U70
IF NOT TRUE, CHECK V_E OR
WHY U701–10 IS BEING PULL
NO
IS WAVEFORM AT U701–11 ALWAYS LOW ?
YES
C
NO
CHECK R713, R715, AND C708

RECEIVER AUDIO AND SQUELCH CONTROL
TROUBLESHOOTING CHART









EEPS–35636–O

SYMBOLS AND ABBREVIATIONS USED IN THE CHART

ALL VOLTAGE MEASUREMENTS ARE DC, UNLESS OTHERWISE STATED. AC VOLTAGES ARE MEASURED WITH AN AVERAGE RESPONDING METER.

= TEST TO BE DONE

= DECISION

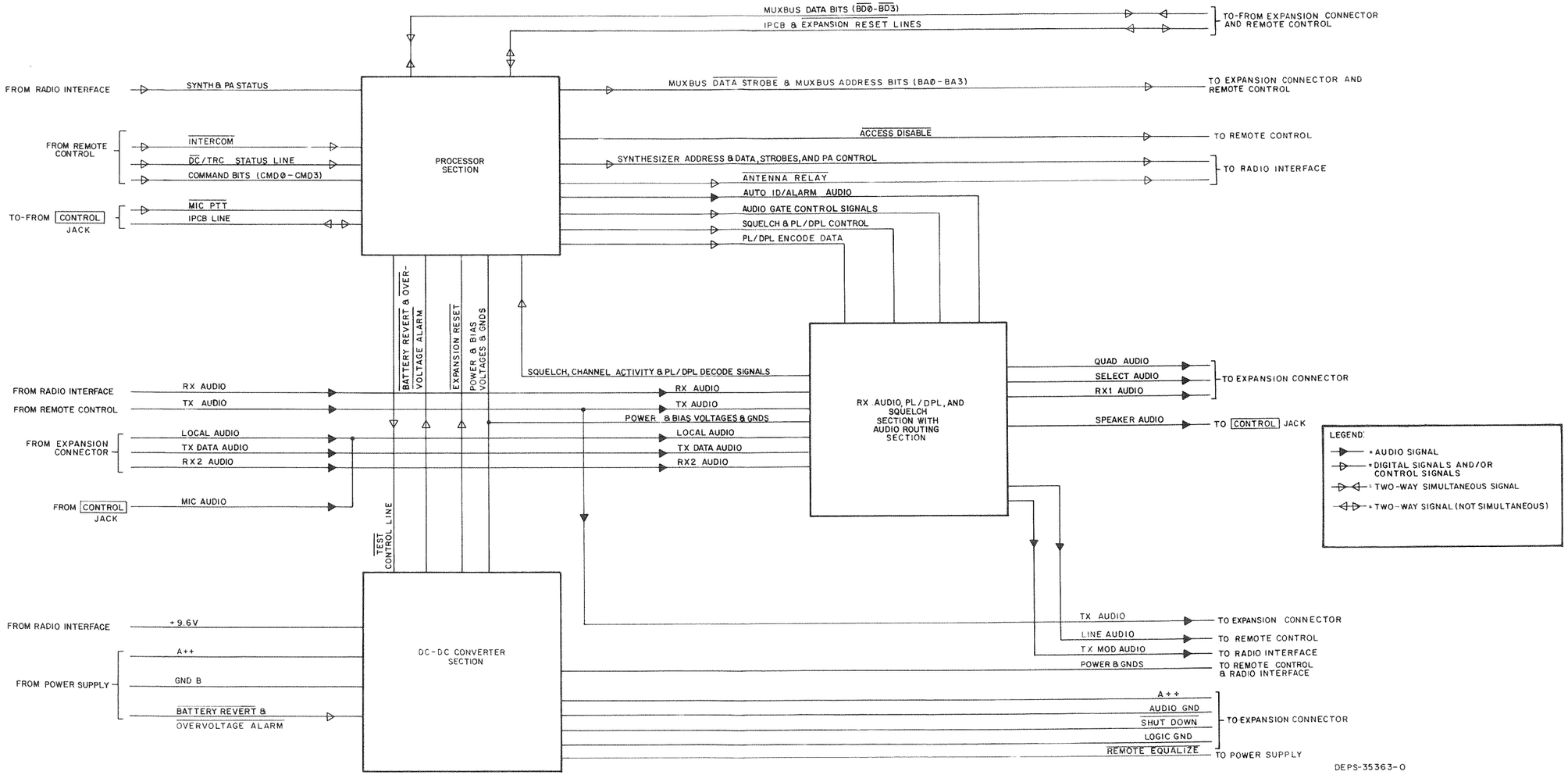
= SOURCE OF FAULT

TS	= TROUBLESHOOTING
U1550–3	= PIN 3 OF U1550
CW	= CLOCKWISE
CCW	= COUNTERCLOCKWISE

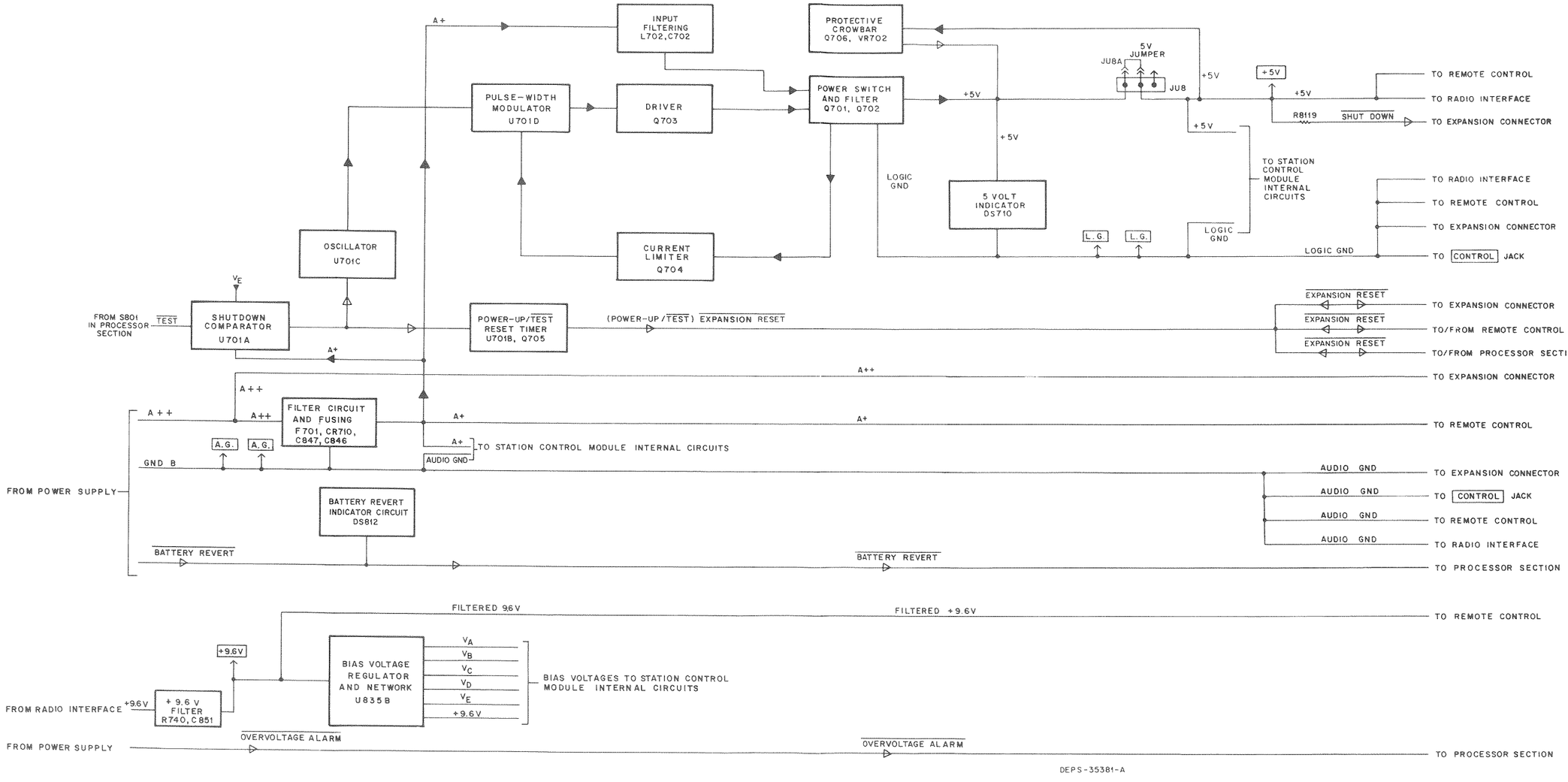
TROUBLESHOOTING PREREQUISITES:

1. ENERGIZE STATION. RECEIVE SYNTHESIZER MUST BE LOCKED (RX LOCK LED LIT). IF NOT, PERFORM RECEIVER TROUBLESHOOTING PROCEDURE.
2. PL DISABLE STATION BY PUTTING S802 IN THE PL DIS POSITION (UP).
3. ACCESS DISABLE STATION BY PUTTING S801 IN THE "ACC DIS" POSITION. (UP).
4. PROVIDE A MEANS OF LISTENING TO LOCAL AUDIO. PLUG PORTABLE TEST SET INTO J812.
5. THERE SHOULD BE NO RF SIGNAL PRESENT AT THE RECEIVER INPUT J11 (DISCONNECT ANTENNA).
6. WHEN TROUBLESHOOTING IS COMPLETE, READJUST THE AUDIO AND REPEATER SQUELCH SECTION TO PROPER SYSTEM SPECIFICATIONS.

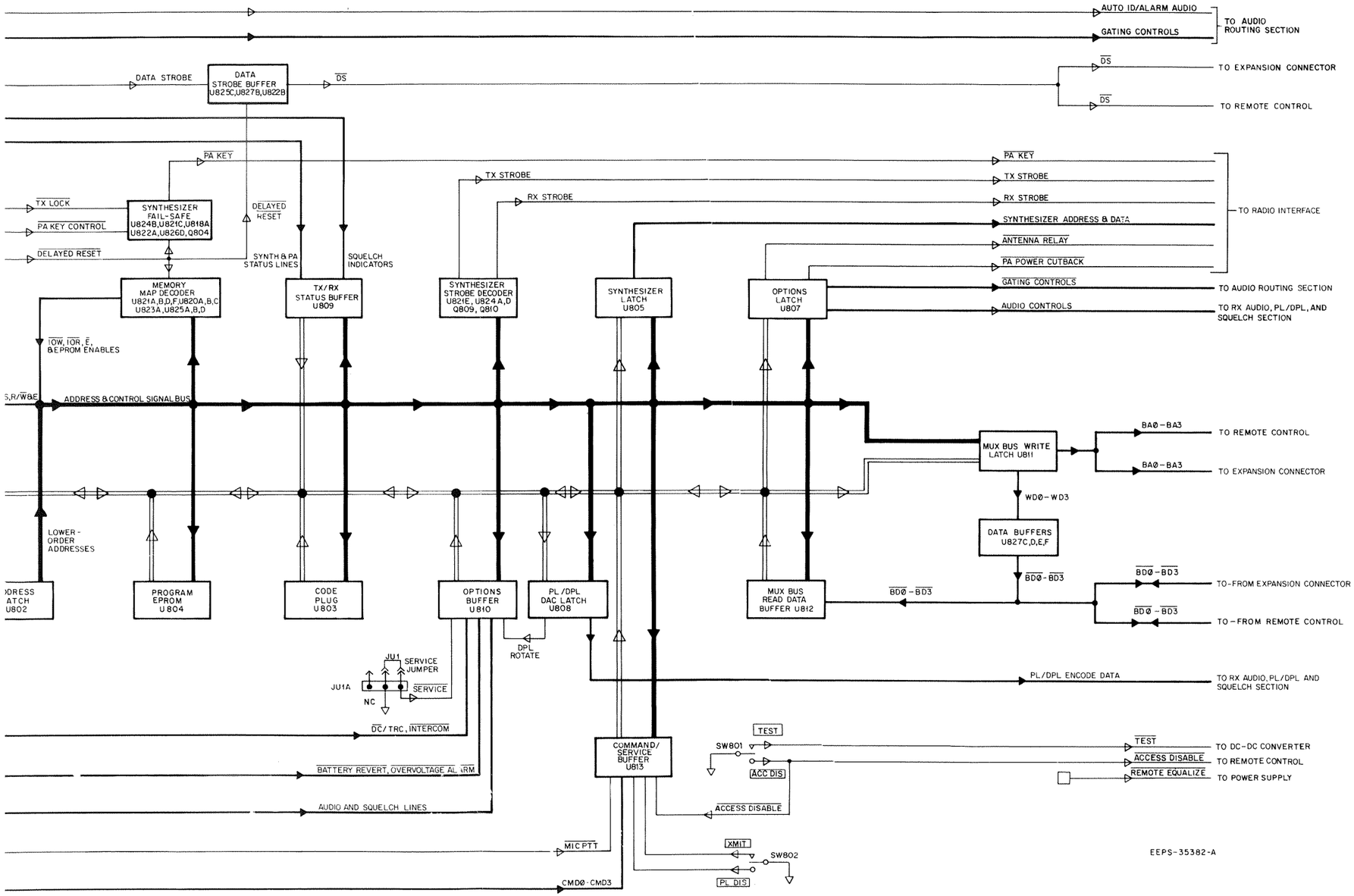
STATION CONTROL BOARD
OVERALL BLOCK DIAGRAM



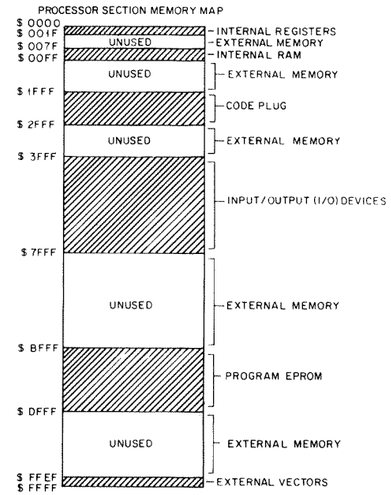
DC-DC CONVERTER
BLOCK DIAGRAM



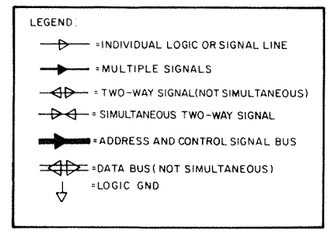
MICROPROCESSOR
BLOCK DIAGRAM

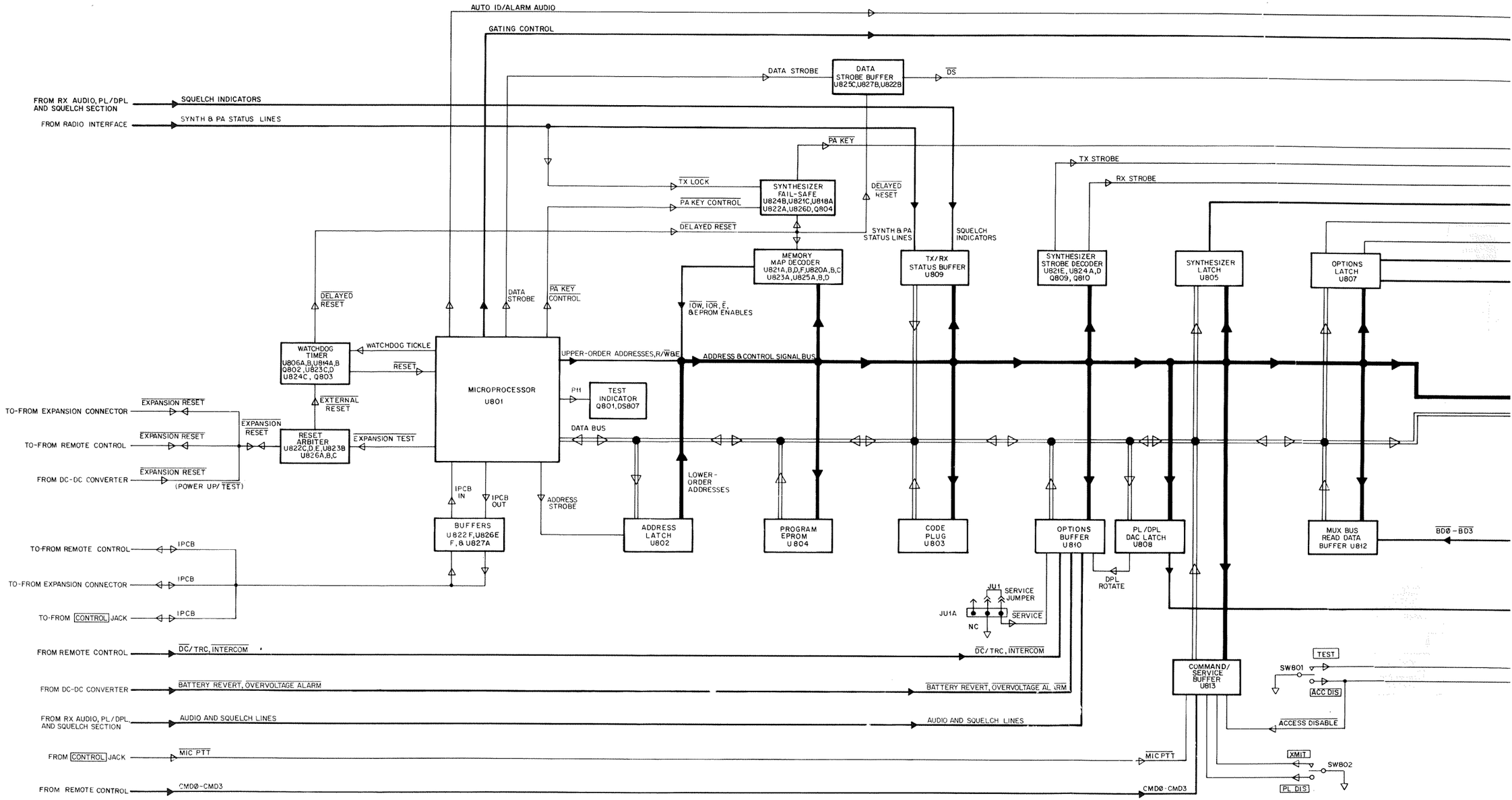


PROCESSOR SECTION MEMORY MAP

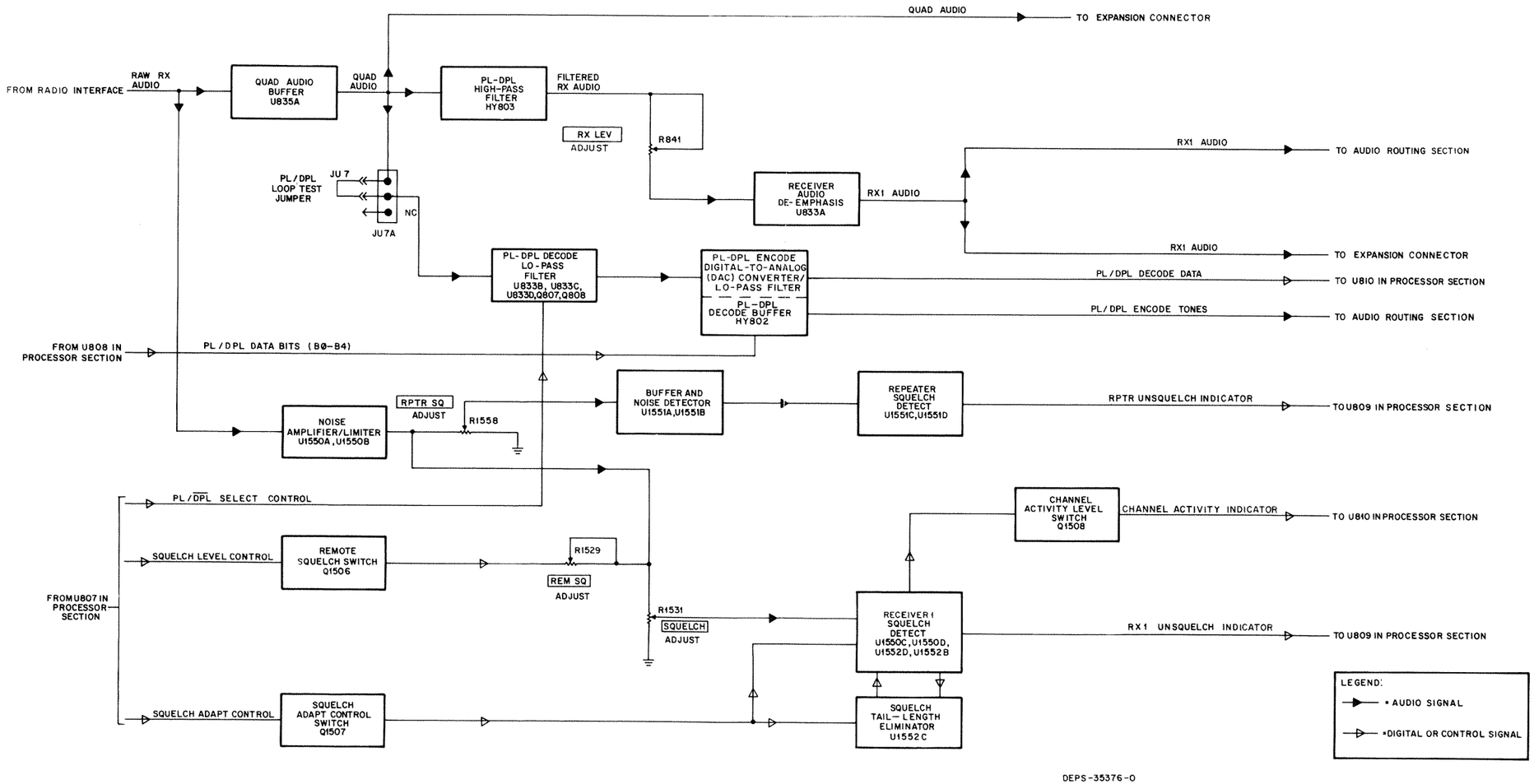


LEGEND



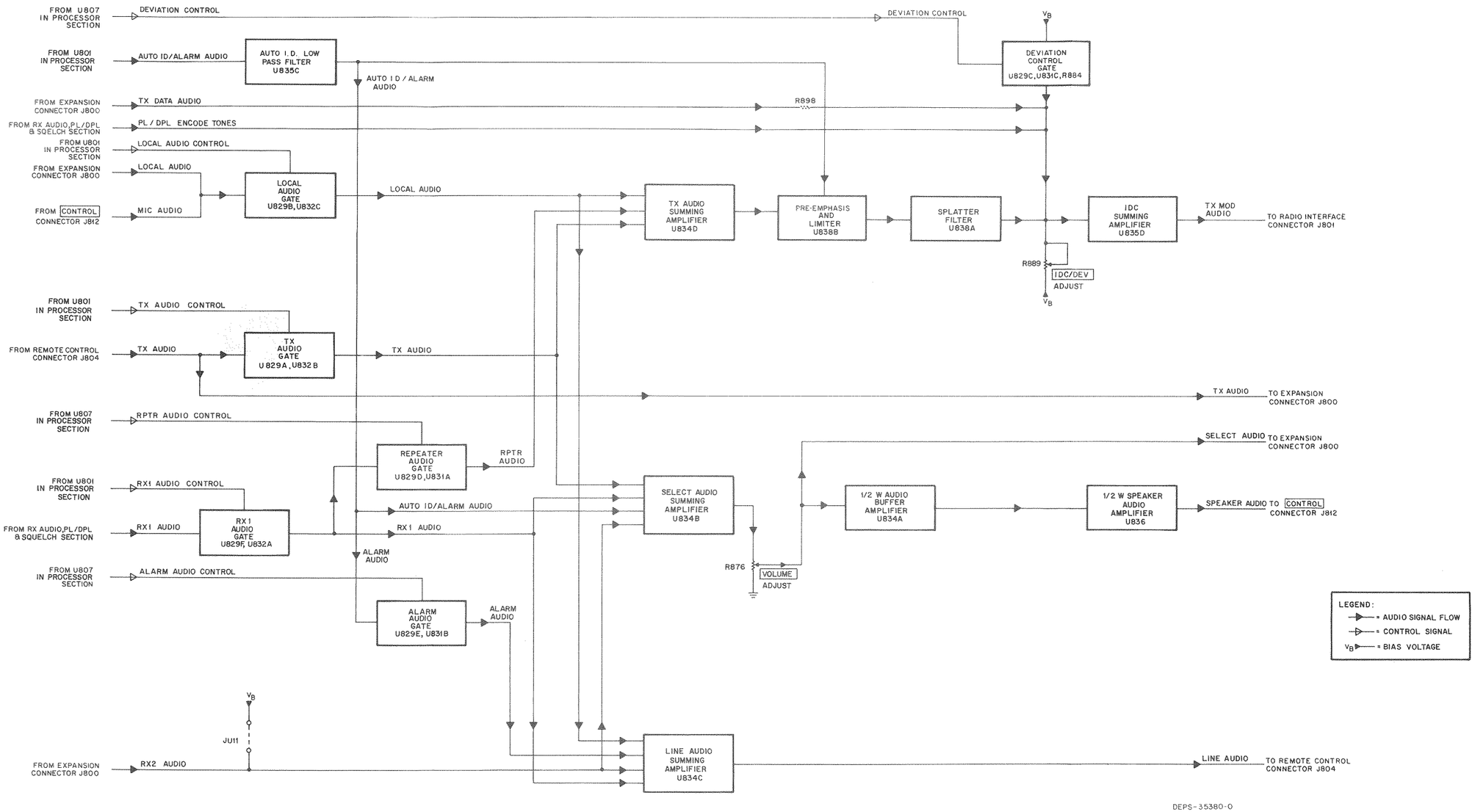

AUTO ID/ALARM AUDIO
GATING CONTROL
DATA STROBE
DATA STROBE BUFFER U825C,U827B,U822B
DS
FROM RX AUDIO, PL/DPL AND SQUELCH SECTION
SQUELCH INDICATORS
FROM RADIO INTERFACE
SYNTH & PA STATUS LINES
PA KEY
TX STROBE
RX STROBE
TX LOCK
PA KEY CONTROL
DELAYED RESET
SYNTHESIZER FAIL-SAFE U824B,U821C,U818A U822A,U826D,Q804
DELAYED RESET
SYNTH & PA STATUS LINES
SQUELCH INDICATORS
MEMORY MAP DECODER U821A,B,D,F,U820A,B,C U823A,U825A,B,D
TX/RX STATUS BUFFER U809
SYNTHESIZER STROBE DECODER U821E, U824A,D Q809, Q810
SYNTHESIZER LATCH U805
OPTIONS LATCH U807
DELAYED RESET
DATA STROBE
PA KEY CONTROL
IOW, IOR, E, & E PROM ENABLES
WATCHDOG TIMER U806A,B,U814A,B Q802, U823C,D U824C, Q803
WATCHDOG TICKLE
RESET
MICROPROCESSOR U801
UPPER-ORDER ADDRESSES, R/WBE
ADDRESS & CONTROL SIGNAL BUS
P11
TEST INDICATOR Q801, DS807
DATA BUS
EXTERNAL RESET
TO-FROM EXPANSION CONNECTOR
EXPANSION RESET
TO-FROM REMOTE CONTROL
EXPANSION RESET
FROM DC-DC CONVERTER
EXPANSION RESET
(POWER UP/TEST)
EXPANSION RESET
RESET ARBITER U822C,D,E, U823B U826A,B,C
EXPANSION TEST
IPCB IN
IPCB OUT
ADDRESS STROBE
LOWER-ORDER ADDRESSES
BUFFERS U822F,U826E F,& U827A
ADDRESS LATCH U802
PROGRAM EPROM U804
CODE PLUG U803
OPTIONS BUFFER U810
PL/DPL DAC LATCH U808
MUX BUS READ DATA BUFFER U812
BD0 - BD3
TO-FROM REMOTE CONTROL
IPCB
TO-FROM EXPANSION CONNECTOR
IPCB
TO-FROM CONTROL JACK
IPCB
JU1 SERVICE JUMPER
JU1A
SERVICE
NC
DPL ROTATE
FROM REMOTE CONTROL
DC/TRC, INTERCOM
DC/TRC, INTERCOM
FROM DC-DC CONVERTER
BATTERY REVERT, OVERVOLTAGE ALARM
BATTERY REVERT, OVERVOLTAGE ALARM
FROM RX AUDIO, PL/DPL AND SQUELCH SECTION
AUDIO AND SQUELCH LINES
AUDIO AND SQUELCH LINES
COMMAND/ SERVICE BUFFER U813
TEST
SW801
ACC DIS
ACCESS DISABLE
FROM CONTROL JACK
MIC PTT
MIC PTT
XMIT
SW802
PL DIS
FROM REMOTE CONTROL
CMD0-CMD3
CMD0-CMD3

RECEIVER AUDIO AND SQUELCH CONTROL
BLOCK DIAGRAM



DEPS-35376-O

AUDIO ROUTING AND CONTROL
BLOCK DIAGRAM



TLN2423A STATION CONTROL MODULE

CIRCUIT BOARD DETAILS

SHOWN FROM COMPONENT SIDE

COMPONENT SIDE - BD-EEPS-37438-A
SOLDER SIDE - BD-EEPS-37439-A
OL-EEPS-37440-B

J812

AUDIO GND	5	6	LOGIC GND
MIC PTT	3	4	MIC AUDIO
IPCB	1	2	SPEAKER AUDIO

J800

QUAD AUDIO	39	40	AUDIO REF
AUDIO REF	37	38	RX1 AUDIO
RX2 AUDIO	35	36	TX AUDIO
LOCAL AUDIO	33	34	TX DATA AUDIO
AUDIO SPARE	31	32	SELECT AUDIO
AUDIO SPARE	29	30	AUDIO SPARE
LOGIC SPARE	27	28	AUDIO SPARE
LOGIC SPARE	25	26	LOGIC SPARE
SHUTDOWN	23	24	LOGIC SPARE
LOGIC GND	21	22	DS
BD2	19	20	BD3
BD0	17	18	BD1
BA2	15	16	BA3
BA0	13	14	BA1
IPCB	11	12	RESET
AUDIO GND	9	10	AUDIO GND
AUDIO GND	7	8	AUDIO GND
A++	5	6	AUDIO GND
A++	3	4	A++
A++	1	2	A++

J804

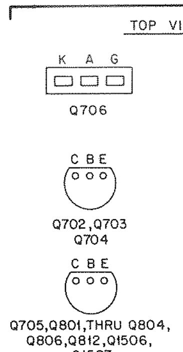
LOGIC GND	26	25	+5V
BA0	24	23	BA1
BA2	22	21	BA3
BD0	20	19	BD1
BD2	18	17	BD3
DS	16	15	RESET
IPCB	14	13	LOGIC SPARE
INTERCOM	12	11	DC/TRC
ACCESS DISABLE	10	9	CMD0
CMD1	8	7	CMD2
CMD3	6	5	TX AUDIO
LINE AUDIO	4	3	+9.6V
AUDIO GND	2	1	A+

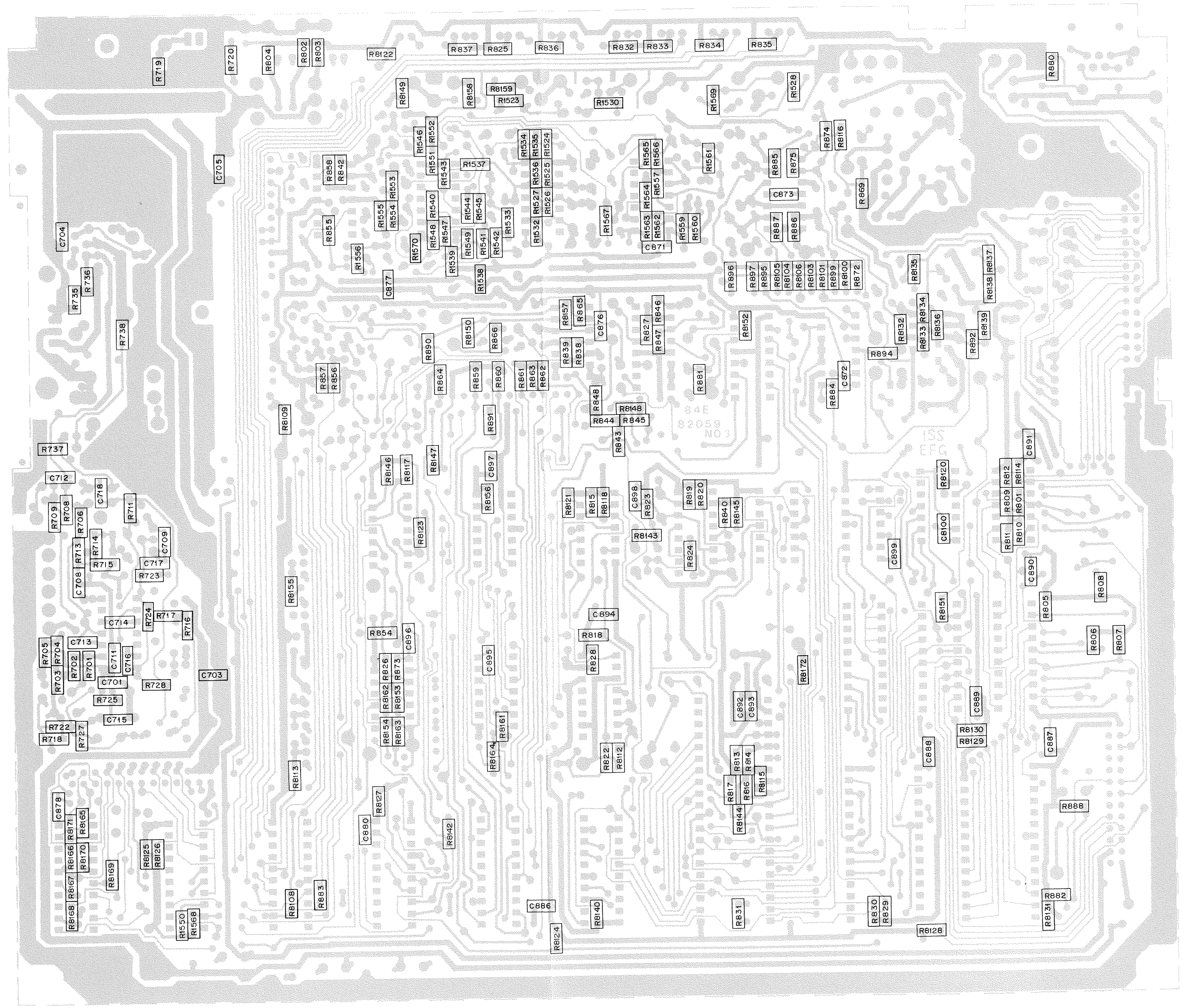
J801

TX STROBE	26	25	RX STROBE
SA0	24	23	SD3
SA1	22	21	SD2
SA2	20	19	SD1
TX LOOP	18	17	SD0
PA POWER CUTBACK	16	15	RX LOCK
PA KEY	14	13	RX LOOP
PA ON	12	11	LOGIC GND
PA FULL POWER	10	9	+5V
TX LOCK	8	7	ANTENNA RELAY
AUDIO GND	6	5	RX AUDIO
AUDIO GND	4	3	TX MOD AUDIO
AUDIO GND	2	1	+9.6V

BASE DETAILS

TOP VIEWS

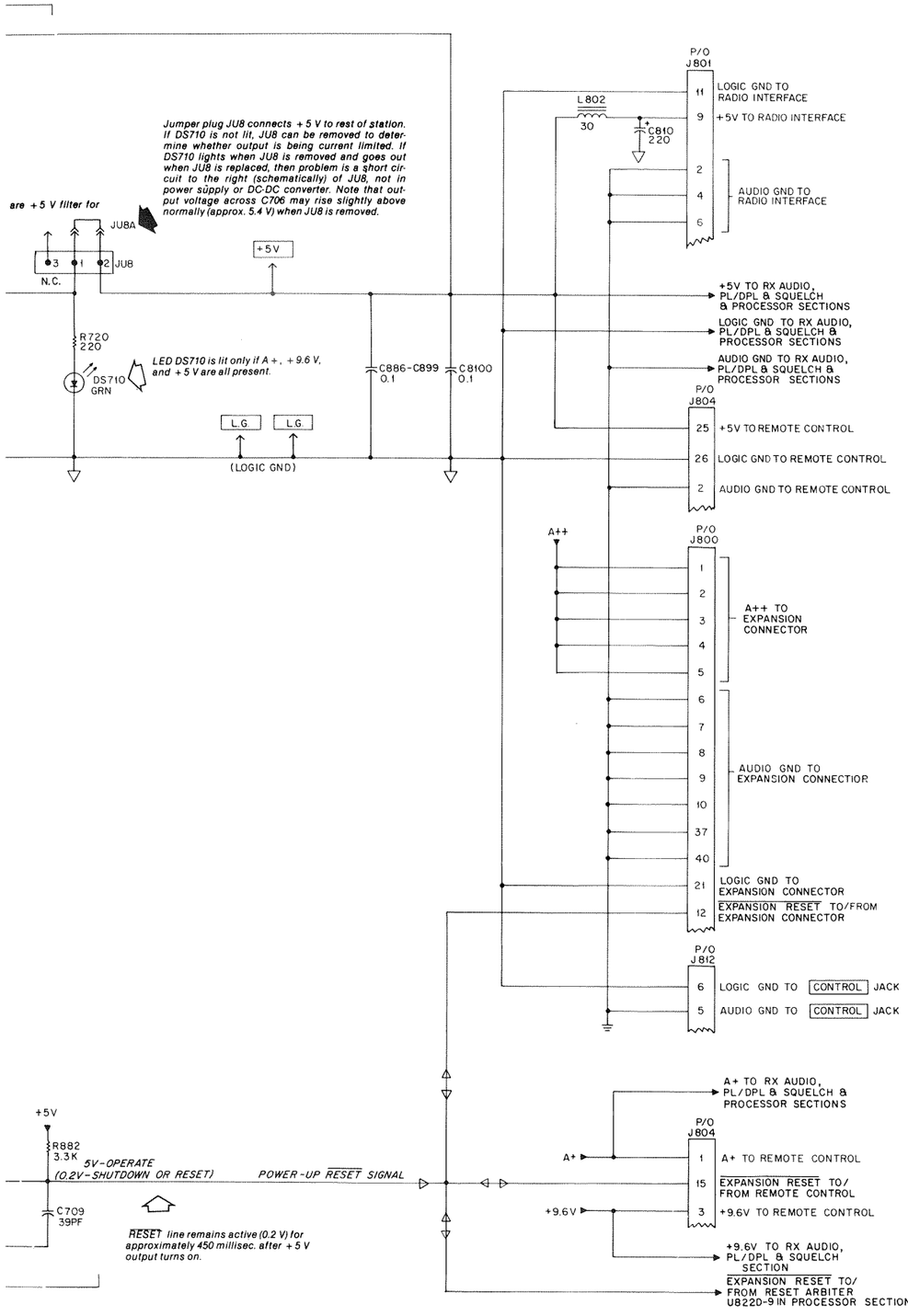


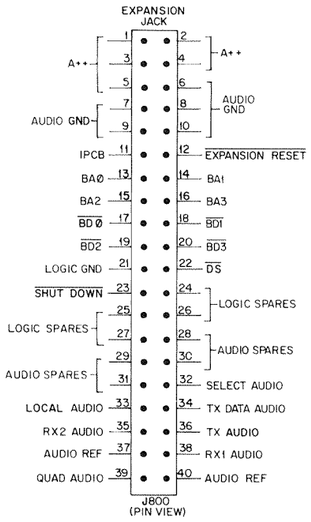


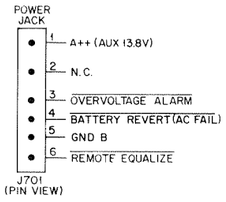
SOLDER SIDE BD-EEPS-37444-A
OL-EEPS-37445-A

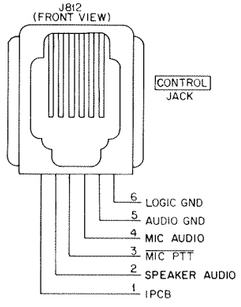
SHOWN FROM SOLDER SIDE

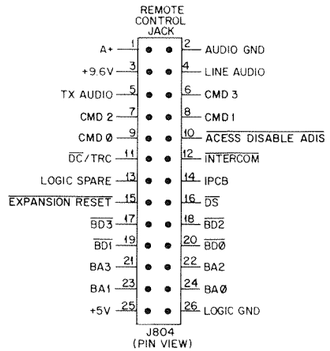
DC-DC CONVERTER
SCHEMATIC DIAGRAM

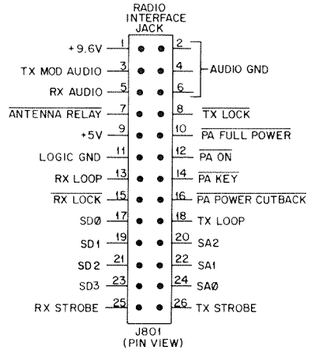


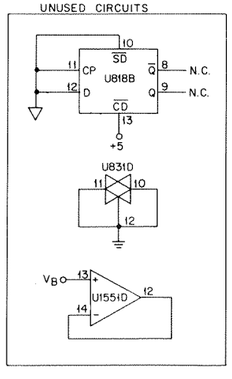












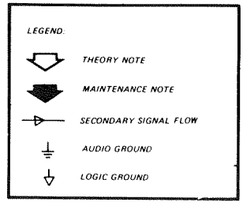
EEPS-35047-A

NOTES:

1. Unless otherwise specified, all resistor values are in ohms and all inductor values are in microhenries, and all capacitor values are in microfarads.
2. Voltage measurements must be performed with a high-impedance meter (at least 10 megohm/volt or greater for increased accuracy).

Station Control Board Integrated Circuit Data Chart

Ref. Designation	+5 V (Pin)	+9.6 V (Pin)	Logic Gnd (Pin)	Audio Gnd (Pin)	N.C. (Pin)	Description
U701	A+ on Pin 3		—	12	—	Open Collector Output Quad Comparator
U702 thru 800	—	—	—	—	—	Not Used
U801	7, 21	—	1	—	—	Microprocessor
U802	20	—	10	—	—	Octal Tri-State Latch
U803	28	—	12	—	—	4k x 8 EPROM
U804	1, 28	—	14	—	—	8k x 8 EPROM
U805	20	—	10	—	—	Octal Latch
U806	16, 2, 3, 10	—	8, 6, 14	—	12, 13	Dual Monostable
U807, 808	20	—	10	—	—	Octal Latch
U809, 810	20	—	10	—	—	Octal Buffer
U811	20	—	10	—	—	Octal Latch
U812, 813	20	—	10	—	2-5	Octal Buffer
U814	16, 2, 11	—	8, 6, 14	—	—	Dual Monostable
U815, 816, 817	—	—	—	—	—	Not Used
U818	14, 1, 13	—	7, 2, 10-12	—	6, 8, 9	Dual D Flip-Flop
U819	—	—	—	—	—	Not Used
U820	14	—	7	—	—	Triple 3-Input NAND
U821, 822	14	—	7	—	—	Hex Inverter
U823	14	—	7	—	—	Quad NAND
U824, 825	14	—	7	—	—	Quad AND
U826, 827	14	—	7	—	—	Open Collector Output Hex Inverter
U828	—	—	—	—	—	Not Used
U829	1, 13	16	8	—	—	Hex Level Shifter
U830	—	—	—	—	—	Not Used
U831	—	14	—	7, 10-12	—	Quad Analog Switch
U832	—	16	—	6-8	—	Triple 2-Channel Mux Switch
U833, 834, 835	—	4	—	11	—	Quad Op Amp
U836	—	—	—	3	—	1/2 W Audio Amp
U837	—	—	—	—	—	Not Used
U838	—	—	—	4	—	Dual Op Amp
U839 thru 1549	—	—	—	—	—	Not Used
U1550, 1551	—	11	—	7	—	Quad Op Amp
U1552	—	4	—	11	—	Quad Op Amp



PARTS INFORMATION IS LOCATED AT THE END OF THIS SECTION

DC-DC CONVERTER

Driver Q702 and power transistor Q701 comprise the +5 V power switch.

Current limiter Q704 turns on when current in R731-R734 increases sufficiently, forcing U701D to turn off power switch by pulling U701D-11 high.

VR702 6V

Q706

R719 24

C703 0.1

A+

L702

C702 660

C704 0.1

Q701 M9829

R734 1

R733 1

R732 1

R731 1

R738 47

Q704 M9643

R737 820

POWER TRANSISTOR OUTPUT COLLECTOR OF Q701 A+ = 14V, V9.6 = 9.4V 10 US/DIV., 5V/DIV

15V 10V 5V 0V

24US 19US

R735 100

R736 390

Q702 M9328

L701

C705 0.1

R721 2.7

L703

CR702

Noise suppression is provided by CR702, L703, AND R721.

CR701

CR701 conducts after Q701-Q702 turn off, maintaining L701 current and clamping Q701-Q702 collectors to within approximately 1 V of ground.

Components C705, C706, L701 are +5 V filter for Q701-Q702 squarewave output.

Jumper plug JU8 connects +5 V to rest of station. If DS710 is not lit, JU8 can be removed to determine whether output is being current limited. If DS710 lights when JU8 is removed and goes out when JU8 is replaced, then problem is a short circuit to the right (schematically) of JU8, not in power supply or DC-DC converter. Note that output voltage across C706 may rise slightly above normally (approx. 5.4 V) when JU8 is removed.

JU8A

JU8

3 1 2

N.C.

+5V

C706 1000

R720 220

DS710 GRN

LED DS710 is lit only if A+, +9.6 V, and +5 V are all present.

C886-C899 0.1

C8100 0.1

L.G. L.G.

(LOGIC GND)

P/O J801

11 LOGIC GND TO RADIO INTERFACE

9 +5V TO RADIO INTERFACE

2 4 6 AUDIO GND TO RADIO INTERFACE

L802 30

C810 220

+5V TO RX AUDIO, PL/DPL & SQUELCH & PROCESSOR SECTIONS

LOGIC GND TO RX AUDIO, PL/DPL & SQUELCH & PROCESSOR SECTIONS

AUDIO GND TO RX AUDIO, PL/DPL & SQUELCH & PROCESSOR SECTIONS

P/O J804

25 +5V TO REMOTE CONTROL

26 LOGIC GND TO REMOTE CONTROL

2 AUDIO GND TO REMOTE CONTROL

A++

P/O J800

1 2 3 4 5 A++ TO EXPANSION CONNECTOR

6 7 8 9 10 37 40 AUDIO GND TO EXPANSION CONNECTIOR

21 LOGIC GND TO EXPANSION CONNECTOR

12 EXPANSION RESET TO/FROM EXPANSION CONNECTOR

P/O J812

6 LOGIC GND TO CONTROL JACK

5 AUDIO GND TO CONTROL JACK

+9.6V

R703 12K

R702 56K

R704 22K

OSCILLATOR OUTPUT PIN 14 OF U701C A+ = 14V, V9.6 = 9.4V 10US/DIV., 2V/DIV.

8V 6V 4V 2V GND (0V) REF

43US 43US

CR705

R706 3.9K

CR707

CR706

C718 39PF

V_E

R701 180K

U701C

drops to 0.3 V for 1.2 VM comparator U701D. s high impedance state. I701C-14 voltage to rise ximately 43 microsec.

R705 2.7K

C711 39PF

C701 .001

CR704

PWM COMPARATOR(-) INPUT PIN 10 OF U701D A+ = 14V, V9.6 = 9.4V 10 US/DIV., 1V/DIV.

6V 5V 4V 3V 2V 1V 0V

18US 25US

C713 39PF

Q703 M9643

C712 39PF

R708 620

R710 330

R709 3.3K

R714 120K

CR703

U701D

Pulse width modulator (PWM) comparator U701D controls power switching through driver Q703 to produce +5 V ±5% output at JU8A-2.

R718 3.9K

R722 10K

R713 8.2K

R715 2.7K

C708 .01

PWM COMPARATOR (+) INPUT PIN 11 OF U701D A+ = 14V, V9.6 = 9.4V 10US/DIV., 1V/DIV.

5V 4V 3V 2V 1V 0V

18US 25US

PWM COMPARATOR OUTPUT PIN 13 OF U701D A+ = 14V, V9.6 = 9.4V 10US/DIV., 5V/DIV.

20V 15V 10V 5V 0V

25US 18US

R725 1M

C715 39PF

R730 2.1K

R717 100

C714 39PF

U701A

7.26V-OPERATE (0.1V-SHUTDOWN)

R729 1.91K

R716 560

R707 8.2K

CR708

CR709

R727 390

C710 0.22

Capacitor C710 begins charging when shutdown comparator U701A-2 goes high. When voltage on C710 reaches (+) input voltage on U701B-7, U701B-1 goes low, pulling down Q705 base voltage to turn it off and allow RESET line to go high (operate).

C716 39PF

R728 3.9K

U701B

0.1V-OPERATE (0.7V-SHUTDOWN)

R724 22K

+9.6V

R723 8.2K

C717 39PF

Q705 M9528

+5V

R882 3.3K

C709 39PF

5V-OPERATE (0.2V-SHUTDOWN OR RESET)

POWER-UP RESET SIGNAL

RESET line remains active (0.2 V) for approximately 450 millisec. after +5 V output turns on.

A+ TO RX AUDIO, PL/DPL & SQUELCH & PROCESSOR SECTIONS

P/O J804

A+ 1 A+ TO REMOTE CONTROL

15 EXPANSION RESET TO/FROM REMOTE CONTROL

+9.6V 3 +9.6V TO REMOTE CONTROL

+9.6V TO RX AUDIO, PL/DPL & SQUELCH SECTION

EXPANSION RESET TO/FROM RESET ARBITER U822D-9 IN PROCESSOR SECTION

RESET TIMER

DC-DC CONVERTER

BIAS GENERATOR

5.1V → V_A

4.8V → V_C

4.1V → V_D

BIAS VOLTAGES TO RX AUDIO, PL/DPL & SQUELCH SECTION

+9.6V

R1538 3.3K

R1539 180

R1541 39

C1563 10

C1550 10

R1542 2.7K

P/O J801

+9.6V — 1 — R740 2.7

R838 10K

C869 100PF

U835B (6, 5, 7)

4.8V → V_B

R839 10K

C829 10

C830 1

R739 220 — 5.1V → V_E

C851 100

C871–C873 0.1

C876 0.1

C877 0.1

VR701 5.1V

Protective crowbar circuit formed by Q706, R719, and VR702 blows A+ fuse F701 if 5 V rises above approx. 6.3 V due to failure of DC-DC Converter.

VR702 6V

R719 24

Q706

Driver Q702 and power transistor Q701 comprise the +5 V power switch.

A+

C703 0.1

L702

R734 1

R733 1

R732 1

R731 1

Q704 M9643

R737 820

R738 47

Q701 M9829

Current limiter Q704 turns on when current in R731-R734 increases sufficiently, forcing U701D to turn off power switch by pulling U701D-11 high.

C702 660

C704 0.1

R735 100

POWER TRANSISTOR OUTPUT
COLLECTOR OF Q701
A+ = 14V, V9.6 = 9.4V
10US/DIV., 5V/DIV

15V 10V 5V 0V

24US 19US

R736 390

Q702 M9328

L701

C705 0.1

R721 2.7

CR702

L703

Noise suppression is provided by CR702, L703, AND R721.

CR701

CR701 conducts after Q701-Q702 turn off, maintaining L701 current and clamping Q701-Q702 collectors to within approximately 1 V of ground.

Components C705, C706, L701, Q701-Q702 squarewave output.

C706 1000

+9.6V

R703 12K

R702 56K

R704 22K

OSCILLATOR OUTPUT
PIN 14 OF U701C
A+ = 14V, V9.6 = 9.4V
10US/DIV., 2V/DIV.

8V 6V 4V 2V GND (0V) REF

43US 43US

CR705

R706 3.9K

CR707

CR706

C718 39PF

V_E

R701 180K

U701C (9, 8, 14)

Oscillator U701C output drops to 0.3 V for 1.2 microsec. to trigger PWM comparator U701D. When U701C-14 goes to its high impedance state, it allows the voltage at U701C-14 voltage to rise and charge C701 for approximately 43 microsec.

C711 39PF

C701 .001

R705 2.7K

CR704

Q703 M9643

PWM COMPARATOR(-) INPUT
PIN 10 OF U701D
A+ = 14V, V9.6 = 9.4V
10US/DIV., 1V/DIV.

6V 5V 4V 3V 2V 1V 0V

18US 25US

R711 1.8K

C712 39PF

R708 620

R710 330

CR703

R709 3.3K

C713 39PF

U701D (10, 11, 13)

R714 120K

+9.6V — R718 3.9K

R722 10K

Pulse width modulator (PWM) comparator U701D controls power switching through driver Q703 to produce +5 V ± 5% output at JU8A-2.

Divider network R729 and R730 uses A+ to provide comparison voltage against V_E (5.1 V) reference voltage. When A+ rises above 12 V threshold, U701A-2 goes high and allows station to operate. If A+ then falls below 10.3 V, U701A-2 goes low, turning off 5 V DC-DC converter, shutting down station, and resetting U701B (reset timer). Note that momentarily depressing test switch SW801 allows station power-up without first reaching 12 V threshold, by temporarily lowering reference voltage at U701A-4 (useful for operating from 12 V battery power).

A+ V_E

R717 100

R730 2.1K

C714 39PF

U701A (4, 5, 3, 2, 12)

7.26V-OPERATE (0.1V-SHUTDOWN)

R729 1.91K

R716 560

R707 8.2K

CR708

CR709

R727 390

C710 0.22

Capacitor C710 begins charging when shutdown comparator U701A-2 goes high. When voltage on C710 reaches (+) input voltage on U701B-7, U701B-1 goes low, pulling down Q705 base voltage to turn it off and allow RESET line to go high (operate).

PWM COMPARATOR (+) INPUT
PIN 11 OF U701D
A+ = 14V, V9.6 = 9.4V
10US/DIV., 1V/DIV.

5V 4V 3V 2V 1V 0V

18US 25US

PWM COMPARATOR OUTPUT
PIN 13 OF U701D
A+ = 14V, V9.6 = 9.4V
10US/DIV., 5V/DIV.

20V 15V 10V 5V 0V

25US 18US

R713 8.2K

C708 .01

R715 2.7K

R725 1M

C715 39PF

+9.6V

R723 8.2K

Q705 M9528

C716 39PF

U701B (6, 7, 1)

0.1V-OPERATE (0.7V-SHUTDOWN)

V_E — R728 3.9K

R724 22K

C717 39PF

SHUTDOWN COMPARATOR

P/O J701

A++ TO EXPANSION CONNECTOR

CR710 provides reverse polarity protection for A+ using circuits.

AUX 13.8V — 1 — (A++) — 10A — F701 3A — A+

A.G. A.G. (AUDIO GND)

C847 .01

C846 10

CR710

GND B — 5

OVERVOLTAGE ALARM — 3 → TO U810-8 IN PROCESSOR SECTION

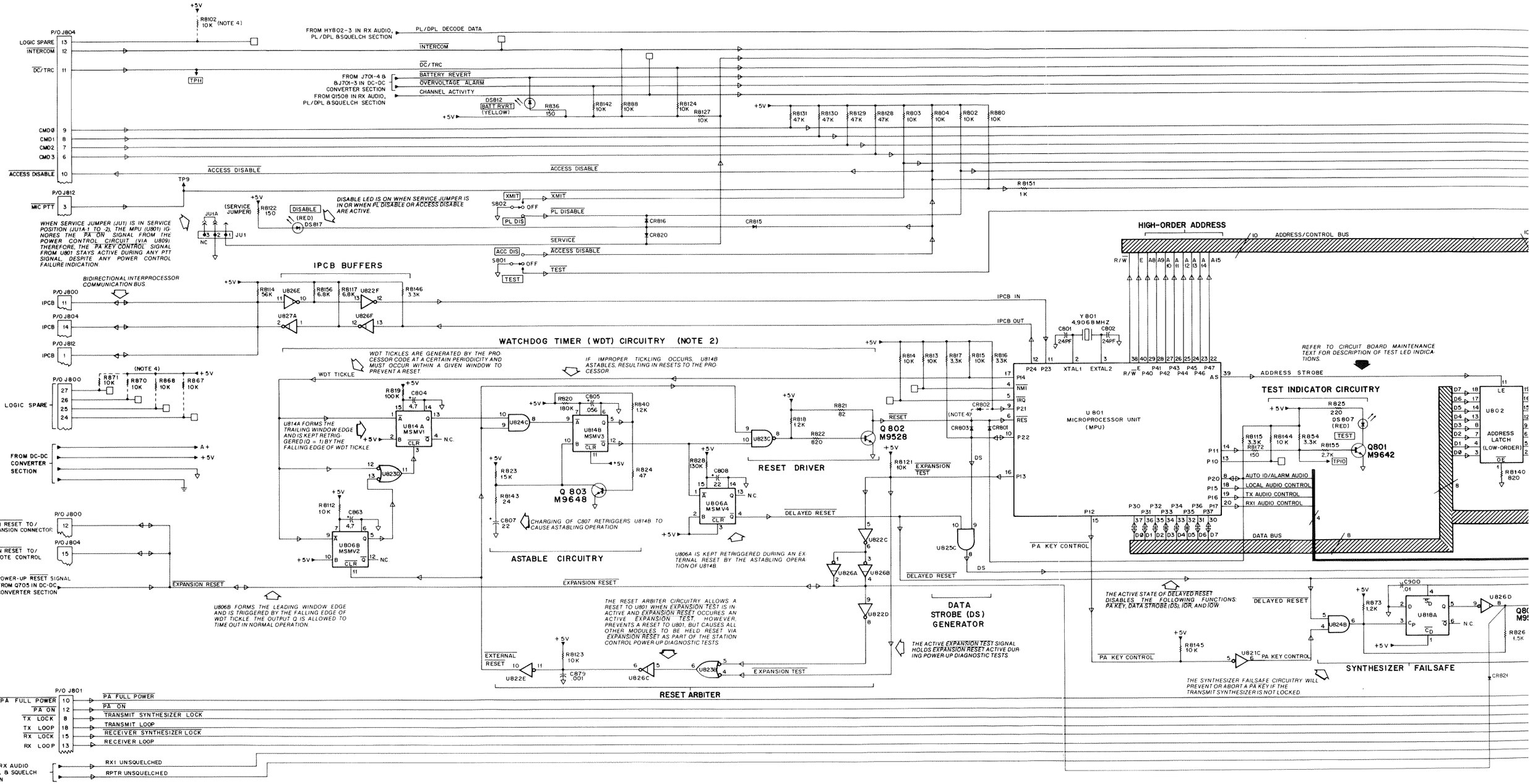
AC FAIL — 4 — (BATTERY REVERT) → TO U810-7 IN PROCESSOR SECTION

N.C. — 2

TEST FROM SW801 TEST

RESET TIMER

MICROPROCESSOR
SCHEMATIC DIAGRAM



PARTS INFORMATION IS LOCATED AT THE END OF THIS SECTION

HIGH-ORDER ADDRESS

ADDRESS/CONTROL BUS

R/W E A8 A9 A10 A11 A12 A13 A14 A15

MEMORY MAP DECODE CIRCUITRY

IOR IS USED AS AN ENABLE SIGNAL (ALONG WITH AN ADDRESS LINE) TO SELECT INPUT (READ) DEVICES. IOW IS USED SIMILARLY TO ENABLE OUTPUT (WRITE) DEVICES.

REFER TO CIRCUIT BOARD MAINTENANCE TEXT FOR DESCRIPTION OF TEST LED INDICATIONS.

TEST INDICATOR CIRCUITRY

U801 MICROPROCESSOR UNIT (MPU)

Y801 4.9068 MHZ

C801 24PF C802 24PF

IPCB IN

IPCB OUT

ADDRESS STROBE

DATA BUS

PA KEY CONTROL

AUTO ID/ALARM AUDIO

LOCAL AUDIO CONTROL

TX AUDIO CONTROL

RX1 AUDIO CONTROL

RESET DRIVER

Q802 M9528

Q801 M9642

Q804 M9528

RESET ARBITER

DATA STROBE (DS) GENERATOR

THE ACTIVE EXPANSION TEST SIGNAL HOLDS EXPANSION RESET ACTIVE DURING POWER-UP DIAGNOSTIC TESTS.

U806A IS KEPT RETRIGGERED DURING AN EXTERNAL RESET BY THE ASTABLING OPERATION OF U814B.

THE ACTIVE STATE OF DELAYED RESET DISABLES THE FOLLOWING FUNCTIONS: PA KEY, DATA STROBE (DS), IOR, AND IOW.

SYNTHESIZER FAILSAFE

THE SYNTHESIZER FAILSAFE CIRCUITRY WILL PREVENT OR ABORT A PA KEY IF THE TRANSMIT SYNTHESIZER IS NOT LOCKED.

STATUS INDICATORS

LED's ARE ON TO INDICATE THE ACTIVE STATE OF THE SIGNAL THEY REPRESENT.

I/O SIGNALS TRUNK

DPL ROTATE

PL/DPL DECODE DATA
DPL ROTATE
INTERCOM
SERVICE
DC/TRC
BATTERY REVERT
OVERVOLTAGE ALARM
CHANNEL ACTIVITY

CMD0
CMD1
CMD2
CMD3
XMIT
PL DISABLE
ACCESS DISABLE
MIC PTT

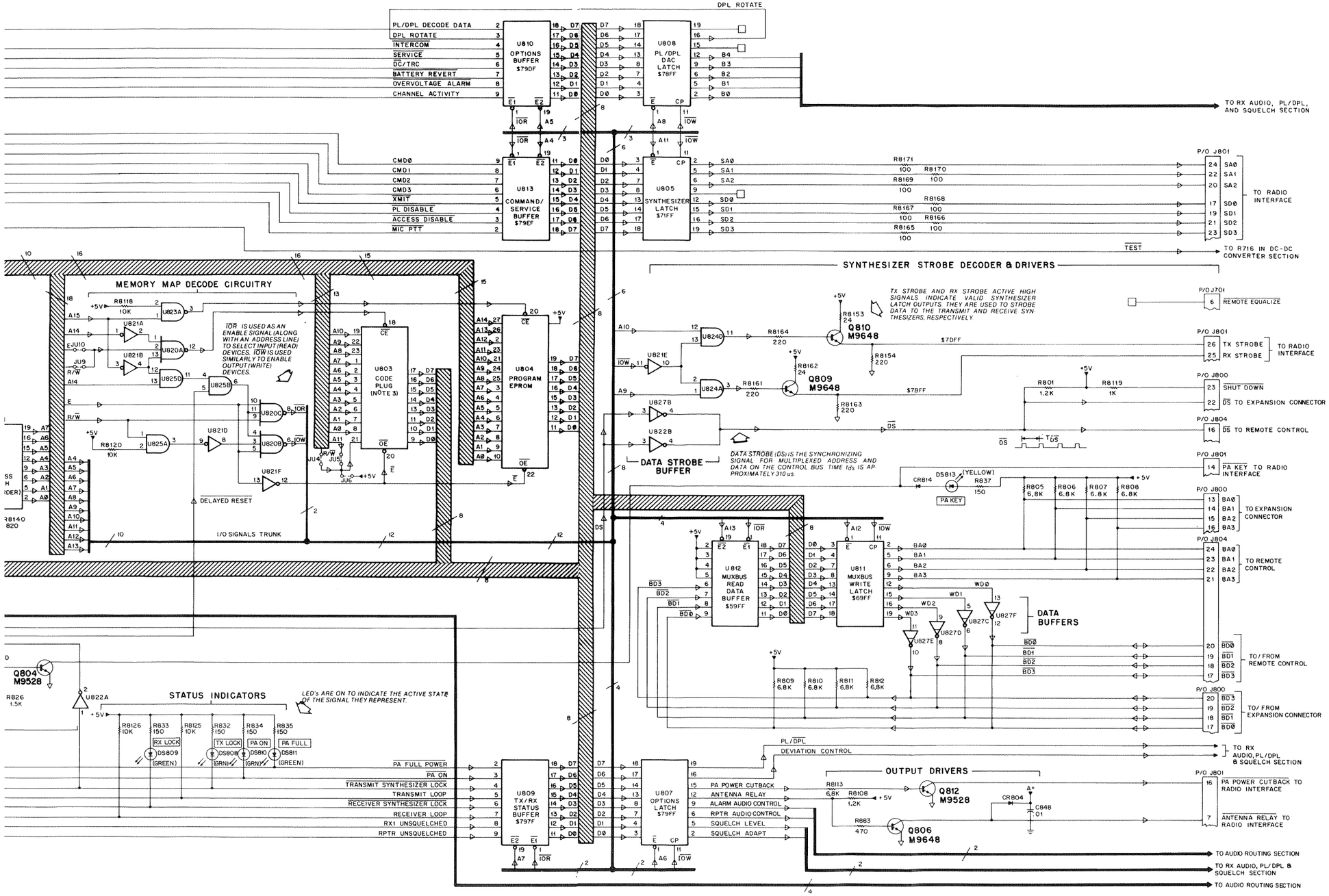
PA FULL POWER
PA ON
TRANSMIT SYNTHESIZER LOCK
TRANSMIT LOOP
RECEIVER SYNTHESIZER LOCK
RECEIVER LOOP
RX1 UNSQUELCHED
RPTR UNSQUELCHED

PA POWER CUTBACK
ANTENNA RELAY
ALARM AUDIO CONTROL
RPTR AUDIO CONTROL
SQUELCH LEVEL
SQUELCH ADAPT

SA0 SA1 SA2 SD0 SD1 SD2 SD3

B4 B3 B2 B1 B0

DATA STROBE BUFFER

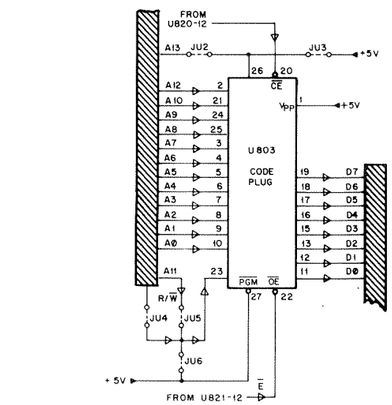


NOTES:

1. Unless otherwise specified, all resistor values are in ohms and all capacitor values are in microfarads.
2. All gates in the Watchdog Timer and Reset Circuitry are shown functionally to depict normal station operation (i.e., not in reset). All other gates are shown functionally to depict the signal in its active state.
3. The Code Plug U803 uses a double footprint (outline) and wiring to accommodate those station control modules with a 2k × 8 RAM or 2k × 8, 8k × 8, or 16k × 8 EPROM's; see schematic detail below.
4. Parts denoted by a dashed line indicate that the board layout accommodates the addition of these parts for future expansion.

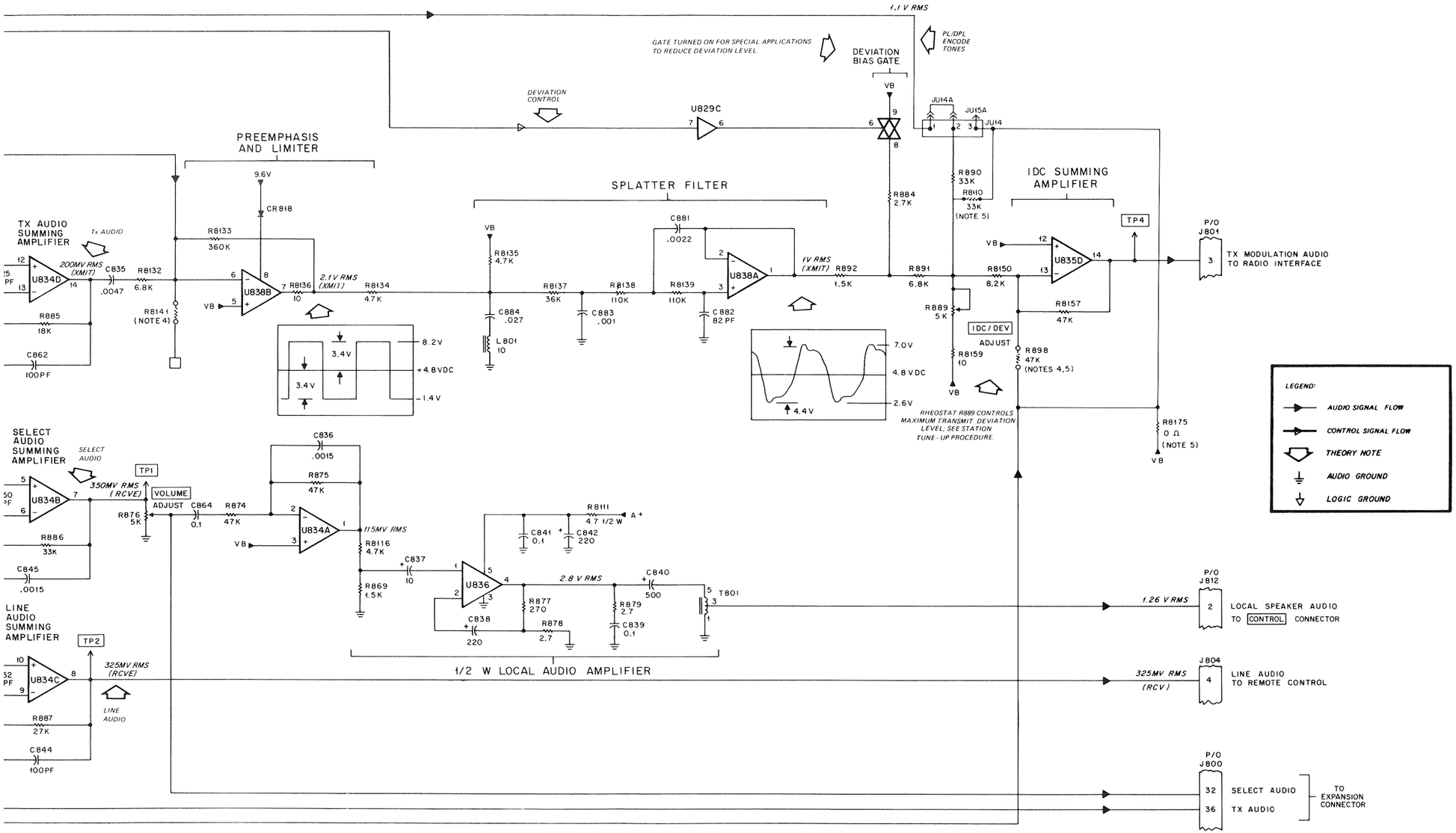
Diode/Jumper Use Chart

Ref. Designation	Normal Position	Description
CR801	IN	Out for mode where program code PC0 = 1
CR802	OUT	In for mode where program code PC1 = 0
CR803	IN	Out for mode where program code PC2 = 1
JU1	OUT	In to disable software power control and enable PA fail alarm
JU2	OUT	In for 16k × 8 EPROM
JU3	IN	Out for 16k × 8 EPROM
JU4	OUT	In for 2k × 8 RAM
JU5	IN	Out for 2k × 8 EPROM; Out for 2k × 8 RAM
JU6	OUT	In for 2k × 8 EPROM
JU7	IN	Out to drive PL/DPL decoder from an external test generator, or when performing the PL/DPL loop test.
JU8	IN	Out to service +5 V dc-dc converter.
JU9	IN	Out for 2k × 8 RAM
JU10	OUT	In for 2k × 8 RAM
JU11	IN	JU11 & JU12 couple VB to select & line audio summers when RX2 audio is unused.
JU12	IN	JU11 & JU12 couple VB to select & line audio summers when RX2 audio is unused.
JU13	OUT	In when HY803 is omitted.
JU14	IN	Out when JU15 is in.
JU15	OUT	In when TX Data audio drives the IDCsummer through R890.



EEPS-35049-B

AUDIO ROUTING
SCHEMATIC DIAGRAM



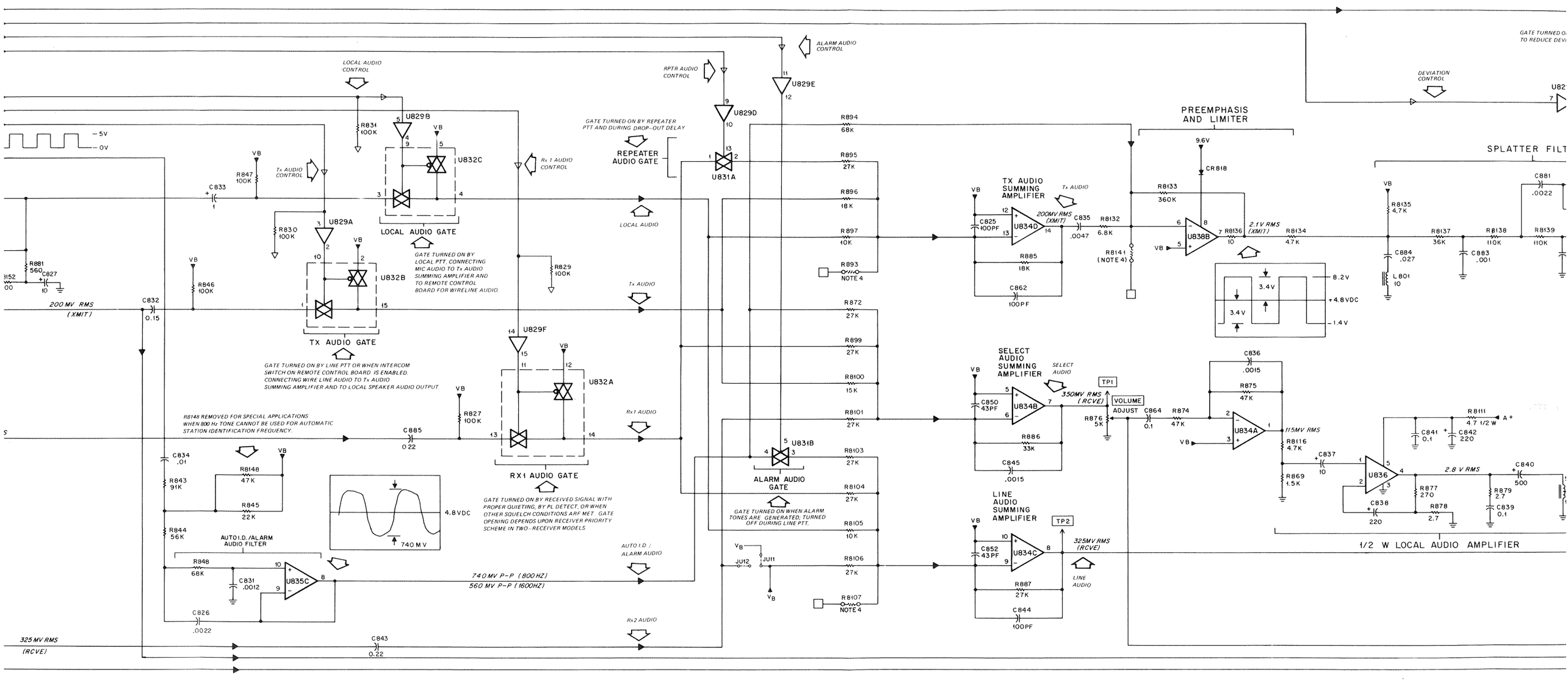
NOTES:

1. Unless otherwise specified, all resistor values are in ohms, all capacitor values are in microfarads, and all inductor values are in millihenries.
2. Unless otherwise specified, all voltage measurements are DC and should be made using a DVM with at least 10 megohms/volt input impedance.
3. Jumper JU11 is normally in, out for two-receiver models.
4. Resistors R893, R898, R8107, and R8141 (shown as dashed lines) are used for special audio requirements. R893 provides an extra transmit audio input without gating control. R898 provides an extra input that bypasses pre- emphasis and IDC (use of R898 requires a separate FCC filing). R8107 provides an extra wireline audio input without gating control. R8141 provides an extra transmit audio input that bypasses pre-emphasis.
5. Resistors R898, R8110, and R8175 are used to configure the IDC summing amplifier input (U835D-13) per the following table:

Reference Symbol	*MSF 5000* Station	*MSF 5000* With Option C369	*PURC 500* Transmitters
R898	IN	OUT	IN
R8110	IN	IN	OUT
R8175	IN	OUT	OUT

EEPS-35048-8

PARTS INFORMATION IS LOCATED AT THE END OF THIS SECTION


LOCAL AUDIO CONTROL
RPTR AUDIO CONTROL
ALARM AUDIO CONTROL
DEVIATION CONTROL
GATE TURNED ON BY REPEATER PTT AND DURING DROP-OUT DELAY
REPEATER AUDIO GATE
Tx AUDIO CONTROL
Rx 1 AUDIO CONTROL
LOCAL AUDIO GATE
GATE TURNED ON BY LOCAL PTT, CONNECTING MIC AUDIO TO Tx AUDIO SUMMING AMPLIFIER AND TO REMOTE CONTROL BOARD FOR WIRELINE AUDIO
LOCAL AUDIO
Tx AUDIO
TX AUDIO GATE
GATE TURNED ON BY LINE PTT OR WHEN INTERCOM SWITCH ON REMOTE CONTROL BOARD IS ENABLED, CONNECTING WIRE LINE AUDIO TO Tx AUDIO SUMMING AMPLIFIER AND TO LOCAL SPEAKER AUDIO OUTPUT
R8148 REMOVED FOR SPECIAL APPLICATIONS WHEN 800 Hz TONE CANNOT BE USED FOR AUTOMATIC STATION IDENTIFICATION FREQUENCY.
RX1 AUDIO GATE
GATE TURNED ON BY RECEIVED SIGNAL WITH PROPER QUIETING, BY PL DETECT, OR WHEN OTHER SQUELCH CONDITIONS ARE MET. GATE OPENING DEPENDS UPON RECEIVER PRIORITY SCHEME IN TWO-RECEIVER MODELS.
ALARM AUDIO GATE
GATE TURNED ON WHEN ALARM TONES ARE GENERATED; TURNED OFF DURING LINE PTT.
AUTO I.D./ALARM AUDIO FILTER
AUTO I.D. / ALARM AUDIO
Rx1 AUDIO
Rx2 AUDIO
TX AUDIO SUMMING AMPLIFIER
SELECT AUDIO SUMMING AMPLIFIER
LINE AUDIO SUMMING AMPLIFIER
SELECT AUDIO
LINE AUDIO
PREEMPHASIS AND LIMITER
SPLATTER FILT
VOLUME ADJUST
1/2 W LOCAL AUDIO AMPLIFIER
-5V
-0V
VB
200 MV RMS (XMIT)
740 MV P-P (800 HZ)
560 MV P-P (1600 HZ)
4.8 VDC
740 M V
325 MV RMS (RCVE)
200MV RMS (XMIT)
350MV RMS (RCVE)
325MV RMS (RCVE)
2.1V RMS (XMIT)
115MV RMS
2.8 V RMS
9.6V
8.2V
+4.8VDC
-1.4V
3.4V
A+
TP1
TP2
NOTE 4
U829A
U829B
U829D
U829E
U829F
U831A
U831B
U832A
U832B
U832C
U834A
U834B
U834C
U834D
U835C
U836
U838B
R830 100K
R831 100K
R833 100K
R834 100K
R846 100K
R847 100K
R827 100K
R829 100K
R881 560
R8152 100
C827 10
C832 0.15
C833 1
C834 .01
C885 0.22
C843 0.22
R843 91K
R844 56K
R845 22K
R8148 47K
R848 68K
C831 .0012
C826 .0022
R894 68K
R895 27K
R896 18K
R897 10K
R893
R872 27K
R899 27K
R8100 15K
R8101 27K
R8103 27K
R8104 27K
R8105 10K
R8106 27K
R8107
JU11
JU12
C825 100PF
C862 100PF
R885 18K
C835 .0047
R8132 6.8K
R8141 (NOTE 4)
C850 43PF
C845 .0015
R886 33K
C852 43PF
C844 100PF
R887 27K
R8133 360K
CR818
R8135 4.7K
C884 .027
L801 10
R8136 10
R8134 4.7K
R8137 36K
R8138 110K
R8139 110K
C881 .0022
C883 .001
C836 .0015
R875 47K
R876 5K
C864 0.1
R874 47K
R8116 4.7K
R869 1.5K
C837 10
C841 0.1
C842 220
R8111 4.7 1/2 W
C838 220
R877 270
R878 2.7
R879 2.7
C839 0.1
C840 500

FROM HY802-17 IN RX AUDIO, PL/DPL & SQUELCH SECTION

PL/DPL ENCODE TONES

DEVIATION

FROM U807 IN PROCESSOR SECTION

ALARM AUDIO

RPTR AUDIO

LOGIC HIGH SIGNAL (2.4 V OR GREATER) TURNS ON RESPECTIVE AUDIO GATE

CONTROL SIGNALS

LOCAL AUDIO

RX1 AUDIO

FROM U801 IN PROCESSOR SECTION

TX AUDIO

+5V

0V

AUDIO I.D./ ALARM AUDIO

P/O J800

LOCAL AUDIO FROM EXPANSION CONNECTOR 33

P/O J812

MIC AUDIO FROM CONTROL CONNECTOR 4

TP8

R881 560

C827 10

+9.6V R8152 100

P/O J804

TX AUDIO FROM REMOTE CONTROL BOARD 5

200 MV RMS (XMIT)

C832 0.15

C833 1

VB

R847 100K

R846 100K

R834 100K

R830 100K

R829 100K

LOCAL AUDIO CONTROL

Tx AUDIO CONTROL

Rx 1 AUDIO CONTROL

U829B

U832C

U829A

U832B

LOCAL AUDIO GATE

GATE TURNED ON BY LOCAL PTT, CONNECTING MIC AUDIO TO Tx AUDIO SUMMING AMPLIFIER AND TO REMOTE CONTROL BOARD FOR WIRELINE AUDIO.

TX AUDIO GATE

GATE TURNED ON BY LINE PTT OR WHEN INTERCOM SWITCH ON REMOTE CONTROL BOARD IS ENABLED, CONNECTING WIRE LINE AUDIO TO Tx AUDIO SUMMING AMPLIFIER AND TO LOCAL SPEAKER AUDIO OUTPUT.

U829F

U832A

RX1 AUDIO GATE

GATE TURNED ON BY RECEIVED SIGNAL WITH PROPER QUIETING, BY PL DETECT, OR WHEN OTHER SQUELCH CONDITIONS ARE MET. GATE OPENING DEPENDS UPON RECEIVER PRIORITY SCHEME IN TWO-RECEIVER MODELS.

RPTR AUDIO CONTROL

ALARM AUDIO CONTROL

U829D

U829E

GATE TURNED ON BY REPEATER PTT AND DURING DROP-OUT DELAY

REPEATER AUDIO GATE

U831A

LOCAL AUDIO

Tx AUDIO

Rx1 AUDIO

AUTO I.D./ ALARM AUDIO

Rx2 AUDIO

U831B

ALARM AUDIO GATE

GATE TURNED ON WHEN ALARM TONES ARE GENERATED; TURNED OFF DURING LINE PTT.

R894 68K

R895 27K

R896 18K

R897 10K

R893 NOTE 4

R872 27K

R899 27K

R8100 15K

R8101 27K

R8103 27K

R8104 27K

R8105 10K

R8106 27K

R8107 NOTE 4

JU11

JU12

RX1 AUDIO FROM U833-1 IN RX AUDIO, PL/DPL & SQUELCH SECTION

325 MV RMS (RCVE)

R8148 REMOVED FOR SPECIAL APPLICATIONS WHEN 800 Hz TONE CANNOT BE USED FOR AUTOMATIC STATION IDENTIFICATION FREQUENCY.

C885 0.22

R827 100K

C834 .01

R843 91K

R844 56K

R8148 47K

R845 22K

4.8 VDC

740 MV

AUTO I.D./ALARM AUDIO FILTER

R848 68K

C831 .0012

C826 .0022

U835C

740 MV P-P (800 HZ)

560 MV P-P (1600 HZ)

DC POWER FROM DC-DC CONVERTER SECTION

4.8V

A+

VB

+9.6V

+5V

FROM EXPANSION CONNECTOR

P/O J800

RX2 AUDIO 35

TX DATA AUDIO 34

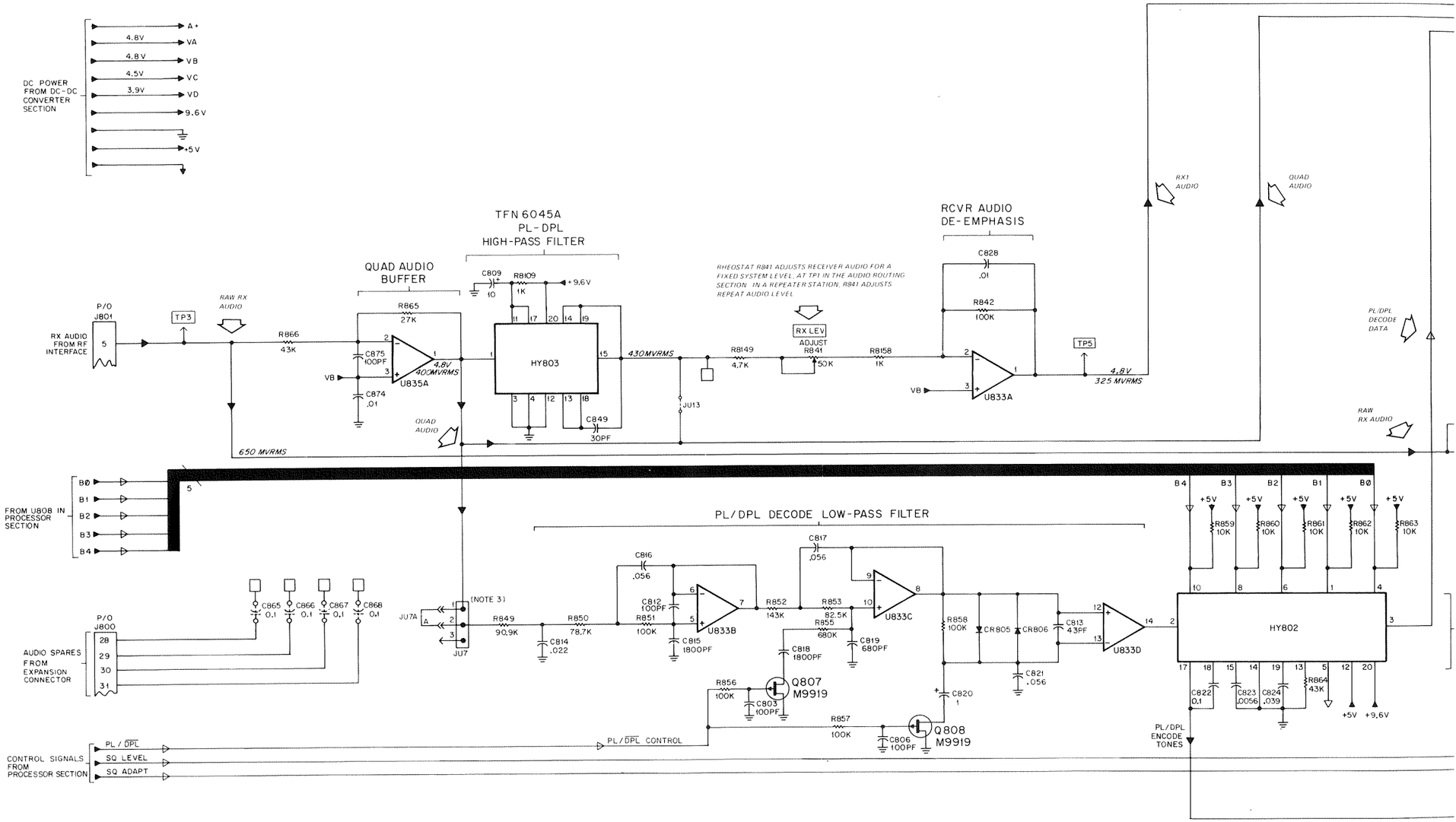
325 MV RMS (RCVE)

C843 0.22

SQUELCH CONTROL
SCHEMATIC DIAGRAM

Notes:

1. Unless otherwise specified, all resistor values are in ohms, all capacitor values are in microfarads, and all inductor values are in microhenries.
2. Unless otherwise specified, all voltage measurements are dc and should be made using a DVM with at least 10 megohms/volt input impedance for increased accuracy.
3. Jumper JU7 is normally in but may be removed on some models to enable a "PL Loop Test".



TFN 6045A
PL-DPL
GH-PASS FILTER

HY803

RHEOSTAT R841 ADJUSTS RECEIVER AUDIO FOR A FIXED SYSTEM LEVEL. AT TP1 IN THE AUDIO ROUTING SECTION. IN A REPEATER STATION, R841 ADJUSTS REPEAT AUDIO LEVEL

RCVR AUDIO
DE-EMPHASIS

RX LEV
ADJUST
R841
50K

TP5

4.8V
325 MVRMS

430MVRMS

RX1
AUDIO

QUAD
AUDIO

PL/DPL
DECODE
DATA

RAW
RX AUDIO

POSITIVE GOING NOISE SPIKES AT U1551B-6 (NOISE DETECTOR) BECOME LARGER NEGATIVE GOING SPIKES AT U1551B-4 THAT CAUSE THE AVERAGE VOLTAGE TO DECREASE FROM THE NO NOISE, FULLY QUIETED VOLTAGE OF 4.8 VOLTS AT U1551B-4

RPTR SQUELCH BUFFER

RPTR SQ
ADJUST

1.5 V DC FULL UNSQUELCHED
9 V DC FULL SQUELCHED

REPEATER SQUELCH DETECT

NOISE DETECTOR

NOISE AMPLIFIER

AMPLIFIER/
LIMITER

NOISE DETECTOR

POSITIVE GOING NOISE SPIKES AT U1550-14 (NOISE DETECTOR) BECOME LARGER NEGATIVE GOING SPIKES AT U1550-12 THAT CAUSE THE AVERAGE VOLTAGE TO DECREASE FROM THE NO NOISE, FULLY QUIETED VOLTAGE OF 4.8 VOLTS AT U1550-12

0 V DC FULL UNSQUELCHED
8.4 V DC FULL SQUELCHED

AUDIO SQUELCH BUFFER

REM. SQUELCH SWITCH

ADAPT CONTROL SWITCH

PL/DPL DECODE LOW-PASS FILTER

TRN4372A
DIGITAL-TO-ANALOG
CONVERTER/LOW-
PASS FILTER

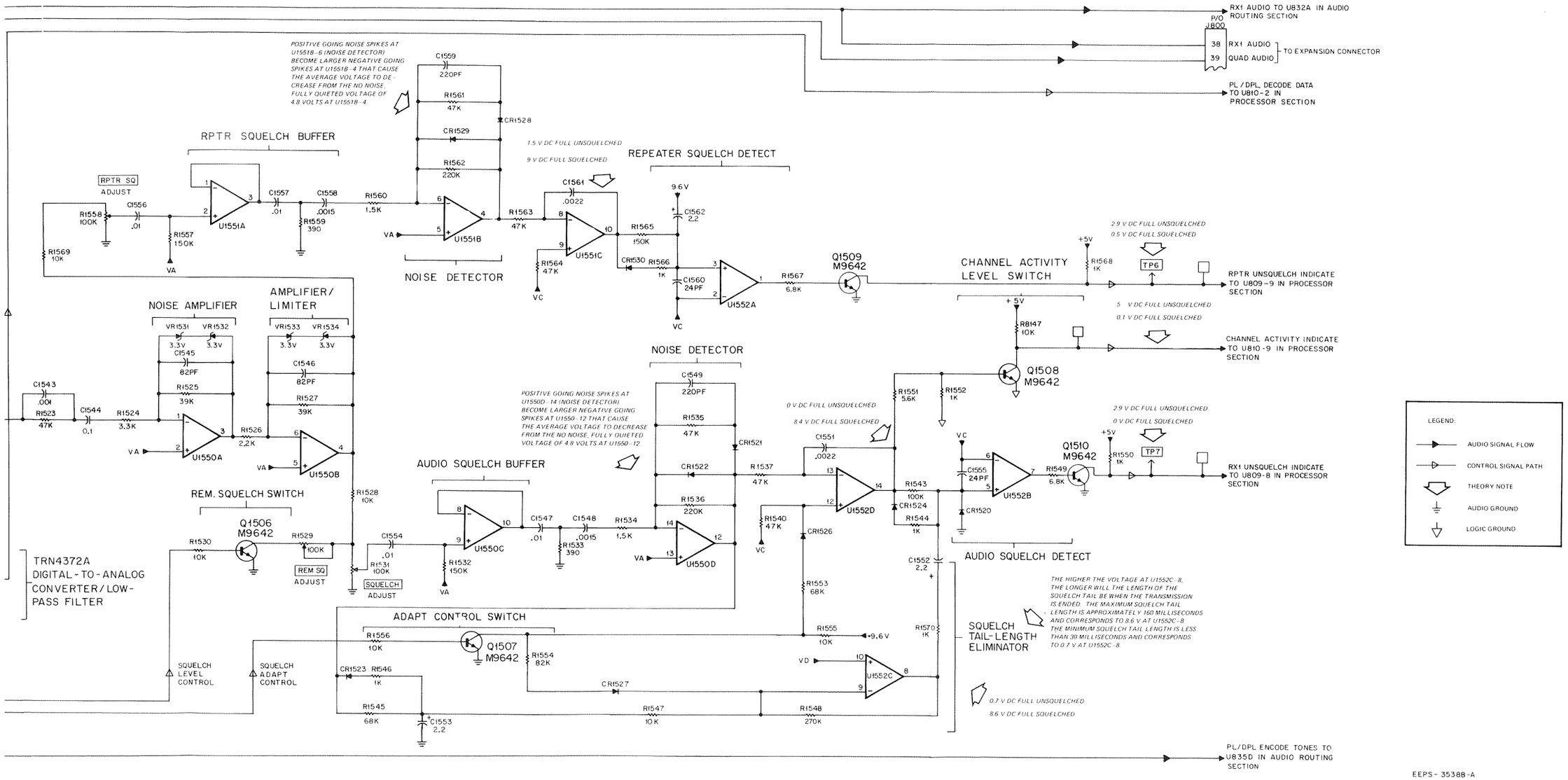
HY802

PL/DPL
ENCODE
TONES

SQUELCH
LEVEL
CONTROL

SQUELCH
ADAPT
CONTROL

PL/DPL CONTROL


RX1 AUDIO TO U832A IN AUDIO ROUTING SECTION
P/O J800
38 RX1 AUDIO
39 QUAD AUDIO
TO EXPANSION CONNECTOR
PL/DPL DECODE DATA TO U810-2 IN PROCESSOR SECTION
POSITIVE GOING NOISE SPIKES AT U1551B-6 (NOISE DETECTOR) BECOME LARGER NEGATIVE GOING SPIKES AT U1551B-4 THAT CAUSE THE AVERAGE VOLTAGE TO DECREASE FROM THE NO NOISE, FULLY QUIETED VOLTAGE OF 4.8 VOLTS AT U1551B-4.
RPTR SQUELCH BUFFER
RPTR SQ ADJUST
R1558 100K
C1556 .01
R1557 150K
R1569 10K
U1551A
C1557 .01
C1558 .0015
R1559 390
R1560 1.5K
C1559 220PF
R1561 47K
CR1528
CR1529
R1562 220K
1.5 V DC FULL UNSQUELCHED
9 V DC FULL SQUELCHED
REPEATER SQUELCH DETECT
C1561 .0022
9.6V
C1562 2.2
R1563 47K
U1551B
U1551C
R1564 47K
R1565 150K
CR1530
R1566 1K
C1560 24PF
U1552A
R1567 6.8K
Q1509 M9642
NOISE DETECTOR
CHANNEL ACTIVITY LEVEL SWITCH
2.9 V DC FULL UNSQUELCHED
0.5 V DC FULL SQUELCHED
+5V
R1568 1K
TP6
RPTR UNSQUELCH INDICATE TO U809-9 IN PROCESSOR SECTION
5 V DC FULL UNSQUELCHED
0.1 V DC FULL SQUELCHED
CHANNEL ACTIVITY INDICATE TO U810-9 IN PROCESSOR SECTION
+5V
R8147 10K
Q1508 M9642
NOISE AMPLIFIER
AMPLIFIER/ LIMITER
VR1531 3.3V
VR1532 3.3V
C1545 82PF
VR1533 3.3V
VR1534 3.3V
C1546 82PF
C1543 .001
R1523 47K
C1544 0.1
R1524 3.3K
R1525 39K
R1527 39K
R1526 2.2K
U1550A
U1550B
C1549 220PF
R1535 47K
CR1521
CR1522
R1536 220K
POSITIVE GOING NOISE SPIKES AT U1550D-14 (NOISE DETECTOR) BECOME LARGER NEGATIVE GOING SPIKES AT U1550-12 THAT CAUSE THE AVERAGE VOLTAGE TO DECREASE FROM THE NO NOISE, FULLY QUIETED VOLTAGE OF 4.8 VOLTS AT U1550-12.
0 V DC FULL UNSQUELCHED
8.4 V DC FULL SQUELCHED
C1551 .0022
R1537 47K
R1551 5.6K
R1552 1K
2.9 V DC FULL UNSQUELCHED
0 V DC FULL SQUELCHED
+5V
R1550 1K
TP7
Q1510 M9642
R1549 6.8K
RX1 UNSQUELCH INDICATE TO U809-8 IN PROCESSOR SECTION
AUDIO SQUELCH BUFFER
REM. SQUELCH SWITCH
Q1506 M9642
R1530 10K
R1529 100K
REM SQ ADJUST
C1554 .01
R1531 100K
SQUELCH ADJUST
R1528 10K
C1547 .01
C1548 .0015
R1533 390
R1534 1.5K
R1532 150K
U1550C
U1550D
R1540 47K
CR1526
R1543 100K
CR1524
R1544 1K
U1552B
CR1520
VC
C1555 24PF
R1553 68K
C1552 2.2
AUDIO SQUELCH DETECT
TRN4372A DIGITAL-TO-ANALOG CONVERTER/LOW-PASS FILTER
ADAPT CONTROL SWITCH
Q1507 M9642
R1556 10K
R1554 82K
R1555 10K
+9.6 V
R1570 1K
SQUELCH TAIL-LENGTH ELIMINATOR
THE HIGHER THE VOLTAGE AT U1552C-8, THE LONGER WILL THE LENGTH OF THE SQUELCH TAIL BE WHEN THE TRANSMISSION IS ENDED. THE MAXIMUM SQUELCH TAIL LENGTH IS APPROXIMATELY 160 MILLISECONDS AND CORRESPONDS TO 8.6 V AT U1552C-8. THE MINIMUM SQUELCH TAIL LENGTH IS LESS THAN 30 MILLISECONDS AND CORRESPONDS TO 0.7 V AT U1552C-8.
0.7 V DC FULL UNSQUELCHED
8.6 V DC FULL SQUELCHED
VD
U1552C
CR1527
R1545 68K
C1553 2.2
R1547 10K
R1548 270K
CR1523
R1546 1K
SQUELCH LEVEL CONTROL
SQUELCH ADAPT CONTROL
PL/DPL ENCODE TONES TO U835D IN AUDIO ROUTING SECTION
LEGEND:
AUDIO SIGNAL FLOW
CONTROL SIGNAL PATH
THEORY NOTE
AUDIO GROUND
LOGIC GROUND

EEPS-35388-A

PARTS LISTS

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R724	6-11024A81	22k
R725	6-11024B22	1 meg
R727	6-11024A39	390
R728	6-11024A63	3.9k
R729	6-11049C22	1.91k ±1%; 1/4 W; conventional
R730	6-11049C26	2.1k ±1%; 1/4 W; conventional
R731 thru 734	6-125B70	1; 1/2 W; conventional
R735	6-11024A25	100
R736	6-11024A39	390
R737	6-11024A47	820
R738	6-11024A17	47
R739	6-11009E33	220; 1/4 W; conventional
R740	6-124B55	2.7; 1/4 W; conventional
R801	6-11024A53	1.5k
R802, 803, 804	6-11024A73	10k
R805 thru 812	6-11024A69	6.8k
R813, 814, 815	6-11024A73	10k
R816, 817	6-11024A61	3.3k
R818	6-11024A49	1k
R819	6-11024A97	100k
R820	6-11024B04	180k
R821	6-11045A23	82; 1/2 W; conventional
R822	6-11024A47	820
R823	6-11024A77	15k
R824	6-11024A17	47
R825	6-11024A33	220
R826	6-11024A53	1.5k
R827	6-11024A97	100k
R828	6-11024B01	130k
R829	6-11024A97	100k
R830	6-11024A97	100k
R831	6-11024A97	100k
R832 thru 836	6-11024A29	150
R837	6-11024A29	150
R838, 839	6-11024A73	10k
R840	6-11024A53	1.5k
R841	18-83686N03	variable; 50k; conventional (receive audio level)
R842	6-11024A97	100k
R843	6-11024A96	91k
R844	6-11024A91	56k
R845	6-11024A81	22k
R846, 847	6-11024A97	100k
R848	6-11024A93	68k
R849	6-10621D84	90.9k ±1%; conventional
R850	6-10621D78	78.7k ±1%; conventional
R851	6-10621D88	100k ±1%; conventional
R852	6-10621E04	143k ±1%; conventional
R853	6-10621D80	82.5k ±1%; conventional
R854	6-11024A61	3.3k
R855	6-11024B18	680k
R856, 857	6-11024A97	100k
R858	6-11024A97	100k
R859 thru 863	6-11024A73	10k
R864	6-11024A88	43k
R865	6-11024A83	27k
R866	6-11024A88	43k
R869	6-11024A53	1.5k
R872	6-11024A83	27k
R873	6-11024A53	1.5k
R874, 875	6-11024A89	47k
R876	18-82787K09	variable; 5k; conventional (VOLUME)
R877	6-11045A35	270; 1/2 W; conventional
R878, 879	6-124B55	2.7, 1/4 W; conventional
R880	6-11024A73	10k
R881	6-11024A43	560
R882	6-11024A61	3.3k
R883	6-11024A41	470
R884	6-11024A59	2.7k
R885	6-11024A79	18k
R886	6-11024A85	33k
R887	6-11024A83	27k
R888	6-11024A73	10k
R889	18-83686N05	variable; 5k; conventional (IDC-deviation level)
R890	6-11024A85	33k
R891	6-11024A69	6.8k
R892	6-11024A53	1.5k
R894	6-11024A93	68k
R895	6-11024A83	27k
R896	6-11024A79	18k
R897	6-11024A73	10k
R899	6-11024A83	27k
R1523	6-11024A89	47k
R1524	6-11024A61	3.3k
R1525	6-11024A87	39k
R1526	6-11024A57	2.2k
R1527	6-11024A87	39k
R1528	6-11024A73	10k
R1529	18-83686N01	variable; 100k; conventional (remote squelch level)
R1530	6-11024A73	10k
R1531	18-82787K08	variable; 100k; conventional (SQUELCH)
R1532	6-11024B02	150k
R1533	6-11024A39	390
R1534	6-11024A53	1.5k
R1535	6-11024A89	47k
R1536	6-11024B06	220k

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R1537	6-11024A89	47k
R1538	6-11024A61	3.3k
R1539	6-11024A31	180
R1540	6-11024A89	47k
R1541	6-11024A39	390
R1542	6-11024A59	2.7k
R1543	6-11024A97	100k
R1544	6-11024A49	1k
R1545	6-11024A93	68k
R1546	6-11024A49	1k
R1547	6-11024A73	10k
R1548	6-11024B08	270k
R1549	6-11024A69	6.8k
R1550	6-11024A49	1k
R1551	6-11024A67	5.6k
R1552	6-11024A49	1k
R1553	6-11024A93	68k
R1554	6-11024A95	82k
R1555, 1556	6-11024A73	10k
R1557	6-11024B02	150k
R1558	18-83686N01	variable; 100k; conventional (repeater squelch level)
R1559	6-11024A39	390
R1560	6-11024A53	1.5k
R1561	6-11024A89	47k
R1562	6-11024B06	220k
R1563, 1564	6-11024A89	47k
R1565	6-11024B02	150k
R1566	6-11024A49	1k
R1567	6-11024A69	6.8k
R1568	6-11024A49	1k
R1569	6-11024A73	10k
R1570	6-11024A49	1k
R8100	6-11024A77	15k
R8101, 8102	6-11024A83	27k
R8103, 8104	6-11024A83	27k
R8105	6-11024A73	10k
R8106	6-11024A83	27k
R8108	6-11024A53	1.5k
R8109	6-11024A49	1k
R8111	6-125B61	4.7; 1/2 W; conventional
R8112	6-11024A73	10k
R8113	6-11024A69	6.8k
R8114	6-11024A91	56k
R8115	6-11024A61	3.3k
R8116	6-11024A65	4.7k
R8117	6-11024A69	6.8k
R8118	6-11024A73	10k
R8119	6-11009A49	1k; 1/4 W; conventional
R8120, 8121	6-11024A73	10k
R8122	6-11024A29	150
R8123 thru 8127	6-11024A73	10k
R8128 thru 8131	6-11024A89	47k
R8132	6-11024A69	6.8k
R8133	6-11024B11	360k
R8134	6-11024A65	4.7k
R8135	6-11024A65	4.7k
R8136	6-11024A01	10
R8137	6-11024A86	36k
R8138, 8139	6-11024A98	110k
R8140	6-11024A47	820
R8142	6-11024A73	10k
R8143	6-11024A10	24
R8144 thru 8145	6-11024A73	10k
R8146	6-11024A61	3.3k
R8147	6-11024A73	10k
R8148	6-11024A89	47k
R8149	6-11024A65	4.7k
R8150	6-11024A71	8.2k
R8151	6-11024A49	1k
R8152	6-11024A25	100
R8153	6-11024A10	24
R8154	6-11024A33	220
R8155	6-11024A59	2.7k
R8156	6-11024A69	6.8k
R8157	6-11024A89	47k
R8158	6-11024A49	1k
R8159	6-11024A01	10
R8161	6-11024A33	220
R8162	6-11024A10	24
R8163, 8164	6-11024A33	220
R8165 thru 8171	6-11024A25	100
R8172	6-11024A29	150
		switch:
S801, 802	40-83685N01	spdt
		transformer, auto:
T801	25-83687N01	pri: leads 1 to 5; ref. 16 ohms ±10% sec: leads 1 to 3; load imp. 3.2 ohms ±5%
		integrated circuit: (see note 1)
U701	51-84371K74	quad comparator
U801	51-83625M66	microprocessor; type MC6803
U802	51-83627M03	octal tri-state latch
U805	51-82609M77	octal latch
U806	51-84561L11	dual monostable

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
U807, 808	51-82609M77	octal latch
U809, 810	51-83627M96	octal buffer
U811	51-82609M77	octal latch
U812, 813	51-83627M96	octal buffer
U814	51-84561L11	dual monostable
U818	51-83627M93	dual D flip-flop
U820	51-84561L08	triple 3-input NAND
U821, 822	51-84561L03	hex inverter
U823	51-83627M94	quad NAND
U824, 825	51-84561L07	quad AND gate
U826, 827	51-84561L78	hex open collector output inverter
U829	51-83627M88	hex level shifter
U831	51-82884L48	quad analog switch
U832	51-82884L65	triple 2-channel mux
U833, 834, 835	51-82609M05	quad op amplifier
U836	51-83629M33	1/2 watt audio amplifier
U838	51-82609M33	dual op amplifier
U1550, 1551	51-83629M06	quad op amplifier
U1552	51-83629M09	quad op amplifier
		voltage regulator: (see note 1)
VR701	48-83461E40	Zener; 5.1 V
VR702	48-83461E27	Zener; 6 V
VR1531 thru 1534	48-82256C26	Zener; 3.3 V
		crystal: (see note 1)
Y801	48-82611M15	4.9068 MHz
		mechanical parts
	2-10971A16	NUT, hex: M3-0.5mm; 2 used
	3-83497N04	SCREW, machine: M3-0.5 × 8 mm; 2 used
	9-84881F02	SOCKET, 28-contact; U804
	9-84924E01	SOCKET, 24-contact; U803
	14-83820M03	INSULATOR, power supply
	14-84602K02	INSULATOR, crystal socket
	26-83130N01	SHIELD, bottom
	26-83131N01	SHIELD, top
	26-83192N01	HEAT SINK; U836
	26-83192N02	HEAT SINK; Q701
	29-10271A15	TERMINAL, testpoint; 15 used
	29-82906N01	TERMINAL, fuse mounting; 2 used

notes:

1. For optimum performance, crystals, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.
2. Chip resistors are numerically coded for value, code format is: AAB; where AA are the two most significant value digits, and B is the number of zeros following the value digits. For example, a chip coded 103 is a 10k ohm resistor.

parts list

TRN5195A Station Control Board — PL-8165-C

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed conventional; uF ±5%; 50 V: unless otherwise stated
C701	21-11013A61	.001; chip
C702	23-82601A48	660 +100-10%; 40 V
C703 thru 705	21-11032B13	0.1 +80-20%; chip
C706	23-82747L26	1000 +100-10%; 12 V
C708	21-11032A21	.01 ±10%; chip
C709	21-11031A29	39 pF; chip
C710	8-11023A29	0.22
C711 thru 718	21-11031A29	39 pF; chip
C801, 802	21-11022G39	24 pF
C803	21-11022K42	100 pF
C804	23-11013E09	4.7 ±10%; 25 V
C805	8-11017A15	.056
C806	21-11022K42	100 pF
C807, 808	23-11013C11	22 ±10%; 15 V
C809	23-11013E13	10 ±10%; 25 V
C810	23-11019A48	220 ±20%; 10 V
C812	21-11022K42	100 pF
C813	21-11022G45	43 pF
C814	8-11017A11	.022
C815	21-84393M02	1800 pF
C816, 817	8-11017A15	.056
C818	21-84393M02	1800 pF
C819	21-84393M01	680 pF
C820	23-11013E01	1 ±10%; 25 V
C821	8-11017A15	.056
C822	8-11017A17	0.1
C823	8-11017A19	.0056
C824	8-11017A30	.039
C825	21-11022K42	100 pF
C826	8-11017A03	.0022
C827	23-11019A20	10; 25 V
C828	8-11017A08	.01
C829	23-11019A20	10 ±20%
C830	23-11019A09	1 ±20%
C831	8-11017A24	.0012; 100 V
C832	8-11023A27	0.15
C833	23-11019A09	1 ±20%
C834	8-11017A08	.01
C835	8-11017A06	.0047
C836	8-11017A02	.0015
C837	23-11019A20	10 ±20%; 25 V
C838	23-84665F06	220 ±10%; 25 V
C839	8-11017A17	0.1
C840	23-83210A19	500 ±10%; 20 V
C841	8-11017A17	0.1
C842	23-84665F06	220 ±10%; 25 V
C843	8-11023A29	0.22
C844	21-11022K42	100 pF
C845	8-11017A02	.0015
C846	23-11019A20	10 ±20%; 25 V
C847, 848	21-11021G07	.01 +100-0%
C849	21-82877B06	30 pF ±10%
C850	21-11022G45	43 pF
C851	23-11019A45	100 ±20%; 16 V
C852	21-11022G45	43 pF
C862	21-11022K42	100 pF
C863	23-11013E09	4.7 ±10%; 25 V
C864	8-11017A17	0.1
C869	21-11022K42	100 pF
C871, 872, 873	21-11032B13	0.1 +80-20%; chip
C874	8-11017A08	.01
C875	21-11022K42	100 pF
C876, 877, 878	21-11032B13	0.1 +80-20%; chip
C879	8-11017A01	.001
C880	21-11032B13	0.1 +80-20%; chip
C881	8-11017A03	.0022
C882	21-11022K40	82 pF
C883	8-11017A01	.001
C884	8-11017A29	.027
C885	8-11023A29	0.22
C886 thru 899	21-11032B13	0.1 +80-20%; chip
C900	21-83596E09	.01 +80%-20%; 200 V
C1543	8-11017A01	.001
C1544	8-11017A17	0.1
C1545, 1546	21-11022K40	82 pF
C1547	8-11017A08	.01
C1548	8-11017A02	.0015
C1549	21-11022K50	220 pF
C1550	23-11013E13	10 ±10%; 25 V
C1551	8-11017A03	.0022
C1552, 1553	23-11013E05	2.2 ±10%; 25 V
C1554	8-11017A08	.01
C1555	21-11022K27	24 pF
C1556, 1557	8-11017A08	.01
C1558	8-11017A02	.0015
C1559	21-11022K50	220 pF
C1560	21-11022K27	24 pF
C1561	8-11017A03	.0022
C1562	23-11013E05	2.2 ±10%; 25 V
C1563	23-11013E13	10 ±10%; 25 V
C8100	21-11032B13	0.1 +80-20%; chip
		diode: (see note 1)
CR701	48-82525G18	silicon
CR702	48-82466H13	silicon
CR703 thru 709	48-11034D01	silicon
CR710	48-82466H13	silicon
CR801	48-84616A09	hot carrier
CR803	48-84616A09	hot carrier
CR804	48-11034A01	silicon
CR805, 806	48-11034D01	silicon
CR814, 815, 816	48-11034A01	silicon
CR818	48-11034A01	silicon
CR820	48-11034A01	silicon
CR821	48-84616A09	hot carrier
CR1520 thru 1522	48-84616A01	hot carrier
CR1523	48-11034A01	silicon
CR1524	48-11034D01	silicon
CR1526, 1527	48-11034D01	silicon
CR1528, 1529	48-84616A01	hot carrier
CR1530	48-11034A01	silicon
		light emitting diode: (see note 1)
DS710	48-84404E04	green
DS807	48-88245C28	red
DS808 thru 811	48-88245C29	green
DS812, 813	48-88245C30	yellow
DS817	48-88245C28	red
		fuse:
F701	65-139764	3 amp; 32 V
		connector, jumper:
JU1A	9-84728L01	2-contact; female jumper plug (service jumper)
JU1	28-84729L02	3-contact; male PCB header
JU2 thru 6	—	wire staple (see diagram jumper table)
JU7A	9-84728L01	2-contact; female jumper plug (PL-DPL ckt.)
JU7	28-84729L02	3-contact; male PCB header
JU8A	9-84728L01	2-contact; female jumper plug (+5 V dc ckt.)
JU8	28-84729L02	3-contact; male PCB header
JU9 thru 13	—	wire staple (see diagram jumper table)
JU14A	9-84728L01	2-contact; female jumper plug
JU14	28-84729L02	3-contact; male PCB leader
		connector, receptacle:
J701	28-82984N13	6-contact; male (DC power)
J800	28-10586A10	40-contact; male (Mux bus)
J801	28-83136N01	26-contact; female (radio interface)
J804	28-83136N01	26-contact; female (remote control)
J812	9-83112N01	6-contact; female (CONTROL)
		coil, rf:
L701	24-82380N01	69 turns; toroid
L702	25-82786N01	choke; bar core
L703	24-83977B01	choke; 1.5 turns
L801	24-82415N02	choke; 10 mH
L802	24-83397L01	choke; 30 uH
		transistor: (see note 1)
Q701	48-869829	PNP; type M9829
Q702	48-869328	PNP; type M9328
Q703, 704	48-869643	PNP; type M9643
Q705	48-869528	NPN; type M9528
Q706	48-83875D05	SCR; type M7505
Q801	48-869642	NPN; type M9642
Q802	48-869528	NPN; type M9528
Q803	48-869648	NPN; type M9648
Q804	48-869528	NPN; type M9528
Q806	48-869648	NPN; type M9648
Q807, 808	48-869919	FET, P-channel; type M9919
Q809, 810	48-869648	NPN; type M9648
Q812	48-869528	NPN; type M9528
Q1506 thru 1510	48-869642	NPN; type M9642
		resistor, fixed chip; ±5%; 1/8 W: (see note 2) unless otherwise stated
R701	6-11024B04	180k
R702	6-11024A91	56k
R703	6-11024A75	12k
R704	6-11024A81	22k
R705	6-11024A59	2.7k
R706	6-11024A63	3.9k
R707	6-11009A71	8.2k
R708	6-11024A47	820
R709	6-11024A61	3.3k
R710	6-11045A37	330; 1/2 W; conventional
R711	6-11024A55	1.8k
R713	6-11024A71	8.2k
R714	6-11024A99	120k
R715	6-11024A59	2.7k
R716	6-11024A43	560
R717	6-11024A25	100
R718	6-11024A63	3.9k
R719	6-11024A10	24
R720	6-11024A33	220
R721	6-124B55	2.7; 1/4 W; conventional
R722	6-11024A73	10k
R723	6-11024A71	8.2k
R724	6-11024A81	22k
R725	6-11024B22	1 meg
R727	6-11024A39	390
R728	6-11024A63	3.9k
R729	6-11049C22	1.91k ±1%; 1/4 W; conventional
R730	6-11049C26	2.1k ±1%; 1/4 W; conventional
R731 thru 734	6-125B70	1; 1/2 W; conventional
R735	6-11024A25	100
R736	6-11024A39	390
R737	6-11024A47	820
R738	6-11024A17	47
R739	6-11009E33	220; 1/4 W; conventional
R740	6-124B55	2.7; 1/4 W; conventional
R801	6-11024A53	1.5k
R802, 803, 804	6-11024A73	10k
R805 thru 812	6-11024A69	6.8k
R813, 814, 815	6-11024A73	10k
R816, 817	6-11024A61	3.3k
R818	6-11024A49	1k
R819	6-11024A97	100k
R820	6-11024B04	180k
R821	6-11045A23	82; 1/2 W; conventional
R822	6-11024A47	820
R823	6-11024A77	15k
R824	6-11024A17	47
R825	6-11024A33	220
R826	6-11024A53	1.5k
R827	6-11024A97	100k
R828	6-11024B01	130k
R829	6-11024A97	100k
R830	6-11024A97	100k
R831	6-11024A97	100k
R832 thru 836	6-11024A29	150
R837	6-11024A29	150
R838, 839	6-11024A73	10k
R840	6-11024A53	1.5k
R841	18-83686N03	variable; 50k; conventional (receive audio level)
R842	6-11024A97	100k
R843	6-11024A96	91k
R844	6-11024A91	56k
R845	6-11024A81	22k
R846, 847	6-11024A97	100k
R848	6-11024A93	68k
R849	6-10621D84	90.9k ±1%; conventional
R850	6-10621D78	78.7k ±1%; conventional
R851	6-10621D88	100k ±1%; conventional
R852	6-10621E04	143k ±1%; conventional
R853	6-10621D80	82.5k ±1%; conventional
R854	6-11024A61	3.3k
R855	6-11024B18	680k
R856, 857	6-11024A97	100k
R858	6-11024A97	100k
R859 thru 863	6-11024A73	10k
R864	6-11024A88	43k
R865	6-11024A83	27k
R866	6-11024A88	43k
R869	6-11024A53	1.5k
R872	6-11024A83	27k
R873	6-11024A53	1.5k
R874, 875	6-11024A89	47k
R876	18-82787K09	variable; 5k; conventional (VOLUME)
R877	6-11045A35	270; 1/2 W; conventional
R878, 879	6-124B55	2.7, 1/4 W; conventional
R880	6-11024A73	10k
R881	6-11024A43	560
R882	6-11024A61	3.3k
R883	6-11024A41	470
R884	6-11024A59	2.7k
R885	6-11024A79	18k
R886	6-11024A85	33k
R887	6-11024A83	27k
R888	6-11024A73	10k
R889	18-83686N05	variable; 5k; conventional (IDC-deviation level)
R890	6-11024A85	33k
R891	6-11024A69	6.8k
R892	6-11024A53	1.5k
R894	6-11024A93	68k
R895	6-11024A83	27k
R896	6-11024A79	18k
R897	6-11024A73	10k
R899	6-11024A83	27k
R1523	6-11024A89	47k
R1524	6-11024A61	3.3k
R1525	6-11024A87	39k
R1526	6-11024A57	2.2k
R1527	6-11024A87	39k
R1528	6-11024A73	10k
R1529	18-83686N01	variable; 100k; conventional (remote squelch level)
R1530	6-11024A73	10k
R1531	18-82787K08	variable; 100k; conventional (SQUELCH)
R1532	6-11024B02	150k
R1533	6-11024A39	390
R1534	6-11024A53	1.5k
R1535	6-11024A89	47k
R1536	6-11024B06	220k
R1537	6-11024A89	47k
R1538	6-11024A61	3.3k
R1539	6-11024A31	180
R1540	6-11024A89	47k
R1541	6-11024A39	390
R1542	6-11024A59	2.7k
R1543	6-11024A97	100k
R1544	6-11024A49	1k
R1545	6-11024A93	68k
R1546	6-11024A49	1k
R1547	6-11024A73	10k
R1548	6-11024B08	270k
R1549	6-11024A69	6.8k
R1550	6-11024A49	1k
R1551	6-11024A67	5.6k
R1552	6-11024A49	1k
R1553	6-11024A93	68k
R1554	6-11024A95	82k
R1555, 1556	6-11024A73	10k
R1557	6-11024B02	150k
R1558	18-83686N01	variable; 100k; conventional (repeater squelch level)
R1559	6-11024A39	390
R1560	6-11024A53	1.5k
R1561	6-11024A89	47k
R1562	6-11024B06	220k
R1563, 1564	6-11024A89	47k
R1565	6-11024B02	150k
R1566	6-11024A49	1k
R1567	6-11024A69	6.8k
R1568	6-11024A49	1k
R1569	6-11024A73	10k
R1570	6-11024A49	1k
R8100	6-11024A77	15k
R8101, 8102	6-11024A83	27k
R8103, 8104	6-11024A83	27k
R8105	6-11024A73	10k
R8106	6-11024A83	27k
R8108	6-11024A53	1.5k
R8109	6-11024A49	1k
R8111	6-125B61	4.7; 1/2 W; conventional
R8112	6-11024A73	10k
R8113	6-11024A69	6.8k
R8114	6-11024A91	56k
R8115	6-11024A61	3.3k
R8116	6-11024A65	4.7k
R8117	6-11024A69	6.8k
R8118	6-11024A73	10k
R8119	6-11009A49	1k; 1/4 W; conventional
R8120, 8121	6-11024A73	10k
R8122	6-11024A29	150
R8123 thru 8127	6-11024A73	10k
R8128 thru 8131	6-11024A89	47k
R8132	6-11024A69	6.8k
R8133	6-11024B11	360k
R8134	6-11024A65	4.7k
R8135	6-11024A65	4.7k
R8136	6-11024A01	10
R8137	6-11024A86	36k
R8138, 8139	6-11024A98	110k
R8140	6-11024A47	820
R8142	6-11024A73	10k
R8143	6-11024A10	24
R8144 thru 8145	6-11024A73	10k
R8146	6-11024A61	3.3k
R8147	6-11024A73	10k
R8148	6-11024A89	47k
R8149	6-11024A65	4.7k
R8150	6-11024A71	8.2k
R8151	6-11024A49	1k
R8152	6-11024A25	100
R8153	6-11024A10	24
R8154	6-11024A33	220
R8155	6-11024A59	2.7k
R8156	6-11024A69	6.8k
R8157	6-11024A89	47k
R8158	6-11024A49	1k
R8159	6-11024A01	10
R8161	6-11024A33	220
R8162	6-11024A10	24
R8163, 8164	6-11024A33	220
R8165 thru 8171	6-11024A25	100
R8172	6-11024A29	150
		switch:
S801, 802	40-83685N01	spdt
		transformer, auto:
T801	25-83687N01	pri: leads 1 to 5; ref. 16 ohms ±10% sec: leads 1 to 3; load imp. 3.2 ohms ±5%
		integrated circuit: (see note 1)
U701	51-84371K74	quad comparator
U801	51-83625M66	microprocessor; type MC6803
U802	51-83627M03	octal tri-state latch
U805	51-82609M77	octal latch
U806	51-84561L11	dual monostable
U807, 808		
U809, 810		
U811		
U812, 813		
U814		
U818		
U820		
U821, 822		
U823		
U824, 825		
U826, 827		
U829		
U831		
U832		
U833, 834, 835		
U836		
U838		
U1550, 1551		
U1552		
VR701		
VR702		
VR1531 thru 1534		
Y801		

notes:

1. For optimum circuits must
2. Chip resistor AA are the tw following the resistor.