MOTOROLA INC.
Communications
Sector

TONE REMOTE CONTROL MODULE

MODEL TLN2421A (2-WIRE)
MODEL TLN2422A (4-WIRE)

1. GENERAL DESCRIPTION

Tone remote control (TRC) allows control of a base station from a remote location using a pair of wires (wireline) which need not have dc continuity. Control is accomplished using a tone remote control console that sends a sequence of control tones which are interpreted by the base station. A station function normally corresponds to a function tone of a predefined frequency. All function tones must be preceded by a high level guard tone (HLGT, usually 2175 Hz) which alerts the station for a sequence of one or more function tones. On non-duplex stations, receiver audio is muted when HLGT is detected so that there will be no interfering audio signals on the wireline when function tones are being received. Upon receipt of the function tone(s), the appropriate function(s) are executed by the station. An example might be the monitor function, which disables receiver PL; the monitor function tone frequency is usually designated 2050 Hz.

Figure 1 illustrates the sequence of tones involved in a line push-to-talk (LPTT) function. In such a case, the function tone must be defined as a transmit function on a certain channel (i.e., 1950 Hz is usually defined as the function tone for keying on channel 1). If a LPTT function tone is sent, the remote control console follows the function tone by a continuous low level guard tone (LLGT), which is at the same frequency as HLGT but at an amplitude 30 dB lower. LLGT is a pilot tone that is present, along with the transmitted audio, for the duration of the transmission. At the end of the transmission, the station de-keys after LLGT is no longer detected *and* there is no longer any high-level audio activity on the wireline. The station uses audio activity as a criterion for terminating the LPTT transmission because high levels of transmit audio can mask the LLGT signal and make it undetectable. Therefore, in order to avoid de-keying prematurely, the station will remain keyed until LLGT is not detected *and* the $\overline{\text{ACTIVITY}}$ signal on the TRC board is high (inactive). The $\overline{\text{ACTIVITY}}$ line on TRC is a signal to the microprocessor. This signal goes low (active) when audio is present on the wireline at a level of up to 10 dB below the average peak speech level (which is approximately equal to the HLGT amplitude).

During a LPTT function, the LLGT is removed from the transmitted audio by a notch filter on the TRC board. This notch filter is tuned to the guard tone frequency (usually 2175 Hz).

When not in the LPTT mode, the TRC board accepts receiver audio from the station control board, passes it through a notch filter (tuned to guard tone), and then through a line driver for transmission down the wireline to the remote console. The receive notch filter prevents false HLGT detection due to possible receiver audio components near guard tone frequency (since on a 2-wire board the receiver audio output and transmit audio/tone inputs are tied together at the wireline).

The TRC board is also capable of generating tones, which may be mixed with the receive audio for transmission down the wireline. In addition, a special test routine called "Tone Test" causes the TRC board to generate its own test tones for service and alignment.

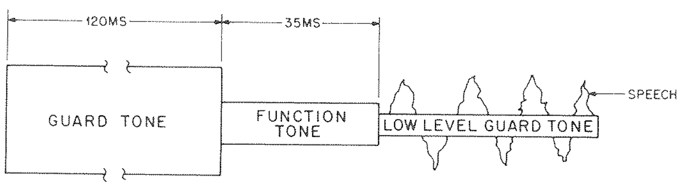


Figure 1. Tone Remote Control Signaling Format

The TRC board is microprocessor-controlled with customer specified features stored in a code plug. This affords a large degree of flexibility in defining function tone frequencies without the cost or complexity of a separate, dedicated hardware decoder for each frequency.

2. AUDIO SECTION THEORY OF OPERATION AND TROUBLESHOOTING

2.1 GENERAL

Receiver audio is gated through the station control board and passed through a guard tone notch filter on the TRC board. This processed audio is then applied to the phone line. Transmit audio passes through a sample-and-hold AGC, then a guard tone notch filter before being routed to the station control board. The remote control tones are combined with the transmit audio prior to the notch filter. These tones are routed through the tone processing section to the MPU, U1008-8.

Measurement of voltage levels should be made at op-amp outputs, *never* on the (-) input pins. A complete list of voltage measurements using the internal tone test routine appears in subsequent paragraphs of this section.

2.2 RECEIVE AUDIO PATH

Audio from the receiver is gated by station control circuitry to J804-4, which mates with ribbon connector P1001-4 on the tone remote control board. Receiver audio passes through muting gate U1027A to audio filter U1023B. The receive audio signal should be visible on the HP (for high pass) and LP (for low pass) outputs of U1023B, with dc average level of V_B = 4.7 volts. Audio frequencies below 2175 Hz will appear at a higher level on the LP output than on the HP output, and conversely for audio signals above 2175 Hz. The HP and LP outputs should be 180° out of phase. The HP and LP outputs are summed into U1021-C to form a notch at the guard tone frequency. The notch output is U1021-8. Note that audio is normally *not measureable* on TP9. This test point is only used during filter alignment when receiver audio is muted. (See the filter alignment procedure.)

Receive audio muting is controlled by the microprocessor (MPU, U1008) through transistor switch Q1016, which controls muting gates U1027A and U1025D. When high-level guard tone is detected or a line LPTT is in progress, the receiver audio will be muted (Q1016 collector will be at ground potential) except when the C332 Full Duplex Option is ordered. If the receiver audio is not muted, it passes to the line audio shaping filter, U1021D, which has unity gain (input voltage equals output voltage) for frequencies below 3000 Hz. Tones generated by the MPU to be sent down the wireline sum into U1021C at a level (relative to receiver audio) determined by gates U1025A and U1025B. The tone output on U1021C-8 relative to receiver audio (±5 kHz deviation of 1 kHz tone) is approximately -3 dB when gate U1025A is on, -13 dB when U1025B is on, and (if JU29 is in) -30 dB when both U1025A and U1025B are off if the MPU (U1008) is toggling pin 9. Tones generated by the MPU are applied to the wireline whether receiver audio is muted or not. JU29 may be added in custom applications where low level guard tone must be encoded by the tone remote control board.

The output of the line audio shaping filter (U1021-14) is split into opposing phases in line driver where the receiver audio is applied to the line transformer and the phone line. On 2-wire tone remote control boards, the line driver audio is also applied to the input of the transmit audio/tone detection path through T1001-12. A portion of the line driver audio is fed into the input amplifier of the transmit audio/tone detection path, via JU26/R1154, out of phase with the receiver audio appearing on T1001-12. This is done in order to at least partially cancel the receive audio so that a tone from a control console may be more easily detected in the presence of receiver audio. On 4-wire boards JU26/R1154 should be out.

The receive guard tone notch filter may be bypassed, if desired, on 4-wire audio full duplex boards (in which the transmit and receive audio have separate lines) by removing R1120 (JU20) and installing R1148 (JU21).

For test purposes, audio from a signal source may be fed into the receive audio path between TP6 and audio ground (TP3) if foil jumper JU27 is cut (JU27 must be reconnected by soldering in a wire after testing is finished). The peak sine wave voltage applied to TP6 should be approximately 1 volt. At a frequency near guard tone (normally 2175 Hz) the audio will be attenuated by the notch filter. However, at other frequencies between 300 and 3000 Hz, the audio should pass from TP6 to the phone line. Note that the outputs of U1023B (pins 18, 19, 20) and U1021-8 normally appear noisy due to the high frequency switching nature of U1023. If the correct signal or dc levels do not appear at the outputs of U1023B (18-20), check U1023-11 to see that a 111.52 kHz clock signal is present. This clock signal should be a voltage swing of approximately 0.4 to 3 volts.

2.3 TRANSMIT AUDIO PATH

The input from the phone line is applied to U1018-2, along with the line driver audio cancelling voltage (described previously) via JU26/R1154. The gain of U1018D is controlled by FET transistor Q1011. The lower the dc gate voltage on Q1011, the higher the gain, since a more negative gate voltage tends to turn off the FET, creating maximum feedback resistance across U1018-2 to U1018-1. The voltage on U1018-2 is amplified by a factor of 20 by U1018B. The output of U1018B feeds the transmit guard tone notch filter via R1146

(JU18). In applications where this notch filter must be bypassed, R1146 (JU18) should be removed and R1147 (JU19) should be installed. The transmit notch is formed by summing the two outputs from U1023A in the same manner as the receive notch filter described previously. The output of the transmit notch appears on TP5, with gain controlled by R1056 (XMIT LEV). The setting of R1056 normally does not have to be changed from the factory setting because the sample and hold AGC compensates for any phone line loss, as described in the following paragraph.

The output of U1018B (pin 7) feeds the reference comparators of the AGC, U1022A, B, and C. If the peak voltage on TP11 exceeds the threshold of U1022B (+5.8 V) in the positive direction, the output of U1022B pulses high, causing current to pass through R1073 and charge C1034 through CR1012. Similarly, if the peak minimum voltage on TP11 dips below the threshold of U1022A (+3.6 V), U1022A will allow a pulse of current to charge C1034. As C1034 charges, the dc voltage on the gate of Q1011 rises, reducing the drain-source resistance and reducing the gain of U1018A, which in turn reduces the voltage level on TP11. This process continues until the voltage on TP11 is just equal to the threshold of U1022B minus the threshold of U1022A, which is 5.8-3.6 = 2.2 V P-P.

The "sample and hold" action of the AGC occurs when a new high-level guard tone is received. Upon detection of HLGT by the MPU (U1008), the AGC RESET bit (which had been low when no line push-to-talk was preset) goes high. After approximately 6 msec., the Tone Detect line goes high, causing the gain of the FET to rapidly increase (as a discharged C1035 is placed in parallel with the smaller C1034, reducing the gate voltage on Q1011), and also turning off Q1010 to allow a higher gain in U1018D stage. This causes a momentary rise in the ac voltage level on TP11 above the usual compression point of 0 dBm, as shown on the schematic diagram. During the time that the peak voltage on TP11 is more than 0.7 V higher than the 1.1 V peak (0 dBm) threshold, comparators U1022C and Q1009 are actuated to provide faster than normal attack (gain reduction) time. In this manner the gain is always reset to maximum at the beginning of a new line push-to-talk, then reduced as necessary until HLGT is at 0 dBm (which is the AGC compression point) as measured on TP11. This assures full deviation regardless of the amplitude of any audio signal on the line just prior to the line push-to-talk.

During LPTT, the auto level control ALC action of the AGC causes the gain to freeze for input audio levels below approximately -10 dB relative to the average peak speech level. This preserves the natural characteristics of speech without any pumping effect characteristic of some other AGC circuits. Such pumping may be audible in intercom operation during servicing. The AGC gain is frozen during line push-to-talk if the ACTIVITY line is high. When a signal in the range of approximately 0 to -10 dBm is present on TP11, U1020A amplifies the signal sufficiently to trigger U1022D and cause the ACTIVITY line to remain low, allowing C1034 and C1035 to discharge through R1093 and very slowly increase the gain. When the input signal is below this range the ACTIVITY line remains high. The ACTIVITY line is also used by the MPU (U1008) as one of the signaling criterion described previously.

The transmit notch filter tuning is factory adjusted and should not normally require field adjustment. It may be realigned using internally generated guard tone or by injecting a guard tone frequency signal on the wireline. If the latter is done, TP10 should be temporarily grounded to TP14 on the tone remote control board to prevent the MPU from resetting AGC gain due to HLGT detection. With the guard tone signal applied to the L1 line terminals (from the remote console, for example), R1058 should be adjusted for minimum guard tone signal on TP5 of the tone remote control board. This will result in maximum guard tone frequency rejection in the transmit audio during CPTT.

When not in a LPTT mode, the AGC circuit has rapid attack and decay times. Therefore, if an audio signal is applied to the L1 phone line terminals at a level of -5 dBm (.44 V rms) or higher, at a frequency other than guard tone (a good choice is 1000 Hz), the ac voltage level on TP11 should be 0 ± 1 dBm. The signal should also be observable at the output of the transmit notch filter on TP5 at a level determined by the XMIT LEV (R1056) setting, typically around 450 mV rms. If no signal is observed on TP11, the dc voltage should be verified as approximately 4.7 V. Also, the dc voltage on C1034 should be near zero, to keep FET Q1011 off and allow maximum gain in the U1018D stage. If C1034 is found to have a positive dc voltage on it when there is no signal on TP11, the operation of comparators U1022A, B, and C should be checked. If C1034 voltage is correct (0 V), and a signal cannot be obtained on TP11, remove the drain or source lead of Q1011. If the signal now appears, replace Q1011. If the 1000 Hz signal is present on TP11 but not on TP5 (and R1056 is *not* fully counterclockwise), check the HP and LP outputs of U1023A (the outputs normally appear noisy). The 1 kHz signal should be visible with a dc average level of V_B = 4.7 V. If the 1 kHz signal is not visible there, check the clock signal on U1023A-10. The clock should be 111.52 kHz (for 2175 Hz guard tone), swinging from approximately 0.4 to 3 volts.

3. TONE PROCESSING SECTION

Inputs to this section originate from TP11 (the output of U1018B) in the transmit audio path. When looking for guard tone (during standby), the audio routed through the guard tone bandpass filter is selected by gate U1027C and applied to the limiter. When looking for function tone (after HLGT is detected), U1027C applies unfiltered audio to the limiter. The limiter consists of a gain stage (U1020C) which also provides some broad band filtering, followed by a limiter stage that converts the signal to a square wave. The output of U1020D drives transistor Q1005, which provides an input to the MPU U1008 (pin 8). The input to U1008 is a square wave which swings from 0 to 5 V. During LPTT, U1027C continually switches between audio from TP11 and audio from the bandpass filter.

The tone processing section also contains a clock divider for U1023 and U1024 (bandpass and notch filters). These IC's require a high-frequency clock input that is derived from the MPU "E" clock. The input to U1014 (pin 2) should be a 1.2267 MHz square wave, and the output of the divider (U1014 pin 11) should be a 111.52 MHz square wave with jumpers set for 2175 Hz guard tone (normal value).

In addition to sending receiver audio down the wireline, the tone remote control board has the capacity to generate tones and apply them to the wireline as well. This may occur for example, in the line loop test routine (which is an optional feature) where the tone remote control board responds to a pre-defined wireline (function tone) command by generating a 1004 Hz tone for 6.8 seconds to enable an operator at the remote control console to check phone line operation. Tones are generated by the MPU U1008 and appear on pin 9 as a square wave. This signal passes through the tone encode filter consisting of U1020B and U1018A. This circuit filters the square waves generated by the MPU until they are approximately sinusoidal. The output of the tone encode filter is applied to the line driver where it may be mixed with receive audio (if the receive audio gates on tone remote control are not muted) and applied to the wireline.

4. DIGITAL CONTROL AND DISPLAY SECTION THEORY OF OPERATION

4.1 MPU DESCRIPTION

The tone remote control module uses a Motorola MC6803 MPU, programmed to operate in Mode 2, which has multiplexed data/addresses (lower order), external interrupt vectors, internal random-access memory (RAM), and a 4.9068 MHz crystal-controlled clock source, but no internal read-only memory (ROM). The MPU operating mode is determined by the inputs at ports P20 through P22 (pins 8 through 10 of U1008). With a diode in the circuit for a particular port, its input bit is translated as a logic 0 on the trailing edge of the $\overline{\text{RESET}}$ pulse at U1008-6. Without a diode and by using a pull-up resistor to +5 V, a mode input bit is interpreted as a logic 1 on the $\overline{\text{RESET}}$ pulse trailing edge. Therefore, with diodes in for P22 and P20, but out for P21, the MPU is configured for mode 2 operation. Refer to MC6801 8-Bit Single-Chip Microcomputer Reference Manual MC6801RM(AD) for more detailed information. Ports 1 and 2 of the MPU are used for various input and output (I/O) signals. Port 3 is dedicated to multiplexed data (D0-D7) and low-order address bits (A0-A7). Port 4 is dedicated to the high-order address bits. Key control signals are described in the following paragraphs. The particular applications of the MPU's I/O lines are shown on the schematic diagrams at the end of this section. More detailed electrical specifications for these lines are available in the MC6801 Microcomputer Reference Manual MC6801RM(AD).

4.2 CONTROL INPUT/OUTPUT PINS

4.2.1 Read/ $\overline{\text{Write}}$ (R/ $\overline{\text{W}}$), pin 38

The R/ $\overline{\text{W}}$ output strobe is an active low pulse that is generated for an MPU read or write to the Port 3 data register in the MPU, depending upon the MPU's control configuration. The R/ $\overline{\text{W}}$ pulse, approximately one E-cycle wide (that cannot be varied), is used for memory map decoding and as a strobe input to the code plug in some applications.

4.2.2 Address Strobe (AS), pin 39

The AS (address strobe) output is used as a Latch Enable (LE) input for Address Latch (Low-Order) U1009. Low order address bits (A0-A7) are latched into U1009 from the DATA bus on the falling edge of the address strobe.

4.2.3 Enable (E), pin 40

The E signal is the primary MPU system timing signal and synchronizes all DATA bus transfers. An MPU E-cycle (or bus cycle) consists of a negative half-cycle of E followed by a positive half-cycle. The data bus is active only while E is high or, equivalently, during $\overline{\text{E}}$. The E signal is inverted to provide $\overline{\text{E}}$, the required enable input to the program EPROM (U1012) and code plug (U1011), and to clock the IPCB input flip-flop (U1004B).

4.2.4 IPCB OUT, pin 12, IPCB IN, pin 11

These pins provide the serial communication transmit (IPCB OUT) and receiver (IPCB IN) lines of the MPU. They are connected to the bidirectional Interprocessor Communications Bus (IPCB) via the IPCB buffer circuit.

4.2.5 MUXbus $\overline{\text{IRQ}}$, pins 5 and 16 (P13)

The MUXbus $\overline{\text{IRQ}}$ (MUXbus interrupt request) input to the MPU is generated upon receipt of the $\overline{\text{DS}}$ (data strobe) signal from the station control module. The MUXbus interrupt request informs the tone remote control MPU that valid MUXbus data is contained in the MUXbus read data buffer and the buffer is ready to be serviced. During power-up diagnostics, the MUXbus interrupt request is read through pin 16 (P13) of the MPU.

4.2.6 INTERCOM/AGC INHIBIT, pin 13 (P10)

Pin 13 (P10) of the MPU serves as both an input and an output function. The INTERCOM switch (S1002) provides a high (OFF) or low (ON) input that is polled by the MPU once every millisecond to determine the status of the line. If the INTERCOM switch is on, the corresponding MUXbus bit (BD0) will be activated. If the switch is off, the bit will be turned off. When the tone remote control board is polled by the station control module, switch status is transmitted to the station control module via the MUXbus.

The AGC INHIBIT output from the MPU is applied to the automatic gain control circuit in the audio section to inhibit AGC operation when internally generated tones are applied to the wireline. This prevents the AGC circuit from reducing the gain in the transmit audio path during this interval.

4.2.7 ACTIVITY, pin 15 (P12)

The ACTIVITY input to the MPU is provided by the activity detector in the audio section and informs the MPU of the presence or absence of audio in the transmit audio (Tx AUDIO) signal path. The ACTIVITY input is high when no audio is detected and low when audio of sufficient level is present. When the ACTIVITY input is low it maintains a wireline push-to-talk in the presence of high level transmit audio signals, which may clock out the low level guard tone.

4.3 MICROPROCESSOR CONTROL BUS SIGNALS

Port 3 consists of P30 through P37 (pins 37 to 30 of U1008) and is used for the multiplexed low-order address bits and data bits D0-D7. Thus, depending upon the internal MPU programming control, port 3 will output the eight low-order address bits or port 3 will provide or accept eight bits of data via the DATA bus. Port 4 consists of P40 through P47 (pins 29 to 22 of U1008) and is dedicated to the high-order address bits. That is, port 4 will not accept inputs, being used only to output the eight higher order bits or any particular address.

4.4 WATCHDOG TIMER DESCRIPTION

When the MPU (U1008) is operating properly, it outputs tickle pulses to the watchdog timer (WDT) on pin 10 that are characterized by a given periodicity, as shown on the waveform for normal operation on the schematic and listed in Table 1. The watchdog timer circuit monitors this period and, if the pulses are not within a predetermined range (i.e., timing window), the watchdog timer circuit resets the MPU. At the same time, it prevents other circuits from experiencing any ill effects of a MPU control section malfunction by holding them reset until the MPU is again operating properly.

Monostable multivibrators (MSMV) U1016A and U1016B are used to set the tickle-pulse period range by forming a window in which the pulse must occur. In normal operation, U1016A is kept retriggered by the negative-going edge of the MPU tickle pulse. The U1016A time constant determines the maximum allowable tickle period. If tickle pulses occur too far apart, U1016A times out, and generates a reset pulse through U1016B and Q1014. The U1016B time constant determines the minimum allowable tickle period. If tickle pulses occur too close together, the normal output from U1016B allows the "too-early" tickle pulse through NAND gate U1015B to clear MSMV U1016A, which again causes a reset pulse to be generated by U1017B and Q1014.

The MPU reset occurs in the following manner. Retriggerable monostable multivibrator (MSMV) U1017B generates a WD RESET pulse whose duration is determined by its time constant (established by C1013 and R1023). This occurs when the A input at pin U1017-9 goes active (low) as a result of missing or improper tickle pulses from MPU U1008, which indicates improper MPU operation. As part of the reset procedure, the B input (pin 10) of U1017B goes inactive (low) through the action of Q1006 being turned on by the Q output from U1017B. With the B input of U1017 inactive, the MPU has time to sequence through its startup routines and begin outputting tickle pulses; the first

Table 1. Timing Parameter Chart

Parameter	Description	Timing Range	Average	Units
t_W	Watchdog Timer Tickle Period	35-71	52	ms
t_{WDP}	Watchdog Timer Tickle Pulse Width	20-1300	170	uS
t_1	MSMV U1016A Time Constant	89-214	135	ms
t_2	MSMV U1016B Time Constant	9-21	14	ms
t_{WND}	Window Width (t_1-t_2)	68-205	121	ms
t_3	MSMV U1017B Time Constant	2.5-4.5	3.5	ms
t_4	MSMV U1017A Time Constant	490-1389	800	ms
t_5	Astable Time Constant (C1014, R1019)	14-230	40	ms

tickle pulse should occur about six milliseconds after the trailing edge of the RESET pulse. However, if no tickle pulse occurs, the A input remains active and another RESET pulse is generated when the charging circuit C1014-R1019 reaches the MSMV triggering level at the B input of U1017B. This astable operation will continuously attempt to reset the MPU as long as improper tickling occurs. Note that the tickle line of the MPU (U1008-10) is pulled low by CR1002 each time the MPU is reset. Such a sequence should not be confused with the normal tickle pulse waveform, which is a train of narrow positive pulses spaced approximately 52 msec. apart (see waveform on schematic). When the MPU properly outputs a tickle pulse after being reset, the A input for U1017B goes inactive (high) and prevents any additional RESET pulses from occurring due to the astable operation of U1017B.

An external reset function for the watchdog timer circuit is incorporated in the following manner. As long as the EXPANSION RESET signal is held active (low), U1017B will be held reset by U1017-11 "R" input. Furthermore, the MPU will be held in a reset condition by the action of NAND gate U1015C. The high output of U1015C enables the delayed reset MSMV U1017A which is retriggered by the E signal at pin 1. The EXPANSION RESET signal is also used to clear MSMV U1016B, so that when the WDT tickle signal floats high through R1004 immediately following a reset, another reset does not occur due to a low output from U1015.

The DELAYED RESET and DELAYED RESET outputs from U1017A are used to hold other circuits of the digital control and display, audio, and tone processing sections inactive until the MPU properly tickles the WDT circuit and astable operation has ceased. The time constant for U1017A is such that the delayed reset signals are active long enough to guarantee that two proper tickle pulses will occur after the final RESET to the MPU (a single tickle pulse could be the result of a MPU malfunction). During an EXPANSION RESET from another board, U1015C keeps U1017A retriggered so that it cannot time out early.

4.5 RESET ARBITER DESCRIPTION

The reset arbiter circuit performs two functions. First, the MPU can generate a REMOTE RESET signal without resetting itself. When the REMOTE RESET signal at U1008-19 switches low, the low is applied directly to U1015A-2 before a high signal propagates to U1015A-1 via Q1008, Q1007, and U1007F. Therefore, U1015A-3 remains high and no EXTERNAL RESET signal occurs. When the REMOTE RESET signal switches high, U1015A-3 switches momentarily low until a low signal propagates to U1015A-1. This low signal is short enough, however, that capacitor C1009 cannot charge up to a logic high level and therefore, no EXTERNAL RESET signal occurs. Second, when a reset command, generated externally to the tone remote control board, is received, the reset arbiter circuit produces an MPU reset. This is accomplished since the inactive state of the REMOTE RESET signal allows the EXPANSION RESET signal through NAND gate U1015A to become the EXTERNAL RESET signal. The EXTERNAL RESET generates a MPU reset as described previously, and can occur due to RESET from the remote control connector. The EXTERNAL RESET signal may originate on the station control board, or on another board connected to station control through the expansion bus connector (see station control section).

4.6 MEMORY DEVICES DESCRIPTION

The main executable code for the tone remote control board is stored in program EPROM U1012, (an 8k × 8 EPROM). U1012 contains the operating program for the board. It interacts with the personality data stored in code plug U1011, and reacts to inputs from the MUXbus and tone commands from the wireline. New versions of the Tone Remote Control Software, TRN5186A, may be developed and be shipped as new features, not currently available, are added to the design. When a new version becomes available, a new part number will be assigned although the kit number, TRN5186A, will be unchanged. In some cases the new version of software may require an updated version code plug, TRN5190A, to operate.

Failure to update the TRC code plug when installing a new TRC software ROM may result in a code plug error at power-up. Always order a new code plug (U1011) from the factory, or have the old code plug reprogrammed on a Motorola R-1800A Digital Analyzer/ Controller whenever replacing the software ROM with a part number different from the original part number. This will ensure that the software and code plug versions are compatible.

The other memory device for the processor section is code plug U1011, which stores the tone remote control module configuration (personality) data. It is a 4k × 8 EPROM device. Table 2 gives the memory locations of these devices and provides a memory map of all other tone remote control functions.

4.7 ADDRESS LATCH DESCRIPTION

The address latch (U1009) is used to hold the low-order address bits from the multiplexed address/ data lines output at port 3 of the MPU. Latch U1009 is transparent (i.e., passes a signal as if it were not there) while the Latch Enable (LE) input is high. The LE signal is the ADDRESS STROBE (AS) signal from the MPU, and when the AS signal goes low (inactive), the address bits are latched into U1009. The address lines of U1009 are output to the ADDRESS/CONTROL bus, forming part of the total address used to control the various parts of the processor section.

Table 2. MSF 5000 Tone Remote Control Memory Map

Name	Type	Software Address Used	Comments
Internal Registers	R/W	$0000-$001F	—
External Memory	—	$0020-$007F	Unused — See Code Plug
Internal RAM	R/W	$0080-$00FF	—
External Memory	—	$0100-$1FFF	Unused — See Code Plug
Code Plug	R	$2000-$2FFF	Hardware Allows Use of $0000-$3FFF
I/O Devices*	R/W	Defined as Follows	Hardware Allows Use of $4000-$7FFF
Bus Read Data Buffer	R	$59FF	A13 • IOR
MUXbus Latch	W	$69FF	IOW
Hardware Latch	W	$71FF	A11 • IOW
System ROM	R	$C000-$DFFF	Hardware Allows Use of $8000-$FFFF
Internal ROM Space	—	$F800-$FFEF	Unused
External Vectors	R	$FFF0-$FFFF	$DFF0-$DFFF Used to Read Software $FFFF-$FFFF
*Undefined I/O Devices	R/W	$79F0-$79FF	Address, as shown will not select a device

NOTE: The symbol "$" preceding any alphanumeric character(s) means that the character(s) are HEX coded.

4.8 ADDRESS DECODING DESCRIPTION

The Input/Output Read (IOR) and input/output write (IOW) are two control signals that are generated by the memory map decoder circuits to allow selection of I/O devices in the processor section. The IOR signal provides an enable for the group of I/O devices that the processor reads (i.e., obtains data from), while the IOW signal provides an enable for the group of I/O devices to which the processor writes (i.e., passes data to). The control signals and addresses used for I/O device selection are listed in the station control board memory map chart of Table 2.

4.9 HARDWARE LATCH DESCRIPTION

The MPU writes eight different control signals to the hardware latch (U1013). The function of each control signal is discussed elsewhere in this section.

4.10 CHANNEL SELECT SWITCH

S1001 selects the station operating channel when the Access Disable switch on the station control module is activated. The four outputs from the switch are connected to the command service buffer IC (U813) on the station control module. The MPU on the station control module reads the switch outputs and selects the station operating channel.

4.11 MUXbus WRITE LATCH DESCRIPTION

This latch (U1002) holds information that will be written to the station control connector (P1001) by the processor section. The four outputs are routed through open-collector inverter buffers to become the multiplexed write-data corresponding to the current bus address.

4.12 MUXbus READ DATA BUFFER DESCRIPTION

Four inputs (BA0-BA3) to buffer U1001 provide address information while the remaining four are used to read the multiplexed bus-data bits (BD0 through BD3) that are present at the station control connector. See the station console module section of this manual for a more complete discussion of MUXbus operation.

4.13 FRONT PANEL INDICATORS DESCRIPTION

The light-emitting diodes (LED's), used as indicators on the front panel of the tone remote control module are color-coded according to their function. The red (test) LED indicates a failure or servicing status.

IMPORTANT

Stations should not normally be returned to operation after service while any red LED is on.

5. MAINTENANCE AND TROUBLESHOOTING

5.1 GENERAL

In order to operate a tone remote control board, it must be connected to a working station control board. For dc power connections to the station control board when operating outside a station, refer to the Station Control Module section. The tone remote control board is capable of generating its own test tones using a routine called tone test, described elsewhere in this section. These test tones may be used to align and troubleshoot the tone remote control board, and may also be used as a general purpose audio signal source for troubleshooting other boards.

5.2 SELF DIAGNOSTIC ROUTINES

5.2.1 General

The tone remote control board features self-diagnostic routines that make it possible to troubleshoot the digital circuits with standard bench test equipment (e.g., oscilloscope) in most cases. The board is equipped with a self-diagnostic routine that it performs where the station is first powered up, or whenever the ACC DIS/TEST switch (on the front panel of the station control module) is put into the TEST position. The routine checks the integrity of MPU U1008, program EPROM U1012, Code Plug U1011, the MUXbus read/write circuits, and the serial port (IPCB) read/write circuits, in that order. If any of these basic blocks fail the self test, the MPU flashes the TEST LED repeatedly, a specified number of times (one, two, three, or four times), to indicate the failure that was discovered. It then waits about 1.5 seconds and resets the board by failing to tickle the watchdog timer circuit. Refer to the watchdog timer paragraphs in this section of the manual. When the watchdog circuit resets the board, the TEST LED flashes once, with a flash that is shorter than the failure indication flashes. After the watchdog timer resets the board, the diagnostic routine is repeated. If the board fault remains unchanged, the routine locates it again, flashes the TEST LED, and resets the board again. The result is that the board sends a sequence of flashes, a short flash, another sequence of flashes, a short flash, etc. The interpretation of the TEST LED indications is given in the self-diagnosed failures paragraphs in this section of the manual. Note that on a properly running board, the TEST LED should not light after power-up reset.

The tone remote control board has its own TEST LED which is different from that on the station control board. If the station control TEST LED indicates a problem on that board, then the tone remote control TEST LED will probably also be lit since if the MUXbus (which is run by station control) is not operating, tone remote control will not pass the MUXbus power-up diagnostic routine. Generally, if both TEST LEDs are on, the problem probably lies on the station control board. This may be verified by disconnecting the ribbon cable between the two boards (from J804 on station control) to determine if the TEST LED on station control goes out without tone remote control connected. The station control board should be capable of running with or without the tone remote control board connected.

The tone remote control board may fail in such a way that the program routines cannot be run, including the power-up self diagnostic routine described previously. This indicates a major digital circuit failure. The watchdog circuits aid in determining these failures, yet keep the tone remote control board from interfering with station operation until the program routines are again running correctly. When this type of failure occurs, the TEST LED is on steadily, or else flashing at a rapid rate (many times per second). Troubleshooting this type of failure is described in the watchdog reset failure paragraph in this section.

Another possible failure is associated with EXPANSION connector J800, termed Expansion Reset failure. The expansion drive circuits on the station control board work with a limited total length of flat cable and a limited number of external modules (including any remote control board). If a capacitive load in excess of 288 picofarads, including the capacitance of the flat cable and all integrated circuit loads, is attached to the Expansion Reset line, the station control board may reset at the end of the power-up self-diagnostic routine. This would result in a series of short flashes on the station control TEST LED spaced about 2 seconds apart, and would keep the tone remote control TEST LED on continuously. See the Station Control Module section for further details.

5.2.2 Watchdog Reset Failure

This type of board failure is indicated when the TEST LED is on steadily, or else flashing at a rapid rate (many times per second). When this major digital circuit failure indication is seen, the following procedure should aid in finding this failed circuit.

Step 1. Use an oscilloscope in the dc coupled mode of operation to look at the signal at the reset (RES) pin of the MPU, U1008-6. The normal signal at this pin is always high. A series of low pulses, of 2 milliseconds duration, approximately, occurring every 10 milliseconds to 250 milliseconds, indicates a type of reset caused by the MPU watchdog circuit when it finds a fault in the series of MPU tickle pulses. If this type of signal is present at U1008-6, proceed to Step 2. If the signal at U1008-6 is always low, the fault is probably in the reset arbiter circuits, proceed to the reset arbiter paragraphs in this section of the manual.

Step 2. Look at the signal at the watchdog tickle (WDT tickle) pin of the MPU, U1008-10. The signal should be high during the short reset pulse. The signal should switch low within 10 milliseconds of the time that reset pin U1008-6 switches high. After this point, a high pulse should occur approximately every 53 milliseconds. If the WDT tickle signal does not switch low after the reset pulse, this indicates that the board is failing at the beginning of the self-diagnostic routine. The board fault is probably in one of four areas: either MPU U1008 is faulty, program EPROM U1012 is faulty, Address Latch U1011 is faulty, or there is a short circuit on one of the MPU address or data lines. Proceed to Step 6. If the U1008 WDT tickle signal does go low after the reset signal, then either the WDT tickle signal pulses are not spaced properly (approximately 53 milliseconds apart), or there is a failure in the watchdog timer circuitry. To troubleshoot this type of failure, proceed to Step 3.

Step 3. When WDT tickle pin U1008-10 goes low, U1016-13 should switch high, making U1017-9 high. Look for these signals to occur before proceeding. If they do not, look for some fault causing this malfunction.

Step 4. Check the signal at U1016-5. It should go high when WDT tickle pin U1008-10 goes low, and stay high for approximately 9 to 21 milliseconds, and then switch low until the WDT tickle signal switches from high to low again. If the WDT tickle signal goes high sometime before U1016-5 goes low, then both pins U1015-4 and U1015-5 are high making U1015-6 low. This will reset the MPU via U1016A and U1017B. This action indicates that the self-diagnostic routines are not running properly. Proceed to Step 7.

Step 5. Check U1016-13 again. If this pin is staying high for more than 80 milliseconds before switching low, this indicates that the self-diagnostic routines are not running properly. Proceed to Step 7.

Step 6. Look at the E (Enable) pin U1008-40. The signal on this pin should be a square wave that is low for 408 nanoseconds and high for 408 nanoseconds. If this signal is not present, or has the wrong duty-cycle, check the supply lines to the MPU and the connections to crystal Y1001 and capacitors C1001 and C1002. If all these connections are correct and the proper signal is not present, replace MPU U1008.

Step 7. Look at Address Strobe (AS) pin U1008-39. The signal on this pin should be a square wave that is high for 200 nanoseconds and low for 600 nanoseconds. If this pin is not changing, or has the wrong duty-cycle look for a short circuit on the line. If there is no short, either MPU U1008 or Address Latch U1008 is defective.

Step 8. Look at: the High-Order Address pins U1008-22 through -29; the Low-Order Address pins U1009-2, -5, -6, -9, -12, -15, -16, and -19; and the data pins at U1008-30 through -37. If any of these pins are not changing state (are either always high or always low) look for a short circuit on that line.

Step 9. Look at MPU programming pin U1008-8 and U1008-10. When U1008-6 goes low, these pins should also be low. When U1008-6 switches high, the pins also switch high, momentarily. If these pins do not go low, check programming diodes CR1002 and CR1015. MPU U1008-6 can be forced low by putting S801 to the TEST position on the front panel, or by grounding TP6 to TP1 on tone remote control board.

Step 10. If none of the previous steps reveals a fault, then probably either Program EPROM U1012 or MPU U1008 is damaged and should be replaced. Return to Step 1.

5.2.3 Self-Diagnosed Failures

As on station control, certain tone remote control board faults are indicated by a series of 1, 2, 3, or 4 flashes of its TEST LED, followed in about 1.5 seconds by a short flash (the MPU resetting itself), followed about 4 seconds later by another series of 1 through 4 flashes, etc. This recurring pattern indicates that the self-diagnostic routine is running and is detecting a fault in the station control board circuits. The meaning of the different sets of flashes is as follows:

- One Flash —

  This indicates that either MPU U1008 or Program EPROM U1012 is defective and should be replaced.

- Two Flashes —

  This indicates that Code Plug U1011 is defective and should be replaced.

- Three Flashes —

  This indicates that the tone remote control board has detected a failure during the MUXbus test. The board first tests to see if the MUXbus address lines are cycling properly. A failure results if either the addresses are not cycling (a station control failure) or the tone remote board cannot read the lines properly. The board then tests whether it can read and write onto the MUXbus data lines. If this test is failed, check to see that the station control board is toggling the MUXbus address lines, BA0-BA3. Next, check to see that the DS signal from station control is reaching U1008 pin 5 through U1004A. Also check that the outputs of U1002 and U1001 are toggling.

- Four Flashes —

  This indicates that interprocessor communication bus (IPCB) signal on ribbon connector P1001 is not operating properly. The self-diagnostic routine determines this by writing a string of high and low levels to the IPCB and reading the string back. If the read and write circuits fail or if the IPCB line is shorted, the self-diagnostic routine indicates a failure. If station control passes the IPCB test, but tone remote control does not, the problem is isolated to circuits on the tone remote board between MPU U1008 and the IPCB line.

The self-diagnostic routine has another added feature to aid in troubleshooting the IPCB circuits when a fault is indicated. If TP8 is shorted to ground with a jumper, the self-diagnostic routine writes a series of alternating high and low levels to the IPCB line via IPCB Out pin of the

MPU, U1008-12. The line continues to switch from high to low indefinitely until the MPU is again reset. With this continuous signal coming from the MPU, the IPCB read and write circuits can be checked with an oscilloscope.

5.2.4 Reset Arbiter

The following procedure describes and examines faults that are indicated when reset pin U1008-6 of the MPU is always low.

Step 1. Look at the $\overline{\text{EXPANSION RESET}}$ signal on U1007-13 or P1001-15. If this signal is always low, the reset is coming from the station control board. Proceed to the Reset Arbiter section of the station control board description to troubleshoot the problem.

Step 2. If the $\overline{\text{EXPANSION RESET}}$ signal is high but U1008-6 is low, check for a fault in the associated logic circuits (U1007F, U1015A, U1006F, U1015D, U1015C, Q1014).

5.3 ALIGNMENT AND TROUBLESHOOTING USING INTERNALLY GENERATED TEST TONES

5.3.1 Tone Test Routine

The tone remote control board contains a test routine called Tone Test in which the microprocessor (U1008) generates its own test tones at any one of several different frequencies. These tones, which originate as a square wave on pin 9 of MPU U1008, are applied to the tone encode filter (U1020B and U1018A), whose output is approximately sinusoidal. The tones are then applied to the line driver at any one of three selectable levels. The tone appears on the wireline output terminals on the side of the station (L1 screws on 2-wire models, L2 on 4-wire). These tones may be fed back into the transmit line audio input terminals on 4-wire boards by connecting the L1 terminals to the L2 terminals (disconnect phone lines first). On 2-wire boards the line audio output is already connected to the transmit audio input so it is only necessary to disconnect the phone line to feed audio into the transmit path. On 2-wire models, if it is intended to inject the tones into the transmit path, the phone line should be disconnected. This will ensure enough unbalance in the cancellation circuit to provide good input level into the transmit path. The phone line may always be left connected if the object of the test is to intentionally send a test tone down the wireline.

The generated tones may also be used as a general purpose audio generator. If the phone line is disconnected from the L1 (L2 on a 4-wire board) terminals, these terminals become a non-polarized, floating output with dc blocking that may be applied to the input of another board or device. For example, if either of the L1 (L2 on a 4-wire board) terminals is ground to the "A.G." test pin in station control, and the other terminal is connected to TP8 on station control, then a test tone may be fed into the local audio input of the station control board. The amplitude of the tone may be adjusted using the "Line Lev" control if desired, and the frequency is selected using the following procedure.

5.3.2 Tone Test Access Procedure

The following set-up uses Tone Test to quickly check the operation of the tone remote control board by looping the output of the line driver back into the transmit audio input, where it is amplified and ultimately detected by the microprocessor U1008. If the microprocessor detects the tone that it is sending it turns on the front panel TONE DETECT LED.

Step 1. Disconnect phone line(s) from station. On 4-wire stations, connect L1 to L2 (to cause encoded tones to Loop back to station).

Step 2. Momentarily ground TP12 to TP1 (logic ground). All three yellow LED's on front panel (TONE DETECT, TONE SEND, and LINE PTT) should begin blinking on and off slowly.

Step 3. Toggle INTERCOM switch on, then off. If 2175 Hz is being properly generated by the microprocessor the TONE SEND LED will be on, and a 2175 Hz tone should be present on the phone line terminals. If this 2175 Hz tone is also being properly decoded, the TONE DETECT LED will also be on. Normally, TONE SEND and TONE DETECT should both be on at this time. This tests all circuits between the microprocessor tone output pin (U1008-9) and limiter input pin (U1008-8), including the operation of the processor itself.

Step 4. Toggling the INTERCOM switch further will produce various tones as shown in Table 3 (i.e., toggling up and down four more times will produce a 1950 Hz test tone on phone line). For each frequency, the TONE SEND LED will indicate that the tone is being sent by the microprocessor, and if that tone is properly detected the TONE DETECT LED will light.

NOTE

If the INTERCOM switch is not toggled for 3 minutes, the tone test routine times out and automatically ends. If desired, it can be restarted by momentarily connecting TP12 to TP1 again.

Step 5. To end tone test, momentarily depress the TEST switch on front panel of the station control module. This ends the tone test and resets the station.

5.3.3 Troubleshooting Using Tone Test

As the INTERCOM switch is toggled while in the Tone Test mode, the frequencies of the tones generated and

Table 3. Tone Frequency Selection

Number of INTERCOM Switch Toggles (After Grounding TP12)	Resultant Tone and Amplitude Relative to Line Level Setting
0	None. All 3 yellow LED's blink.
1	2175 Hz @ approx. -3 dB (High Level Guard Tone)
2	None or 2175 Hz @ 30 dB (depending on options)
3	2175 Hz -13 dB
4	2050 Hz -13 dB
5	1950 Hz -13 dB
6	1850 Hz -13 dB
7	1750 Hz -13 dB
8	1650 Hz -13 dB
9	1550 Hz -13 dB
10	1450 Hz -13 dB
11	1350 Hz -13 dB
12	1250 Hz -13 dB
13	1150 Hz -13 dB
14	1050 Hz -13 dB
15	950 Hz -13 dB
16	850 Hz -13 dB
17	750 Hz -13 dB
18	650 Hz -13 dB
19	Starts over with 1

their relative amplitudes vary according to Table 3. In addition, certain hardware in the transmit audio tone detection path is exercised. On the first toggle (high level guard tone), analog gate U1027C is switched to feed the output of the guard tone bandpass filter into the limiter for detection (U1027-9 should be approximately 9.6 V). On toggles 3 through 18 U1027C is switched to the opposite position, so that the audio which is fed to the tone limiter bypasses the guard tone bandpass filter. In this way both paths are exercised.

As an aid to troubleshooting, Table 4 lists the peak ac voltage and dc (average) voltage of several points in the receive audio/line driver path and transmit audio/tone processing path. The peak ac voltages may be converted to rms by multiplying times 0.707, or to peak-peak by multiplying times 2. All values are valid only with the Tone Test in the first toggle of intercom switch (high level guard tone; see Table 3), and the line driver adjusted to 0 dBm into 600-ohm resistive load (at 5 kHz received signal deviation, 1 kHz frequency). On 4-wire boards, L1 phone line terminals should be connected to L2 terminals. All other phone line connections should be removed from the L1 and L2 terminals for this test on both 4-wire and 2-wire boards.

IMPORTANT

Do not attempt to measure ac voltages on the (-) inputs of op-amps. Instead, measure voltage at the op-amp outputs.

In addition to generating and detecting its own tones, the Tone Test feature can be used to determine if the input tone from another device is on frequency. For example, on the first toggle the microprocessor will light the TONE DETECT LED if it receives a 2175 ±10 Hz input on the L1 terminals. This signal need not be exactly the same frequency as the tone being generated by the microprocessor that appears at the line driver output. A remote control console could be tested for its ability to send 2175 Hz using this feature. If the Intercom switch is toggled into the fifth position, the TONE DETECT LED will light when a 1950 Hz tone is received. The LED will remain on only for the duration of the tone, so it will appear as a momentary flash for tones of short duration such as function tones. Similarly, the Tone Test routine can be used to detect the presence of any other tone listed in Table 3 depending on the number of toggles of the intercom switch. To set up the tone remote control board for detecting external tones, proceed as follows.

Step 1. Temporarily ground pin 5 of U1020D to TP3 (analog ground). This prevents the generated tones from reaching line driver and looping back into transmit audio path.

Step 2. Connect the source of external tones to the L1 phone line input terminals.

Step 3. Momentarily connect TP12 to TP1 to enter the tone test mode. Then, toggle the intercom switch the correct number of times for detection of the desired frequency, according to Table 3. The TONE DETECT LED will light if tone is present.

NOTE

If the INTERCOM switch is not toggled for 3 minutes, the tone test routine times out and automatically ends. If desired, it can be restarted by momentarily connecting TP12 to TP1.

5.3.4 Adjustments

Setting of the LINE LEV control is covered in the Installation section of this manual. Setting of XMIT LEV and AGC controls is covered in the Maintenance section of this manual.

5.3.5 Filter Alignment

The tone remote control board contains two notch filters and two bandpass filters. All are factory tuned and normally require no adjustment. However, if realignment is desired it can easily be done using the internal tone test routine. This is accomplished as follows.

Step 1. Using a short jumper connect TP17 to TP18. On 4-wire stations connect L1 to L2. Connect the volt-

Table 4. Tone Remote Control Board Voltage Measurements

Test Point	Peak AC Voltage	DC Level (average value)
U1008 pin 9	±2.4 V	2.4 V
U1020 pin 7	±0.24 V	4.7 V
U1018 pin 8	±0.7 V	4.7 V
U1021 pin 8	±0.22 V	2.2 V
U1021 pin 14	±0.22 V	2.2 V
U1021 pin 1	±0.22 V	2.9 V
U1021 pin 7	±0.22 V	2.9 V
Q1012 and Q1013 emitters	±0.22 V	2.2 V
Q1012 and Q1013 collectors	4-Wire: approx. ±.78 V 2-Wire: approx. ±1.6 V	12.8 V 12.8 V
Phone Line Terminals (L1)	4-Wire: approx. ±.78 V 2-Wire: approx. ±1.6 V	0 V
U1018 pin 1	±55 mV	4.7 V
TP11	±1.1 V	4.7 V
TP16	±1.9 V	4.7 V
TP15	±1.7 V	4.7 V
U1020 pin 8	±3.3 V	3.9 V
U1020 pin 14	±3.5 V	3.7 V
TP10	±2 V	2 V

meter or oscilloscope (-) lead to analog ground, TP3 or TP14 on tone remote control board.

Step 2. Momentarily connect TP12 to TP1 (logic ground). All three yellow LEDs on TRC front panel should blink slowly on and off.

Step 3. Toggle the INTERCOM switch on and off twice, then use potentiometer R1119 to tune receive notch for null (minimum voltage) on TP9.

NOTE

After 3 minutes the tone test routine automatically ends. If this happens it may be restarted by repeating Step 2.

Step 4. Remove the jumper connected between TP17 and TP18.

Step 5. Set the level on TP11 to -6 dBm using AGC control R1088.

Step 6. Toggle the INTERCOM switch again (this is the third toggle after entering tone test). Tune the transmit notch filter for null (minimum voltage) on TP5 by adjusting potentiometer R1058.

Step 7. Tune the guard tone bandpass filter by adjusting R1051 for maximum voltage on TP16. Tune the second section of the filter by adjusting R1046 for maximum voltage on TP15.

Step 8. Return AGC control R1088 to its normal (fully clockwise) setting.

Alignment of the transmit notch filter to an external source of guard tone (such as the remote control console) may sometimes be desirable. If this is the case, the following procedure should be used.

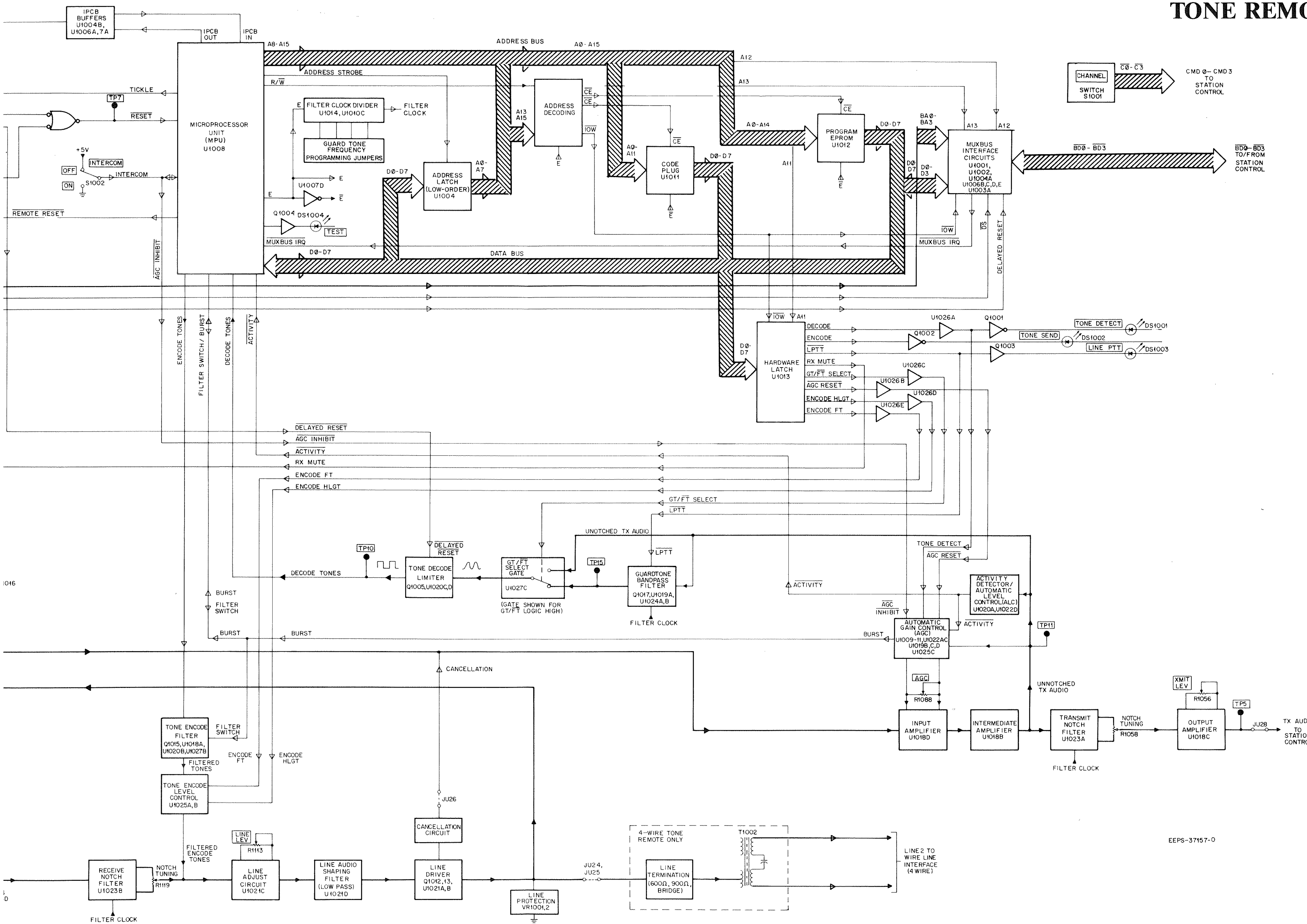
Step 1. Temporarily connect a jumper between TP10 and TP1 (logic ground).

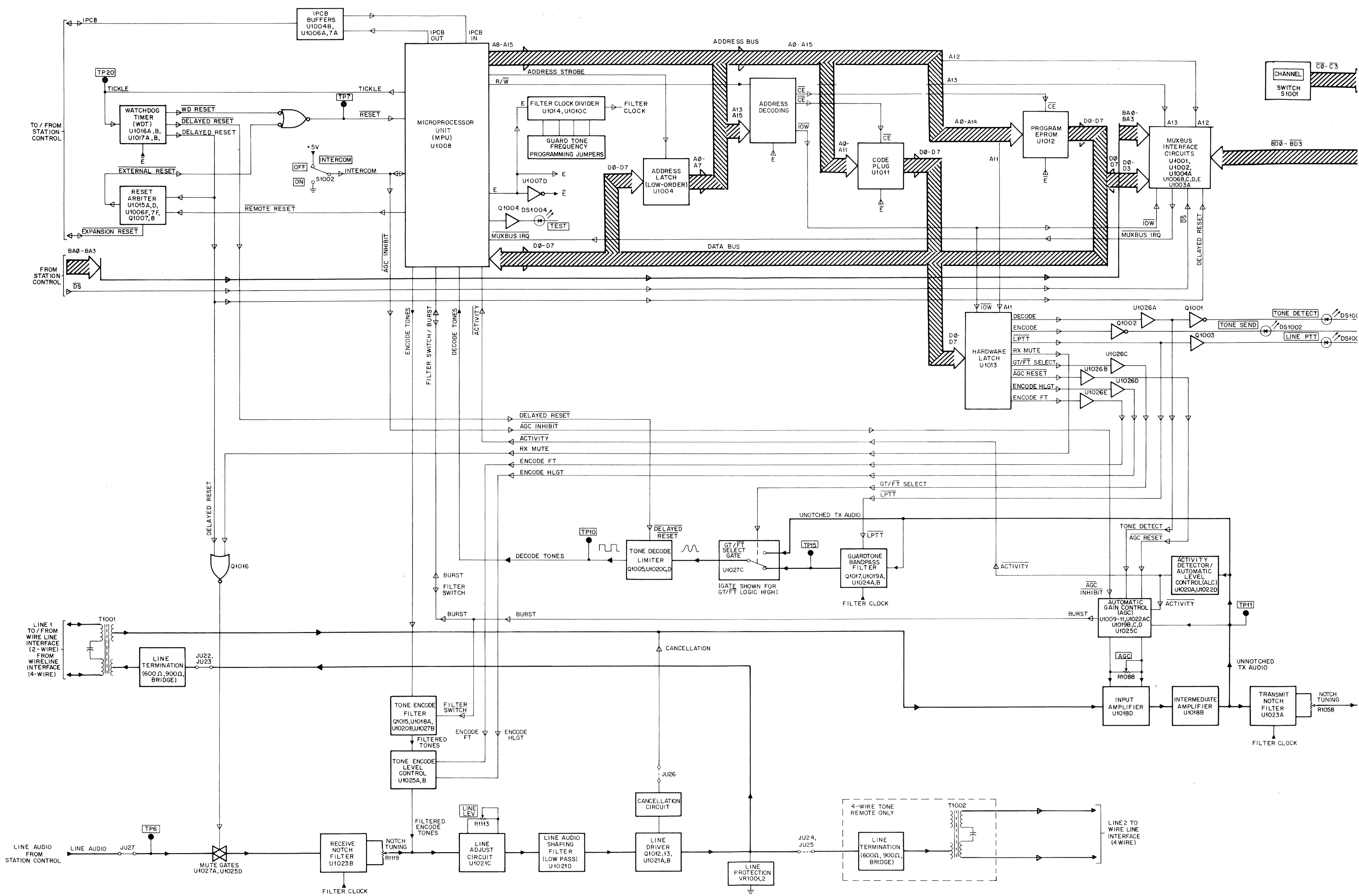
Step 2. Connect the guard tone source to L1 phone line terminals on side of station. The tone amplitude should be between -35 and +11 dBm.

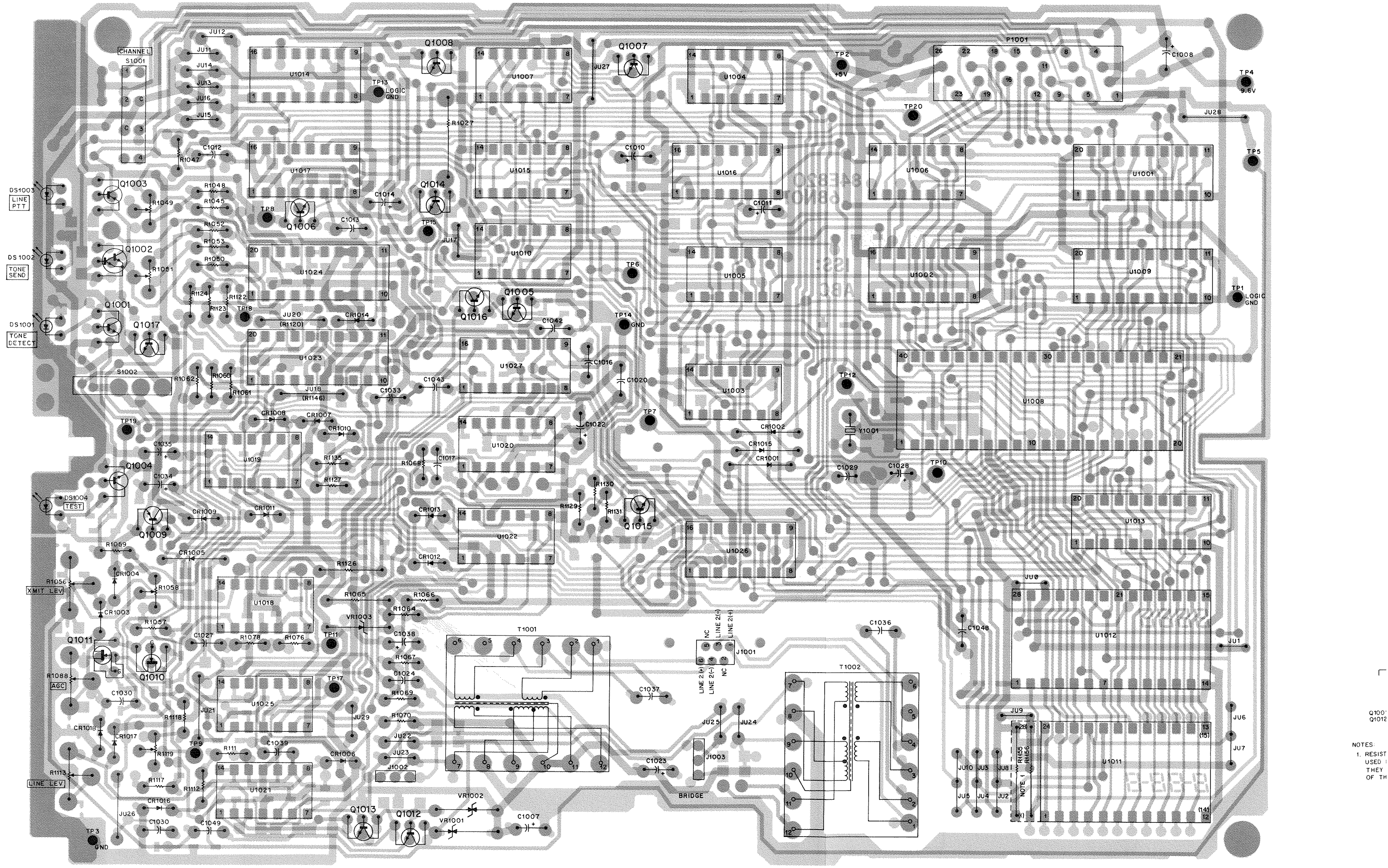
Step 3. Tune R1058 for null (minimum voltage) on TP5 of the tone remote control board (relative to analog ground on TP3 or TP14).

Step 4. Remove the jumper installed in Step 1.

TONE REMOTE CONTROL BOARDS
SIMPLIFIED BLOCK DIAGRAM

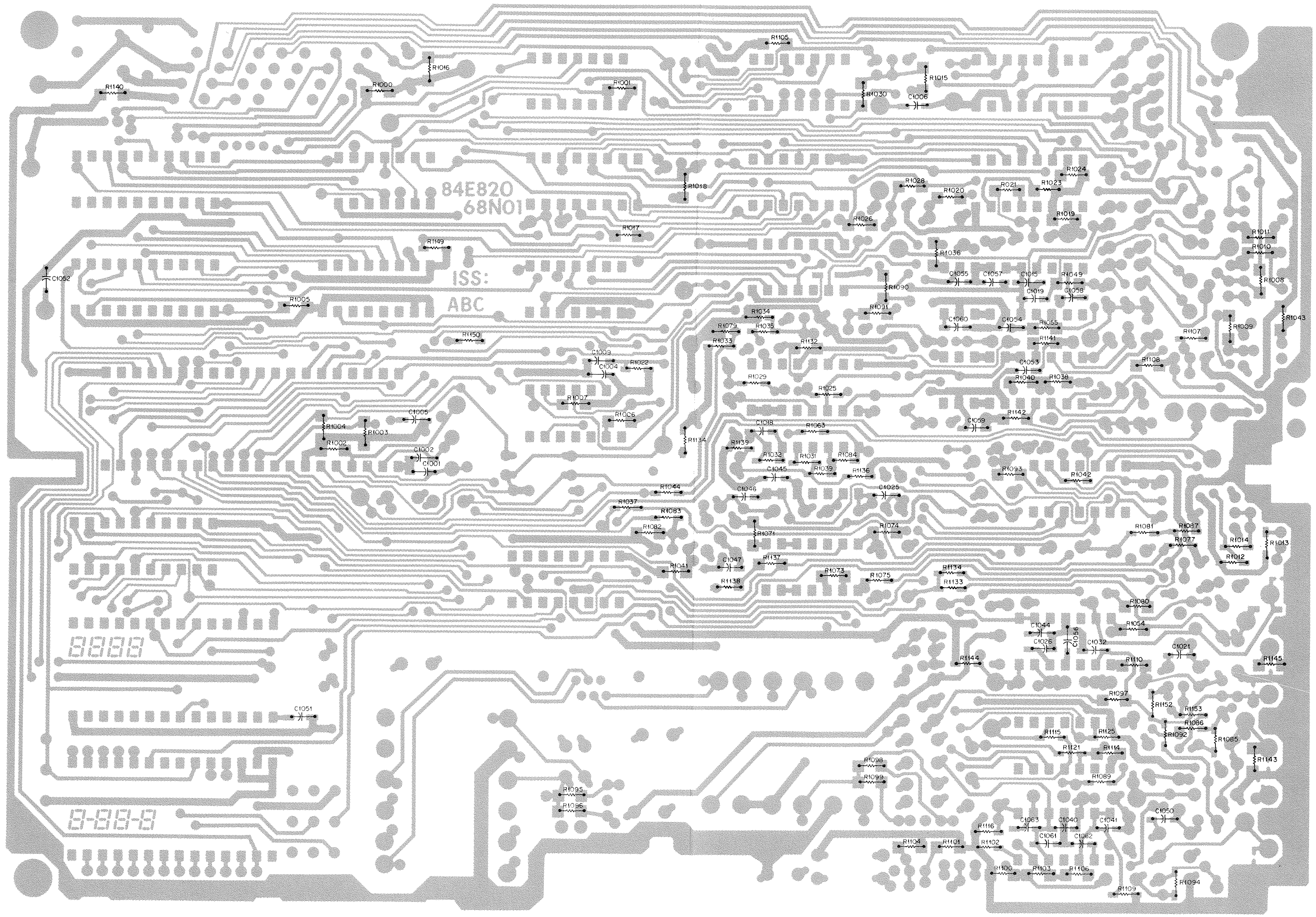


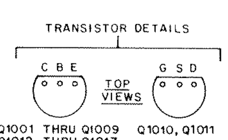

IPCB BUFFERS U1004B, U1006A,7A
IPCB
IPCB OUT
IPCB IN
MICROPROCESSOR UNIT (MPU) U1008
A8-A15
ADDRESS BUS
A0-A15
ADDRESS STROBE
R/W
TP20
TICKLE
WATCHDOG TIMER (WDT) U1016A,B, U1017A,B,
WD RESET
DELAYED RESET
TP7
RESET
TO / FROM STATION CONTROL
EXTERNAL RESET
RESET ARBITER U1015A,D, U1006F,7F, Q1007,8
REMOTE RESET
EXPANSION RESET
+5V
INTERCOM
OFF
ON
S1002
FILTER CLOCK DIVIDER U1014, U1010C
FILTER CLOCK
GUARD TONE FREQUENCY PROGRAMMING JUMPERS
U1007D
Q1004
DS1004
TEST
MUXBUS IRQ
D0-D7
ADDRESS LATCH (LOW-ORDER) U1004
ADDRESS DECODING
CODE PLUG U1011
PROGRAM EPROM U1012
MUXBUS INTERFACE CIRCUITS U1001, U1002, U1004A U1006B,C,D,E U1003A
CHANNEL SWITCH S1001
C0-C3
BD0-BD3
BA0-BA3
DATA BUS
FROM STATION CONTROL
DS
AGC INHIBIT
ENCODE TONES
FILTER SWITCH / BURST
DECODE TONES
ACTIVITY
DELAYED RESET
HARDWARE LATCH U1013
DECODE
ENCODE
LPTT
RX MUTE
GT/FT SELECT
AGC RESET
ENCODE HLGT
ENCODE FT
U1026A
Q1001
Q1002
Q1003
TONE DETECT
TONE SEND
LINE PTT
DS1002
Q1016
TP10
DECODE TONES
TONE DECODE LIMITER Q1005,U1020C,D
GT/FT SELECT GATE U1027C
(GATE SHOWN FOR GT/FT LOGIC HIGH)
TP15
GUARDTONE BANDPASS FILTER Q1017,U1019A, U1024A,B
FILTER CLOCK
UNOTCHED TX AUDIO
ACTIVITY DETECTOR/ AUTOMATIC LEVEL CONTROL(ALC) U1020A,U1022D
AUTOMATIC GAIN CONTROL (AGC) U1009-11,U1022AC U1019B,C,D U1025C
TP11
BURST
FILTER SWITCH
LINE 1 TO/FROM WIRE LINE INTERFACE (2-WIRE) FROM WIRELINE INTERFACE (4-WIRE)
T1001
LINE TERMINATION (600Ω,900Ω, BRIDGE)
JU22, JU23
CANCELLATION
UNNOTCHED TX AUDIO
INPUT AMPLIFIER U1018D
INTERMEDIATE AMPLIFIER U1018B
TRANSMIT NOTCH FILTER U1023A
NOTCH TUNING R1058
R1088
TONE ENCODE FILTER Q1015,U1018A, U1020B,U1027B
FILTERED TONES
TONE ENCODE LEVEL CONTROL U1025A,B
JU26
CANCELLATION CIRCUIT
LINE AUDIO FROM STATION CONTROL
JU27
TP6
MUTE GATES U1027A,U1025D
RECEIVE NOTCH FILTER U1023B
NOTCH TUNING R1119
FILTERED ENCODE TONES
LINE LEV R1113
LINE ADJUST CIRCUIT U1021C
LINE AUDIO SHAPING FILTER (LOW PASS) U1021D
LINE DRIVER Q1012,13, U1021A,B
LINE PROTECTION VR1001,2
JU24, JU25
4-WIRE TONE REMOTE ONLY
T1002
LINE TERMINATION (600Ω, 900Ω, BRIDGE)
LINE 2 TO WIRE LINE INTERFACE (4 WIRE)



SHOWN FROM COMPONENT SIDE

SOLDER SIDE BD-EEPS-37969-O
COMPONENT SIDE BD-EEPS-37970-O
OL-EEPS-37971-A





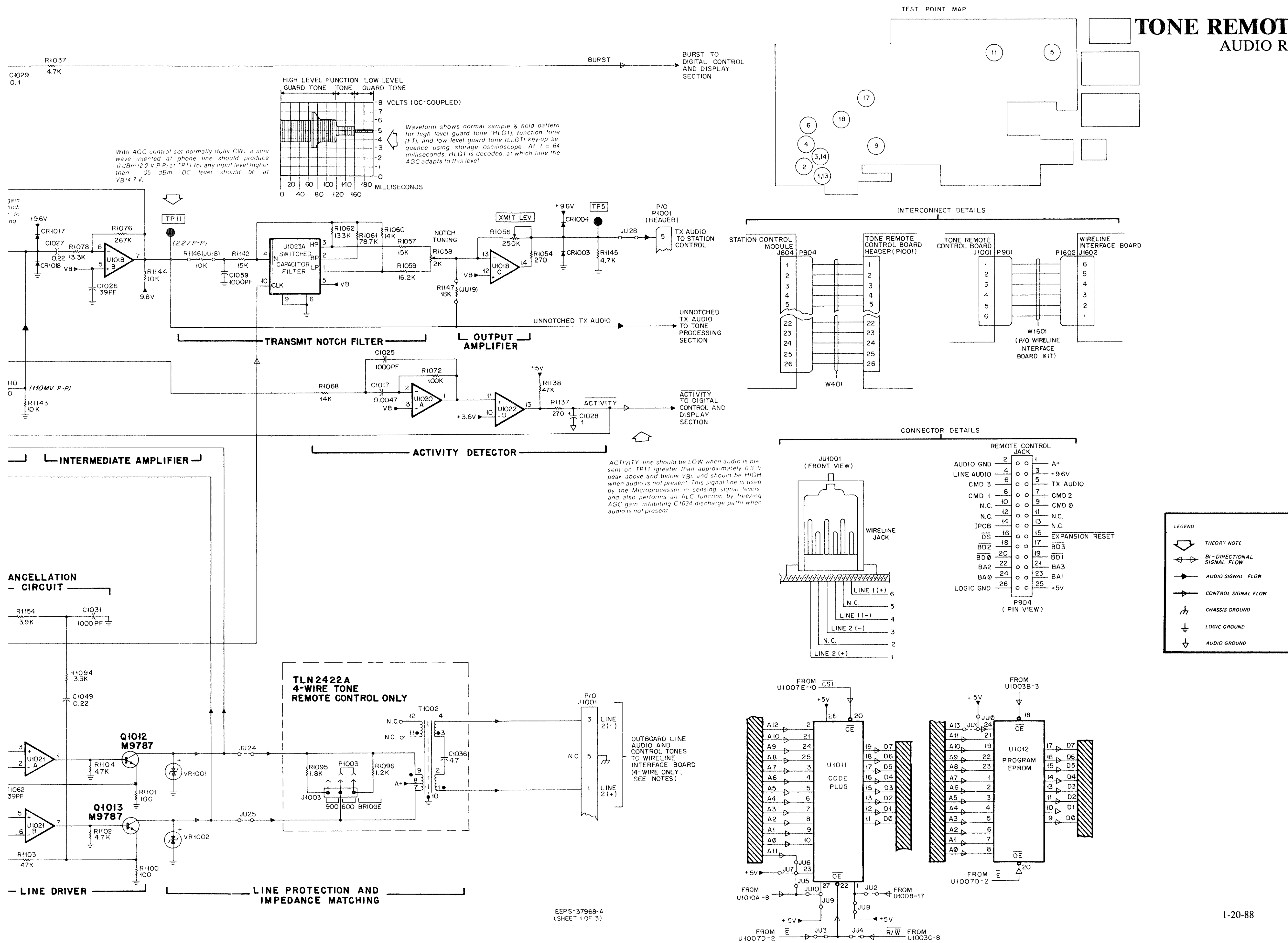
NOTES:

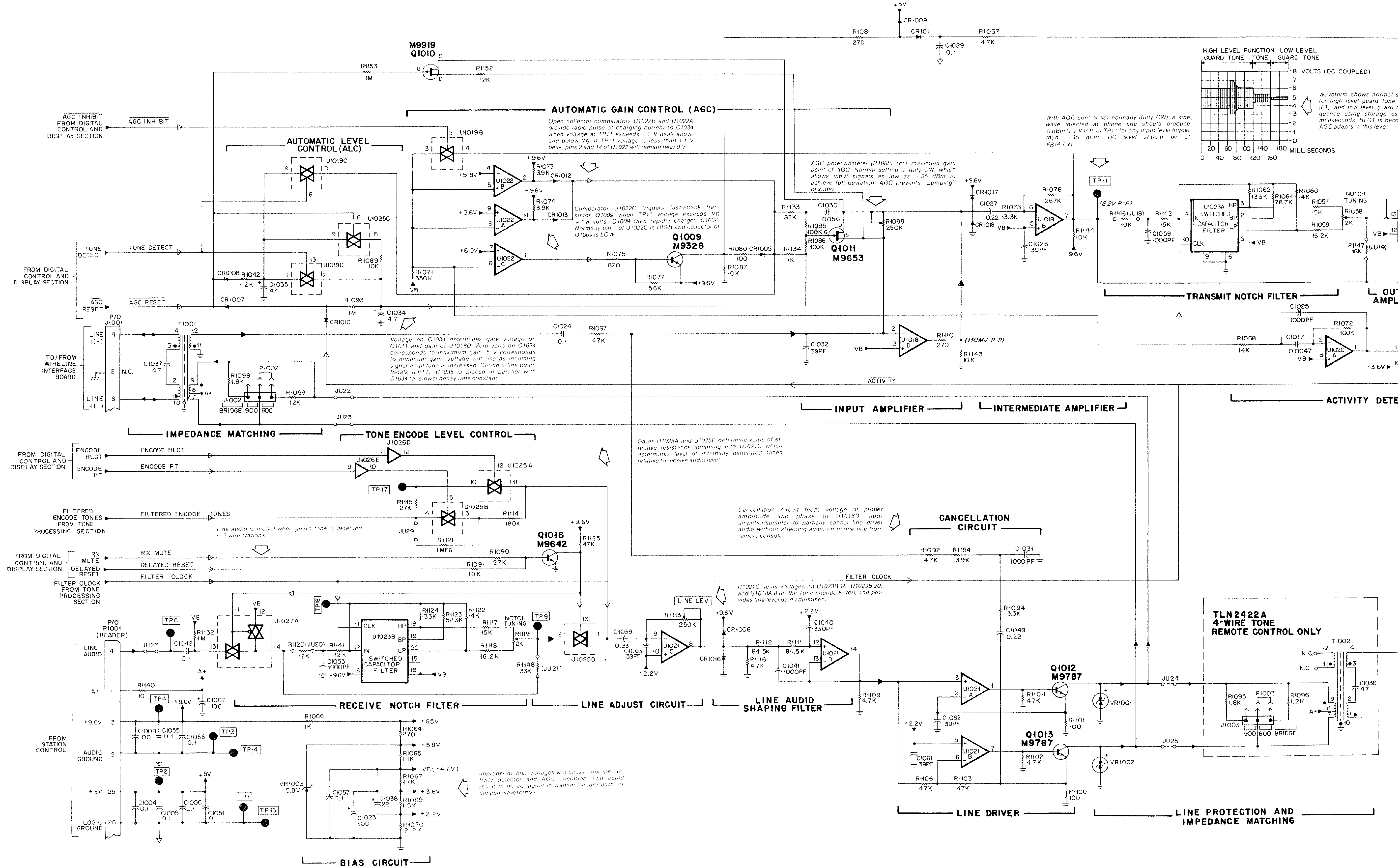
1. RESISTORS R1155 AND R1156 ARE USED FOR POSITIONING U1011. THEY ARE NOT ELECTRICALLY PART OF THE CIRCUIT.

SHOWN FROM SOLDER SIDE

SOLDER SIDE 80-EEPS-37972-0
OL-EEPS-37973-0

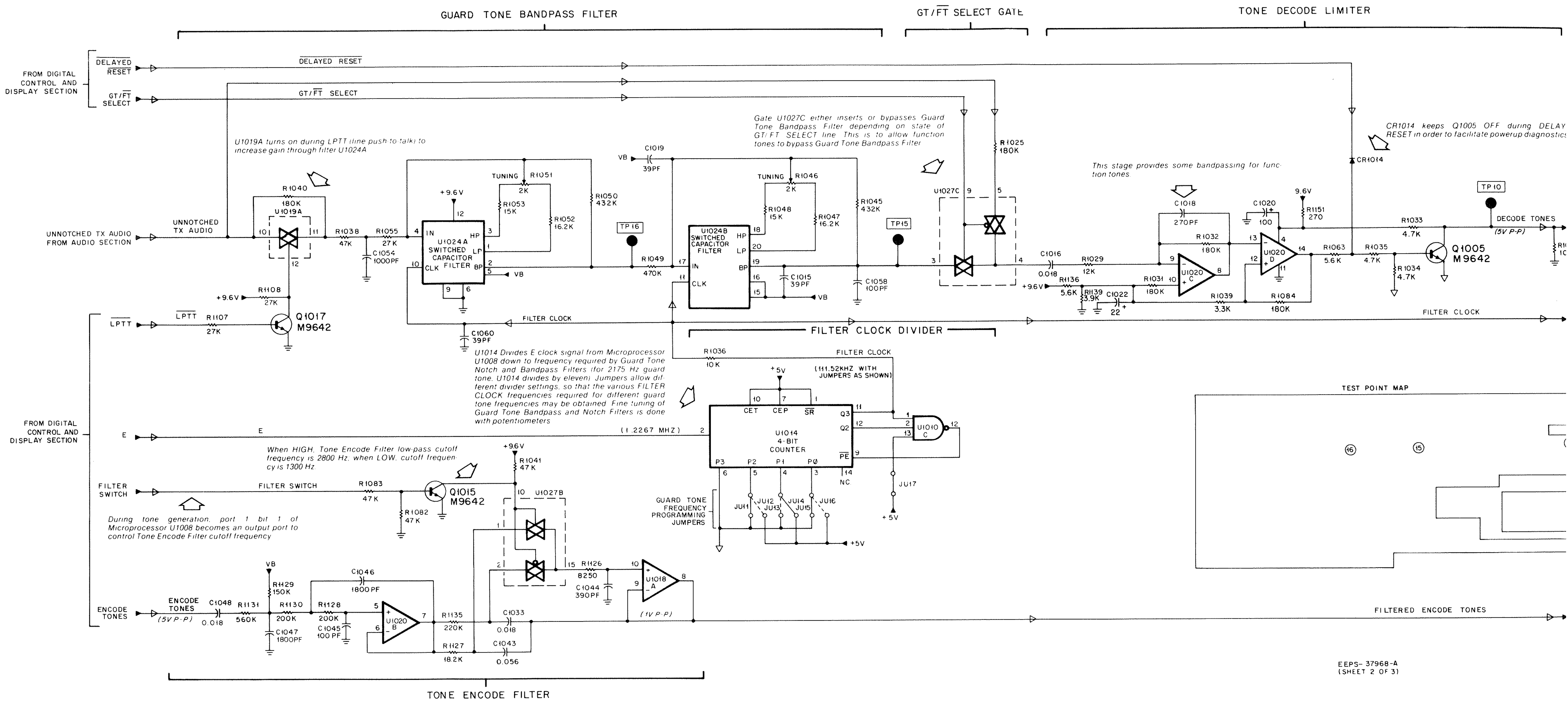
TONE REMOTE CONTROL BOARDS
AUDIO ROUTING SCHEMATIC DIAGRAM

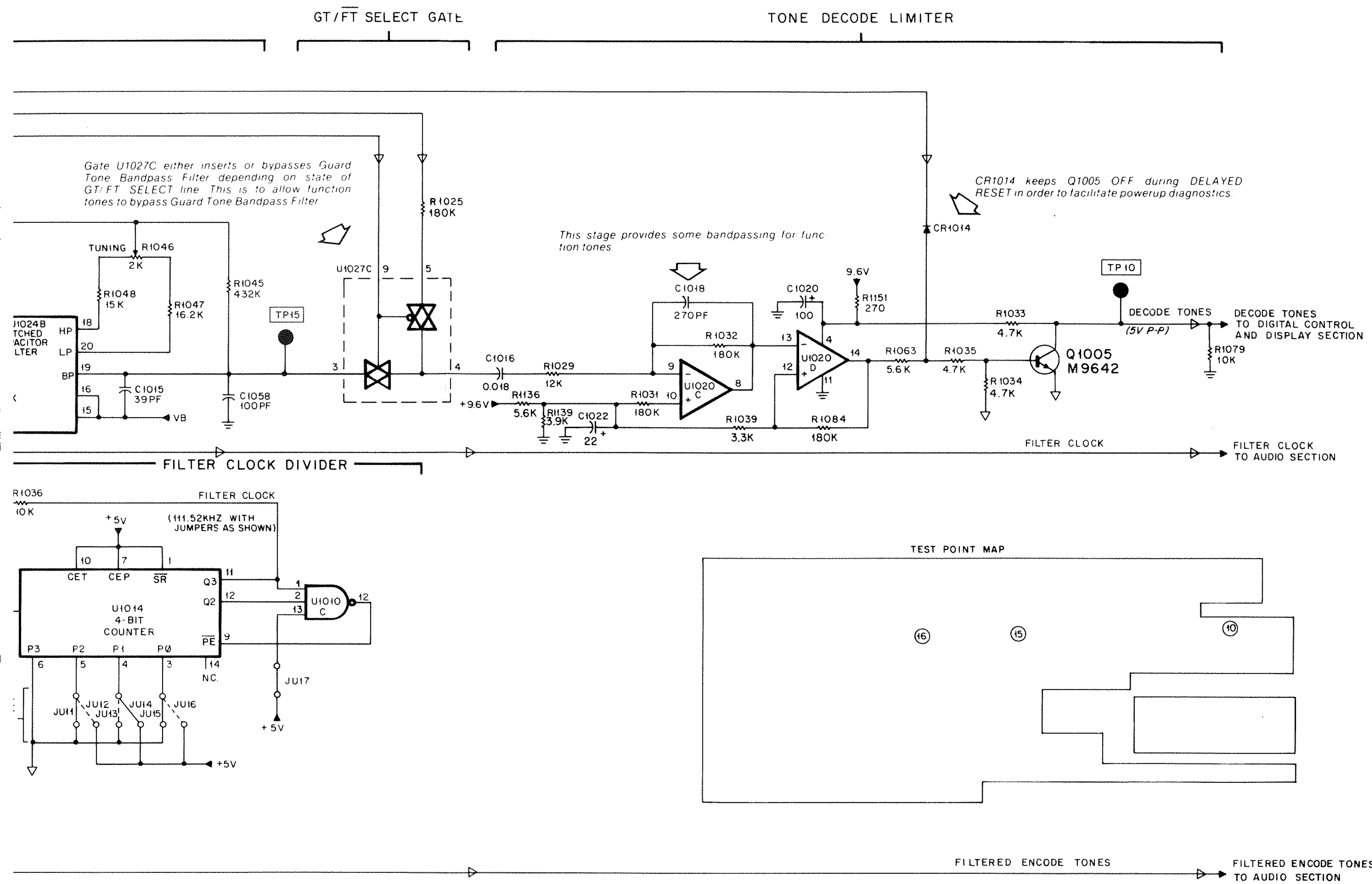




AUTOMATIC GAIN CONTROL (AGC)
Open collector comparators U1022B and U1022A provide rapid pulse of charging current to C1034 when voltage at TP11 exceeds 1.1 V peak above and below VB. If TP11 voltage is less than 1.1 V peak, pins 2 and 14 of U1022 will remain near 0 V.
Comparator U1022C triggers fast-attack transistor Q1009 when TP11 voltage exceeds VB + 1.8 volts. Q1009 then rapidly charges C1034. Normally pin 1 of U1022C is HIGH and collector of Q1009 is LOW.
AUTOMATIC LEVEL CONTROL (ALC)
AGC INHIBIT FROM DIGITAL CONTROL AND DISPLAY SECTION
TONE DETECT
AGC RESET
FROM DIGITAL CONTROL AND DISPLAY SECTION
TO/FROM WIRELINE INTERFACE BOARD
Voltage on C1034 determines gate voltage on Q1011 and gain of U1018D. Zero volts on C1034 corresponds to maximum gain. 5 V corresponds to minimum gain. Voltage will rise as incoming signal amplitude is increased. During a line push-to-talk (LPTT), C1035 is placed in parallel with C1034 for slower decay time constant.
AGC potentiometer (R1088) sets maximum gain point of AGC. Normal setting is fully CW, which allows input signals as low as -35 dBm to achieve full deviation. AGC prevents "pumping" of audio.
With AGC control set normally (fully CW), a sine-wave injected at phone line should produce 0 dBm (2.2 V P-P) at TP11 for any input level higher than -35 dBm. DC level should be at VB (4.7 V).
HIGH LEVEL GUARD TONE
FUNCTION TONE
LOW LEVEL GUARD TONE
VOLTS (DC-COUPLED)
MILLISECONDS
Waveform shows normal s for high level guard tone (FT), and low level guard t quence using storage os milliseconds. HLGT is deco AGC adapts to this level
M9919 Q1010
Q1009 M9328
Q1011 M9653
TRANSMIT NOTCH FILTER
ACTIVITY DETE
INPUT AMPLIFIER
INTERMEDIATE AMPLIFIER
IMPEDANCE MATCHING
TONE ENCODE LEVEL CONTROL
FROM DIGITAL CONTROL AND DISPLAY SECTION
ENCODE HLGT
ENCODE FT
FILTERED ENCODE TONES FROM TONE PROCESSING SECTION
Line audio is muted when guard tone is detected in 2-wire stations
Gates U1025A and U1025B determine value of effective resistance summing into U1021C which determines level of internally generated tones relative to receive audio level
Cancellation circuit feeds voltage of proper amplitude and phase to U1018D input amplifier/summer to partially cancel line driver audio without affecting audio on phone line from remote console
CANCELLATION CIRCUIT
RX MUTE
DELAYED RESET
FILTER CLOCK
Q1016 M9642
FILTER CLOCK FROM TONE PROCESSING SECTION
U1021C sums voltages on U1023B-18, U1023B-20, and U1018A-8 (in the Tone Encode Filter), and provides line level gain adjustment
LINE LEV
NOTCH TUNING
RECEIVE NOTCH FILTER
LINE ADJUST CIRCUIT
LINE AUDIO SHAPING FILTER
Q1012 M9787
Q1013 M9787
LINE DRIVER
LINE PROTECTION AND IMPEDANCE MATCHING
TLN2422A 4-WIRE TONE REMOTE CONTROL ONLY
FROM STATION CONTROL
LINE AUDIO
AUDIO GROUND
LOGIC GROUND
Improper dc bias voltages will cause improper activity detector and AGC operation, and could result in no ac signal in transmit audio path (or clipped waveforms)
BIAS CIRCUIT

TONE REMOTE CONTROL BOARDS
TONE PROCESSING SCHEMATIC DIAGRAM





EEPS-37968-A
(SHEET 2 OF 3)

NOTES:

1. Unless otherwise specified, resistor values are in ohms and capacitor values in microfarads.

Line Connection Chart

Application	Line 1 J1001-4(—), —6(+)	Line 2 J1001-1(+), -3(—)
2-Wire	Inbound Tx Audio and Control Tones; Outbound Line Audio and Control Tones	Not Used
4-Wire	Inbound Tx Audio and Control Tones	Outbound Line Audio and Control Tones

2. The Tone Remote Control printed circuit board accommodates alternative CODE PLUG (U1011) and PROGRAM EPROM (U1012) IC configurations as shown below. The Digital Control and Display section of this schematic shows the normal configuration.

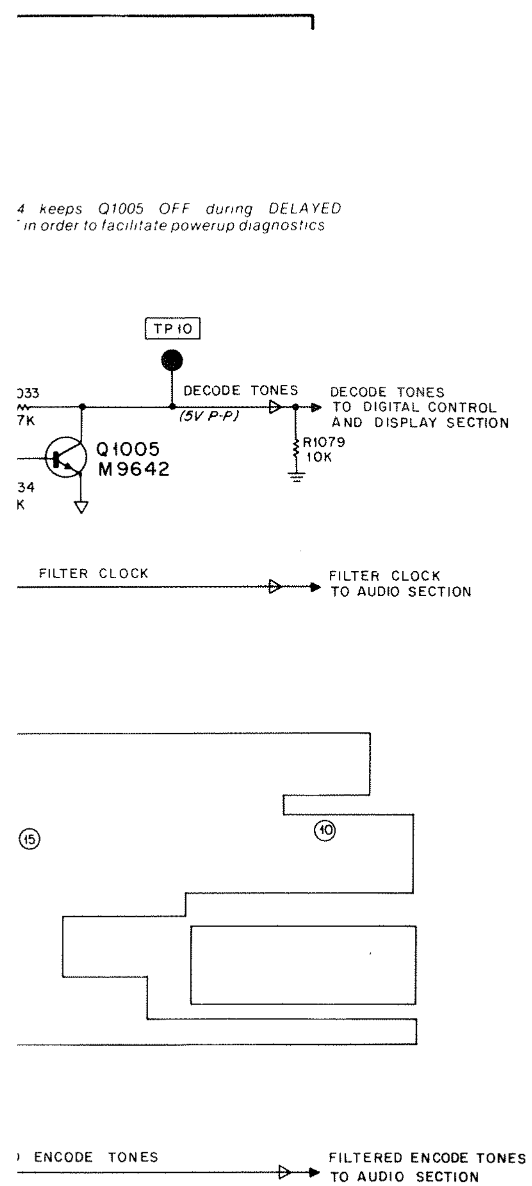
Jumper Table

Jumper Desig.	Normal Status	Description
JU0	OUT	(IN for special application only)
JU1	IN	Normal operation (foil jumper)
JU2	OUT	(IN for special application only)
JU3	IN	Normal operation (foil jumper)
JU4	OUT	(IN for special application only)
JU5	OUT	(IN for special application only)
JU6	IN	Normal operation (foil jumper)
JU7	OUT	(IN for special application only)
JU8	IN	Normal operation (foil jumper)
JU9	IN	Normal operation (foil jumper)
JU10	OUT	(IN for special application only)
		Jumpers JU11-JU16 may require modification if Code Plug U1011 is altered to recognize a guard tone freq other than 2175 Hz. The Normal Status column indicates a jumper configuration for a 2175 Hz guard tone. W jumper is IN, a zero (0) ohm resistor (Motorola part no. 6-11009F23) has been used as a jumper to facilitate insertion manufacturing techniques. A 1/2-inch length of +24 AWG insulated wire may be used as a jumper i changes are required.
		WARNING If jumper combinations are modified, make absolutely certain that jumpers in the following pairs are not *both* IN:
JU11	IN	JU11 and JU12
JU12	OUT	JU13 and JU14
JU13	OUT	JU15 and JU16
JU14	IN	Otherwise, the +5 V power source will be shorted directly to ground.
JU15	IN	
JU16	OUT	
		Guard tone frequencies and the jumper combinations necessary to select them are listed in the following t

Guard Tone Freq. (Hz)	JU11	JU12	JU13	JU14	JU15	JU16
	Jumper Designation					
2100	IN	OUT	OUT	IN	IN	OUT
2175	IN	OUT	OUT	IN	IN	OUT
2325	IN	OUT	OUT	IN	OUT	IN
2432	IN	OUT	OUT	IN	OUT	IN
2700	OUT	IN	IN	OUT	IN	OUT

NOTE
Certain guard tone frequencies are in the same band and are selected by the same jumper combinations.

Jumper Desig.	Normal Status	Description
JU17	IN	Normal operation (foil jumper)
JU18	IN	IN: 18k resistor (R1146) to use Transmit Notch Filter (see JU19); OUT: To bypass Transmit Notch Filter (see JU19)
JU19	OUT	OUT: To use Transmit Notch Filter (see JU18); IN: 18k resistor to bypass Transmit Notch Filter (see JU18)
JU20	IN	IN: 15k resistor (R1120) to use Receive Notch Filter (see JU21); OUT: To bypass Receive Notch Filter (see JU21)
JU21	OUT	OUT: To use Receive Notch Filter (see JU20); IN: 33k resistor (R1148) to bypass Receive Notch Filter (see JU20)
JU22	IN	IN: 2-wire applications; OUT: 4-wire applications
JU23	IN	IN: 2-wire applications; OUT: 4-wire applications
JU24	OUT	OUT: 2-wire applications; IN: 4-wire applications
JU25	OUT	OUT: 2-wire applications; 3.9k resistor (R1154) on 600 ohm lines, wire on 900 ohm lines IN: 4-wire applications
JU26	IN	IN: 2-wire applications; OUT: 4-wire applications
JU27	IN	Provides line audio input (foil jumper)
JU28	IN	Provides Tx Audio output (foil jumper)



NOTES:

1. Unless otherwise specified, resistor values are in ohms and capacitor values in microfarads.

Line Connection Chart

Application	Line 1 J1001-4(—), —6(+)	Line 2 J1001-1(+), -3(—)
2-Wire	Inbound Tx Audio and Control Tones; Outbound Line Audio and Control Tones	Not Used
4-Wire	Inbound Tx Audio and Control Tones	Outbound Line Audio and Control Tones

2. The Tone Remote Control printed circuit board accommodates alternative CODE PLUG (U1011) and PROGRAM EPROM (U1012) IC configurations as shown below. The Digital Control and Display section of this schematic shows the normal configuration.

Jumper Table

Jumper Desig.	Normal Status	Description
JU0	OUT	(IN for special application only)
JU1	IN	Normal operation (foil jumper)
JU2	OUT	(IN for special application only)
JU3	IN	Normal operation (foil jumper)
JU4	OUT	(IN for special application only)
JU5	OUT	(IN for special application only)
JU6	IN	Normal operation (foil jumper)
JU7	OUT	(IN for special application only)
JU8	IN	Normal operation (foil jumper)
JU9	IN	Normal operation (foil jumper)
JU10	OUT	(IN for special application only)

Jumpers JU11-JU16 may require modification if Code Plug U1011 is altered to recognize a guard tone frequency other than 2175 Hz. The Normal Status column indicates a jumper configuration for a 2175 Hz guard tone. Where a jumper is IN, a zero (0) ohm resistor (Motorola part no. 6-11009F23) has been used as a jumper to facilitate auto-insertion manufacturing techniques. A 1/2-inch length of +24 AWG insulated wire may be used as a jumper if field changes are required.

WARNING

If jumper combinations are modified, make absolutely certain that jumpers in the following pairs are not *both* IN:

JU11 and JU12
JU13 and JU14
JU15 and JU16

Otherwise, the +5 V power source will be shorted directly to ground.

Jumper Desig.	Normal Status
JU11	IN
JU12	OUT
JU13	OUT
JU14	IN
JU15	IN
JU16	OUT

Guard tone frequencies and the jumper combinations necessary to select them are listed in the following table.

Guard Tone Freq. (Hz)	Jumper Designation JU11	JU12	JU13	JU14	JU15	JU16
2100	IN	OUT	OUT	IN	IN	OUT
2175	IN	OUT	OUT	IN	IN	OUT
2325	IN	OUT	OUT	IN	OUT	IN
2432	IN	OUT	OUT	IN	OUT	IN
2700	OUT	IN	IN	OUT	IN	OUT

NOTE

Certain guard tone frequencies are in the same band and are selected by the same jumper combinations.

Jumper Desig.	Normal Status	Description
JU17	IN	Normal operation (foil jumper)
JU18	IN	IN: 18k resistor (R1146) to use Transmit Notch Filter (see JU19); OUT: To bypass Transmit Notch Filter (see JU19)
JU19	OUT	OUT: To use Transmit Notch Filter (see JU18); IN: 18k resistor to bypass Transmit Notch Filter (see JU18)
JU20	IN	IN: 15k resistor (R1120) to use Receive Notch Filter (see JU21); OUT: To bypass Receive Notch Filter (see JU21)
JU21	OUT	OUT: To use Receive Notch Filter (see JU20); IN: 33k resistor (R1148) to bypass Receive Notch Filter (see JU20)
JU22	IN	IN: 2-wire applications; OUT: 4-wire applications
JU23	IN	IN: 2-wire applications; OUT: 4-wire applications
JU24	OUT	OUT: 2-wire applications; IN: 4-wire applications
JU25	OUT	OUT: 2-wire applications; 3.9k resistor (R1154) on 600 ohm lines, wire on 900 ohm lines IN: 4-wire applications
JU26	IN	IN: 2-wire applications; OUT: 4-wire applications
JU27	IN	Provides line audio input (foil jumper)
JU28	IN	Provides Tx Audio output (foil jumper)

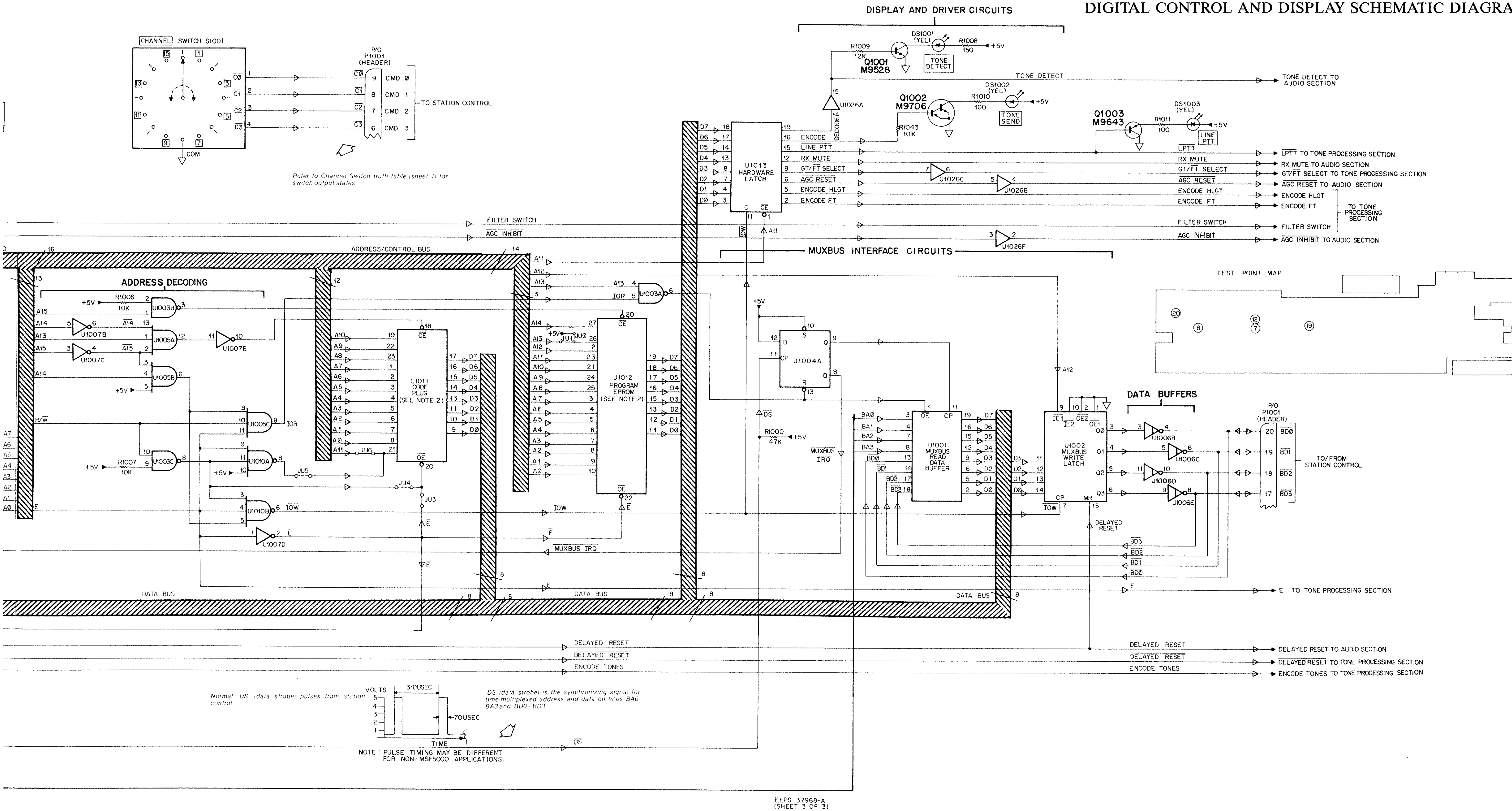
Channel Switch Truth Table

S1001 Position	P1001-6 CMD 3 (C3)	P1001-7 CMD 2 (C2)	P1001-8 CMD 1 (C1)	P1001-9 CMD 0 (C0)
(0)	H	H	H	H
1	H	H	H	L
(2)	H	H	L	H
3	H	H	L	L
(4)	H	L	H	H
5	H	L	H	L
(6)	H	L	L	H
7	H	L	L	L
(8)	L	H	H	H
9	L	H	H	L
(10)	L	H	L	H
11	L	H	L	L
(12)	L	L	H	H
13	L	L	H	L
(14)	L	L	L	H
15	L	L	L	L

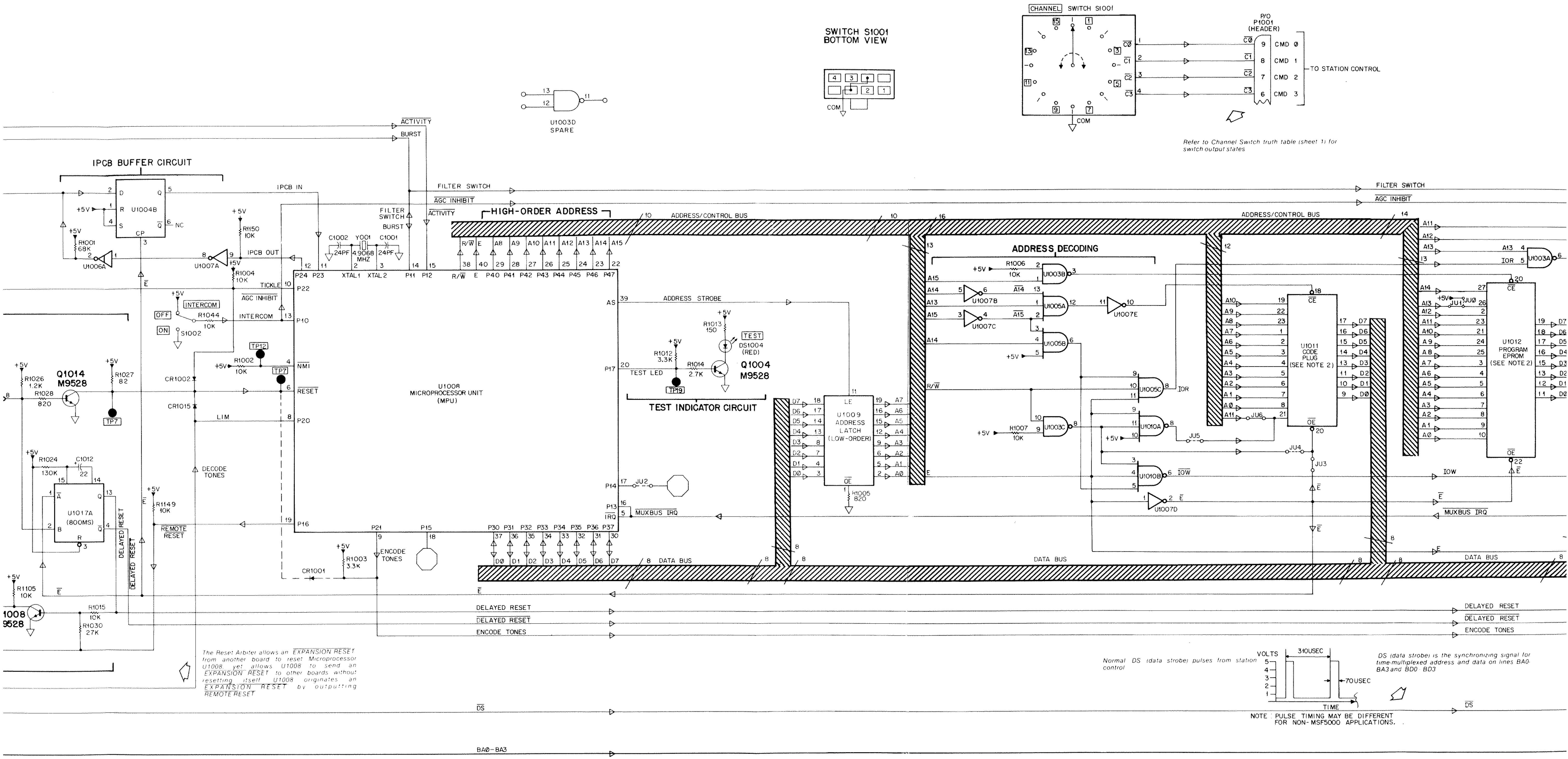
Note: H = +5 V; L = -0 V

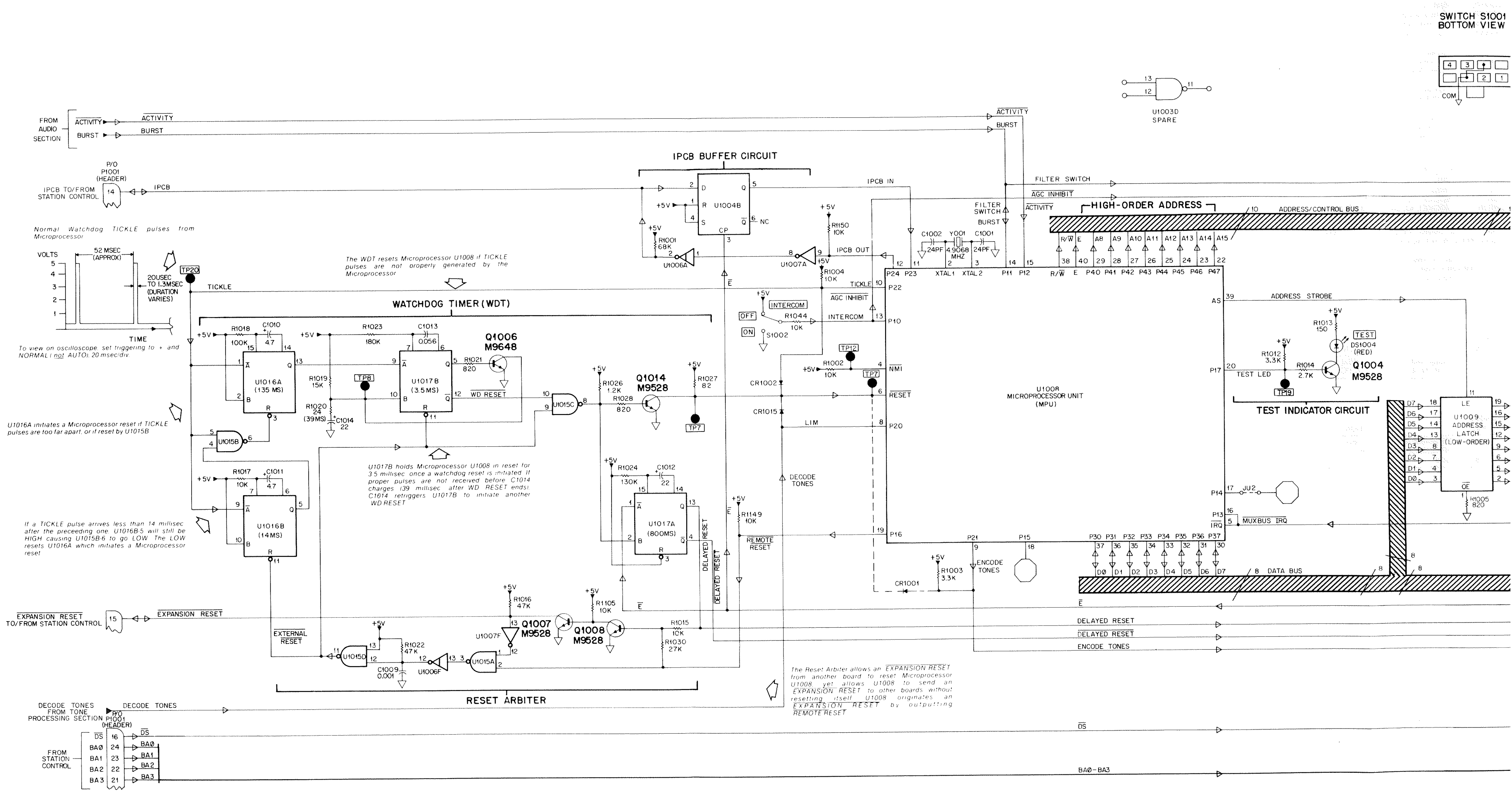
Integrated Circuit Data Chart

Ref. Desig.	+5 V (Pin)	+9. 6 V (Pin)	Logic Gnd (Pin)	Audio Gnd (Pin)	Description
U1001	20	—	10	—	Octal D Latch
U1002	16	—	8	—	Quad Tri-State Latch
U1003	14	—	7	—	Quad NAND
U1004	14	—	7	—	Dual D Flip-Flop
U1005	14	—	7	—	Triple 3-Input NAND
U1006	14	—	7	—	Hex Inverter
U1007	14	—	7	—	Hex Inverter
U1008	7, 21	—	1	—	Microprocessor
U1009	20	—	10	—	Octal Tri-State Latch
U1010	14	—	7	—	Triple 3-Input NAND
U1011	1, 24	—	12	—	4k × 8 EPROM (CODE PLUG)
U1012	1, 28	—	14	—	8k × 8 EPROM (PROGRAM)
U1013	20	—	10	—	Octal Latch
U1014	16	—	8	—	4-Bit Counter
U1015	14	—	7	—	Quad NAND
U1016	16	—	8	—	Dual Monostable
U1017	16	—	8	—	Dual Monostable
U1018	—	4	—	11	Quad Op Amp
U1019	—	14	—	7	Quad Analog Switch
U1020	—	4	—	11	Quad Op Amp
U1021	—	4	—	11	Quad Op Amp
U1022	—	3	—	12	Quad Comparator
U1023	—	7, 8	—	13, 14	Dual Switched Capacitor Filter
U1024	—	7, 8	—	13, 14	Dual Switched Capacitor Filter
U1025	—	14	—	7	Quad Analog Switch
U1026	1, 13	16	—	8	Hex Level Shifter
U1027	—	16	—	6, 7, 8	Triple 2-Channel MUX Switch



DISPLAY AND DRIVER CIRCUITS
CHANNEL SWITCH S1001
P/O P1001 (HEADER)
CMD 0
CMD 1
CMD 2
CMD 3
TO STATION CONTROL
COM
Refer to Channel Switch truth table (sheet 1) for switch output states
Q1001 M9528
TONE DETECT
Q1002 M9706
TONE SEND
Q1003 M9643
LINE PTT
U1013 HARDWARE LATCH
ENCODE
LINE PTT
RX MUTE
GT/FT SELECT
AGC RESET
ENCODE HLGT
ENCODE FT
FILTER SWITCH
AGC INHIBIT
TONE DETECT TO AUDIO SECTION
LPTT TO TONE PROCESSING SECTION
RX MUTE TO AUDIO SECTION
GT/FT SELECT TO TONE PROCESSING SECTION
AGC RESET TO AUDIO SECTION
TO TONE PROCESSING SECTION
AGC INHIBIT TO AUDIO SECTION
MUXBUS INTERFACE CIRCUITS
ADDRESS/CONTROL BUS
ADDRESS DECODING
TEST POINT MAP
U1011 CODE PLUG (SEE NOTE 2)
U1012 PROGRAM EPROM (SEE NOTE 2)
U1004A
U1001 MUXBUS READ DATA BUFFER
U1002 MUXBUS WRITE LATCH
DATA BUFFERS
TO/FROM STATION CONTROL
DELAYED RESET
DATA BUS
MUXBUS IRQ
E TO TONE PROCESSING SECTION
DELAYED RESET TO AUDIO SECTION
DELAYED RESET TO TONE PROCESSING SECTION
ENCODE TONES TO TONE PROCESSING SECTION
ENCODE TONES
Normal DS (data strobe) pulses from station control
DS (data strobe) is the synchronizing signal for time-multiplexed address and data on lines BA0-BA3 and BD0-BD3
VOLTS
310USEC
70USEC
TIME
NOTE: PULSE TIMING MAY BE DIFFERENT FOR NON-MSF5000 APPLICATIONS.
EEPS-37968-A (SHEET 3 OF 3)


IPCB BUFFER CIRCUIT
U1004B
U1006A
U1007A
R1001 68K
R1150 10K
R1004 10K
IPCB IN
IPCB OUT
TICKLE
AGC INHIBIT
INTERCOM
OFF
ON
S1002
R1044 10K
ACTIVITY
BURST
FILTER SWITCH
AGC INHIBIT
HIGH-ORDER ADDRESS
ADDRESS/CONTROL BUS
C1002
Y001
C1001
24PF
4.9068 MHZ
XTAL1
XTAL2
U1008
MICROPROCESSOR UNIT
(MPU)
NMI
RESET
R1002 10K
TP12
TP7
CR1002
CR1015
LIM
DECODE TONES
Q1014
M9528
R1026 1.2K
R1028 820
R1027 82
R1024 130K
C1012 22
U1017A
(800MS)
R1149 10K
REMOTE RESET
DELAYED RESET
R1105 10K
Q1008
M9528
R1015 10K
R1030 27K
R1003 3.3K
ENCODE TONES
CR1001
ADDRESS STROBE
R1013 150
TEST
DS1004
(RED)
R1012 3.3K
R1014 2.7K
Q1004
M9528
TEST LED
TP19
TEST INDICATOR CIRCUIT
JU2
MUXBUS IRQ
DATA BUS
U1009
ADDRESS
LATCH
(LOW-ORDER)
R1005 820
U1003D
SPARE
SWITCH S1001
BOTTOM VIEW
COM
CHANNEL SWITCH S1001
P/O
P1001
(HEADER)
CMD 0
CMD 1
CMD 2
CMD 3
TO STATION CONTROL
Refer to Channel Switch truth table (sheet 1) for switch output states
ADDRESS DECODING
R1006 10K
U1003B
U1007B
U1007C
U1005A
U1007E
U1005B
U1005C
IOR
U1010A
U1003C
R1007 10K
JU5
JU4
JU3
JU6
U1010B
IOW
U1007D
U1011
CODE
PLUG
(SEE NOTE 2)
U1012
PROGRAM
EPROM
(SEE NOTE 2)
JU1
JU0
U1003A
DELAYED RESET
ENCODE TONES
DS
BA0-BA3
The Reset Arbiter allows an EXPANSION RESET from another board to reset Microprocessor U1008 yet allows U1008 to send an EXPANSION RESET to other boards without resetting itself. U1008 originates an EXPANSION RESET by outputting REMOTE RESET
Normal DS (data strobe) pulses from station control
VOLTS
310USEC
70USEC
TIME
NOTE: PULSE TIMING MAY BE DIFFERENT FOR NON-MSF5000 APPLICATIONS.
DS (data strobe) is the synchronizing signal for time-multiplexed address and data on lines BA0-BA3 and BD0-BD3


SWITCH S1001
BOTTOM VIEW
COM
U1003D
SPARE
FROM AUDIO SECTION
ACTIVITY
BURST
P/O P1001 (HEADER)
IPCB TO/FROM STATION CONTROL
IPCB
IPCB BUFFER CIRCUIT
U1004B
U1006A
U1007A
IPCB IN
IPCB OUT
FILTER SWITCH
AGC INHIBIT
HIGH-ORDER ADDRESS
ADDRESS/CONTROL BUS
Normal Watchdog TICKLE pulses from Microprocessor
VOLTS
52 MSEC (APPROX)
20USEC TO 1.3MSEC (DURATION VARIES)
TIME
To view on oscilloscope, set triggering to + and NORMAL (not AUTO); 20 msec/div.
TICKLE
The WDT resets Microprocessor U1008 if TICKLE pulses are not properly generated by the Microprocessor
WATCHDOG TIMER (WDT)
U1016A (135 MS)
U1017B (3.5MS)
Q1006 M9648
WD RESET
U1015C
Q1014 M9528
U1016A initiates a Microprocessor reset if TICKLE pulses are too far apart, or if reset by U1015B
U1015B
U1016B (14MS)
U1017B holds Microprocessor U1008 in reset for 3.5 millisec once a watchdog reset is initiated. If proper pulses are not received before C1014 charges (39 millisec after WD RESET ends), C1014 retriggers U1017B to initiate another WD RESET
If a TICKLE pulse arrives less than 14 millisec after the preceeding one, U1016B-5 will still be HIGH causing U1015B-6 to go LOW. The LOW resets U1016A which initiates a Microprocessor reset
U1017A (800MS)
DELAYED RESET
REMOTE RESET
INTERCOM
S1002
OFF
ON
U1008 MICROPROCESSOR UNIT (MPU)
ADDRESS STROBE
TEST LED
TEST INDICATOR CIRCUIT
Q1004 M9528
DS1004 (RED)
U1009 ADDRESS LATCH (LOW-ORDER)
MUXBUS IRQ
DATA BUS
DECODE TONES
ENCODE TONES
LIM
EXPANSION RESET TO/FROM STATION CONTROL
EXPANSION RESET
EXTERNAL RESET
U1015D
U1006F
U1015A
U1007F
Q1007 M9528
Q1008 M9528
RESET ARBITER
The Reset Arbiter allows an EXPANSION RESET from another board to reset Microprocessor U1008, yet allows U1008 to send an EXPANSION RESET to other boards without resetting itself. U1008 originates an EXPANSION RESET by outputting REMOTE RESET
DECODE TONES FROM TONE PROCESSING SECTION
FROM STATION CONTROL
DS
BA0
BA1
BA2
BA3
BA0-BA3

TONE REMOTE CONTROL BOARDS
PARTS LISTS

parts list

TRN5185A Tone Remote Control Board (2-Wire)
TRN5187A Tone Remote Control Board (4-Wire) PL-8554-C

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ±5%; 50 V: unless otherwise stated
C1001	21-11031A24	24 pF; chip
C1002	21-11031A24	24 pF; chip
C1004	21-11032B13	0.1 +80-20%; chip
C1005	21-11032B13	0.1 +80-20%; chip
C1006	21-11032B13	0.1 +80-20%; chip
C1007	23-11019A46	100 ±20%; 25 V
C1008	23-11019A46	100 ±20%; 25 V
C1009	21-11031A61	1000 pF ±5%; chip
C1010	23-11013E09	4.7 ±10%; 25 V
C1011	23-11013E09	4.7 ±10%; 25 V
C1012	23-11013C11	22 ±10%; 15 V
C1013	8-11017A15	0.056
C1014	23-11013C11	22 ±10%; 15 V
C1015	21-11031A29	39 pF; chip
C1016	8-11017A10	0.018
C1017	8-11017A06	0.0047
C1018	21-11031A49	270 pF; chip
C1019, 1020	21-11031A29	39 pF; chip
C1021	NOT USED	
C1022	23-11019A27	22; 25 V
C1023	23-11019A46	100; ±20%; 25 V
C1024	8-11051A13	0.1 ±5%; 63 V
C1025	21-11031A61	1000 pF; chip
C1026	21-11031A29	39 pF ±10%; chip
C1027	8-11051A15	0.22 ±5%; 63 V
C1028	23-11019A09	1
C1029	8-11051A13	0.1 ±5%; 63 V
C1030	8-11017A15	0.056
C1031	8-11017A01	0.001
C1032, 1033	21-11031A29	39 pF; chip
C1034	23-11013E09	4.7 ±10%; 25 V
C1035	23-84538G29	47; ±20%; 10 V
C1036	23-82028P07	4.7 ±20%; 200 V (TRN5187A)
C1037	23-82028P07	4.7 ±20%; 200 V
C1038	23-11019A27	22; ±20%; 25 V
C1039	8-11051A16	0.33 ±5%; 63 V
C1040	21-11031A51	330 pF; chip
C1041	21-11031A61	1000 pF; chip
C1042	8-11051A13	0.1 ±5%; 63 V
C1043	8-11017A15	0.056
C1044	21-11031A53	390 pF; chip
C1045	21-11031A39	100 pF; chip
C1046, 1047	21-11031A65	1800 pF; chip
C1048	8-11017A10	0.018
C1049	8-11051A15	0.22 ±5%; 63 V
C1050	NOT USED	
C1051, 1052	21-11032B13	0.1 +80-20%; chip
C1053	21-11031A61	1000 pF; chip
C1054	21-11031A61	1000 pF; chip
C1055	21-11032B13	0.1 +80-20%; chip
C1056	21-11032B13	0.1 +80-20%; chip
C1057	21-11032B13	0.1 +80-20%; chip
C1058	21-11031A39	100 pF; chip
C1059	21-11031A61	1000 pF; chip
C1060	NOT USED	
C1061 thru 1063	21-11031A29	39 pF; chip
		diode: (see note)
CR1001	NOT USED	
CR1002	48-84616A09	hot carrier
CR1003 thru 1004	48-11034D01	silicon
CR1005	48-11034A01	silicon
CR1006 thru 1013	48-11034D01	silicon
CR1014	48-11034A01	silicon
CR1015	48-84616A09	hot carrier
CR1016 thru 1018	48-11034D01	silicon
		light emitting diode: (see note)
DS1001 thru 1003	48-88245C30	YEL
DS1004	48-88245C28	RED
		connector, receptacle
J1001	9-84206N01	female; 6-contact
J1002	28-84729L02	male, 3-contact
J1003	28-84729L02	male, 3-contact (TRN5187A)
		jumper, resistive:
JU1011	6-11009B23	0 ohms
JU1014, 1015	6-11009B23	0 ohms
JU1020	6-11009A77	15k ±5%; 1/4 W
JU1022 thru 1025	6-11009B23	0 ohms
		connector, plug:
P1001	30-83139N02	26-contact; p/o W401
P1002	9-84728L01	2-contact
P1003	9-84728L01	2-contact (TRN5187A)
		transistor: (see note)
Q1001	48-869528	NPN; type M9528
Q1002	48-869706	NPN; type M9706, Darlington
Q1003	48-869643	PNP; type M9643
Q1004	48-869528	NPN; type M9528
Q1005	48-869642	NPN; type M9642
Q1006	48-869648	NPN; type M9648
Q1007	48-869528	NPN; type M9528
Q1008	48-869528	NPN; type M9528
Q1009	48-869328	PNP; type M9328
Q1010	48-869919	NPN; type M9919
Q1011	48-869653	JFET, N-channel; type M9653
Q1012	48-869787	NPN; type M9787
Q1013	48-869787	NPN; type M9787
Q1014	48-869528	NPN; type M9528
Q1015 thru 1017	48-869642	NPN; type M9642
		resistor, fixed chip; ±5%; 1/8 W: unless otherwise stated
R1000	6-11024A89	47k
R1001	6-11024A93	68k
R1002	6-11024A73	10k
R1003	6-11024A61	3.3k
R1004	6-11024A73	10k
R1005	6-11024A47	820
R1006, 1007	6-11024A73	10k
R1008	6-11024A29	150
R1009	6-11024A75	12k
R1010, 1011	6-11024A25	100
R1012	6-11024A61	3.3k
R1013	6-11024A29	150
R1014	6-11024A59	2.7k
R1015	6-11024A73	10k
R1016	6-11024A89	47k
R1017	6-11024A73	10k
R1018	6-11024A97	100k
R1019	6-11024A77	15k
R1020	6-11024A10	24
R1021	6-11024A47	820
R1022	6-11024A89	47k
R1023	6-11024B04	180k
R1024	6-11024B01	130k
R1025	6-11024B04	180k
R1026	6-11024A51	1.2k
R1027	6-125A23	82; 1/2 W; carbon composition
R1028	6-11024A47	820
R1029	6-11024A75	12k
R1030	6-11024A83	27k
R1031, 1032	6-11024B04	180k
R1033, 1034	6-11024A65	4.7k
R1035	6-11024A65	4.7k
R1036	6-11024A73	10k
R1037	6-11024A65	4.7k
R1038	6-11024A89	47k
R1039	6-11024A61	3.3k
R1040	6-11024B04	180k
R1041	6-11024A89	47k
R1042	6-11024A51	1.2k
R1043	6-11024A75	12k
R1044	6-11024A73	10k
R1045	6-11049T50	432k ±1%; carbon film
R1046	18-83452F02	variable; 2k ±10%; 1/2 W
R1047	6-11040S12	16.2k; ±1/2%; carbon film
R1048	6-11040S09	15k; ±1/2%; carbon film
R1049	6-11024B14	470k
R1050	6-11049T50	432k; ±1%; carbon film
R1051	18-83452F02	variable; 2k ±10%; 1/2 W
R1052	6-11040S12	16.2k ±1/2%; 1/4 W, carbon film
R1053	6-11040S09	15k ±1/2%; 1/4 W, carbon film
R1054	6-11024A35	270
R1055	6-11024A83	27k
R1056	18-83686N06	variable; 250k ±20%
R1057	6-11040S09	15k ±0.5%; 1/4 W
R1058	18-83452F02	variable; 2k (Xmit Lev) ±10%; 1/2 W
R1059	6-11040S12	16.2k ±0.5%; 1/4 W, carbon film
R1060	6-11049S06	14k ±1%; 1/4 W, carbon film
R1061	6-11049S78	78.7 ±1%; 1/4 W, carbon film
R1062	6-11049S04	13.3k ±1%; 1/4 W, carbon film
R1063	6-11024A67	5.6k
R1064	6-11009E35	270; 1/4 W, carbon film
R1065	6-11009A50	1.1k; 1/4 W, carbon film
R1066	6-11009E49	1k; 1/4 W, carbon film
R1067	6-11009E50	1.1k; 1/4 W, carbon film
R1068	6-11049S06	14k ±1%; 1/4 W, carbon film
R1069	6-11009E53	1.5k; 1/4 W, carbon film
R1070	6-11009E57	2.2k; 1/4 W, carbon film
R1071	6-11024B10	330k
R1072	6-11009E97	100k; 1/4 W
R1073, 1074	6-11024A63	3.9k
R1075	6-11024A47	820
R1076	6-11049T30	267k ±1%; 1/4 W, carbon film
R1077	6-11024A67	5.6k
R1078	6-11049S04	13.3k ±1%; 1/4 W, carbon film
R1079	6-11024A73	10k
R1080	6-11024A25	100
R1081	6-11024A35	270
R1082, 1083 1084	6-11024A89	47k
R1085, 1086	6-11024A97	100k
R1087	6-11024A73	10k
R1088	18-83686N06	variable; 250k ±20%; 1/4 W (AGC)
R1089	6-11024A73	10k
R1090, 1091	6-11024A73	10k
R1092	6-11024A65	4.7k
R1093	6-11024B22	1 meg
R1094	6-11024A61	3.3k
R1095	6-11024A55	1.8k
R1096	6-11024A51	1.2k
R1097	6-11024A89	47k
R1098	6-11024A55	1.8k
R1099	6-11024A51	1.2k
R1100, 1101	6-11024A25	100
R1102	6-11024A65	4.7k
R1103	6-11024A89	47k
R1104	6-11024A65	4.7k
R1105	6-11024A73	10k
R1106	6-11024A89	47k
R1107, 1108	6-11024A73	10k
R1109	6-11024A65	4.7k
R1110	6-11024A35	270
R1111	6-11049S81	84.5k ±1%; 1/4 W, carbon film
R1112	6-11009E97	100k; 1/4 W, carbon film
R1113	18-83686N06	variable; 250k ±20%; 1/4 W, (Line Lev)
R1114	6-11024B04	180k
R1115	6-11024A93	68k
R1116	6-11024A65	4.7k
R1117	6-11040S09	15k ±1/2%; 1/4 W, carbon film
R1118	6-11040S12	16.2k ±1/2%; 1/4 W, carbon film
R1119	18-83452F02	variable; 2k ±10%; 1/2 W
R1120 (JU20)	6-11024A75	12k
R1121	6-11024B22	1 meg.
R1122	6-11049S06	14k ±1%; 1/4 W, carbon film
R1123	6-11049S61	52.3k ±1%; 1/4 W, carbon film
R1124	6-11049S04	13.3k ±1%; 1/4 W, carbon film
R1125	6-11024A89	47k
R1126	6-11049R83	8250 ±1%; 1/4 W; carbon film
R1127	6-11049S17	18.2k ±1%; 1/4 W; carbon film
R1128	6-11049T18	200k ±1%; 1/4 W; carbon film
R1129	6-11049T06	150k ±1%; 1/4 W; carbon film
R1130	6-11049T18	200k ±1%; 1/4 W; carbon film
R1131	6-11009F16	560k; 1/4 W
R1132	6-11024B22	1 meg
R1133	6-11024A95	82k
R1134	6-11024A49	1k
R1135	6-11009F06	220k; 1/4 W, carbon film
R1136	6-11024A67	5.6k
R1137	6-11024A35	270
R1138	6-11024A89	47k
R1139	6-11024A71	3.9k
R1140	6-11024A01	10
R1141	6-11024A75	12k
R1142	6-11024A77	15k
R1143, 1144	6-11024A73	10k
R1145	6-11024A65	4.7k
R1146 (JU18)	6-11009A73	10k; 1/4 W; carbon film
R1147, 1148	NOT USED	
R1149, 1150	6-11009E73	10k; 1/4 W, carbon film
R1151	6-11024A35	270
R1152	6-11024A75	12k
R1153	6-11024B22	1 meg
R1154 (JU26)	6-11009A63	3.9k; 1/4 W; carbon film (TRN5186A only)
R1155, 1156	6-11009D22	1 meg.
		switch:
S1001	40-82270M03	rotary, 16-position (Channel select switch)
S1002	40-83685N07	toggle, spdt (Intercom switch)
		transformer, audio:
T1001	25-83036L01	pri: leads 1 to 2 & 3 to 4; res. 25 ohms sec: leads 7 to 9 & 11 to 12; res. 250 ohms
T1002	25-83036L01	pri: leads 1 to 2 & 3 to 4; res. 25 ohms sec: leads 7 to 9 & 11 to 12; res. 250 ohms (TRN5187A)
		integrated circuit: (see note)
U1001	51-82609M67	octal D latch
U1002	51-83627M95	quad tri-state latch
U1003	51-83627M94	quad NAND
U1004	51-83627M93	dual D flip-flop
U1005	51-84561L44	triple 3-input NAND
U1006	51-84561L78	hex inverter
U1007	51-84561L03	hex inverter
U1008	51-83625M66	microprocessor
U1009	51-83627M03	octal tri-state latch
U1010	51-84561L08	triple 3-input NAND
U1011	p/o TRN5190	
U1012	p/o TRN5186	
U1013	51-82609M77	octal latch
U1014	51-82609M83	4-bit counter
U1015	51-83627M94	quad NAND
U1016, 1017	51-84561L11	dual monostable
U1018	51-83629M09	quad op amp
U1019	51-82884L48	quad analog switch
U1020	51-82609M05	quad op amp
U1021	51-83629M09	quad op amp

REFERENCE SYMBOL	
U1022	51
U1023, 1024	51
U1025	51
U1026	51
U1027	51
VR1001, 1002	48
VR1003	48
Y1001	48
W401	30

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	14
	9-
	9-

notes:
1. For optimum perfo circuits must be o
2. Chip resistors are AA are the two mo following the value resistor.

TRN5190A Code Plug

REFERENCE SYMBOL	
U1011	5

TRN5186A Software Ki

REFERENCE SYMBOL	
U1012	51
	54

parts list

TRN5185A Tone Remote Control Board (2-Wire)
TRN5187A Tone Remote Control Board (4-Wire) PL-8554-C

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ±5%; 50 V: unless otherwise stated
C1001	21-11031A24	24 pF; chip
C1002	21-11031A24	24 pF; chip
C1004	21-11032B13	0.1 +80-20%; chip
C1005	21-11032B13	0.1 +80-20%; chip
C1006	21-11032B13	0.1 +80-20%; chip
C1007	23-11019A46	100 ±20%; 25 V
C1008	23-11019A46	100 ±20%; 25 V
C1009	21-11031A61	1000 pF ±5%; chip
C1010	23-11013E09	4.7 ±10%; 25 V
C1011	23-11013E09	4.7 ±10%; 25 V
C1012	23-11013C11	22 ±10%; 15 V
C1013	8-11017A15	0.056
C1014	23-11013C11	22 ±10%; 15 V
C1015	21-11031A29	39 pF; chip
C1016	8-11017A10	0.018
C1017	8-11017A06	0.0047
C1018	21-11031A49	270 pF; chip
C1019, 1020	21-11031A29	39 pF; chip
C1021	NOT USED	
C1022	23-11019A27	22; 25 V
C1023	23-11019A46	100; ±20%; 25 V
C1024	8-11051A13	0.1 ±5%; 63 V
C1025	21-11031A61	1000 pF; chip
C1026	21-11031A29	39 pF ±10%; chip
C1027	8-11051A15	0.22 ±5%; 63 V
C1028	23-11019A09	1
C1029	8-11051A13	0.1 ±5%; 63 V
C1030	8-11017A15	0.056
C1031	8-11017A01	0.001
C1032, 1033	21-11031A29	39 pF; chip
C1034	23-11013E09	4.7 ±10%; 25 V
C1035	23-84538G29	47; ±20%; 10 V
C1036	23-82028P07	4.7 ±20%; 200 V (TRN5187A)
C1037	23-82028P07	4.7 ±20%; 200 V
C1038	23-11019A27	22; ±20%; 25 V
C1039	8-11051A16	0.33 ±5%; 63 V
C1040	21-11031A51	330 pF; chip
C1041	21-11031A61	1000 pF; chip
C1042	8-11051A13	0.1 ±5%; 63 V
C1043	8-11017A15	0.056
C1044	21-11031A53	390 pF; chip
C1045	21-11031A39	100 pF; chip
C1046, 1047	21-11031A65	1800 pF; chip
C1048	8-11017A10	0.018
C1049	8-11051A15	0.22 ±5%; 63 V
C1050	NOT USED	
C1051, 1052	21-11032B13	0.1 +80-20%; chip
C1053	21-11031A61	1000 pF; chip
C1054	21-11031A61	1000 pF; chip
C1055	21-11032B13	0.1 +80-20%; chip
C1056	21-11032B13	0.1 +80-20%; chip
C1057	21-11032B13	0.1 +80-20%; chip
C1058	21-11031A39	100 pF; chip
C1059	21-11031A61	1000 pF; chip
C1060	NOT USED	
C1061 thru 1063	21-11031A29	39 pF; chip
		diode: (see note)
CR1001	NOT USED	
CR1002	48-84616A09	hot carrier
CR1003 thru 1004	48-11034D01	silicon
CR1005	48-11034A01	silicon
CR1006 thru 1013	48-11034D01	silicon
CR1014	48-11034A01	silicon
CR1015	48-84616A09	hot carrier
CR1016 thru 1018	48-11034D01	silicon
		light emitting diode: (see note)
DS1001 thru 1003	48-88245C30	YEL
DS1004	48-88245C28	RED
		connector, receptacle
J1001	9-84206N01	female; 6-contact
J1002	28-84729L02	male, 3-contact
J1003	28-84729L02	male, 3-contact (TRN5187A)
		jumper, resistive:
JU1011	6-11009B23	0 ohms
JU1014, 1015	6-11009B23	0 ohms
JU1020	6-11009A77	15k ±5%; 1/4 W
JU1022 thru 1025	6-11009B23	0 ohms
		connector, plug:
P1001	30-83139N02	26-contact; p/o W401
P1002	9-84728L01	2-contact
P1003	9-84728L01	2-contact (TRN5187A)
		transistor: (see note)
Q1001	48-869528	NPN; type M9528
Q1002	48-869706	NPN; type M9706, Darlington
Q1003	48-869643	PNP; type M9643
Q1004	48-869528	NPN; type M9528
Q1005	48-869642	NPN; type M9642
Q1006	48-869648	NPN; type M9648
Q1007	48-869528	NPN; type M9528
Q1008	48-869528	NPN; type M9528
Q1009	48-869328	PNP; type M9328
Q1010	48-869919	NPN; type M9919
Q1011	48-869653	JFET, N-channel; type M9653
Q1012	48-869787	NPN; type M9787
Q1013	48-869787	NPN; type M9787
Q1014	48-869528	NPN; type M9528
Q1015 thru 1017	48-869642	NPN; type M9642
		resistor, fixed chip; ±5%; 1/8 W: unless otherwise stated
R1000	6-11024A89	47k
R1001	6-11024A93	68k
R1002	6-11024A73	10k
R1003	6-11024A61	3.3k
R1004	6-11024A73	10k
R1005	6-11024A47	820
R1006, 1007	6-11024A73	10k
R1008	6-11024A29	150
R1009	6-11024A75	12k
R1010, 1011	6-11024A25	100
R1012	6-11024A61	3.3k
R1013	6-11024A29	150
R1014	6-11024A59	2.7k
R1015	6-11024A73	10k
R1016	6-11024A89	47k
R1017	6-11024A73	10k
R1018	6-11024A97	100k
R1019	6-11024A77	15k
R1020	6-11024A10	24
R1021	6-11024A47	820
R1022	6-11024A89	47k
R1023	6-11024B04	180k
R1024	6-11024B01	130k
R1025	6-11024B04	180k
R1026	6-11024A51	1.2k
R1027	6-125A23	82; 1/2 W; carbon composition
R1028	6-11024A47	820
R1029	6-11024A75	12k
R1030	6-11024A83	27k
R1031, 1032	6-11024B04	180k
R1033, 1034	6-11024A65	4.7k
R1035	6-11024A65	4.7k
R1036	6-11024A73	10k
R1037	6-11024A65	4.7k
R1038	6-11024A89	47k
R1039	6-11024A61	3.3k
R1040	6-11024B04	180k
R1041	6-11024A89	47k
R1042	6-11024A51	1.2k
R1043	6-11024A75	12k
R1044	6-11024A73	10k
R1045	6-11049T50	432k ±1%; carbon film
R1046	18-83452F02	variable; 2k ±10%; 1/2 W
R1047	6-11040S12	16.2k; ±1/2%; carbon film
R1048	6-11040S09	15k; ±1/2%; carbon film
R1049	6-11024B14	470k
R1050	6-11049T50	432k; ±1%; carbon film
R1051	18-83452F02	variable; 2k ±10%; 1/2 W
R1052	6-11040S12	16.2k ±1/2%; 1/4 W, carbon film
R1053	6-11040S09	15k ±1/2%; 1/4 W, carbon film
R1054	6-11024A35	270
R1055	6-11024A83	27k
R1056	18-83686N06	variable; 250k ±20%
R1057	6-11040S09	15k ±0.5%; 1/4 W
R1058	18-83452F02	variable; 2k (Xmit Lev) ±10%; 1/2 W
R1059	6-11040S12	16.2k ±0.5%; 1/4 W, carbon film
R1060	6-11049S06	14k ±1%; 1/4 W, carbon film
R1061	6-11049S78	78.7 ±1%; 1/4 W, carbon film
R1062	6-11049S04	13.3k ±1%; 1/4 W, carbon film
R1063	6-11024A67	5.6k
R1064	6-11009E35	270; 1/4 W, carbon film
R1065	6-11009A50	1.1k; 1/4 W, carbon film
R1066	6-11009E49	1k; 1/4 W, carbon film
R1067	6-11009E50	1.1k; 1/4 W, carbon film
R1068	6-11049S06	14k ±1%; 1/4 W, carbon film
R1069	6-11009E53	1.5k; 1/4 W, carbon film
R1070	6-11009E57	2.2k; 1/4 W, carbon film
R1071	6-11024B10	330k
R1072	6-11009E97	100k; 1/4 W
R1073, 1074	6-11024A63	3.9k
R1075	6-11024A47	820
R1076	6-11049T30	267k ±1%; 1/4 W, carbon film
R1077	6-11024A67	5.6k
R1078	6-11049S04	13.3k ±1%; 1/4 W, carbon film
R1079	6-11024A73	10k
R1080	6-11024A25	100
R1081	6-11024A35	270
R1082, 1083 1084	6-11024A89	47k
R1085, 1086	6-11024A97	100k
R1087	6-11024A73	10k
R1088	18-83686N06	variable; 250k ±20%; 1/4 W (AGC)
R1089	6-11024A73	10k
R1090, 1091	6-11024A73	10k
R1092	6-11024A65	4.7k
R1093	6-11024B22	1 meg
R1094	6-11024A61	3.3k
R1095	6-11024A55	1.8k
R1096	6-11024A51	1.2k
R1097	6-11024A89	47k
R1098	6-11024A55	1.8k
R1099	6-11024A51	1.2k
R1100, 1101	6-11024A25	100
R1102	6-11024A65	4.7k
R1103	6-11024A89	47k
R1104	6-11024A65	4.7k
R1105	6-11024A73	10k
R1106	6-11024A89	47k
R1107, 1108	6-11024A73	10k
R1109	6-11024A65	4.7k
R1110	6-11024A35	270
R1111	6-11049S81	84.5k ±1%; 1/4 W, carbon film
R1112	6-11009E97	100k; 1/4 W, carbon film
R1113	18-83686N06	variable; 250k ±20%; 1/4 W, (Line Lev)
R1114	6-11024B04	180k
R1115	6-11024A93	68k
R1116	6-11024A65	4.7k
R1117	6-11040S09	15k ±1/2%; 1/4 W, carbon film
R1118	6-11040S12	16.2k ±1/2%; 1/4 W, carbon film
R1119	18-83452F02	variable; 2k ±10%; 1/2 W
R1120 (JU20)	6-11024A75	12k
R1121	6-11024B22	1 meg.
R1122	6-11049S06	14k ±1%; 1/4 W, carbon film
R1123	6-11049S61	52.3k ±1%; 1/4 W, carbon film
R1124	6-11049S04	13.3k ±1%; 1/4 W, carbon film
R1125	6-11024A89	47k
R1126	6-11049R83	8250 ±1%; 1/4 W; carbon film
R1127	6-11049S17	18.2k ±1%; 1/4 W; carbon film
R1128	6-11049T18	200k ±1%; 1/4 W; carbon film
R1129	6-11049T06	150k ±1%; 1/4 W; carbon film
R1130	6-11049T18	200k ±1%; 1/4 W; carbon film
R1131	6-11009F16	560k; 1/4 W
R1132	6-11024B22	1 meg
R1133	6-11024A95	82k
R1134	6-11024A49	1k
R1135	6-11009F06	220k; 1/4 W, carbon film
R1136	6-11024A67	5.6k
R1137	6-11024A35	270
R1138	6-11024A89	47k
R1139	6-11024A71	3.9k
R1140	6-11024A01	10
R1141	6-11024A75	12k
R1142	6-11024A77	15k
R1143, 1144	6-11024A73	10k
R1145	6-11024A65	4.7k
R1146 (JU18)	6-11009A73	10k; 1/4 W; carbon film
R1147, 1148	NOT USED	
R1149, 1150	6-11009E73	10k; 1/4 W, carbon film
R1151	6-11024A35	270
R1152	6-11024A75	12k
R1153	6-11024B22	1 meg
R1154 (JU26)	6-11009A63	3.9k; 1/4 W; carbon film (TRN5186A only)
R1155, 1156	6-11009D22	1 meg.
		switch:
S1001	40-82270M03	rotary, 16-position (Channel select switch)
S1002	40-83685N07	toggle, spdt (Intercom switch)
		transformer, audio:
T1001	25-83036L01	pri: leads 1 to 2 & 3 to 4; res. 25 ohms sec: leads 7 to 9 & 11 to 12; res. 250 ohms
T1002	25-83036L01	pri: leads 1 to 2 & 3 to 4; res. 25 ohms sec: leads 7 to 9 & 11 to 12; res. 250 ohms (TRN5187A)
		integrated circuit: (see note)
U1001	51-82609M67	octal D latch
U1002	51-83627M95	quad tri-state latch
U1003	51-83627M94	quad NAND
U1004	51-83627M93	dual D flip-flop
U1005	51-84561L44	triple 3-input NAND
U1006	51-84561L78	hex inverter
U1007	51-84561L03	hex inverter
U1008	51-83625M66	microprocessor
U1009	51-83627M03	octal tri-state latch
U1010	51-84561L08	triple 3-input NAND
U1011	p/o TRN5190	
U1012	p/o TRN5186	
U1013	51-82609M77	octal latch
U1014	51-82609M83	4-bit counter
U1015	51-83627M94	quad NAND
U1016, 1017	51-84561L11	dual monostable
U1018	51-83629M09	quad op amp
U1019	51-82884L48	quad analog switch
U1020	51-82609M05	quad op amp
U1021	51-83629M09	quad op amp
U1022	51-84371K74	quad comparator
U1023, 1024	51-83629M76	dual switched capacitor filter
U1025	51-82884L48	quad analog switch
U1026	51-83627M88	hex level shifter
U1027	51-82884L65	triple 2-channel MUX
		voltage regulator: (see note)
VR1001, 1002	48-82022N05	suppressor, transient; 63 V
VR1003	48-82256C61	Zener; 5.8 V
		crystal:
Y1001	48-82611M15	4.9068 MHz
		cable, ribbon, assembly:
W401	30-83139N02	26-conductor; flat; 1.5" used (Remote Control); includes ref. item P804 and PCB header P1001
		mechanical parts
	29-10271A15	PIN, bubble; 20 used
	14-84602K02	INSULATOR, crystal
	9-82808R09	SOCKET, IC: 24 contact (U1101)
	9-82808R10	SOCKET, IC: 28 contact (U1012)

notes:

1. For optimum performance, crystals, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.
2. Chip resistors are numerically coded for value, code format is: AAB; where AA are the two most significant value digits, and B is the number of zeros following the value digits. For example, a chip coded 103 is a 10k ohm resistor.

TRN5190A Code Plug Kit PL-8564-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		integrated circuit: (see note)
U1011	51-90002B02	EPROM; 4k x 8 (CODE PLUG)

TRN5186A Software Kit PL-8555-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		integrated circuit: (see note)
U1012	51-90006C23	EPROM; 8k x 8 (PROGRAM)
	54-84691N16	label