

J501

AUX +13.8V (A++) 2
AUDIO GROUND (GND A) 1

(PIN VIEW)

REFERENCE SYNTHESIZER POWER

P262B
RX LOCK# 7 8 SD2
SD3 9 SD1
SD0 10 SA0
RX LOOP 11 SA1
RAW RX AUDIO 12 SA2
AGC REF (800/896 MHz) 13 RX STROBE
MAIN +13.8V (A++) 14 +5V

(PIN VIEW)

UNIBOARD RECEIVER SYNTHESIZER

P801
RX2 LOCK# 2 1 +9.6V
TX MOD AUDIO 4 1
RAW RX2 AUDIO 6 1
TX LOCK# 8 1
PA FULL POWER# 10 1
PA ON# 12 1
PA KEY# 14 1
PA POWER CUTBACK# 16 1
TX LOOP 18 1
SA2 20 1
SA1 22 1
SA0 24 1
TX STROBE 26 1
RX1 LOCK# 28 1
SD1 30 1
SD0 32 1
RX1 LOOP 34 1
RX1 STROBE 36 1

(PIN VIEW)

CONTROL TRAY INTERFACE

P322B
TRANSMIT MOD AUDIO 7 8 +9.6V
SD0 9 AUDIO GROUND (GND A)
SD3 10 SD2
TX LOOP 11 TX LOCK#
SA0 12 MOD ENABLE
SA2 13 SA1
TX STROBE 14

(PIN VIEW)

UNIBOARD TRANSMIT SYNTHESIZER

P901
SA2 8 9 SD2
SD1 10 SD1
SD0 11 SD0
RX2 STROBE 12 SD3
AUDIO GROUND (GND A) 13 MAIN +13.8V (A+)
RAW RX2 AUDIO 14 MAIN +13.8V (A+)
AUDIO GROUND (GND A) 15 N.C.
RX2 LOCK# 16 N.C.

(PIN VIEW)

2ND RF TRAY INTERFACE

P402B
DRIVER FORWARD VOLTAGE 7 8 PA KEY#
PA FULL POWER# 9 CIRCULATOR LOAD TEMPERATURE
METERING FINAL REFLECTED VOLTAGE 10 THERMAL SUM POINT
MAIN +13.8V (A++) 11 AUDIO GROUND (GND A)
NORMALIZED IF ENVELOPE (800/896 MHz) 12 METERING FINAL FORWARD VOLTAGE
PA POWER CUTBACK# 13 PA ON#
14

(PIN VIEW)

UNIBOARD POWER CONTROL

J500
AUX +13.8V (A++) 3
+9.6V 2
ANTENNA RELAY ENABLE# 1

(PIN VIEW)

ANTENNA RELAY CONTROL

P603
1 AUX +13.8V (A++)
2 MAIN +13.8V (A++)
3 AUDIO GROUND (GND A)
4 GND B
5 OVERVOLTAGE ALARM#
6 BATTERY REVERT# (AC FAIL#)
7 PLUG KEY
8 N.C.
9 N.C.

(PIN VIEW)

MAIN POWER SUPPLY

P701
1 AUX +13.8V (A++)
2 PLUG KEY
3 OVERVOLTAGE ALARM#
4 BATTERY REVERT# (AC FAIL#)
5 GND B
6 NORMALIZED IF ENVELOPE (800/896 MHz)

(PIN VIEW)

STATION DC POWER CONTROL

J502
FINAL REFLECTED VOLTAGE 6 3 PA KEY#
AUDIO GROUND (GND A) 5 2 CIRCULATOR LOAD TEMPERATURE
FINAL FORWARD VOLTAGE 4 1 FINAL HEATSINK TEMPERATURE

(PIN VIEW)

FINAL PA INTERFACE

J512



(PIN VIEW)

CIRCULATOR LOAD TEMPERATURE

NOTE: AN ASTERICK FOLLOWING
A SIGNAL NAME INDICATES
AN ACTIVE LOW

J596
N.C. 6 3 PA KEY#
AUDIO GROUND (GND A) 5 2 N.C.
DRIVER FORWARD VOLTAGE 4 1 DRIVER HEATSINK TEMPERATURE

(PIN VIEW)

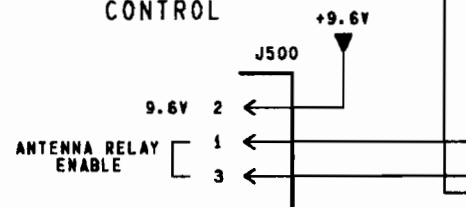
DRIVER PA INTERFACE

UNIB
POV
CON

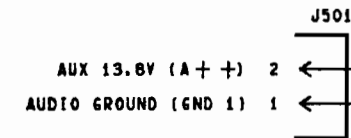
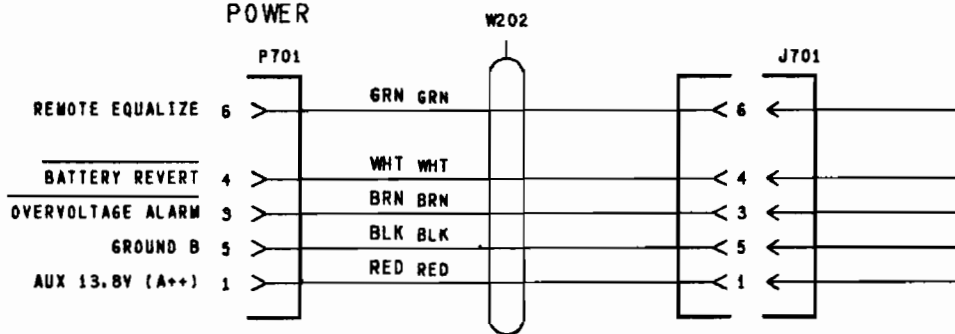
NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE IN OHMS, ALL CAPACITOR VALUES ARE IN MICROFARADS.

ANTENNA RELAY
CONTROL



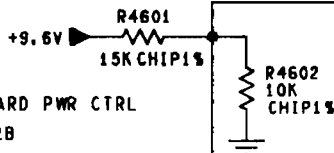
CONTROL TRAY
POWER



REFERENCE SYNTHESIZE
POWER

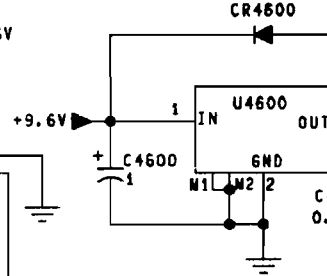
UNIBOARD POWER CONTROL

UNIBOARD PWR CTRL
P402B

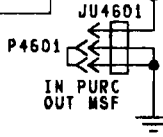
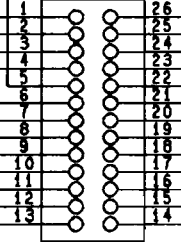


TRANSMIT SYNTH

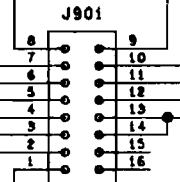
P322B



STATION CTRL
P801

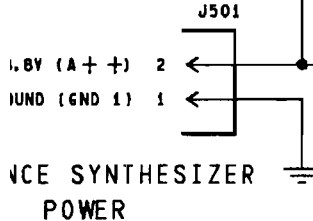
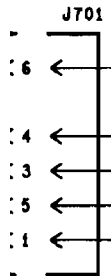
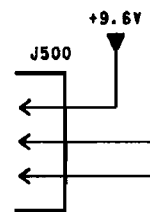


DATA / 2ND REC

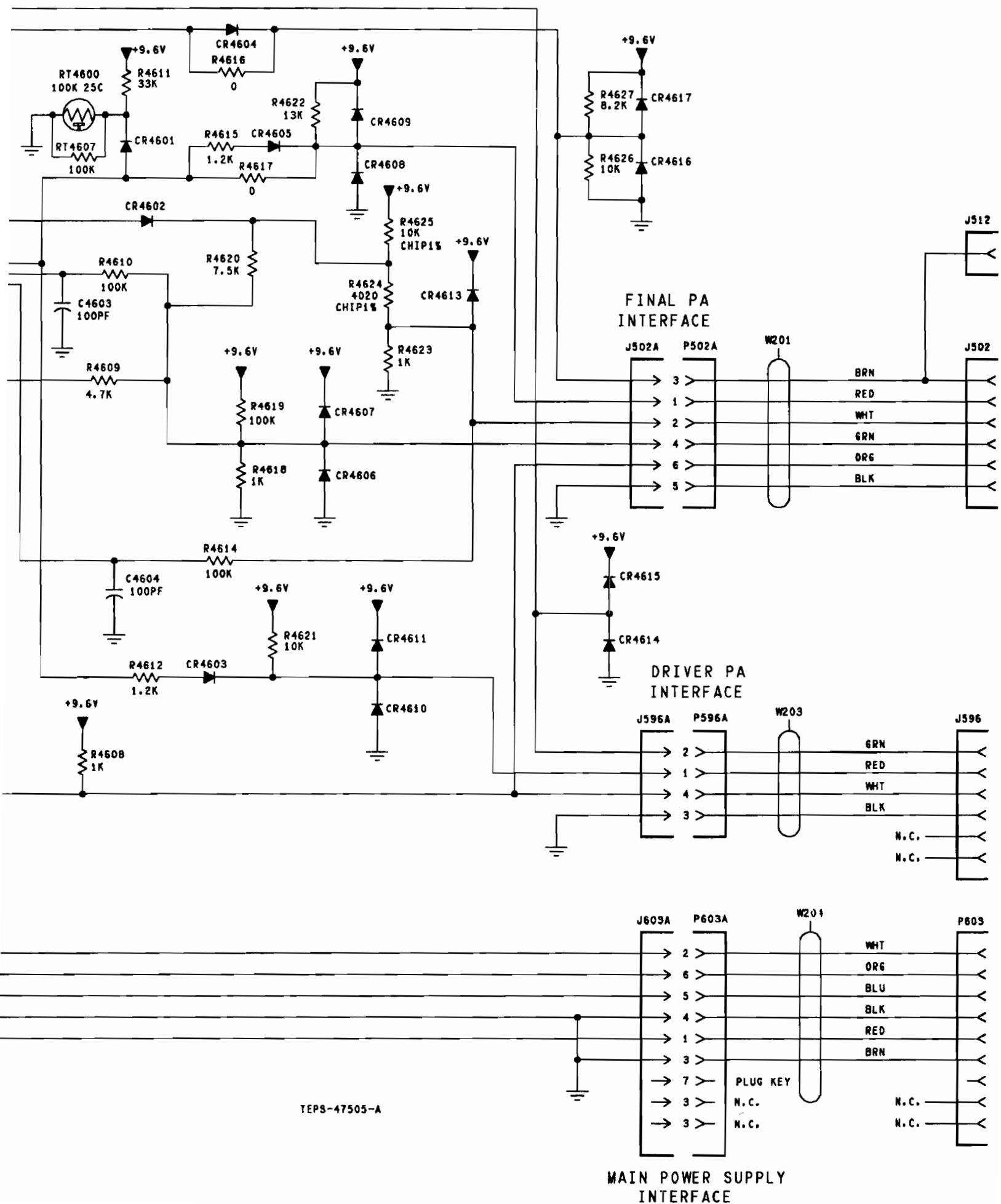


RESISTORS
ARE IN

LAY

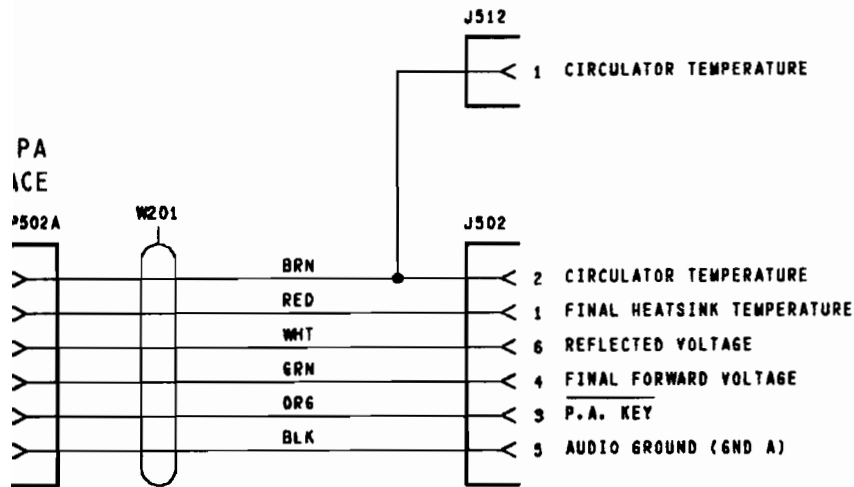


POWER SYNTHESIZER
POWER

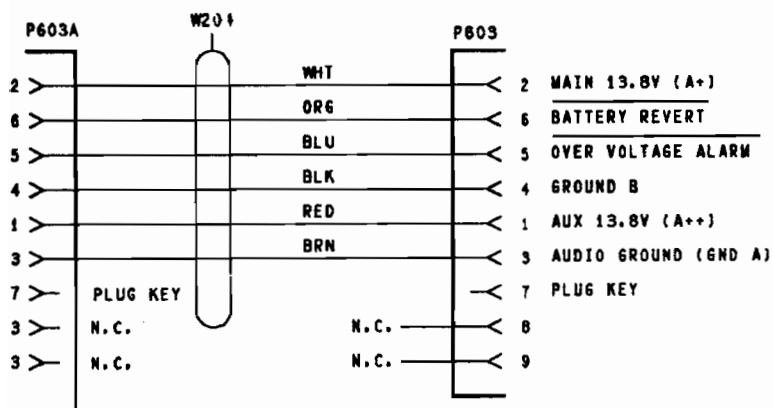
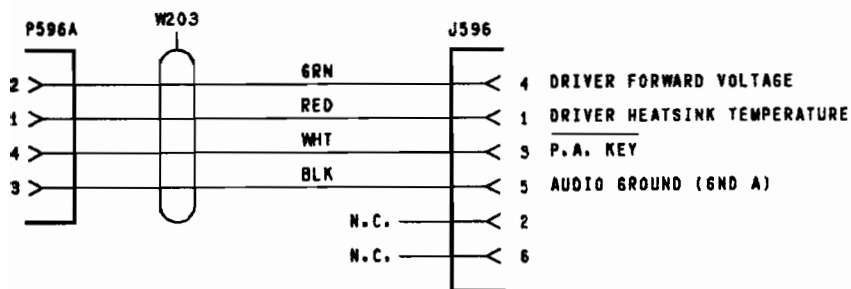


INTERCONNECT BOARD

SCHEMATIC DIAGRAM



VER PA
ERFACE



WER SUPPLY
RFACE

INTERCONNECT BOARD

SIGNAL INTERCONNECT CHART

MASTER BILL OF MATERIAL CHART

INTERCONNECT CHART

CONNECTOR DESCRIPTION		REF. DES.	FUNCTION		NOTES
ANTENNA RELAY POWER	J500		AUDIO GROUND (GND A)		
FINAL PA INTERFACE	J502A		GND B		
UNIBOARD RECEIVER SYNTHESIZER	P262B		ASC REF (800/896MHZ)		
UNIBOARD TRANSMIT SYNTHESIZER	P322B		MAIN +13.8V (A+)		
UNIBOARD POWER CONTROL	P402B		AUX +13.8V (A++)		
MAIN POWER SUPPLY	P603A		+5V		
STATION DC POWER CONTROL	P701A		+9.6V		
CONTROL TRAY INTERFACE	P801		ANTENNA RELAY ENABLE *		
2ND RF TRAY INTERFACE	P901		BATTERY REVERT * (AC FAIL *)		
REFERENCE SYNTHESIZER POWER	J501		CIRCULATOR LOAD TEMPERATURE		9, 14
CIRCULATOR LOAD TEMPERATURE	J512		FINAL FORWARD VOLTAGE		10, 11
DRIVER PA CONTROL	J596A		FINAL HEATSINK TEMPERATURE		6, 9
MSF/PURC SELECTOR	J4601		DRIVER HEATSINK TEMPERATURE		6
			MOD ENABLE		
			OVERVOLTAGE ALARM *		
			PA FULL POWER *		
			PA KEY *		
			PA ON *		
			PA POWER CUTBACK *		9
			RX2 LOCK *		
			RAW RX2 AUDIO		
			RX2 STROBE		
			RAW RX (RX1) AUDIO		7
			RX (RX1) LOCK *		7, 8, 14
			RX (RX1) LOOP		7
			RX (RX1) STROBE		7
			FINAL REFLECTED VOLTAGE		13
			NORMALIZED IF ENVELOPE (800/896MHZ)		
			SAB (SYNTH ADPS BIT 0)		
			SA1 (SYNTH ADPS BIT 1)		
			SA2 (SYNTH ADPS BIT 2)		
			SD0 (SYNTH DATA BIT 0)		
			SD1 (SYNTH DATA BIT 1)		
			SD2 (SYNTH DATA BIT 2)		

[illegible]

1. THIS CHART SHOWS ALL INTERCONNECTIONS MADE BY THE PLATING ON BOTH SIDES OF THE INTERCONNECT BOARD AND INCLUDES CABLING WHERE APPLICABLE.
2. ALL PIN NUMBERS IN EACH VERTICAL COLUMN ARE ELECTRICALLY COMMON UNLESS NOTED (SEE NOTES 6-13).
3. TO TRACE INTERCONNECTIONS FROM ANY STARTING POINT TO ALL OTHER COMMON POINTS PROCEED AS FOLLOWS:
 - STEP 1. FIND THE CONNECTOR DESCRIPTION OR REFERENCE DESIGNATION ON THE LEFT HAND COLUMN OF THE CHART.
 - STEP 2. FIND THE DESIRED PIN NUMBER, ALL PINS OF A SPECIFIC CONNECTOR ARE LISTED IN THE ROW THAT EXTENDS TO THE RIGHT.
 - STEP 3. NOTE THE FUNCTION OF THE DESIRED PIN. THE FUNCTION IS LISTED AT THE TOP OF THE COLUMN IN WHICH THE PIN NUMBER APPEARS, ALL OTHER PINS LISTED IN THE SAME COLUMN HAVE THE SAME FUNCTION. TRACE BACK TO THE LEFT HAND COLUMN TO FIND THE DESCRIPTIONS AND REFERENCE DESIGNATIONS OF OTHER CONNECTIONS HAVING ELECTRICALLY COMMON PINS.
4. (#) INDICATES FUNCTION SOURCE.

EXAMPLE:
RADIO INTERFACE CONNECTOR, P801, PIN 24 PROVIDES THE SAO (SYNTHESIZER ADDRESS BIT 0) INPUT TO THE INTERCONNECT BOARD FOR DISTRIBUTION TO THE TRANSMIT SYNTHESIZER CONNECTOR P322B, PIN 3 AND RECEIVER SYNTHESIZER CONNECTOR P262B, PIN 10.
5. (*) INDICATES ACTIVE LOW SIGNAL.
6. FINAL HEATSINK TEMPERATURE (AND DRIVER HEATSINK TEMPERATURE, IF APPLICABLE) GIVE(S) P402B PIN 10, THERMAL SUM POINT.
7. THESE ARE CALLED RX ON UNIBOARD CONNECTOR, BUT RX1 ON STATION CONTROL CONNECTOR TO DISTINGUISH FROM RX2 SIGNALS.
8. JUMPER J4601 GROUNDS RX (RX1) LOCK ON PURC STATIONS, J4601 PINS 1,2,3 ARE COMMON ON PURC ONLY, JUMPER MUST BE IN OPEN POSITION FOR MSF STATIONS.
9. DIRECT CONNECTION ONLY ON TRN7140A.
10. DIRECT CONNECTION ONLY ON TRN7140A, TRN7141A, TRN7164A, AND TRN7169A.
11. SIGNAL IS FED THROUGH CIRCUITRY TO GIVE P402B, PIN 12, METERING FINAL FORWARD VOLTAGE, EXCEPT ON TRN7140A, WHERE METERING IS DONE ON THE UNIBOARD.
12. FINAL REFLECTED VOLTAGE ON J502A IS FED THROUGH CIRCUITRY TO GIVE P402B, PIN 5, METERING FINAL REFLECTED VOLTAGE, EXCEPT ON TRN7140A, WHERE NO REFLECTED METERING IS PROVIDED.
13. J502A, PIN 3 SOURCES SIGNAL FOR TRN7140A AND TRN7169A, WHILE J512, PIN 1 SOURCES SIGNAL FOR TRN7142A.