SECURE CAPABLE STATION CONTROL BOARD

MODELS TLN3182A
TLN3188A
TLN3189A

1. INTRODUCTION

1.1 OVERVIEW

This document describes the operation of the Secure capable Station Control Board (SSCB), which has been designed for use in the Digital *MSF* 10000 repeater/base station. The kit number of the SSCB depends upon the frequency band of the station in which the SSCB is used:

TLN3182A - VHF/UHF NB
TLN3188A - UHF
TLN3189A - VHF

The SSCB is housed in the control tray attached to the top of the RF tray, and is compatible with the Trunked Tone Remote Control (TTRC) board (TLN3185A, TLN3114A) as well as the optional Secure Module (TLN3045A). The SSCB also maintains compatibility with all existing optional expansion modules which can be housed in an expansion tray attached to the top of the control tray.

2. FUNCTIONAL DESCRIPTION

2.1 DC-DC CONVERTER

2.1.1 Operation

The dc-dc converter is a current-mode controlled forward converter operating at 200 kHz. It produces + 5 V for the SSCB and the other connected control tray boards. It also incorporates various self- and system protection features. Input to the converter is the Aux 13.8 V (A+ +) voltage. Reference voltage for the circuit is generated internal to the control chip, U843. System protection features are handled by U842C for overvoltage faults, U842B for under voltage faults, and U842A for insufficient A+ + voltage to protect against over discharge of batteries during battery revert. U842A also provides a test function (Reset_switch*) which allows the converter to run regardless of the input voltage, and concurrently resets the station.

While any of the above fault conditions hold the station reset, only the overvoltage condition will force the converter to shut down. In this case, the converter will turn off and allow the 5 V to discharge down to approximately 2 V before attempting to restart. For a hard fault, the supply will continuously turn off and attempt restart while holding the station in the reset mode. Overcurrent protection for the power supply is provided automatically on a pulse-by-pulse basis due to the current mode control topology (U843-pin 3).

2.1.2 Troubleshooting

In the event of incorrect voltage measured at TP6, Jumper JU12 can be removed to disconnect the station load from the power supply as well as isolating part of the protection circuitry. Before doing this, the type of fault should be determined. If the supply is cycling on and off from approximately 2 V to 6 V, the most likely failure is in the feedback divider network (R2, R7). Either R2 is open or the wrong value, or R7 is shorted or the wrong value. If the fault disappears when the jumper is removed, the problem is in the protection circuit (U842C and associated components).

Overvoltage faults can be caused by any series element from T1 to JU12, as well as feedback divider network errors and failures in the control and driver circuitry on the primary side of the transformer. Overcurrent faults caused by short circuits external to the power supply can be isolated by removal of JU12. Since the supply goes into a fold-back mode during overcurrent, the output voltage drops very rapidly once the current limit threshold value is reached (approximately 1.5 amps). Problems with the station stuck in reset mode with valid + 5 V present at TP6 are most likely caused by circuitry associated with U842B, U842D, Q706, or Q705.

2.2 AUDIO PROCESSING SECTION

The Audio Processing section consists of three parts: receive audio processing, transmit audio processing, and audio routing.

2.2.1 Receive Audio Processing Section

2.2.1.1 OPERATION

The schematic diagram for this section is on the top left part of Sheet 4. The input to the receive audio processing section is baseband audio, which is demodulated from the RF signal by the receiver in the RF tray.

2.2.1.2 TROUBLESHOOTING

When a strong RF signal is applied to the receiver, the demodulated baseband FM (audio) should be present at

technical writing services
1301 E. Algonquin Road, Schaumburg, IL 60196

68P81083E92-O
8/31/90-UP

RX1 AUDIO (U811-14). For an RF signal with 60% deviation at a 1 kHz modulation frequency, the RX1 AUDIO level should be about 350 mV rms. If this audio is not present, first check the +9.6V supply on TP5 and the VB bias level on U819-12. Next, verify that JU11 is in the proper position. Also check the signal at TP3 QUAD AUDIO, which is not filtered or gated. This signal should have a level of about 300 mV rms. If audio is present at TP3 but not at U811-14, try adjusting the Rx level digital pot U824. If none of these methods works, one of the circuit blocks in the receive audio processing section may have malfunctioned. Each of the following blocks may be checked on an input-to-output basis and repaired if found faulty: PL filter U841, digital pot U824, expander U815, flutter-fighter hybrid HY804, audio gate U811, and op-amps U818 and U819.

2.2.2 Transmit Audio Processing Section

2.2.2.1 OPERATION

The schematic diagram of the transmit audio processing section is shown on the top right part of Sheet 3. The output of this section is TX MOD AUDIO, which is sent to the FM modulator to be impressed upon the RF output of the transmitter, and sent out over the air. This section has several inputs that originate from the SSCB audio routing circuitry.

2.2.2.2 TROUBLESHOOTING

When a large audio signal is applied to the microphone input with a local PTT, the limited and filtered audio signal should be present on TX MOD AUDIO at TP4. If this audio is not present, check the +9.6V supply at TP5 and the VB bias level at U838-5. If the TX MOD AUDIO signal is not found, make sure the mic audio is present at the Tx audio summing amp output U814-1. If this signal is absent, check the Audio Routing Section described in the next paragraph. Also check the signal at U838-7, which should be in full limit (driving the op-amp to its supply rails). Trace the flow of this signal through the splatter filter (U838-7, U838-1, U837-7, U8200-1). The splatter filter output should be similar in peak to peak amplitude to the limiter output, but not so much of a square wave (that is, closer to sinusoidal). If audio is present at U8200-1 but not at TP4, try adjusting the Max Deviation level digital pot, U831. If none of these methods works, one of the circuit blocks in the transmit audio processing section may have malfunctioned. Each of these blocks may be checked on an input to output basis, and any bad ones repaired or replaced.

2.2.3 Audio Routing section

2.2.3.1 OPERATION

Most of the audio routing section is shown on the left half of schematic Sheet 3. Its primary function is to properly distribute audio signals from all sources to all destinations connected to the SSCB. The audio routing section operates on the following audio inputs and outputs, as shown in Tables 1 and 2.

Table 1. Audio Input Description

Inputs	Description
TX AUDIO	Notch filtered audio from TTRC wireline
IN MRTI AUDIO	Audio from MRTI phone patch
LOCAL AUDIO	General purpose audio to/from expansion modules (also common with MIC AUDIO signal)
MIC AUDIO	Audio from local user microphone
RX1 AUDIO	Audio from receive audio processing section
ALERT TONE AUDIO	Audio from alert tone encoder on SSCB
SECURE RX AUDIO	Audio from optional secure board for speaker/wireline
RX2 AUDIO	Processed audio from optional 2nd rcvr board
CODED MOD AUDIO	Audio from optional secure board to be transmitted
TKG MOD AUDIO	TDATA/failsoft from TTRC to be transmitted
SEC ALERT TONES	Tones from option secure board (encode/decode only)
TX DATA AUDIO	General purpose data from expansion modules
GCC DATA AUDIO	1200 or 4800 baud data from optional GCC
RAW TX AUDIO	Unfiltered audio from TTRC wireline
PL ENCODE AUDIO	Audio from PL/connect tone encoder on SSCB
RAC_LN_AUD	Encoder output of optional RAC expansion module

Table 2. Audio Output Description

Outputs	Description
SUMMED TX AUDIO	Audio to transmit audio processing section
LINE AUDIO	Audio to TTRC wireline
SELECT AUDIO	Volume adjusted audio to expansion modules (especially DMP speaker)
OUT MRTI AUDIO	Audio to MRTI phone patch
SPKR AUDIO	Amplified audio to local user speaker
TX AUDIO	Wireline audio to secure board for encryption and to expansion modules
RAW TX AUDIO	Unfiltered wireline audio to optional secure transparent board
LOCAL AUDIO	Local audio to optional secure board for encryption
IN MRTI AUDIO	Audio from MRTI phone patch to secure board for encryption

Some audio inputs are enabled using audio gates, which respond to various PTT and squelch conditions as shown in Table 3. Some other audio inputs are enabled using 3 pin jumpers (see jumper table). TX DATA AUDIO can be summed into the SSCB transmit path before or after the maximum deviation adjust circuit (JU4). GCC DATA AUDIO can be routed through the pre-emphasis/splatter filter path for 1200 baud data or after the maximum deviation adjust for 4800 baud data (JU6).

Table 3. Audio Gate Enabling

Condition	Audio Gate
TX AUDIO	U810A
IN MRTI AUDIO	U817B
LOCAL/MIC AUDIO	U810C
RX1 AUDIO	U810B
ALERT TONE AUDIO	U817C/U817D

2.2.3.2 TROUBLESHOOTING

The routing performed in this section depends on the configuration of the SSCB in the station. This configuration is determined by two factors: code plug programming and jumper settings. If the audio routing section is not performing as expected, one of these two factors is most likely to be the problem. Refer to the jumper table to determine proper jumper settings, and refer to the software description for proper code plug programming. If these two items are found to be correct, and audio routing problems still exist, the circuitry in this section should be checked.

First, check the +9.6V supply at TP5 and the VB bias level at U810-1. If an audio gate does not operate as expected, check the audio gate control input. A high level (about +9.6V) at the control inputs of T-gates U810, U811, and U812 allows audio to pass through the positive gate (no bubble shown at the input) and shuts off the signal from passing through the negative gate (with a bubble). Conversely, a low level on the control input allows audio to pass through the negative gate and shuts off the positive gate. Thus, for audio gate U817, a high level (about +9.6V) at the control input allows audio to pass, and a low level shuts it off. If the control input is correct, but the gate does not respond properly, the audio gate IC is probably bad. If the control input is not as expected, check the level shifters U813 and U816. These ICs shift the 0-5V ASIC control outputs to the 0-9.6V levels required by the audio gates. A low voltage on the input of the level shifter should drive the output low, and a +5V level on the input should drive the output to +9.6V. If that's not what happens, the level shifter IC is probably bad. If none of the foregoing checks isolates the cause of the audio routing problem, check quad summing amp U814. If audio is present on the resistor inputs but not on the outputs, and the +9.6V and VB levels are correct, U814 is probably bad.

2.3 SQUELCH CIRCUITRY

The squelch detection circuitry on the SSCB responds to the signal strength of the incoming receiver audio. The QUAD AUDIO signal from TP3 is routed both to the receiver and to the repeater squelch detectors. These detectors drive control lines to the logic section, which are used in keyup and gating arbitration. For information on PL and DPL coded squelch operation, refer to the logic section of this description.

2.3.1 Troubleshooting

Properly operating squelch detectors should indicate squelch conditions when an RF signal below the adjusted threshold is being received. The detectors should unsquelch as soon as the signal strength goes above the set level. If the squelch circuit malfunctions, first try adjusting the digital pots in the receiver and repeater squelch detection circuits. A relatively easy and quick way to check the operation of the squelch circuitry is to use the ACC DIS switch on the front panel to enable the front panel Squelch control. With no RF input to the station, a noisy signal should appear on TP3 QUAD AUDIO. With the Squelch control fully CW, this noisy input should squelch the receive audio. With the Squelch control full CCW, the detector should not squelch the receiver, and the noisy signal should pass through to the speaker. If the receive channel has PL/DPL connect tone enabled, the PL DIS switch must also be used to hear the signal at the speaker. If these simple checks don't isolate the source of a squelch problem, refer to the squelch troubleshooting chart in the manual.

2.4 LOGIC HARDWARE SECTION

The logic hardware description can be broken down into five broad parts: microprocessor core, data communications circuitry, tone encoders/decoders, general I/O, and reset circuitry.

Many of the functions of the logic section are implemented with Application Specific Integrated Circuits (ASICs). The SSCB uses two of these custom ASICs, which were specifically designed for this product. The ASICs can operate in one of two modes, depending on the state of the MODE pin (18). U801 operates in the standard mode (with MODE pulled high), and serves as a specialized microprocessor support chip, with additional I/O and data communication features. U802 operates in the I/O mode (with MODE pulled low), and serves as an addressable collection of input buffers and output latches.

2.4.1 Microprocessor Core

The schematic diagram of the microprocessor core is located on Sheet 2. Its function is to run the software that controls the station. Most of the core functions are carried out using five integrated circuits.

2.4.2 Data Communications Circuitry

The SSCB logic section communicates with other modules in the station through three primary channels; the IPCB, the MUXbus, and the high speed ring (HSR).

2.4.3 General Input/Output

The SSCB logic section has a great deal of input/output (I/O) capability, which is needed to control station functions and monitor station status. The I/O section also allows a local user to change the state of the station, and to observe station status conditions.

2.4.4 Tone Processing

2.4.4.1 TONE ENCODING AND DECODING

Two 4-bit encoders are included on the SSCB. They are driven by 8-bit latch OL10 from the I/O ASIC. The tone decoding capabilities of the SSCB are complementary to its tone encoding functions. The SSCB detects incoming PL tones or DPL codewords in a conventional coded squelch system, and incoming connect/disconnect tones in a trunked system. These tones and/or codewords are part of the receiver modulation.

2.4.5 Reset Circuitry

The power up reset circuitry is shown on the bottom of schematic Sheet 1. A block diagram of this section is also shown in Figure 1.

DELAYED RESET is inverted by Q822 to form EXPANSION RESET*, which should hold other control tray boards and expansion modules in reset during SSCB self-diagnostics. The microprocessor can also activate EXPANSION RESET* during normal program execution, by turning on Q823 with a general purpose output pin.

2.4.6 Logic Hardware Troubleshooting

The SSCB software is capable of generating several error codes on the front panel seven segment display. Refer to the SSCB software description section for a list of these diagnostic error codes.

If there is a suspected failure in the SSCB logic section first check the +5V power supply pins on each of the logic devices U800 through U804, and on U807. Next, look at the RESET* line at TP10. This line should be at a steady high, with no superimposed pulses. Also look at the DELAYED RESET line, which should be at a steady low with no superimposed pulses. If the signals on the reset lines are not as expected, check to see that ICs U800 through U804 are all properly seated in their sockets. (Improper seating is especially likely for 28-pin DIP U803.) Also verify that EPROM U803 is programmed with the correct version of the software for the particular SSCB being worked on. (U803 must be compatible with the EEPROM codeplug programming internal to U800, or the system will not work) Next, check to see that the address timing signals (A0–A7) for the demultiplexed low order address bus are present at the relevant outputs of U801 (pins 66–73). If the A0–A7 address timing signals are not found, ASIC U801 is probably bad. If ASIC U801 and EPROM U803 both seem to be OK, and the RESET* line is high, next check microprocessor U800. A properly functioning U800 will drive the E line (U800-5) with a 1.9872 MHz square wave. If all these chips seem to be functioning properly, check ASIC U802 for data bus inputs as well as correct output latch levels.

If an error code indicates that there is a problem with the HSR, first verify that JU1 and JU2 are installed in the correct positions. Next, verify that HSR CLK is an E/2 frequency square wave, and that HSR SYN goes high every 40 HSR CLK cycles. If these signals seem to be correct, but HSR problems still exist, remove the modules from J804 and/or J803, and place JU1/JU2 in the HSR loopback position (JU1 alternate, JU2 normal position). If the error code persists with all other modules disconnected and the HSR looped back by JU1/JU2, then U801 is probably bad.

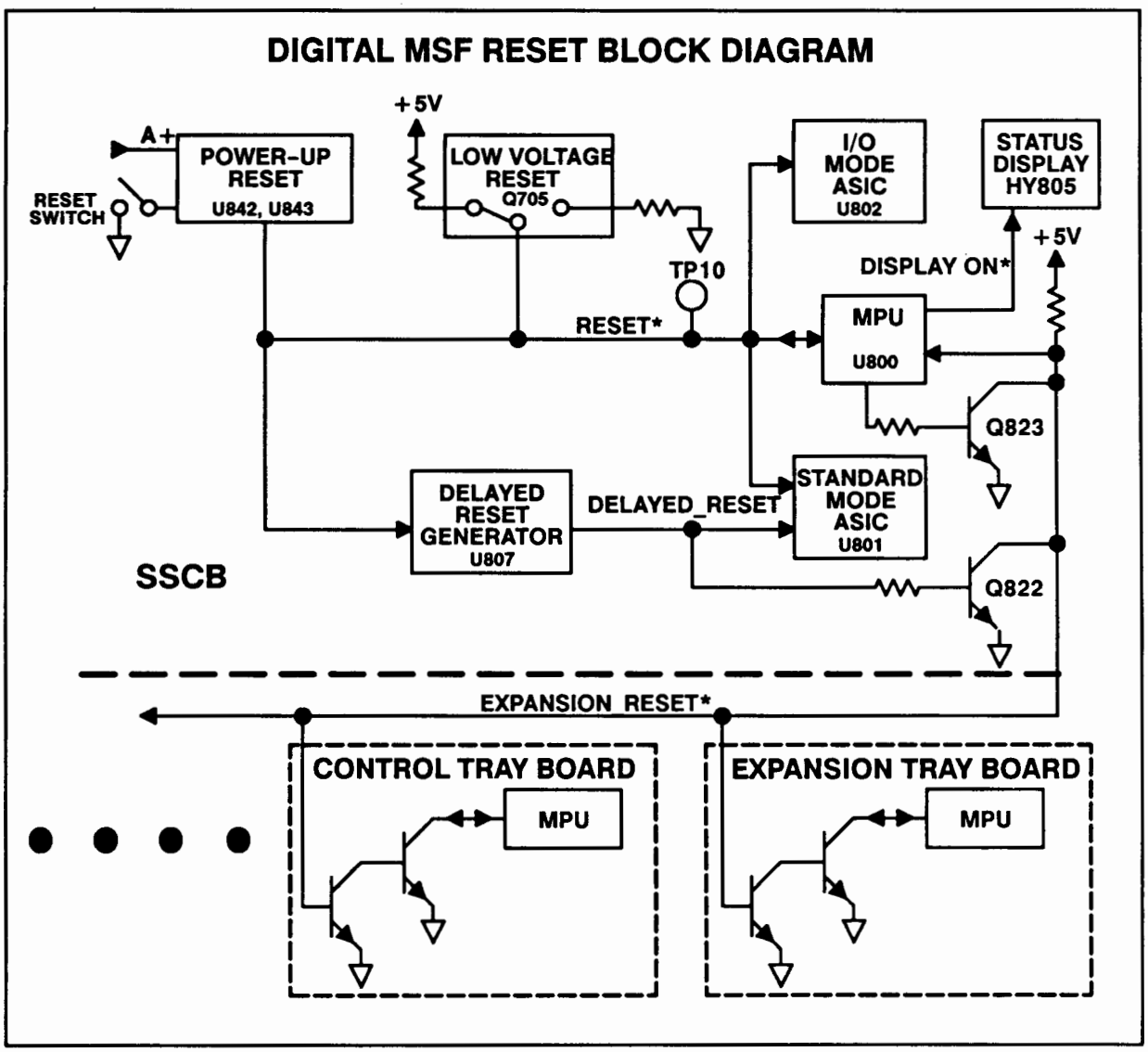


Figure 1. Reset Block Diagram

If problems are encountered with the MUXbus, verify that DS* is a 3105 Hz square wave and that the address lines are being driven. The address nibble BA0–BA3 must be incremented modulo–16 for proper operation. This means that the BA0 line (which toggles at DS*/2 rate = 1553 Hz) should toggle twice as fast as BA1 (DS*/4 = 776 Hz), which is twice as fast as BA2 (DS*/8 = 388 Hz), which is twice as fast as BA3 (DS*/16 = 194 Hz). To verify proper MUXbus data generation, the SSCB can be forced to write to the MUXbus BD0*–BD3* bits. When a MUXbus data bit is set at only one MUXbus address, the signal on the specific MUXbus data pin should be a short low-going pulse from the 5V high level, repeating at a frequency of DS*/16 = 194 Hz. The following chart indicates one way to force the SSCB to drive a MUXbus data bit at only one address: If these signals cannot be verified, ASIC U801 is probably bad.

Table 4. MUXbus Addressing

Signal	Action
BD0* (U801-38)	depress XMIT switch
BD1* (U801-39)	depress XMIT switch
BD2* (U801-40)	ground TP9 (LOC PTT)
BD3* (U801-41)	set to CH1-using ACC DIS, SELECT/CHANGE switch

The procedures for troubleshooting the tone encoders/decoders and wattmeter buffers are similar to those already suggested for troubleshooting the audio sections. Each circuit block can be analyzed on an input to output basis, and any malfunctions isolated and repaired.

When a PL signal is present on the receive audio, the PL DECODE DATA (U800–32) signal should be a 0–5V

square wave of the same frequency. An easy way to verify the wattmeter buffer operation is to monitor the buffer outputs (FWD PWR U806–8 and RFL PWR U806–14). The DC levels on these outputs should respond to front panel Po power adjustments while the transmitter is keyed. The tone encoders can be checked by looking at the output of the D/A filters. When an alarm condition is present, an alert tone sine wave burst should be visible at U818–1. Alarm tones can be generated by setting DMP bits at MUXbus address 12. When PL/DPL/connect tones are being generated, a sine wave should be visible at U8200–1. DPL code 031 can be generated by keying the station with a LOC PTT with the station set to channel 1, mode 1.

2.5 SOFTWARE DESCRIPTION

The Station Control board firmware begins execution at the location contained in its RESET vector whenever the station powers-up or is reset. This location is the beginning of the main background routine of the Station Control board firmware. Once initialized, this routine is basically nothing but an endless loop (the background) which calls all of the non-interrupt-driven routines. However, at its beginning, the firmware calls a startup diagnostics module, "sscb_reset_diags.asm," which runs to completion before the background loop begins. As the name implies, this module performs diagnostic tests of the Station Control board. When the diagnostics begin (i.e.: immediately upon station power-up), all segments and digits of the three digit, seven segment Status display LED should light, and stay lit until the circuitry that drives the display has been verified. This indicates that the Station Control board has started its diagnostics.

The sscb_reset_diags.asm routine must initialize some of the registers in the microprocessor before the actual hardware diagnostic tests can start. These registers determine the microprocessor's Computer Operating Properly (COP) watchdog time-out time; set up the Serial Communications Interface (SCI) to communicate at the same baud rate and with the same message protocol as the other boards on the Inter-Processor Communications Bus (IPCB), and set up a service to bypass the flag that normally tells the board to access its EEPROM.

When initialization is complete, the routine sets an output pin to hold the Expansion Reset line active. This prevents the on-board circuitry that activated Expansion Reset immediately upon Station reset or power-up from releasing the line after about 200 milliseconds, which would hold any and all remote boards in reset. The Station Control board diagnostics now begin. Since these tests can yield a number of error conditions, errors are indicated either by flashing the Station Control board's entire Status display or by displaying a formatted error code within the Status window. There are two types of error classes: fatal and non-fatal. Fatal errors are severe enough to prevent proper operation of the Station Control board, and cause the Station Control board to reset. Non-fatal errors, however, are just warnings. They are not severe enough to prevent operation, and should not cause a reset.

Failures of some of the initial diagnostics tests described below are indicated by flashing of the entire Status display. At this point, the operation of the display-driving circuitry, IRQ-interrupts, and external RAM has not yet been verified. The display-driving circuitry and IRQ interrupts are required for displaying error codes within the Status window, and the external RAM is needed to hold the error codes for display. The Status window display cannot be used until those tests have been done.

All failures that flash the entire Status display are fatal errors. For each error of this type that it finds, the sscb_reset_diags.asm routine calls a specific error handler routine, which contains a number peculiar to that error. The error handler flashes the Status display for that specific number of repetitions, to identify the error. It then goes into a wait condition, not servicing the COP timer, which eventually times-out and resets the Station Control board. Failures that display error codes in the status window, on the other hand, may be fatal or non-fatal. When sscb_reset_diags.asm detects an error of that type, it calls a different error handler routine, which writes an error code value to the front-panel Status window. If the error code is fatal, the Station Control firmware displays it for five seconds and then stops servicing its COP timer. Again, COP eventually times-out and resets both the Station Control Board and, via the Expansion Reset line, any board(s) connected to it. If the error code is non-fatal, the Station Control firmware displays it for two seconds and continues without a reset.

If a fatal error is left uncorrected, the test that found it will, of course, fail again, re-display the same error code, and once more reset. This is an endless cycle that will continue until the failure is corrected.

Sscb_reset_diags.asm checks two major sections of the Station Control board hardware: the digital hardware and the audio hardware. Internal digital diagnostic tests are done first, followed by external digital diagnostic tests, followed by audio diagnostic tests. All tests are performed after every Station Control board reset. Internal digital diagnostic tests are tests which verify operation of the Station Control board's digital circuitry as stand-alone hardware. External digital diagnostic tests verify operation of the Station Control board's digital circuitry as part of the overall Station Control Tray. Finally, audio diagnostic tests verify operation of the Station Control board's audio circuitry.

The first internal digital diagnostic test checks that the segment-select lines of the Status display and the internal IRQ signal are working properly. If not, the specific error handler called should flash the entire display twice, then reset the board.

The second internal digital diagnostic test checks that each of the eight bits in every byte of the external RAM can be toggled high and low. After each RAM byte is checked, it is cleared so that all RAM bytes will initially be zero when the diagnostics are complete. If any external RAM byte fails this test, the specific error handler called should flash the entire display four times, then reset the board.

The third internal digital diagnostic test checks that the IRQ (Interrupt Request) is working. The IRQ interrupt

should be generated whenever 640 microprocessor E-cycles have been clocked by the MUXbus-driving portion of the standard ASIC. It should occur every 320.061 μsec (640 cycles at 1,987,200 cycles per second). It signals the Station Control board that new MUXbus data is ready to be read, updates the Station Control Software System Timer, and controls the multiplexing of the front-panel display. If this interrupt test fails, the specific error handler called should flash the entire display twice, then reset the board. If it passes, the front-panel display, which should have shown three eights (8.8.8.) up to this point, should become blank.

The fourth internal digital diagnostic test checks that each of the eight bits in every byte of the internal RAM in the microprocessor can be toggled high and low. After each RAM byte is checked, it is cleared so that all RAM bytes will initially be zero when the diagnostics are complete. If any byte fails to pass this test, an error handler routine is called to write the relevant fatal error code to the front-panel Status window. (This and all the following diagnostic tests display their results in the Status window, since at this point the display circuitry has passed its diagnostic tests and is, therefore, available.)

The next section of the sscb_reset_diags.asm routine checks the microprocessor configuration, i.e. checks the information stored in its CONFIG register. If the information is wrong, the routine checks to determine whether or not it can be corrected without total erasure. If so, sscb_reset_diags.asm makes the correction and writes a fatal error code to the Status window. If not, sscb_reset_diags.asm erases the CONFIG register, which erases the entire internal EEPROM, and reprograms CONFIG for the desired features. (Note that erasing the CONFIG register erases the entire internal EEPROM, which is the codeplug.) The routine then writes a different fatal error code to the Status window. In either case, COP will then time-out and reset the system.

Being reset will, of course, restart the diagnostics (i.e.: repeat sscb_reset_diags.asm). However, since the CONFIG register was (ideally) corrected before the system reset, this test should not fail on the second pass. Note, though, that if the internal EEPROM was erased, the Station Control firmware may get caught in a fatal error loop due to some other error.

Unless otherwise specified, failures in all the following tests are fatal errors. When one of these happens, the diagnostics write a fatal error message to the status window, and reset the system. In fact, until the problem is corrected, the system may be expected to continually recycle the diagnostic routines, failing and resetting repeatedly at the same point, which is the "fatal error loop" referred to above.

The diagnostic routine next calculates the single-byte-add checksum of the Station Control firmware. The test fails if this calculated checksum does not match the value stored in the Station Control firmware.

Sscb_reset_diags.asm next tests the Standard and I/O ASICs. The ASIC tests are considered to be internal tests, meaning that each ASIC is tested as a stand-alone device; i.e.: all outputs are looped back to the inputs. (In the external diagnostics section of the routine, the ASICs are tested as part of the overall Station Control Tray.) The first test performed on the Standard ASIC is verification of its Output Latches. The test routine writes a known set of data to the Output Latches; then reads back the corresponding loopback Input Buffers. The test fails if the Output Latches and Input Buffers do not agree.

The second test of the Standard ASIC checks the MUXbus circuitry. The routine first checks MUXbus address cycling. Next, it checks the operation of the the Data Strobe line, verifying that both 1s and 0s can be read at all MUXbus addresses. A discrepancy in either addressing or data integrity is a failure.

The next set of tests on the Standard ASIC is associated with the High Speed Ring (HSR). The first HSR test is an operational check of the Ring Synchronization and Ring Clock lines. The diagnostic routine first reads two watchdog bits (one for Ring Sync and one for Ring Clock), in the Standard ASIC hardware to determine whether or not Ring Sync and Ring Clock are operating properly. Next, it writes a known set of data to the Station Control portion of the HSR, and then reads back the entire HSR. If the data written to and read back from the Station Control portion do not match, or if the Trunked Tone Remote Control and Secure portions are not zero, the HSR fails. (The Station Control board is in internal test mode at this point, and should not be connected to the HSR. Therefore, the Trunked Tone Remote Control and Secure boards should not be able to write to the HSR.) If the test passes, it repeats with an inverted version of the same data set, using the same pass/fail criteria.

The next section of sscb_reset_diags.asm compares various parameters of the Station Control codeplug and the Station Control firmware. The codeplug data must first be read from EEPROM into RAM. (If an external, serially-addressed EEPROM is present on the Station Control board, its data will also be read into RAM. A serially-addressed EEPROM that does not respond to commands is a failure.) After the routine reads the EEPROM(s), it clears the flag that has bypassed EEPROM access prior to this point. The first comparison is between the Module ID stored in the codeplug and the Module ID stored in the firmware. The second comparison is between the codeplug version and the firmware version. The third comparison is between the single-byte-add checksum of the Station Control codeplug. as calculated by the diagnostic routine, and the checksum value stored in the Station Control codeplug. A mismatch in any of these comparisons is a failure.

The routine next checks to determine whether or nor there was a reset during an EEPROM update. An image of the EEPROM is always kept in RAM. A user can write this RAM image (which he or she may have modified) to the EEPROM by issuing a Write-EEPROM-From-RAM command via the IPCB. This command first erases the entire EEPROM, setting all bytes to

hexadecimal value FF. The firmware then does a byte-by-byte copy of the modified RAM image to the EEPROM area, which can take up to 15 seconds. The copy starts at the ***second*** byte in the EEPROM address space. The ***first*** byte, which was previously set to FF hex during the erasure, is not overwritten until the copy has been completed, at which time it is set to 00. If the copy is interrupted by a reset before completion, that doesn't happen. Therefore, if the first byte in the EEPROM address space is non-zero it indicates that the EEPROM may be corrupted, and is a failure.

The routine next checks to determine whether or nor there was a reset during a user area update. What's stored in the user area is dynamically-changeable data that must be preserved between resets, so this area is part of the EEPROM address space. An update of the user-area should reprogram only the bytes in that section of the EEPROM, one of which is a user-area check byte that functions for the user area in the same way that the first byte of the EEPROM functions for the entire EEPROM. That is, the check byte is initially erased to FF hex, and cleared to 00 when the update is completed. Therefore, a non-zero value of the check byte indicates that the user area may be corrupted, and the diagnostics will flag it as a failure.

The last of the internal tests in the diagnostic routine checks the IPCB. The routine writes a test pattern to the IPCB, then checks to determine whether or not the data was received properly.

At this point, the internal Station Control diagnostics are complete. Audio diagnostic tests may now begin. The Disable LED should light to indicate that the digital hardware tests have been completed, and dashes (---) should be displayed in the front-panel Status window to indicate that audio diagnostics are in progress.

The diagnostic routines first check the Analog-to-Digital (A-to-D) Converters of the microprocessor. If any of the A-to-D Converters fail, the diagnostics should send a ***non***-fatal error code to the Status window for display. A non-fatal error that occurs in this section of the diagnostics is handled differently from fatal errors that occurred in the previous section. Once the non-fatal error code is displayed, the operator has two seconds to activate the Acc Dis switch on the front panel of the station. This "freezes" the system at the current stage of the diagnostics, to expedite troubleshooting. (Among its other advantages, this allows audio gating, which may not be possible in normal operation.) If the switch is hit late, freezing the routine at the wrong stage, the operator can simply hit the Reset switch and try again on the next pass.

Failures in all of the remaining tests are non-fatal errors; and should display the appropriate non-fatal error codes in the Status window.

The routine first checks the PL Tone generator circuit. If the192.8 Hz tone is not present at the appropriate A-to-D Converter input when the tone is enabled, the test fails.

The routine next checks the Alert Tone generator. If the 1000 Hz tone is not present at the appropriate A-to-D Converter input when the tone is enabled, the test fails.

The routine next checks the Station Control board for PL signal at the transmitter. If the 192.8 Hz tone is not present at the TP4 A-to-D Converter input when the tone is enabled, the test fails.

The routine next checks the alert tones at the the transmitter. If a 1 KHz test tone shows an unusual characteristic at TP4 while the maximum deviation EEPOT is adjusted, or the test tone is present when it should not be, the test fails.

The routine next checks the receiver audio paths. If a 1 KHz test tone shows an unusual characteristic in the receive path while the receive level EEPOT is adjusted, the test fails.

The routine next uses the alert-tone encoder to apply a 100 Hz tone to the PL-decoder input, and checks for proper waveform at that input. If an unexpected tone period is detected, the test fails.

The routine next tests the receiver and repeater squelch circuits. With loose squelch, the absence of receiver or repeater squelch activity is a failure. With tight squelch, the presence of receiver or repeater squelch activity is a failure. If these tests pass, while retaining the same tight squelch, the diagnostics cause a signal to be looped back to the squelch-detector circuits to simulate receiver quieting. Absence of squelch activity is now a failure.

The routine next checks Line and Receive Audio paths for continuity. A 1000 Hz test tone is used for this purpose, and if it is either there when it shouldn't be, or not there when it should, the test fails. The diagnostics then check the Repeat path in the same way, with the same test tone.

Finally, the diagnostics re-enable the 1000 Hz test tone, and check for it at TP1 (select audio). If it's not there, the test fails. Lastly, the routine disables the tone and checks for it again. This time, the test fails if it is there.

Audio diagnostics are now completed. At this point, the dashes (—) should be blanked from the Status window to indicate this to the operator.

The routine should now attempt to set all EEPOTs to the shadow values kept within EEPROM. If any one EEPOT takes too long to set, that is a fatal error, the relevant fatal error code code will be generated and displayed in the Status window, and the system will reset. This is the last point at which an SSCB error can occur. If that doesn't happen, Expansion Reset is now released, allowing the remote boards to begin their own diagnostics. The routine will indicate this by displaying the version number of the Station Control firmware in the Status window.

When each remote board completes its own internal diagnostics, it waits for an instruction from Station Control. This can be either a "shut up" or a "wake up" command. (The routines that control this on remote boards

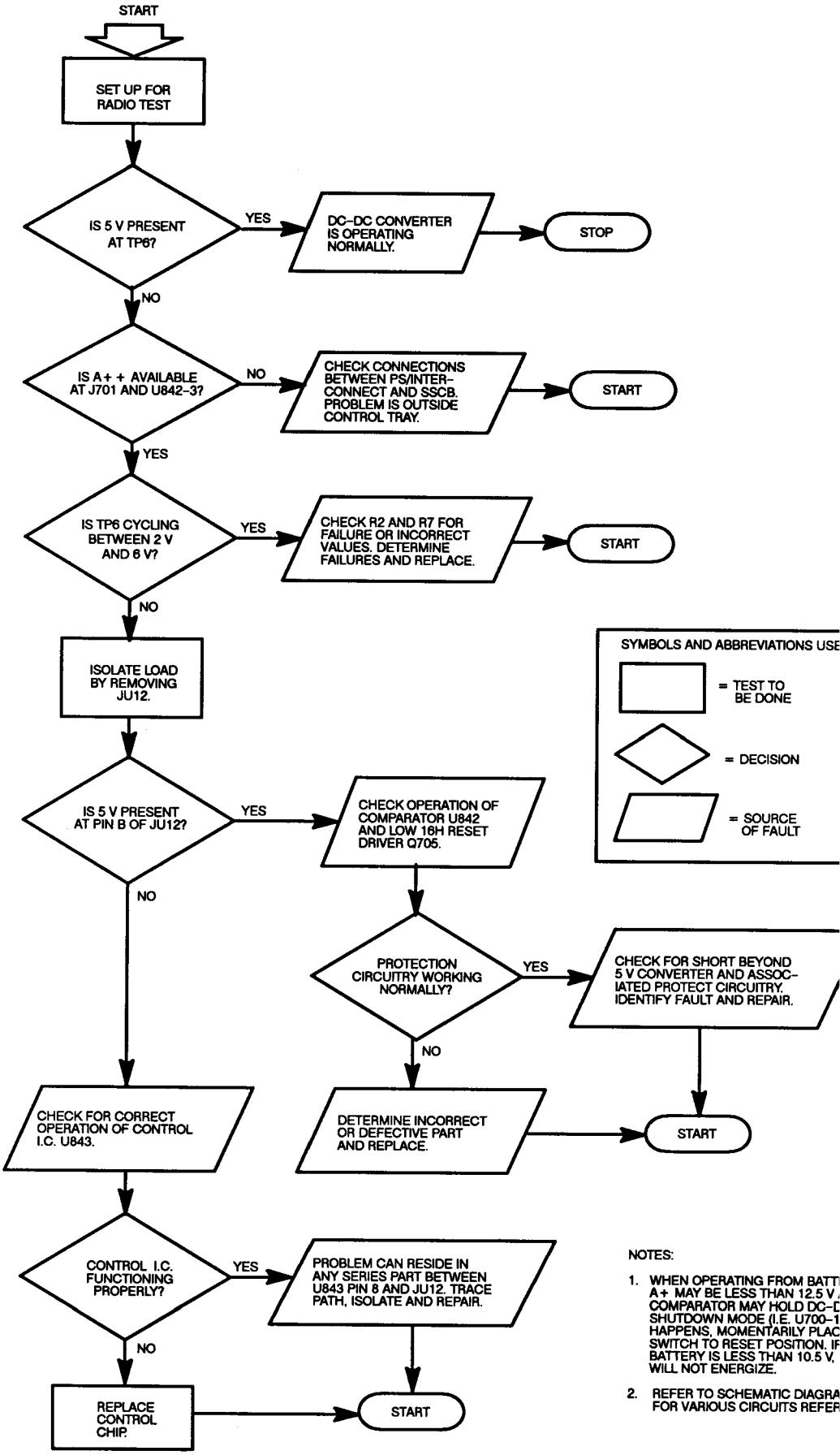
time-out in 10 seconds. If they receive no commands before time-out, they put their boards into background mode.) At this point in its execution, the diagnostics routine simply orders all remote boards to shut up. If any board refuses to comply, mutiny is assumed and a fatal error results.

While the diagnostic software is attempting to communicate with the remote boards, and also while each remote board is performing its own external diagnostics, the Status window will again display three dashes (—) to indicate this condition.

When all boards have agreed to shut up, Station Control asks the first one (TTRC, if present) to wake up and begin its own external diagnostics. The board has five seconds to send something over the IPCB. This can be its own IPCB test message, a fatal or non-fatal error code, or its firmware version number. Error codes received will be displayed in the Status window (fatal ones, of course, will remain in the window for five seconds before the Station Control board resets the entire station.) Reception of a remote board's firmware version number signals the completion of that board's diagnostics. Before displaying the version number, however, Station Control requests the Station Type and System Version bytes from the remote board. If any of those bytes don't match what Station Control has stored within its codeplug as the correct value, that is a fatal error. (This check ensures that only compatible boards can be used within a station). If all bytes match, the version number of the board goes up in the Status window, and the next remote board in line is called up to go through the same procedure. This procedure continues until there are no more remote boards in line. Any remote board that refuses to wake on command is, again, assumed to be in rebellion, and will cause a fatal error.

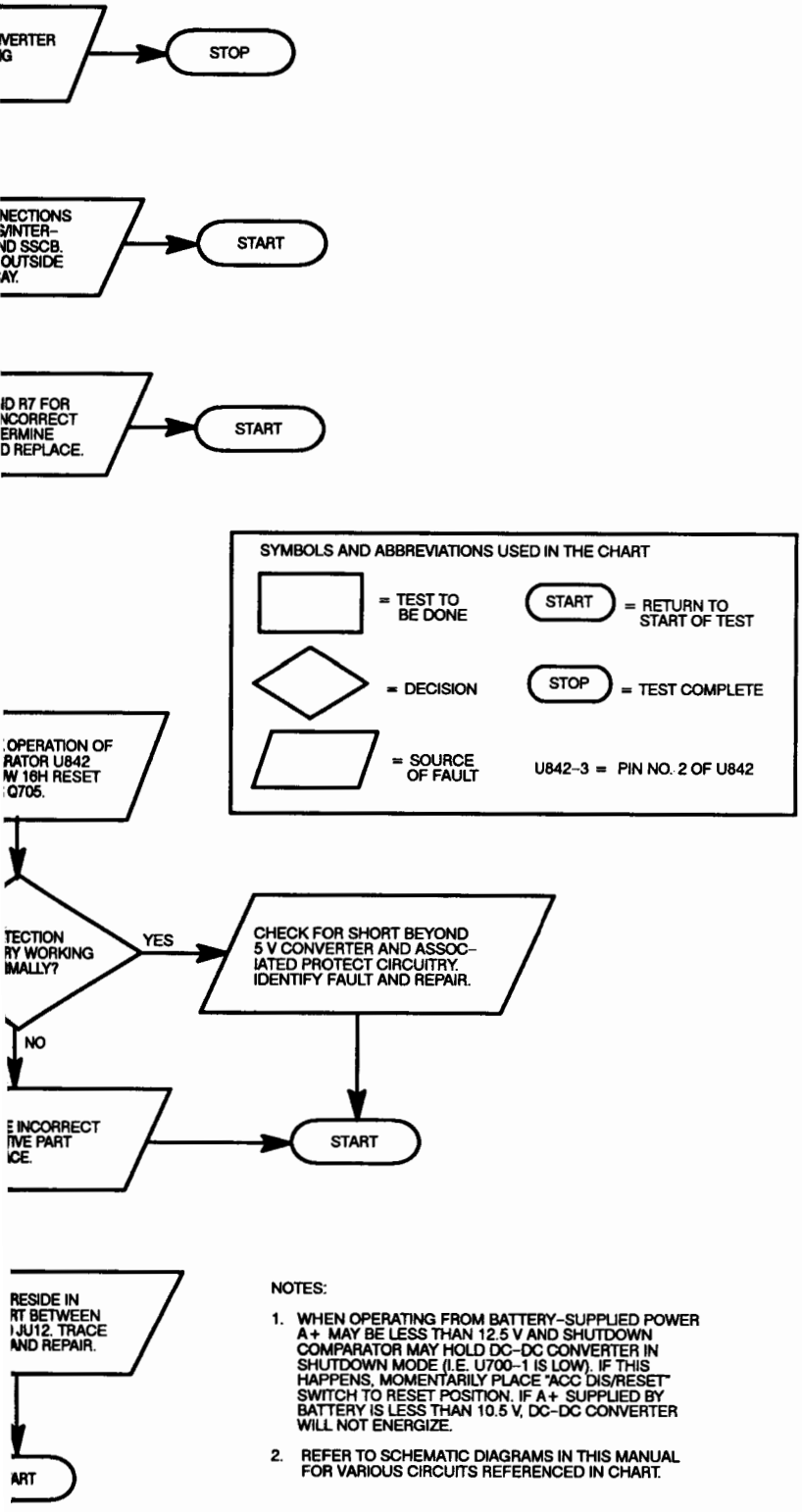
When the firmware version numbers of all remote boards in the station have been displayed in the Status window of the Station Control board, this means that all boards have run and passed their individual diagnostic routines. Having reached this point, sscb_reset_diags.asm will turn off the Disable LED, and issue a command to each board in turn to enter its background mode. This is the last chance for a remote board to mutiny by refusing the command, creating a fatal error and resetting the system. Assuming that no remote board chooses to do this, Station Control will now clear the Status window, call a variable-initialization routine, and go into its own background processing mode.

This page was originally blank.


START
SET UP FOR RADIO TEST
IS 5 V PRESENT AT TP6?
YES
DC–DC CONVERTER IS OPERATING NORMALLY.
STOP
NO
IS A+ + AVAILABLE AT J701 AND U842–3?
NO
CHECK CONNECTIONS BETWEEN PS/INTER-CONNECT AND SSCB. PROBLEM IS OUTSIDE CONTROL TRAY.
START
YES
IS TP6 CYCLING BETWEEN 2 V AND 6 V?
YES
CHECK R2 AND R7 FOR FAILURE OR INCORRECT VALUES. DETERMINE FAILURES AND REPLACE.
START
NO
ISOLATE LOAD BY REMOVING JU12.
SYMBOLS AND ABBREVIATIONS USE
= TEST TO BE DONE
= DECISION
= SOURCE OF FAULT
IS 5 V PRESENT AT PIN B OF JU12?
YES
CHECK OPERATION OF COMPARATOR U842 AND LOW 16H RESET DRIVER Q705.
NO
PROTECTION CIRCUITRY WORKING NORMALLY?
YES
CHECK FOR SHORT BEYOND 5 V CONVERTER AND ASSOC-IATED PROTECT CIRCUITRY. IDENTIFY FAULT AND REPAIR.
NO
CHECK FOR CORRECT OPERATION OF CONTROL I.C. U843.
DETERMINE INCORRECT OR DEFECTIVE PART AND REPLACE.
START
CONTROL I.C. FUNCTIONING PROPERLY?
YES
PROBLEM CAN RESIDE IN ANY SERIES PART BETWEEN U843 PIN 8 AND JU12. TRACE PATH, ISOLATE AND REPAIR.
NO
REPLACE CONTROL CHIP.
START
NOTES:
1. WHEN OPERATING FROM BATT
A+ MAY BE LESS THAN 12.5 V
COMPARATOR MAY HOLD DC–D
SHUTDOWN MODE (I.E. U700–1
HAPPENS, MOMENTARILY PLAC
SWITCH TO RESET POSITION. IF
BATTERY IS LESS THAN 10.5 V,
WILL NOT ENERGIZE.
2. REFER TO SCHEMATIC DIAGRA
FOR VARIOUS CIRCUITS REFER

SECURE CAPABLE STATION CONTROL BOARD

DC—DC CONVERTER TROUBLESHOOTING CHART

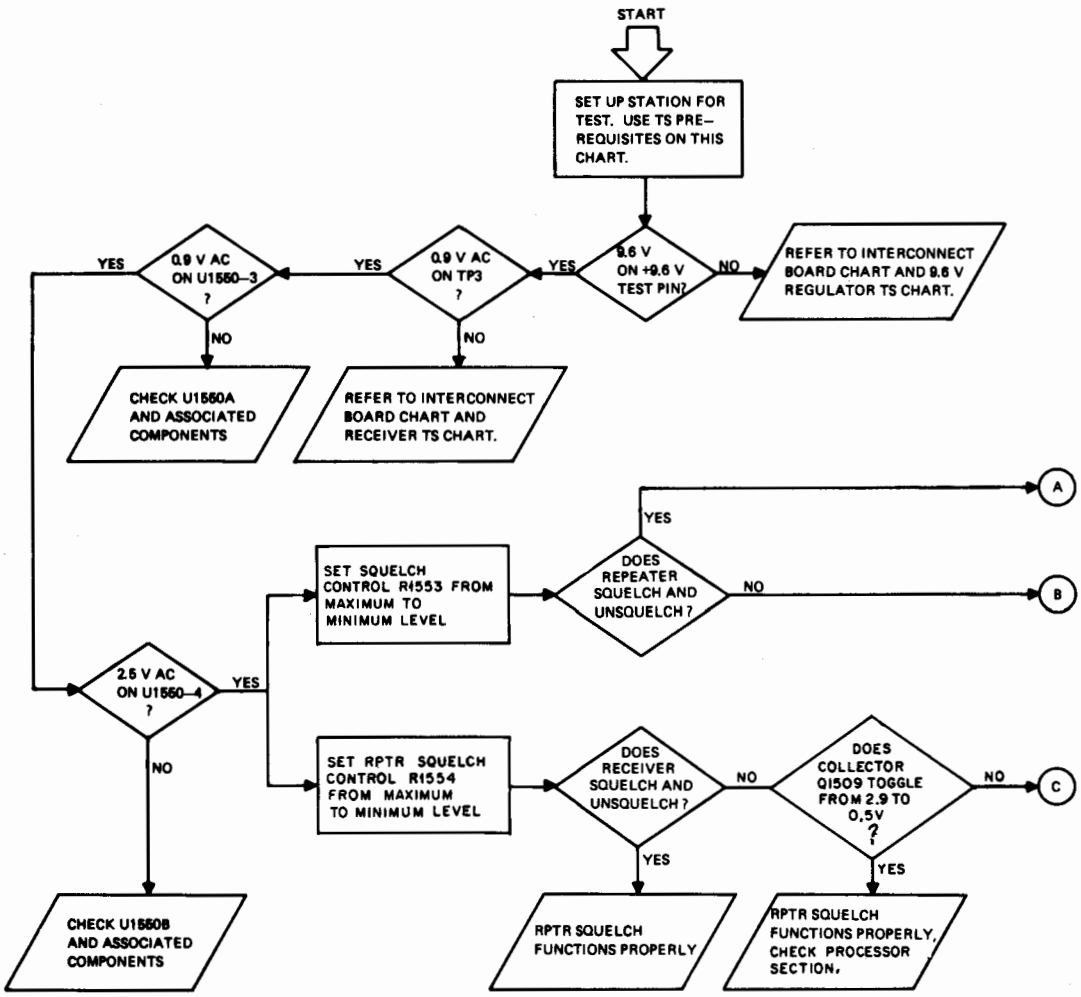


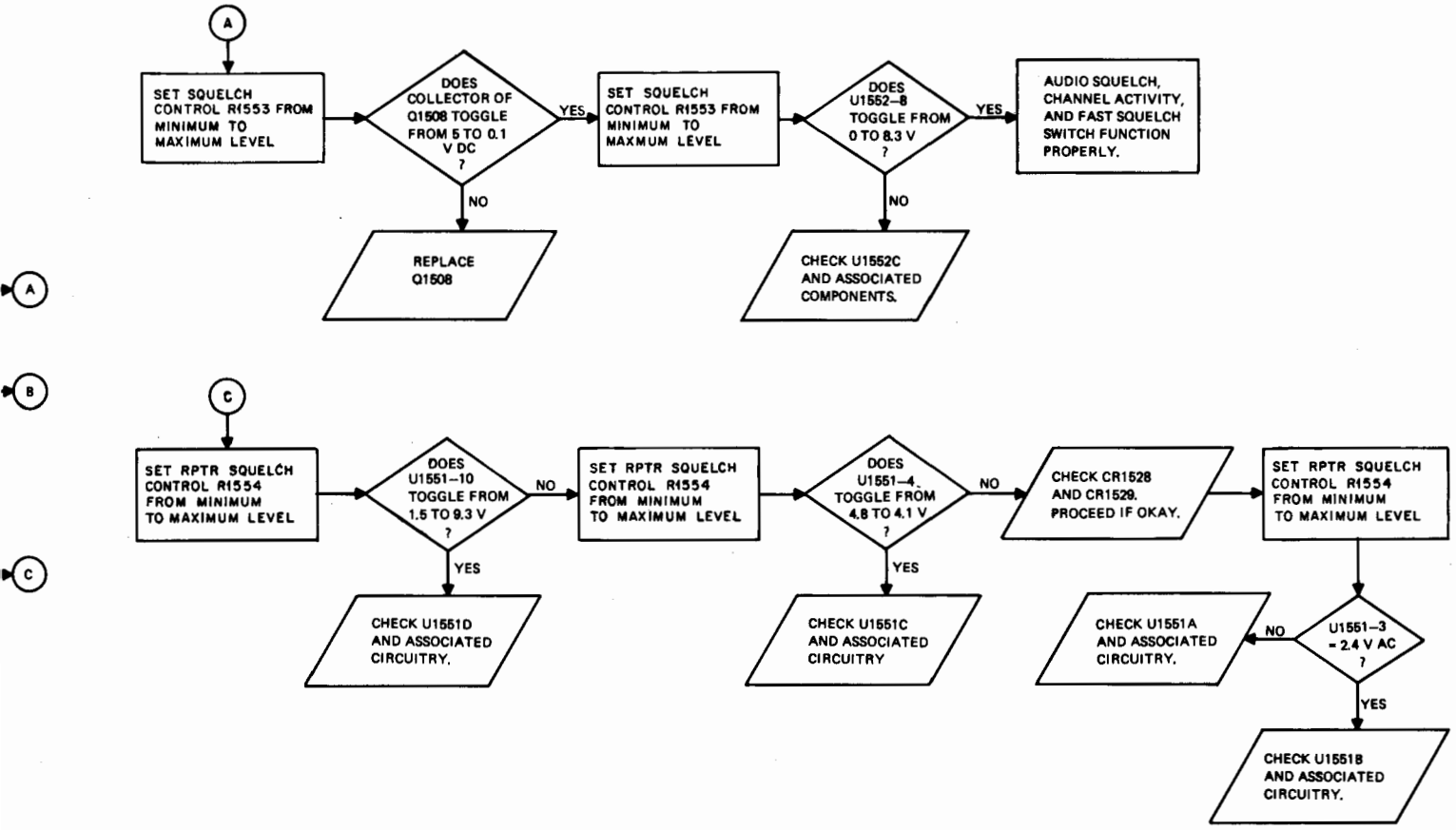
NOTES:

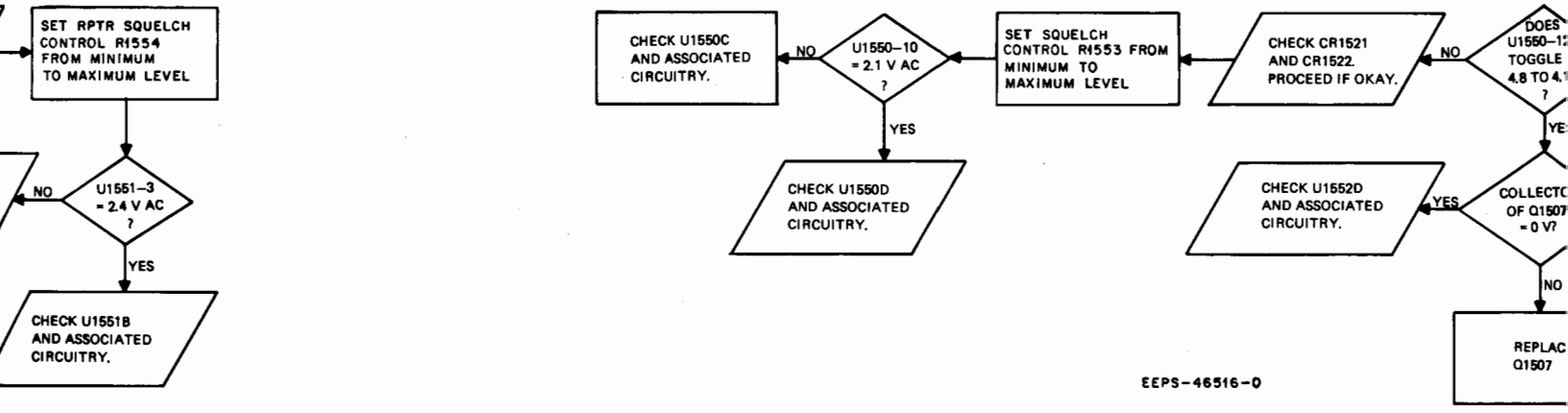
1. WHEN OPERATING FROM BATTERY-SUPPLIED POWER A+ MAY BE LESS THAN 12.5 V AND SHUTDOWN COMPARATOR MAY HOLD DC-DC CONVERTER IN SHUTDOWN MODE (I.E. U700-1 IS LOW). IF THIS HAPPENS, MOMENTARILY PLACE "ACC DIS/RESET" SWITCH TO RESET POSITION. IF A+ SUPPLIED BY BATTERY IS LESS THAN 10.5 V, DC-DC CONVERTER WILL NOT ENERGIZE.
2. REFER TO SCHEMATIC DIAGRAMS IN THIS MANUAL FOR VARIOUS CIRCUITS REFERENCED IN CHART.

SECURE CAPABLE STATION CONTROL BOARD

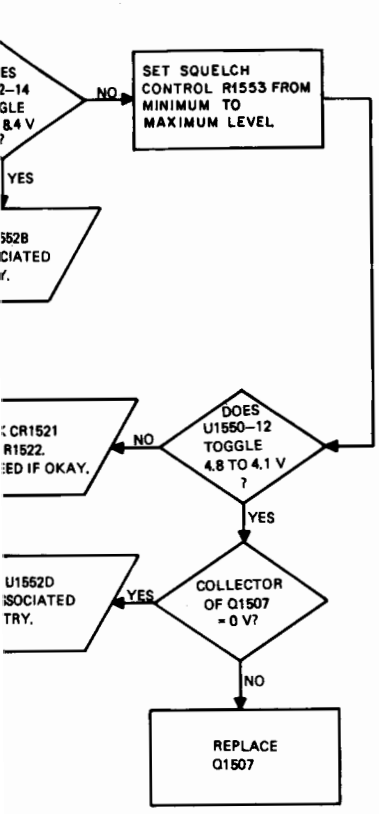
RECEIVER AUDIO AND SQUELCH CONTROL TROUBLESHOOTING CHART




A
SET SQUELCH CONTROL R1553 FROM MINIMUM TO MAXIMUM LEVEL
DOES COLLECTOR OF Q1508 TOGGLE FROM 5 TO 0.1 V DC ?
YES
NO
REPLACE Q1508
SET SQUELCH CONTROL R1553 FROM MINIMUM TO MAXMUM LEVEL
DOES U1552–8 TOGGLE FROM 0 TO 8.3 V ?
YES
NO
CHECK U1552C AND ASSOCIATED COMPONENTS.
AUDIO SQUELCH, CHANNEL ACTIVITY, AND FAST SQUELCH SWITCH FUNCTION PROPERLY.
A
B
C
SET RPTR SQUELCH CONTROL R1554 FROM MINIMUM TO MAXIMUM LEVEL
DOES U1551–10 TOGGLE FROM 1.5 TO 9.3 V ?
NO
YES
CHECK U1551D AND ASSOCIATED CIRCUITRY.
SET RPTR SQUELCH CONTROL R1554 FROM MINIMUM TO MAXIMUM LEVEL
DOES U1551–4 TOGGLE FROM 4.8 TO 4.1 V ?
NO
YES
CHECK U1551C AND ASSOCIATED CIRCUITRY
CHECK CR1528 AND CR1529. PROCEED IF OKAY.
SET RPTR SQUELCH CONTROL R1554 FROM MINIMUM TO MAXIMUM LEVEL
U1551–3 = 2.4 V AC ?
NO
YES
CHECK U1551A AND ASSOCIATED CIRCUITRY.
CHECK U1551B AND ASSOCIATED CIRCUITRY.


B
SET SQUELCH CONTROL R1553 FROM MINIMUM TO MAXIMUM LEVEL
DOES RX1 UNSQ TOGGLE 2.9 TO 0V ?
NO
YES
REFER TO AUDIO ROUTING & CONTROL SECTION TS CHART
SET SQUELCH CONTROL R1553 FROM MINIMUM TO MAXIMUM LEVEL
DOES U1552–14 TOGGLE 0 TO 8.4 V ?
NO
YES
CHECK U1552B AND ASSOCIATED CIRCUITRY.
SET RPTR SQUELCH CONTROL R1554 FROM MINIMUM TO MAXIMUM LEVEL
U1551–3 = 2.4 V AC ?
NO
YES
CHECK U1551B AND ASSOCIATED CIRCUITRY.
CHECK U1550C AND ASSOCIATED CIRCUITRY.
U1550–10 = 2.1 V AC ?
NO
YES
CHECK U1550D AND ASSOCIATED CIRCUITRY.
SET SQUELCH CONTROL R1553 FROM MINIMUM TO MAXIMUM LEVEL
CHECK CR1521 AND CR1522. PROCEED IF OKAY.
NO
CHECK U1552D AND ASSOCIATED CIRCUITRY.
YES
NO
YES

EEPS-46516-0



SYMBOLS AND ABBREVIATIONS USED IN THE CHART

ALL VOLTAGE MEASUREMENTS ARE DC, UNLESS OTHERWISE STATED.
AC VOLTAGES ARE MEASURED WITH AN AVERAGE RESPONDING METER.

= TEST TO BE DONE

= DECISION

= SOURCE OF FAULT

TS	= TROUBLESHOOTING
U1550–3	= PIN 3 OF U1550
CW	= CLOCKWISE
CCW	= COUNTERCLOCKWISE

TROUBLESHOOTING PREREQUISITES:

1. ENERGIZE STATION. RECEIVE SYNTHESIZER MUST BE LOCKED (RX LOCK LED LIT). IF NOT, PERFORM RECEIVER TROUBLESHOOTING PROCEDURE.
2. PL DISABLE STATION BY PUTTING SW800 IN THE PL DIS POSITION (UP).
3. ACCESS DISABLE STATION BY PUTTING SW801 IN THE "ACC DIS" POSITION. (UP)
4. PROVIDE A MEANS OF LISTENING TO LOCAL AUDIO. PLUG PORTABLE TEST SET INTO J812.
5. THERE SHOULD BE NO RF SIGNAL PRESENT AT THE RECEIVER INPUT (DISCONNECT ANTENNA).
6. WHEN TROUBLESHOOTING IS COMPLETE, READJUST THE AUDIO AND REPEATER SQUELCH SECTION TO PROPER SYSTEM SPECIFICATIONS.

parts list

TRN7008A Display Board — PL-11223-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		connector:
J805A, 805B	2883547T01	male: 8-contact
		light emitting diode: (see note)
DS8200 thru 8202	4882771L03	red, 7-segment display
		non-referenced items
	5483865R01	LABEL, bar code

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

TRN7352A/TRN7357A/TRN7358A SSCB BOARD — PL-11694-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ±5% 50V: unless otherwise stated
C701	2113740B57	220pF
C702	2113740B71	820pF
C703	2113740B73	.001
C704	2113741B69	0.1
C705,706	2311049A19	10 ± 10% 25V
C707	2113741B69	0.1
C708	2311049A19	10 ± 10% 25V
C709	2311049A08	1.0 ± 10% 35V
C710,711	2311049A22	33 ± 10% 16V
C712	2311049A19	10 ± 10% 25V
C713	2311049A08	1.0 ± 10% 35V
C714	2311049A19	10 ± 10% 25V
C715	2113740B49	100pF
C716	2311049A19	10 ± 10% 25V
C717	2113741B69	0.1
C718	2311019A45	100 ± 20% 16V
C719	2311049A19	10 ± 10% 25V
C721	2311049A22	33 ± 10% 16V
C722,723	2113741B69	0.1
C800	2113741B45	.01
C801	2113740B59	270pF
C802 thru 808	2113741B69	0.1
C810	2113741B69	0.1
C812	2311049A19	10 ± 10% 25V
C814,815	2113740B34	24pF
C817	2113740B65	470pF
C819	2113741B69	0.1
C820	2113741B45	.01
C822	2311049A08	1.0 ± 10% 35V
C823 thru 828	2113741B69	0.1
C829	2113740B49	100pF
C830	2113741B69	0.1
C1543	2113740B73	.001
C1544	0811051A13	0.1 63V
C1545,1546	2113740B47	82pF
C1547	0811017A08	.01
C1548	2113740B76	.0015
C1549	2113740B57	220pF
C1551	0811017A05	.0033
C1552,1553	2311049A10	2.2 ± 10% 35V
C1554	0811017A01	.001 (TRN7352A)
	0811017A08	.01 (TRN7357A/TRN7358A)
C1555	2113740B34	24pF
C1556	0811017A01	.001 (TRN7352A)
	0811017A08	.01 (TRN7357A/TRN7358A)
C1557	0811017A08	.01
C1558	2113740B76	.0015
C1559	2113740B73	.001
C1560	2113740B34	24pF
C1561	0811017A05	.0033
C1562	2311049A10	2.2 ± 10% 35V
C1564	2113741B21	.022 (TRN7352A)
	2113741B37	.0047 (TRN7357A/TRN7358A)
C1579	2113740B57	220pF
C8100,8101	2113740B49	100pF
C8102	0811017A08	.01
C8103	0811051A09	.022 63V
C8104	0811017A08	.01
C8105	2383210A19	500 -10+100% 20V
C8106	0811051A13	0.1 63V
C8107,8108	0811051A08	.015 63V
C8109	2384665F06	220 -10+150% 25V
C8111	0811017A05	.0033
C8112	2311049A15	4.7 ± 10% 35V
C8113	2113740B49	100pF
C8114,8115	2113740B57	220pF
C8116	0811051A15	0.22 63V
C8117	2311049A10	2.2 ± 10% 35V
C8118	2311049A08	1.0 ± 10% 35V
C8119	0811017A05	.0033
C8120	0811017A08	.01
C8121	2113740B57	220pF
C8122,8123	2311049A08	1.0 ± 10% 35V
C8124	0811051A13	0.1 63V
C8125	2311049A08	1.0 ± 10% 35V
C8126 thru 8130	2113740B49	100pF
C8131 thru 8133	2113740B40	43pF
C8134	2311049A08	1.0 +0.1
C8135	0811051A15	0.22 63V
C8136	2311049A19	10 ± 10% 25V
C8137 thru 8140	0811051A15	0.22 63V
C8141	2113741B45	.01
C8142 thru 8150	2113741B69	0.1
C8151	2311049A15	4.7 ± 10% 35V
C8152	2113740B49	100pF
C8153	2113741B45	.01
C8154	2113740B49	100pF
C8156	2113740B49	100pF
C8157	2113741B45	.01
C8158	0811051A10	.033 63V
C8159	0811051A12	.068 63V
C8160	2113740B49	100pF
C8161	0811017A05	.0033
C8162	0811051A13	0.1 63V
C8163	2113740B74	.0012
C8164	2311049A08	1.0 ± 10% 35V
C8165	2113740B76	.0015
C8169	2113740B40	43pF
C8170	0811051A15	0.22 63V

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
C8173	0811017A08	.01
C8174	2113740B57	220pF
C8175,8176	2311049A08	1.0 ± 10% 35V
C8177	2311049A10	2.2 ± 10% 35V
C8178	2311049A08	1.0 ± 10% 35V
C8179 thru 8191	2113741B69	0.1
C8193	2113741B69	0.1
C8195 thru 8198	2113741B69	0.1
C8200	2113741B33	.0033
C8201	2113740B55	180pF
C8202	2113741B45	.01
C8203	2113741B37	.0047
C8204	2113740B73	.001
C8205	0811051A15	0.22 63V
C8207	2113740B73	.001
C8209,8210	0811051A13	0.1 63V
C8214 thru 8216	2113740B73	.001
C8218	0811051A15	0.22 63V
C8219	2113741B69	0.1
C8220	2113740B73	.001
C8225	2113740B73	.001
C8230	2113740B57	220pF
C8231	2113740B73	.001
C8300 thru 8303	0811051A11	.047 63V
C8304	2311049A19	10 ± 10% 25V
C8305,8306	0811051A11	.047 63V
C8307	2113740B36	30pF
		diode: (see note)
CR801,802	4811058A11	silicon
CR803	4805129M41	silicon
CR804 thru 807	4811058A11	silicon
CR809	4811058A11	silicon
CR1520 thru 1522	4805129M41	silicon
CR1523,1524	4811058A11	silicon
CR1526,1527	4811058A11	silicon
CR1528,1529	4805129M41	silicon
CR1530	4811058A11	silicon
CR1531	4805129M41	silicon
CR8100,8101	4883654H01	silicon
CR8102,8103	4811058A11	silicon
CR8107	4811058A11	silicon
CR8110	4805129M41	silicon
CR8112,8113	4805129M41	silicon
CR8115,8116	4883654H01	silicon
CR8200 thru 8203	4805129M41	silicon
		light emitting diode: (see note)
DS800 thru 803	4888245C22	green
DS804	4888245C23	yellow
DS805	4888245C24	red
		connector:
J701	2882984N13	male: 6-contact
J800	2882296R34	male: 40-contact
J801	2882505T03	male: 26-contact
J802	2883143M03	male: 14-contact
J803	2882505T05	male: 40-contact
J804	2882505T04	male: 34-contact
J806,807	0984231B03	female: 2-contact
J812	0983112N01	female: 6-contact
		jumper:
JU1 thru 17	2880002R03	male: 3-contact
		coil:
L700	2484386T01	25uH
L701	2484266T01	150Uh
L702	2484386T01	25uH
L800	2411047A25	10uH
		transistor: (see note)
Q700	4884233T01	MOSFET type M33T01
Q705	4811056A08	PNP type M56A08
Q800	4811056A08	PNP type M56A08
Q801	4811056A03	NPN type M56A03
Q802	4800869642	NPN type M9642
Q803,804	4811056A03	NPN type M56A03
Q805	4800869642	NPN type M9642
Q806,807	4811056A03	NPN type M56A03
Q808	4811056A23	NPN type M56A23
Q809 thru 811	4811056C21	NPN type M56C21
Q813,814	4811056A03	NPN type M56A03
Q816,817	4811046A03	NPN type M56A03
Q821	4800869653	JFET N-channel
Q822,823	4811056A03	NPN type M56A03
Q1507 thru 1510	4811056A03	NPN type M56A03
Q8100	4811056A03	NPN type M56A03
Q8101,8102	4800869919	JFET P-channel
Q8200 thru 8207	4811056A08	PNP type M56A08
Q8208 thru 8212	4811056A23	NPN type M56A23

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		resistor, fixed: ±5% 1/8W unless otherwise stated
R700	0611077A98	10k
R701	0611077A88	3.9k
R702	0611077A50	100
R703	0611077A74	1k
R704	0611077B31	220k
R705	0611077F99	12.1k ± 1%
R706	0611077F28	2.21k ± 1%
R707	0611077H30	267k ± 1%
R708	0611077F91	10k ± 1%
R709	0611077E94	1k ± 1%
R710	0611077F99	12.1k ± 1%
R711	0611077B35	330k
R712	0611077B23	100k
R713	0611077F91	10k ± 1%
R714	0611077B13	39k
R715	0611077B15	47k
R716	0611077F63	5.11k ± 1%
R717	0611077B35	330k
R718	0611077B07	22k
R719	0611077A50	100
R720	0611077A36	27
R721	0611077B47	1 meg
R722	0611077B31	220k
R723,724	0683962T01	1.0 1W
R725	0611077F91	10k ± 1%
R726	0611077G09	15k ± 1%
R727	0611077A98	10k
R728	0611077H85	1 meg ± 1%
R729	0611077B29	180k
R730	0611077A01	0-ohm jumper
R731	0683962T01	1.0 ± 1%
R732,733	0611086D04	0.62 2W
R736	0611009A33	220 1/4W
R737	0611077A84	2.7k
R738	0611077A64	390
R739	0611077A98	10k
R740	0611077A56	180
R741	0611077A98	10k
R742	0611077A86	3.3k
R743	0611086A03	1.0 1W
R748	0611077A78	1.5k
R800	0611077A54	150
R801	0611077A88	3.9k
R802	0611077A01	0-ohm jumper
R803,804	0611077A88	3.9k
R805	0611077A42	47
R806	0611077A98	10k
R807	0611077A94	6.8k
R809,810	0611077A94	6.8k
R812	0611077A78	1.5k
R813	0611077A32	18
R814	0611077A56	180
R815	0611077A32	18
R816	0611077A90	4.7k
R817	0611077A82	2.2k
R818	0611077A52	120
R819	0611077A32	18
R820	0611077A56	180
R821	0611077A78	1.5k
R822	0611077A56	180
R823	0611077A82	2.2k
R824	0611077A80	1.8k
R825	0611077A82	2.2k
R826	0611077A98	10k
R827	0611077A88	3.9k
R828	0611077B07	22k
R829	0611077A94	6.8k
R830 thru 836	0611077A98	10k
R837,838	0611077A50	100
R839	0611077A98	10k
R840,841	0611077A50	100
R842	0611077A98	10k
R843 thru 845	0611077A50	100
R846	0611077A52	120
R847,848	0611077A98	10k
R849	0611077B09	27k
R850	0611077A98	10k
R851	0611077A58	220
R852	0611077B47	1 meg
R854	0611077A98	10k
R855	0611077A92	5.6k
R856 thru 858	0611077A98	10k
R861	0611077B09	27k
R862	0611077A88	3.9k
R863	0611077A54	150
R866	0611077A98	10k
R867	0611077A78	1.5k
R868 thru 871	0611077A98	10k
R872	0611077A54	150
R873	0611077A98	10k
R874	0611077A54	150
R875	0611077A80	1.8k
R876	0611077A98	10k
R877	0611077A54	150
R878	0611077A90	4.7k
R879	0611077A82	2.2k
R880	0611077A78	1.5k

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R881	0611077A98	10k
R882	0611077A82	2.2k
R883,884	0611077A98	10k
R885	0611077A90	4.7k
R887	0611077A98	10k
R888	0611077B39	470k
R889	0611077A98	10k
R890	0611077A74	1k
R891	0611077A98	10k
R893	0611077A98	10k
R894	0611077B23	100k
R895 thru 898	0611077A98	10k
R1523	0611077B15	47k
R1524	0611077A86	3.3k
R1525	0611077B13	100k (TRN7352A)
	0611077B23	39k (TRN7357A)
	0611077B17	56k (TRN7358A)
R1526	0611077A82	2.2k
R1527	0611077B35	330k (TRN7352A)
	0611077B13	39k (TRN7357A)
	0611077B17	56k (TRN7358A)
R1532	0611077B07	22k (TRN7352A)
	0611077B27	150k (TRN7357A/TRN7358A)
R1533	0611077A64	390
R1534	0611077A78	1.5k
R1535	0611077B25	120k (TRN7352A)
	0611077B23	100k (TRN7357A/TRN7358A)
R1536	0611077B37	220k (TRN7352A/TRN7357A)
	0611077B39	470k (TRN7358A)
R1537	0611077B15	47k
R1540	0611077B15	47k
R1543	0611077B23	100k
R1544	0611077A74	1k
R1545	0611077B19	68k
R1546	0611077A74	1k
R1547	0611077A98	10k
R1548	0611077B33	270k
R1549	0611077A94	6.8k
R1550	0611077A98	10k
R1553	0611077B19	68k
R1554	0611077B21	82k
R1555,1556	0611077A98	10k
R1557	0611077B07	22k (TRN7352A)
	0611077B27	150k (TRN7357A/TRN7358A)
R1559	0611077A64	390
R1560	0611077B15	47k
R1561	0611077B25	120k (TRN7352A)
	0611077B23	100k (TRN7357A/TRN7358A)
R1562	0611077B37	220k (TRN7352A/TRN7357A)
	0611077B39	470k (TRN7358A)
R1563	0611077B15	47k
R1565,1566	0611077A74	1k
R1567	0611077A94	6.8k
R1568	0611077A98	10k
R1570	0611077A74	1k
R1571	0611077A98	10k (TRN7352A/TRN7357A)
	0611077B21	82k (TRN7358A)
R1572	0611077A01	0-ohm jumper (TRN7357A/TRN7358A)
	—	not used (TRN7352A)
R1573,1574	0611077A91	5.1k (TRN7352A/TRN7357A)
	0611077B14	43k (TRN7358A)
R1575	0611077A92	5.6k
R1576	0611077B27	150k
R1578	0611077A78	1.5k
R1599	1882787K08	var 100k ±20% 1/4W
R8100 thru 8103	0611077B01	12k
R8105	0611077B23	100k
R8106 thru 8107	0611077A98	10k
R8108	0611077A94	6.8k
R8109	0611077B01	12k
R8110	0611077B13	39k
R8111	0611077A98	10k
R8112	0611077A94	6.8k
R8113,8114	0611077A86	3.3k
R8115	0611077A94	6.8k
R8116	0611077A88	3.9k
R8117	0611009B26	2.7 1/4W
R8118	0611077A88	3.9k
R8119	0611077A67	510
R8120	0611077A68	560
R8121	0611086A08	4.7 1W
R8122	0611077A26	10
R8123	0611077B37	390k
R8124	0611077A94	6.8k
R8125	0611077A98	10k
R8127	0611077A94	6.8k
R8128	0611077A86	3.3k
R8129	0611077A78	1.5k
R8130	0611077H43	365k ±1%
R8131	0611077A98	10k
R8132	0611077A92	5.6k
R8133	0611077B23	100k
R8134	0611077B17	56k
R8135	1882787K09	var 10 1/4W
R8136	0611077B05	18k
R8137	0611077B09	27k
R8138,8139	0611077B11	33k
R8141	0611077B03	15k
R8142,8143	0611077B07	22k
R8144	0611077A98	10k
R8146	0611077B03	15k

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R8147	0611077B09	27k
R8148	0611077A98	10k
R8149	0611077B09	27k
R8150	0611077B23	100k
R8152,8153	0611077B09	27k
R8153,8154	061177A98	10k
R8155	0611077B09	27k
R8156	0611077B23	100k
R8157 thru 8159	'0611077B09	27k
R8162	0611077B07	22k
R8163	0611077B09	27k
R8164	0611077A98	10k
R8165,8166	0611077B09	27k
R8167	0611077B23	100k
R8168	0611077B30	200k
R8169	0611077B23	100k
R8170	0611077A68	560
R8171	0611077B30	200k
R8172	0611077A50	100
R8173,8174	0611077B23	100k
R8175	0611077B09	27k
R8176	0611077A91	5.1k
R8177	0611077B09	27k
R8178,8179	0611077B14	43k
R8180	0611077B09	27k
R8181 thru 8185	0611077B18	62k
R8186	0611077B15	47k
R8187	0611077B14	43k
R8188	0611077B23	100k
R8189	0611077B43	680k
R8190	0611077B23	100k
R8191	0611077A98	10k
R8192	0611077A86	3.3k
R8193	0611077A98	10k
R8194	0611077B23	100k
R8195	0611077A88	3.9k
R8196,8197	0611077A76	1.2k
R8200	0611077A78	1.5k
R8201	0611077A50	100
R8202	0611077A78	1.5k
R8203	0611077A90	4.7k
R8204	0611077A50	100
R8205,8206	0611077A78	1.5k
R8207	0611077A82	2.2k
R8208	0611077A50	100
R8209,8210	0611077A78	1.5k
R8211	0611077A84	2.7k
R8212	0611077A50	100
R8213,8214	0611077A78	1.5k
R8215	0611077B11	33k
R8216	0611077A50	100
R8217,8218	0611077A78	1.5k
R8219	0611009B23	0-ohm jumper
R8220	0611077A50	100
R8221,8222	0611077A78	1.5k
R8223	0611077B23	100k
R8224	0611077A78	1.5k
R8225	0611077A50	100
R8226	0611077A78	1.5k
R8227	0611077B23	100k
R8228	0611077A50	100
R8229,8230	0611077A78	1.5k
R8231	0611077G88	100k ±1%
R8232,8233	0611077A98	10k
R8236,8237	0611077A98	10k
R8239,8240	0611077A98	10k
R8242,8243	0611077H18	200k ±1%
R8244	0611077G88	100k ±1%
R8245	0611077B23	100k
R8246	0611077G88	100k ±1%
R8247	0611077H18	200k ±1%
R8248	0611077G88	100k ±1%
R8249	0611077H18	200k ±1%
R8250	0611077G88	100k ±1%
R8251 thru 8254	0611077H18	200k ±1
R8255,8256	0611077B23	100k
R8257	0611077G88	100k ±1%
R8258	0611077H18	200k ±1%
R8259	0611077G88	100k ±1%
R8260	0611077H18	200k ±1%
R8261	0611077G88	100k ±1%
R8262,8263	0611077H18	200k ±1%
R8272	0611077G88	100k ±1%
R8275	0611077H85	1 meg ±1%
R8276	0611077H30	267k ±1%
R8277	0611077A98	10k
R8278	0611077H50	432k ±1%
R8279	0611077H26	243k ±1%
R8280	0611077H43	365k ±1%
R8281	0611077B13	39k
R8282,8283	0611077H85	1 meg ±1%
R8284	0611077H30	267k ±1%
R8285	0611077H50	432k ±1%
R8286	0611077A98	10k
R8287	0611077A74	1k
R8288	0611077H26	243k ±1%
R8289	0611077H85	1 meg ±1%
R8290	0611077H43	365k ±1%
R8291	0611077B13	39k
R8292	0611077A86	3.3k
R8293	0611077B23	100k

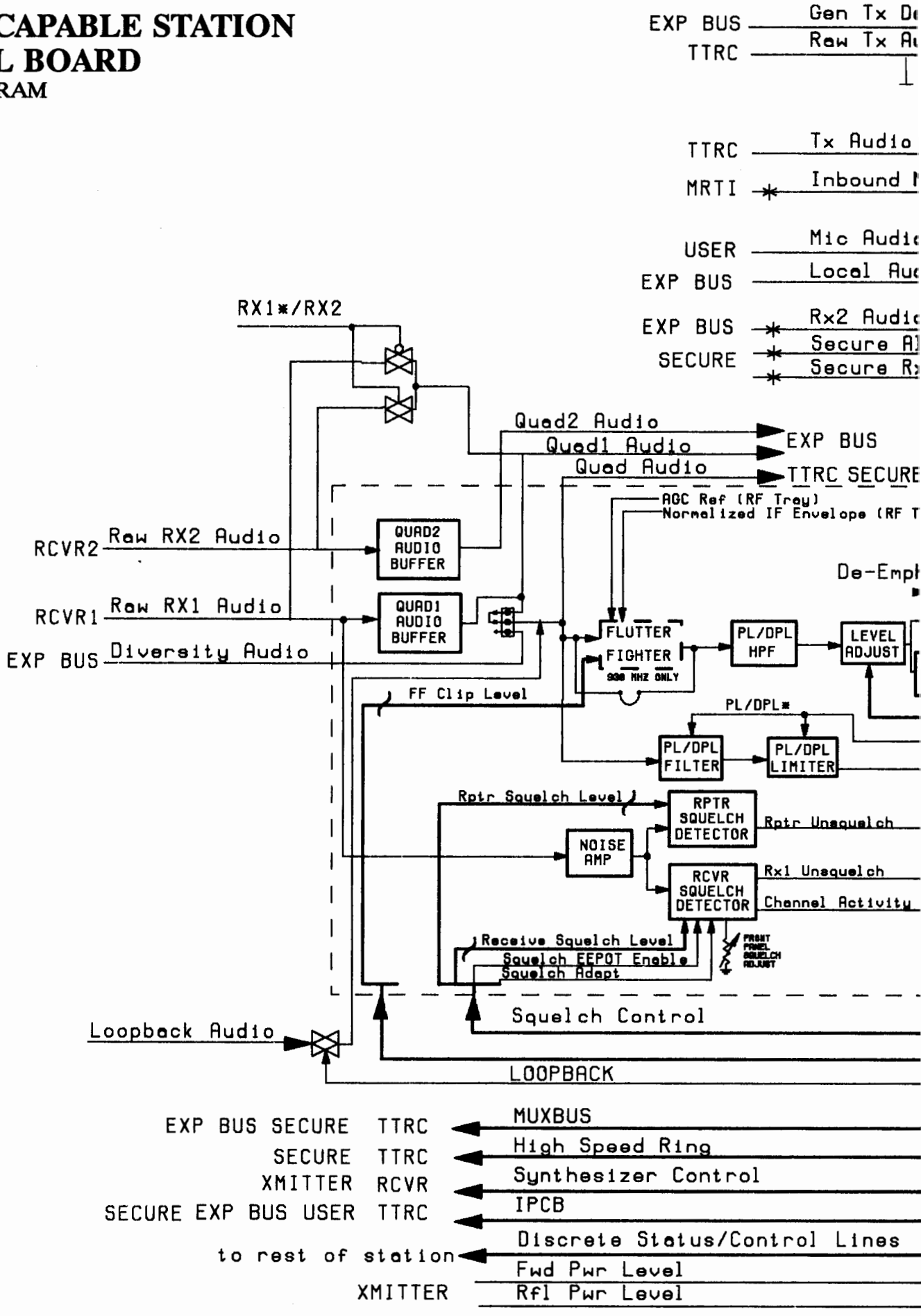
SECURE CAPABLE STATION CONTROL BOARD
PARTS LISTS

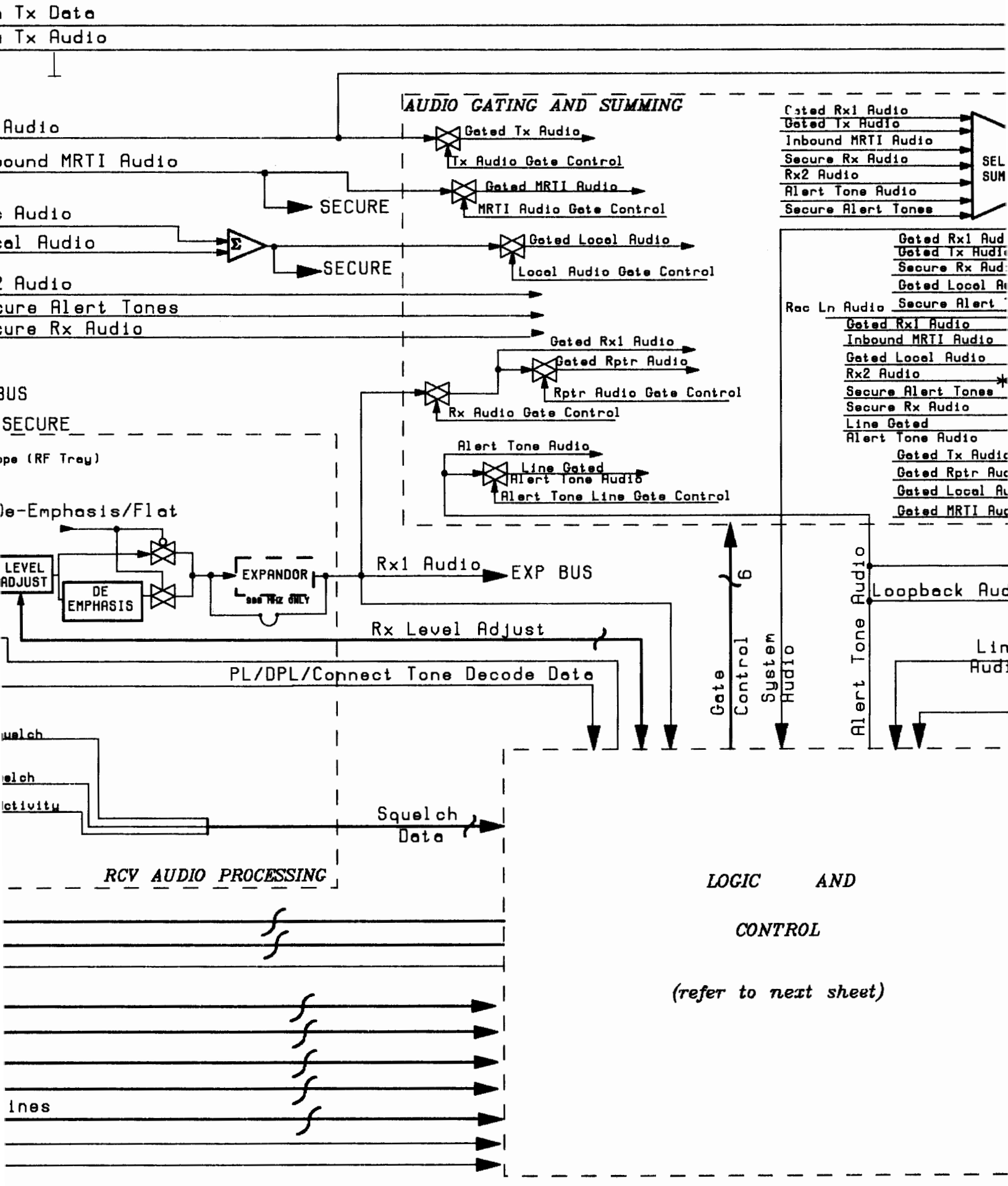
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R8294	0611077B11	33k
R8295	0611077B23	100k
R8300	0611077B23	100k
R8310 thru 8313	0611077B15	47k
R8314	0611077A98	10k
R8315	0611077A94	6.8k
R8316	0611077A98	10k
R8318	0611077B23	100k
R8335 thru 8339	0611077A74	1k
R8340	0611077A98	10k
R8344	0611077A68	560
R8345 thru 8347	0611077A50	100
R8348	0611077A98	10k
R8349	0611077B30	200k
R8400	0611077A67	510
R8401,8402	0611077A92	5.6k
R8403	0611077B01	12k
R8404	0611077B11	33k
R8405	0611077A84	2.7k
R8406	0611077B15	47k
R8407	0611077A74	1k
R8408	0611077B35	330k
R8409	0611077B45	820k
R8410	0611077E15	150 ± 1%
R8411	0611077B45	820k
R8412	0611077E73	604 ± 1%
R8413	0611009B23	0-ohm jumper
R8414	0611077A43	51
R8415	0611077B03	15k
		switch:
SW800,801	4083980R04	spdt toggle
SW802	4083980R05	spdt toggle
		transformer:
T700	2584265T01	power
		test point:
TP1 thru 11	2910271A15	terminal pin
		]integrated circuit: (see note)
U800	5197024A01	2.1 MHz max interclock 8-bit MCU
U801,802	5184494R03	ASIC
U804	5184064F76	32k x 8 RAM
U806	5183222M10	quad operational amplifier
U807	5184320A35	timer
U810 thru 812	5184887K60	2-chan analog multiplexer/demultiplexer
U813	5184704M19	hex-level log-level converter shifter
U814	5184621K32	quad operational amplifier
U816	5184704M19	hex-level log-level converter shifter
U817	5184887K73	quad bilateral switch
U818,819	5184621K32	quad operational amplifier
U821	5184621K32	quad operational amplifier
U824	5182802R24	50k ± 10% 15mW digitally controlled pot
U830	5184621K33	quad operational amplifier
U831	5182802R24	50k ± 10% 15mW digitally controlled pot
U837,838	5184621K85	dual operational amplifier
U839	5184704M19	hex-level log-level converter shifter
U840	5184887K60	2-chan analog multiplexer/demultiplexer
U841	5184621K85	dual operational amplifier
U842	5183222M64	quad comparator
U843	5184371T01	signaling current control module
U1550,1551	5183222M03	quad operational amplifier
U1552	5183222M10	quad operational amplifier
U1553,1554	5182802R24	50k ± 10% 16mW digitally controlled pot
U8200	5184621K32	quad operational amplifier
		voltage regulator: (see note)
VR701	4883461E40	Zener: 5.1V
VR702	4882256C26	Zener: 3.3V
VR1531	4882256C26	Zener: 3.3V
VR1532	4882256C26	Zener: 3.3V (TRN7357A/TRN7358A)
	4811034A23	Zener: 2.7V (TRN7352A)
VR1533	4882256C26	Zener: 3.3V (TRN7357A/TRN7358A
	4811034a23	Zener, 2.7 V (TRN7352A)
VR1531	4882256C26	Zener: 3.3V
		crystal: (see note)
Y800	4880113K04	7.9488 MHz
	non-referenced items	
	0310945A11	SCREW, tapping: P3.12 x 1.27 x 8; 2 used for J800
	0982449T01	SOCKET, 52-contact: for U800
	0982449T03	SOCKET, 84-contact: for U801,802
	0982808R02	SOCKET, 8-contact: for U808
	0982808R10	SOCKET: 28-contact: for U803
	0983729M17	RECEPTACLE: 20-contact: 2 used for J800
	0984181L01	CONNECTOR, 2-contact jumper: for JU1-JU17
	2683373P02	HEAT SINK: for Q700
	4380054K02	SPACER, PCB support
	5483865R01	LABEL, white bar code
	5484246T01	LABEL, bar code
	7505295B01	PAD, crystal base: for Y800
	TRN7008A	BOARD, display

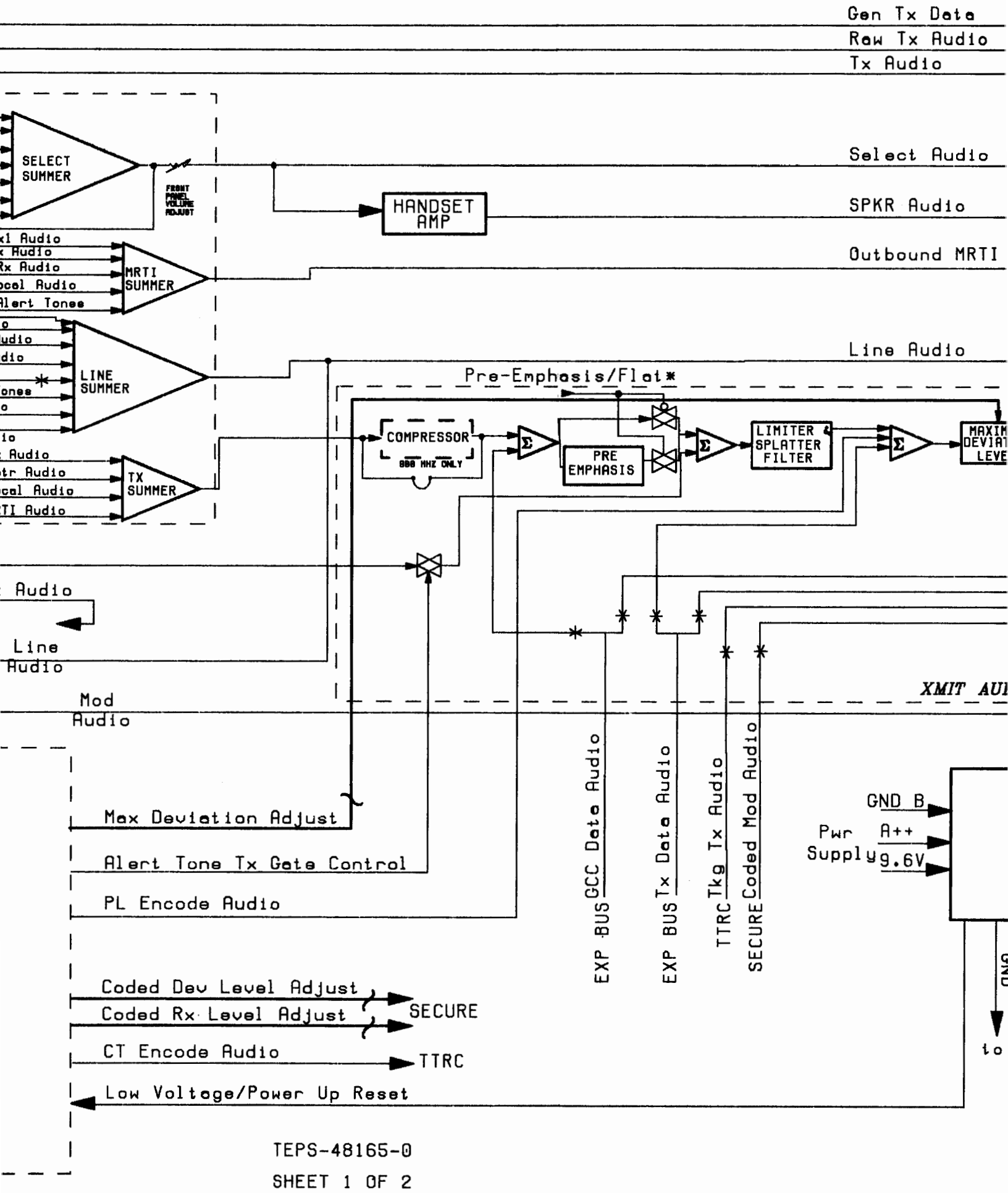
note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

SECURE CAPABLE STATION CONTROL BOARD

BLOCK DIAGRAM

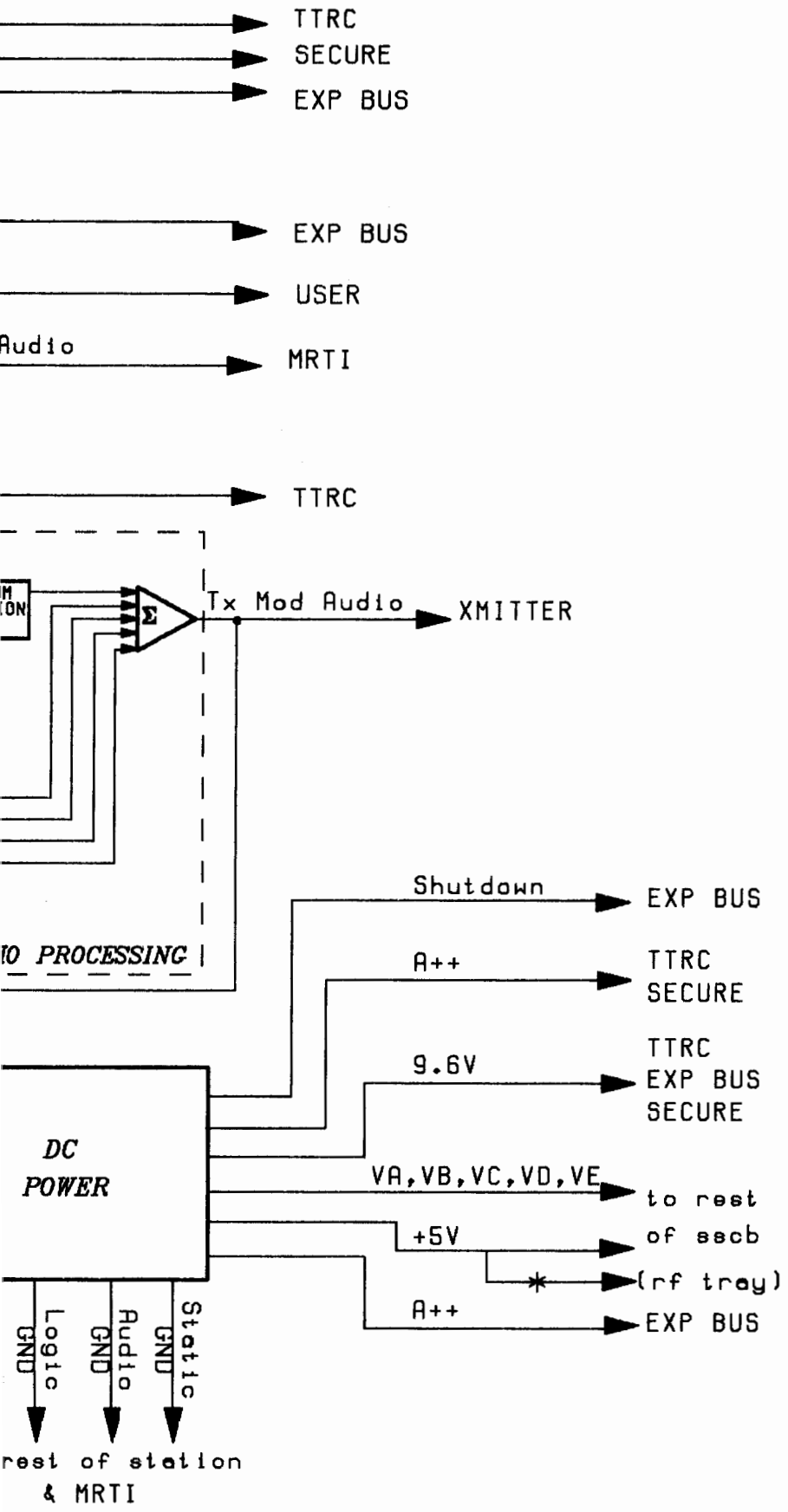



Tx Data
Tx Audio
AUDIO GATING AND SUMMING
Audio
Gated Tx Audio
Tx Audio Gate Control
ound MRTI Audio
SECURE
Gated MRTI Audio
MRTI Audio Gate Control
Audio
al Audio
SECURE
Gated Local Audio
Local Audio Gate Control
Audio
ure Alert Tones
ure Rx Audio
Gated Rx1 Audio
Gated Rptr Audio
Rptr Audio Gate Control
Rx Audio Gate Control
BUS
SECURE
pe (RF Tray)
Alert Tone Audio
Line Gated
Alert Tone Audio
Alert Tone Line Gate Control
e-Emphasis/Flat
LEVEL ADJUST
DE EMPHASIS
EXPANDOR
Rx1 Audio
EXP BUS
Rx Level Adjust
PL/DPL/Connect Tone Decode Data
Gate Control
System Audio
Alert Tone Audio
Loopback Aud
Squelch Data
RCV AUDIO PROCESSING
LOGIC AND
CONTROL
(refer to next sheet)
lines

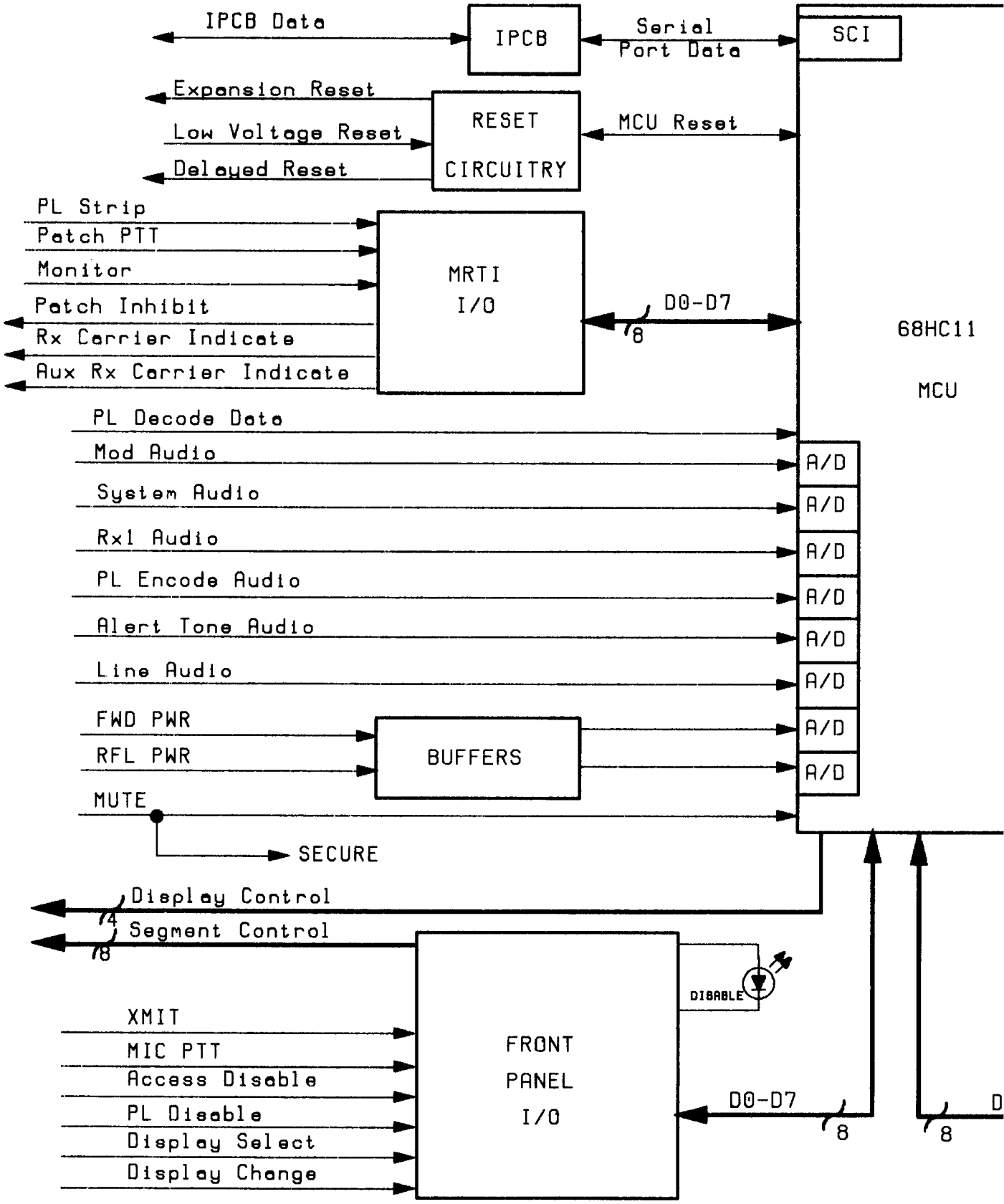


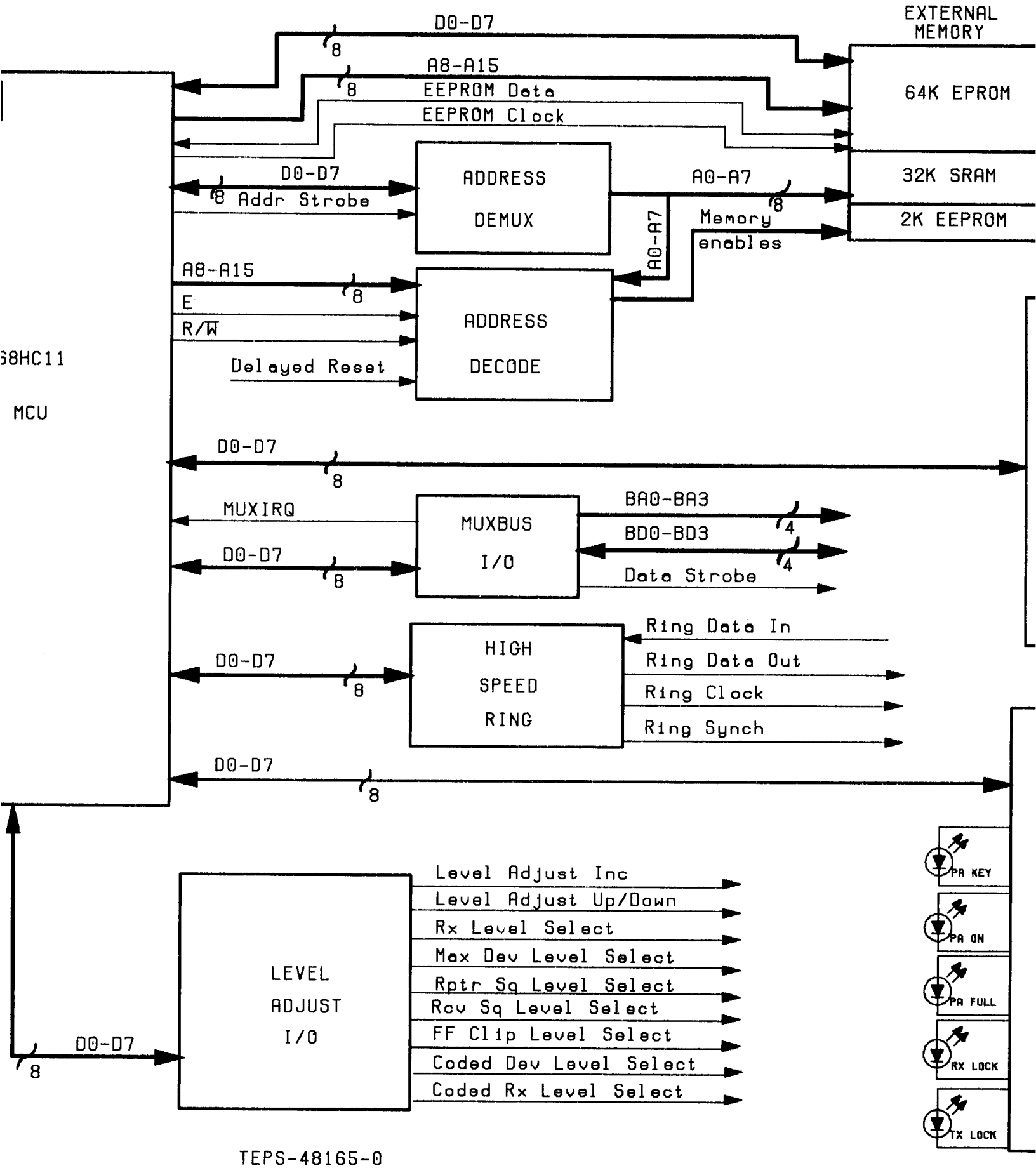
TEPS-48165-0

SHEET 1 OF 2



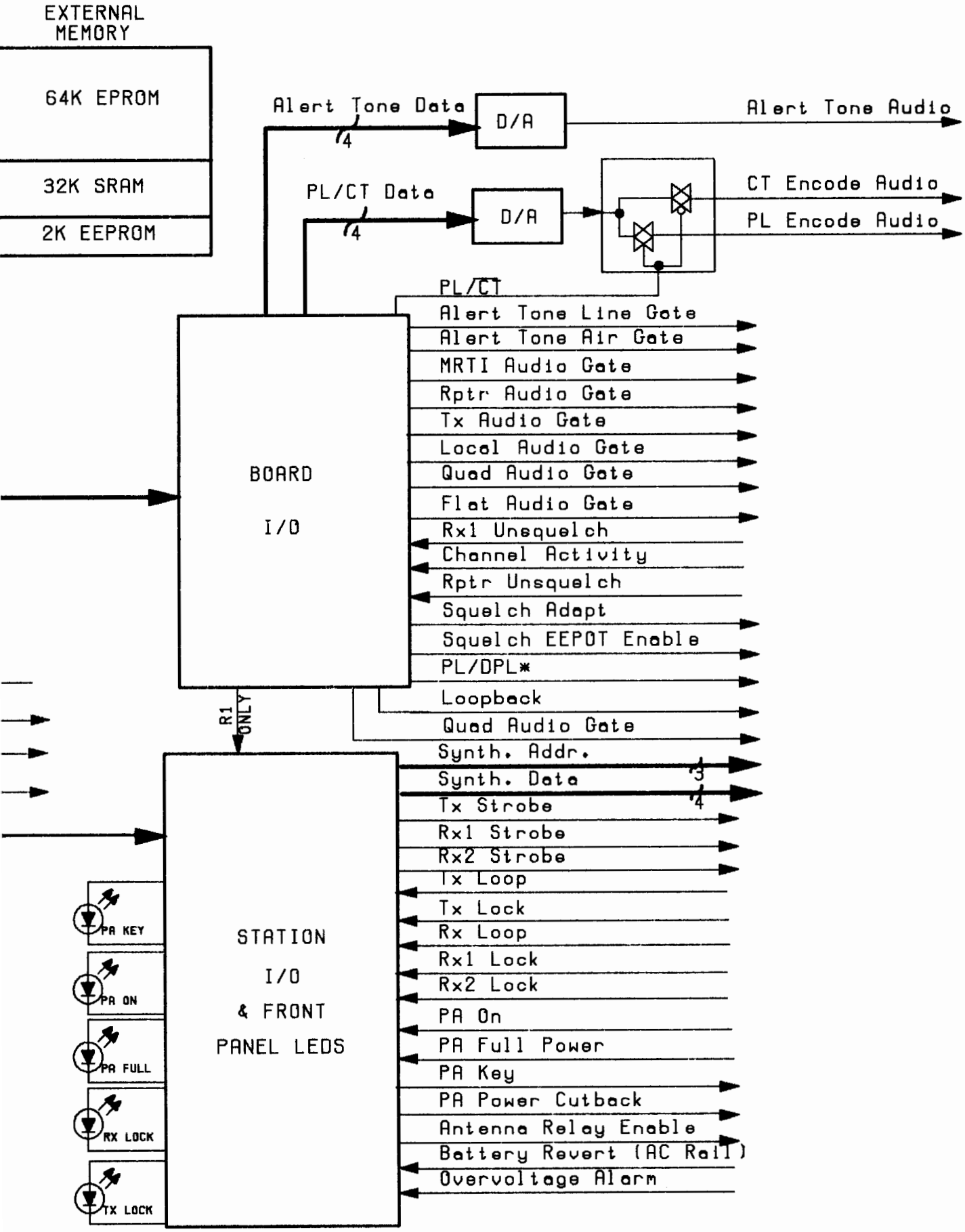
*Lines with this symbol can be jumpered to control board function


IPCB Data
IPCB
Serial Port Data
SCI
Expansion Reset
Low Voltage Reset
Delayed Reset
RESET CIRCUITRY
MCU Reset
PL Strip
Patch PTT
Monitor
Patch Inhibit
Rx Carrier Indicate
Aux Rx Carrier Indicate
MRTI I/O
D0-D7
8
68HC11 MCU
PL Decode Data
Mod Audio
System Audio
Rx1 Audio
PL Encode Audio
Alert Tone Audio
Line Audio
FWD PWR
RFL PWR
BUFFERS
A/D
MUTE
SECURE
Display Control
4
Segment Control
8
DISABLE
XMIT
MIC PTT
Access Disable
PL Disable
Display Select
Display Change
FRONT PANEL I/O
D0-D7
8
D
8



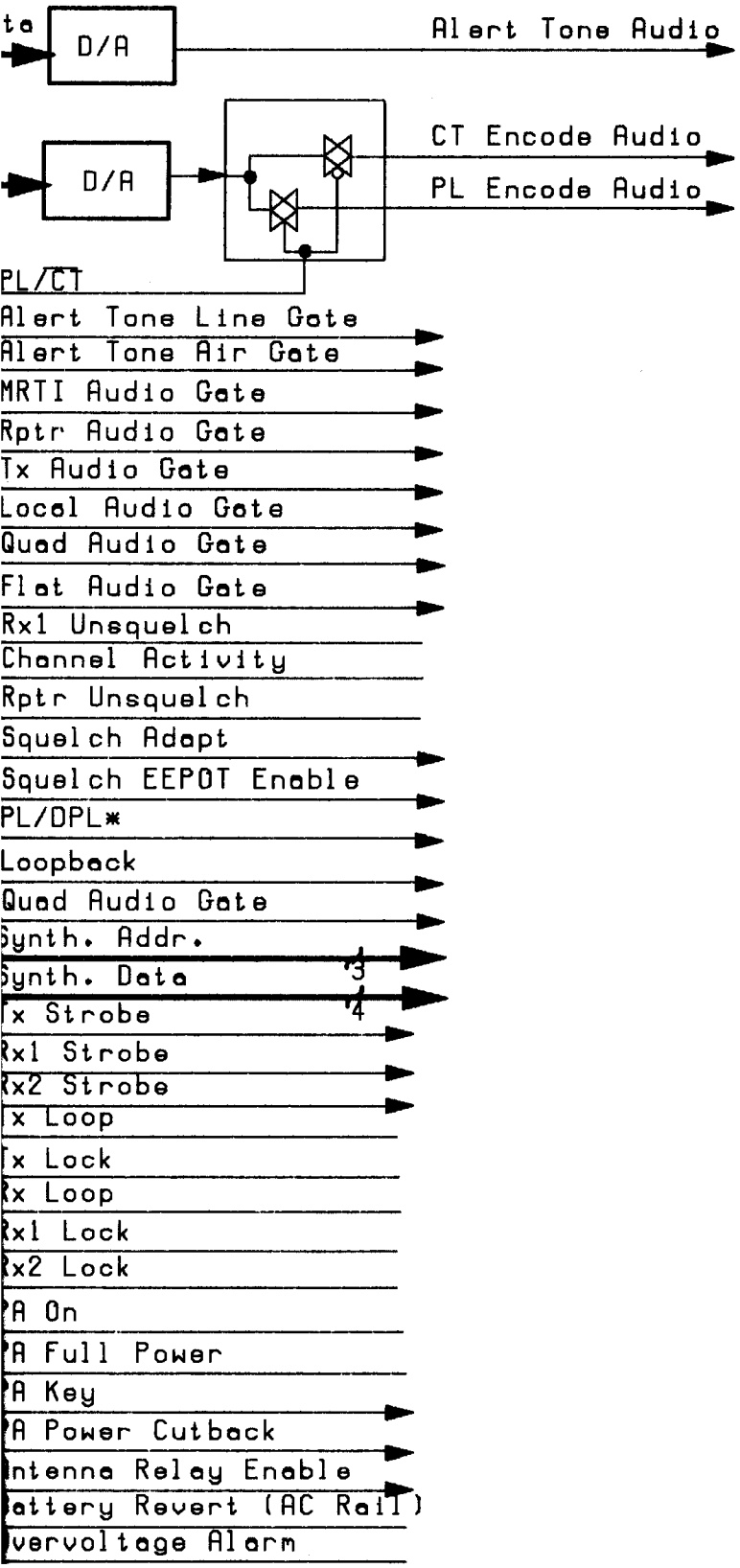
TEPS-48165-0

SHEET 2 OF 2


EXTERNAL MEMORY
64K EPROM
32K SRAM
2K EEPROM
Alert Tone Data
4
D/A
Alert Tone Audio
PL/CT Data
4
D/A
CT Encode Audio
PL Encode Audio
PL/CT
Alert Tone Line Gate
Alert Tone Air Gate
MRTI Audio Gate
Rptr Audio Gate
Tx Audio Gate
Local Audio Gate
Quad Audio Gate
Flat Audio Gate
Rx1 Unsquelch
Channel Activity
Rptr Unsquelch
Squelch Adapt
Squelch EEPOT Enable
PL/DPL*
Loopback
Quad Audio Gate
BOARD
I/O
R1 ONLY
Synth. Addr.
Synth. Data
3
4
Tx Strobe
Rx1 Strobe
Rx2 Strobe
Tx Loop
Tx Lock
Rx Loop
Rx1 Lock
Rx2 Lock
PA On
PA Full Power
PA Key
PA Power Cutback
Antenna Relay Enable
Battery Revert (AC Rail)
Overvoltage Alarm
STATION
I/O
& FRONT
PANEL LEDS
PA KEY
PA ON
PA FULL
RX LOCK
TX LOCK

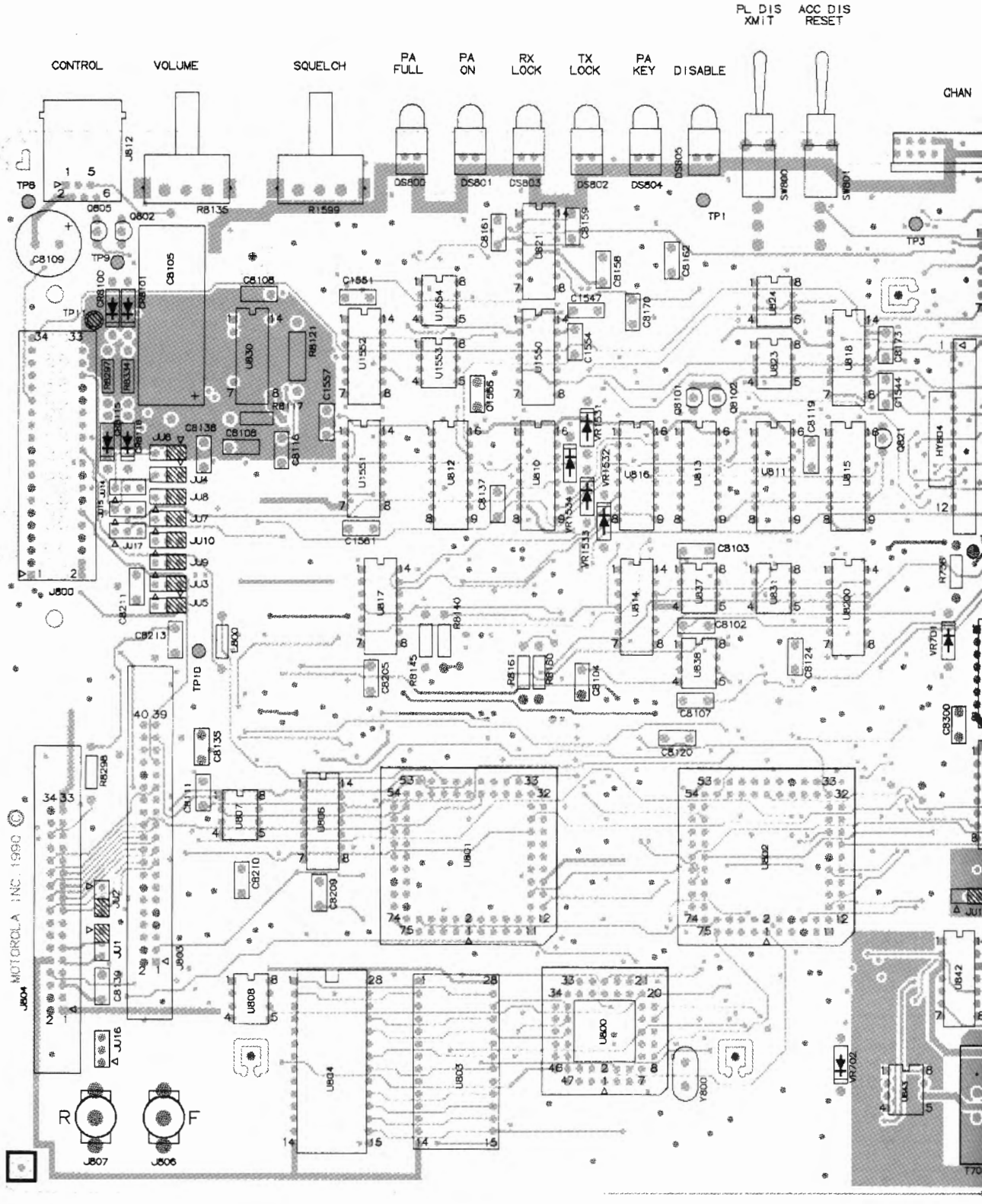
SECURE CAPABLE STATION CONTROL BOARD

BLOCK DIAGRAM



SECURE CAPABLE STATION CONTROL BOARD

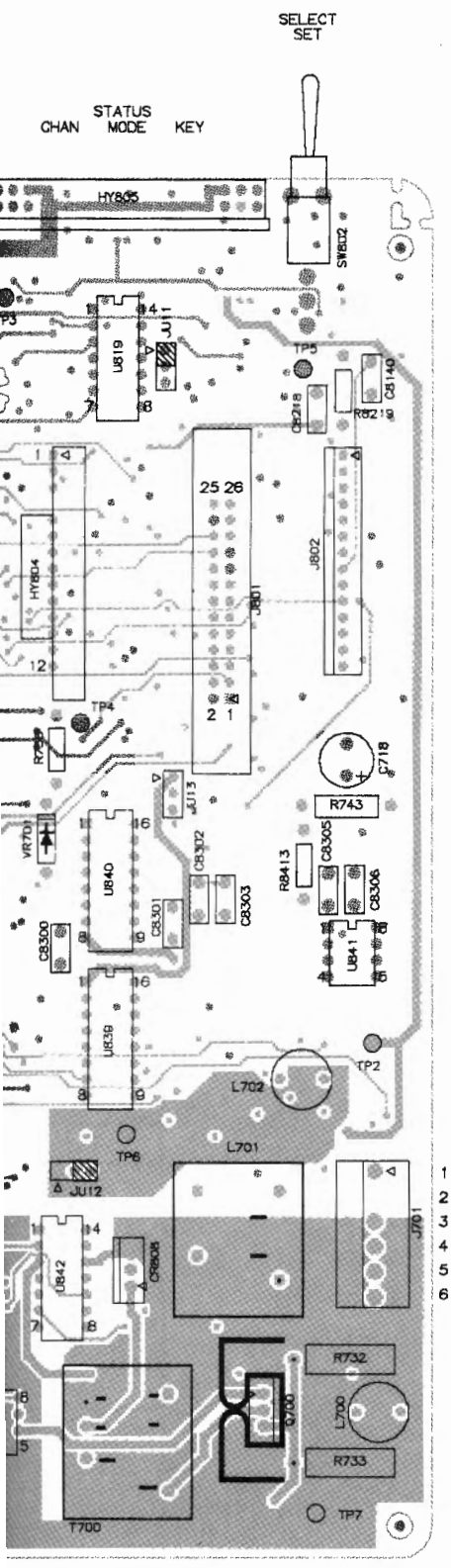
CIRCUIT BOARD DETAIL



SHOWN FROM COMPONENT SIDE

OL - TEPS - 48145-O

BD - TEPS - 48146-O



1 Aux +13.8V (A++)
2
3 Overvoltage Alarm *
4 Battery Revert * (AC Fail*)
5 Gnd B
6 Normalized IF Envelope (800/896 MHz)

NOTE:

AN ASTERISK (*) FOLLOWING A SIGNAL NAME INDICATES AN ACTIVE LOW LEVEL SIGNAL.

J802
PIN OUT DETAIL

1	Logic Gnd
2	MRTI PL Strip *
3	Logic Gnd
4	MRTI Monitor *
5	MRTI PTT *
6	Logic Gnd
7	Audio Gnd
8	IN MRTI Audio
9	Logic Gnd
10	Out MRTI Audio
11	MRTI Rx Carrier
12	MRTI Inhibit
13	N.C.
14	MRTI Aux Indicate
15	N.C.
16	A++
17	A++
18	Audio Gnd
19	N.C.
20	N.C.

J800
PIN OUT DETAIL

Quad 1 Audio	39	40	Audio Ground
Audio Gnd	37	38	Rx1 Audio
Rx2 Audio	35	36	Tx Audio
Local Audio	33	34	Tx Data Audio
GCC/RAC Data Audio	31	32	Select Audio
Quad 2 Audio	29	30	Diversity Audio
Audio Spare	27	28	Gen Tx Data
Logic Spare	25	26	Audio Spare
Shut Down	23	24	Logic Spare
Logic Gnd	21	22	DS *
BD2 *	19	20	BD3 *
BD0 *	17	18	BD1 *
BA2	15	16	BA3
BA0	13	14	BA1
IPCB	11	12	Expansion Reset *
Audio Gnd	9	10	Audio Gnd
Audio Gnd	7	8	Audio Gnd
A++	5	6	Audio Gnd
A++	3	4	A++
A++	1	2	A++

J801
PIN OUT DETAIL

Tx Strobe	26	25	Rx1 Strobe
SA0	24	23	SD3
SA1	22	21	SD2
SA2	20	19	SD1
Tx Loop	18	17	SD0
PA Power Cutback *	16	15	Rx1 Lock *
PA Key *	14	13	Rx1 Loop
PA On *	12	11	AGC Ref (800/896)
PA Full Power *	10	9	Rx2 Strobe
Tx Lock *	8	7	Antenna Relay Enable *
Raw Rx2 Audio	6	5	Raw Rx1 Audio
Audio Gnd (Gnd A)	4	3	Tx Mod Audio
Rx2 Lock *	2	1	+9.6V

J803
PIN OUT DETAIL

Audio Gnd	40	39	+5V
N.C.	38	37	Key Battery Gnd
N.C.	36	35	Coded Rx Level *
Secure Alert Tones	34	33	Expansion Reset *
Coded Mod Level *	32	31	Level Inc
Level U/D *	30	29	IPCB
In MRTI Audio	28	27	Quad Audio
N.C.	26	25	DS *
BA0	24	23	BA1 *
BA2	22	21	BA3 *
BD0 *	20	19	BD1 *
BD2 *	18	17	BD3 *
Logic Gnd	16	15	HSR Syn
Logic Gnd	14	13	HSR Clock
Logic Gnd	12	11	HSR to Secure
Logic Gnd	10	9	HSR In
Local Audio	8	7	Coded Mod Audio
Raw Tx Audio	6	5	Tx Audio
Secure Rx Audio	4	3	+9.6V
Audio Gnd	2	1	Audio Gnd

J804
PIN OUT DETAIL

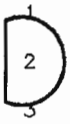
Audio Gnd	34	33	+5V
A++	32	31	+5V
Gen Tx Data	30	29	Mute
Expansion Reset *	28	27	Connect Tone Audio
IPCB	26	25	DS *
BA0	24	23	BA1
BA2	22	21	BA3
BD0 *	20	19	BD1 *
BD2 *	18	17	BD3 *
Logic Gnd	16	15	HSR Syn
Logic Gnd	14	13	HSR Clock
Logic Gnd	12	11	HSR from TTRC
Logic Gnd	10	9	HSR Out
Quad Audio	8	7	TKG Mod Audio
Raw Tx Audio	6	5	Tx Audio
Line Audio	4	3	9.6V
Audio Gnd	2	1	A++

J812
PIN OUT DETAIL

IPCB	6	5	Spkr Audio
MIC PTT *	4	3	MIC Audio
Audio Ground	2	1	Logic Ground

TRANSISTOR DET
(TOP VIEW)

4800869642
4800869328
4800869643
4811043C05
4811043C26
4811043C06



1 -EMITTER
2 -BASE
3 -COLLECT

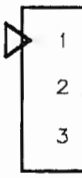
4811043C37
4800869653

1 -DRAIN
2 -SOURCE
3 -GATE

4800869822

1 -EMITTE
2 -BASE
3 -COLLEC

4883875D



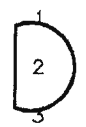
1 -CATHO
2 -ANODE
3 -GATE

NOTE: SHADED
DEFAULT

REQ'S BD-TEPS-48146

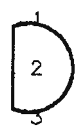
NSISTOR DETAILS
(TOP VIEW)

4800869642
4800869328
4800869643
4811043C05
4811043C26
4811043C06



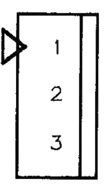
1 -EMITTER
2 -BASE
3 -COLLECTOR

4811043C37
4800869653



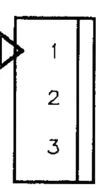
1 -DRAIN
2 -SOURCE
3 -GATE

4800869829

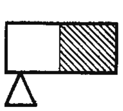


1 -EMITTER
2 -BASE
3 -COLLECTOR

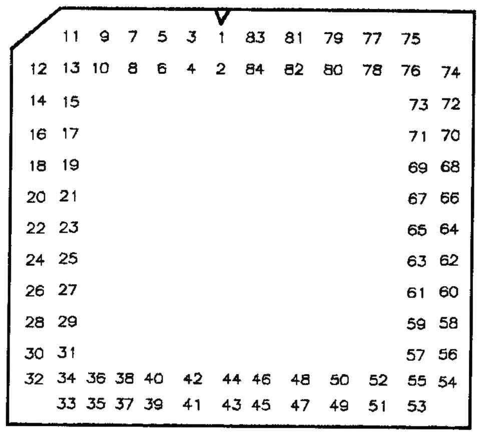
4883875D05



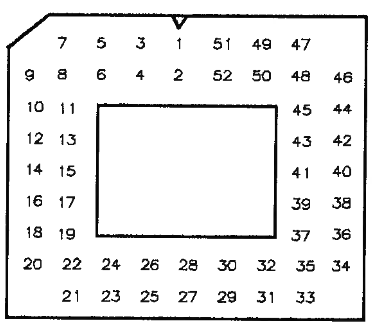
1 -CATHODE
2 -ANODE
3 -GATE



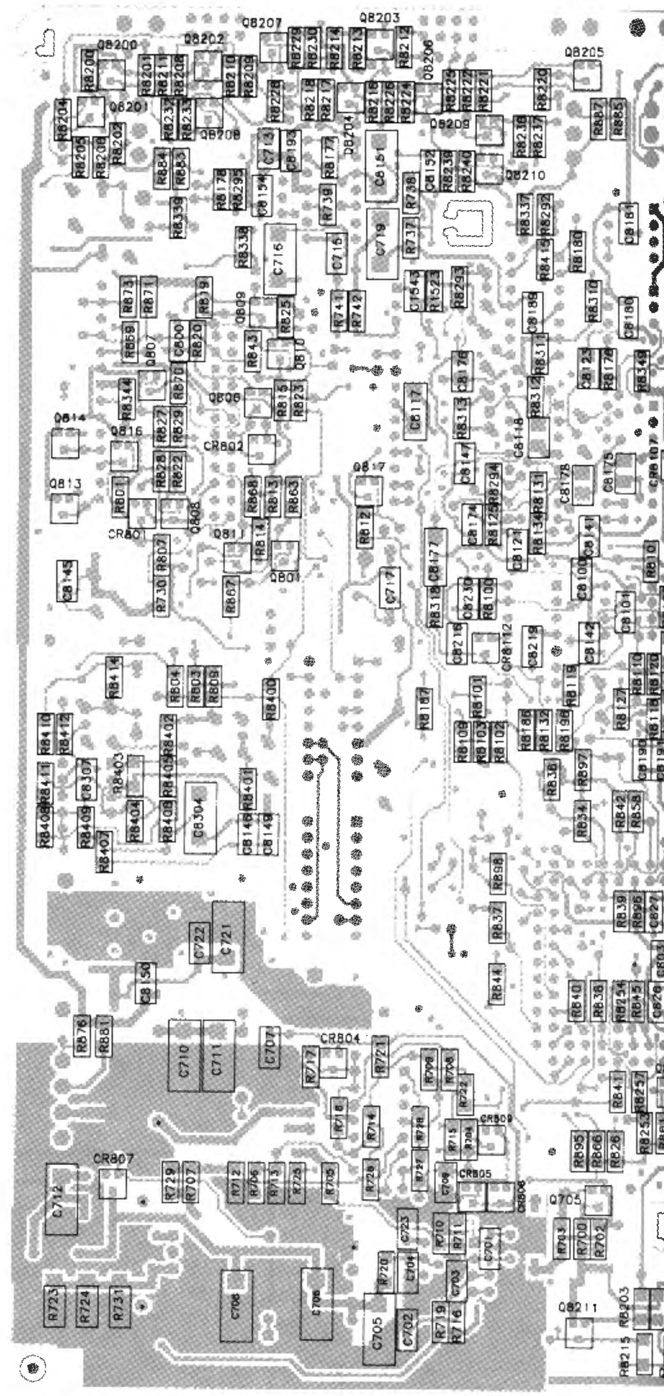
E: SHADED AREA INDICATES
DEFAULT JUMPER POSITION.



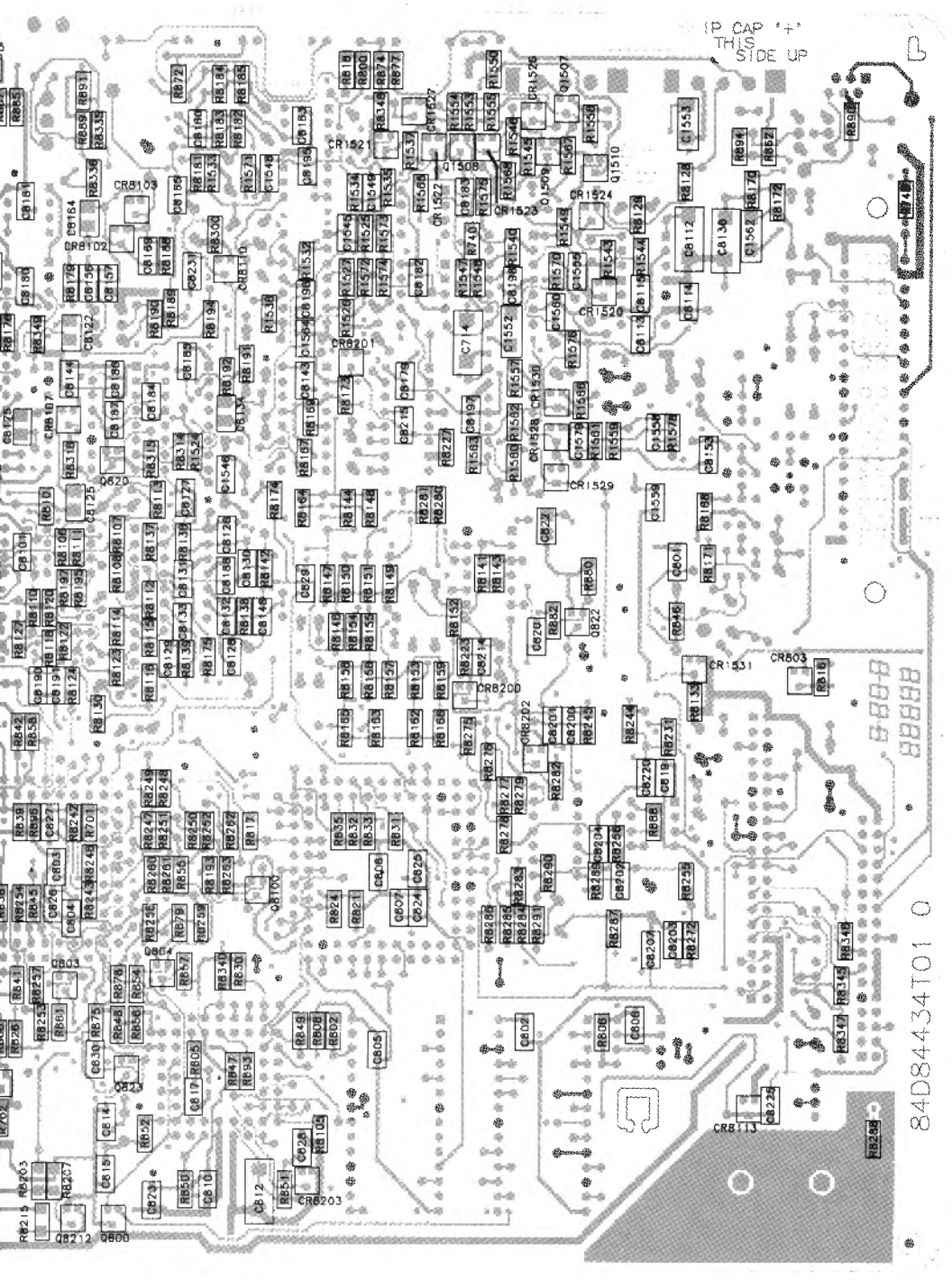
ASIC SOCKET DETAIL



uP SOCKET DETAIL



SHOWN FROM SOLDER SIDE



PNP
4811056A08
4811056B08
4811056C08

NPN
4811056A03
4811056B03
4811056C21

DARLINGTON NPN
4811056A23
4811056B23
4811056C23

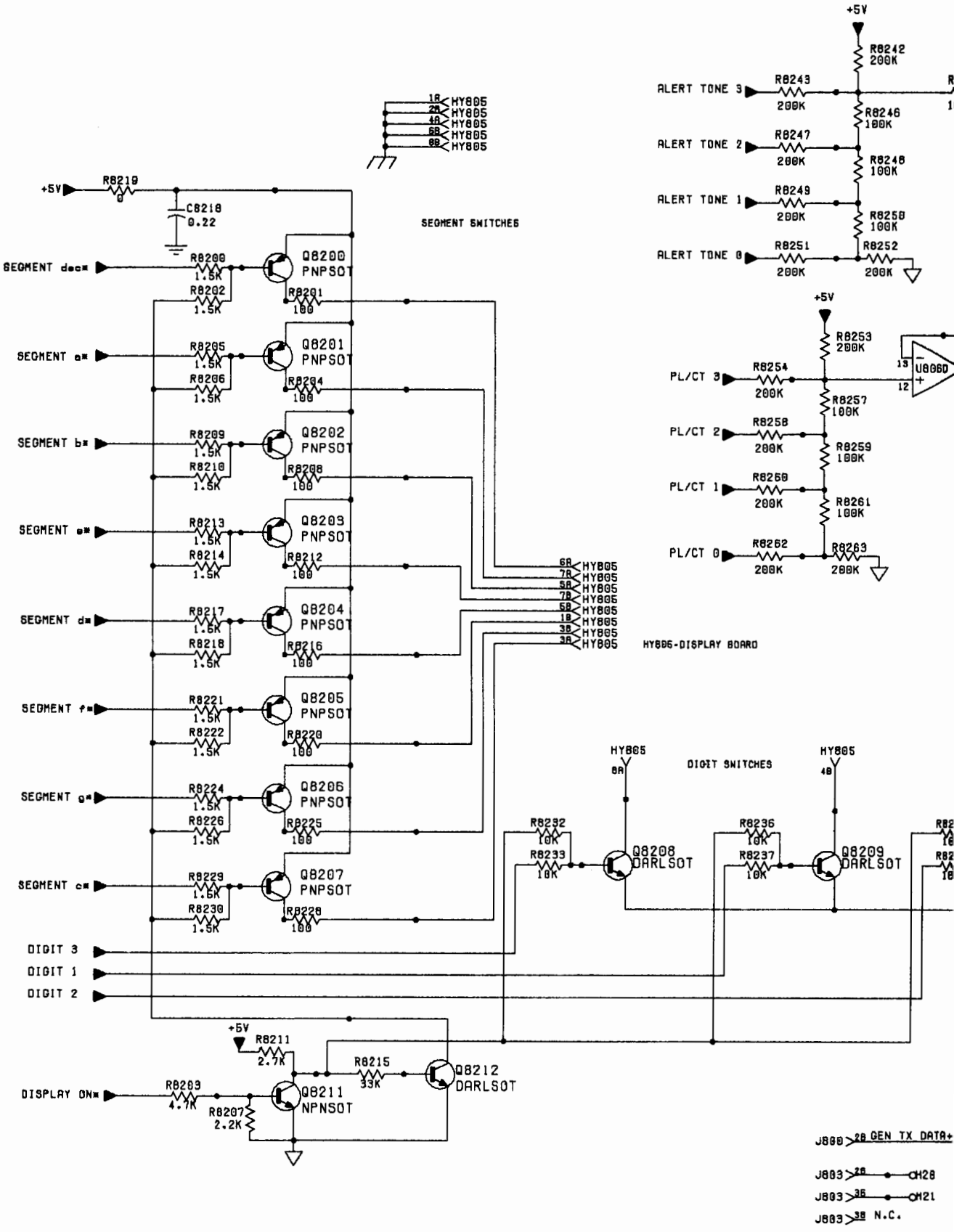
DIODE
4811058A11
4811058B11
4811058C11
4805129M41
4811058A04
4811058B04
4811058C04

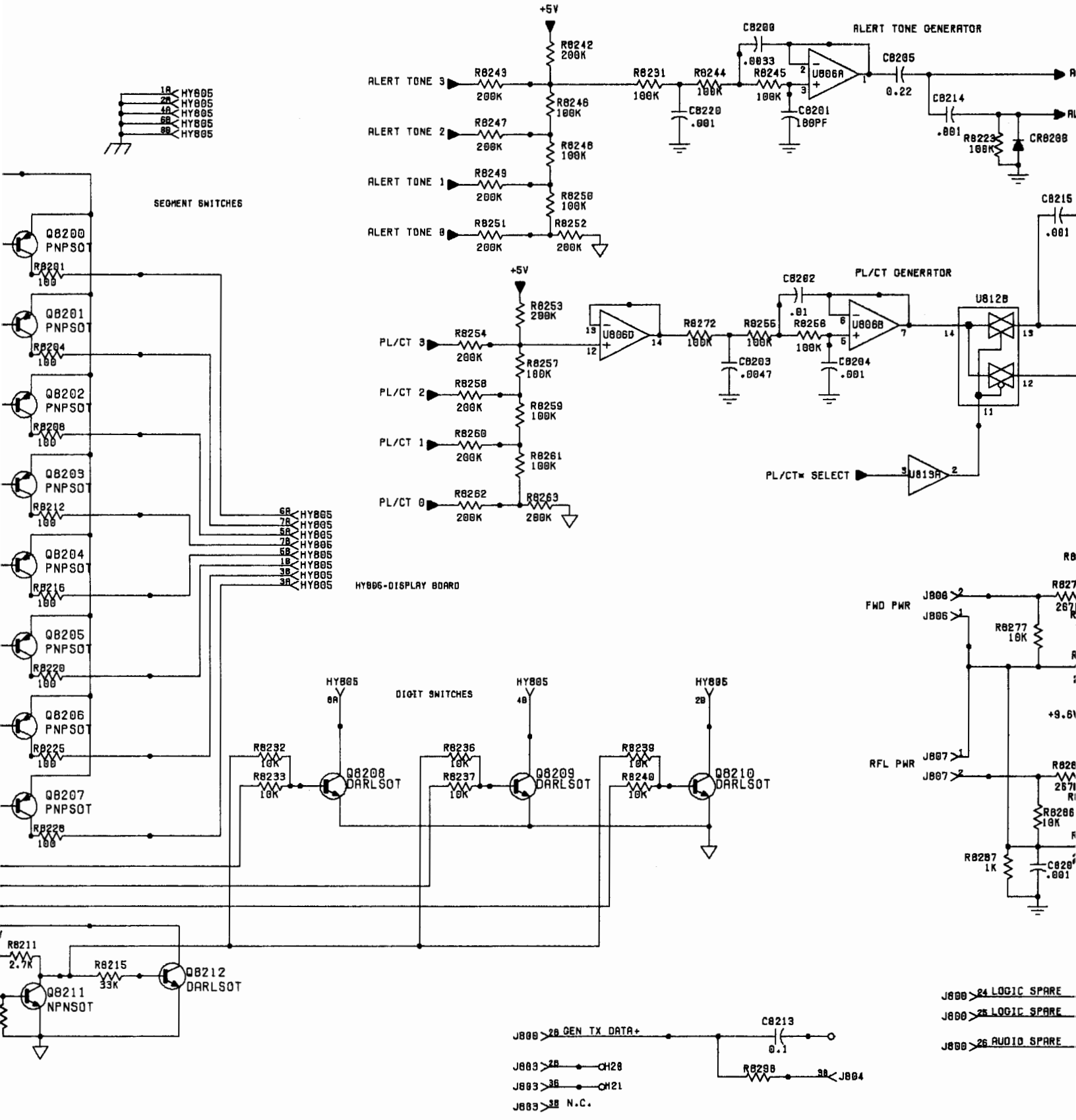
DUAL DIODE
4884336R03

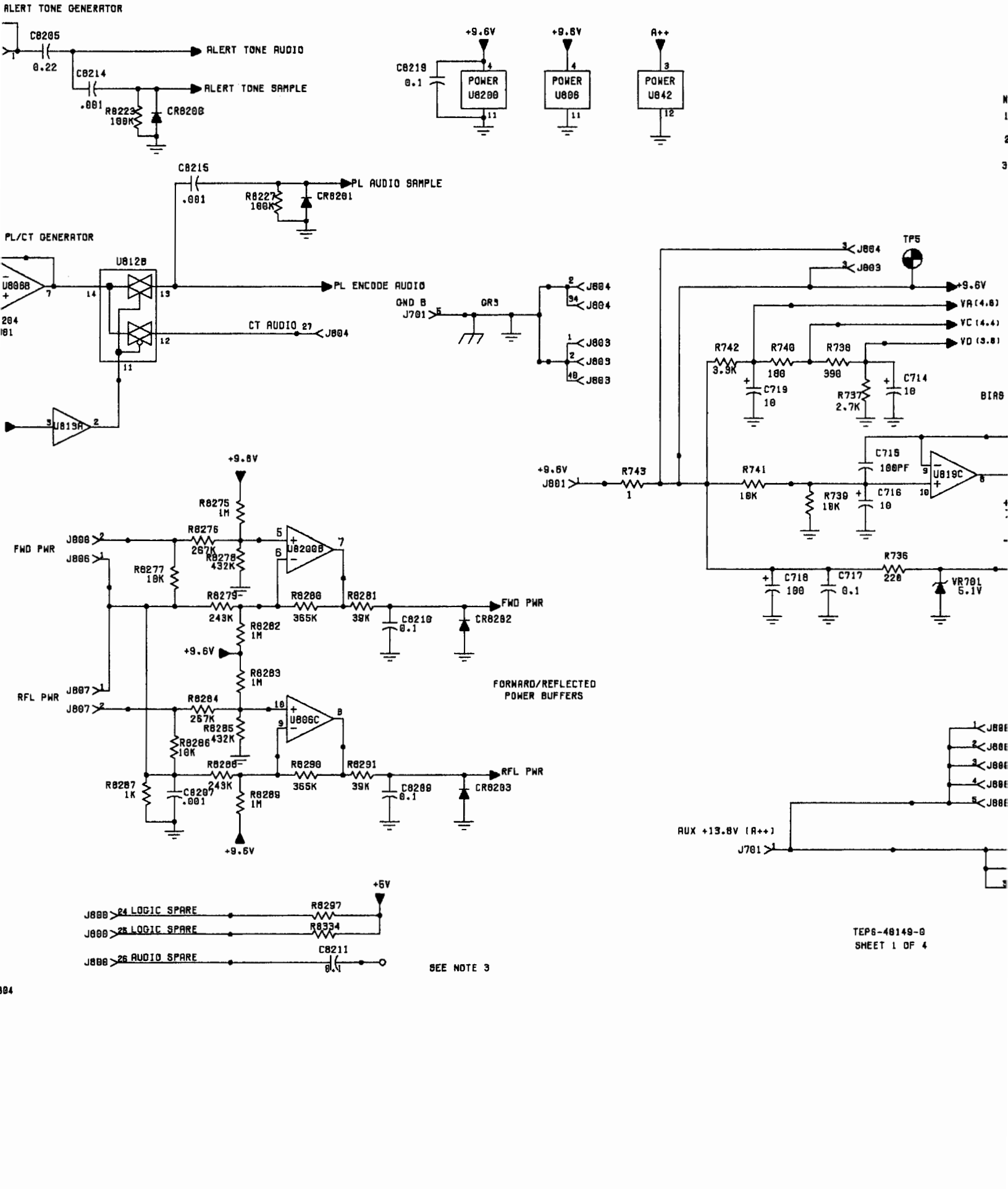
STANDARD SOT
PACKAGE PIN-OUT

OL -TEPS-48148-0

BD -TEPS-48147-0

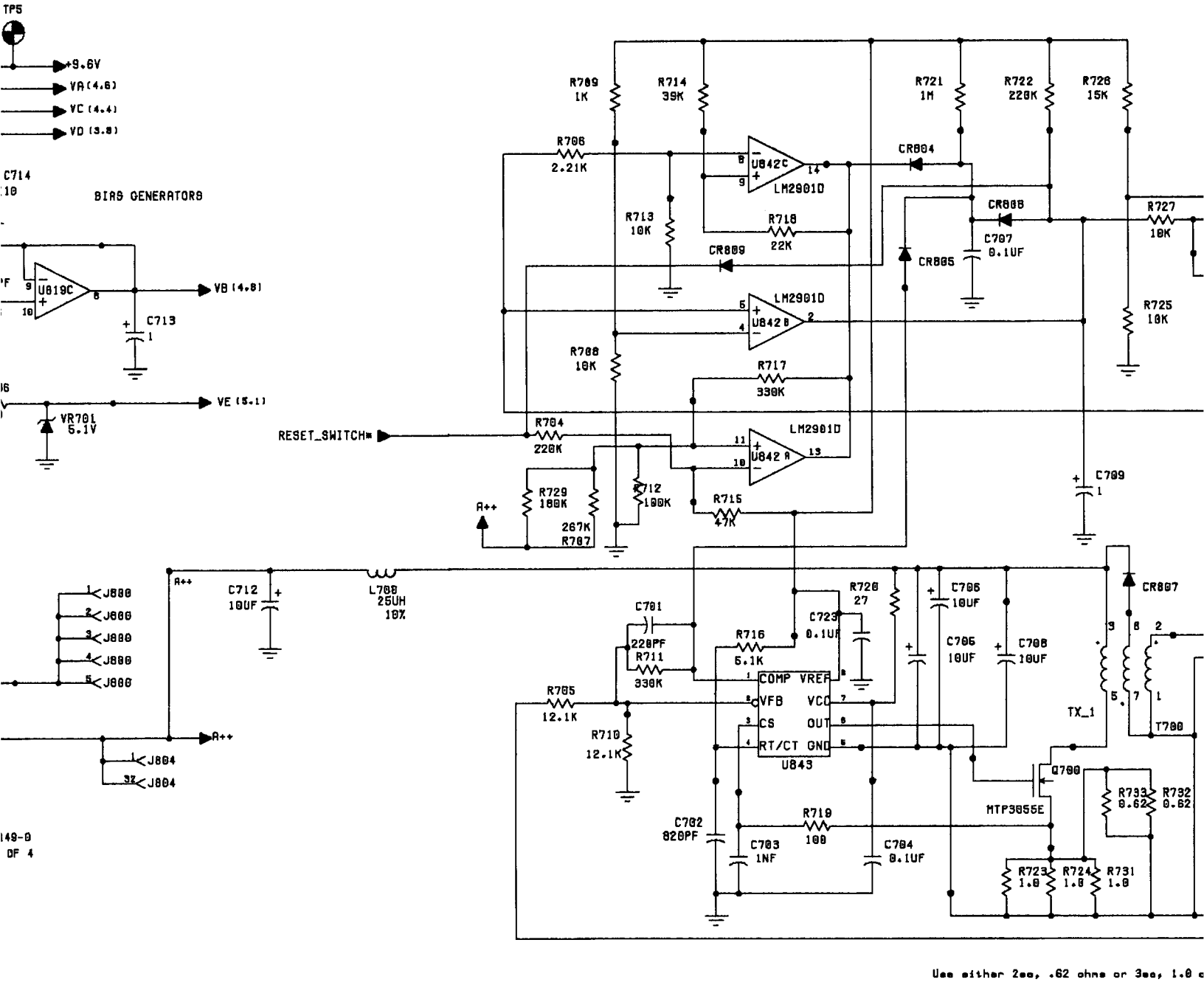

+5V
R8242 200K
ALERT TONE 3
R8243 200K
R8246 100K
ALERT TONE 2
R8247 200K
R8248 100K
ALERT TONE 1
R8249 200K
R8250 100K
ALERT TONE 0
R8251 200K
R8252 200K
1A HY805
2A HY805
4A HY805
6A HY805
8A HY805
SEGMENT SWITCHES
+5V
R8219 0
C8218 0.22
SEGMENT dec=
R8200 1.5K
R8202 1.5K
Q8200 PNPSOT
R8201 100
SEGMENT a=
R8205 1.5K
R8206 1.5K
Q8201 PNPSOT
R8204 100
SEGMENT b=
R8209 1.5K
R8210 1.5K
Q8202 PNPSOT
R8208 100
SEGMENT e=
R8213 1.5K
R8214 1.5K
Q8203 PNPSOT
R8212 100
SEGMENT d=
R8217 1.5K
R8218 1.5K
Q8204 PNPSOT
R8216 100
SEGMENT f=
R8221 1.5K
R8222 1.5K
Q8205 PNPSOT
R8220 100
SEGMENT g=
R8224 1.5K
R8226 1.5K
Q8206 PNPSOT
R8225 100
SEGMENT c=
R8229 1.5K
R8230 1.5K
Q8207 PNPSOT
R8228 100
6A HY805
7A HY805
5A HY805
7B HY805
5B HY805
1B HY805
3B HY805
3A HY805
HY805-DISPLAY BOARD
+5V
R8253 200K
PL/CT 3
R8254 200K
R8257 100K
PL/CT 2
R8258 200K
R8259 100K
PL/CT 1
R8260 200K
R8261 100K
PL/CT 0
R8262 200K
R8263 200K
U806D
13
12
HY805 8A
DIGIT SWITCHES
HY805 4B
R8232 10K
R8233 10K
Q8208 DARLSOT
R8236 10K
R8237 10K
Q8209 DARLSOT
DIGIT 3
DIGIT 1
DIGIT 2
+5V
R8211 2.7K
R8215 33K
Q8212 DARLSOT
DISPLAY ON=
R8203 4.7K
R8207 2.2K
Q8211 NPNSOT
J800 28 GEN TX DATA+
J803 28 CH28
J803 26 CH21
J803 38 N.C.


ALERT TONE GENERATOR
SEGMENT SWITCHES
DIGIT SWITCHES
PL/CT GENERATOR
HY805-DISPLAY BOARD
+5V
ALERT TONE 3
ALERT TONE 2
ALERT TONE 1
ALERT TONE 0
PL/CT 3
PL/CT 2
PL/CT 1
PL/CT 0
PL/CT= SELECT
FWD PWR
RFL PWR
Q8200 PNPSOT
Q8201 PNPSOT
Q8202 PNPSOT
Q8203 PNPSOT
Q8204 PNPSOT
Q8205 PNPSOT
Q8206 PNPSOT
Q8207 PNPSOT
Q8208 DARLSOT
Q8209 DARLSOT
Q8210 DARLSOT
Q8211 NPNSOT
Q8212 DARLSOT
U806A
U806B
U806C
U806D
U812B
U813A
J806
J807
J808
J803
J804
GEN TX DATA+
H28
H21
N.C.
LOGIC SPARE
LOGIC SPARE
AUDIO SPARE


ALERT TONE GENERATOR
C8205
0.22
ALERT TONE AUDIO
C8214
.001
ALERT TONE SAMPLE
R8223
100K
CR8208
+9.6V
C8219
0.1
POWER
U8200
+9.6V
POWER
U806
A++
POWER
U842
C8215
.001
R8227
100K
CR8201
PL AUDIO SAMPLE
PL/CT GENERATOR
U8128
PL ENCODE AUDIO
CT AUDIO
J804
GND B
J701
CR9
J804
J803
J803
J803
J804
J804
TP5
J803
+9.6V
VA (4.8)
VC (4.4)
VD (3.8)
R742
3.9K
R740
180
R738
390
C719
10
R737
2.7K
C714
10
BIAS
C715
100PF
U819C
+9.6V
J801
R743
1
R741
10K
R739
10K
C716
10
R736
220
C718
100
C717
0.1
VR701
5.1V
+9.6V
R8275
1M
FWD PWR
J808
J806
R8276
267K
R8278
432K
U8200B
R8277
10K
R8279
243K
R8280
365K
R8281
39K
C8210
0.1
CR8202
FWD PWR
R8282
1M
+9.6V
R8283
1M
RFL PWR
J807
J807
R8284
267K
R8285
432K
U806C
R8286
10K
R8288
243K
R8290
365K
R8291
39K
C8209
0.1
CR8203
RFL PWR
R8287
1K
C8207
.001
R8289
1M
+9.6V
FORWARD/REFLECTED
POWER BUFFERS
AUX +13.8V (A++)
J701
+5V
J808
24 LOGIC SPARE
R8297
J808
25 LOGIC SPARE
R8334
J808
26 AUDIO SPARE
C8211
0.1
SEE NOTE 3
TEP6-48149-0
SHEET 1 OF 4

NOTES:

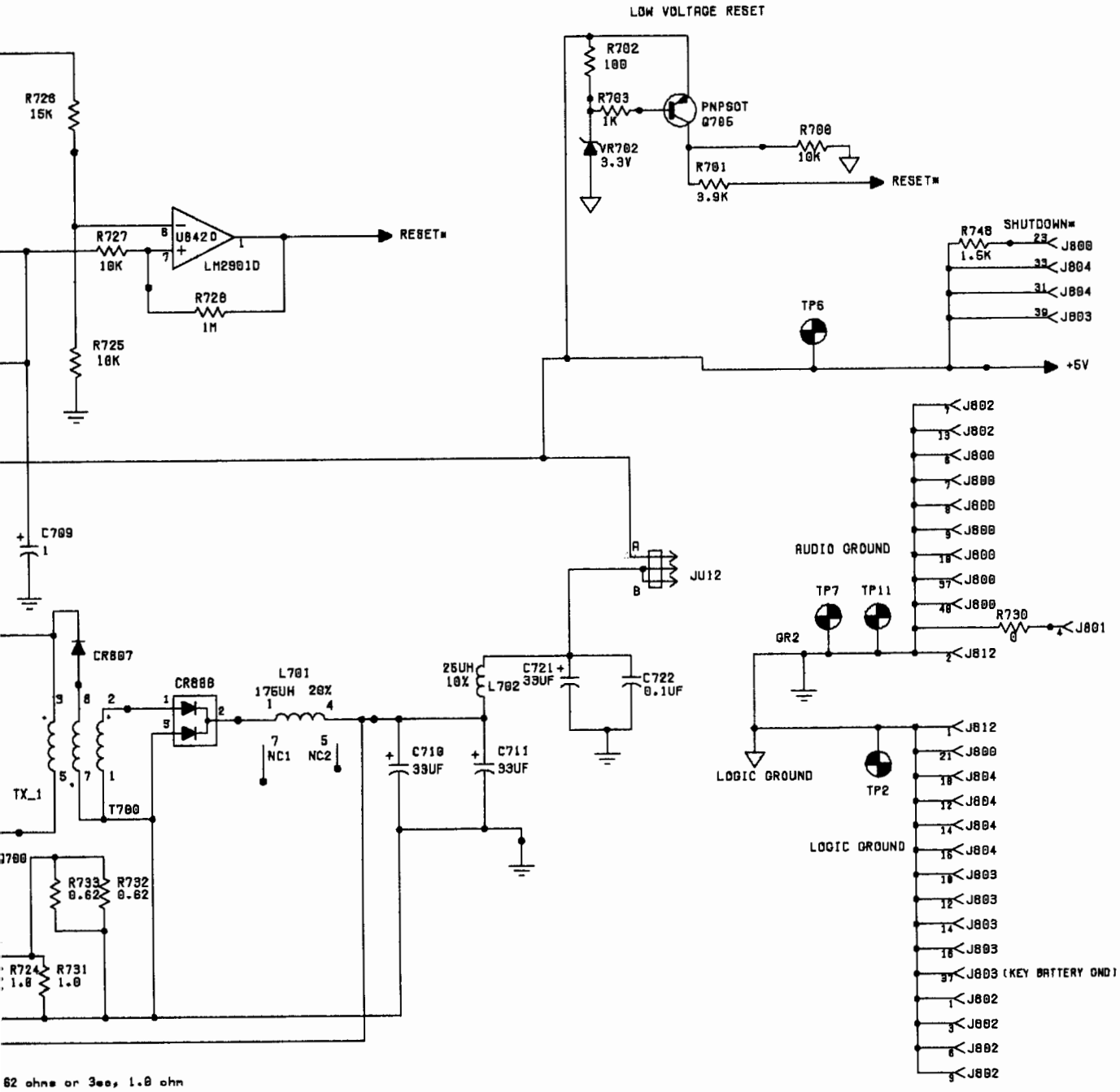
1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but may be added for special applications.



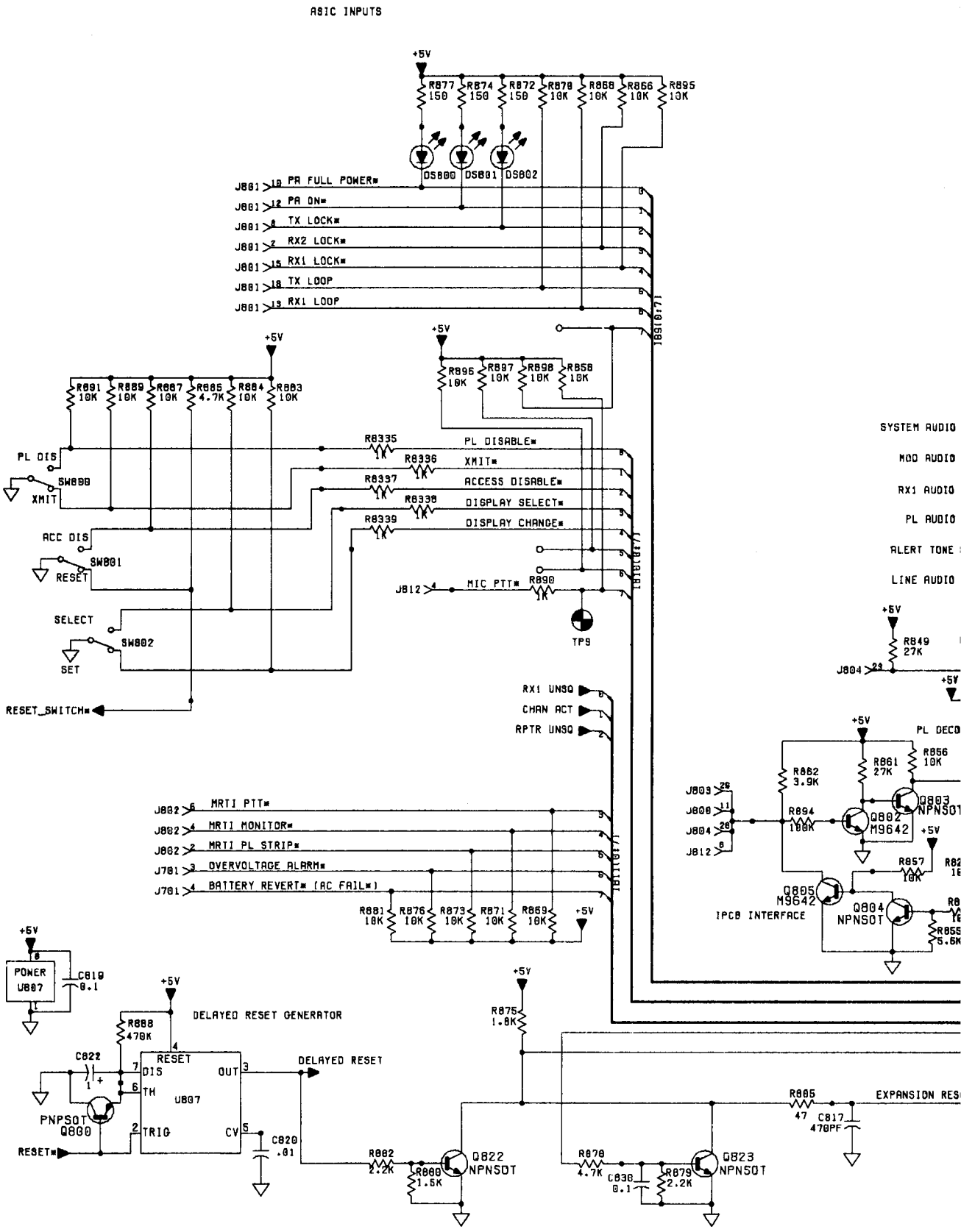
Use either 2ea, .62 ohms or 3ea, 1.0 o

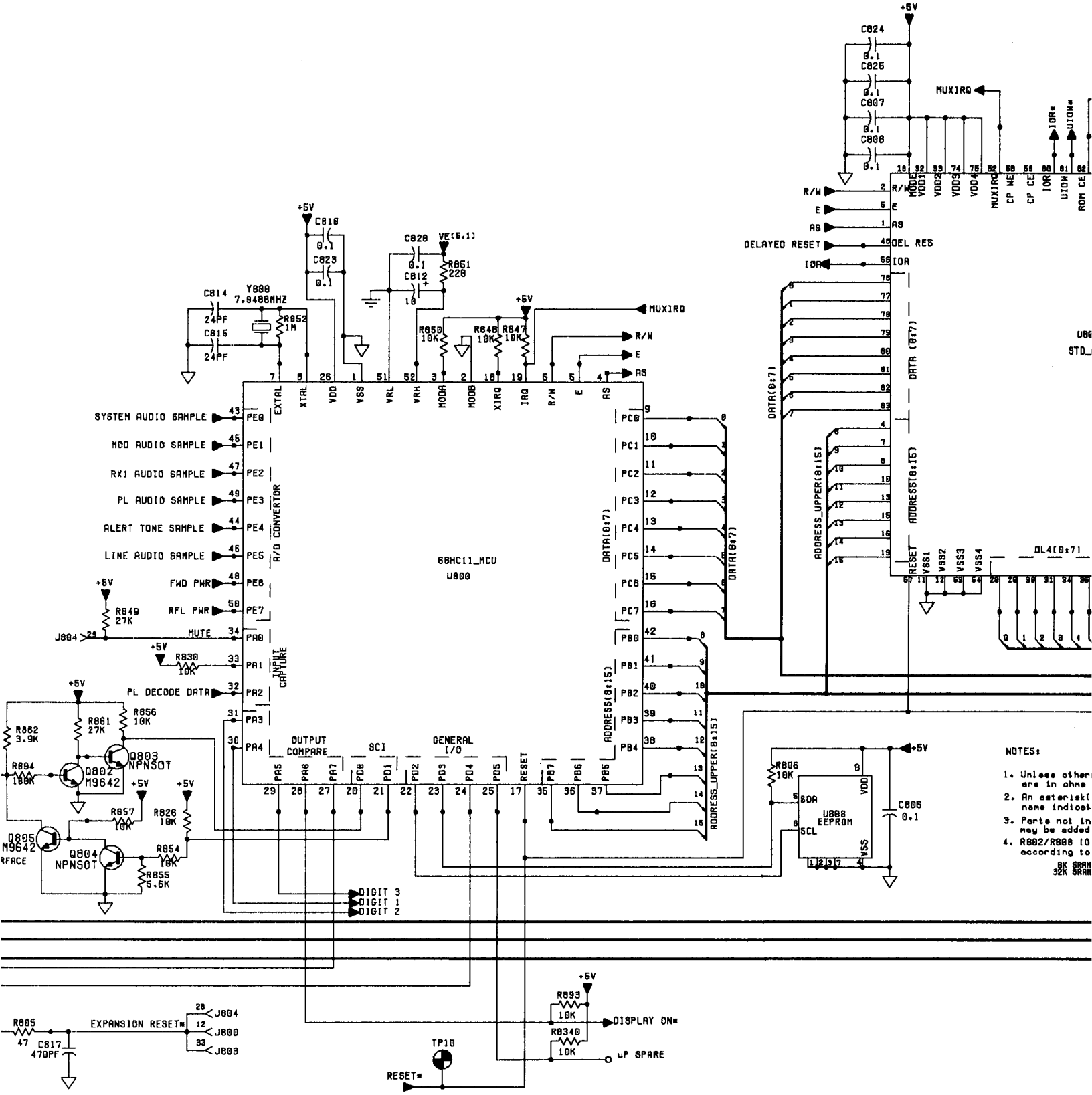
149-0
OF 4

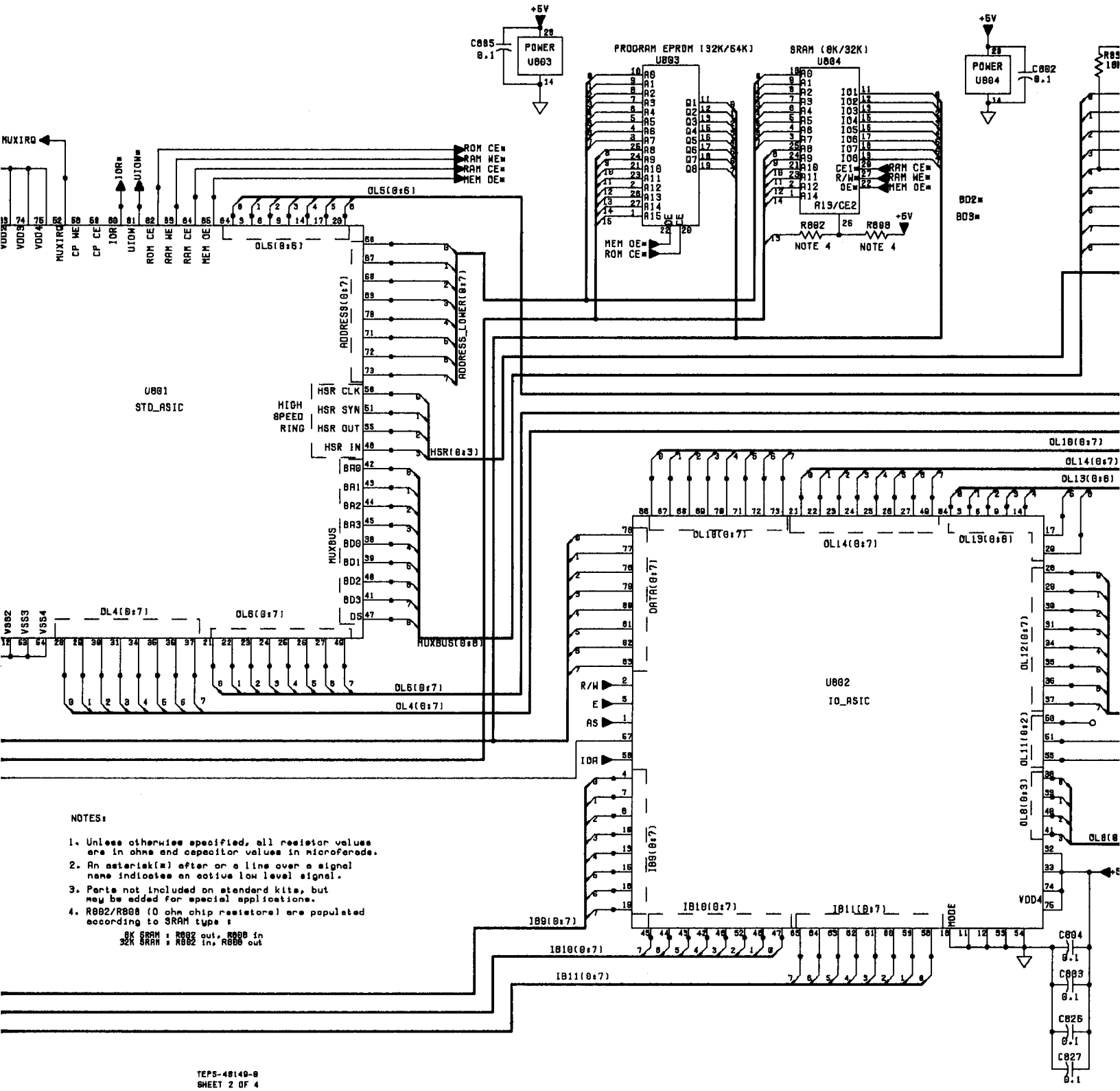
SECURE CAPABLE STATION CONTROL BOARD
SCHEMATIC DIAGRAM



SECURE CAPABLE STATION CONTROL BOARD
SCHEMATIC DIAGRAM



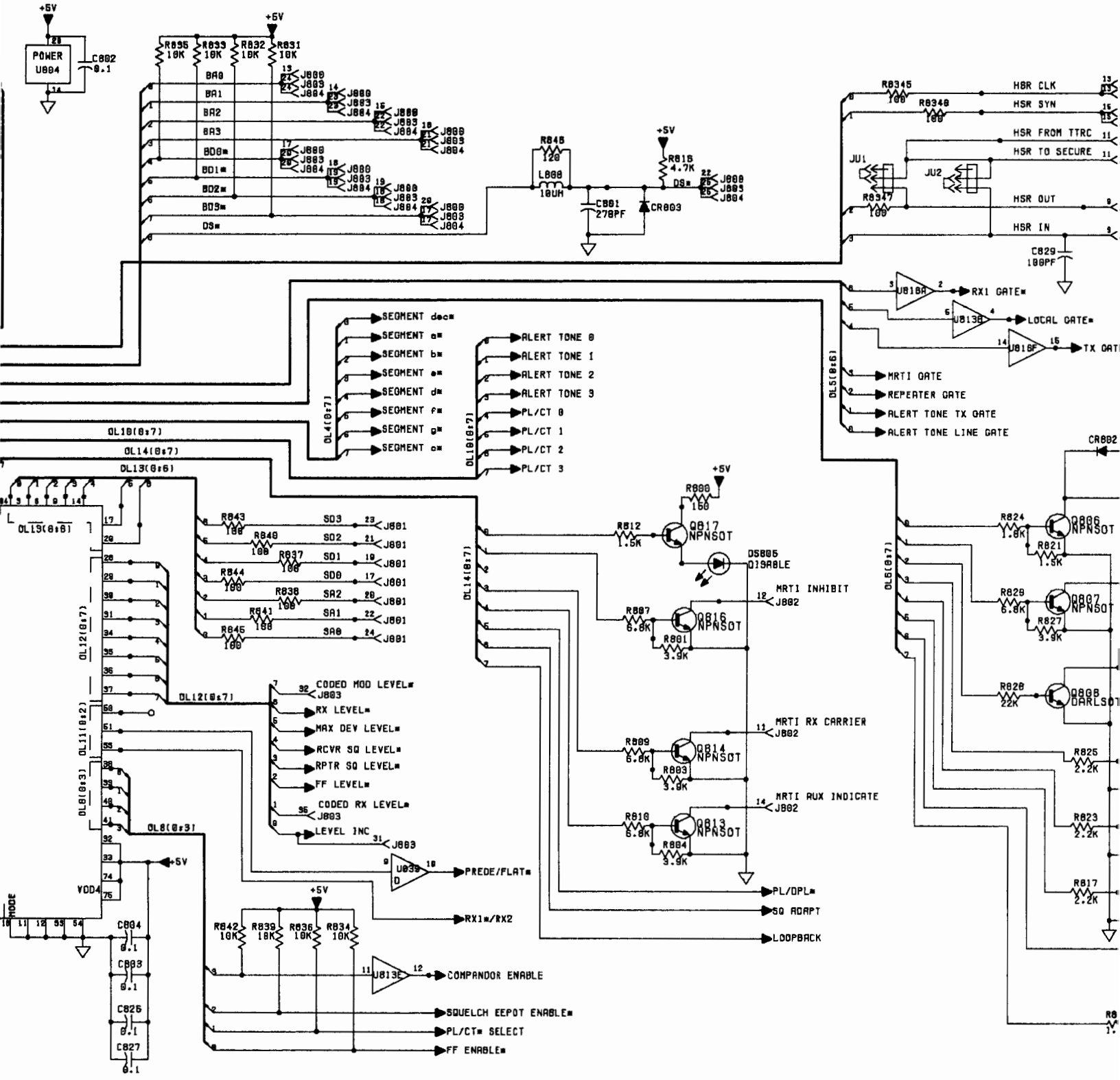

+5V
C824
0.1
C825
0.1
C807
0.1
C808
0.1
MUXIRQ
IOR*
UIOW*
R/W
E
AS
DELAYED RESET
IOR
DEL RES
MODA
VDD1
VDD2
VDD3
VDD4
MUXIRQ
CP WE
CP CE
IOR
UIOW
ROM CE
DATA(8:7)
ADDRESS(8:15)
RESET
VSS1
VSS2
VSS3
VSS4
C810
0.1
C823
0.1
C820
0.1
VE(5.1)
C812
10
R861
220
C814
24PF
C815
24PF
Y800
7.9488MHZ
R852
1M
R650
10K
R648
10K
R647
10K
MUXIRQ
R/W
E
AS
EXTAL
XTAL
VDD
VSS
VRL
VRH
MODA
MODB
XIRQ
IRQ
R/W
E
AS
SYSTEM AUDIO SAMPLE
MDO AUDIO SAMPLE
RX1 AUDIO SAMPLE
PL AUDIO SAMPLE
ALERT TONE SAMPLE
LINE AUDIO SAMPLE
FWD PWR
RFL PWR
MUTE
PE0
PE1
PE2
PE3
PE4
PE5
PE6
PE7
PA0
A/D CONVERTOR
68HC11_MCU
U800
DATA(8:7)
ADDRESS(8:15)
R849
27K
J804
R830
10K
PA1
INPUT CAPTURE
PL DECODE DATA
PA2
PA3
PA4
OUTPUT COMPARE
SCI
GENERAL I/O
PA5
PA6
PA7
PD0
PD1
PD2
PD3
PD4
PD5
RESET
PB7
PB6
PB5
PB0
PB1
PB2
PB3
PB4
R862
3.9K
R861
27K
R856
10K
R894
100K
Q802
M9642
Q803
NPNSOT
R857
10K
R826
10K
Q805
M9642
RFACE
Q804
NPNSOT
R854
10K
R855
5.6K
DIGIT 3
DIGIT 1
DIGIT 2
R806
10K
U808
EEPROM
SDA
SCL
VDD
VSS
C805
0.1
NOTES:
1. Unless other
are in ohms
2. An asterisk(
name indicat
3. Parts not in
may be added
4. R802/R808 (0
according to
8K SRAM
32K SRAM
R885
47
C817
470PF
EXPANSION RESET*
J804
J800
J803
R893
10K
R8340
10K
DISPLAY ON*
uP SPARE
TP10
RESET*

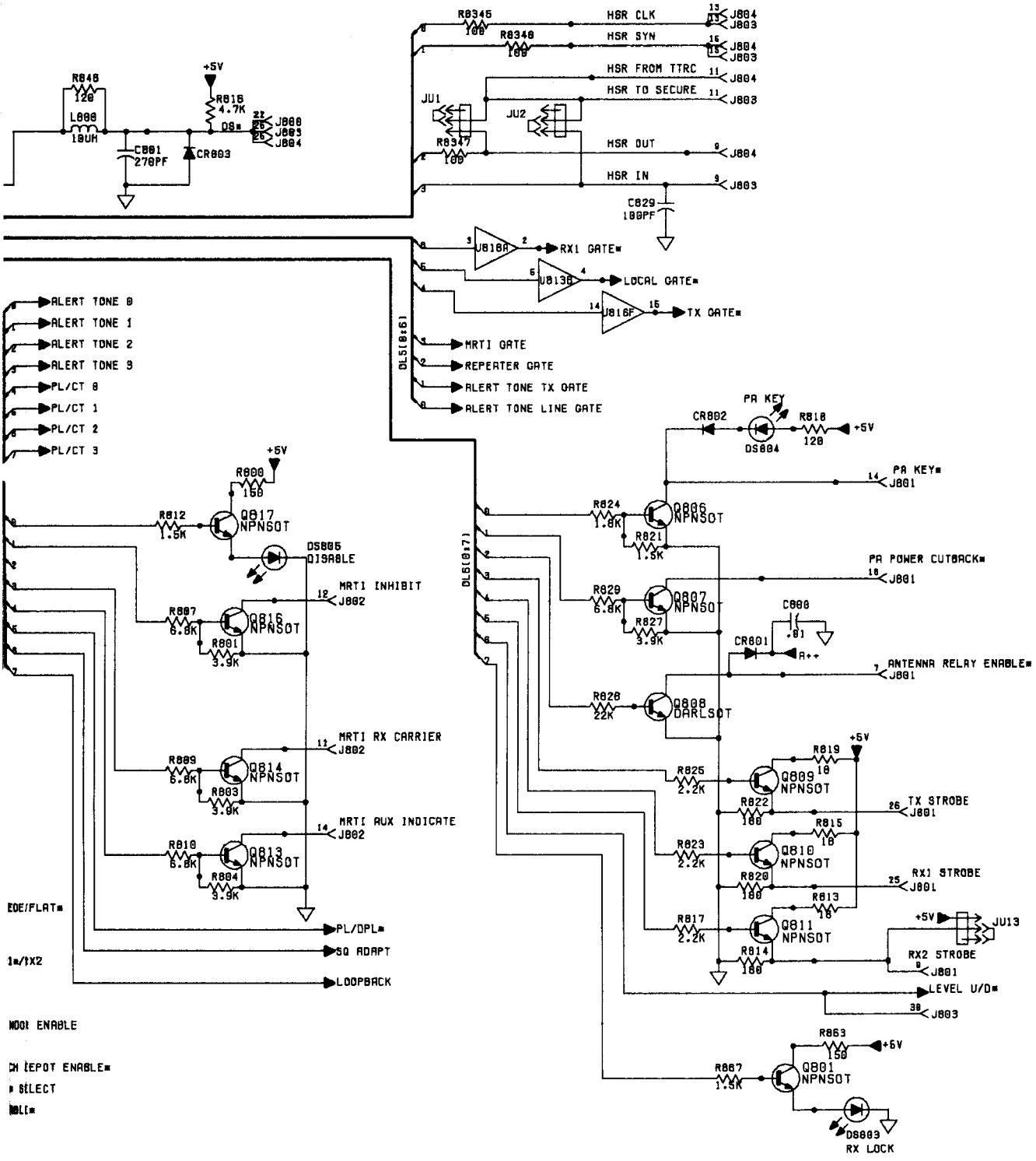


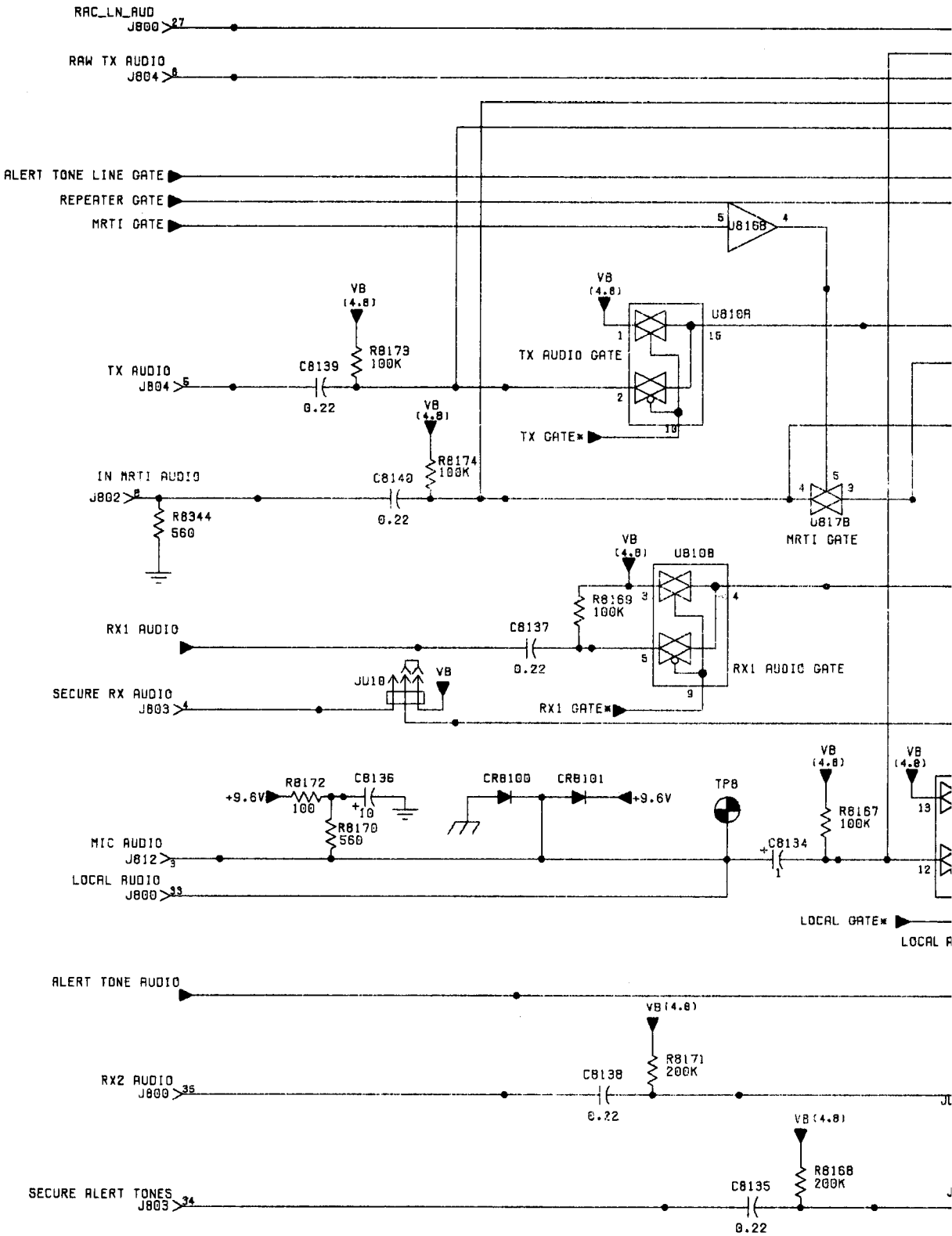
NOTES:

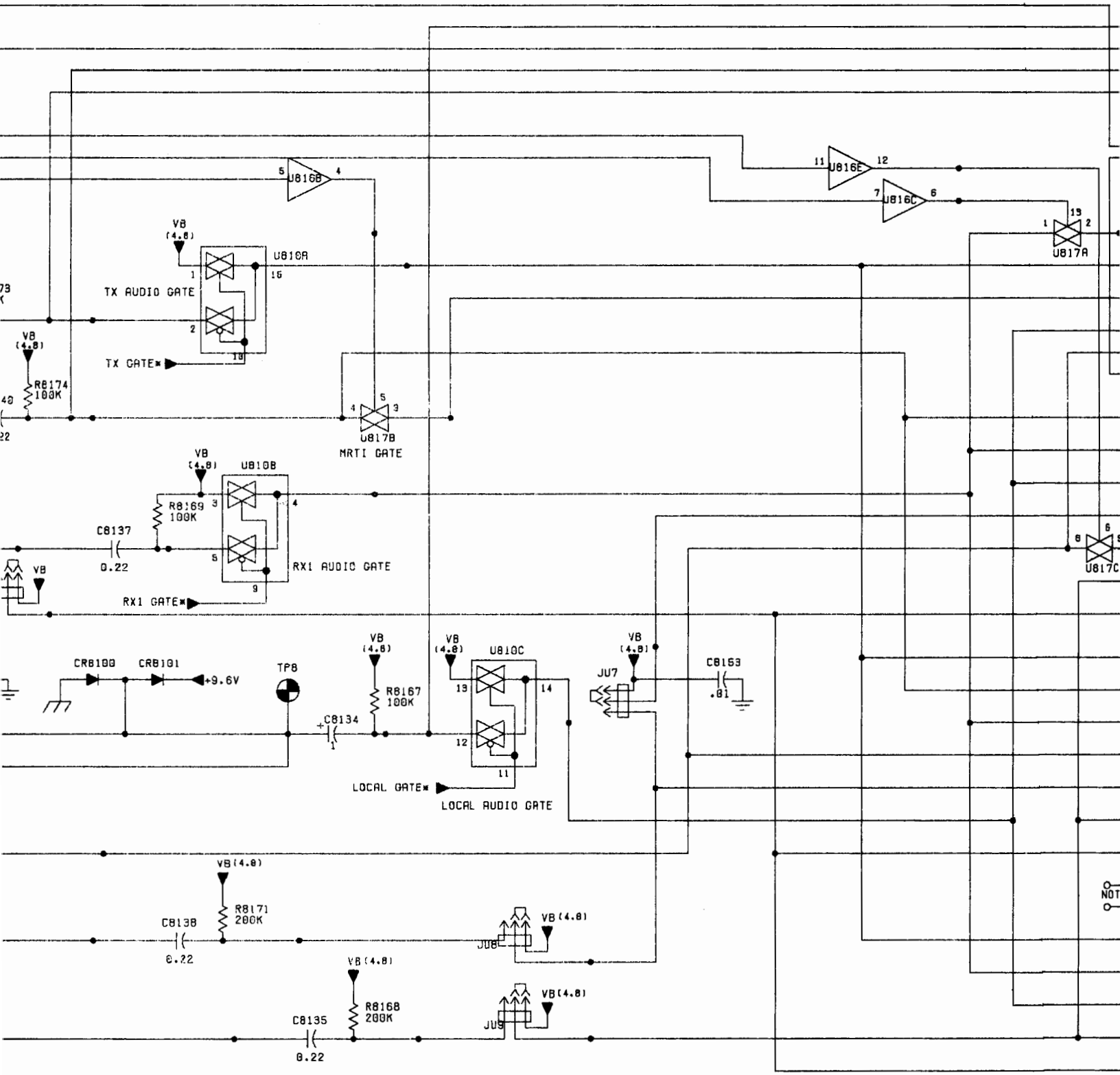
1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(=) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but may be added for special applications.
4. R802/R808 (0 ohm chip resistors) are populated according to SRAM type :

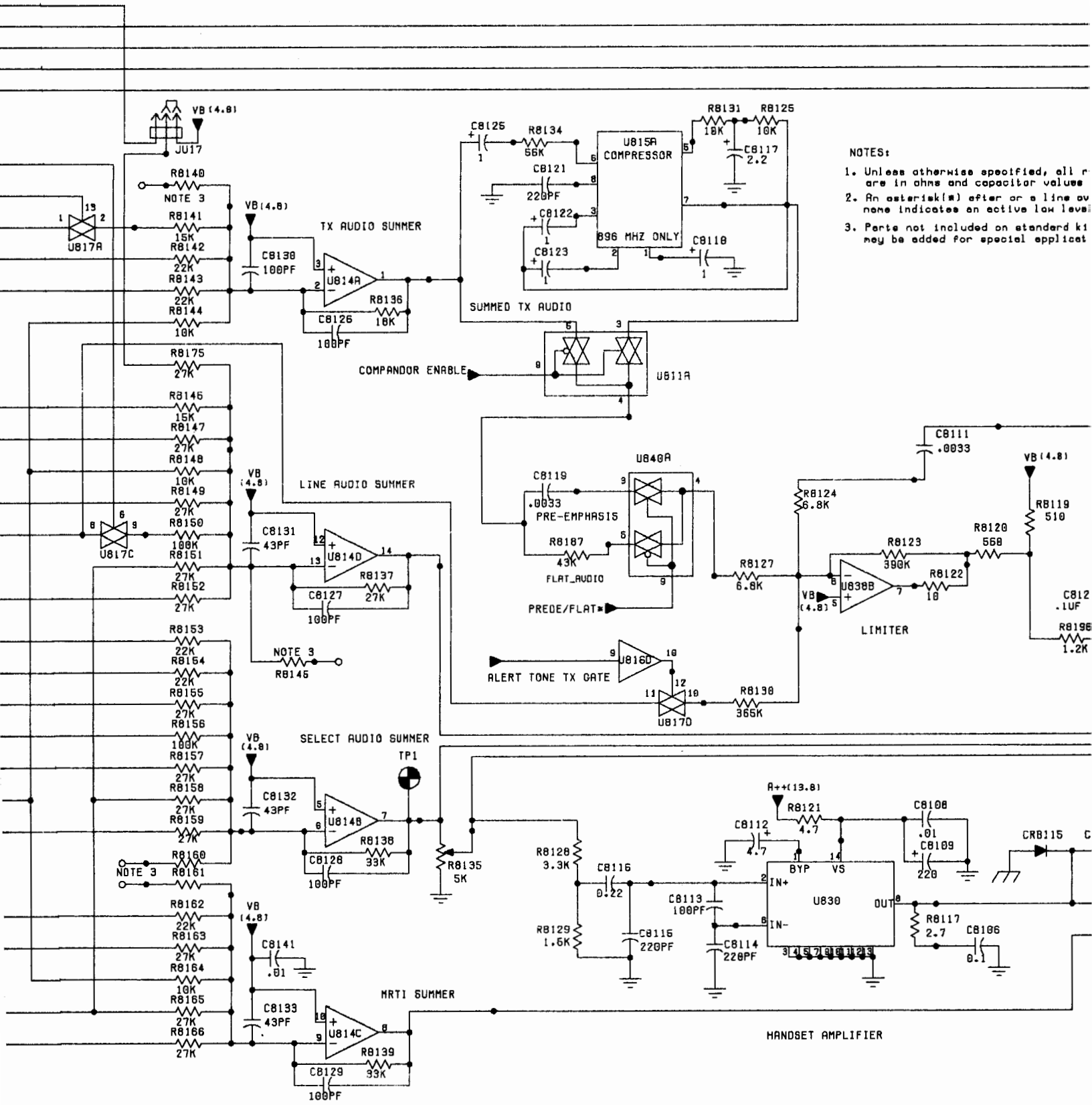
   8K SRAM : R802 out, R808 in
   32K SRAM : R802 in, R808 out


+5V
POWER U804
C802 0.1
R835 10K
R833 10K
R832 10K
R831 10K
BA0
BA1
BA2
BA3
BD0*
BD1*
BD2*
BD3*
DS*
J800
J803
J804
R845 120
L800 10UH
C801 270PF
CR803
R816 4.7K
DS*
R8345 100
R8348 100
R8347 100
HSR CLK
HSR SYN
HSR FROM TTRC
HSR TO SECURE
HSR OUT
HSR IN
JU1
JU2
C829 100PF
U818A
U813B
U816F
RX1 GATE*
LOCAL GATE*
TX GATE
MRTI GATE
REPEATER GATE
ALERT TONE TX GATE
ALERT TONE LINE GATE
OL5(0:6)
OL4(0:7)
SEGMENT dec*
SEGMENT a*
SEGMENT b*
SEGMENT e*
SEGMENT d*
SEGMENT f*
SEGMENT g*
SEGMENT c*
OL10(0:7)
ALERT TONE 0
ALERT TONE 1
ALERT TONE 2
ALERT TONE 3
PL/CT 0
PL/CT 1
PL/CT 2
PL/CT 3
OL14(0:7)
OL13(0:6)
OL19(0:6)
OL12(0:7)
OL11(0:2)
OL8(0:3)
R843 100
R840 100
R837 100
R844 100
R838 100
R841 100
R845 100
SD3
SD2
SD1
SD0
SA2
SA1
SA0
R800 150
R812 1.5K
Q817 NPNSOT
DS805 Q19A8LE
MRTI INHIBIT
J802
R807 6.8K
Q816 NPNSOT
R801 3.9K
R809 6.8K
Q814 NPNSOT
R803 3.9K
MRTI RX CARRIER
R810 6.8K
Q813 NPNSOT
R804 3.9K
MRTI AUX INDICATE
CR802
R824 1.8K
Q806 NPNSOT
R821 1.5K
R829 6.8K
Q807 NPNSOT
R827 3.9K
R828 22K
Q808 DARLSOT
R825 2.2K
R823 2.2K
R817 2.2K
CODED MOD LEVEL*
RX LEVEL*
MAX DEV LEVEL*
RCVR SQ LEVEL*
RPTR SQ LEVEL*
FF LEVEL*
CODED RX LEVEL*
LEVEL INC
J803
U839D
PREDE/FLAT*
RX1*/RX2
PL/DPL*
SQ ADAPT
LOOPBACK
VDD4
MODE
C804 0.1
C803 0.1
C825 0.1
C827 0.1
R842 10K
R839 10K
R836 10K
R834 10K
U813E
COMPANDOR ENABLE
SQUELCH EEPOT ENABLE*
PL/CT* SELECT
FF ENABLE*


R846
120
L800
10UH
C801
270PF
CR803
+5V
R815
4.7K
DS*
J808
J805
J804
R8345
100
R8348
100
R8347
100
HSR CLK
HSR SYN
HSR FROM TTRC
HSR TO SECURE
HSR OUT
HSR IN
J804
J803
JU1
JU2
C829
100PF
U816A
U816B
U816F
RX1 GATE*
LOCAL GATE*
TX GATE*
DL5(0:6)
MRTI GATE
REPEATER GATE
ALERT TONE TX GATE
ALERT TONE LINE GATE
ALERT TONE 0
ALERT TONE 1
ALERT TONE 2
ALERT TONE 3
PL/CT 0
PL/CT 1
PL/CT 2
PL/CT 3
DL6(0:7)
PA KEY
CR802
DS804
R818
120
+5V
PA KEY*
J801
R824
1.8K
Q806
NPN5OT
R821
1.5K
PA POWER CUTBACK*
R829
6.8K
Q807
NPN5OT
R827
3.9K
C808
.01
CR801
ANTENNA RELAY ENABLE*
R828
22K
Q808
DARL5OT
R819
10
R825
2.2K
Q809
NPN5OT
R822
100
TX STROBE
R815
10
R823
2.2K
Q810
NPN5OT
R820
100
RX1 STROBE
R813
10
R817
2.2K
Q811
NPN5OT
R814
100
JU13
RX2 STROBE
LEVEL U/D*
R800
150
R812
1.5K
Q817
NPN5OT
DS805
DI9A8LE
MRTI INHIBIT
R807
6.8K
Q816
NPN5OT
R801
3.9K
R809
6.8K
Q814
NPN5OT
R803
3.9K
MRTI RX CARRIER
R810
6.8K
Q813
NPN5OT
R804
3.9K
MRTI AUX INDICATE
EDE/FLAT*
PL/DPL*
SQ ADAPT
LOOPBACK
R863
150
R867
1.5K
Q801
NPN5OT
DS803
RX LOCK

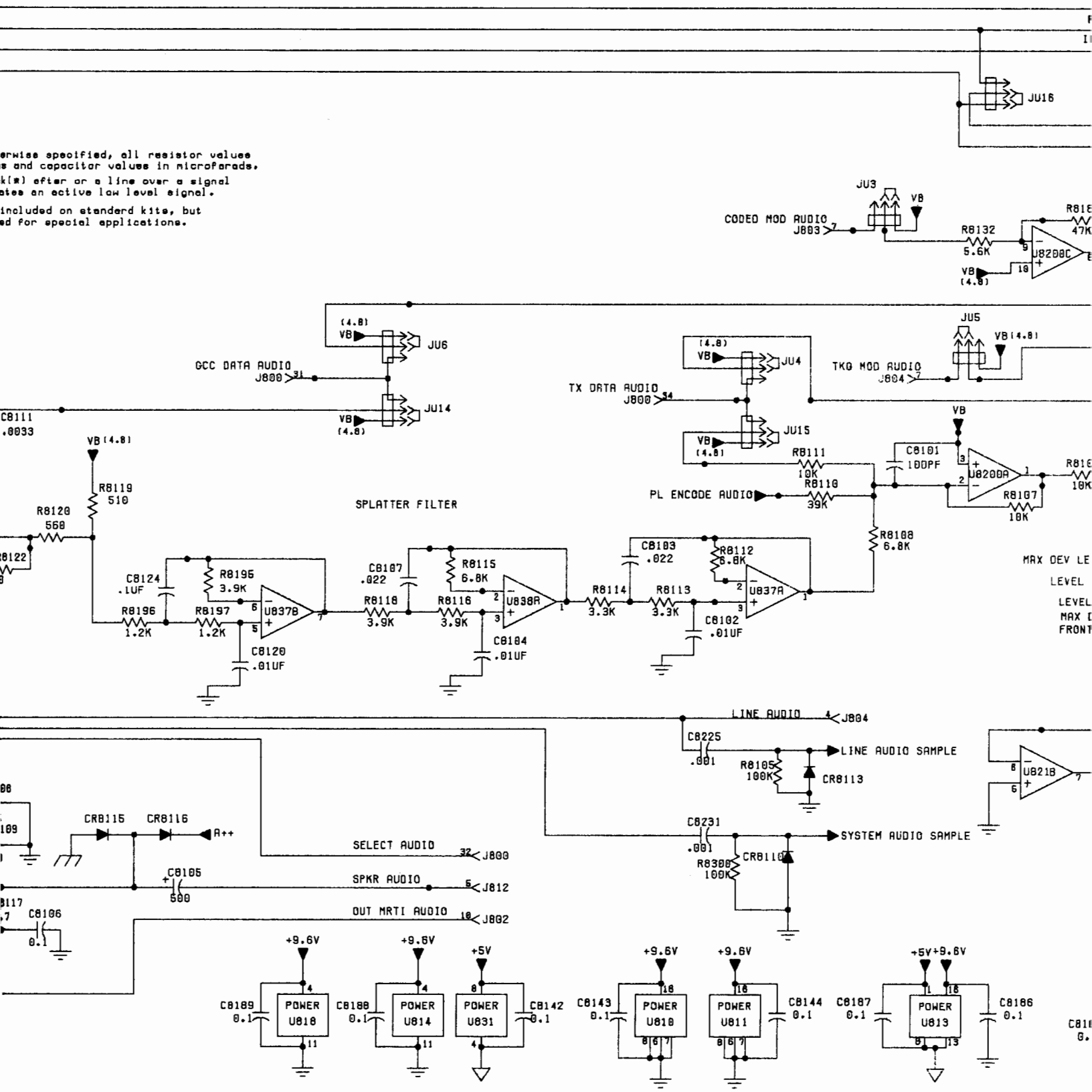

RAC_LN_AUD
J800 27
RAW TX AUDIO
J804 6
ALERT TONE LINE GATE
REPEATER GATE
MRTI GATE
U816B
VB (4.8)
R8173 100K
C8139 0.22
TX AUDIO
J804 5
U810A
TX AUDIO GATE
TX GATE*
R8174 100K
IN MRTI AUDIO
J802 8
R8344 560
C8140 0.22
U817B
MRTI GATE
U810B
R8169 100K
RX1 AUDIO
C8137 0.22
RX1 AUDIO GATE
RX1 GATE*
SECURE RX AUDIO
J803 4
JU10
R8172 100
C8136 10
+9.6V
R8170 560
CR8100
CR8101
TP8
R8167 100K
C8134 1
MIC AUDIO
J812 3
LOCAL AUDIO
J800 33
LOCAL GATE*
ALERT TONE AUDIO
R8171 200K
C8138 0.22
RX2 AUDIO
J800 35
R8168 200K
C8135 0.22
SECURE ALERT TONES
J803 34


U816B
U816E
U816C
U817A
VB (4.8)
U816A
TX AUDIO GATE
TX GATE*
R8174 100K
U817B
MRTI GATE
U810B
R8169 100K
C8137 0.22
RX1 AUDIO GATE
RX1 GATE*
CR8100
CR8101
+9.6V
TP8
C8134 1
R8167 100K
U810C
JU7
C8153 .01
LOCAL GATE*
LOCAL AUDIO GATE
R8171 200K
C8138 0.22
JU8
R8168 200K
C8135 0.22
JU9
U817C

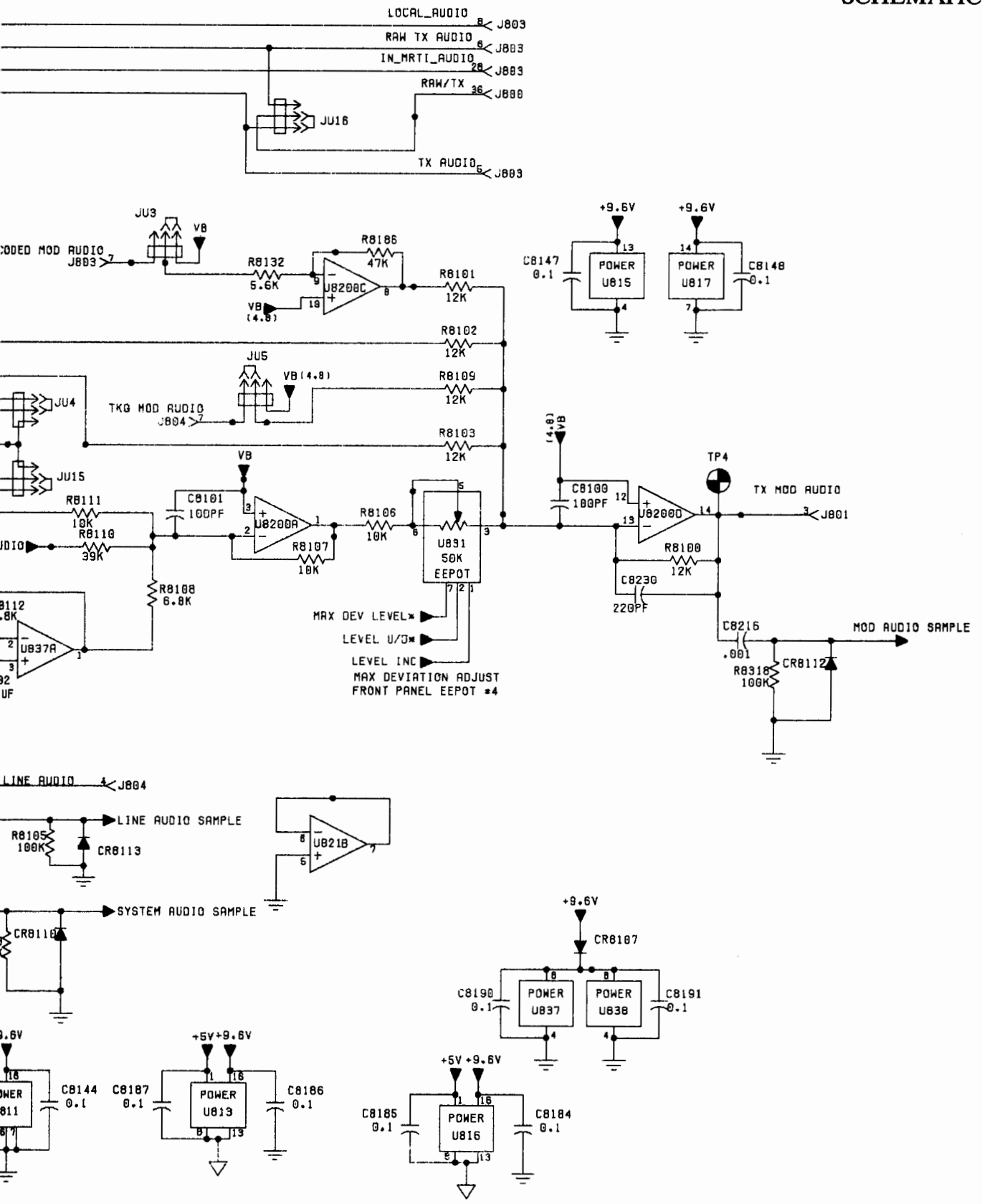

NOTES:
1. Unless otherwise specified, all r
are in ohms and capacitor values
2. An asterisk(*) after or a line ov
name indicates an active low level
3. Parts not included on standard ki
may be added for special applicat
VB (4.8)
JU17
R8140
NOTE 3
U817A
R8141
15K
R8142
22K
R8143
22K
R8144
10K
TX AUDIO SUMMER
C8130
100PF
U814A
R8136
10K
C8126
100PF
C8125
R8134
56K
C8121
220PF
C8122
C8123
U815A
COMPRESSOR
896 MHZ ONLY
R8131
10K
R8125
10K
C8117
2.2
C8118
SUMMED TX AUDIO
COMPANDOR ENABLE
U811A
R8175
27K
R8146
15K
R8147
27K
R8148
10K
R8149
27K
R8150
100K
R8151
27K
R8152
27K
U817C
LINE AUDIO SUMMER
C8131
43PF
U814D
R8137
27K
C8127
100PF
NOTE 3
R8145
U840A
C8119
.0033
PRE-EMPHASIS
R8187
43K
FLAT_AUDIO
PREDE/FLAT*
R8127
6.8K
R8124
6.8K
C8111
.0033
R8123
390K
R8120
560
R8119
510
U838B
R8122
10
LIMITER
C812
.1UF
R8196
1.2K
U816D
R8130
365K
ALERT TONE TX GATE
U816D
R8153
22K
R8154
22K
R8155
27K
R8156
100K
R8157
27K
R8158
27K
R8159
27K
R8160
NOTE 3
R8161
SELECT AUDIO SUMMER
TP1
C8132
43PF
U814B
R8138
33K
C8128
100PF
R8135
5K
R8128
3.3K
R8129
1.6K
C8116
0.22
C8116
220PF
A++(13.8)
R8121
4.7
C8112
4.7
C8108
.01
C8109
220
CRB115
C8113
100PF
C8114
220PF
U830
BYP
VS
IN+
IN-
OUT
R8117
2.7
C8106
0.1
HANDSET AMPLIFIER
R8162
22K
R8163
27K
R8164
10K
R8165
27K
R8166
27K
C8141
.01
C8133
43PF
U814C
R8139
33K
C8129
100PF
MRTI SUMMER

erwise specified, all resistor values
s and capacitor values in microfarads.
k(#) after or a line over a signal
ates an active low level signal.

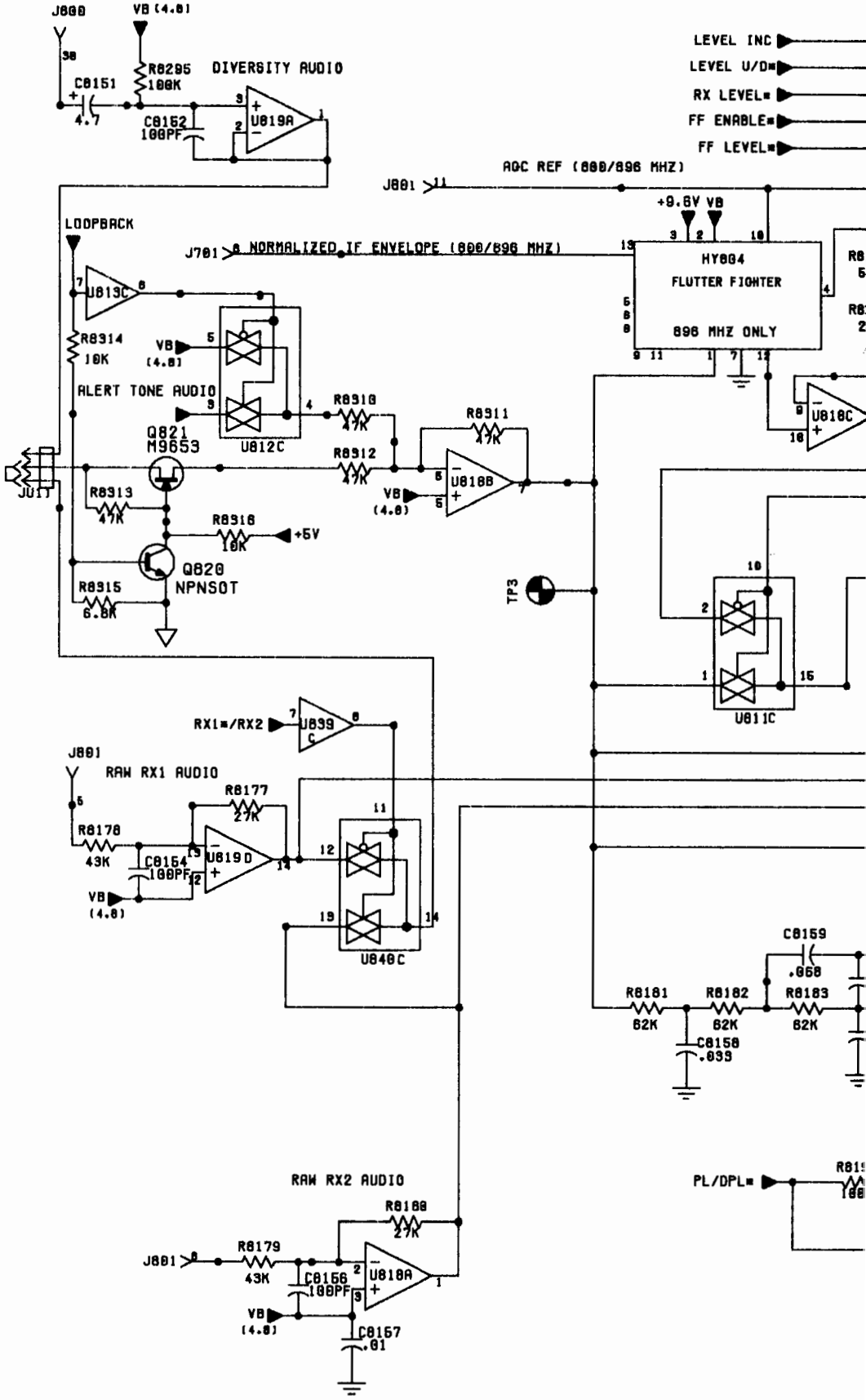
included on standard kits, but
ed for special applications.

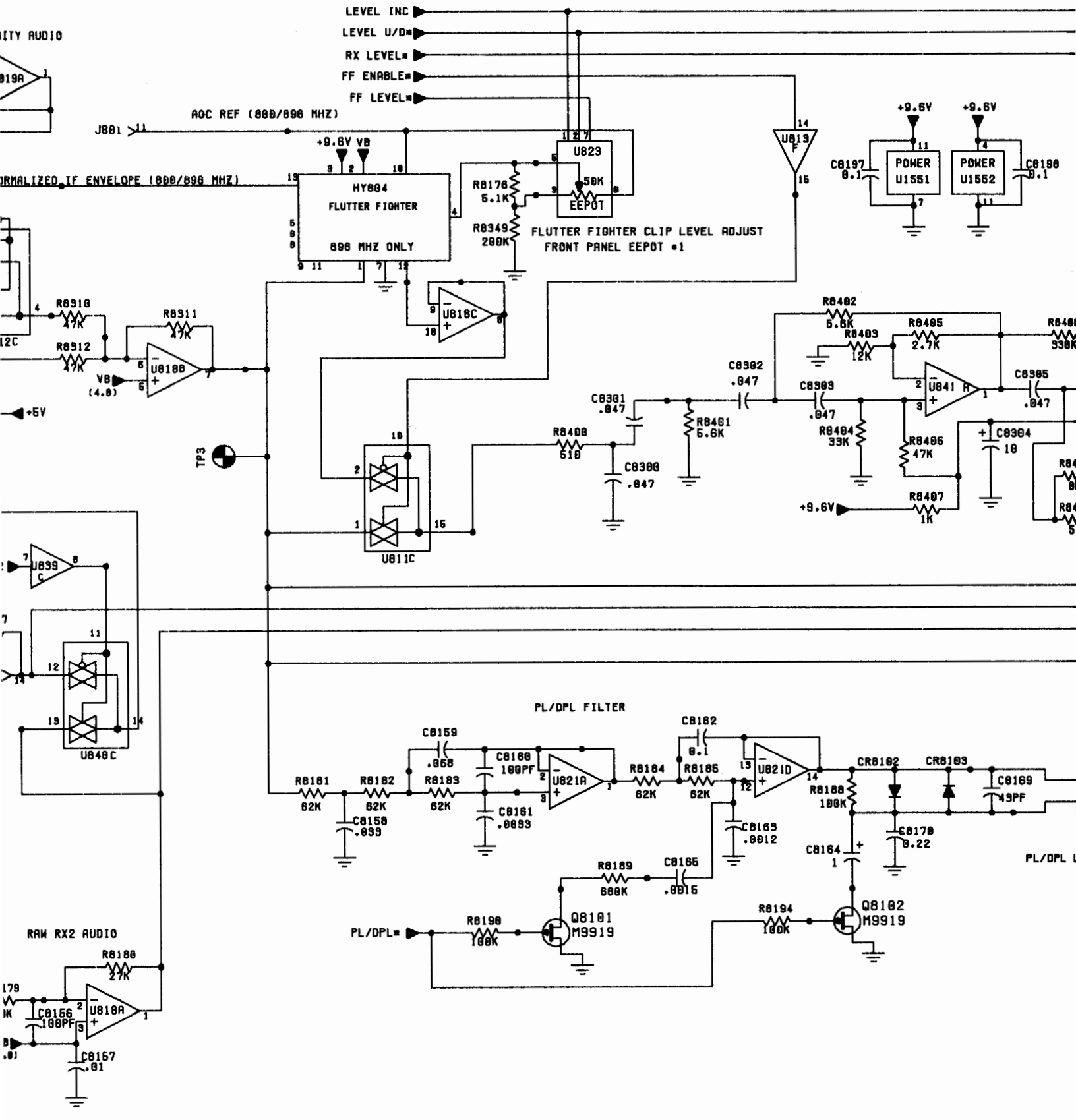


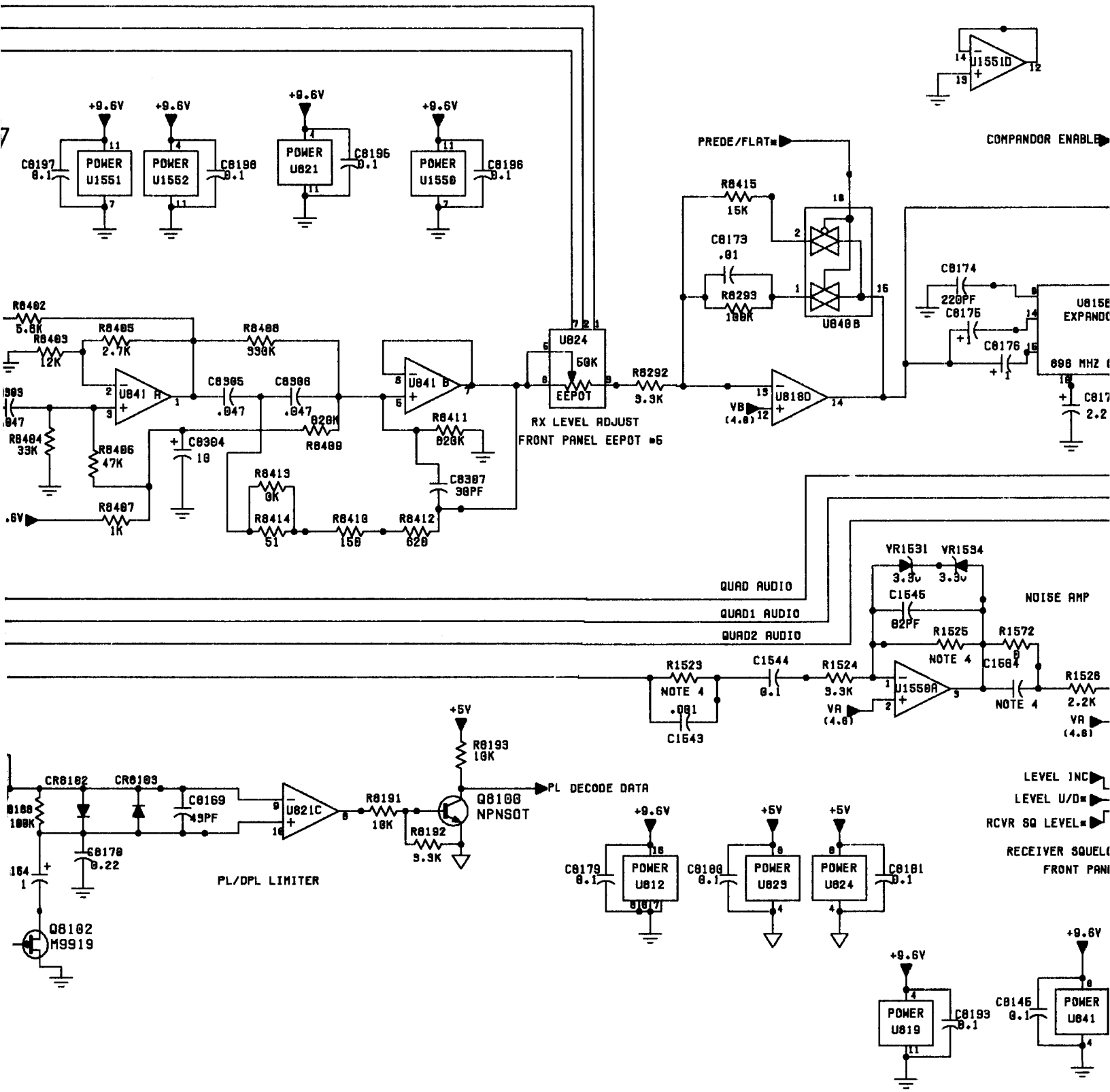
SECURE CAPABLE STATION CONTROL BOARD
SCHEMATIC DIAGRAM

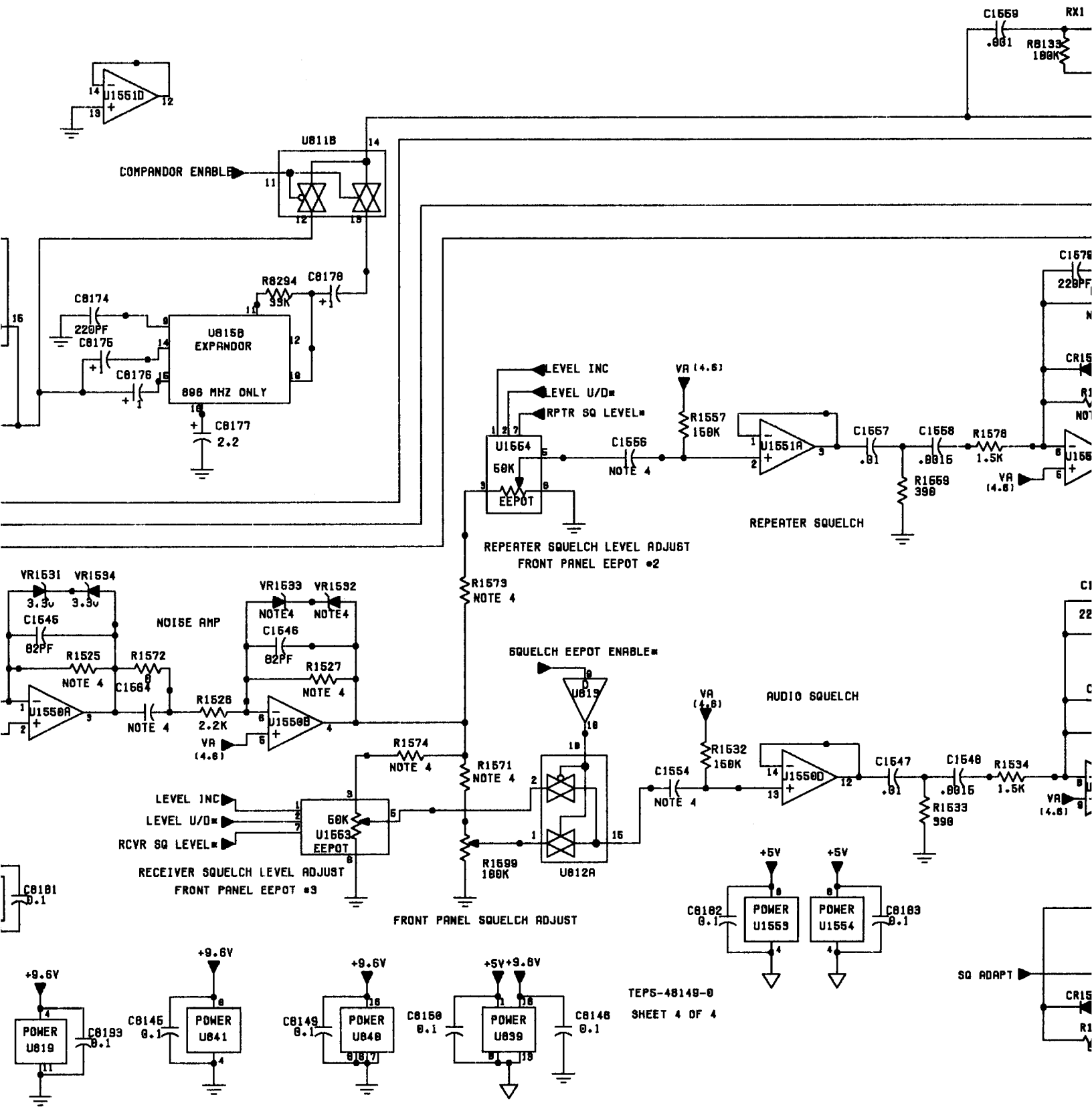


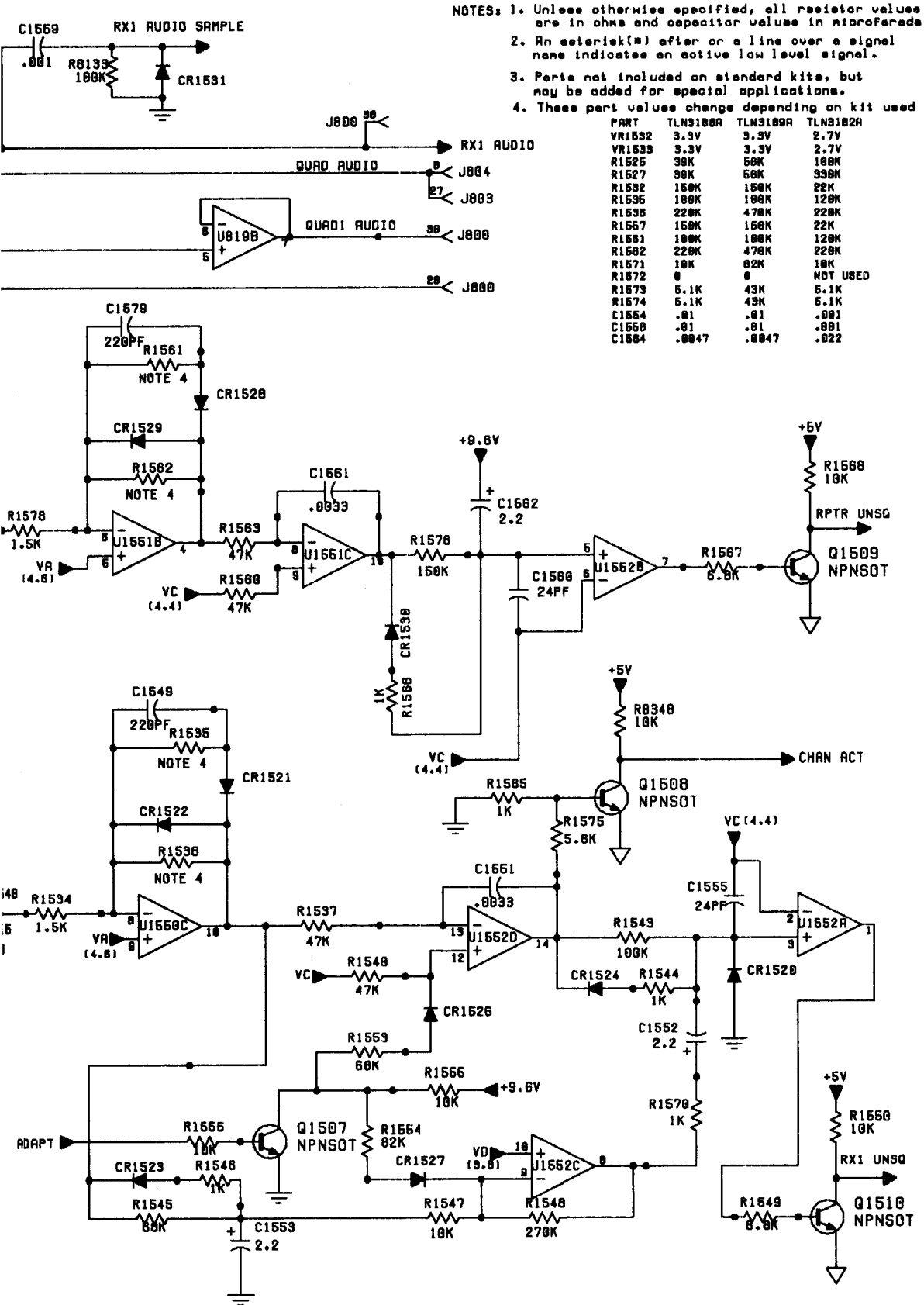
SECURE CAPABLE STATION CONTROL BOARD
SCHEMATIC DIAGRAM




LEVEL INC
LEVEL U/D
RX LEVEL
FF ENABLE
FF LEVEL
AGC REF (800/896 MHZ)
J801
+9.6V VB
HY804
FLUTTER FIGHTER
896 MHZ ONLY
U823
R8178 5.1K
50K
EEPOT
R8349 200K
FLUTTER FIGHTER CLIP LEVEL ADJUST
FRONT PANEL EEPOT #1
U819F
+9.6V
POWER U1551
POWER U1552
C8197 0.1
C8198 0.1
ORMALIZED IF ENVELOPE (800/896 MHZ)
R8310 47K
R8311 47K
R8312 47K
U818B
VB (4.8)
+5V
U818C
R8402 5.6K
R8403 12K
R8405 2.7K
U841 A
C8302 .047
C8303 .047
C8305 .047
C8301 .047
R8401 5.6K
R8404 33K
R8406 47K
C8304 10
R8408 510
C8300 .047
R8407 1K
TP3
U811C
U839 C
U840C
PL/DPL FILTER
C8159 .068
C8160 100PF
C8182 0.1
R8181 62K
R8182 62K
R8183 62K
C8158 .039
C8161 .0033
U821A
R8184 62K
R8185 62K
U821D
CR8182
CR8183
C8169 49PF
R8188 100K
C8163 .0012
C8170 0.22
C8164 1
R8189 680K
C8165 .0015
R8198 100K
Q8101 M9919
R8194 100K
Q8102 M9919
PL/DPL=
RAW RX2 AUDIO
R8180 27K
C8156 100PF
U818A
C8157 .01


+9.6V
C8197 0.1
POWER U1551
POWER U1552
C8198 0.1
POWER U821
C8195 0.1
POWER U1550
C8196 0.1
U1551D
PREDE/FLAT=
COMPANDOR ENABLE
R8415 15K
C8173 .01
R8293 100K
U840B
C8174 220PF
C8175
C8176
U815E EXPANDO
896 MHZ
R8402 5.6K
R8403 12K
R8405 2.7K
R8408 330K
U841 A
C8305 .047
C8306 .047
820K
R8409
C8304 10
R8406 47K
R8404 33K
U841 B
R8411 820K
C8307 30PF
R8413 0K
R8414 51
R8410 150
R8412 620
U824
50K
EEPOT
R8292 3.3K
U818D
VB (4.8)
RX LEVEL ADJUST
FRONT PANEL EEPOT =6
R8407 1K
QUAD AUDIO
QUAD1 AUDIO
QUAD2 AUDIO
VR1531 3.3v
VR1534 3.3v
C1545 82PF
NOISE AMP
R1525 NOTE 4
R1572 0
C1564 NOTE 4
R1523 NOTE 4
C1544 0.1
R1524 9.3K
U1550A
R1528 2.2K
VA (4.8)
.081
C1543
+5V
R8193 10K
CR8102
CR8103
C8169 49PF
U821C
R8191 10K
Q8100 NPNSOT
PL DECODE DATA
R8192 9.3K
C8178 0.22
PL/DPL LIMITER
Q8102 M9919
LEVEL INC
LEVEL U/D=
RCVR SQ LEVEL=
RECEIVER SQUELC
FRONT PANI
C8179 0.1
POWER U812
C8180 0.1
POWER U829
POWER U824
C8181 0.1
C8193 0.1
POWER U819
C8146 0.1
POWER U841


C1559
.001
RX1
R8133
100K
U1561D
U811B
COMPANDOR ENABLE
R8294
33K
C8178
C8174
220PF
C8175
C8176
U8158
EXPANDOR
800 MHZ ONLY
C8177
2.2
LEVEL INC
LEVEL U/D=
RPTR SQ LEVEL=
U1554
50K
EEPOT
C1556
NOTE 4
R1557
150K
VA (4.8)
U1551A
C1557
.01
C1558
.0015
R1578
1.5K
R1559
390
REPEATER SQUELCH
REPEATER SQUELCH LEVEL ADJUST
FRONT PANEL EEPOT #2
VR1531
VR1534
3.3v
3.3v
C1545
82PF
R1525
NOTE 4
R1572
0
C1564
NOTE 4
NOISE AMP
U1550A
R1526
2.2K
VR1533
VR1532
NOTE4
NOTE4
C1546
82PF
R1527
NOTE 4
U1550B
R1573
NOTE 4
SQUELCH EEPOT ENABLE=
U819
R1574
NOTE 4
R1571
NOTE 4
R1599
100K
U812A
LEVEL INC
LEVEL U/D=
RCVR SQ LEVEL=
50K
U1553
EEPOT
RECEIVER SQUELCH LEVEL ADJUST
FRONT PANEL EEPOT #3
FRONT PANEL SQUELCH ADJUST
C8181
0.1
C1554
NOTE 4
R1532
150K
U1550D
AUDIO SQUELCH
C1547
.01
C1548
.0015
R1534
1.5K
R1533
390
+5V
+5V
C8182
0.1
POWER
U1553
POWER
U1554
C8183
0.1
+9.6V
POWER
U819
C8193
0.1
+9.6V
C8145
0.1
POWER
U841
+9.6V
C8149
0.1
POWER
U848
+5V+9.6V
C8150
0.1
POWER
U839
C8146
0.1
TEP5-48149-0
SHEET 4 OF 4
SQ ADAPT


C1559
.001
RX1 AUDIO SAMPLE
R8133
100K
CR1531
J800
RX1 AUDIO
QUAD AUDIO
J804
J803
U819B
QUAD1 AUDIO
J800
J800
NOTES: 1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but may be added for special applications.
4. These part values change depending on kit used
PART TLN3188A TLN3189A TLN3182A
VR1532 3.3V 3.3V 2.7V
VR1533 3.3V 3.3V 2.7V
R1525 39K 68K 100K
R1527 39K 68K 330K
R1532 150K 150K 22K
R1535 100K 100K 120K
R1536 220K 470K 220K
R1557 150K 150K 22K
R1561 100K 100K 120K
R1562 220K 470K 220K
R1571 10K 82K 10K
R1572 0 0 NOT USED
R1573 5.1K 43K 5.1K
R1574 5.1K 43K 5.1K
C1554 .01 .01 .001
C1558 .01 .01 .001
C1564 .0047 .0047 .022
C1579
220PF
R1561
NOTE 4
CR1528
CR1529
R1562
NOTE 4
R1578
1.5K
U1551B
VA
(4.8)
R1563
47K
C1661
.0033
U1551C
VC
(4.4)
R1560
47K
+9.6V
C1662
2.2
R1578
150K
C1560
24PF
U1552B
R1567
6.8K
+5V
R1568
10K
RPTR UNSQ
Q1509
NPNSOT
CR1530
1K
R1566
C1549
220PF
R1535
NOTE 4
CR1521
CR1522
R1536
NOTE 4
R1534
1.5K
U1550C
VA
(4.8)
R1537
47K
C1551
.0033
U1552D
R1548
47K
VC
CR1526
R1559
68K
R1566
10K
+9.6V
+5V
R8348
10K
CHAN ACT
VC
(4.4)
R1565
1K
Q1508
NPNSOT
R1575
5.6K
VC(4.4)
C1555
24PF
U1552A
R1543
100K
CR1524
R1544
1K
CR1528
C1552
2.2
R1570
1K
ADAPT
R1556
10K
Q1507
NPNSOT
R1564
82K
CR1523
R1546
1K
R1545
68K
C1553
2.2
CR1527
VD
(9.6)
U1552C
R1547
10K
R1548
270K
+5V
R1550
10K
RX1 UNSQ
R1549
6.8K
Q1510
NPNSOT