MOTOROLA INC.
Communications
Sector

SECURE CAPABLE STATION CONTROL BOARD

MODELS TLN3043A
TLN3059A
TLN3090A

1. INTRODUCTION

1.1 OVERVIEW

This document describes the operation of the Secure capable Station Control Board (SSCB). The SSCB has been designed for use in the Digital MSF5000 repeater/base station. The kit number of the SSCB depends upon the frequency band of the station in which the SSCB is used :

TLN3043A - UHF
TLN3059A - VHF
TLN3090A - 800

The SSCB is housed in the control tray attached to the top of the RF tray. The SSCB is compatible with the Trunked Tone Remote Control (TTRC) board (TLN3114A, TLN3112A) as well as the optional secure module (TLN3045A). The SSCB also maintains compatibility with all existing optional expansion modules which can be housed in an expansion tray attached to the top of the control tray.

1.2 SSCB FUNCTIONS

The following list briefly outlines the functions of the SSCB. The specific circuit functionality is described in detail in the next section.

- Control frequency synthesizers in RF tray
  - Drive address and data for transmit and two receive synthesizers.
  - Drive Tx Strobe, Rx1 Strobe, and Rx2 Strobe
  - Drive front panel RX LOCK LED
- Process receiver audio
  - Quad Audio buffering (for 2 receivers and diversity audio)
  - Flutter Fighter (and clip level set)
  - PL high pass filter
  - Rx audio level adjustment
  - De-emphasise
  - Expansion
- Process transmit audio
  - Compression
  - Pre-emphasis
  - IDC limiting
  - Splatter filtering
  - Deviation level adjustment
- Amplify select audio for local handset
- Audio routing (gating and summing)
- Squelch
  - Audio and repeater carrier squelch detect (and threshold set)
  - PL and DPL coded squelch encoding (including reverse burst/turn off code)
  - PL and DPL coded squelch detect
  - Connect/disconnect tone decode (incl. Mute monitoring for holdoff function)
  - Connect/disconnect tone encode
- Alarms/auto-station ID
- Data Communications (read/write)
  - IPCB
  - MUXbus (drive data strobe and address)
  - High Speed Ring (drive HSR CLK and SYN)
  - Discrete logic lines to rest of SSCB/station
- Interface to local user
  - Read front panel switches and control jack inputs
  - Write to front panel LEDs and 7-segment display

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- DC power
  - Convert station power (A+/+9.6V) to logic supply
  - Generate DC levels for audio biasing and s squelch reference
  - Grounding for control shelf
- PTT Control
  - PTT priorities
  - PTT time out
  - Repeater drop out delay
- Transmitter Control
  - Generate PA key up signal
  - Switch antenna relay
  - Monitor PA status/drive PA power cutback/PA alarm
- MRTI Interface
  - Control inputs/outputs
  - Audio inputs/outputs
- TSTAT
  - Monitor forward and reflected power levels
  - Generate TSTAT signal
- MCU system operation
  - Address decoding
  - Bus demultiplexing
- Reset (expansion, delayed, COP, low voltage, power up)
- Other
  - Self Diagnostics (loopback, A/D audio monitor ing)

2. FUNCTIONAL DESCRIPTION

2.1 DC-DC CONVERTER

2.1.1 OPERATION

The DC-DC converter section is used to generate all DC voltages required by the SSCB and the other control tray boards. The schematic diagram for this section is shown on the right half of Sheet 1. This section uses two DC voltage inputs provided by the station. A+ + is the auxiliary +13.8V voltage generated in the main station power supply and routed to the SSCB via the interconnect board to J701. This voltage is fused (3A) and filtered to form the A+ voltage used by the control tray boards. Unfused A+ + is also routed directly to the expansion connector J800 for use by expansion tray modules. +9.6V is generated by a voltage regulator mounted in the RF tray and is routed to the SSCB via the interconnect board to J801. This voltage is also filtered to form the +9.6V voltage used by the control tray boards. The SSCB takes station ground from J701 (GND B), and at this connector the three control tray grounds are formed: logic ground, audio ground, and static ground.

The primary function of the DC-DC converter section is to use the A+ and +9.6V voltages to generate the +5V voltage used in the logic circuitry of the control tray boards. This is achieved using a pulse-width-modulated (PWM) switching converter. The converter's reference voltage, VE, is generated from +9.6V current through 5.1V zener diode VR701. VE is used in the shutdown comparator U700A to turn off the switcher if the A+ voltage is too low. When not shutdown, U700D forms a free-running oscillator at a switching frequency of approximately 22 kHz. U700C compares the output of the converter with the reference VE and modulates the pulse width (or duty cycle) of the power switch formed by Q700 and Q701. The output of the power switch is filtered and held by C701. Toroid L700 is used to maintain charge on C701 while the power switch is off, providing higher efficiency. Q702 forms a current limiting circuit which will reduce the output voltage level when current through the parallel combination of R716-R719 exceeds approximately 2.5 amps. Over-voltage protection is provided by Q704 which will trigger and blow the A+ fuse when the converter output exceeds the 6V required to breakdown zener diode VR700. U700B is used to reset the SSCB and is described in the logic section of this description.

Bias voltages for other circuits on the SSCB are also generated in this section. VB is generated by dividing and buffering +9.6V using U819C. VB is approximately 4.7V and is used as the primary bias voltage in all the audio processing circuits on the SSCB. VA (4.6V), VC (4.4V), and VD (3.8V) are generated using simple voltage dividers sourced by +9.6V and are used as reference voltages in the squelch section of the SSCB. As well as providing the switcher reference, the VE voltage is also used as the reference high voltage VRH for the A/D converter channels on microprocessor U800.

2.1.2 TROUBLESHOOTING

When the DC-DC converter is functioning normally, TP6 should read +5V DC. If the +5V level signal cannot be verified, check the A+ (~13.8V with 3A fuse) and +9.6V input voltages. JU12 can be removed to disconnect the load from the switcher output. If the +5V level is cor-

rect with JU12 out, but falls low with JU12 in, there is most likely a short somewhere in the SSCB +5V load. If the 3A fuse F700 blows when power is applied to the board, then check power switch Q701 and crowbar switch Q704. If these simple checks fail to resolve the problem, then refer to the DC-DC converter troubleshooting chart in the service manual.

2.2 AUDIO PROCESSING SECTION

The Audio Processing section consists of three parts : receive audio processing, transmit audio processing, and audio routing.

2.2.1 RECEIVE AUDIO PROCESSING SECTION

2.2.1.1 OPERATION

The schematic diagram for this section is on the top left part of Sheet 4. The input to the receive audio processing section is baseband audio which is demodulated from the RF signal by the receiver in the RF tray. This audio is labeled RAW RX1 AUDIO on the schematic and originates at J801. U819D buffers this audio signal to form QUAD1 AUDIO (quadrature). In standard one-receiver stations, QUAD1 AUDIO is routed through JU11 to the loopback switch, Q821. This switch normally passes the audio through to TP3 via U818B to generate QUAD AUDIO. Q821 will mute receiver audio during audio loopback diagnostics. If JU11 is moved to the alternate position, DIVERSITY AUDIO from an optional "diversity" board via U819A is routed to QUAD AUDIO at TP3. U818A buffers RAW RX2 AUDIO from an optional second receiver to form QUAD2 AUDIO. The QUAD1 AUDIO and QUAD2 AUDIO signals are both routed to the expansion connector for processing by optional expansion modules. QUAD AUDIO is routed to the remainder of the receive audio processing section, as well as to the squelch and tone detector circuits. QUAD AUDIO is also routed to the optional secure transparent module for processing in a coded voice system and to the TTRC board for processing in a trunked system.

The QUAD AUDIO signal is the input to the "flutter-fighter" hybrid HY804. This hybrid circuit is used in stations where multi-path fading can cause degradation of the receiver audio (particularly in 900 MHz stations with 12.5 kHz channel spacings). The hybrid circuit attenuates the receiver audio during fading to attempt to cancel the audio pops commonly heard in these systems. The flutter-fighter circuit will also attenuate weak, noisy signals to further improve audio quality. The hybrid uses two signals from the IF circuitry in the RF tray, NORMALIZED IF ENVELOPE via J701 and AGC REF via J801. The flutter-fighter "clip level" controls the operating point of the hybrid circuit and can be adjusted using digital pot U823. The hybrid circuit output is buffered by U818C and sent to audio gate U811C which controls whether QUAD AUDIO or flutter-fighter output is sent to the next audio stage.

The output of U811C is routed to the PL (for Private Line) filter hybrid HY803. This filter is used to attenuate low frequency receive audio components due to PL/DPL/connect tone coded squelch signals. These frequency components are not desired components of the receiver audio response. The filter gain is about 0.6dB at 1kHz and is flat from 400Hz to 3 kHz. The filter will attenuate signals up to 400Hz and is required to attenuate all signals under 200Hz by -30dB in order to insure that PL residual hum is more than 30dB below rated receiver audio output.

The output of the PL high pass filter is sent to the level adjust and de-emphasis circuit. The gain of this circuit is controlled by varying the series input resistance of the inverting amplifier U818D using digital pot U824. This is done to adjust the level of receiver audio distributed throughout the station. The frequency response of this circuit provides the -6 dB/octave de-emphasis required in the FM system. This de-emphasis of receive audio cancels out the symmetrical pre-emphasis performed at the transmitting end of the RF link.

The output of the de-emphasis circuit drives the expandor. This circuit comprises the receive portion of the "companding" operation performed on the system audio in stations with 12.5 kHz channel spacing. This is done to increase the effective dynamic audio range for narrow band systems. The expanding done on the receive audio cancels out the compression performed at the transmitting end of the RF link. The expansion ratio is 1:2; that is, every 1 dB of change in input level produces 2 dB of change in expanded output level. The output of the expandor is sent to audio gate U811B to control whether the audio is expanded or not. The input level at which gate U811B output is the same with or without expansion is called the "crossover point" and corresponds to the audio level present with approximately 40% receiver deviation. The output of gate U811B is the output of the receive audio processing section labeled RX1 AUDIO and is sent to the audio routing section to be distributed throughout the station. RX1 AUDIO is also sent to the expansion connector J800 for processing by optional expansion tray modules.

2.2.1.2 TROUBLESHOOTING

When a strong RF signal is applied to the receiver, the baseband FM modulation should be present on RX1 AUDIO (U811-14). For an RF signal with 60% deviation of a 1kHz tone, the RX1 AUDIO level should be about 350 mVrms . If this audio is not present, then this section could be the problem. Check the +9.6V supply on TP5 and the VB bias level on U819-12. If the RX1 AUDIO signal is not found, make sure JU11 is in the proper position. Also check the signal at TP3 QUAD AUDIO (~300 mV rms), which is not filtered or gated. If audio is present on TP3 but not on U811-14, then try adjusting the Rx level

digital pot U824. If these attempts fail, one of the circuit blocks in the receive audio processing section may have malfunctioned. Each of these blocks may be checked on a input to output basis and fixed if found faulty: PL filter hybrid HY803, digital pot U824, expandor U815, flutter-fighter hybrid HY804, audio gate U811, or op-amps U818,U819.

2.2.2 TRANSMIT AUDIO PROCESSING SECTION

2.2.2.1 OPERATION

The schematic diagram of the transmit audio processing section is shown on the top right part of Sheet 3. The output of this section is TX MOD AUDIO and is sent to the RF FM modulator for transmission over the air. This section has several inputs originating from the SSCB audio routing circuitry.

The output of the TX Audio summing amp, SUMMED TX AUDIO, drives the compressor, U815A. This circuit comprises the transmit portion of the "companding" operation performed on the system audio in stations with 12.5 kHz channel spacing. This is done to increase the effective dynamic audio range for narrow band systems. The compressing done on the transmit audio cancels out the expansion performed at the receiving end of the RF link. The compression ratio is 2:1; that is, every 2 dB of change in input level produces 1 dB of change in compressed output level. The output of the compressor is sent to audio gate U811A to control whether the audio is compressed or not. The input level at which gate U811A output is the same with or without compression is called the "crossover point" and corresponds to the audio level required to yield approximately 40% transmitter deviation.

The output of gate U811A is sent to the pre-emphasis and limiter circuit. The gain of inverting amplifier U838B is designed to limit the level of audio sent to the modulator to ensure that maximum transmitter deviation is not exceeded (with low audio inputs, the limiter acts as a simple linear gain stage). When the station is properly adjusted, this circuit begins to limit with an audio input level yielding more than 60% maximum system transmitter deviation. Diode CR8107 is used to provide greater limiter symmetry since the op-amp will drive closer to the positive supply rail than it can to ground. The frequency response of this circuit provides the 6 dB/octave pre-emphasis required in the FM system. This pre-emphasis of transmit audio is canceled out by a symmetrical de-emphasis circuit at the receiving end of the RF link.

The output of the limiter is sent to the splatter filter. This is a five-pole low pass filter formed by U838A and U837A. This low pass filter is required to prevent high frequency content above 3 kHz from causing the transmitted RF signal to "splatter" into adjacent channels. This filter also contains a series resonant notch at approximately 16 kHz in order to allow the filter to meet all relevant FCC splatter specs.

The output of the splatter filter along with other audio signals is sent to the maximum deviation adjust circuit. The gain of this circuit is adjusted by controlling the series input resistance of inverting amplifier U8200D using digital pot U831. This level must be set to compensate for circuit parameter and transmit VCO sensitivity variations to yield the station's maximum transmit deviation with a large audio input level.

2.2.2.2 TROUBLESHOOTING

When a large audio signal is applied to the microphone input with a local PTT, the limited filtered audio signal should be present on TX MOD AUDIO at TP4. If this audio is not present, then this section could be the problem. Check the +9.6V supply on TP5 and the VB bias level on U838-5. If the TX MOD AUDIO signal is not found, make sure the mic audio is present on the Tx audio summing amp output U814-1. If this signal is absent, check the Audio Routing Section described in the next paragraph. Also check the signal on U838-7, which should be in full limit to the op-amp supply rails. Trace this signal through the splatter filter (U838-1, U837-1, U837-7). The splatter filter output should be similar in amplitude to the limiter output but with the square wave harmonics attenuated. If audio is present on U837-7 but not on TP4, then try adjusting the Max Deviation level digital pot U831. If these attempts fail, one of the circuit blocks in the transmit audio processing section may have malfunctioned. Each of these blocks may be checked on a input to output basis and fixed if found faulty.

2.2.3 AUDIO ROUTING SECTION

2.2.3.1 OPERATION

The audio routing section is shown mainly on the left half of schematic Sheet 3. Its primary function is to properly distribute audio signals from all sources to all destinations connected to the SSCB. The audio routing section operates on the following audio inputs and outputs:

Table 1. Audio Inputs Description

INPUTS	DESCRIPTION
TX AUDIO	Notch filtered audio from TTRC wireline
IN MRTI AUDIO	Audio from MRTI phone patch
LOCAL AUDIO	General purpose audio to/from expansion modules (also common with MIC AUDIO signal)

Table 1. Audio Inputs Description (Continued)	
MIC AUDIO	Audio from local user microphone
RX1 AUDIO	Audio from receive audio processing section
ALERT TONE AUDIO	Audio from alert tone encoder on SSCB
SECURE RX AUDIO	Audio from optional secure board for speaker/ wireline
RX2 AUDIO	Processed audio from optional 2nd rcvr board
CODED MOD AUDIO	Audio from optional secure board to be transmitted
TKG MOD AUDIO	TDATA/failsoft from TTRC to be transmitted
SEC ALERT TONES	Tones from option secure board (encode/decode only)
TX DATA AUDIO	General purpose data from expansion modules
GCC DATA AUDIO	1200 or 4800 baud data from optional GCC
RAW TX AUDIO	Unfiltered audio from TTRC wireline
PL ENCODE AUDIO	Audio from PL/connect tone encoder on SSCB

Table 2. Audio Outputs Description	
OUTPUTS	**DESCRIPTION**
SUMMED TX AUDIO	Audio to transmit audio processing section
LINE AUDIO	Audio to TTRC wireline
SELECT AUDIO	Volume adjusted audio to expansion modules (especially DMP speaker)
OUT MRTI AUDIO	Audio to MRTI phone patch
SPKR AUDIO	Amplified audio to local user speaker
TX AUDIO	Wireline audio to secure board for encryption and to expansion modules
RAW TX AUDIO	Unfiltered wireline audio to optional secure transparent board
LOCAL AUDIO	Local audio to optional secure board for encryption
IN MRTI AUDIO	Audio from MRTI phone patch to secure board for encryption

Some audio inputs are enabled using audio gates in response to various PTT and squelch conditions (TX AUDIO–U810A, IN MRTI AUDIO–U817B, LOCAL/MIC AUDIO–U810C, RX1 AUDIO–U810B, and ALERT TONE AUDIO–U817C/U817D). Some other audio inputs are enabled using 3 pin jumpers (see jumper table). TX DATA AUDIO can be summed into the SSCB transmit path before or after the maximum deviation adjust circuit (JU4). GCC DATA AUDIO can be routed through the pre-emphasis/splatter filter path for 1200 baud data or after the maximum deviation adjust for 4800 baud data (JU6).

The first four audio signals in the output list are generated with summing amplifiers (SUMMED TX AUDIO–U814A, LINE AUDIO–U814D, SELECT AUDIO–U814B, and OUT MRTI AUDIO–U814C). Refer to the block diagram and schematic for inputs to these summing amps. SPKR AUDIO is generated by routing the select audio through front panel VOLUME pot R8135 and then through 1/2W audio amplifier U830. The remaining four signals in the output list are actually input signals that must be routed to other sections of the station. One audio signal which is not an input or an output of this section is the repeater audio which comes from the RX1 audio gate and is routed to the transmit audio processing section under the control of audio gate U817A.

2.2.3.2 TROUBLESHOOTING

The routing performed in this section depends on the configuration of the SSCB in the station. This configuration is determined by two factors: code plug programming and jumper settings. If the audio routing section is not performing as expected, most likely one of these two factors is the problem. Refer to the jumper table to determine proper jumper settings, and refer to the software description for proper code plug programming. If these two items are verified to be correct, and audio routing problems still exist, then the circuitry in this section should be checked.

Check the +9.6V supply on TP5 and the VB bias level on U810–1. If an audio gate will not operate as expected, check the audio gate control input. A high level (~ +9.6V) on the control input of "T-gates" U810, U811, U812 allows audio to pass through the positive gate (no circle) and shut off the signal going into the negative gate (with circle). A low level on the control input will allow audio to pass through the negative gate while muting the positive gate. For audio gate U817, a high level (~ +9.6V) on the control input allows audio to pass, whereas a low

level will mute the audio. If the control input is correct, but the gate does not respond correctly, the audio gate is probably faulty. If the control input is not as expected, check the level shifter U813 or U816. These ICs shift the 0–5V ASIC control output to the 0–9.6V levels required by the audio gates. A low voltage on the input of the level shifter should produce a low level on the output, whereas a +5V level on the input should produce a +9.6V level on the output. If this operation cannot be verified, the level shifter IC is probably faulty. If audio routing problems still exist, and if all audio gates operate correctly with the code plug and jumpers properly configured, then check quad summing amp U814. If audio is present on the resistor inputs but not on the outputs, and the +9.6V and VB levels are correct, then this part is probably faulty.

2.3 SQUELCH CIRCUITRY

The squelch detection circuitry on the SSCB is used to detect the signal strength of the incoming receiver audio. The QUAD AUDIO signal from TP3 is routed to both receiver and repeater squelch detectors. These detectors set control lines to the logic section for use in keyup and gating arbitration. For information on PL/DPL coded squelch operation, refer to the logic section of this description.

The input to amplifier U1550A is a noise pre-emphasis network that boosts the noise content of the input signals above 5 kHz. For squelch processing, the first amplifier/limiter is driven into limit to prevent audio signals from squelching the receiver. Amplifier/limiter U1550B again amplifies the noise signal and re-limits audio signals to provide further protection against audio signals squelching the receiver. The output signal of U1550B is then used to drive both the receiver and repeater squelch circuits.

2.3.1 OPERATION

2.3.1.1 RECEIVER SQUELCH CIRCUITRY

The amplified noise output signal level is normally adjusted by digital pot U1553. This adjustment controls the signal strength required to break receiver squelch. Front panel squelch adjust knob R1599 can be used instead to adjust this level depending on the setting of audio gate U812A. This adjusted audio is routed to the input network of the detector which provides further attenuation of audio and any harmonics generated by audio limiting at the output of U1550B. Noise detector U1550C is a half-wave rectifier amplifier that produces negative-going spikes at its output. The average dc value of these spikes is proportional to the received signal strength. With a weak noisy signal, many negative-going spikes will be produced, resulting in a low average dc output voltage. A strong, quieted signal will have a higher average dc output voltage.

The receiver squelch switching circuit operates in two modes. With a receive signal just above the opening sensitivity, squelch closing is slow (approximately 150 ms), which produces the long squelch tail heard at the end of a received message. The long squelch tail is present to prevent the received message from being chopped during a weak fluttering signal. With a strong signal (approximately 10 dB above opening sensitivity), a squelch closing occurs immediately after the end of a received signal. This prevents the squelch tail from being heard.

Active integrator U1552D provides squelch opening and slow squelch closing. Comparator U1552A compares the detector's average dc output voltage with a reference voltage, VC (4.4V), to determine the level for squelch opening and closing. Fast squelch closing is provided by U1552C. A strong signal charges C1553 through R1545, driving U1552C-8 low. At the end of a strong signal, any noise spikes from the detector are captured by CR1523. This immediately discharges C1553 and forces U1552C-8 high. Then, capacitor C1552 forces U1552A to close the squelch. The SQ ADAPT signal from the logic section will also force squelch closing. This is used during channel change to eliminate squelch tail noise.

The receiver squelch detector produces two outputs to the logic section. The RX1 UNSQ signal is high when a strong signal has broken squelch and is low when a weak signal fails to break squelch. The CHANNEL ACTIVITY signal has the same logic as RX1 UNSQ but always responds quickly with no squelch tail. This is used by the processor in channel-scan applications.

2.3.1.2 REPEATER SQUELCH CIRCUITRY

The repeater squelch detector circuit is very similar to the receiver squelch detector. The output of noise amp U1550B is adjusted by digital pot U1554 and sent to the repeater squelch detector. This adjustment controls the signal strength required to break repeater squelch. After more filtering, this signal is sent to noise detector U1551B which produces negative-going noise spikes similar to those described in the receiver squelch section. Integrator U1551C provides squelch opening and slow squelch closing (squelch closing time is typically 200 ms). Comparator U1552B compares the noise detector output's average DC voltage with a reference voltage, VC (4.4V), to determine the squelch opening and closing switch point. The repeater squelch detector produces the RPTR UNSQ signal which connects to the logic section.

2.3.2 TROUBLESHOOTING

When operating properly, the squelch detectors should indicate squelch conditions with an RF signal below adjusted threshold. The detectors should unsquelch when the signal strength is above the set level. If the squelch circuit does not operate properly, try adjusting the digital pots in the receiver and repeater squelch detection circuits. An easy way to quickly check the operation of the

squelch circuitry is to use the ACC DIS switch on the front panel to enable the use of the front panel Squelch control. If the RF input is disconnected from the station, a noisy signal should appear on TP3 QUAD AUDIO. When the Squelch control is fully CW, this noisy input should cause the receiver squelch detector to squelch the receive audio. When the Squelch control is full CCW, the detector will not squelch the receiver, and the noisy signal will pass through to the speaker. If the receive channel has PL/DPL/connect tone enabled, the PL DIS switch must also be used to hear the signal at the speaker. If these simple checks do not resolve the squelch problem, refer to the squelch troubleshooting chart in the manual.

2.4 LOGIC HARDWARE SECTION

The logic hardware description can be broken down into five broad parts: microprocessor core, data communications circuitry, tone encoders/decoders, general I/O and reset circuitry.

Many of the functions carried out by the logic section are accomplished using an Application Specific Integrated Circuit (ASIC). The SSCB uses two of these custom ASICs specifically designed for this product. The ASIC can operate in one of two modes depending on the state of the MODE pin (pin 18). U801 operates in the standard mode (with MODE pulled high) and serves as a specialized microprocessor support chip with additional I/O and data communication features. U802 operates in the I/O mode (with MODE pulled low) and serves as an addressable collection of input buffers and output latches.

2.4.1 MICROPROCESSOR CORE

The schematic diagram of the microprocessor core is located on Sheet 2. Its function is to run the software program in order to control the station. Most of the core functions are carried out using five integrated circuits.

2.4.1.1 MICROCONTROLLER

U800 is a Motorola 8-bit HCMOS single chip microcontroller. During program execution it generates an 8-bit multiplexed data/low-order address bus, AD(0:7), as well as a high-order address bus, A(8:15). U800 controls the direction and timing of bus transfers with three signals common to 6800 family devices. U800-5 is the E signal, and it functions as the primary clock for all bus transfers. U800 generates the E clock by dividing the external crystal frequency by four (Thus E = 7.9488MHz/4 = 1.9872MHz). U800 controls the direction of bus transfers using the R/W* signal on U800-6. This signal is high when U801 needs to read data off the bus and is low when U801 is writing data to the bus. In order to allow an external latch (in ASIC U801) to demultiplex the data/low-order address bus, U800 also generates the AS (Address Strobe) signal on U800-4. Thus when AS is high AD(0:7) contains the low order address bus A(0:7), but when AS is low AD(0:7) contains the data bus D(0:7).

2.4.1.2 MEMORY

U800 runs the software program contained in 32K CMOS EPROM U803 (27C256). U800 also contains 512 bytes of internal EEPROM Code Plug for station parameter storage. During program execution, U800 can access 192 bytes of internal RAM as well as the external 8K x 8 SRAM U804. U808 is an optional 2K x 8 serial EEPROM which can be added if additional "code plug" space is required.

2.4.1.3 STANDARD MODE ASIC

Many of the "glue" chips commonly required to complete a microprocessor system are replaced in integrated form by standard mode ASIC U801. Since U800 operates with a multiplexed data/low-order address bus AD(0:7), U801 contains an address latch to demultiplex this bus. Thus the low-order address bus A(0:7) is an output of U801.

U801 also contains all the circuitry required to perform full address decoding using the 16-bit expanded address bus for the entire 64K memory space. Thus all required chip select signals are also outputs of U801 (refer to software description for memory allocation) :

- MEM OE* drives the output enable pins on EPROM U803 and SRAM U804. This signal is active low during every read cycle (E and R/W* both high).
- ROM CE* drives the chip enable pin on the EPROM U803. This signal is active low whenever the address bus indicates an access in the EPROM memory space.
- RAM CE* signal drives the chip enable pin on the external SRAM U804. This signal is active low whenever the address bus indicates an access in the external SRAM memory space.
- RAM WE* pin drives the write enable pin on SRAM U804. This signal is active low during normal write cycles (E high and R/W* low)

2.4.2 DATA COMMUNICATIONS CIRCUITRY

The SSCB logic section has three primary media with which to communicate with other modules in the station: The IPCB, the MUXbus, and the high speed ring.

2.4.2.1 IPCB

The IPCB (Inter-Processor Communication Bus) is a low speed (1200 baud) serial link shared among all the control tray boards as well as optional expansion modules. It is also accessible via front panel control jack J812. On the SSCB, U800 interfaces to the IPCB using the SCI (Serial Communications Interface). This link can carry status and control information between modules. The IPCB line is

pulled up on the SSCB and is normally high in the idle state until a module begins to write information onto it (0–5V logic levels). The SCI on U801 has both a receive and a transmit port, and these are buffered by Q802–Q805 and wired together before being routed as the IPCB line to the external connectors.

2.4.2.2 MUXbus

The MUXbus is a time–multiplexed address and data bus capable of carrying 64 bits of control and status information between station modules. The SSCB serves as the MUXbus master and all the circuitry to control the MUXbus is contained in ASIC U801. The MUXbus consists of 16 4–bit data nibbles for a total of 64 bits. The address bits BA0–BA3 are periodically incremented modulo–16 by U801 to access each 4–bit data nibble in a consecutive fashion. The 4–bit data nibble is represented by MUXbus data bits BD0*–BD3*. U801 also asserts the MUXIRQ* signal at every address increment to signal U800 to service the MUXbus data. All multiplexing timing is done using the DS* (Data Strobe) signal generated inside ASIC U801. U801 generates the data strobe signal by internally dividing the E clock signal by 640 (Thus DS* = 1.9872 MHz/640 = 3105 Hz). A resonant echo suppressor circuit comprised of L800, C801 and CR800 serves to cancel echoes caused by transmission line effects on the data strobe line.

2.4.2.3 HIGH SPEED RING

The high speed ring (HSR) is a unique multiprocessor communication mechanism. All the circuitry to implement the HSR is contained in standard mode ASIC U801. The HSR continually circulates a 40 bit packet between all modules in the ring. 16 of these bits can be written to by the SSCB. 16 bits are reserved for writes by the TTRC, and 8 bits are reserved for writes by the optional secure module. All modules can read any of the bits in the 40 bit packet. The SSCB operates as the HSR master; that is, U801 drives the HSR CLK and HSR SYN signals to synchronize all packet transfers. The HSR CLK signal is square wave which defines the bit times within the 40–bit packet. The frequency of the HSR clock is programmable but is normally set to E/2 (0.9936 MHz). The HSR SYN signal is asserted for one bit time at the start of each 40–bit packet in order to properly synchronize all modules on the ring. The SSCB sends its HSR OUT data from U801 to the TTRC on J804. Data from the TTRC's HSR is received on J804 and passed directly to the optional secure module on J803. Data from the secure module's HSR is taken from J803 and sent back to U801 as HSR IN to complete the ring. In a station where either the TTRC or secure module is not present, JU1 and/or JU2 can be set to maintain HSR continuity.

2.4.3 GENERAL INPUT/OUTPUT

The SSCB logic section has a great deal of input/output (I/O) capability to control station functions and monitor station status. The I/O section also allows a local user to change the state of the station and observe station status conditions.

2.4.3.1 INPUT BUFFERS

The logic section monitors discrete status lines from other circuits on the SSCB and other modules in the station using input buffers contained in I/O ASIC U802. There are three input buffers: IB9, IB10, and IB11 (shown on the left side of schematic Sheet 2). Status information from the synthesizers and power control circuits in the RF tray enter the SSCB on J801 and are routed to IB9 on U801 for access by the SSCB software. The PA FULL*, PA ON*, and TX LOCK* lines are also used to pull down front panel LEDs when active. The front panel RX LOCK LED is driven by the SSCB based on the station configuration and the status of the RX LOCK* and RX2 LOCK* input lines. Inputs from the local user come in from the front panel and are routed to IB10. IB11 is used for logic inputs from the MRTI phone patch via J802, from the power supply via J701 and from the SSCB squelch section. Notice that bit 7 of IB9, and bits 5 and 6 of IB10 are spare input buffer lines reserved for future use.

2.4.3.2 OUTPUT LATCHES

ASICs U801 and U802 both contain general purpose addressable output latches used for station control functions. The following list briefly describes the function of these output latches (refer to the right half of schematic Sheet 2):

- OL4 : 7 bit latch from U801. Used to control 7–segment display switches.
- OL5 : 7 bit latch from U801. Used to control gates in audio routing section.
- OL6 : 8 bit latch from U801. Bits 0–5 used to control transmitter and synthesizer functions in the RF tray. Bit 6 used to select direction of digital pot increments. Bit 7 used to drive front panel RX LOCK LED.
- o OL8 : 4 bit open–drain latch from U802. Bits 0 and 3 used to enable Hear Clear audio functions (companding/flutter–fighting). Bit 1 used to select PL/connect tone encoder output destination. Bit 2 used to enable front panel squelch control pot.
- OL10 : 8 bit latch from U802. Used for 2 four bit tone encoders described in the next section
- OL11 : 3 bit latch from U802. Reserved for future use.
- OL12 : 8 bit latch from U802. Used for digital pot selection and increment.
- OL13 : 7 bit latch from U802. Used to load synthesizer address and data to PLL TX and RX synthesizer circuits in RF tray.

- OL14 : 8 bit latch from U802. Bit 0 used to control front panel DISABLE LED. Bits 1,3,4 used to control MRTI phone patch. Bit 6 used to reset squelch tail control circuit during channel change. Bit 7 used to enable audio loopback diagnostics.

2.4.3.3 STATUS DISPLAY

Another important part of the logic I/O is the three digit 7-segment display interface which drives the TRN7008A Display Board inserted on the SSCB. This display is used in normal operation to show channel and mode information (key number information can be shown in optional encode/decode stations). This circuitry is shown on the left half of Sheet 1. This circuit operates as a multiplexed display driver which will alternately switch the three digits on and off at a 40 Hz rate. The segment switches are PNP transistors Q8201–Q8207 controlled by active low outputs from OL4 on U801. The digit switches are darlington NPN transistors Q8208–Q8210 controlled by active high output pins on U800. In addition to the segment and digit controls, an active low control line, labeled DISPLAY ON*, is provided which will turn on all segments in all 3 digits. The DISPLAY ON* signal is driven by an output pin from U800 which powers up low from reset. Therefore, all segments of all 3 digits are illuminated via Q8211 and Q8212 on the display board when the SSCB goes through reset.

2.4.3.4 WATTMETER INTERFACE

The wattmeter interface circuitry comprised of U806C and U806D (shown in the center of schematic Sheet 1) serves to isolate the wattmeter grounds on the phono plug shields from the SSCB ground as well as to provide a linear translation of the wattmeter input range to the A/D dynamic range. The outputs of this circuit are routed to two of the A/D channels on U800 (ports 6 and 7). The FWD PWR signal is proportional to the power level transmitted from the PA output. The SSCB can generate an alarm if this signal is below a preset minimum level during transmitter keyup. The RFL PWR signal is proportional to the reflected power level sensed by the wattmeter due to incorrect matching, etc. The SSCB can generate an alarm if this signal is above a preset maximum limit.

2.4.3.5 AUDIO DIAGNOSTICS

The other six 8-bit A/D channels on the microprocessor are connected to various points in the SSCB audio paths for use in automated diagnostics. A/D ports 0 and 1 on U800 are connected to two particularly important points in the audio path via peak detector interfaces. The TX MOD AUDIO signal from TP4 uses the peak detector formed by U8200A. The system audio signal from TP1 uses the peak detector formed by U821B (both shown on the right side of schematic Sheet 3). These peak detector circuits function by maintaining charge on an output capacitor creating a DC value proportional to the AC signal. The gain of these stages is designed to translate the expected audio range into the 0–5V A/D converter range. This is done to allow for more efficient software monitoring of these DC levels. The four remaining ports are connected to other points in the audio path and are capacitively coupled to the A/D channels. This requires a more complex software algorithm to determine the peak of these time varying waveforms.

2.4.4 TONE PROCESSING

2.4.4.1 TONE ENCODING

Two 4-bit encoders are included on the SSCB. They are driven by 8-bit latch OL10 from I/O ASIC U802. Bits 0–3 of OL10 are used to encode general purpose alert tones. These include station alarms, automatic station ID, and other optional features. The alert tones generally go up to about 1600Hz. This encoder drives a digital to analog converter (D/A) which uses a common R–2R ladder approach shown on the top center of Sheet 1. The output of the R–2R D/A converter is filtered by three pole low pass filter U806A. This filtering is done to reduce the harmonic noise caused by the limited encoder sample rate. The output of this filter is labeled ALERT TONE AUDIO and is sent to the audio routing section to be distributed throughout the SSCB.

The function of bits 4–7 of OL10 depend on the type of system in which the SSCB is operating. For a conventional station with coded squelch, this encoder is used to generate transmit PL tones or DPL code which is sent to the modulator. The encoder will also append a reverse burst sequence for PL coding or a turn off code for DPL. This is done to reduce squelch tail noise at the receiver. For a secure trunked system, this encoder encodes connect tone/disconnect tone and routes the encoder output via U8200B to the TTRC. The PL/connect tones generally go up to about 200Hz. This encoder also drives a digital to analog converter (D/A) which uses the same R–2R ladder approach as the alert tone encoder. The output of the R–2R D/A converter is filtered by three pole low pass filter U806B. This filtering is done to reduce the harmonic noise caused by the limited encoder sample rate. Audio gate U812B is used to control the destination of this encoder output.

2.4.4.2 TONE DECODING

Complementary to the tone encoding functions on the SSCB are the tone decoding capabilities. The SSCB will detect incoming PL tones or DPL codewords for a conventional coded squelch system, and it will detect incoming connect/disconnect tones in a trunked system. When present these tones/codewords are part of the receiver modulation and hence appear on the QUAD AUDIO signal. This signal is fed into a five pole low pass filter shown on the bottom of schematic Sheet 4. This filter is comprised of U821A and U821D and is designed to attenuate

all signals higher than the highest PL/DPL/connect tone frequencies required for decoding. The output of this filter is sent to the PL limiter U821C. The output of the limiter is level shifted by Q8100 to a 0–5V level and labeled PL DECODE DATA. This signal is routed to a special timer within microprocessor U800 called an "input capture". The input capture is a software programmable timer which is sensitive to transitions on the input pin. The software program can observe the timing of these transitions to determine a PL/DPL or connect/disconnect tone detect.

One special feature of the SSCB is "smart connect tone decode" capability. To implement this feature, the SSCB monitors the MUTE line from the TTRC. If the proper pulse is detected on the MUTE line (U800–34), the SSCB will temporarily remove the requirement for a connect tone detect. This function is used in some trunking systems to decrease overall system radio access time.

2.4.5 RESET CIRCUITRY

The power up reset circuitry is shown on the bottom of schematic Sheet 1. A block diagram of the reset circuitry is shown in Figure 1. Upon power up, C724 is discharged, causing a high voltage on comparator U700B–2 to turn on reset driver Q706 and activate the RESET* signal. As this capacitor is allowed to charge, U700B–2 will go low, turning off the reset driver Q706 and deactivating RESET*. This time constant is approximately 600 ms in duration, and thus the RESET* will be low for 600 ms after the 5V converter begins normal operation. Two other inputs to this circuit can cause C724 to discharge, resulting in a SSCB RESET*. When the A+ input voltage drops too low, shutdown comparator U700A–1 will go low, discharging C724 through CR708 causing a RESET*. Also, the front panel TEST switch, when depressed, will cause C724 to discharge through CR707, again causing a RESET*.

To prevent erroneous writes to U800 internal EEPROM during power up, power down or low voltage conditions, it is critical to activate RESET* whenever the +5V converter output drops too low. This is accomplished using low voltage reset generator Q705 shown on the top right of schematic Sheet 1. This PNP transistor is normally on, pulling up the RESET* line through R701 to +5V. When the +5V line drops too low, Q705 will turn off and provide a passive pulldown on the RESET* line through R700. This threshold occurs when the +5V line drops below approximately +3.5V.

U800 also contains a Computer Operating Properly (COP) timer which will generate a reset if the COP timer is not periodically serviced by the software routine. This is to ensure that the SSCB will restart execution if the program looses proper sequence. The COP circuit will generate a short RESET* pulse (~2 E cycles) which will force it to restart at the address indicated by the RESET vector.

The SSCB also contains a circuit which will inhibit some critical functions while the SSCB software performs self-diagnostics. This is achieved using the delayed reset generator circuit U807 shown on the bottom left of schematic Sheet 2. U807 is a 555 timer which will trigger the DELAYED RESET line high when the RESET* input goes low. Once the RESET* line is deactivated, Q800 will turn off, allowing the timer to discharge for a time constant defined by C822 and R888 (approx. 300 ms) before deactivating the DELAYED RESET line. The DELAYED RESET line is an input to ASIC U801 and a high level on it will inhibit functions such as PA keyup and MUXbus writes.

DELAYED RESET is inverted by Q822 to form EXPANSION RESET* which will hold other control tray boards and expansion modules in reset during SSCB self-diagnostics. The microprocessor can also activate EXPANSION RESET* during normal program execution by turning on Q823 with a general purpose output pin.

2.4.6 LOGIC HARDWARE TROUBLESHOOTING

The SSCB software is capable of generating several error codes on the front panel seven segment display. Refer to the SSCB software description section for a list of these diagnostic error codes.

If the SSCB logic section is suspect, check the +5V pins on each of the logic devices U800–U804 and U807. Next, look at the RESET* line on TP10. This line should be high with no pulses on it. Also look at the DELAYED RESET line, which should be low with no pulses on it. If the reset lines are not as expected, check to see that U800–U804 are properly seated in their sockets (especially 28-pin DIP U803). Also verify that EPROM U803 is programmed with the correct version software for this SSCB (U803 must be compatible with EEPROM codeplug internal to U800). Also check to see that the A(0:7) demultiplexed bus is being generated on U801 (pins 66–73). If A(0:7) is not found, then ASIC U801 is probably faulty. If ASIC U801 and EPROM U803 seem OK, and the RESET* line is high, check microprocessor U800. A properly functioning U800 will drive the E line (U800–5) with a 1.9872 MHz square wave. If all these chips are properly functioning, check ASIC U802 for data bus inputs as well as correct output latch levels.

If an error code indicates a problem with the HSR, verify that JU1 and JU2 are in the correct position. Verify that HSR CLK = E/2 frequency square wave and that HSR SYN is high every 40 HSR CLK cycles. If these signals look correct but HSR problems still exist, remove the modules from J804 and/or J803 and place JU1/JU2 in the HSR loopback position (JU1 alternate, JU2 normal position). If the error code persists with all other modules disconnected and the HSR looped back by JU1/JU2, then U801 is probably faulty.

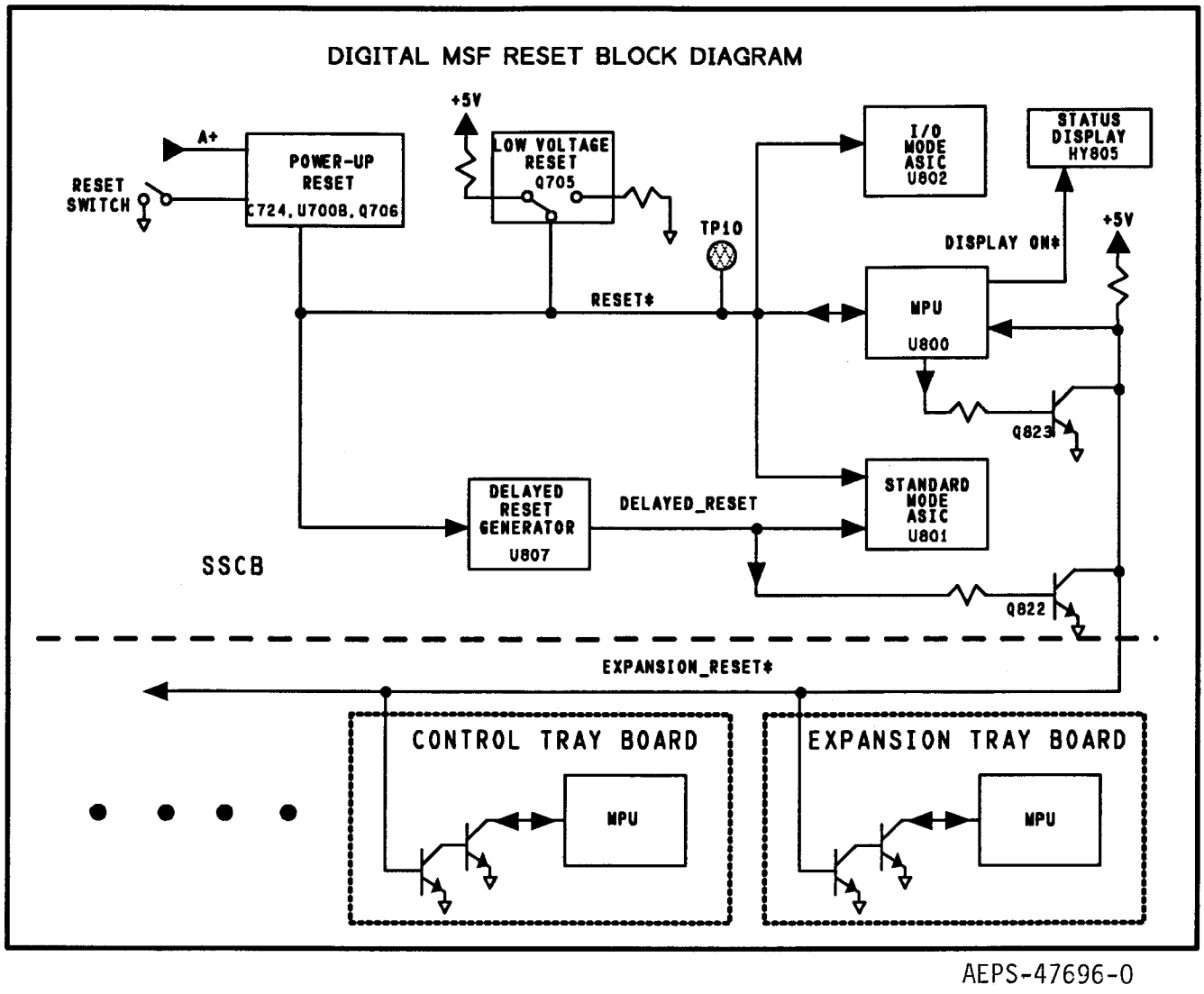


Figure 1. Reset Block Diagram

If problems are encountered with the MUXbus, verify that DS* = 3105 Hz square wave and that the address lines are being driven. For proper operation, the address nibble BA0–BA3 should be incremented modulo-16. This means that the BA0 line (which toggles at DS*/2 rate = 1553 Hz) should toggle twice as fast as BA1 (DS*/4 = 776 Hz), which is twice as fast as BA2 (DS*/8 = 388 Hz), which is twice as fast as BA3 (DS*/16 = 194 Hz). To verify proper MUXbus data generation, the SSCB can be forced to write to the MUXbus BD0*–BD3* bits. When a MUXbus data bit is set at only one MUXbus address, the signal on the specific MUXbus data pin should be a short 0V pulse from the 5V level repeating at a frequency of DS*/16 = 194 Hz. The following chart indicates one way to force the SSCB to drive a MUXbus data bit at only one address: If these signals cannot be verified, then U801 ASIC is probably faulty.

Table 3. MUXBUS Addressing

SIGNAL	ACTION
BD0* (U801-38)	depress XMIT switch
BD1* (U801-39)	depress XMIT switch
BD2* (U801-40)	ground TP9 (LOC PTT)
BD3* (U801-41)	set to CH1-using ACC DIS, SELECT/CHANGE switch

Troubleshooting of the tone encoders/decoders and wattmeter buffers can be accomplished using procedures similar to those suggested in the audio sections. Circuit blocks can be analyzed on an input to output basis and fixed if found to be faulty. When a PL signal is present on the

receive audio, the PL DECODE DATA (U800-32) signal should be a 0-5V square wave of the same frequency. An easy way to verify the wattmeter buffer operation is to monitor the buffer outputs (FWD PWR U806-8 and RFL PWR U806-14). The DC levels on these outputs should respond to front panel Po power adjustments while the transmitter is keyed. The tone encoders can be checked by looking at the output of the D/A filters. When an alarm condition is present, an alert tone sine wave burst should be visible at U818-1. Alarm tones can be generated by setting DMP bits at MUXbus address 12. When PL/DPL/ connect tones are being generated, a sine wave should be visible at U8200-1. DPL code 031 can be generated by keying the station with a LOC PTT while set to channel 1, mode 1.

2.5 SOFTWARE DESCRIPTION

When the station powers-up or is reset, the Station Control board firmware begins execution at the location contained in its "RESET" vector. This location is the beginning of the Station Control board firmware's main background routine. The main background routine is basically an endless loop (the "background") which calls all of the non-interrupt-driven routines. Before entering the background loop, a startup diagnostics module, "sscb_reset_diags.asm", is called which, as the name implies, performs diagnostic tests of the Station Control board. Note that the three-digit, seven-segment LED "Status" display will activate all segments and digits immediately upon station power-up and will stay on until the display-driving circuitry has been verified, providing an indication that the Station Control board has begun performing diagnostics.

The "sscb_reset_diags.asm" routine mainly performs functionality tests of the Station Control Board's hardware circuitry. Before starting the diagnostic tests, however, this routine initializes some microprocessor registers. These registers determine the microprocessor's Computer Operating Properly (COP) watchdog time-out time and set up the Serial Communications Interface (SCI) to communicate at the same baud rate and message protocol as the other boards on the Inter-Processor Communications Bus (IPCB). Also, a flag bypassing service of the board's EEPROM is set at this time.

After initialization of the microprocessor, an output pin is activated to keep the Expansion Reset line activated (otherwise, on-board circuitry, which activated Expansion Reset immediately upon Station reset, would release that line after 200 milliseconds or so), thereby holding any and all remote boards in reset. At this point, the Station Control board diagnostics begin. These tests can yield a number of error conditions, so, in order for the operator to know which diagnostic test failed, the errors are displayed by either flashing the entire Station Control board's "Status" display or by formatting an error code for display within the "Status" window. Two types of error classes exist: fatal and non-fatal. Fatal errors are severe enough to prevent proper operation of the Station Control board, and they will cause the Station Control board to reset. Non-fatal errors, on the other hand, are just warnings and do not prevent operation of the Station Control board, and they do not cause the Station Control board to reset. Failure of some of the initial diagnostics tests, described below, require that flashing of the entire "Status" display, as opposed to an error code within the "Status" window, be used for error indication. The "flashing" must be used because, at this point, the display-driving circuitry, IRQ-interrupts, and external RAM have not been verified. The display-driving circuitry and IRQ interrupts must be operating properly because they are required for displaying error codes within the "Status" window; the external RAM is needed to hold the error codes for display.

All failures which flash the entire "Status" display are fatal errors. These errors cause the "sscb_reset_diags.asm" routine to call an error handler routine with a fixed number. This error handler routine flashes the "Status" display for that fixed number of times and then waits, not servicing the COP timer. Since the COP timer is not serviced, it will eventually time-out and the Station Control board will reset. Failures which display error codes within the front panel display, on the other hand, may be fatal or non-fatal errors. In this case, when an error is detected, "sscb_reset_diags.asm" calls a different error handler routine which writes a value, called an error code, to the front-panel "Status" window. If the error code is fatal, the Station Control firmware will display the error code for five seconds and then stop servicing its COP timer. When the COP timer expires, the Station Control Board will reset and the Expansion Reset line will activate and reset any board connected to it. If the error code is non-fatal, the Station Control firmware displays the error for two seconds and continues. Resets do not occur for non-fatal errors.

In the case of a fatal error left uncorrected, the test which caused the fatal error will fail again, the same error will be displayed and the firmware will reset again. This sequence will continue until the failure is corrected.

"sscb_reset_diags.asm" checks two major sections of the Station Control board: the digital hardware and the audio hardware. "Internal" digital diagnostic tests are performed first, followed by "external" digital diagnostic tests, followed by audio diagnostic tests. All tests are performed after every Station Control board reset. "Internal" digital diagnostic tests refer to tests which verify operation of the Station Control board's digital circuitry as stand-alone hardware. "External" digital diagnostic tests, on the other hand, verify operation of the Station Control board's digital circuitry as part of the overall Station Control Tray. Finally, the audio diagnostic tests verify operation of the Station Control board's audio circuitry.

The first "internal" digital diagnostic test ensures that the segment-select lines of the "Status" display and the internal "IRQ" signal are working properly; if they are not, "sscb_reset_diags.asm" calls the Status-display-flashing

errpr-handler routine with instructions to flash the entire display two times (the Station Control board will reset after those two flashes).

The next "internal" digital diagnostic test ensures that each RAM byte in the external RAM will toggle high and low. After each RAM byte is checked, it is cleared so that all RAM bytes are initially zero. If any external RAM byte fails this test, "sscb_reset_diags.asm" calls the display-flashing error handler routine which uses all segments of the "Status" window as an error indicator. The entire display flashes four times as a result of this error and, as described above, the Station Control board resets because this error handler does not return and does not service the COP.

The next test verifies that the IRQ (Interrupt Request) is working. The IRQ interrupt is the result of 640 microprocessor "E-cycles" having been clocked by the MUXbus-driving portion of the standard ASIC. This interrupt will occur every 320.061 usec (640 cycles at 1,987,200 cycles per second). It serves not only to signal the Station Control board that new MUXbus data is ready to be read, but also updates the Station Contol Software System Timer and drives the multiplexing of the front-panel display. If this interrupt test fails, "sscb_reset_diags.asm" calls the display-flashing error handler routine, causing the entire display to flash two times. If this test passes, the front-panel display, which contains all eights (8.8.8.) up to this point, is now blanked.

The next test ensures that each RAM byte internal to the microprocessor will toggle high and low. After each RAM byte is checked, it is cleared so that all RAM bytes are initially zeros. If any byte fails to pass this test, "sscb_reset_diags.asm" writes a fatal error code to the front-panel "Status" window. Note that for this test and all following tests, "sscb_reset_diags.asm" can put error codes into the "Status" window because the display-driving portions of the board have passed their tests.

The next section of the "sscb_reset_diags.asm" routine checks to see how the microprocessor is configured, i.e. checks what is contained in its CONFIG register. If the CONFIG register is not set up as desired, a check is made to determine if the CONFIG register can be corrected without erasing it. If so, "sscb_reset_diags.asm" makes the correction and writes a fatal error code to the "Status" window. If the CONFIG register must be erased in order to correct it, "sscb_reset_diags.asm" erases the CONFIG register, which erases the entire internal EEPROM, and then reprograms CONFIG for the desired features. Note that erasing the CONFIG register will cause the entire internal EEPROM, which is the codeplug, to be erased. After making the correction, "sscb_reset_diags.asm" writes a fatal error code to the "Status" window.

As for all fatal error codes, these CONFIG re-programmed errors will cause the Station Control Board microprocessor's COP timer to time-out which will activate RESET. Going through a reset will cause the "sscb_reset_diags.asm" routine to be executed again. However, this test is different in that the "sscb_reset_diags.asm" routine has made a correction before writing a fatal error code to the "Status" window. So, upon returning to this part of the routine, the CONFIG register should be correct and the firmware should not fail this test again. Note, however, that if the internal EEPROM was erased, the Station Control firmware will probably get caught in a fatal error loop due to some other error.

Next, "sscb_reset_diags.asm" calculates the single-byte-add checksum of the Station Control firmware. If this calculated checksum does not match the value stored in the Station Control firmware, "sscb_reset_diags.asm" writes a fatal error code to the "Status" window.

After the CONFIG test is complete, "sscb_reset_diags.asm" tests the Standard and I/O ASICs. For these ASIC tests, "internal" tests are still being performed. For the ASIC, "internal" mode means that the ASIC is tested by "sscb_reset_diags.asm" as a stand-alone device; that is, all outputs are looped back to the inputs. Later, when
the "external" diagnostics section of this routine is executed, the ASIC will be tested as part of the overall Station Control Tray. The first test performed on the Standard ASIC is verification of its Output Latches. Known data is written to the Output Latches, after which the corresponding loopback Input Buffers are read. If the Output Latches and Input Buffers do not agree, "sscb_reset_diags.asm" writes a fatal error code to the "Status" window.

Another test of the Standard ASIC is a test of the MUXbus circuitry. First, MUXbus address cycling is verified. Next, proper operation of the the Data Strobe line is checked. While checking for Data Strobe, the "sscb_reset_diags.asm" routine also verifies that "0's" can be read at all MUXbus addresses. If that test passes, the "sscb_reset_diags.asm" routine verifies that "1's" can be read at all MUXbus addresses. These checks verify operation of the MUXbus data and address lines. If any of these tests fail, "sscb_reset_diags.asm" writes a fatal error code to the "Status" window.

The next Standard ASIC tests are associated with the High Speed Ring (HSR). The first HSR test performed is an operational check of the Ring Synchronization and Ring Clock lines. Two "watchdog" bits (one for Ring Sync and one for Ring Clock), in the Standard ASIC hardware, are read to determine if Ring Sync and Ring Clock are operating properly. Next "sscb_reset_diags.asm" writes data to the Station Control portion of the HSR and then reads all portions of the HSR. If the data read from the Station Control portion does not match what was written or if the Trunked Tone Remote Control and Secure portions are not zero, the result is a HSR failure. Note that, since the Station Control board is in "internal" test mode, the Station Control board is not connected to the HSR, so the Trunked Tone Remote Control and Secure boards could

not have written to their portions of the HSR. The inverted version of the data is also written to the Station Control portion of the HSR and the same test is performed. If any of these HSR tests fail, "sscb_reset_diags.asm" writes a fatal error code to the "Status" window.

The next section of "sscb_reset_diags.asm" compares various parameters between the Station Control codeplug and the Station Control firmware. Before any data can be compared, the codeplug data must be transferred from EEPROM to RAM. If an external, serially-addressed EEPROM is present on the Station Control board, its data will also be transferred into RAM. If the serially-address EEPROM does not respond to commands, then a fatal error code will be written to the "Status" window. After transferring the codeplug, the flag that has bypassed service of the EEPROM until now is cleared. First of the comparisons, if the Module ID stored in the codeplug is not the same as the Module ID stored in the firmware, "sscb_reset_diags.asm" writes a fatal error code to the "Status" window. Second, if the codeplug version is not equal to the firmware version, "sscb_reset_diags.asm" writes a different fatal error code to the "Status" window. Thirdly, "sscb_reset_diags.asm" calculates the single-byte-add checksum of the Station Control codeplug. If this calculated checksum does not match the value stored in the Station Control codeplug, another fatal error code is written to the "Status" window.

Next, a check is made to determine if a reset occurred during an EEPROM update. In order to understand why this is a problem, the sequence of events to update the EEPROM must be understood. An image of the EEPROM is always kept in RAM; if a user modifies this RAM copy and wishes to make it "permanent" by writing it to the EEPROM, the user must issue a "write-EEPROM-from-RAM" command via the IPCB. This command causes the firmware to first erase the entire EEPROM, causing all bytes to be set to hexadecimal value "$FF". After erasing the EEPROM, the firmware begins copying the modified RAM image to the EEPROM area byte-by-byte; this copying process can take up to 15 seconds. One byte at the beginning of EEPROM is used as the check byte to determine if all of the RAM image has been copied to the EEPROM. This byte, which is set to '$FF' by the erase, is set to '00' only after all bytes have been copied from the RAM image to the EEPROM. If a reset occurs before this update is completed, this byte will be '$FF' and "sscb_reset_diags.asm" will know that the EEPROM may be corrupted; a fatal error code is then written to the "Status" window.

Another check is made to determine if a reset occurred during a "user area" update. The "user area" consists of dynamically-changable data that must be preserved between resets, so the data resides in EEPROM. When an update of the user-area is requested, only the bytes that reprogramming these bytes, the user-area "check byte" is erased to "$FF", and the check byte is programmed to zeroes when the updating process is finished. If a reset occurs before the update is finished, then the check-byte value of "$FF" will be transferred into RAM during the next diagnostic sequence and "sscb_reset_diags.asm" will then know that the user-area may be corrupted; a unique "user-area corrupt" fatal-error code will then be written to the "Status" window.

Last of the "internal" tests, the IPCB is tested for proper operation. A test pattern is written to the IPCB, and a check is made to ensure reception of the output data; if not received properly, "sscb_reset_diags.asm" will send a fatal-error code to the "Status" window.

At this point, the "internal" Station Control diagnostics are done and "sscb_reset_diags.asm" may begin its audio diagnostic tests. At this point, the "Disable" LED is activated to indicate that the digital hardware tests have completed, and "dashes"("---") are displayed in the front-panel "Status" window to indicate "audio diagnostics in progress". Before starting the actual audio diagnostics, however, the Analog-to-Digital (A-to-D) Converters of the microprocessor are checked to verify that they are operational. If any of the A-to-D Converters fail, "sscb_reset_diags.asm" immediately sends a non-fatal error code to the "Status" window for display. For this test, and the audio diagnostics which follow, once the error (always non-fatal) is displayed, the operator will have two seconds to activate the "Acc Dis" switch on the station's front panel. If the "Acc Dis" switch is activated within that time, the current diagnostic conditions will "freeze" to allow the operator to troubleshoot the failed circuit. Freezing the current diagnostic test may be desirable because this allows audio gating which may not be possible innormal operation. If the operator misses the time to activate the switch, the station can be reset with the Reset switch and the operator can then wait until the failed diagnostic test is executed again.

The first audio circuit which is checked is the PL Tone generator circuit. If the192.8 Hz tone is not present at the appropriate A-to-D Converter when the tone is enabled, "sscb_reset_diags.asm" sends a non-fatal error code to the "Status" window for display.

The next audio test is of the Alert Tone generator. If the 1000 Hz tone is not present at the appropriate A-to-D Converter when the tone is enabled, "sscb_reset_diags.asm" sends a non-fatal error code to the "Status" window for display.

Next, the Station Control board checks for PL at the transmitter. If the 192.8 Hz tone is not present at the TP4 A-to-D Converter when the tone is enabled, "sscb_reset_diags.asm" sends a non-fatal error code to the "Status" window for display.

Alert tones are then checked at the the transmitter; if a 1 KHz test tone shows an unusual characteristic at TP4 while the maximum deviation EEPOT is adjusted, or the

test tone is present when it should not be present, the appropriate error code will be sent to the "Status" window for display.

Receiver audio paths are then tested; if a 1 KHz test tone shows an unusual characteristic into the receive path while the receive level EEPOT is adjusted, the appropriate error code will be sent to the "Status" window for display.

Next, a 100 Hz tone is applied by the alert-tone encoder to the PL-decoder input and checked for proper form at that input; if an unexpected tone period is detected, the appropriate error code will be sent to the "Status" window for display.

The receiver and repeater squelch circuits are tested next. With loose squelch, if receiver or repeater-squelch activity is not detected, an error code will be displayed within the "Status" window. With tight squelch, if receiver or repeater squelch activity is detected, an error code will be displayed within the "Status" window. Using same tight squelch, a signal is "looped back" to the squelch-detector circuits to simulate receiver quieting; if nothing is detected, an error code will be displayed within the "Status" window.

After testing the squelch circuits, the Line and Receive Audio paths are checked for continuity; if a 1000 Hz test tone is not seen when it should be present, or seen when it should not be present, an error code will be displayed within the "Status" window. Similarly, the Repeat path is checked and an error code displayed if test tone is not there when it should or there when it shouldn't be.

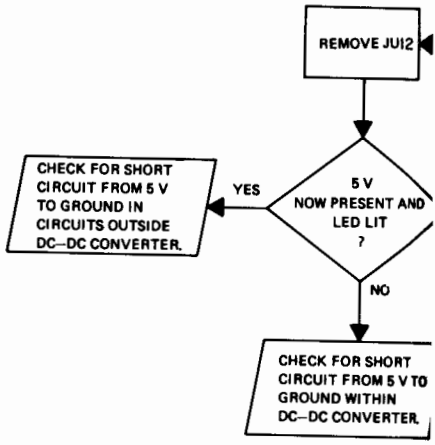
Lastly, the 1 KHz test tone is generated and looked for at TP1 (select audio); if it isn't there, an error code is displayed. The tone is removed and checked for; if still present, another error code is displayed.

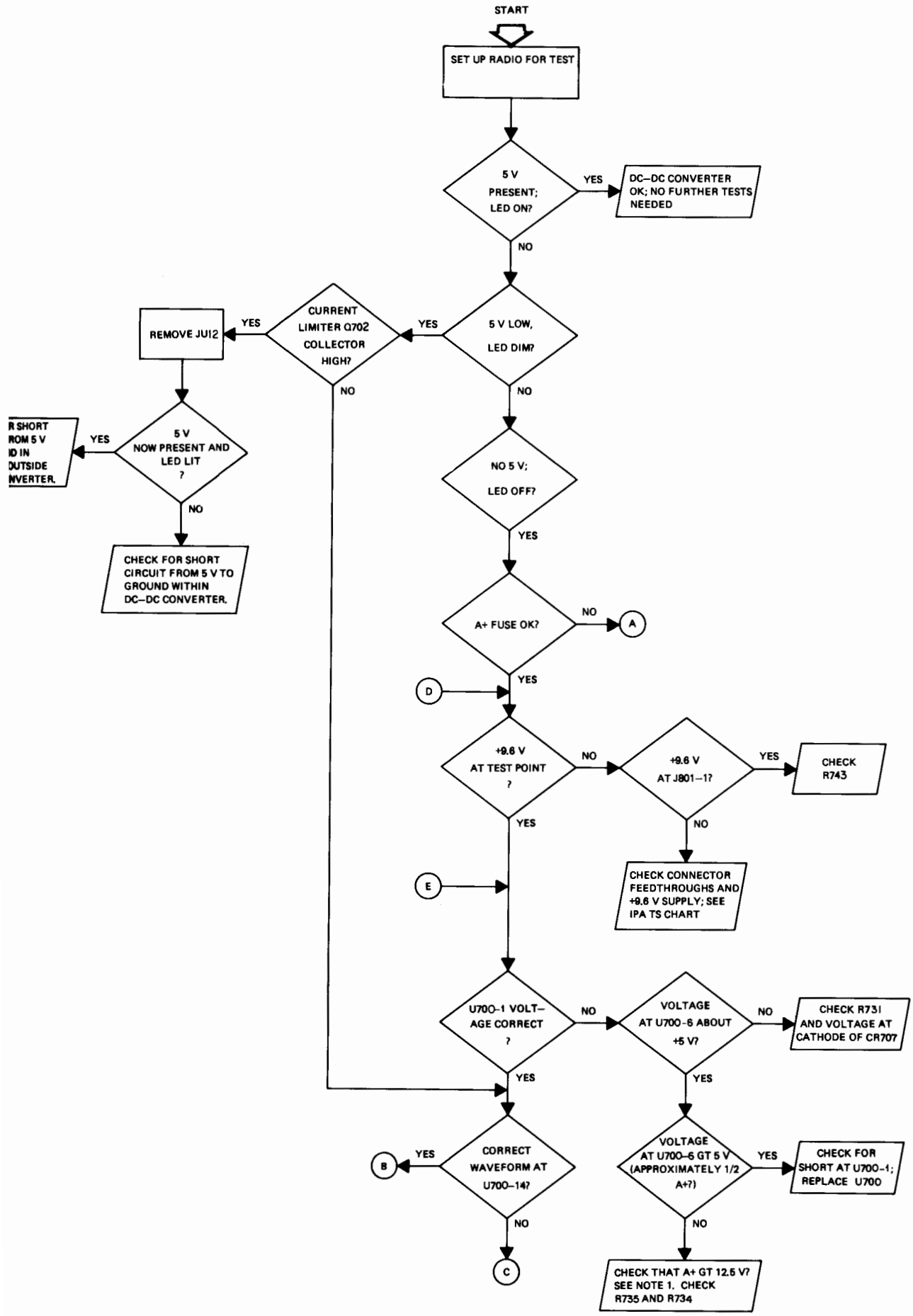
After audio diagnostics, the "dashes" are removed from the front-panel "Status" window, and "sscb_reset_diags.asm" attempts to set all EEPOTs to the "shadow" values kept within EEPROM; if any one EEPOT takes too long to set, a fatal error code will be generated and displayed within the "Status" window. At this point, Expansion Reset is released, allowing the remote boards to begin their diagnostics, and Station Control's firmware version number will be displayed within the "Status" window.

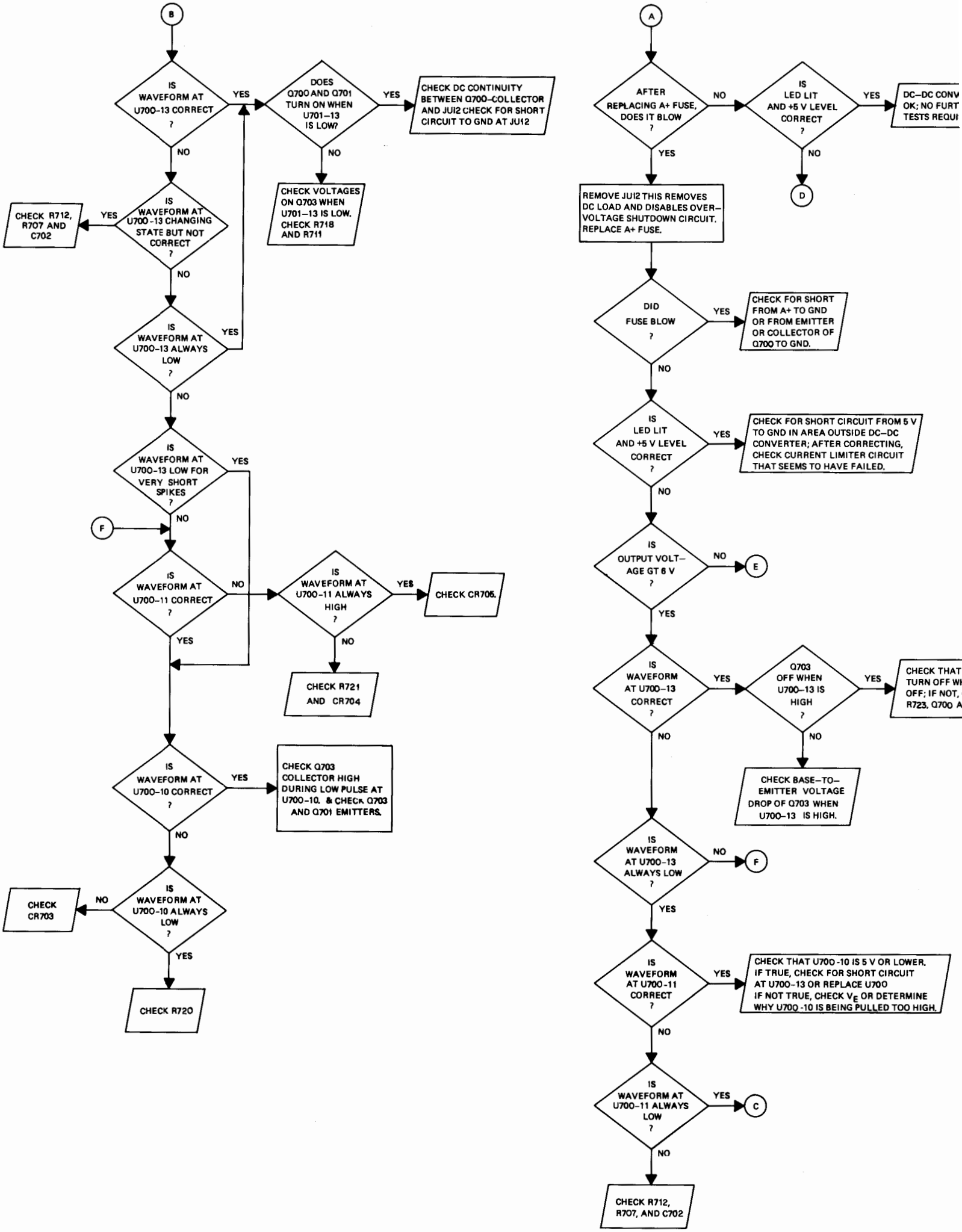
Once each remote board completes its "internal" diagnostics, it will wait for instruction from Station Control, either to "shut up" or "wake up" (if they don't receive any command before 10 seconds elapse, they will assume that Station Control never asked them to reset, and they will enter their own backgrounds). At this point, however, each remote board in the system is asked to please "shut up"; if any board fails to respond to this command, mutiny is assumed and a fatal error code is displayed within the "Status" window. While "sscb_reset_diags.asm" attempts to communicate with the remote boards, and while each remote board is performing its own external diagnostics, the "dashes" ("---") will be displayed in the "Status" window.

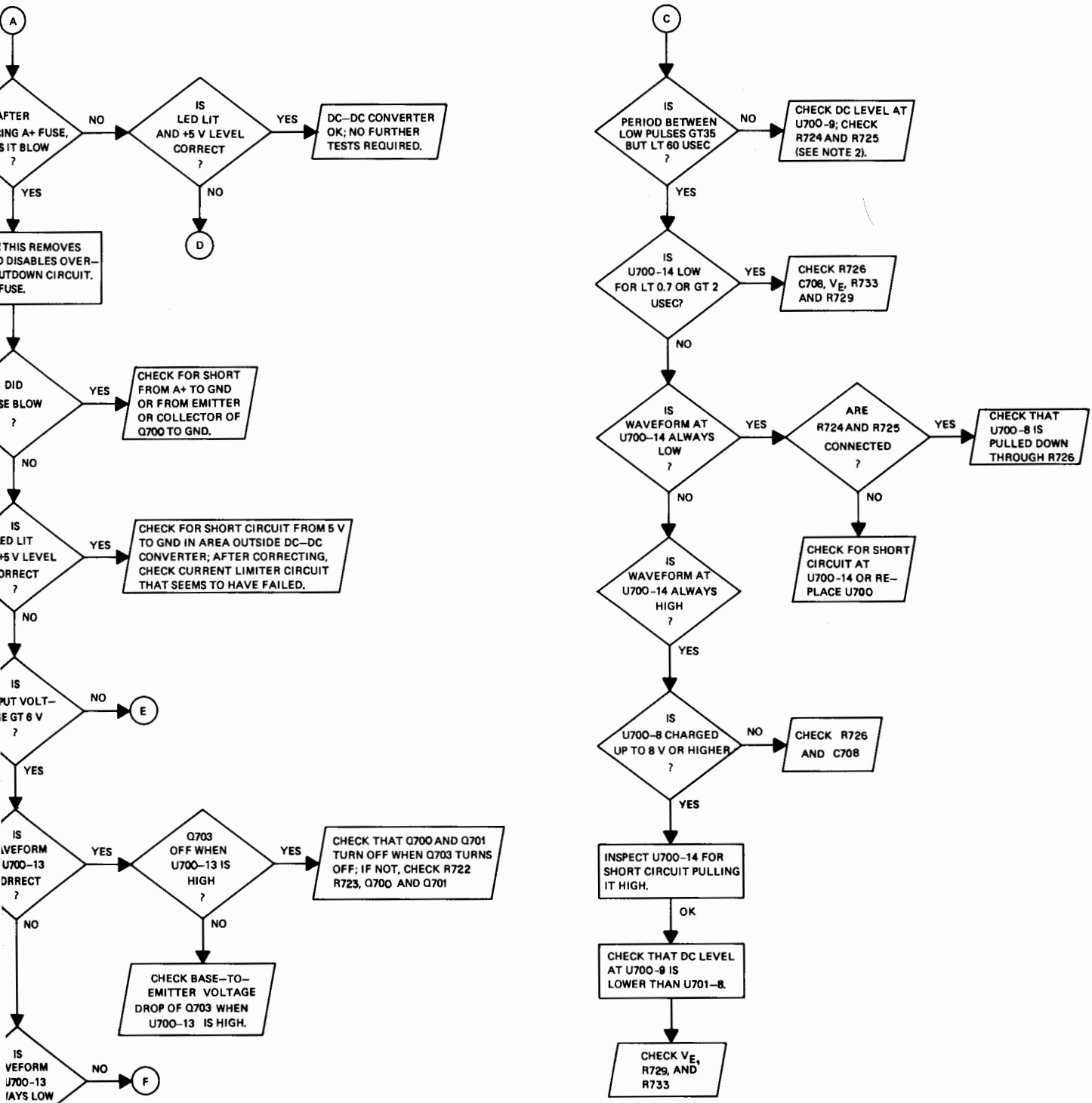
Once each board has "shut up", Station Control will ask the first remote board (TTRC, if present) to "wake up" and begin its external diagnostics. That board has five seconds to send something over the IPCB, either 1) its own IPCB test message, 2) a fatal or non-fatal error code, or 3) its firmware version number. Error codes received will be displayed in the "Status" window (fatal ones, of course, will remain in the window for five seconds before the Station Control board resets the entire station), and reception of the remote board's firmware version number signals the end of that board's diagnostics. Before displaying the version number, Station Control requests the "Station Type" and "System Version" bytes from the remote board; if any of those bytes don't match what Station Control has within its codeplug, a fatal error code will be displayed within the "Status" window (this check ensures that only compatible boards are used within a station). If all bytes match, that remote board's version number will be displayed in the "Status" window, and the next remote board in line (if any, determined by the Station Control codeplug) will be asked to "wake up", and this procedure will repeat until no more remote boards remain to be awoken. If any remote board fails to respond to any "wake up" command, a fatal error code will be displayed within the "Status" window.

After each remote board has had it's firmware version number displayed within the "Status" window of the Station Control board, "sscb_reset_diags.asm" will deactivate its "Disable" LED and ask each board (in turn) to enter its background; once again, if any board fails to respond to the command, a fatal error code will be displayed in the "Status" window. Just before entering its own background, Station Control will clear the "Status" window, call a variable-initialization routine, and begin background processing.


REMOVE JU12
5 V
NOW PRESENT AND
LED LIT
?
YES
CHECK FOR SHORT
CIRCUIT FROM 5 V
TO GROUND IN
CIRCUITS OUTSIDE
DC–DC CONVERTER.
NO
CHECK FOR SHORT
CIRCUIT FROM 5 V TO
GROUND WITHIN
DC–DC CONVERTER.


START
SET UP RADIO FOR TEST
5 V PRESENT; LED ON?
YES
DC–DC CONVERTER OK; NO FURTHER TESTS NEEDED
NO
5 V LOW, LED DIM?
YES
CURRENT LIMITER Q702 COLLECTOR HIGH?
YES
REMOVE JU12
YES
5 V NOW PRESENT AND LED LIT ?
YES
R SHORT ROM 5 V ID IN OUTSIDE NVERTER.
NO
CHECK FOR SHORT CIRCUIT FROM 5 V TO GROUND WITHIN DC–DC CONVERTER.
NO
NO 5 V; LED OFF?
YES
A+ FUSE OK?
NO
A
YES
D
+9.6 V AT TEST POINT ?
NO
+9.6 V AT J801–1?
YES
CHECK R743
NO
CHECK CONNECTOR FEEDTHROUGHS AND +9.6 V SUPPLY; SEE IPA TS CHART
YES
E
U700–1 VOLTAGE CORRECT ?
NO
VOLTAGE AT U700–6 ABOUT +5 V?
NO
CHECK R731 AND VOLTAGE AT CATHODE OF CR707
YES
YES
B
YES
CORRECT WAVEFORM AT U700–14?
NO
C
VOLTAGE AT U700–6 GT 5 V (APPROXIMATELY 1/2 A+?)
YES
CHECK FOR SHORT AT U700–1; REPLACE U700
NO
CHECK THAT A+ GT 12.5 V? SEE NOTE 1. CHECK R735 AND R734
CHECK R712, R707 AND C702
YES
NO
CHECK CR703
F


B
IS WAVEFORM AT U700-13 CORRECT ?
YES
DOES Q700 AND Q701 TURN ON WHEN U701-13 IS LOW?
YES
CHECK DC CONTINUITY BETWEEN Q700-COLLECTOR AND JU12 CHECK FOR SHORT CIRCUIT TO GND AT JU12
NO
CHECK VOLTAGES ON Q703 WHEN U701-13 IS LOW. CHECK R718 AND R711
NO
IS WAVEFORM AT U700-13 CHANGING STATE BUT NOT CORRECT ?
YES
CHECK R712, R707 AND C702
NO
IS WAVEFORM AT U700-13 ALWAYS LOW ?
YES
NO
IS WAVEFORM AT U700-13 LOW FOR VERY SHORT SPIKES ?
YES
NO
F
IS WAVEFORM AT U700-11 CORRECT ?
NO
IS WAVEFORM AT U700-11 ALWAYS HIGH ?
YES
CHECK CR705.
NO
CHECK R721 AND CR704
YES
IS WAVEFORM AT U700-10 CORRECT ?
YES
CHECK Q703 COLLECTOR HIGH DURING LOW PULSE AT U700-10. & CHECK Q703 AND Q701 EMITTERS.
NO
IS WAVEFORM AT U700-10 ALWAYS LOW ?
NO
CHECK CR703
YES
CHECK R720
A
AFTER REPLACING A+ FUSE, DOES IT BLOW ?
NO
IS LED LIT AND +5 V LEVEL CORRECT ?
YES
DC-DC CONV OK; NO FURT TESTS REQUI
NO
D
YES
REMOVE JU12 THIS REMOVES DC LOAD AND DISABLES OVER-VOLTAGE SHUTDOWN CIRCUIT. REPLACE A+ FUSE.
DID FUSE BLOW ?
YES
CHECK FOR SHORT FROM A+ TO GND OR FROM EMITTER OR COLLECTOR OF Q700 TO GND.
NO
IS LED LIT AND +5 V LEVEL CORRECT ?
YES
CHECK FOR SHORT CIRCUIT FROM 5 V TO GND IN AREA OUTSIDE DC-DC CONVERTER; AFTER CORRECTING, CHECK CURRENT LIMITER CIRCUIT THAT SEEMS TO HAVE FAILED.
NO
IS OUTPUT VOLTAGE GT 6 V ?
NO
E
YES
IS WAVEFORM AT U700-13 CORRECT ?
YES
Q703 OFF WHEN U700-13 IS HIGH ?
YES
CHECK THAT TURN OFF WI OFF; IF NOT, R723, Q700 A
NO
NO
CHECK BASE-TO-EMITTER VOLTAGE DROP OF Q703 WHEN U700-13 IS HIGH.
IS WAVEFORM AT U700-13 ALWAYS LOW ?
NO
F
YES
IS WAVEFORM AT U700-11 CORRECT ?
YES
CHECK THAT U700-10 IS 5 V OR LOWER. IF TRUE, CHECK FOR SHORT CIRCUIT AT U700-13 OR REPLACE U700 IF NOT TRUE, CHECK V_E OR DETERMINE WHY U700-10 IS BEING PULLED TOO HIGH.
NO
IS WAVEFORM AT U700-11 ALWAYS LOW ?
YES
C
NO
CHECK R712, R707, AND C702



SYMBOLS AND ABBREVIATIONS USED IN THE CHART

= TEST TO BE DONE

= DECISION

= SOURCE OF FAULT

U701–2 = PIN NO. 2 OF U701

J801–1 = PIN NO. 1 OF J801

GT = GREATER THAN

LT = LESS THAN

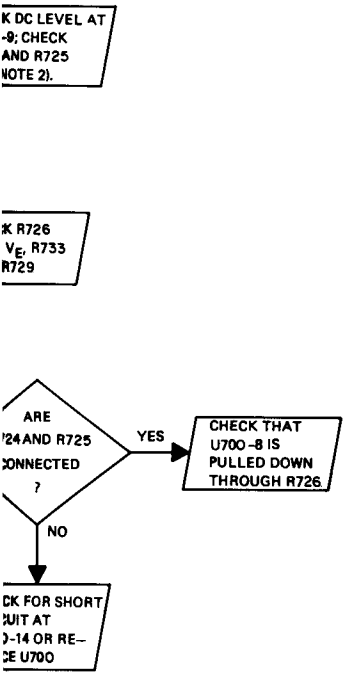
TS = TROUBLESHOOTING

LED = GRN DS710 ON STATION CONTROL BOARD

NOTES:

1. WHEN OPERATING FR A+ MAY BE LESS THAN COMPARATOR MAY HO SHUTDOWN MODE (I.E HAPPENS, MOMENTAR TO RESET POSITION. IF LESS THAN 10.5 V, DC- ENERGIZE.
2. WHEN CHECKING DC L OF OSCILLATOR CIRC IGNORE ANYTHING EL U700-9 SINCE DC LEV
3. REFER TO SCHEMATIC VARIOUS CIRCUITS RE

EEPS–46515–0



NOTES:

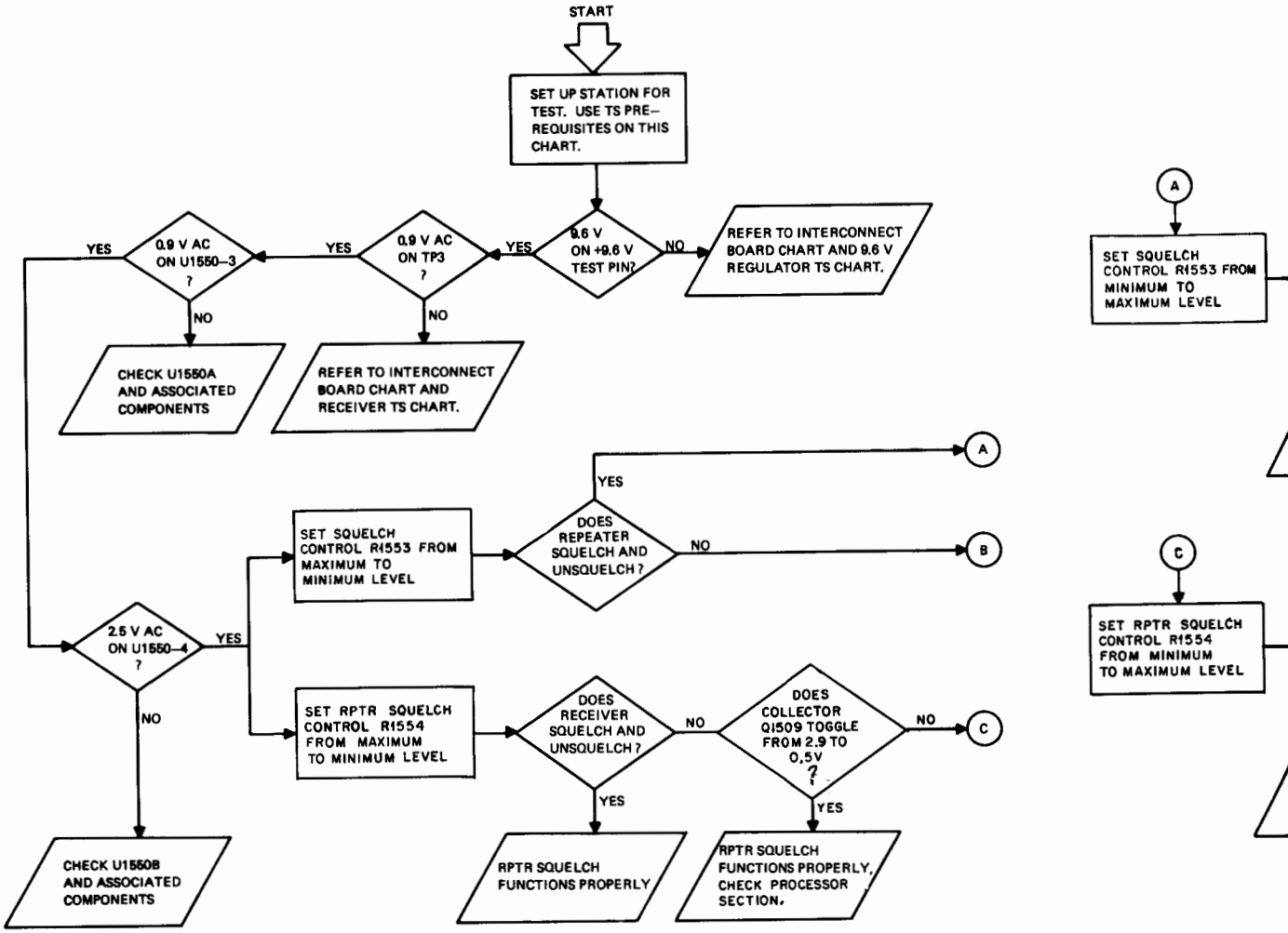
1. WHEN OPERATING FROM BATTERY–SUPPLIED POWER, A+ MAY BE LESS THAN 12.5 V AND SHUTDOWN COMPARATOR MAY HOLD DC–DC CONVERTER IN SHUTDOWN MODE (I.E. U700–1 IS LOW). IF THIS HAPPENS, MOMENTARILY PLACE ACC DIS/RESET SWITCH TO RESET POSITION. IF A+ SUPPLIED BY BATTERY IS LESS THAN 10.5 V, DC–DC CONVERTER WILL NOT ENERGIZE.
2. WHEN CHECKING DC LEVEL AT U700-9, OPERATION OF OSCILLATOR CIRCUIT IS ALWAYS DISTURBED. IGNORE ANYTHING ELSE THAT HAPPENS WHEN PROBING U700-9 SINCE DC LEVEL CAN BE RELIABLY CHECKED.
3. REFER TO SCHEMATIC DIAGRAMS IN THIS MANUAL FOR VARIOUS CIRCUITS REFERENCED IN CHART.

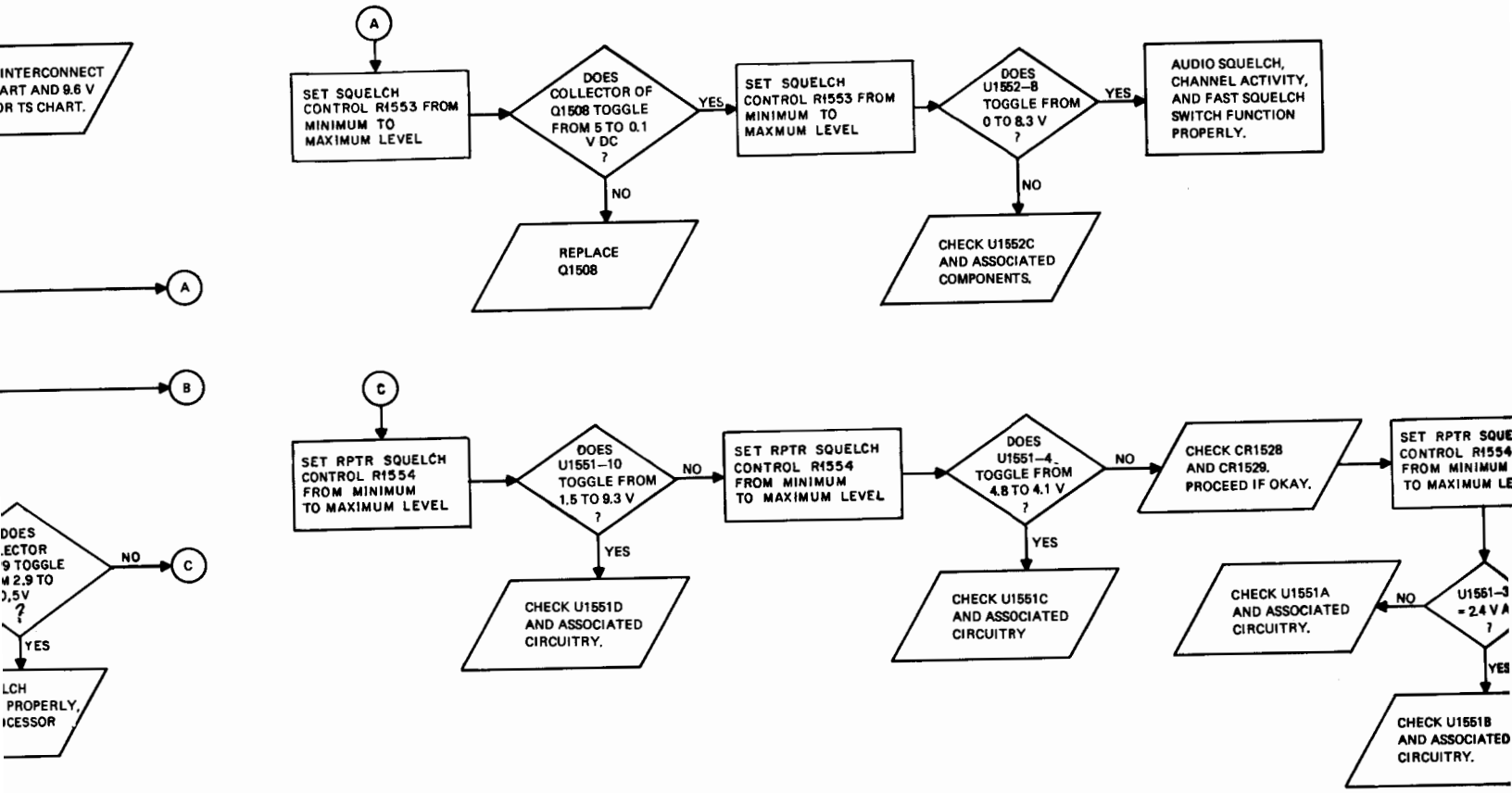
- PIN NO. 2 OF U701
- PIN NO. 1 OF J801
- GREATER THAN
- LESS THAN
- TROUBLESHOOTING
- GRN DS710 ON STATION CONTROL BOARD

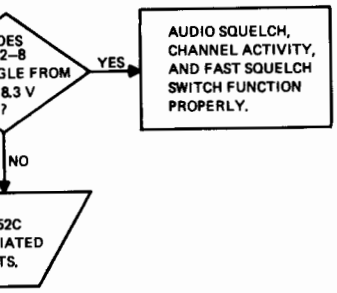
EPS–46515–0

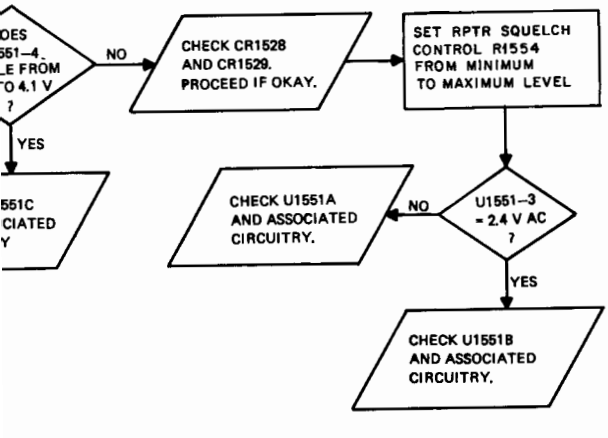
SECURE CAPABLE STATION CONTROL BOARD

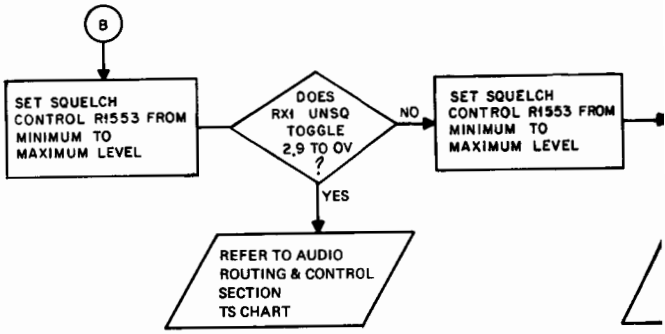
RECEIVER AUDIO AND SQUELCH CONTROL TROUBLESHOOTING CHART

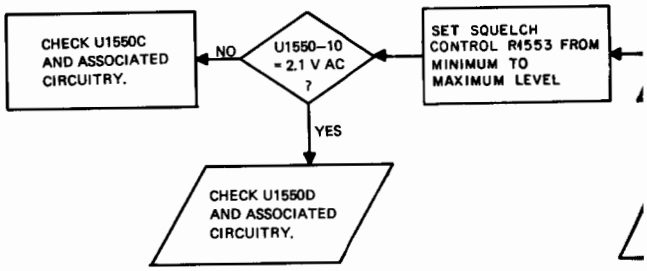


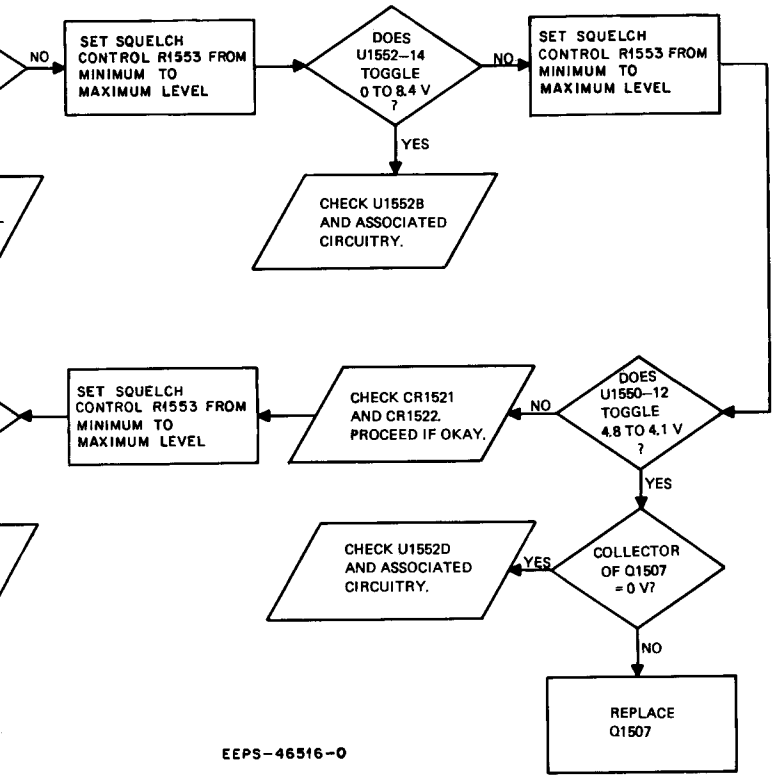

INTERCONNECT
ART AND 9.6 V
OR TS CHART.
A
B
C
DOES
LECTOR
9 TOGGLE
M 2.9 TO
),5V
?
NO
YES
LCH
PROPERLY,
ICESSOR
A
SET SQUELCH CONTROL R1553 FROM MINIMUM TO MAXIMUM LEVEL
DOES COLLECTOR OF Q1508 TOGGLE FROM 5 TO 0.1 V DC ?
YES
NO
REPLACE Q1508
SET SQUELCH CONTROL R1553 FROM MINIMUM TO MAXMUM LEVEL
DOES U1552–8 TOGGLE FROM 0 TO 8.3 V ?
YES
NO
AUDIO SQUELCH, CHANNEL ACTIVITY, AND FAST SQUELCH SWITCH FUNCTION PROPERLY.
CHECK U1552C AND ASSOCIATED COMPONENTS.
C
SET RPTR SQUELCH CONTROL R1554 FROM MINIMUM TO MAXIMUM LEVEL
DOES U1551–10 TOGGLE FROM 1.5 TO 9.3 V ?
NO
YES
CHECK U1551D AND ASSOCIATED CIRCUITRY.
SET RPTR SQUELCH CONTROL R1554 FROM MINIMUM TO MAXIMUM LEVEL
DOES U1551–4 TOGGLE FROM 4.8 TO 4.1 V ?
NO
YES
CHECK U1551C AND ASSOCIATED CIRCUITRY
CHECK CR1528 AND CR1529. PROCEED IF OKAY.
SET RPTR SQUE
CONTROL R1554
FROM MINIMUM
TO MAXIMUM LE
CHECK U1551A AND ASSOCIATED CIRCUITRY.
NO
U1551–3
= 2.4 V A
?
YES
CHECK U1551B AND ASSOCIATED CIRCUITRY.


YES
AUDIO SQUELCH, CHANNEL ACTIVITY, AND FAST SQUELCH SWITCH FUNCTION PROPERLY.
NO


NO
CHECK CR1528 AND CR1529. PROCEED IF OKAY.
SET RPTR SQUELCH CONTROL R1554 FROM MINIMUM TO MAXIMUM LEVEL
YES
CHECK U1551A AND ASSOCIATED CIRCUITRY.
NO
U1551–3 = 2.4 V AC ?
YES
CHECK U1551B AND ASSOCIATED CIRCUITRY.


B
SET SQUELCH CONTROL R1553 FROM MINIMUM TO MAXIMUM LEVEL
DOES RX1 UNSQ TOGGLE 2,9 TO 0V ?
NO
SET SQUELCH CONTROL R1553 FROM MINIMUM TO MAXIMUM LEVEL
YES
REFER TO AUDIO ROUTING & CONTROL SECTION TS CHART


CHECK U1550C AND ASSOCIATED CIRCUITRY.
NO
U1550–10 = 2.1 V AC ?
SET SQUELCH CONTROL R1553 FROM MINIMUM TO MAXIMUM LEVEL
YES
CHECK U1550D AND ASSOCIATED CIRCUITRY.



EEPS-46516-O

SYMBOLS AND ABBREVIATIONS USED IN THE CHART

ALL VOLTAGE MEASUREMENTS ARE DC, UNLESS OTHERWISE STATED. AC VOLTAGES ARE MEASURED WITH AN AVERAGE RESPONDING METER.

= TEST TO BE DONE

= DECISION

= SOURCE OF FAULT

TS	= TROUBLESHOOTING
U1550–3	= PIN 3 OF U1550
CW	= CLOCKWISE
CCW	= COUNTERCLOCKWISE

TROUBLESHOOTING PREREQUISITES:

1. ENERGIZE STATION. RECEIVE SYNTHESIZER MUST BE LOCKED (RX LOCK LED LIT). IF NOT, PERFORM RECEIVER TROUBLESHOOTING PROCEDURE.
2. PL DISABLE STATION BY PUTTING SW800 IN THE PL DIS POSITION (UP).
3. ACCESS DISABLE STATION BY PUTTING SW801 IN THE "ACC DIS" POSITION. (UP)
4. PROVIDE A MEANS OF LISTENING TO LOCAL AUDIO. PLUG PORTABLE TEST SET INTO J812.
5. THERE SHOULD BE NO RF SIGNAL PRESENT AT THE RECEIVER INPUT (DISCONNECT ANTENNA).
6. WHEN TROUBLESHOOTING IS COMPLETE, READJUST THE AUDIO AND REPEATER SQUELCH SECTION TO PROPER SYSTEM SPECIFICATIONS.

parts list

TRN7008A Display Board — PL-11223-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		connector:
J805A,805B	2883547T01	male: 8-contact
		light emitting diode: (see note)
DS8200 thru 8202	4882771L03	red, 7 segment display
		non-referenced items
	5483865R01	LABEL, bar code

TVN6055A Station Control EPROM — PL-11224-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		integrated circuit: (see note)
U804	5191006C01	32k x 8 EPROM

TRN7039A Control Hardware Kit — PL-11225-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		non-referenced items
	1382456T01	BEZEL, station control
	1583186N01	HOUSING, control
	1584078N01	COVER, plastic dust
	3683144N02	KNOB, control: 2 used
	4783154N01	BAR, control support

TRN7061A/TRN7179A/TRN9998A
Secure Capable Station Control Board — PL-11241-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF ±5% 50V unless otherwise stated
C700	2113741B45	.01
C701	2383210A24	1.0 -10+150% 20V
C702	2113741B45	.01
C703	2113741B69	0.1
C704 thru 706	2113740B39	39pF
C707	2113741B69	0.1
C708	2113740B73	.001
C709	2382601A48	660 -10+100% 40V
C710	0811051A15	0.22 63V
C711	2113741B69	0.1
C712	2113741B45	.01
C713	2311049A08	1.0 ±10% 35V
C714	2311049A19	10 ±10% 25V
C715	2113740B49	100pF
C716	2311049A19	10 ±10% 25V
C717	2113741B69	0.1
C718	2311019A45	100 ±20% 16V
C719,720	2311049A19	10 ±10% 25V
C722	2113740B39	39pF
C723	0811051A07	.01 63V
C724 thru 726	2113740B39	39pF
C727	2113741B69	0.1
C800	2113741B45	.01
C801	2113740B68	620pF
C802 thru 811	2113741B69	0.1
C812	2311049A19	10 ±10% 25V
C813 thru 816	2113740B34	24pF
C819	2113741B69	0.1
C820	2113741B45	.01
C822	2311049A08	1.0 ±10% 35V
C823 thru 828	2113741B69	0.1
C829	2113740B49	100pF
C830	2113741B69	0.1
C1543	2113740B73	.001
C1544	0811051A13	0.1 63V
C1545,1546	2113740B47	82pF
C1547	0811051A07	.01 63V
C1548	0811051A02	.0015 63V
C1549	2113740B57	220pF
C1551	0811051A04	.0033 63V
C1552,1553	2311049A10	2.2 ±10% 35V
C1554	0811051A07	.01 63V
C1555	2113740B34	24pF
C1556,1557	0811051A07	.01 63V
C1558	0811051A02	.0015 63V
C1559	2113740B73	.001
C1560	2113740B34	24pF
C1561	0811051A04	.0033 63V
C1562	2311049A10	2.2 ±10% 35V
C1564	2113741B37	.0047
C1579	2113740B57	220pF
C8100,8101	2113740B49	100pF
C8102	0811051A05	.0047 63V
C8103	0811051A11	.047 63V
C8104	0811051A04	.0033 63V
C8105	2383210A19	500 -10+100% 20V
C8106	0811051A13	0.1 63V
C8107	0811051A08	.015 63V
C8108	0811051A07	.01 63V
C8109	2384665F06	220 -10+150% 25V
C8110	0811051A06	.0068 63V
C8111	0811051A04	.0033 63V
C8112	2311049A15	4.7 ±10% 35V
C8113	2113740B49	100pF
C8114,8115	2113740B57	220pF
C8116	0811051A15	0.22 63V
C8117	2311049A10	2.2 ±10% 35V
C8118	2311049A08	1.0 ±10% 35V
C8119	0811051A04	.0033 63V
C8121	2113740B57	220pF
C8122,8123	2311049A08	1.0 ±10% 35V
C8125	2311049A08	1.0 ±10% 35V
C8126,8127	2113740B49	100pF
C8128	0811051A02	.0015 63V
C8129,8130	2113740B49	100pF
C8131 thru 8133	2113740B40	43pF
C8134	2311049A08	1.0 ±10% 35V
C8135	0811051A15	0.22 63V
C8136	2311049A19	10 ±10% 25V
C8137 thru 8140	0811051A15	0.22 63V
C8141	2113741B45	.01
C8142 thru 8144	2113741B69	0.1
C8147,8148	2113741B69	0.1
C8151	2311049A15	4.7 ±10% 35V
C8152	2113740B49	100pF
C8153	2113741B45	.01
C8154	2113740B49	100pF
C8156	2113740B49	100pF
C8157	2113741B45	.01
C8158	0811051A10	.033 63V
C8159	0811051A12	.068 63V
C8160	2113740B49	100pF
C8161	0811051A04	.0033 63V
C8162	0811051A13	0.1 63V
C8163	2113740B74	.0012

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
C8169	2113740B40	43pF
C8170	0811051A15	0.22 63V
C8171	2311049A19	10 ±10% 25V
C8172	2113740B36	30pF
C8173	0811051A07	.01 63V
C8174	2113740B57	220pF
C8175,8176	2311049A08	1.0 ±10% 35V
C8177	2311049A10	2.2 ±10% 35V
C8178	2311049A08	1.0 ±10% 35V
C8179 thru 8191	2113741B69	0.1
C8193	2113741B69	0.1
C8195 thru 8198	2113741B69	0.1
C8200	2113741B33	.0033
C8201	2113740B55	180pF
C8202	2113741B45	.01
C8203	2113741B37	.0047
C8204	2113740B73	.001
C8205	0811051A15	0.22 63V
C8207	2113740B73	.001
C8209,8210	0811051A13	0.1 63V
C8214 thru 8216	2113740B73	.001
C8217	0811051A13	0.1 63V
C8218	0811051A15	0.22 63V
C8219	2113741B69	0.1
C8220	2113740B73	.001
C8225	2113740B73	.001
C8230	2113740B57	220pF
C8231	2113740B73	.001
C8232	0811051A13	0.1 63V
		diode: (see note)
CR700	4882525G18	silicon
CR701	4882466H13	silicon
CR702 thru 708	4811058A11	silicon
CR709	4882466H13	silicon
CR800	4884336R03	silicon
CR801	4811058A11	silicon
CR806	4884336R03	silicon
CR809	4884336R03	silicon
CR815 thru 819	4884336R03	silicon
CR827 thru 840	4884336R03	silicon
CR1520 thru 1522	4805129M41	hot carrier
CR1523,1524	4811058A11	silicon
CR1526,1527	4811058A11	silicon
CR1528,1529	4805129M41	hot carrier
CR1530	4811058A11	silicon
CR1531	4805129M41	hot carrier
CR8102,8103	4811058A11	silicon
CR8105	4884336R03	silicon
CR8107	4811058A11	silicon
CR8108	4884336R03	silicon
CR8110	4805129M41	hot carrier
CR8111	4811058A11	silicon
CR8112,8113	4805129M41	hot carrier
CR8114	4811058A11	silicon
CR8200 thru 8203	4805129M41	hot carrier
		light emitting diode: (see note)
DS800 thru 803	4888245C29	green
DS804	4888245C30	yellow
DS805	4888245C28	red
		fuse:
F700	6500139764	3A 32V
		hybrid:
HY803	TFN6045A	PL high-pass filter
HY805	TRN7008A	display board
		connector:
J701	2882984N13	male: 6-contact
J800	2882296R34	male: 40-contact
J801	2882505T03	male: 26-contact
J802	2883143M04	male: 20-contact
J803	2882505T05	male: 40-contact
J804	2882505T04	male: 34 contact
J806,807	0984231B03	female: phono
J812	0983112N01	female: 6-contact
		jumper:
JU1 thru 12	2810774B02	male: 3-contact
		coil:
L700	2482380N01	400uH
L701	2483977B01	1-1/2 turns
L702	2582786N01	620uH
L800	2411047A25	10uH
L803	2482415N02	10mH
		transistor: (see note)
Q700	4800869829	PNP type M9829
Q701	4800869328	PNP type M9328
Q702,703	4800869643	PNP type M9643
Q704	4883875D05	SCR (silicon controlled diode)
Q705	4811056A08	PNP type M56A08
Q706	4811056A03	NPN type M56A03
Q800	4811056A08	PNP type M56A08
Q801	4811056A03	NPN type M56A03
Q802	4800869642	NPN type M9642
Q803,804	4811056A03	NPN type M56A03
Q805	4800869642	NPN type M9642
Q806,807	4811056A03	NPN type M56A03
Q808 thru 811	4811056A23	NPN type M56A23
Q813,814	4811056A03	NPN type M56A03
Q816,817	4811056A03	NPN type M56A03
Q820	4811056A03	NPN type M56A03
Q821	4800869653	JFET, n-channel type M9653
Q822,823	4811056A03	NPN type M56A03
Q1507 thru 1510	4811056A03	NPN type M56A03
Q8100	4811056A03	NPN type M56A03
Q8200 thru 8207	4811056A08	PNP type M56A08
Q8208 thru 8210	4811056A23	NPN, Darlington type M56A23
Q8211,8212	4811056A03	NPN type M56A03
		resistor, fixed: ±5% 1/8W unless otherwise stated
R700	0611077A98	10k
R701	0611077A88	3.9k
R702	0611077A50	100
R703	0611077A74	1k
R704	0611077A35	24
R705,706	0611077A58	220
R707	0611077A84	2.7k
R708	0611045A37	330 1/2W
R709	0611077B25	120k
R710	0611077A86	3.3k
R711	0611077A72	820
R712	0611077A96	8.2k
R713	0611009F24	2.7 1/4W
R714	0611077A72	820
R715	0611077A42	47
R716 thru 719	0611086A03	1 1W
R720	0611077A80	1.8k
R721	0611077A88	3.9k
R722	0611077A50	100
R723	0611077A64	390
R724	0611077B01	12k
R725	0611077B07	22k
R726	0611077A84	2.7k
R727	0611077A64	390
R728	0611077A88	3.9k
R729	0611077B17	56k
R730	0611077A01	0-ohm jumper
R731	0611077A50	100
R733	0611077B29	180k
R734	0611049C26	2.1k ±1% 1/4W
R735	0611049C22	1.91k ±1! 1/4W
R736	0611009A33	220 1/4W
R737	0611077A84	2.7k
R738	0611077A64	390
R739	0611077A98	10k
R740	0611077A56	180
R741	0611077A98	10k
R742	0611077A86	3.3k
R743	0611086A03	1 1W
R747	0611077A98	10k
R748	0611077A78	1.5k
R749	0611077A96	8.2k
R750	0611077B47	1 meg
R751	0611077A88	3.9k
R752	0611077B07	22k
R753	0611077A96	8.2k
R755	0611077A68	560
R800	0611077A54	150
R801	0611077A88	3.9k
R803,804	0611077A88	3.9k
R806	0611077A98	10k
R807	0611077A94	6.8k
R809,810	0611077A94	6.8k
R812	0611077A78	1.5k
R813	0611077A32	18
R814	0611077A58	220
R815	0611077A32	18
R816	0611077A90	4.7k
R817	0611077A98	10k
R818	0611077A54	150
R819	0611077A32	18
R820	0611077A58	220
R821	0611077A78	1.5k
R822	0611077A58	220
R823	0611077A98	10k
R824	0611077A80	1.8k
R825,826	0611077A98	10k
R827	0611077A88	3.9k
R828	0611077B07	22k
R829	0611077A94	6.8k
R830 thru 836	0611077A98	10k
R837,838	0611077A50	100
R839	0611077A98	10k
R840,841	0611077A50	100
R842	0611077A98	10k
R843 thru 846	0611077A50	100
R847,848	0611077A98	10k

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R849	0611077B09	27k
R850	0611077A98	10k
R851	0611077A58	220
R852,853	0611077B47	1 meg
R854	0611077A98	10k
R855	0611077A92	5.6k
R856 thru 858	0611077A98	10k
R861	0611077B09	27k
R862	0611077A88	3.9k
R863	0611077A54	150
R866	0611077A98	10k
R867	0611077A78	1.5k
R868 thru 871	0611077A98	10k
R872	0611077A54	150
R873	0611077A98	10k
R874	0611077A54	150
R875	0611077A86	3.3k
R876	0611077A98	10k
R877	0611077A54	150
R878	0611077A90	4.7k
R879	0611077A82	2.2k
R880	0611077A78	1.5k
R881	0611077A98	10k
R882	0611077A82	2.2k
R883,884	0611077A98	10k
R885	0611077A90	4.7k
R887	0611077A98	10k
R888	0611077B39	470k
R889	0611077A98	10k
R890	0611077A74	1k
R891	0611077A98	10k
R893	0611077A98	10k
R894	0611077B09	27k
R895 thru 898	0611077A98	10k
R1523	0611077B15 or	47k (TRN7061A, TRN9998A)
	0611077B17	56k (TRN7179A)
R1524	0611077A86	3.3k
R1525	0611077B17 or	56k (TRN7061A)
	0611077B11 or	33k (TRN7179A)
	0611077B13	39k (TRN9998A)
R1526	0611077A82	2.2k
R1527	0611077B17 or	56k (TRN7061A)
	0611077B11 or	33k (TRN7179A)
	0611077B13	39k (TRN9998A)
R1532	0611077B27	150k
R1533	0611077A64	390
R1534	0611077A78	1.5k
R1535	0611077B23 or	100k (TRN7061A, TRN9998A)
	0611077B15	47k (TRN7179A)
R1536	0611077B39 or	470k (TRN7061A)
	0611077B31	220k (TRN7179A,TRN9998A)
R1537	0611077B15	47k
R1540	0611077B15	47k
R1543	0611077B23	100k
R1544	0611077A74	1k
R1545	0611077B19	68k
R1546	0611077A74	1k
R1547	0611077A98	10k
R1548	0611077B33	270k
R1549	0611077A94	6.8k
R1550	0611077A98	10k
R1553	0611077B19	68k
R1554	0611077B21	82k
R1555,1556	0611077A98	10k
R1557	0611077B27	150k
R1559	0611077A64	390
R1560	0611077B15	47k
R1561	0611077B23 or	100k (TRN7061A, TRN9998A)
	0611077B15	47k (TRN7179A)
R1562	0611077B39 or	470k (TRN7061A)
	0611077B31	220k (TRN9998A, TRN7179A)
R1563	0611077B15	47k
R1565,1566	0611077A74	1k
R1567	0611077A94	6.8k
R1568	0611077A98	10k
R1570	0611077A74	1k
R1571	0611077B21 or	82k (TRN7061A)
	0611077A98	10k (TRN9998A, TRN7179A)
R1572	0611077A01	0-ohm jumper
R1573,1574	0611077B14 or	43k (TRN7061A)
	0611077A91	5.1k (TRN9998A, TRN7179A)
R1575	0611077A92	5.6k
R1576	0611077B27	150k
R1578	0611077A78	1.5k
R1599	1882787K08	var 100k ±20% 1/4W
R8100	0611077B05	18k
R8101	0611077A94	6.8k
R8102,8103	0611077B05	18k
R8106	0611077B03	15k
R8107,8108	0611077A98	10k
R8109	0611077B05	18k
R8110	0611077B13	39k
R8111	0611077A98	10k
R8112	0611077A94	6.8k
R8113,8114	0611077A86	3.3k
R8115	0611077B09	27k

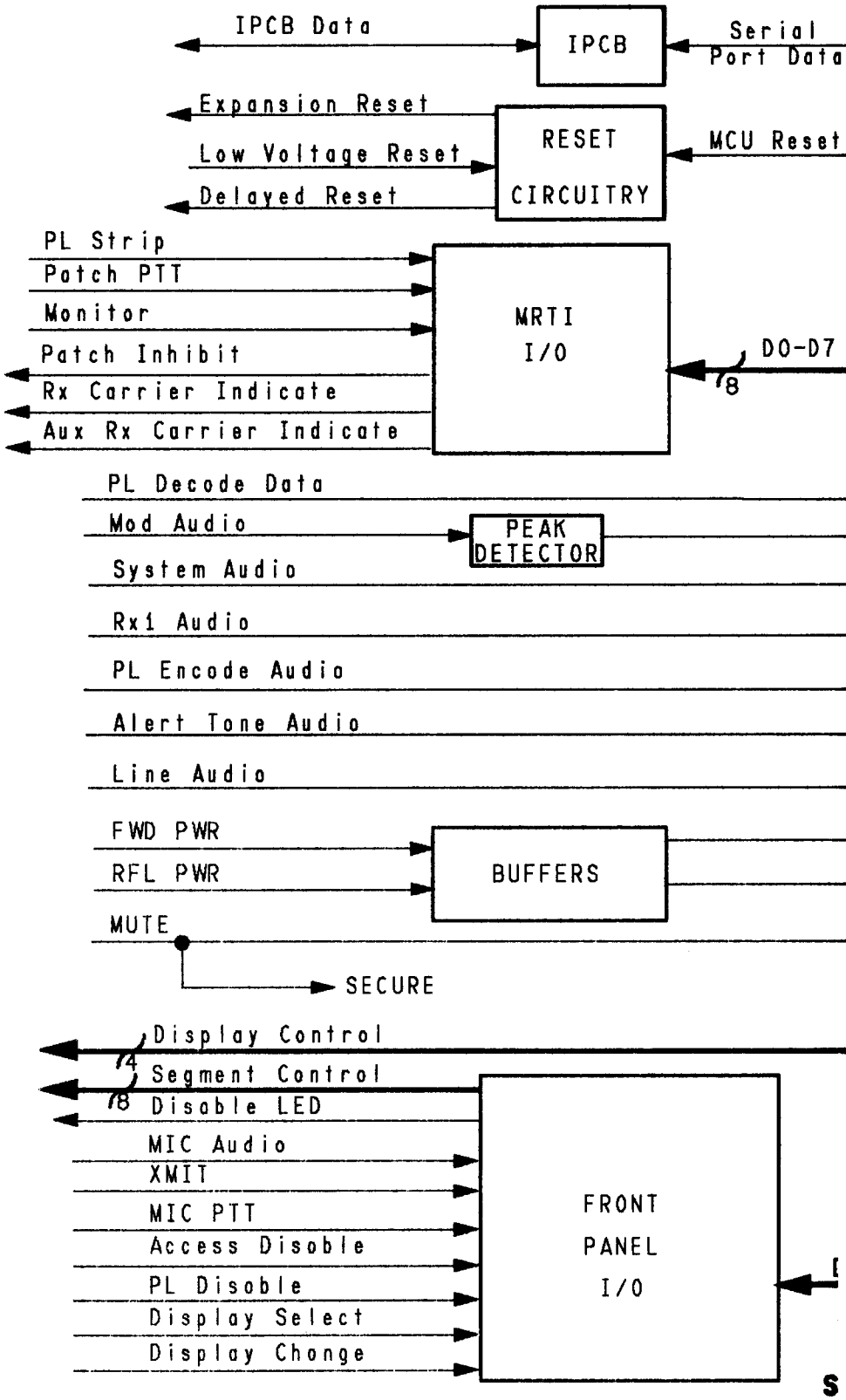
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R8116	0611077A94	6.8k
R8117	0611009B26	2.7 1/4W
R8118	0611077A94	6.8k
R8119	0611077B02	13k
R8120	0611077B03	15k
R8121	0611086A08	4.7 1W
R8122	0611077A26	10
R8123	0611077B39	470k
R8124	0611077A94	6.8k
R8125	0611077A98	10k
R8127	0611077A94	6.8k
R8128	0611077A86	3.3k
R8129	0611077A78	1.5k
R8130	0611077B39	470k
R8131	0611077A98	10k
R8134	0611077B17	56k
R8135	1882787K09	var 5k ±10% 1/4W
R8136	0611077B05	18k
R8137	0611077B09	27k
R8138,8139	0611077B11	33k
R8141	0611077B09	27k
R8142	0611077B07	22k
R8143	0611077B01	12k
R8144	0611077A98	10k
R8146	0611077B01	12k
R8147	0611077B09	27k
R8148	0611077A98	10k
R8149	0611077B09	27k
R8150	0611077B18	62k
R8151,8152	0611077B09	27k
R8153	0611077B07	22k
R8154	0611077B01	12k
R8155	0611077B09	27k
R8156	0611077B18	62k
R8157 thru 8159	0611077B09	27k
R8162	0611077B07	22k
R8163	0611077B09	27k
R8164	0611077A98	10k
R8165,8166	0611077B09	27k
R8167	0611077B23	100k
R8168	0611077B30	200k
R8169	0611077B23	100k
R8170	0611077A68	560
R8171	0611077B30	200k
R8172	0611077A50	100
R8173,8174	0611077B23	100k
R8175	0611077A98	10k
R8176	0611077A91	5.1k
R8177	0611077B09	27k
R8178,8179	0611077B14	43k
R8180	0611077B09	27k
R8181 thru 8185	0611077B18	62k
R8188	0611077B23	100k
R8191	0611077A98	10k
R8192	0611077A86	3.3k
R8193	0611077A98	10k
R8198	0611077A74	1k
R8199	0611077A01	0-ohm jumper
R8200	0611077A78	1.5k
R8201	0611077A44	56
R8202	0611077A78	1.5k
R8203	0611077A90	4.7k
R8204	0611077A44	56
R8205,8206	0611077A78	1.5k
R8207	0611077A82	2.2k
R8208	0611077A44	56
R8209,8210	0611077A78	1.5k
R8211	0611077A90	4.7k
R8212	0611077A44	56
R8213,8214	0611077A78	1.5k
R8215	0611077B11	33k
R8216	0611077A44	56
R8217,8218	0611077A78	1.5k
R8220	0611077A44	56
R8221,8222	0611077A78	1.5k
R8224	0611077A78	1.5k
R8225	0611077A44	56
R8226	0611077A78	1.5k
R8228	0611077A44	56
R8229,8230	0611077A78	1.5k
R8231	0611077G88	100k ±1%
R8232,8233	0611077A98	10k
R8236,8237	0611077A98	10k
R8239,8240	0611077A98	10k
R8242,8243	0611077H18	200k ±1%
R8244	0611077G88	100k ±1%
R8245	0611077B23	100k
R8246	0611077G88	100k ±1%
R8247	0611077H18	200k ±1%
R8248	0611077G88	100k ±1%
R8249	0611077H18	200k ±1%
R8250	0611077G88	100k ±1%
R8251 thru 8254	0611077H18	200k ±1%
R8255,8256	0611077B23	100k
R8257	0611077G88	100k ±1%
R8258	0611077H18	200k ±1%
R8259	0611077G88	100k ±1%
R8260	0611077H18	200k ±1%

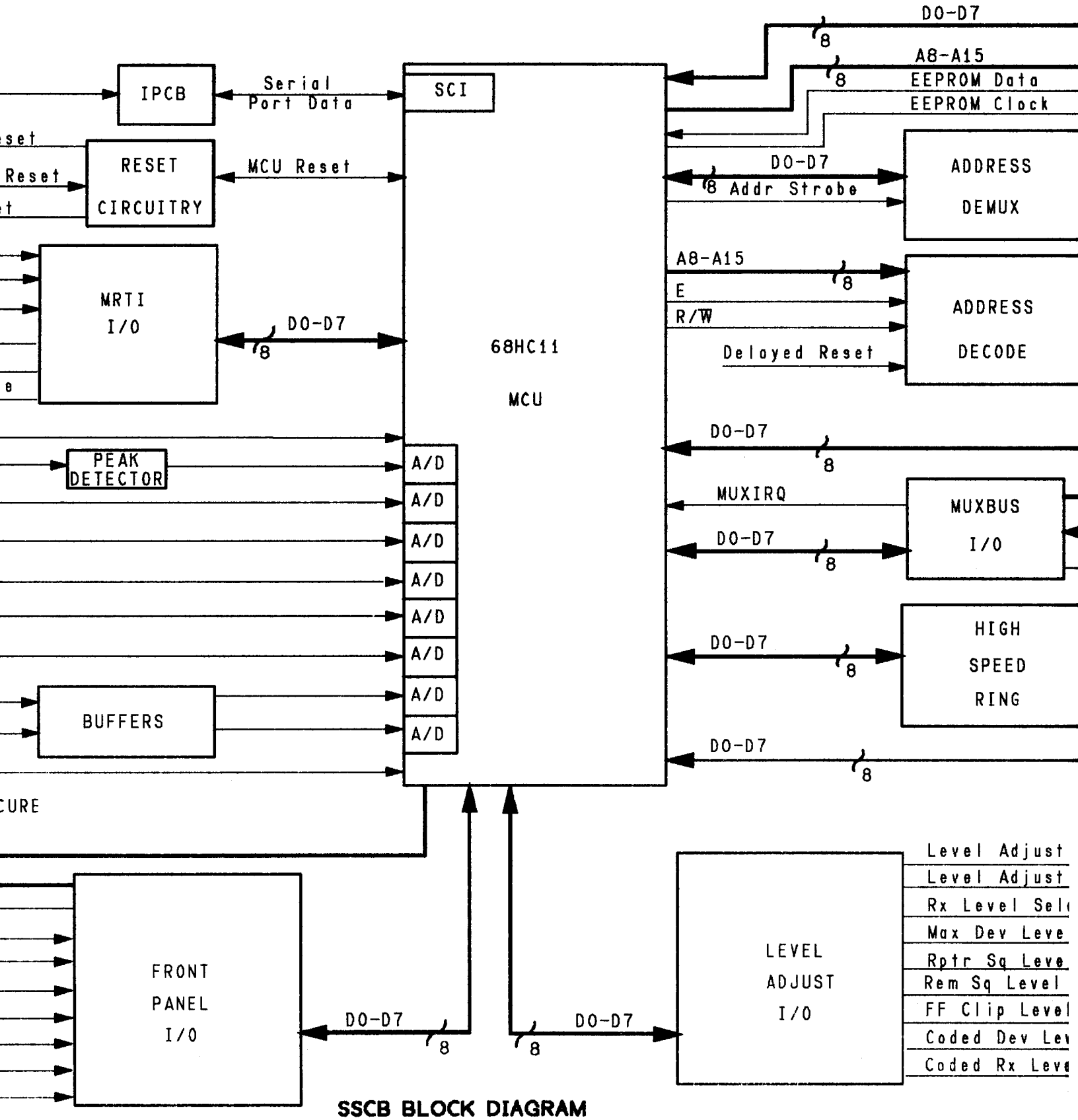
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R8261	0611077G88	100k ±1%
R8262,8263	0611077H18	200k ±1%
R8264,8265	0611077A98	10k
R8272	0611077G88	100k ±1%
R8275	0611077H85	1 meg ±1%
R8276	0611077H30	267k ±1%
R8277	0611077A98	10k
R8278	0611077H50	432k ±1%
R8279	0611077H26	243k ±1%
R8280	0611077H43	365k ±1%
R8281	0611077B13	39k
R8282,8283	0611077H85	1 meg ±1%
R8284	0611077H30	267k ±1%
R8285	0611077H50	432k ±1%
R8286	0611077A98	10k
R8287	0611077A74	1k
R8288	0611077H26	243k ±1%
R8289	0611077H85	1 meg ±1%
R8290	0611077H43	365k ±1%
R8291	0611077B13	39k
R8292	0611077A86	3.3k
R8293	0611077B23	100k
R8294	0611077B11	33k
R8295	0611077A98	10k
R8300	0611077B23	100k
R8302	0611077B23	100k
R8303	0611077B47	1 meg
R8310 thru 8313	0611077B15	47k
R8314	0611077A98	10k
R8315	0611077A94	6.8k
R8316	0611077A98	10k
R8318	0611077B23	100k
R8319	0611077B11	33k
R8320	0611077B23	100k
R8321	0611077B47	1 meg
R8335 thru 8339	0611077A74	1k
R8340	0611077A98	10k
R8344	0611077A68	560
R8345 thru 8347	0611077A50	100
R8348	0611077A98	10k
R8349	0611077B30	200k
R8350	0611077B03	15k
		switch:
SW800,801	4083980R04	spdt toggle
SW802	4083980R05	spdt toggle
		test point:
TP1 thru 10	2910271A15	pin terminal
		integrated circuit: (see note)
U700	5184320A51	quad comparator
U800	5197024A01	8-bit MCU
U801,802	5184494R03	HCMOS ASIC
U804	5184944N51	8k x 8 RAM
U806	5183222M10	quad operational amplifier
U807	5184320A35	timer
U810 thru 812	5184887K60	analog multiplexer/demultiplexer
U813	5184704M19	hex level shifter
U814	5184621K32	quad operational amplifier
U816	5184704M19	hex level shifter
U817	5184887K73	quad bilateral switch
U818,819	5184621K32	quad operational amplifier
U821	5184621K32	quad operational amplifier
U824	5182798R70	digital control potentiometer
U830	5184621K33	1/2 W audio amplifier
U831	5182798R70	digital control potentiometer
U837,838	5184621K85	dual operational amplifier
U1550,1551	5183222M03	quad operational amplifier
U1552	5183222M10	quad operational amplifier
U1553,1554	5182798R70	digital control amplifier
U8200	5184621K32	quad operational amplifier
		voltage regulator: (see note)
VR700	4883461E27	Zener: 6V
VR701	4883461E40	Zener: 5.1V
VR702	4882256C26	Zener: 3.3V
VR1531 thru 1534	4882256C26	Zener: 3.3V
		crystal:
Y800	4880113K04	7.9488 MHz
		non-referenced items
	0210971A16	NUT, machine: M3 x 0.5; for Q700
	0310945A11	SCREW, tapping: P3.12 x 1.27 x 8; 2 used for J800
	0383497N04	SCREW, machine: M3 x 0.5 x 8; for Q700
	0982449T01	SOCKET, 52-contact: for U800
	0982449T03	SOCKET, 84-contact: for U801,802
	0982808R02	SSOCKET, 8-contact: for U808
	0982808R10	SOCKET, 28-contact: for U803
	0983729M17	CONNECTOR, female: 20-contact; 2 used for J800
	0984181L01	JUMPER, shorting: 2-contact 12 used for JU1-JU12
	1483820M03	INSULATOR, heat conductive: for Q700
	1584576N01	SHROUD, fuse: for F700
	2683192N02	HEAT SINK: for Q700
	2982906N01	TERMINAL, fuse: 2 used for F700
	4380054K02	SPACER, PCB support: 4 used
	5483865R01	LABEL, bar code
	7505295B01	PAD, crystal base

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

SECURE CAPABLE STATION CONTROL BOARD

BLOCK DIAGRAM

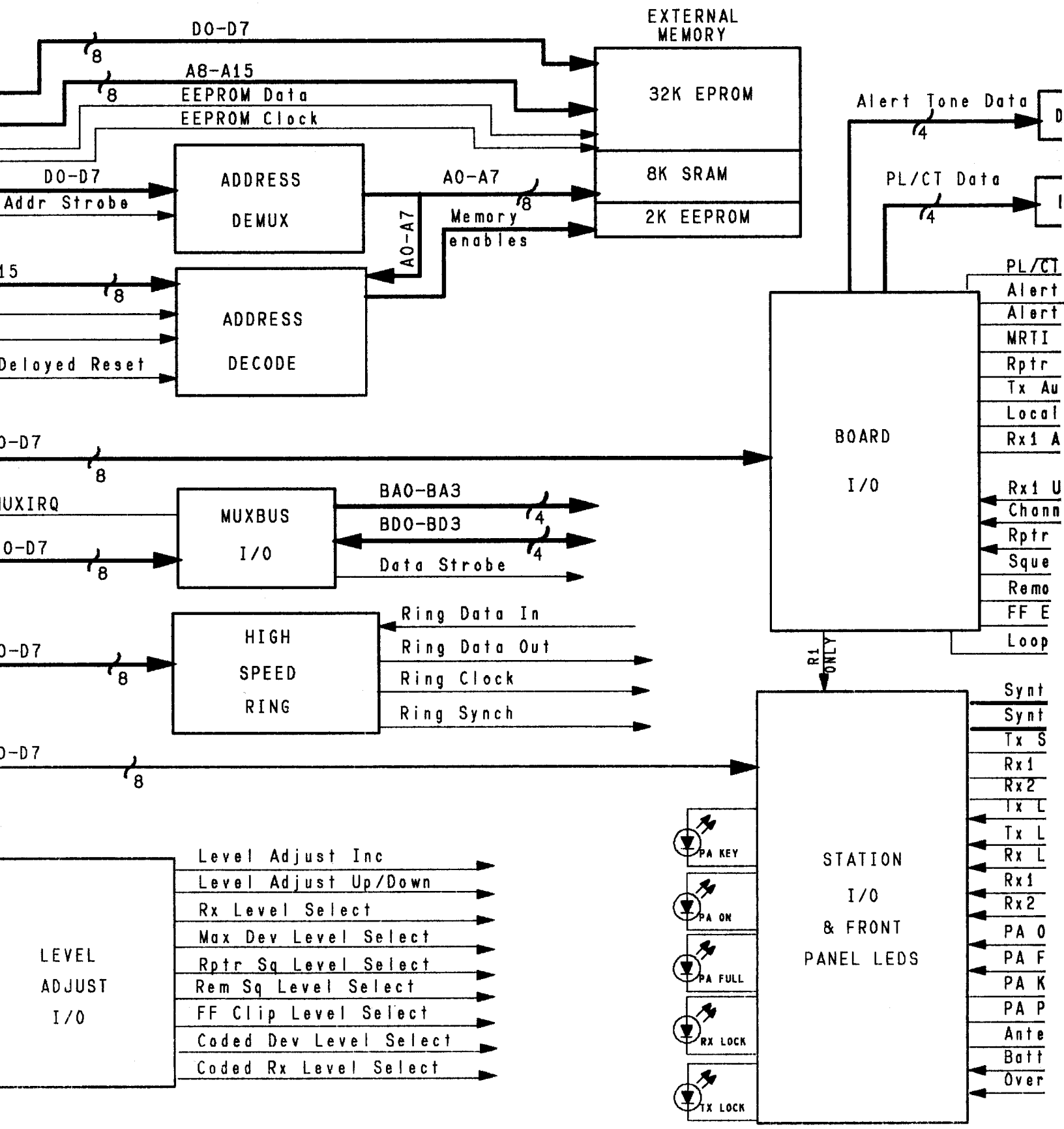


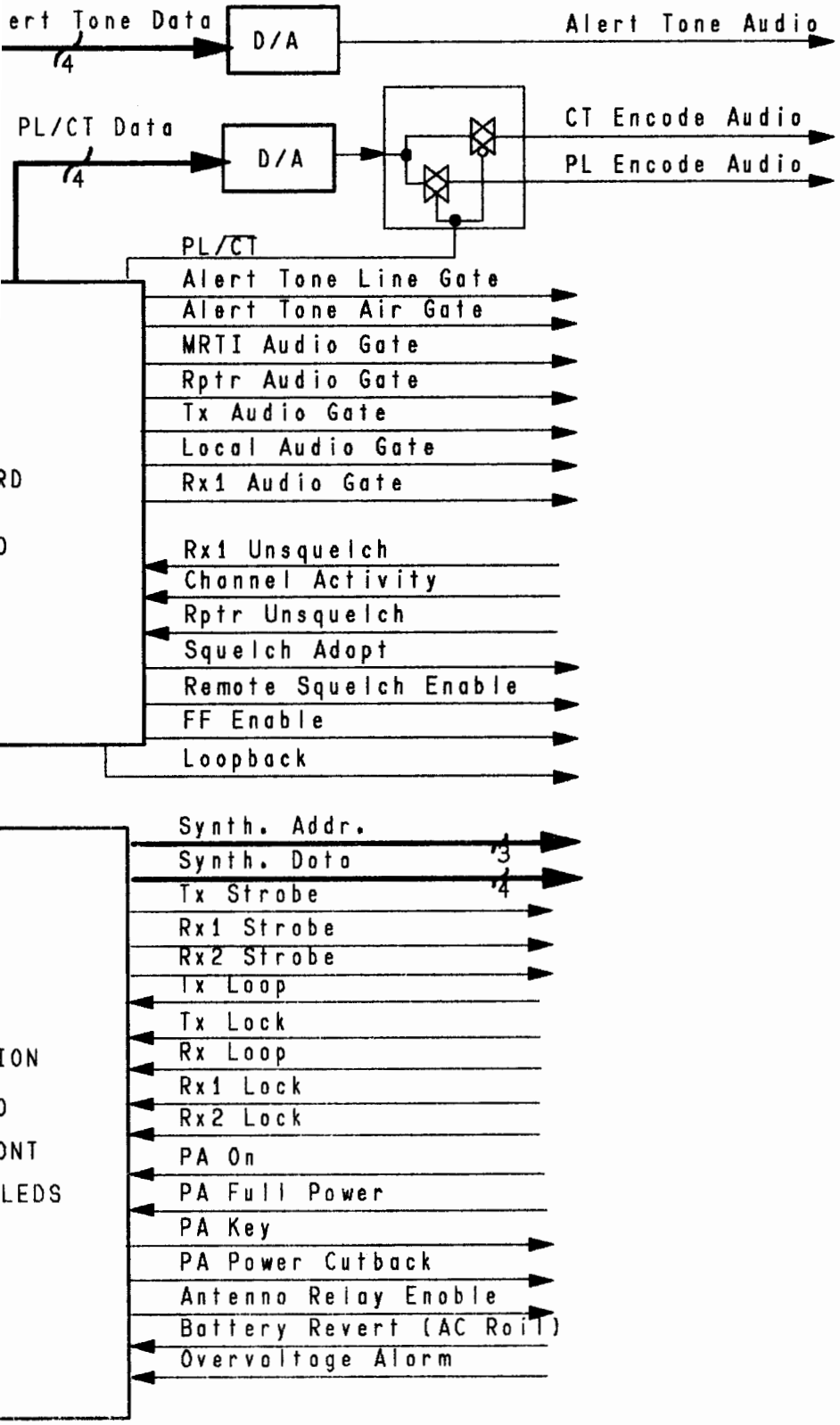


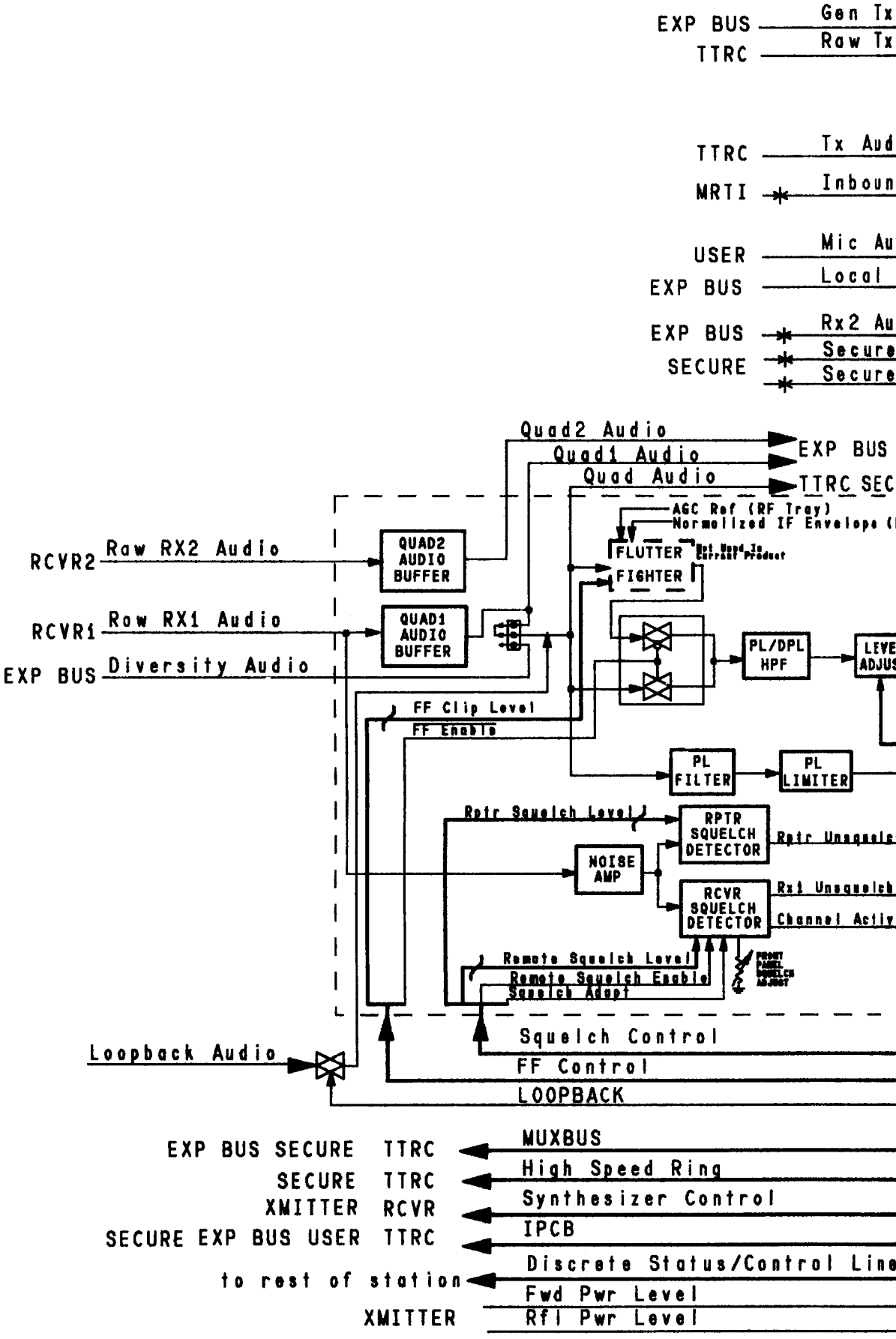
SSCB BLOCK DIAGRAM

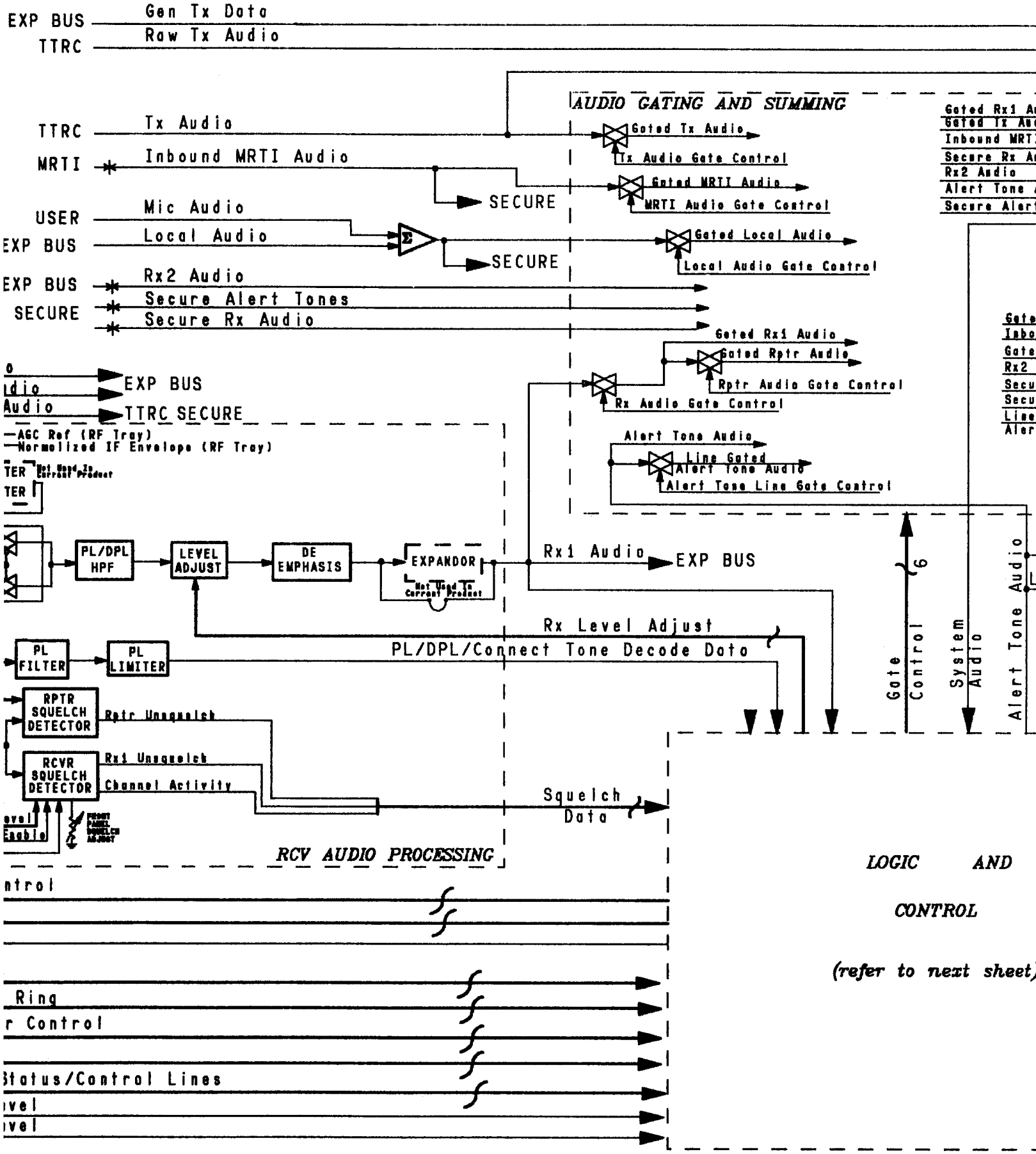
TEPS-47645-0

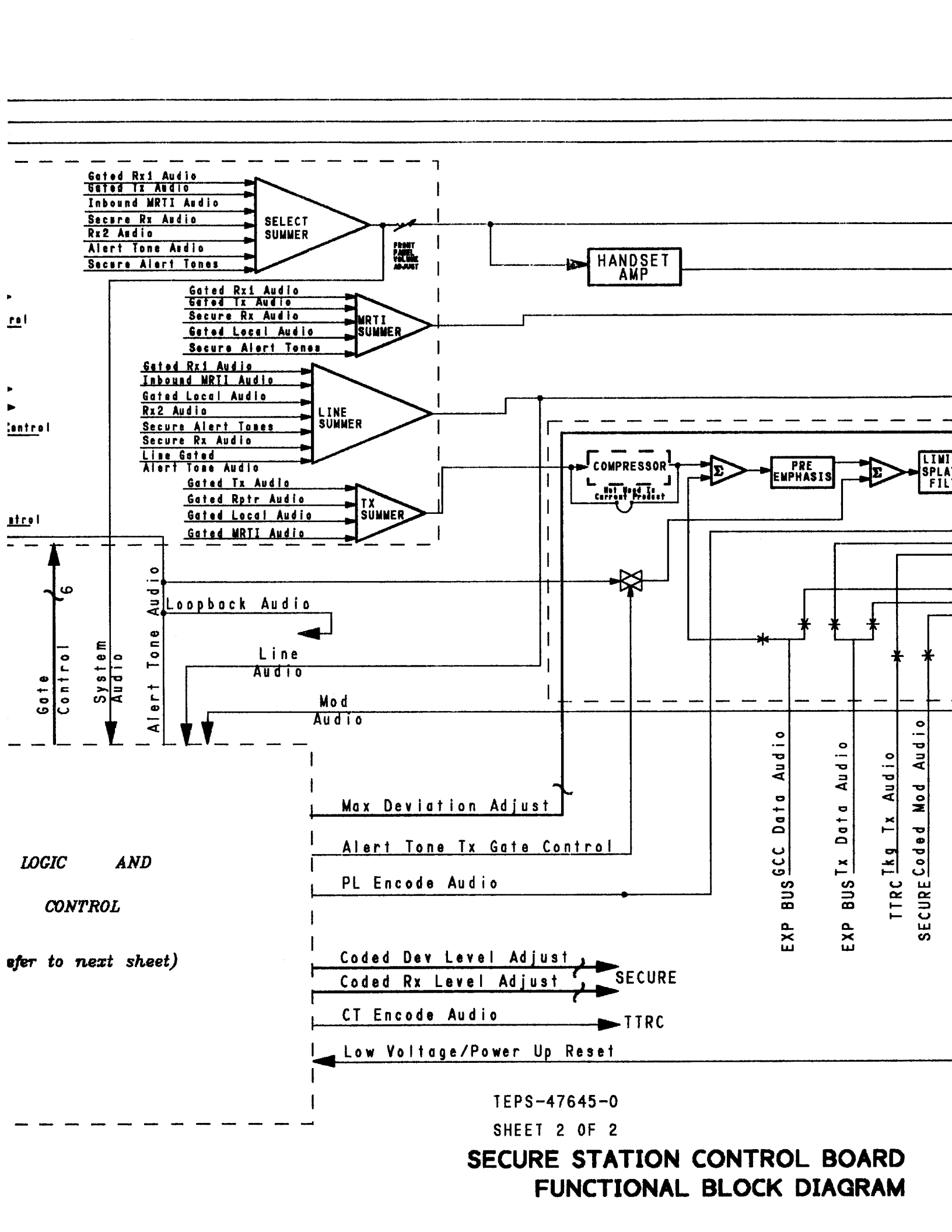
SHEET 1 OF 2


EXTERNAL MEMORY
D0-D7
8
A8-A15
8
EEPROM Data
EEPROM Clock
32K EPROM
8K SRAM
2K EEPROM
D0-D7
Addr Strobe
ADDRESS DEMUX
A0-A7
8
A0-A7
Memory enables
15
8
ADDRESS DECODE
Delayed Reset
Alert Tone Data
4
PL/CT Data
4
PL/CT
Alert
Alert
MRTI
Rptr
Tx Au
Local
Rx1 A
BOARD I/O
Rx1 U
Chann
Rptr
Sque
Remo
FF E
Loop
D-D7
8
MUXIRQ
D0-D7
8
MUXBUS I/O
BA0-BA3
4
BD0-BD3
4
Data Strobe
R1 ONLY
D-D7
8
HIGH SPEED RING
Ring Data In
Ring Data Out
Ring Clock
Ring Synch
D-D7
8
Synt
Synt
Tx S
Rx1
Rx2
Tx L
Tx L
Rx L
Rx1
Rx2
PA 0
PA F
PA K
PA P
Ante
Batt
Over
PA KEY
PA ON
PA FULL
RX LOCK
TX LOCK
STATION I/O & FRONT PANEL LEDS
LEVEL ADJUST I/O
Level Adjust Inc
Level Adjust Up/Down
Rx Level Select
Max Dev Level Select
Rptr Sq Level Select
Rem Sq Level Select
FF Clip Level Select
Coded Dev Level Select
Coded Rx Level Select


ert Tone Data
4
D/A
Alert Tone Audio
PL/CT Data
4
D/A
CT Encode Audio
PL Encode Audio
PL/CT
Alert Tone Line Gate
Alert Tone Air Gate
MRTI Audio Gate
Rptr Audio Gate
Tx Audio Gate
Local Audio Gate
Rx1 Audio Gate
RD
D
Rx1 Unsquelch
Channel Activity
Rptr Unsquelch
Squelch Adopt
Remote Squelch Enable
FF Enable
Loopback
Synth. Addr.
Synth. Data
3
4
Tx Strobe
Rx1 Strobe
Rx2 Strobe
Tx Loop
Tx Lock
Rx Loop
Rx1 Lock
Rx2 Lock
PA On
PA Full Power
PA Key
PA Power Cutback
Antenna Relay Enable
Battery Revert (AC Roll)
Overvoltage Alarm
ION
D
ONT
LEDS


EXP BUS
Gen Tx
TTRC
Raw Tx
TTRC
Tx Aud
MRTI
Inboun
USER
Mic Au
EXP BUS
Local
EXP BUS
Rx2 Au
SECURE
Secure
Secure
Quad2 Audio
EXP BUS
Quad1 Audio
Quad Audio
TTRC SEC
AGC Ref (RF Tray)
Normalized IF Envelope
RCVR2
Raw RX2 Audio
QUAD2 AUDIO BUFFER
FLUTTER
FIGHTER
RCVR1
Raw RX1 Audio
QUAD1 AUDIO BUFFER
EXP BUS
Diversity Audio
PL/DPL HPF
FF Clip Level
FF Enable
PL FILTER
PL LIMITER
Rptr Squelch Level
RPTR SQUELCH DETECTOR
NOISE AMP
RCVR SQUELCH DETECTOR
Rx1 Unsquelch
Channel Activ
Remote Squelch Level
Remote Squelch Enable
Squelch Adapt
Loopback Audio
Squelch Control
FF Control
LOOPBACK
EXP BUS SECURE TTRC
MUXBUS
SECURE TTRC
High Speed Ring
XMITTER RCVR
Synthesizer Control
SECURE EXP BUS USER TTRC
IPCB
to rest of station
Discrete Status/Control Line
Fwd Pwr Level
XMITTER
Rfl Pwr Level

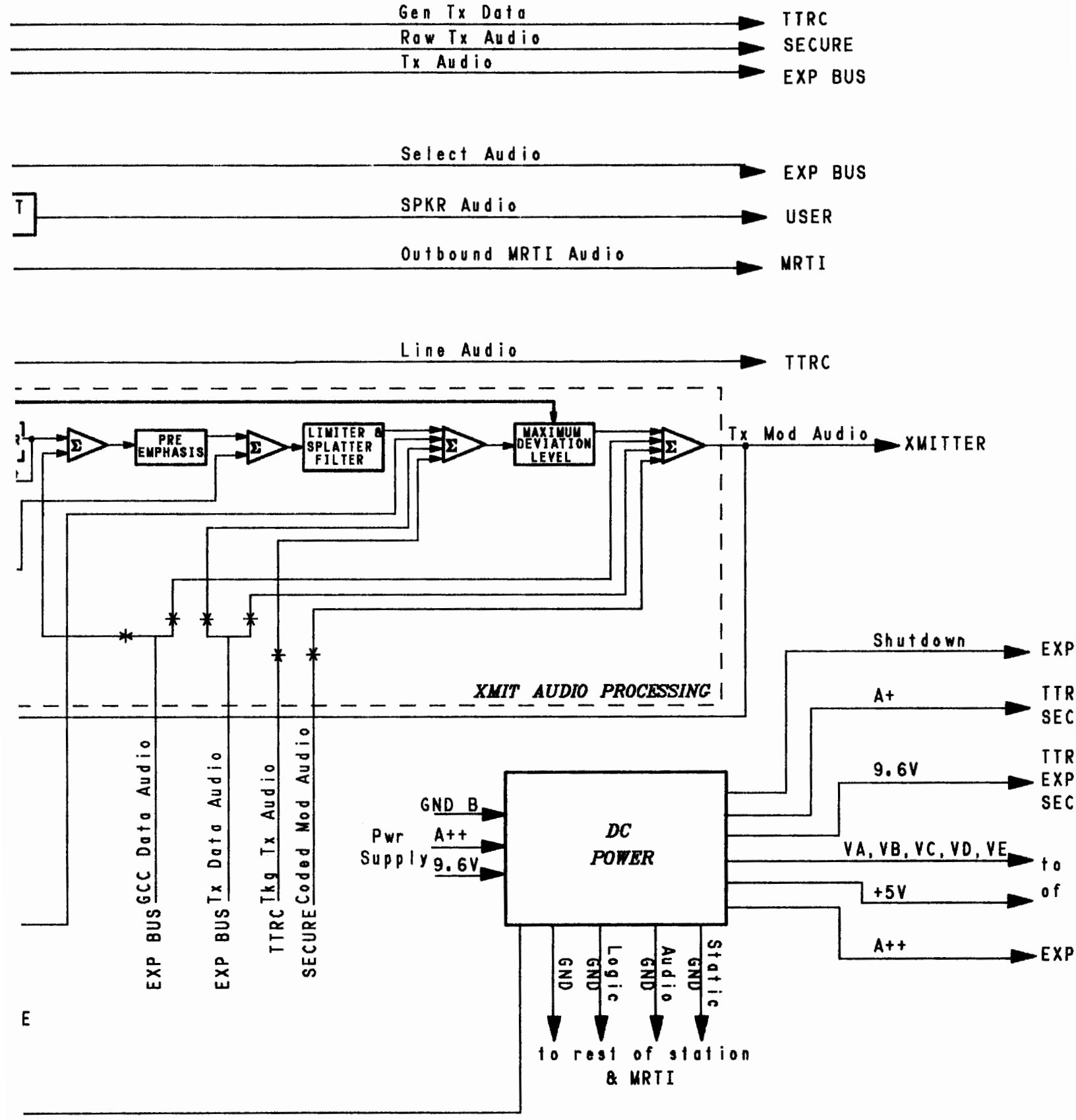

EXP BUS
Gen Tx Data
TTRC
Raw Tx Audio
AUDIO GATING AND SUMMING
TTRC
Tx Audio
Gated Tx Audio
Tx Audio Gate Control
MRTI
Inbound MRTI Audio
SECURE
Gated MRTI Audio
MRTI Audio Gate Control
USER
Mic Audio
EXP BUS
Local Audio
SECURE
Gated Local Audio
Local Audio Gate Control
EXP BUS
Rx2 Audio
SECURE
Secure Alert Tones
Secure Rx Audio
Gated Rx1 Audio
Gated Rptr Audio
Rptr Audio Gate Control
Rx Audio Gate Control
EXP BUS
TTRC SECURE
Alert Tone Audio
Line Gated
Alert Tone Audio
Alert Tone Line Gate Control
AGC Ref (RF Tray)
Normalized IF Envelope (RF Tray)
PL/DPL HPF
LEVEL ADJUST
DE EMPHASIS
EXPANDOR
Rx1 Audio
EXP BUS
Rx Level Adjust
PL/DPL/Connect Tone Decode Data
PL FILTER
PL LIMITER
RPTR SQUELCH DETECTOR
Rptr Unsquelch
RCVR SQUELCH DETECTOR
Rx1 Unsquelch
Channel Activity
Squelch Data
RCV AUDIO PROCESSING
Gate Control
System Audio
Alert Tone Audio
LOGIC AND
CONTROL
(refer to next sheet)
Ring
Control
Status/Control Lines



TEPS-47645-0

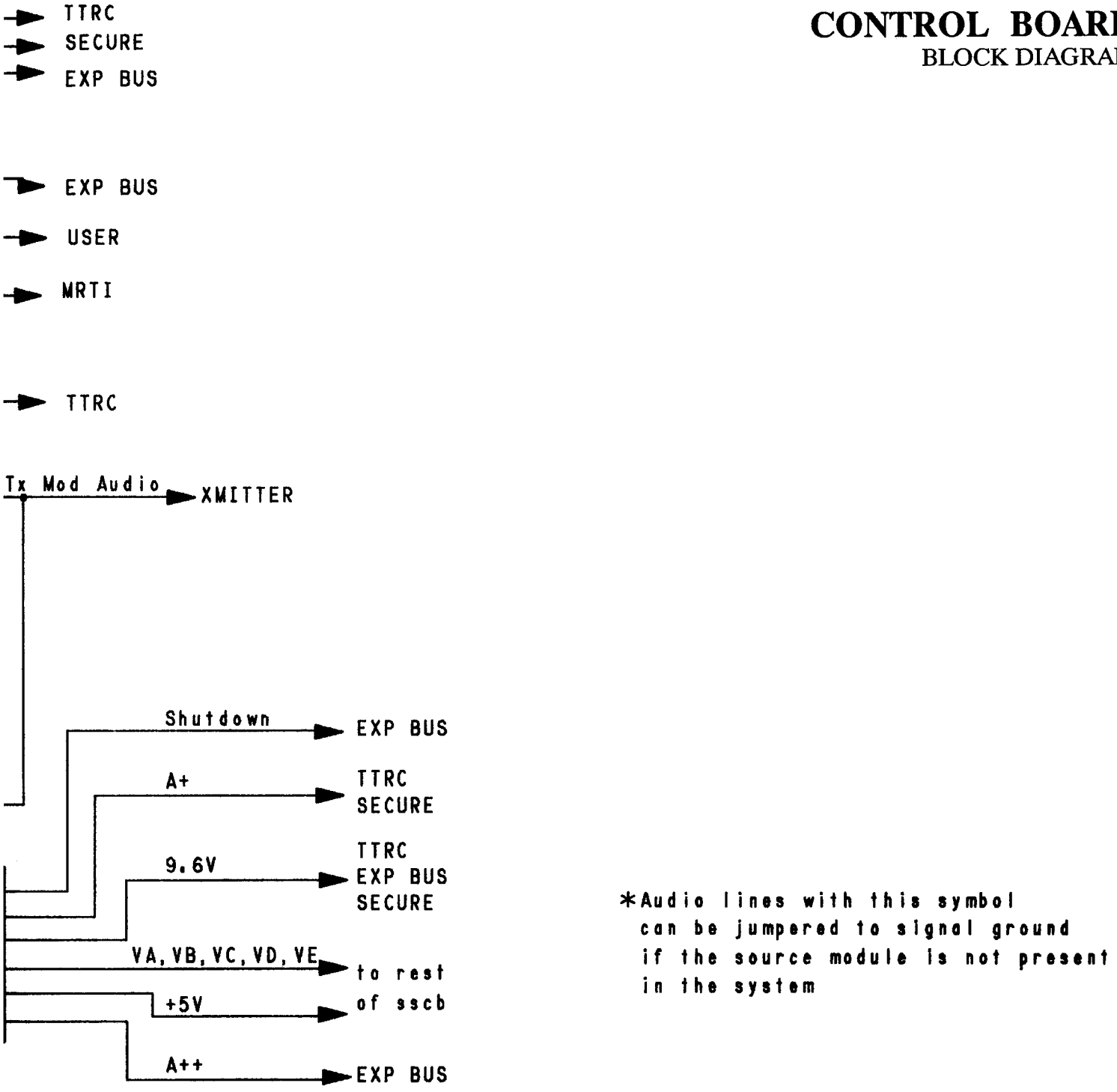
SHEET 2 OF 2

SECURE STATION CONTROL BOARD FUNCTIONAL BLOCK DIAGRAM



N CONTROL BOARD
L BLOCK DIAGRAM

SECURE CAPABLE STATION CONTROL BOARD
BLOCK DIAGRAM

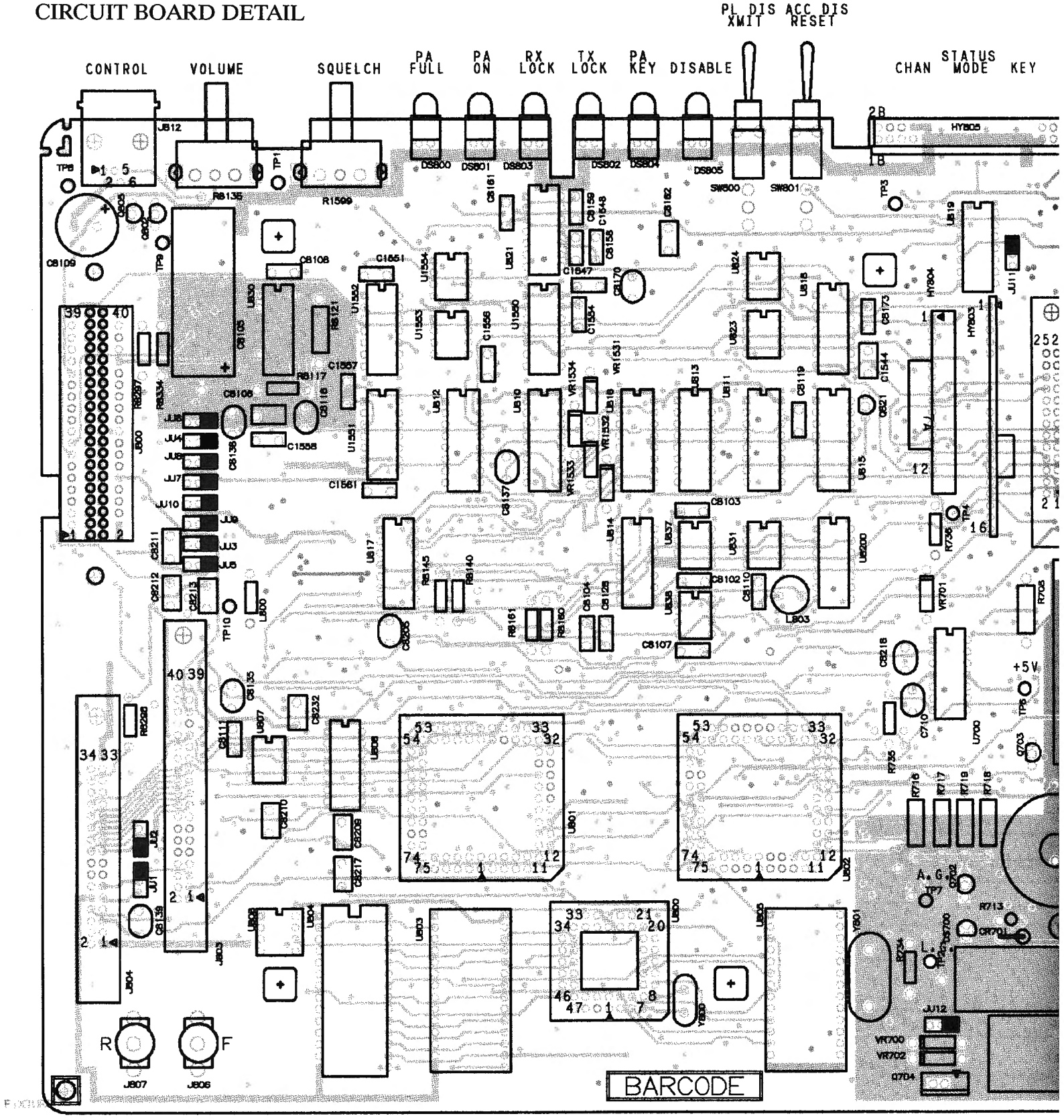


*Audio lines with this symbol can be jumpered to signal ground if the source module is not present in the system

on

SECURE CAPABLE STATION CONTROL BOARD

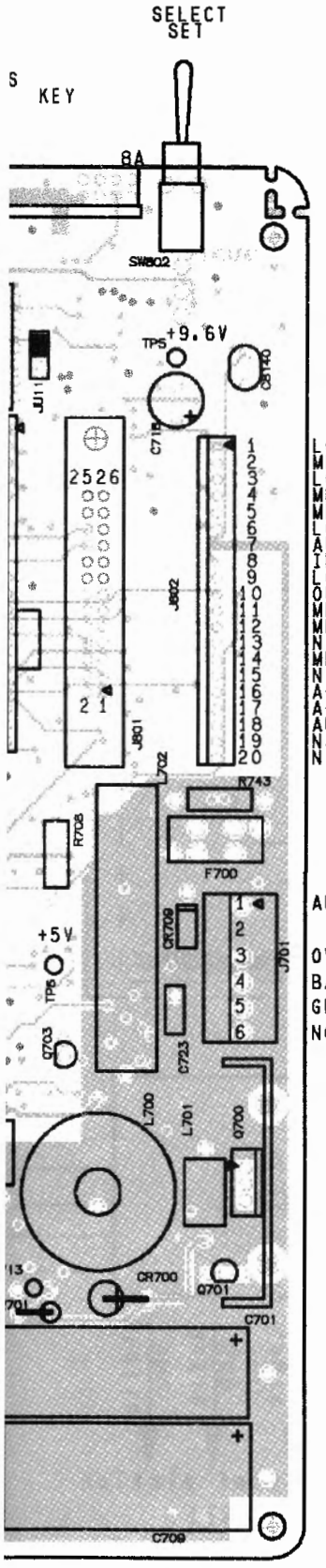
CIRCUIT BOARD DETAIL



SHOWN FROM COMPONENT SIDE

0L-TEPS-47334-0
BD-TEPS-47335-0

NOTE:
AN AS
SIGNA
LO



NOTE:
AN ASTERISK (*) FOLLOWING A SIGNAL NAME INDICATES AN ACTIVE LOW LEVEL SIGNAL

J800

QUAD 1 AUDIO	39	40	AUDIO GND
AUDIO GND	37	38	RX1 AUDIO
RX2 AUDIO	35	36	TX AUDIO
LOCAL AUDIO	33	34	TX DATA AUDIO
GCC DATA AUDIO	31	32	SELECT AUDIO
QUAD 2 AUDIO	29	30	DIVERSITY AUDIO
AUDIO SPARE	27	28	GEN TX DATA +
LOGIC SPARE	25	26	AUDIO SPARE
SHUT DOWN	23	24	LOGIC SPARE
LOGIC GND	21	22	DS*
BD2*	19	20	BD3*
BD0*	17	18	BD1*
BA2	15	16	BA3
BA0	13	14	BA1
IPCB	11	12	EXPANSION RESET*
AUDIO GND	9	10	AUDIO GND
AUDIO GND	7	8	AUDIO GND
A++	5	6	AUDIO GND
A++	3	4	A++
A++	1	2	A++

J801

TX STROBE	26	25	RX1 STROBE
SA0	24	23	SD3
SA1	22	21	SD2
SA2	20	19	SD1
TX LOOP	18	17	SD0
PA POWER CUTBACK*	16	15	RX1 LOCK*
PA KEY*	14	13	RX1 LOOP
PA ON*	12	11	AGC REF(800/896)
PA FULL POWER*	10	9	RX2 STROBE
TX LOCK*	8	7	ANTENNA RELAY ENABLE*
RAW RX2 AUDIO	6	5	RAW RX1 AUDIO
AUDIO GND (GND A)	4	3	TX MOD AUDIO
RX2 LOCK*	2	1	+9.6V

J803

AUDIO GND	40	39	+5V
N.C.	38	37	KEY BATTERY GND
N.C.	36	35	CODED RX LEVEL*
SECURE ALERT TONES	34	33	EXPANSION RESET*
CODED MOD LEVEL*	32	31	LEVEL INC
LEVEL U/D*	30	29	IPCB
IN MRTI AUDIO	28	27	QUAD AUDIO
N.C.	26	25	DS*
BA0	24	23	BA1
BA2	22	21	BA3
BD0*	20	19	BD1*
BD2*	18	17	BD3*
LOGIC GND	16	15	HSR SYN
LOGIC GND	14	13	HSR CLOCK
LOGIC GND	12	11	HSR TO SECURE
LOGIC GND	10	9	HSR IN
LOCAL AUDIO	8	7	CODED MOD AUDIO
RAW TX AUDIO	6	5	TX AUDIO
SECURE RX AUDIO	4	3	+9.6V
AUDIO GND	2	1	AUDIO GND

J804

AUDIO GND	34	33	+5V
A+	32	31	+5V
GEN TX DATA+	30	29	MUTE
EXPANSION RESET*	28	27	CONNECT TONE AUDIO
IPCB	26	25	DS*
BA0	24	23	BA1
BA2	22	21	BA3
BD0*	20	19	BD1*
BD2*	18	17	BD3*
LOGIC GND	16	15	HSR SYN
LOGIC GND	14	13	HSR CLOCK
LOGIC GND	12	11	HSR FROM TTRC
LOGIC GND	10	9	HSR OUT
QUAD AUDIO	8	7	TKG MOD AUDIO
RAW TX AUDIO	6	5	TX AUDIO
LINE AUDIO	4	3	9.6V
AUDIO GND	2	1	A+

J812

IPCB	6	5	SPKR AUDIO
MIC PTT*	4	3	MIC AUDIO
AUDIO GROUND	2	1	LOGIC GROUND

TRANSISTOR DETAILS
(TOP VIEW)

4800869642
4800869328
4800869643
4811043C05

4811043C26
4811043C06

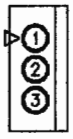
1 -EMITTER
2 -BASE
3 -COLLECTOR

4811043C37
4800869653

BLE*

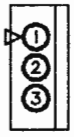
1 -DRAIN
2 -SOURCE
3 -GATE

4800869829



1 -EMITTER
2 -COLLECTOR
3 -BASE

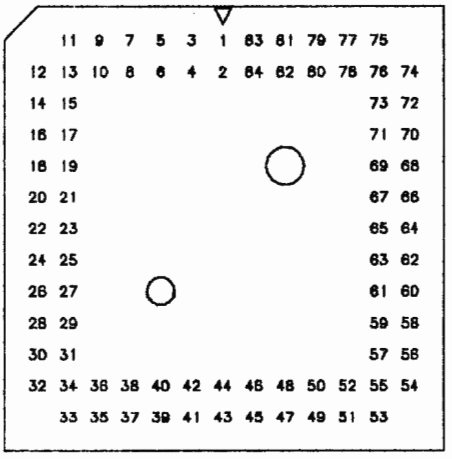
4883875D05



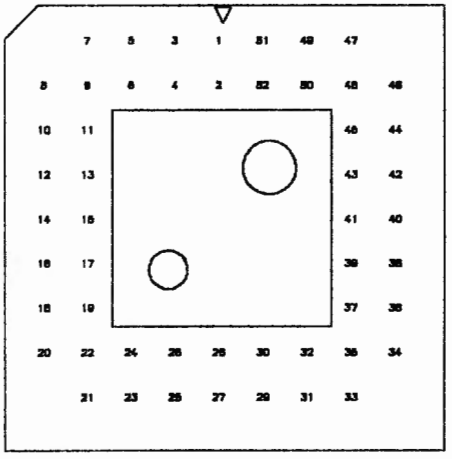
0

1 -CATHODE
2 -ANODE
3 -GATE

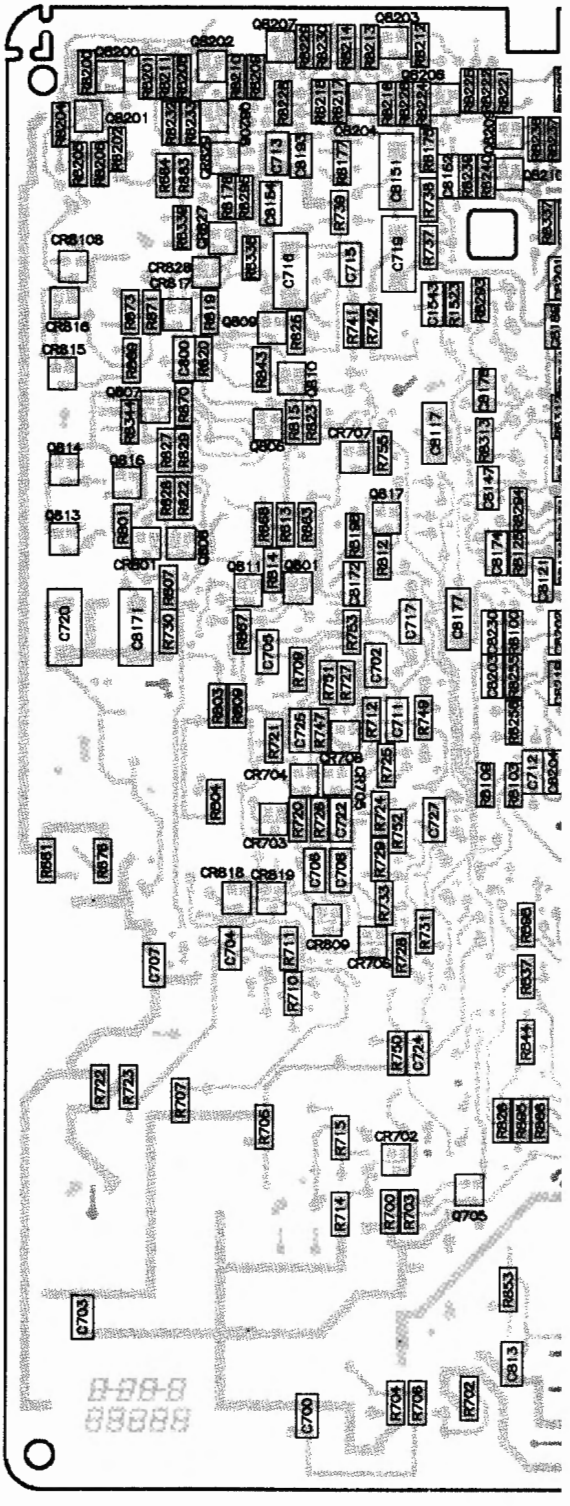
NOTE: SHADED AREA INDICATES
DEFAULT JUMPER POSITION



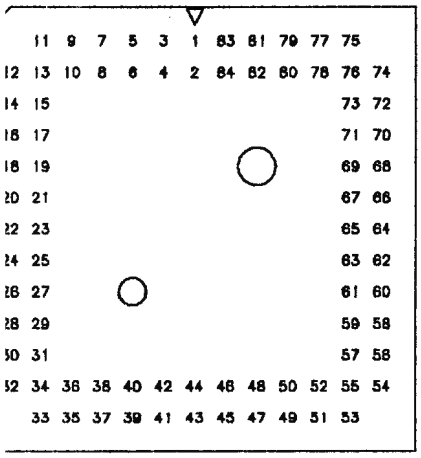
ASIC SOCKET DETAIL



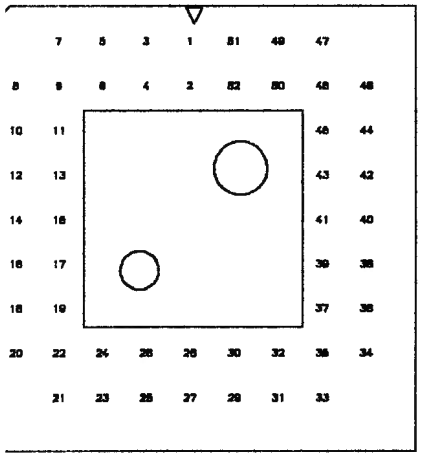
uP SOCKET DETAIL



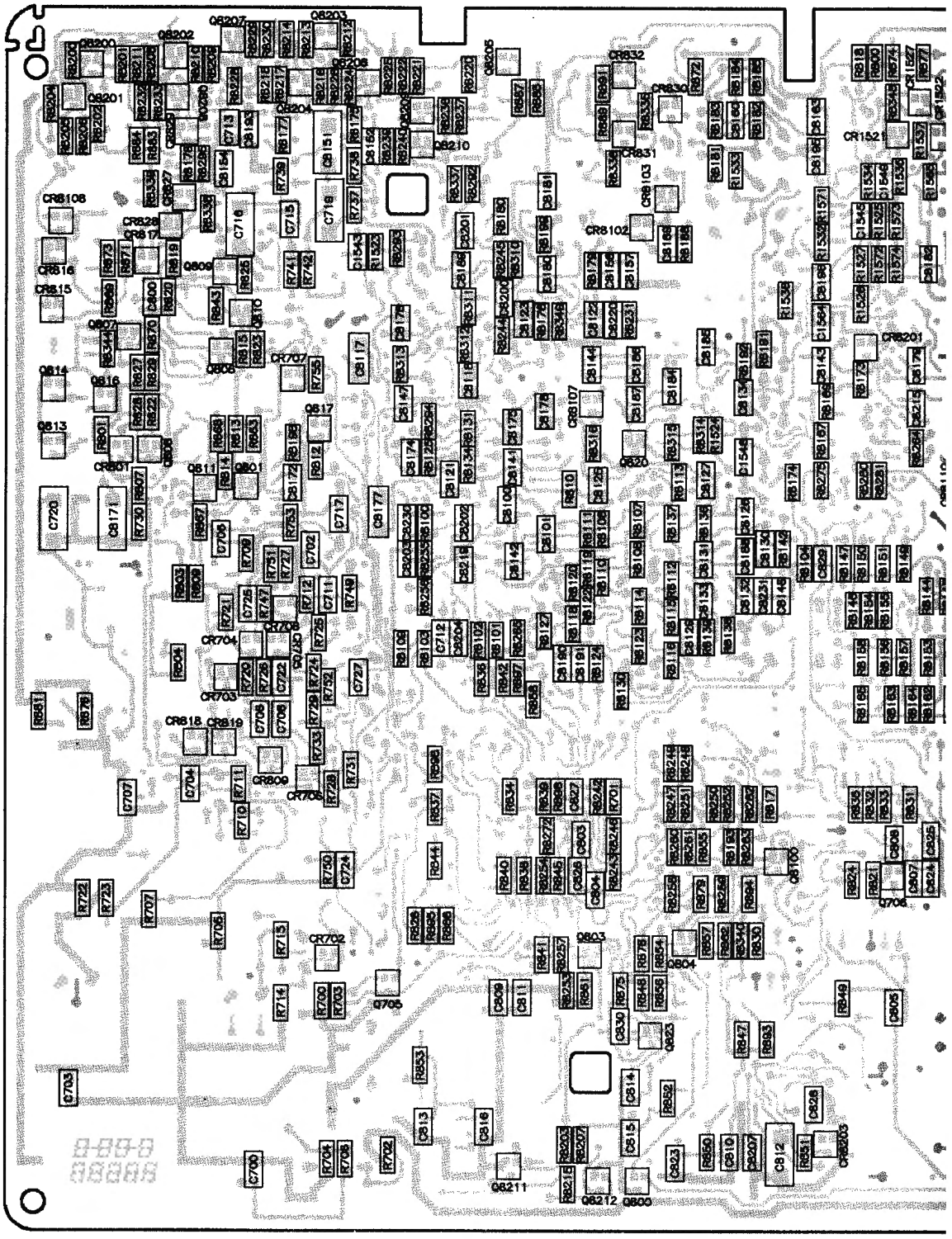
SHOWN FROM SOLDER SIDE



ASIC SOCKET DETAIL

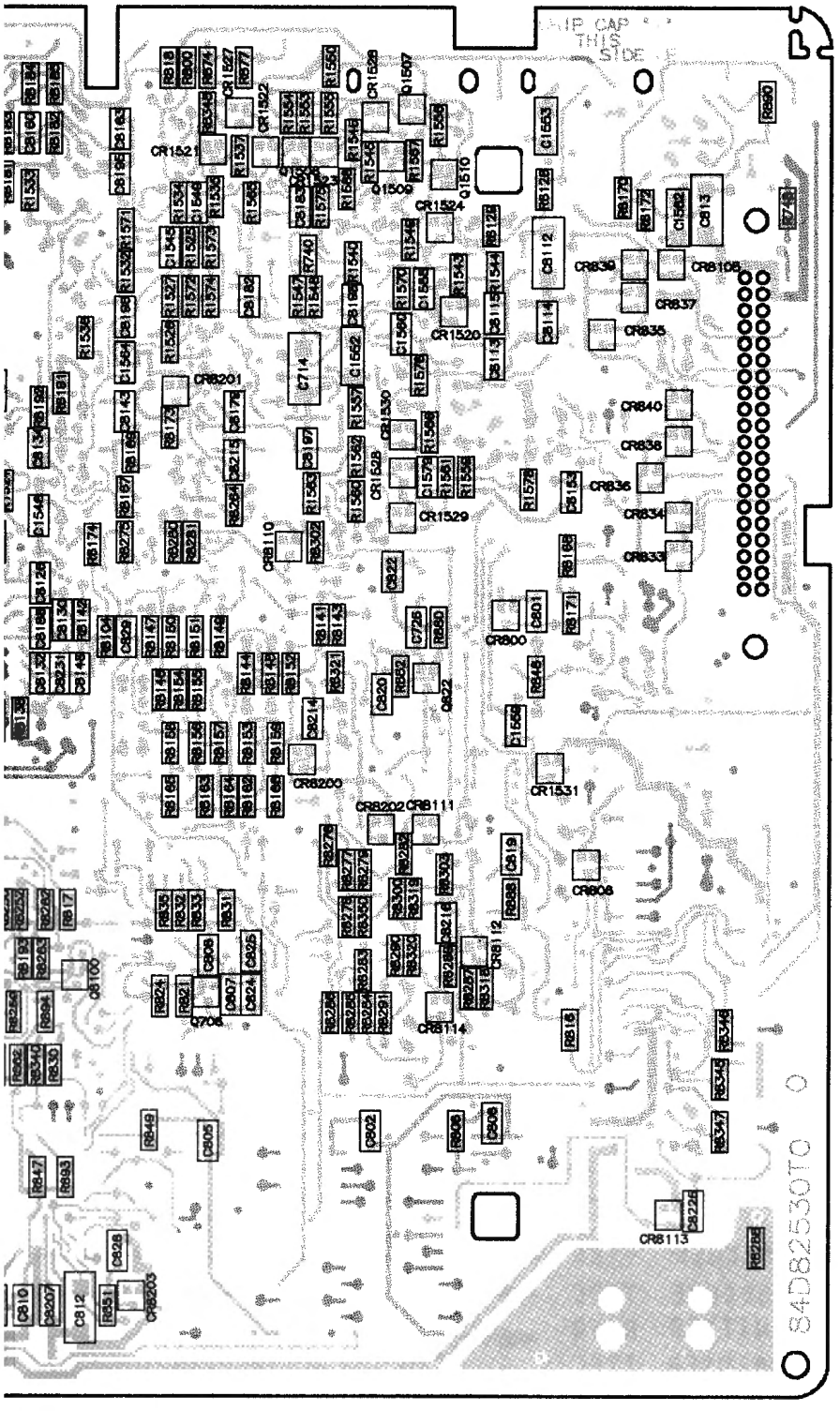


uP SOCKET DETAIL



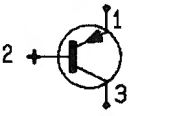
SHOWN FROM SOLDER SIDE

BD-TEPS-47336-0
OL-TEPS-47337-0



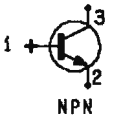
·47336-0

·47337-0



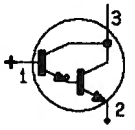
PNP

481105A08
481105B08
481105C08



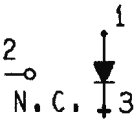
NPN

4811056A03
4811056B03
4811056C03
4811056C21



DARLINGTON NPN

4811056A23
4811056B23
4811056C23

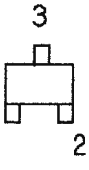


DIODE

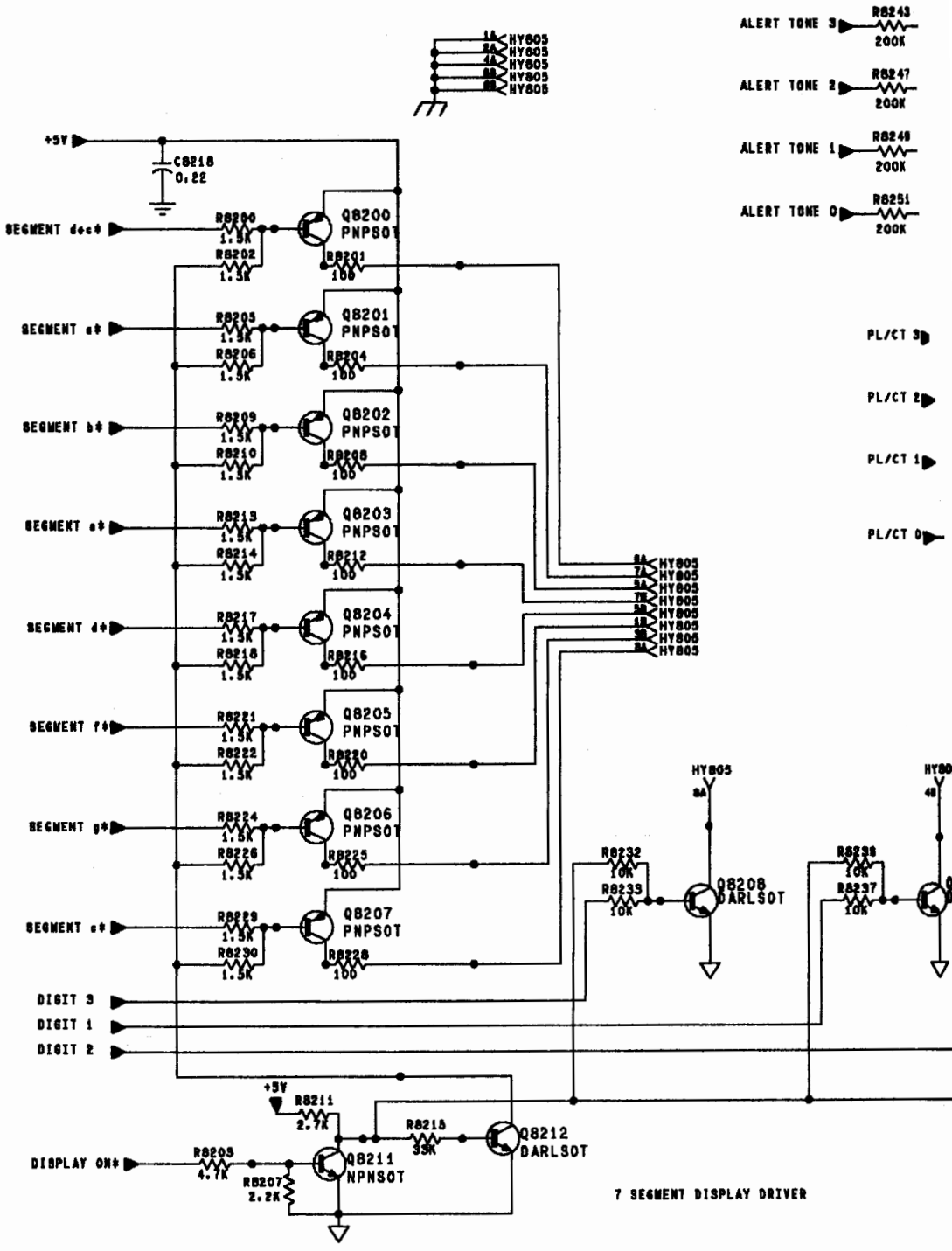
4811058A11
4811058B11
4811058C11
4805129M41
4811058A04
4811058B04
4811058C04

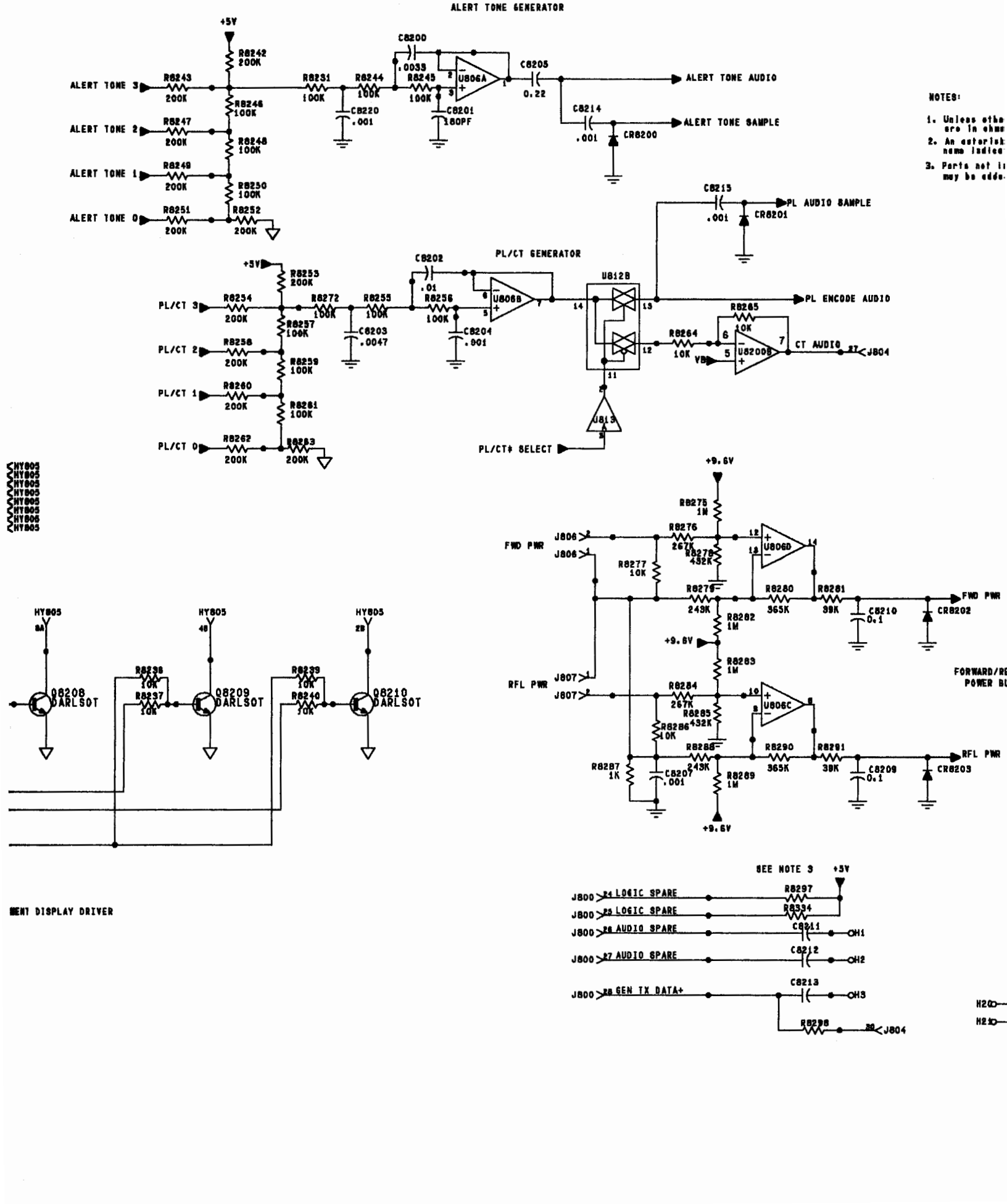
DUAL DIODE

4884336R03



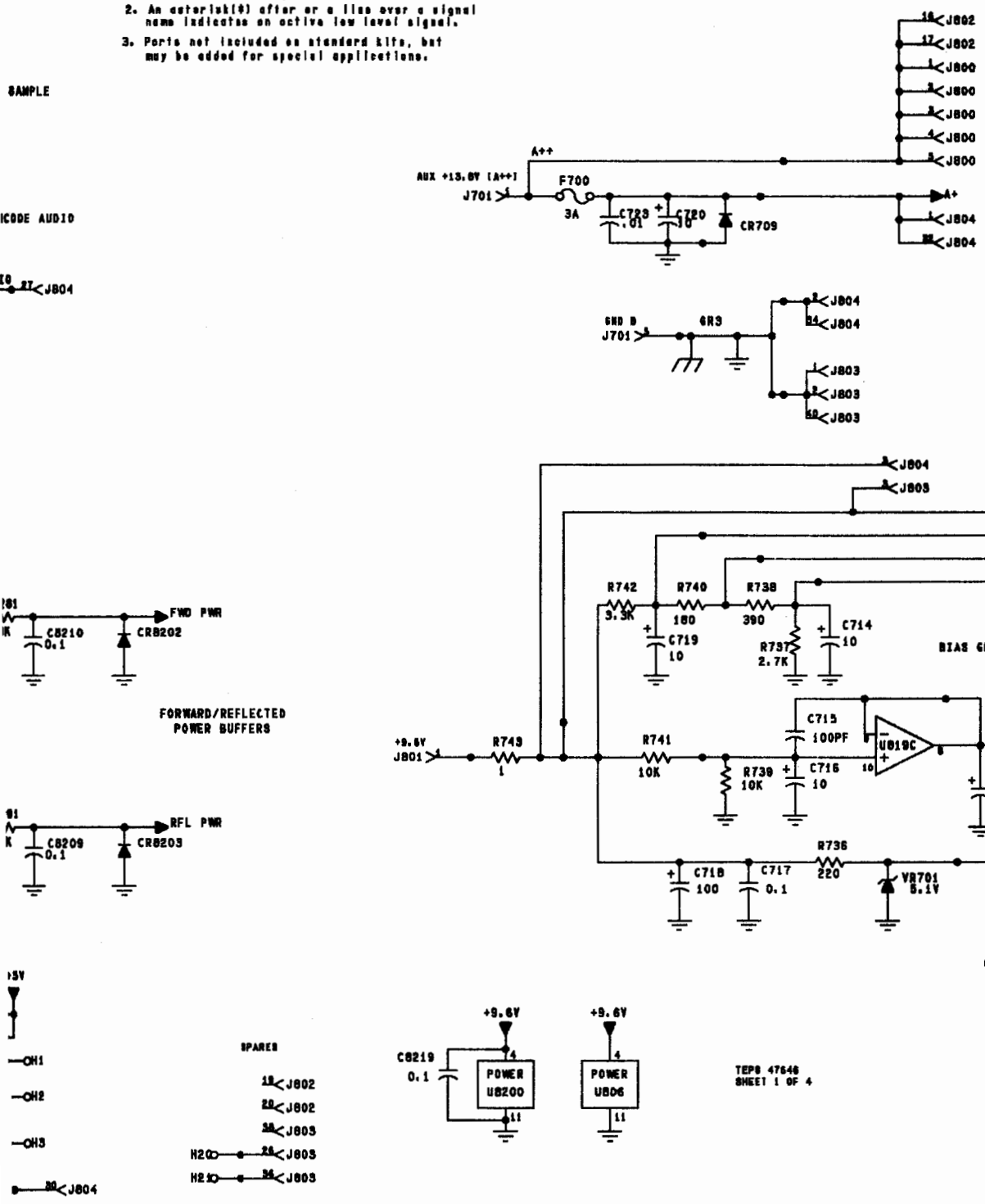
STANDARD SOT
PACKAGE PIN-OUT

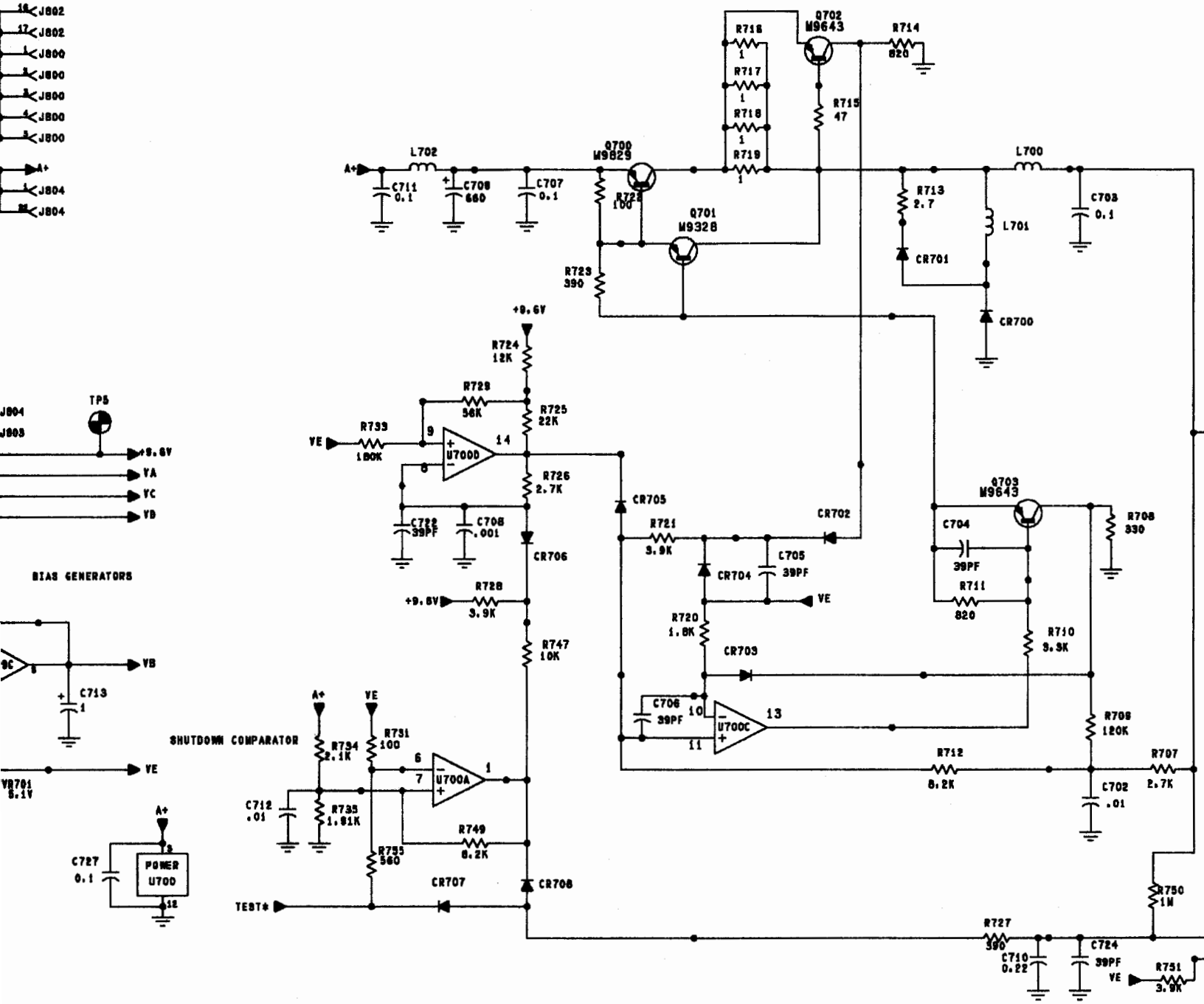

ALERT TONE 3
R8243
200K
ALERT TONE 2
R8247
200K
ALERT TONE 1
R8249
200K
ALERT TONE 0
R8251
200K
+5V
C8218
0.22
SEGMENT d.c.e
SEGMENT a
SEGMENT b
SEGMENT c
SEGMENT d
SEGMENT f
SEGMENT g
SEGMENT e
Q8200 PNPSOT
Q8201 PNPSOT
Q8202 PNPSOT
Q8203 PNPSOT
Q8204 PNPSOT
Q8205 PNPSOT
Q8206 PNPSOT
Q8207 PNPSOT
1.5K
100
PL/CT 3
PL/CT 2
PL/CT 1
PL/CT 0
HYB05
Q8208 DARLSOT
10K
DIGIT 3
DIGIT 1
DIGIT 2
R8211
2.7K
R8215
33K
Q8212 DARLSOT
DISPLAY ON
R8205
4.7K
R8207
2.2K
Q8211 NPNSOT
7 SEGMENT DISPLAY DRIVER


ALERT TONE GENERATOR
+5V
R8242 200K
ALERT TONE 3
R8243 200K
R8231 100K
R8244 100K
C8200 .0033
R8245 100K
U806A
C8205 0.22
ALERT TONE AUDIO
R8246 100K
C8220 .001
C8201 180PF
C8214 .001
CR8200
ALERT TONE SAMPLE
ALERT TONE 2
R8247 200K
R8248 100K
ALERT TONE 1
R8249 200K
R8250 100K
ALERT TONE 0
R8251 200K
R8252 200K
C8215 .001
CR8201
PL AUDIO SAMPLE
PL/CT GENERATOR
+5V
R8253 200K
C8202 .01
PL/CT 3
R8254 200K
R8272 100K
R8255 100K
R8256 100K
U806B
U812B
PL ENCODE AUDIO
R8265 10K
R8264 10K
VB
U8200B
CT AUDIO
J804
R8257 100K
C8203 .0047
C8204 .001
PL/CT 2
R8258 200K
R8259 100K
PL/CT 1
R8260 200K
R8261 100K
PL/CT 0
R8262 200K
R8263 200K
U813
PL/CT# SELECT
HY805
HY805
HY805
HY805
HY805
HY805
HY806
HY805
+9.6V
R8275 1M
FWD PWR
J806
R8276 267K
R8278 432K
U806D
R8277 10K
R8279 243K
R8280 365K
R8281 39K
C8210 0.1
CR8202
FWD PWR
R8282 1M
+9.6V
R8283 1M
RFL PWR
J807
R8284 267K
R8285 432K
U806C
R8286 10K
R8288 243K
R8290 365K
R8291 39K
C8209 0.1
CR8203
RFL PWR
R8287 1K
C8207 .001
R8289 1M
+9.6V
FORWARD/RE
POWER BL
HY805
8A
HY805
4B
HY805
2B
R8236 10K
R8237 10K
R8239 10K
R8240 10K
Q8208 DARLSOT
Q8209 DARLSOT
Q8210 DARLSOT
SEE NOTE 3
+5V
J800 24 LOGIC SPARE
R8297
J800 25 LOGIC SPARE
R8334
J800 26 AUDIO SPARE
C8211
H1
J800 27 AUDIO SPARE
C8212
H2
J800 28 GEN TX DATA+
C8213
H3
R8298
30
J804
H20
H21
MENT DISPLAY DRIVER
NOTES:
1. Unless othe
are in ohm
2. An asterisk
name indica
3. Parts not i
may be adde

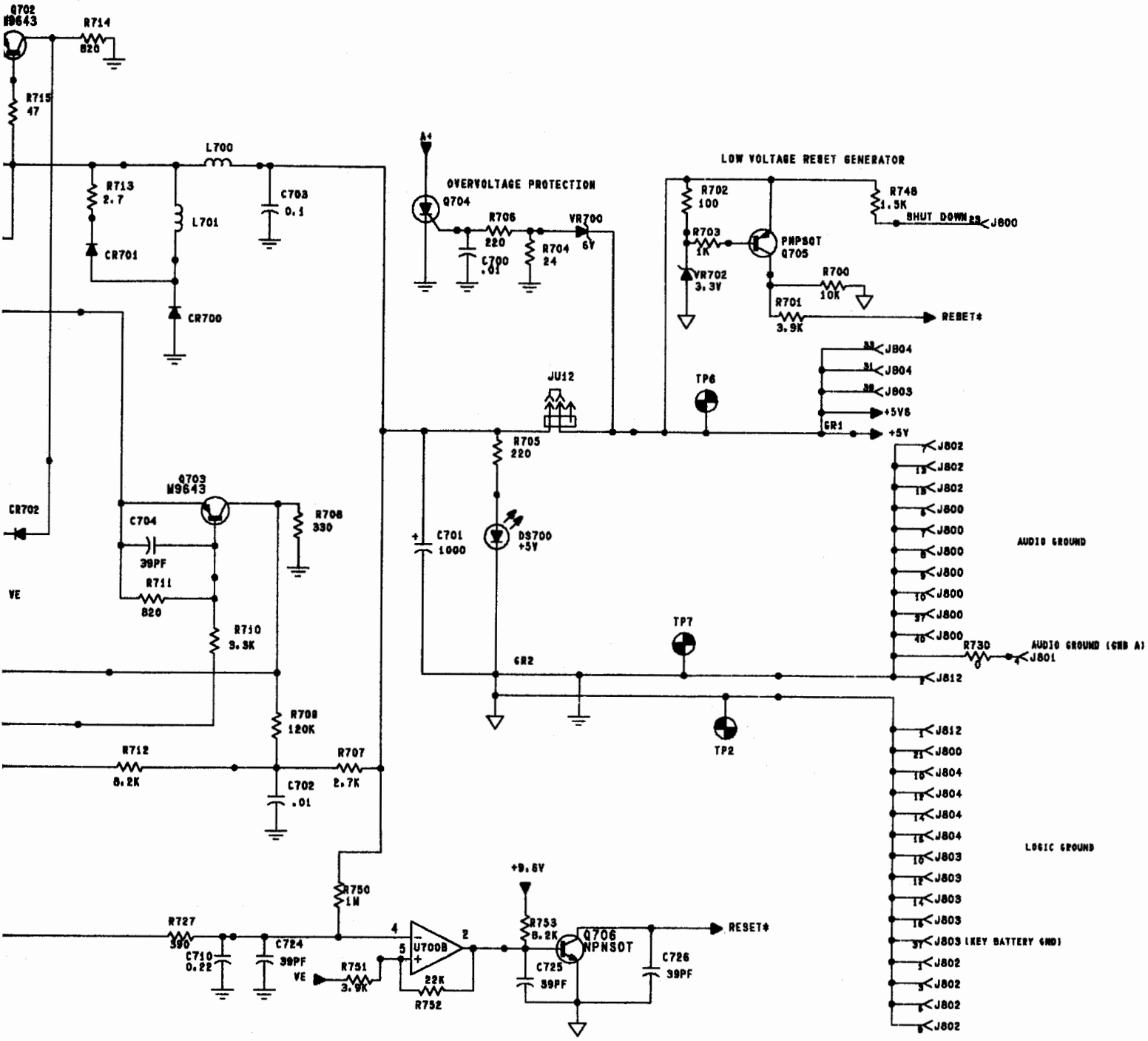
NOTES:

1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but may be added for special applications.



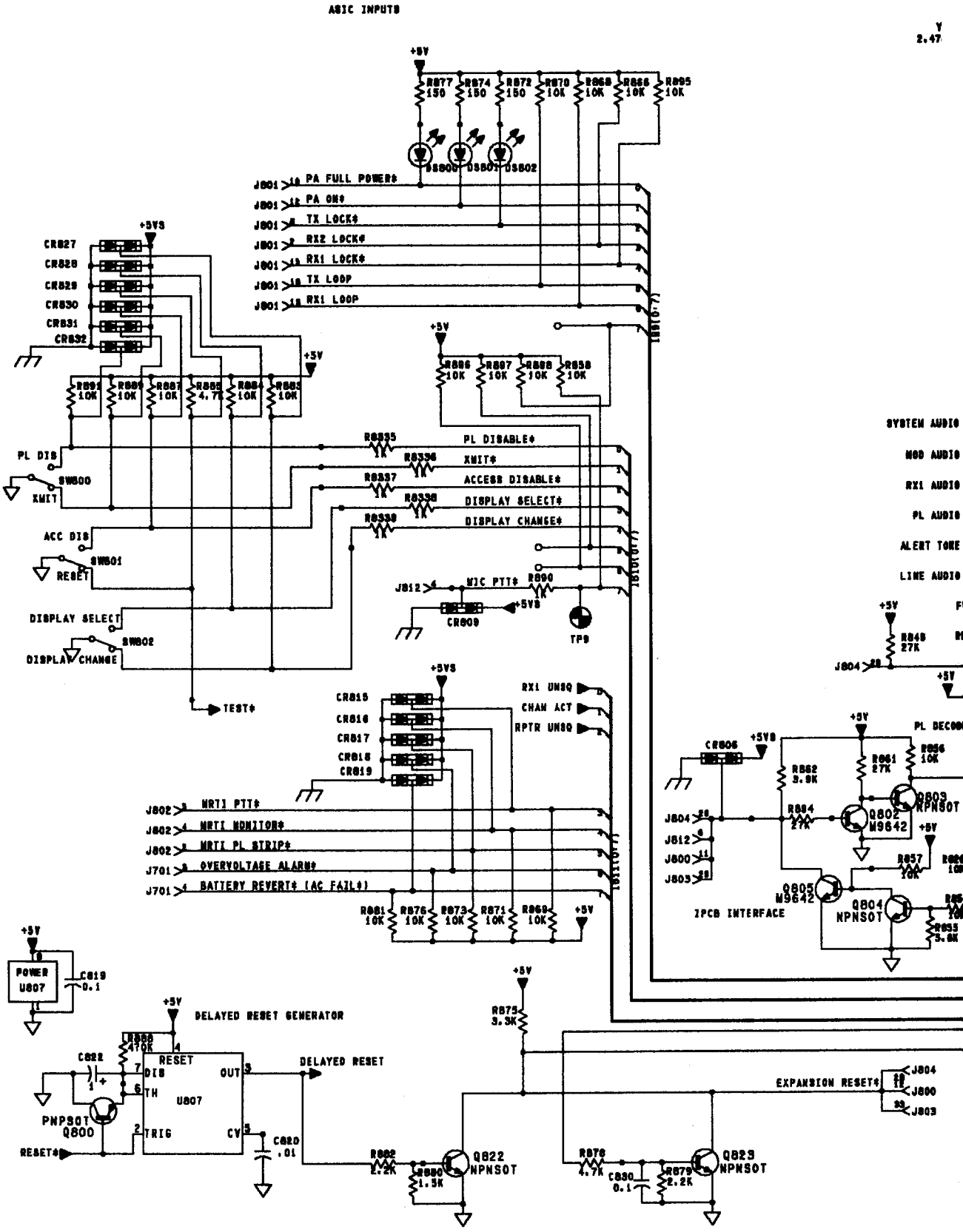

J802
J802
J800
J800
J800
J800
J800
A+
J804
J804
TP5
+9.6V
VA
VC
VB
BIAS GENERATORS
VB
C713
1
VE
VR701
5.1V
A+
C727
0.1
POWER
U700
L702
C711
0.1
C708
660
C707
0.1
Q700
M9829
R722
100
Q702
M9643
R716
1
R717
1
R718
1
R719
1
R715
47
R714
820
Q701
M9328
R723
390
L700
R713
2.7
L701
CR701
CR700
C703
0.1
+9.6V
R724
12K
R729
56K
R725
22K
VE
R733
180K
U700B
R726
2.7K
C722
39PF
C709
.001
CR706
+9.6V
R728
3.9K
R747
10K
CR705
R721
3.9K
CR702
CR704
C705
39PF
VE
Q703
M9643
C704
39PF
R711
820
R708
330
R720
1.8K
CR703
R710
9.3K
C706
39PF
U700C
R709
120K
R712
8.2K
R707
2.7K
C702
.01
SHUTDOWN COMPARATOR
A+
VE
R734
2.1K
R731
100
U700A
C712
.01
R735
1.91K
R749
8.2K
R736
560
CR707
CR708
TEST*
R750
1M
R727
390
C710
0.22
C724
39PF
VE
R751
3.9K

SECURE CAPABLE STATION CONTROL BOARD
SCHEMATIC DIAGRAM

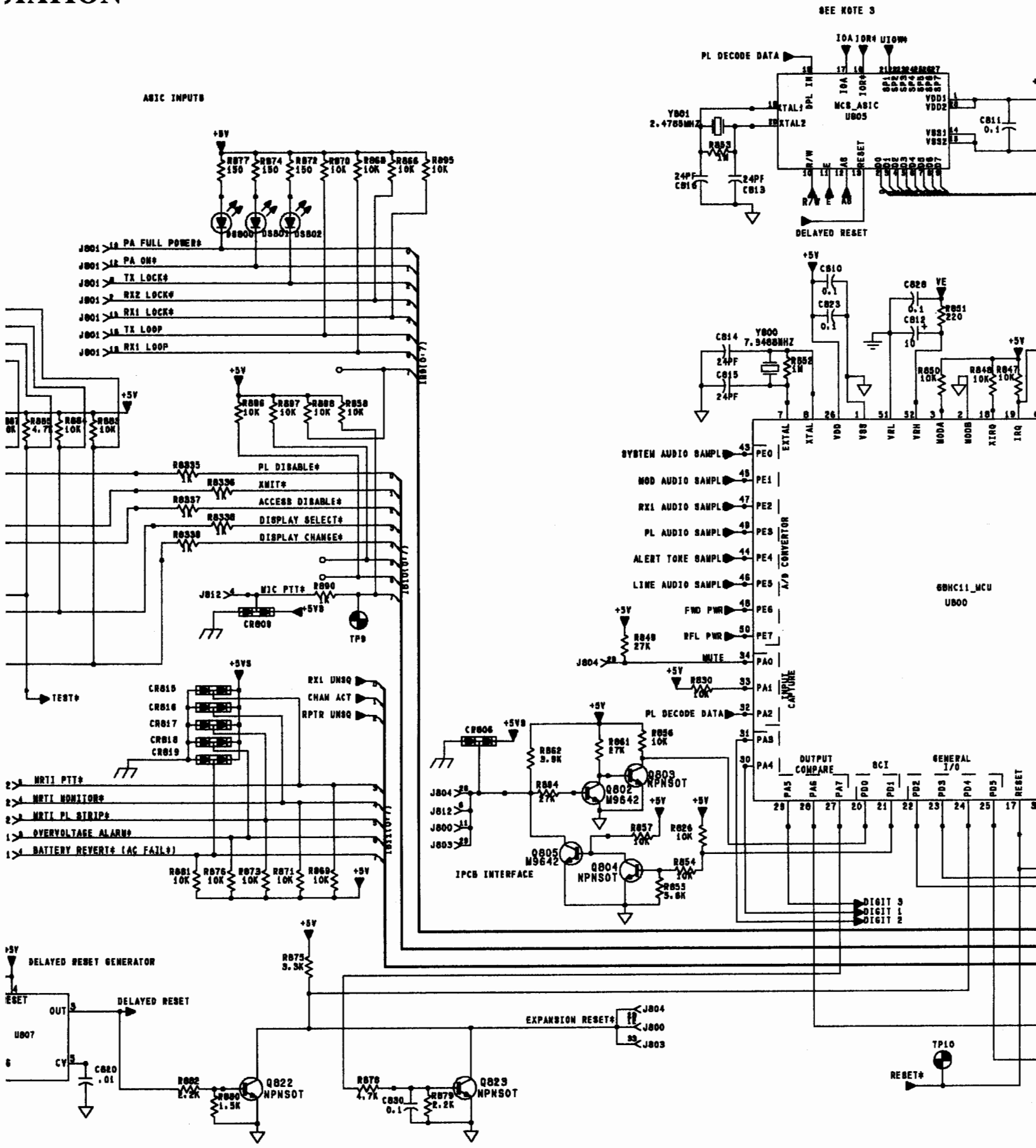


SECURE CAPABLE STATION CONTROL BOARD

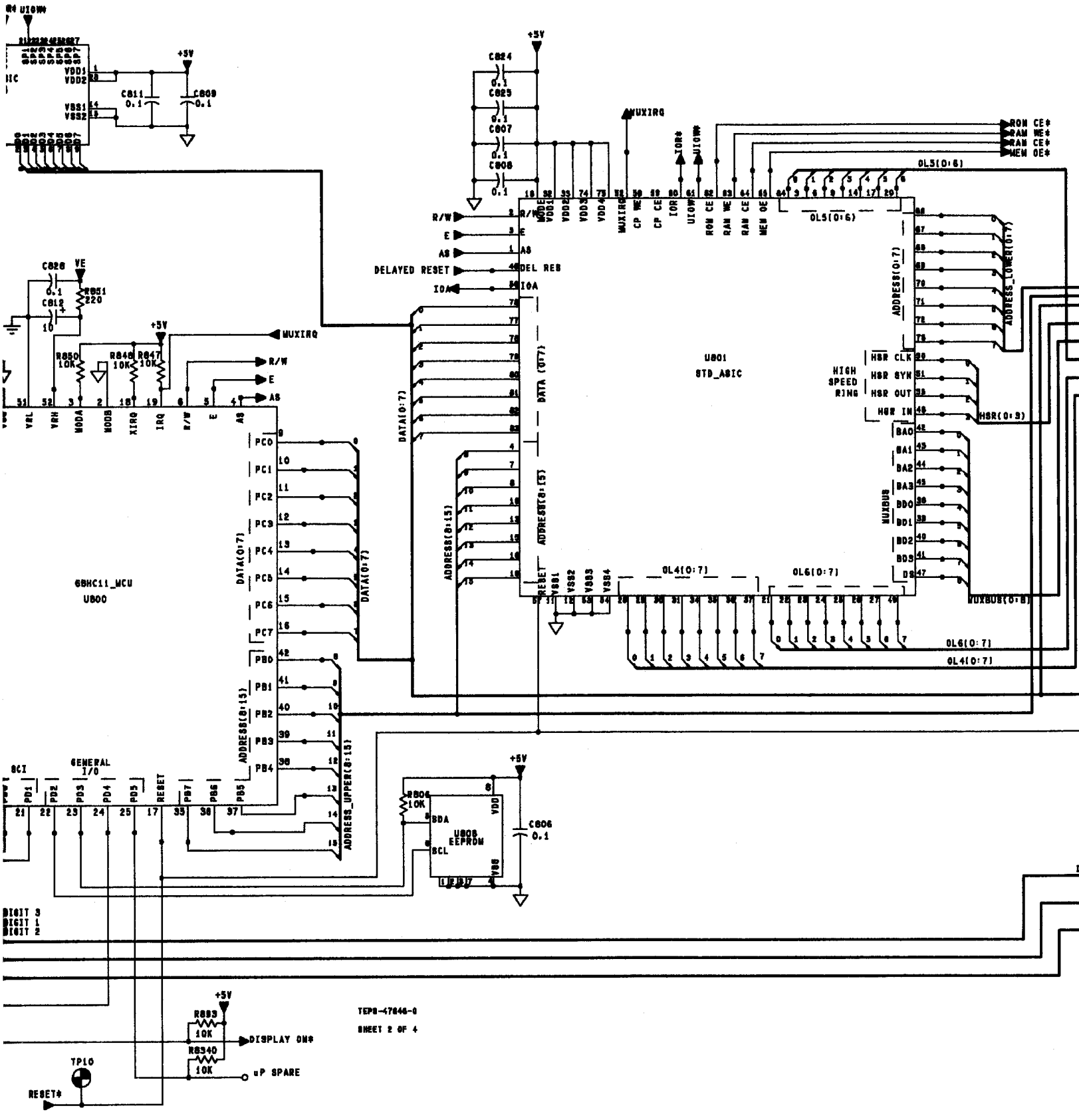
SCHEMATIC DIAGRAM

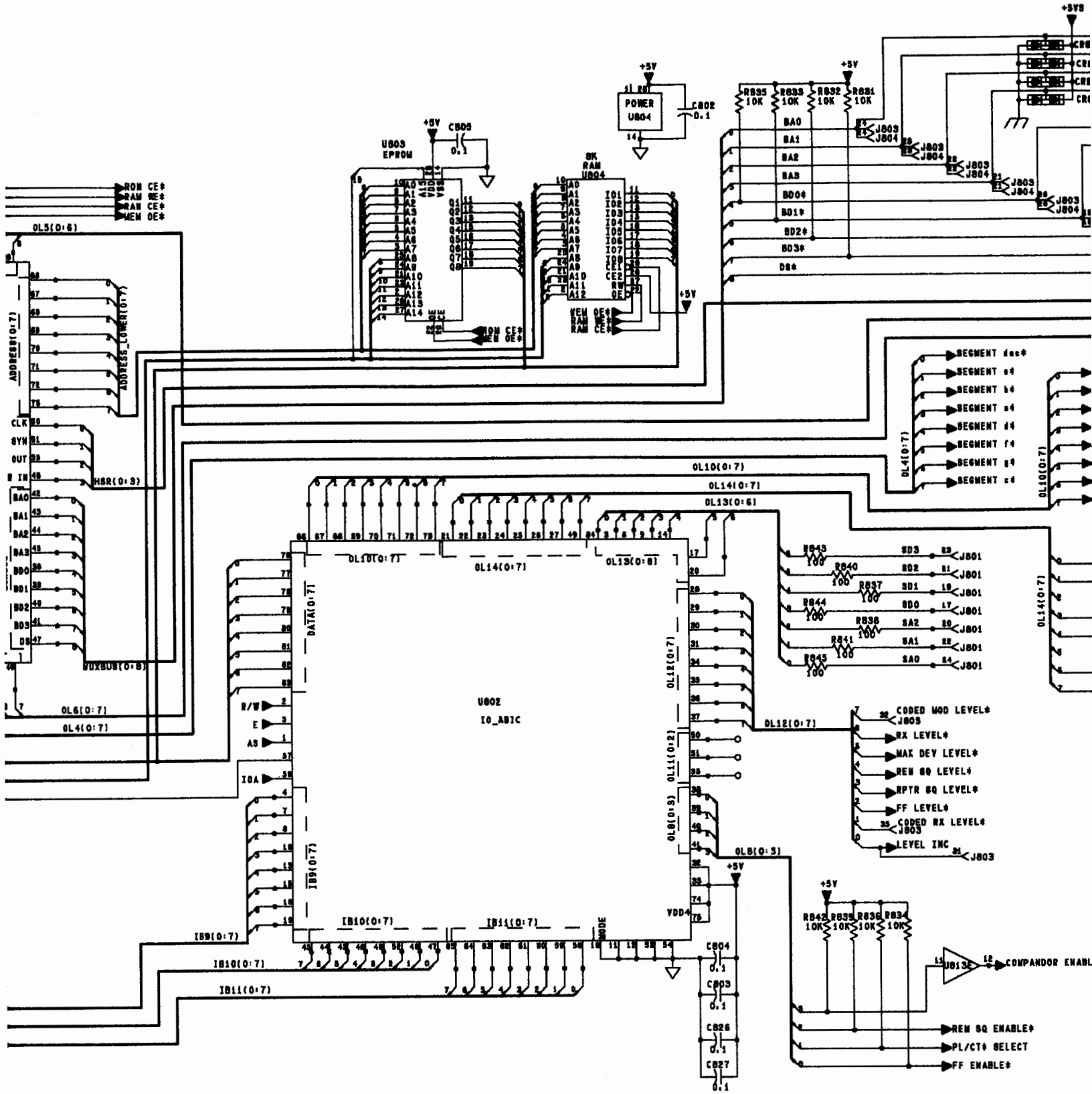


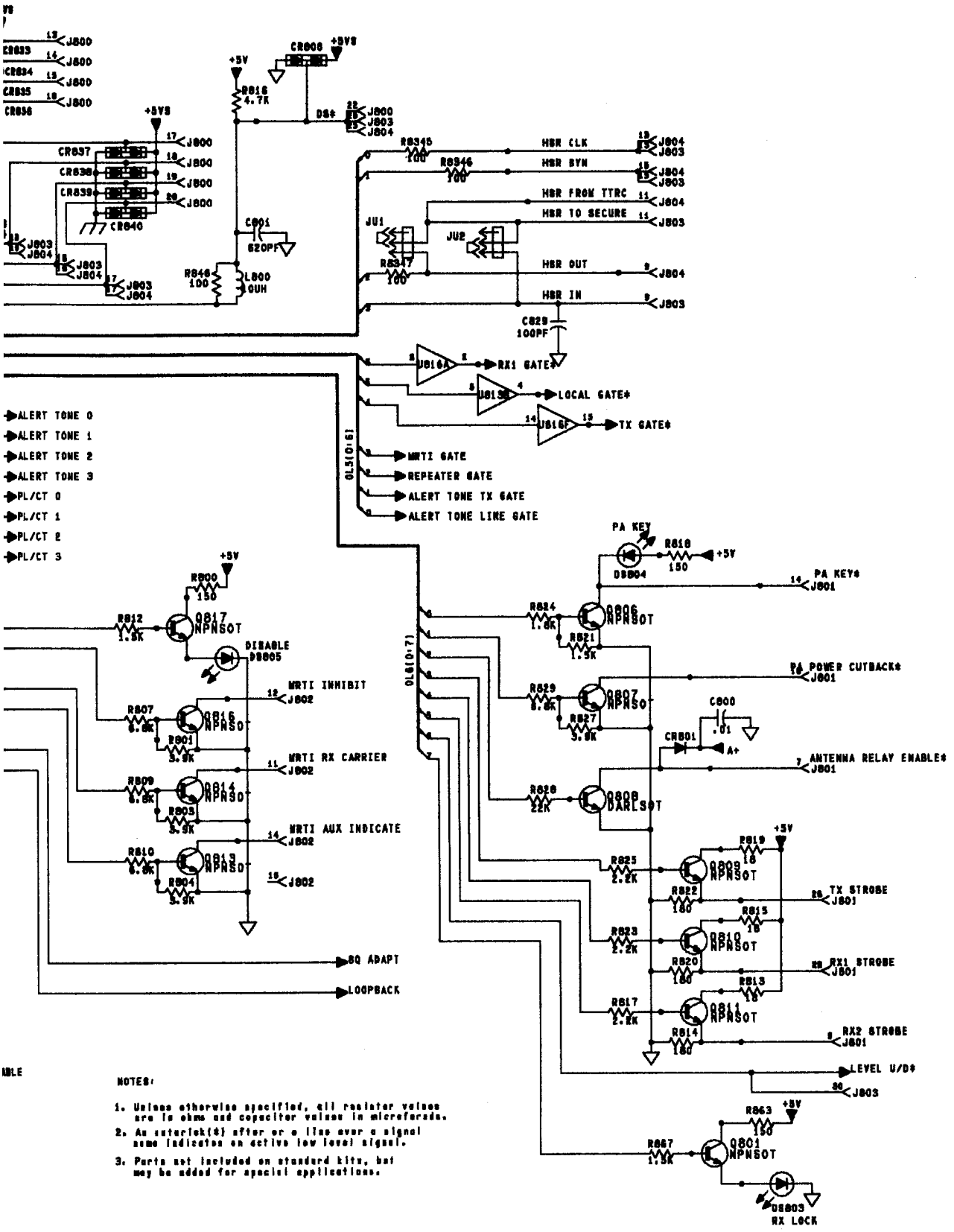
STATION



12/29/89

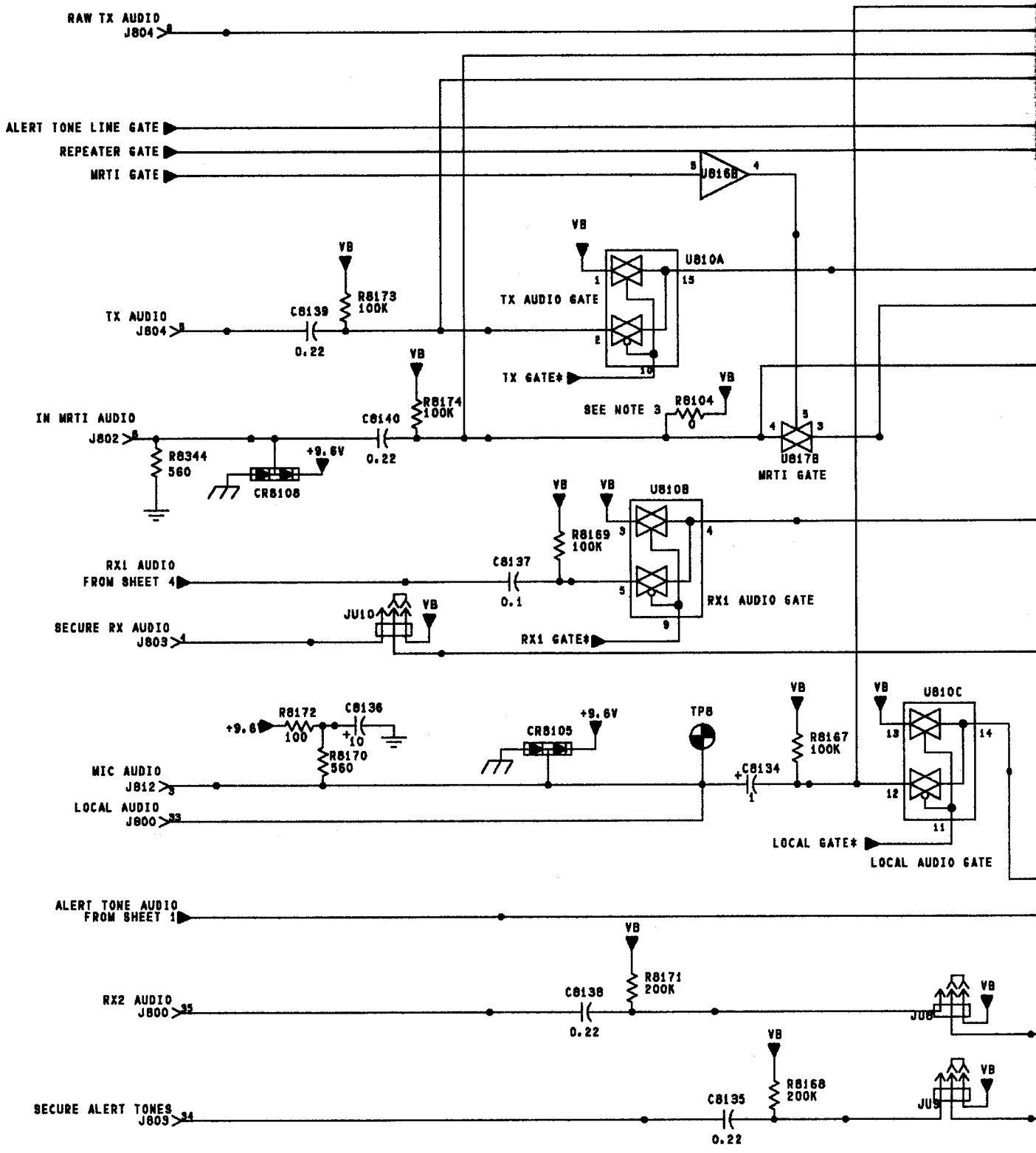

+5V
C824 0.1
C825 0.1
C807 0.1
C808 0.1
MUXIRQ
R/W
E
AS
DELAYED RESET
IOA
U801
STD_ASIC
DATA (0:7)
ADDRESS(0:15)
ADDRESS(0:7)
ADDRESS_LOWER(0:7)
OL5(0:6)
OL4(0:7)
OL6(0:7)
HIGH SPEED RING
HSR CLK
HSR SYN
HSR OUT
HSR IN
HSR(0:3)
MUXBUS
MUXBUS(0:8)
ROM CE*
RAM WE*
RAM CE*
MEM OE*
C826 0.1
C812 10
R851 220
R850 10K
R848 10K
R847 10K
VRL
VRH
MODA
MODB
XIRQ
IRQ
68HC11_MCU
U800
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PB0
PB1
PB2
PB3
PB4
PD1
PD2
PD3
PD4
PD5
RESET
PB7
PB6
PB5
SCI
GENERAL I/O
R806 10K
U805 EEPROM
SDA
SCL
C806 0.1
DIGIT 3
DIGIT 1
DIGIT 2
R893 10K
R8340 10K
DISPLAY ON*
uP SPARE
TP10
RESET*
TEPS-47646-0
SHEET 2 OF 4

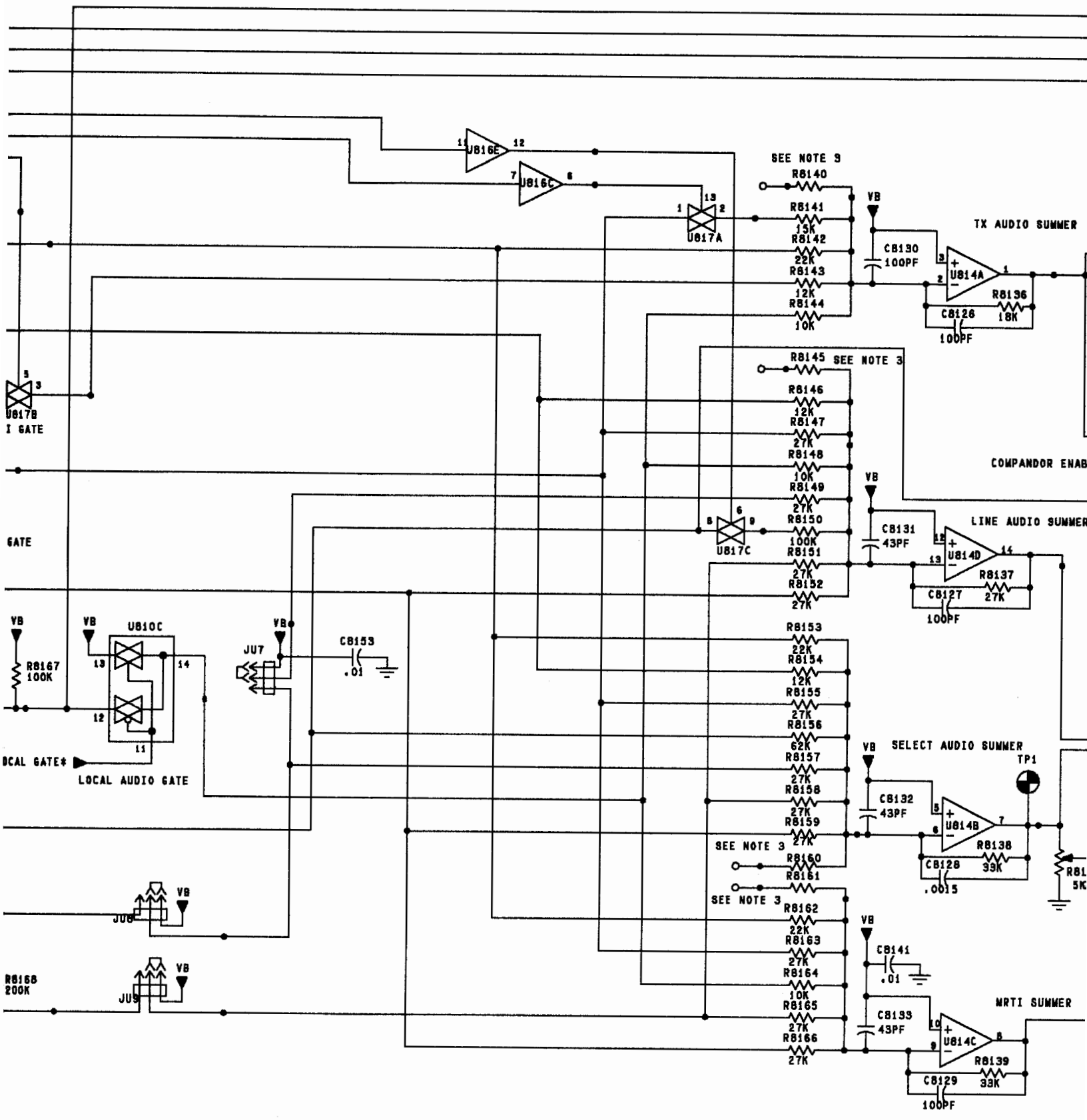

U803
EPROM
8K
RAM
U804
POWER
U804
C802
0.1
C805
0.1
+5V
ROM CE#
RAM WE#
RAM CE#
MEM OE#
OL5(0:6)
ADDRESS(0:7)
ADDRESS_LOWER(0:7)
CLK
SYN
OUT
HSR(0:9)
MUXBUS(0:8)
OL6(0:7)
OL4(0:7)
OL10(0:7)
OL14(0:7)
OL13(0:6)
U802
IO_ABIC
DATA(0:7)
R/W
E
AS
IOA
IB9(0:7)
IB10(0:7)
IB11(0:7)
OL12(0:7)
OL11(0:2)
OL8(0:3)
OLB(0:3)
VDD4
MODE
R835 10K
R833 10K
R832 10K
R831 10K
BA0
BA1
BA2
BA3
BD0#
BD1#
BD2#
BD3#
DS#
J803
J804
SEGMENT dec#
SEGMENT a#
SEGMENT b#
SEGMENT c#
SEGMENT d#
SEGMENT f#
SEGMENT g#
SEGMENT e#
OL1(0:7)
R843
R840
R837
R844
R838
R841
R845
100
SD3
SD2
SD1
SD0
SA2
SA1
SA0
J801
CODED MOD LEVEL#
J805
RX LEVEL#
MAX DEV LEVEL#
REM SQ LEVEL#
RPTR SQ LEVEL#
FF LEVEL#
CODED RX LEVEL#
LEVEL INC
J803
R842 10K
R835 10K
R836 10K
R834 10K
U813E
COMPANDOR ENABL
REM SQ ENABLE#
PL/CT# SELECT
FF ENABLE#
C804
C803
C826
C827
0.1

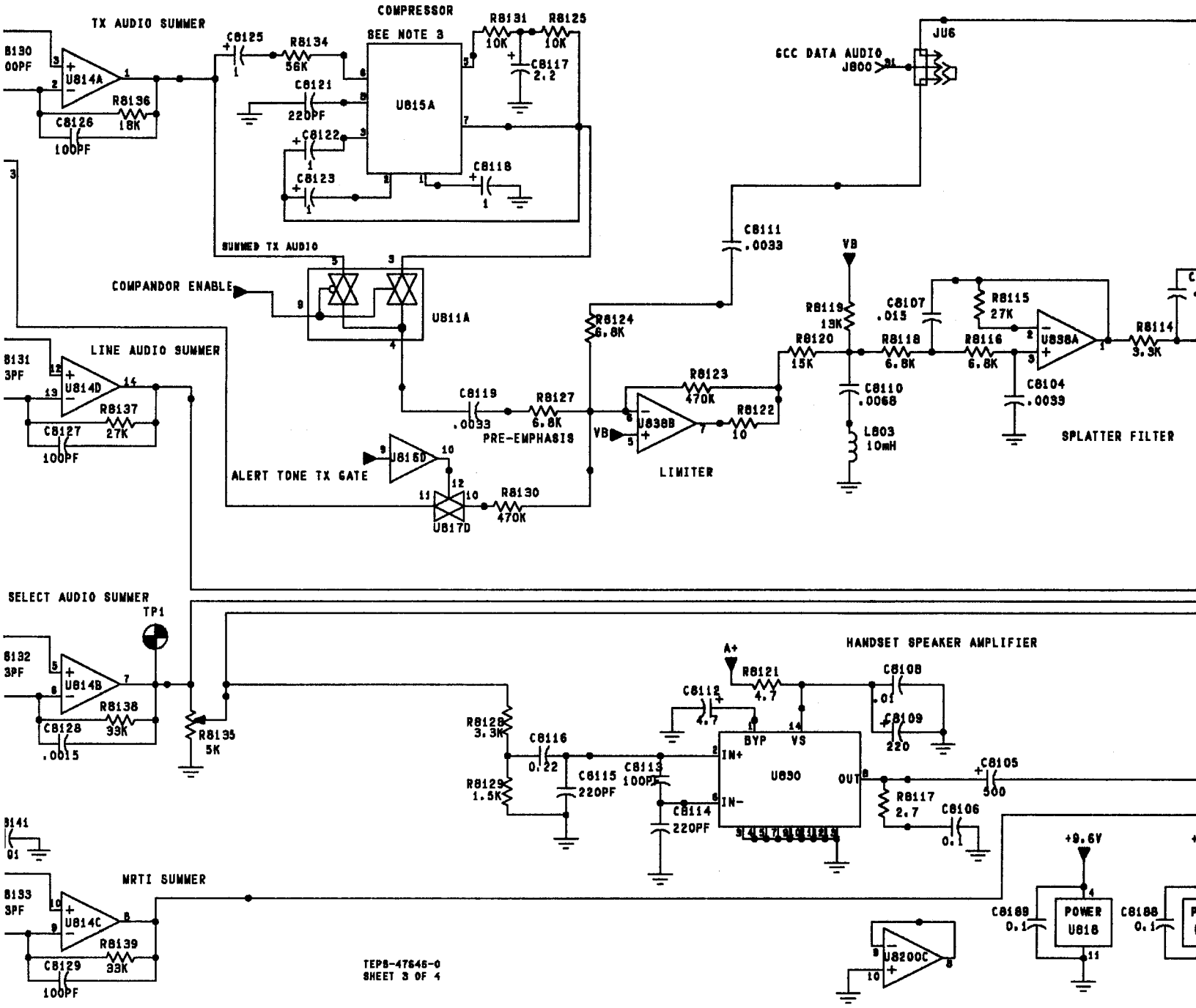


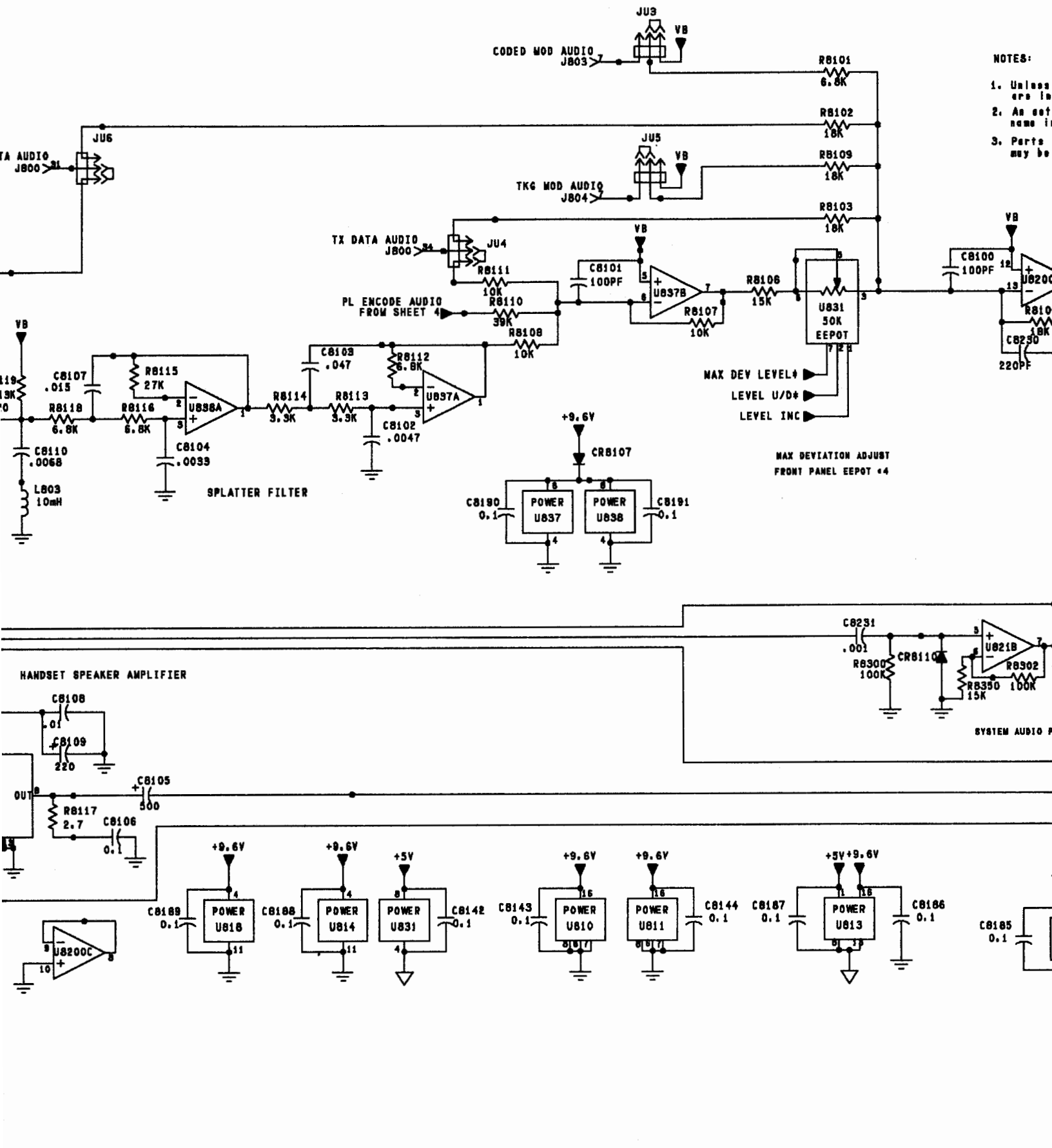
NOTES:

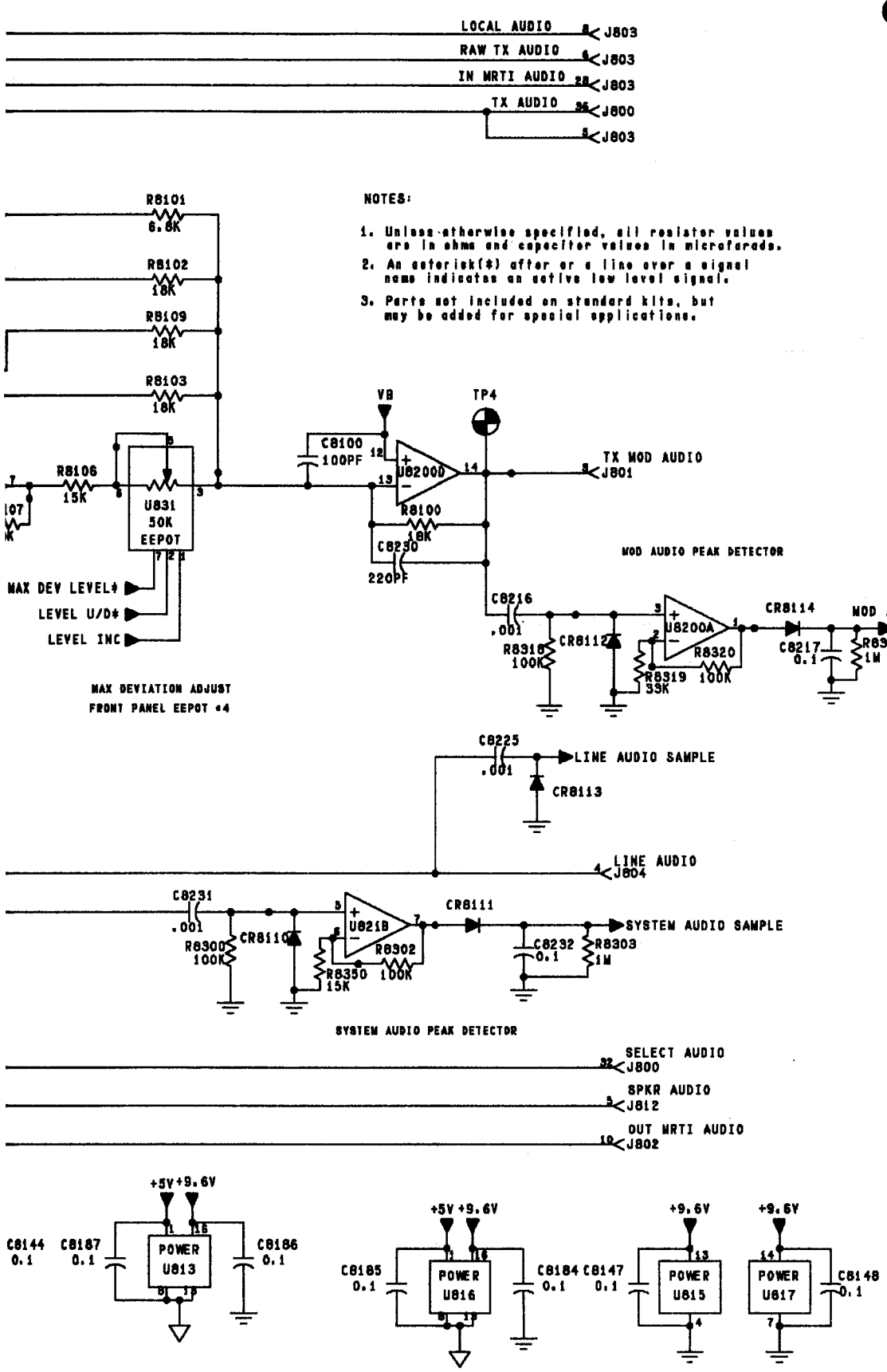
1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but may be added for special applications.


RAW TX AUDIO
J804
ALERT TONE LINE GATE
REPEATER GATE
MRTI GATE
U816B
VB
U810A
TX AUDIO GATE
R8173
100K
C8139
0.22
TX AUDIO
J804
TX GATE*
SEE NOTE 3
R8104
0
R8174
100K
C8140
0.22
IN MRTI AUDIO
J802
R8344
560
+9.6V
CR8108
U817B
MRTI GATE
U810B
R8169
100K
C8137
0.1
RX1 AUDIO
FROM SHEET 4
RX1 AUDIO GATE
JU10
SECURE RX AUDIO
J803
RX1 GATE*
R8172
100
C8136
10
R8170
560
CR8105
TP8
R8167
100K
C8134
U810C
MIC AUDIO
J812
LOCAL AUDIO
J800
LOCAL GATE*
LOCAL AUDIO GATE
ALERT TONE AUDIO
FROM SHEET 1
R8171
200K
C8138
0.22
RX2 AUDIO
J800
JU6
R8168
200K
C8135
0.22
SECURE ALERT TONES
J803
JU5


U816E
U816C
U817A
SEE NOTE 9
R8140
R8141
15K
R8142
22K
R8143
12K
R8144
10K
VB
C8130
100PF
U814A
TX AUDIO SUMMER
R8136
18K
C8126
100PF
U817B
I GATE
R8145 SEE NOTE 3
R8146
12K
R8147
27K
R8148
10K
R8149
27K
R8150
100K
R8151
27K
R8152
27K
U817C
COMPANDOR ENAB
C8131
43PF
U814D
LINE AUDIO SUMMER
R8137
27K
C8127
100PF
GATE
R8167
100K
U810C
JU7
C8153
.01
R8153
22K
R8154
12K
R8155
27K
R8156
62K
R8157
27K
R8158
27K
R8159
27K
SEE NOTE 3
R8160
R8161
SEE NOTE 3
R8162
22K
R8163
27K
R8164
10K
R8165
27K
R8166
27K
OCAL GATE*
LOCAL AUDIO GATE
SELECT AUDIO SUMMER
TP1
C8132
43PF
U814B
R8138
39K
C8128
.0015
R81
5K
JU6
JU5
R8168
200K
C8141
.01
C8133
43PF
U814C
MRTI SUMMER
R8139
33K
C8129
100PF

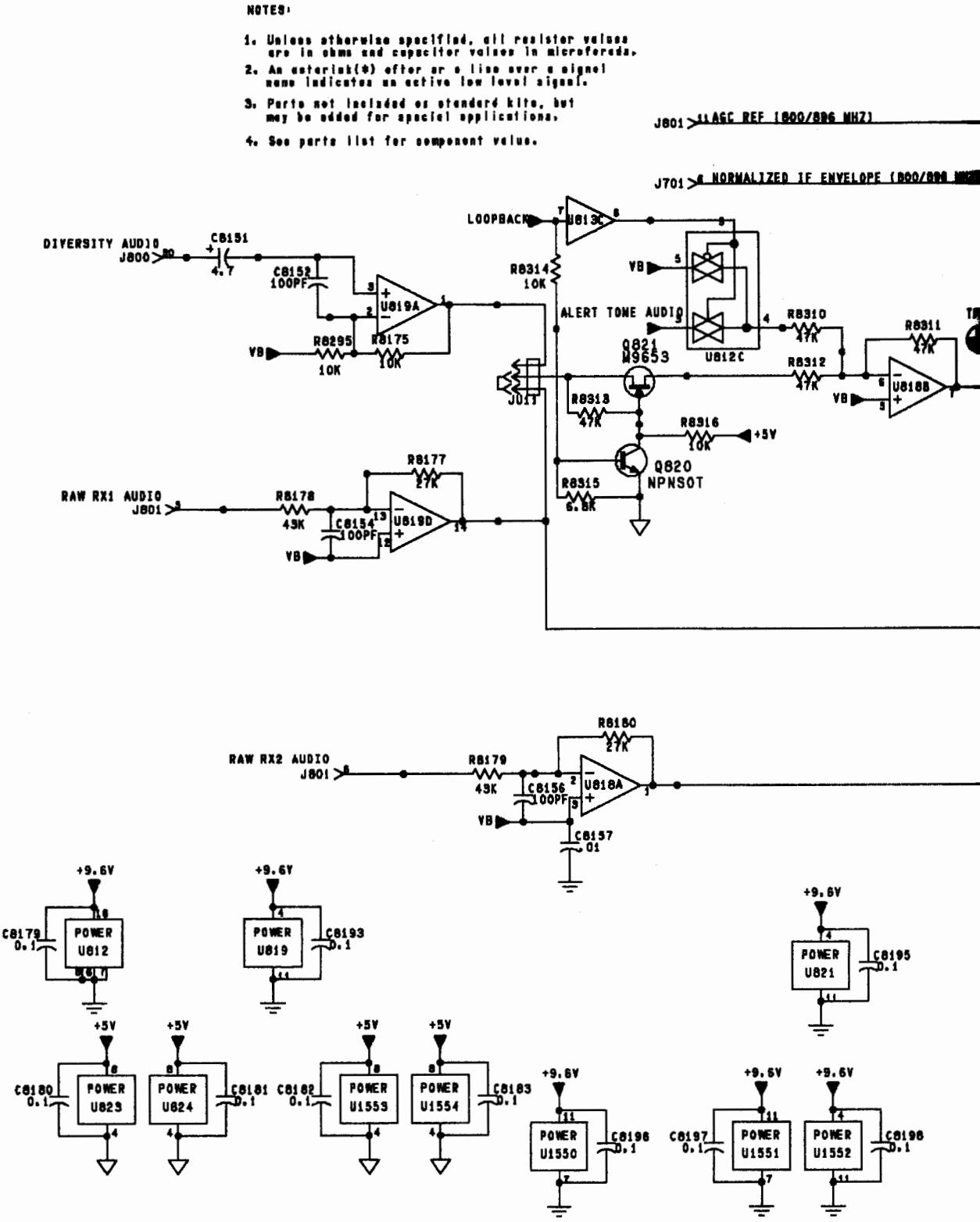

TX AUDIO SUMMER
COMPRESSOR
SEE NOTE 3
U814A
U815A
C8125
R8134
56K
C8121
220PF
C8122
C8123
R8131
10K
R8125
10K
C8117
2.2
C8118
R8136
18K
C8126
100PF
SUMMER TX AUDIO
COMPANDOR ENABLE
U811A
LINE AUDIO SUMMER
U814D
R8137
27K
C8127
100PF
ALERT TONE TX GATE
U816D
U817D
R8130
470K
C8119
.0033
R8127
6.8K
PRE-EMPHASIS
R8124
6.8K
C8111
.0033
GCC DATA AUDIO
J800
JU6
VB
R8119
13K
R8120
15K
C8107
.015
R8118
6.8K
C8110
.0068
L803
10mH
R8115
27K
R8116
6.8K
C8104
.0039
U838A
R8114
3.3K
SPLATTER FILTER
R8123
470K
R8122
10
U838B
LIMITER
SELECT AUDIO SUMMER
TP1
U814B
R8138
39K
C8128
.0015
R8135
5K
HANDSET SPEAKER AMPLIFIER
A+
R8121
4.7
C8112
4.7
C8108
.01
C8109
220
BYP
VS
R8128
3.3K
C8116
0.22
R8129
1.5K
C8115
220PF
C8113
100PF
C8114
220PF
U830
IN+
IN-
OUT
C8105
500
R8117
2.7
C8106
0.1
MRTI SUMMER
U814C
R8139
33K
C8129
100PF
U8200C
+9.6V
POWER
U818
C8189
0.1
C8188
0.1
TEPS-47646-0
SHEET 3 OF 4


JU3
VB
CODED MOD AUDIO
J803
R8101
6.8K
R8102
18K
JU5
VB
R8109
18K
TKG MOD AUDIO
J804
R8103
18K
JU6
TA AUDIO
J800
TX DATA AUDIO
J800
JU4
R8111
10K
C8101
100PF
U837B
R8106
15K
R8107
10K
U831
50K
EEPOT
C8100
100PF
U8200
R8110
39K
PL ENCODE AUDIO
FROM SHEET 4
R8108
10K
MAX DEV LEVEL#
LEVEL U/D#
LEVEL INC
C8103
.047
R8112
6.8K
U837A
C8107
.015
R8115
27K
U838A
R8114
3.3K
R8113
3.3K
C8102
.0047
R8118
6.8K
R8116
6.8K
C8110
.0068
C8104
.0039
L803
10mH
SPLATTER FILTER
+9.6V
CR8107
C8190
0.1
POWER
U837
POWER
U838
C8191
0.1
MAX DEVIATION ADJUST
FRONT PANEL EEPOT #4
C8231
.001
CR8110
R8300
100K
U821B
R8302
100K
R8350
15K
SYSTEM AUDIO
HANDSET SPEAKER AMPLIFIER
C8108
.01
C8109
220
OUT
C8105
500
R8117
2.7
C8106
0.1
U8200C
+9.6V
C8189
0.1
POWER
U816
+9.6V
C8188
0.1
POWER
U814
+5V
POWER
U831
C8142
0.1
+9.6V
C8143
0.1
POWER
U810
+9.6V
POWER
U811
C8144
0.1
+5V
+9.6V
C8187
0.1
POWER
U813
C8186
0.1
C8185
0.1

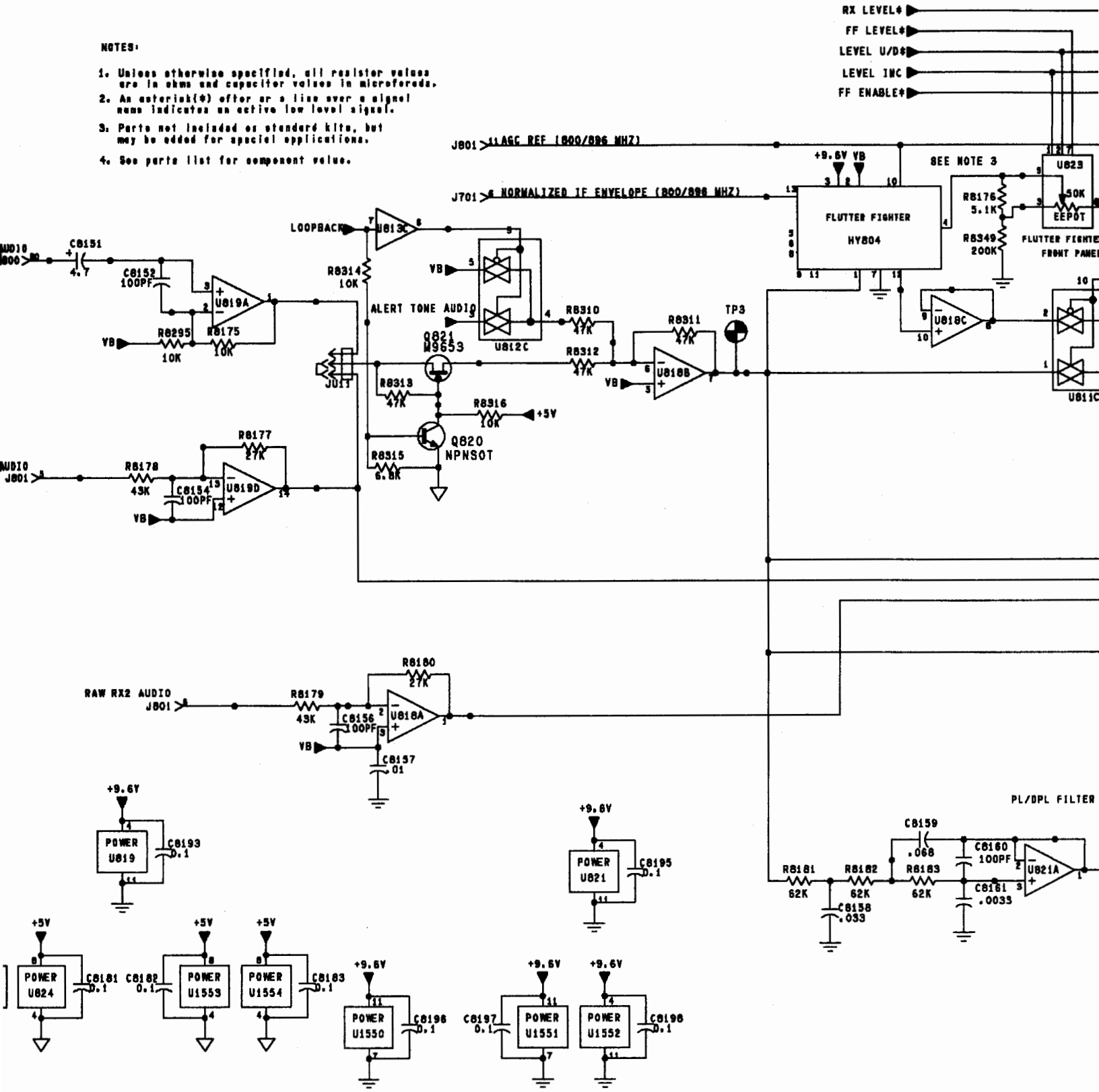

LOCAL AUDIO
RAW TX AUDIO
IN MRTI AUDIO
TX AUDIO
J803
J800
NOTES:
1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but may be added for special applications.
R8101 6.8K
R8102 18K
R8109 18K
R8103 18K
R8106 15K
U831 50K EEPOT
MAX DEV LEVEL*
LEVEL U/D*
LEVEL INC
MAX DEVIATION ADJUST
FRONT PANEL EEPOT #4
VB
TP4
C8100 100PF
U8200D
R8100 18K
C8230 220PF
TX MOD AUDIO
J801
MOD AUDIO PEAK DETECTOR
C8216 .001
R8318 100K
CR8112
U8200A
R8320
R8319 33K
CR8114
C8217 0.1
R8321 1M
MOD AUDIO SAMPLE
C8225 .001
CR8113
LINE AUDIO SAMPLE
LINE AUDIO
J804
C8231 .001
R8300 100K
CR8110
U821B
R8302
R8350 15K
CR8111
C8232 0.1
R8303 1M
SYSTEM AUDIO SAMPLE
SYSTEM AUDIO PEAK DETECTOR
SELECT AUDIO
J800
SPKR AUDIO
J812
OUT MRTI AUDIO
J802
+5V +9.6V
C8144 0.1
C8187 0.1
POWER U813
C8186 0.1
C8185 0.1
POWER U816
C8184 0.1
C8147 0.1
POWER U815
POWER U817
C8148 0.1

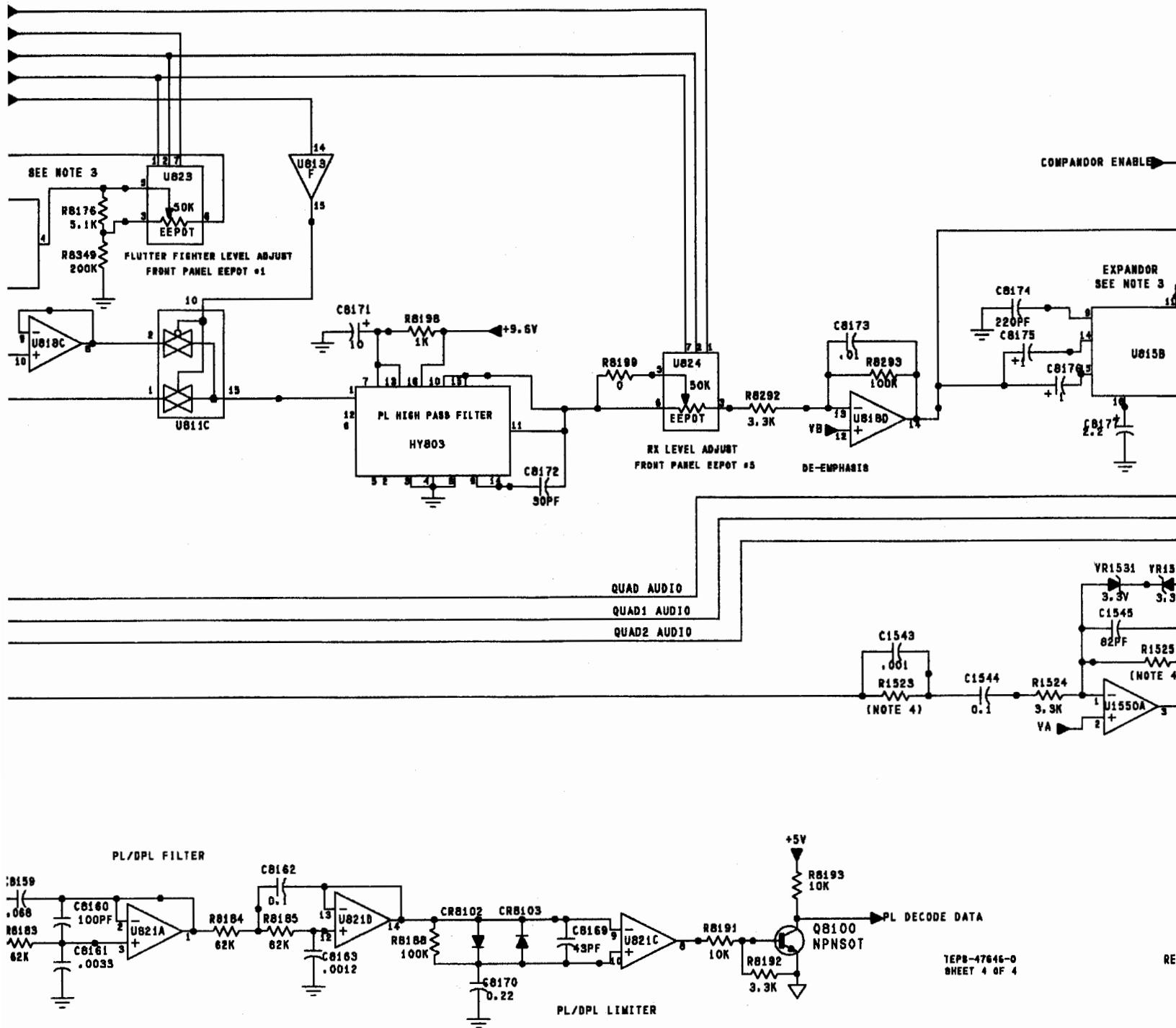
SECURE CAPABLE STATION CONTROL BOARD

SCHEMATIC DIAGRAM

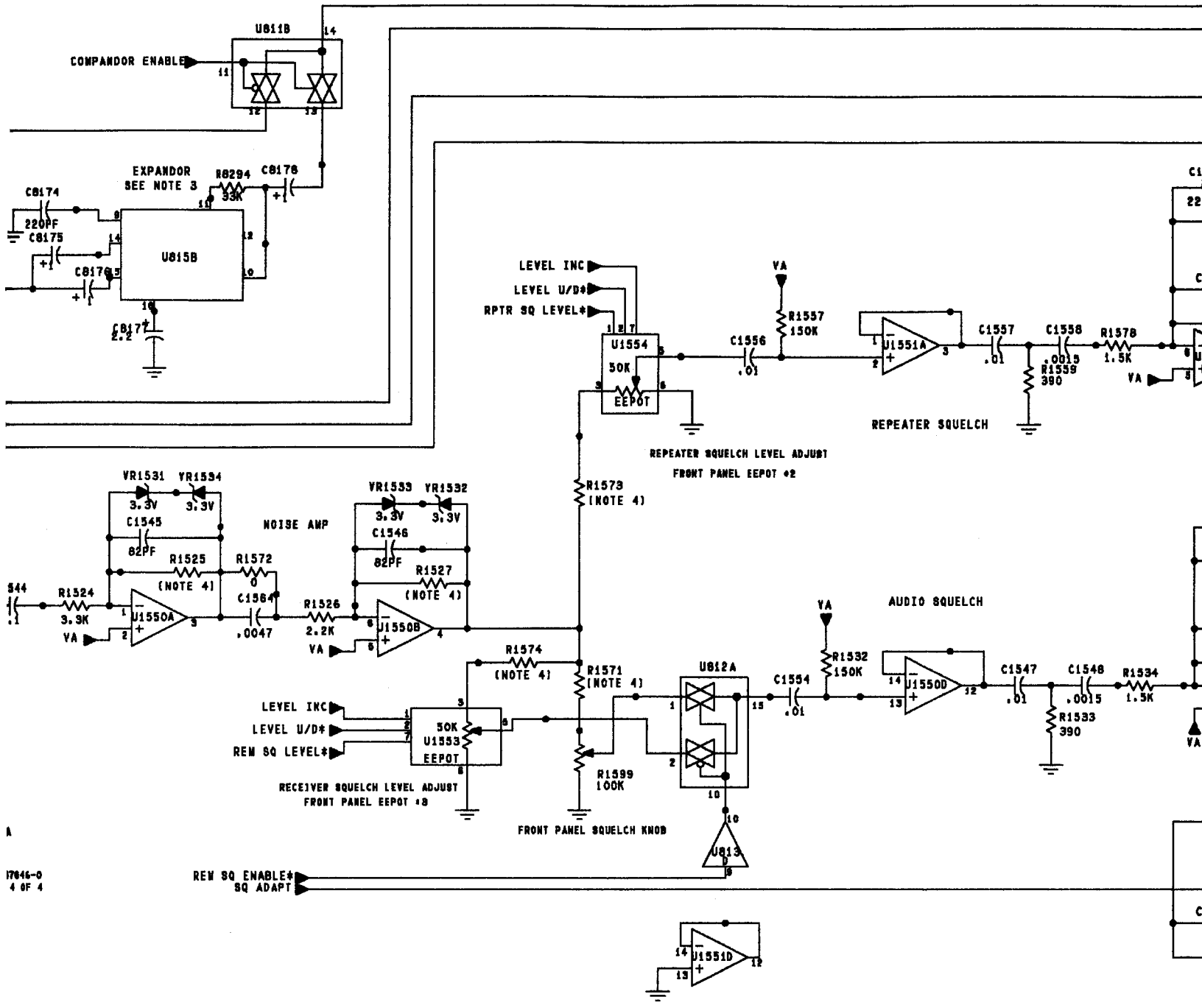


TATION


NOTES:
1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but may be added for special applications.
4. See parts list for component value.
RX LEVEL*
FF LEVEL*
LEVEL U/D*
LEVEL INC
FF ENABLE*
J801 AGC REF (800/896 MHZ)
J701 NORMALIZED IF ENVELOPE (800/896 MHZ)
SEE NOTE 3
FLUTTER FIGHTER
HY804
U829
50K
EEPOT
R8176 5.1K
R8349 200K
FLUTTER FIGHTER FRONT PANEL
LOOPBACK
U813C
R8314 10K
VB
ALERT TONE AUDIO
Q821 M9653
U812C
R8310 47K
R8311 47K
R8312 47K
TP3
U818B
U818C
U811C
JU11
R8313 47K
R8316 10K
+5V
Q820 NPNSOT
R8315 6.8K
C8151 4.7
C8152 100PF
U819A
R8295 10K
R8175 10K
R8177 27K
R8178 43K
C8154 100PF
U819D
RAW RX2 AUDIO J801
R8180 27K
R8179 43K
C8156 100PF
U816A
C8157 .01
PL/DPL FILTER
C8159 .068
C8160 100PF
C8161 .0033
R8181 62K
R8182 62K
R8183 62K
C8158 .033
U821A
+9.6V
POWER U819
C8193 0.1
POWER U821
C8195 0.1
+5V
POWER U824
C8181 0.1
C8182 0.1
POWER U1553
POWER U1554
C8183 0.1
POWER U1550
C8196 0.1
C8197 0.1
POWER U1551
POWER U1552
C8198 0.1


SEE NOTE 3
U823
R8176
5.1K
50K
EEPOT
R8349
200K
FLUTTER FIGHTER LEVEL ADJUST
FRONT PANEL EEPOT #1
U813F
COMPANDOR ENABLE
U818C
U811C
C8171
10
R8198
1K
+9.6V
PL HIGH PASS FILTER
HY803
C8172
30PF
R8199
0
U824
50K
EEPOT
RX LEVEL ADJUST
FRONT PANEL EEPOT #5
R8292
3.3K
C8173
.01
R8293
100K
U818D
VB
DE-EMPHASIS
EXPANDOR
SEE NOTE 3
C8174
220PF
C8175
C8176
U815B
C8177
2.2
QUAD AUDIO
QUAD1 AUDIO
QUAD2 AUDIO
VR1531
3.3V
C1545
82PF
R1525
(NOTE 4
C1543
.001
R1523
(NOTE 4)
C1544
0.1
R1524
3.3K
U1550A
VA

PL/DPL FILTER
C8159
.068
R8183
62K
C8160
100PF
C8161
.0033
U821A
R8184
62K
C8162
0.1
R8185
62K
C8163
.0012
U821B
CR8102
CR8103
R8188
100K
C8170
0.22
PL/DPL LIMITER
C8169
43PF
U821C
+5V
R8193
10K
R8191
10K
R8192
3.3K
Q8100
NPNSOT
PL DECODE DATA
TEPS-47645-0
SHEET 4 OF 4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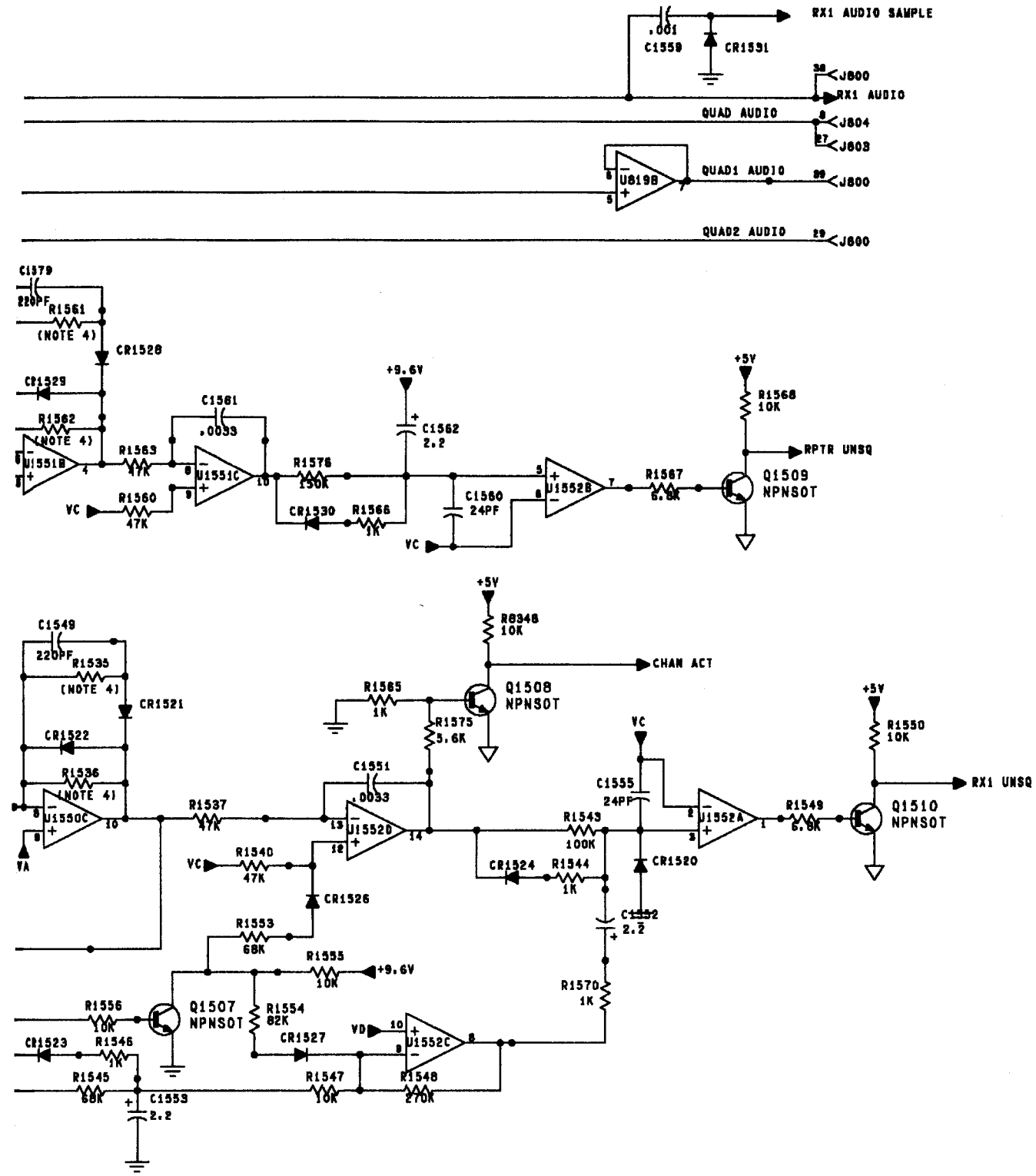
COMPANDOR ENABLE
EXPANDOR
SEE NOTE 3
R8294
33K
C8178
C8174
220PF
C8175
C8176
C8177
2.2
U815B
LEVEL INC
LEVEL U/D*
RPTR SQ LEVEL*
U1554
50K
EEPOT
C1556
.01
R1557
150K
VA
U1551A
C1557
.01
C1558
.0015
R1559
390
R1578
1.5K
REPEATER SQUELCH
REPEATER SQUELCH LEVEL ADJUST
FRONT PANEL EEPOT #2
R1573
(NOTE 4)
VR1531
VR1534
3.3V
3.3V
C1545
82PF
R1525
(NOTE 4)
R1572
0
C1564
.0047
NOISE AMP
VR1533
VR1532
3.3V
3.3V
C1546
82PF
R1527
(NOTE 4)
R1524
3.3K
U1550A
R1526
2.2K
U1550B
R1574
(NOTE 4)
R1571
(NOTE 4)
U812A
C1554
.01
R1532
150K
AUDIO SQUELCH
U1550D
C1547
.01
C1548
.0015
R1534
1.5K
R1533
390
LEVEL INC
LEVEL U/D*
REM SQ LEVEL*
50K
U1553
EEPOT
RECEIVER SQUELCH LEVEL ADJUST
FRONT PANEL EEPOT #3
R1599
100K
FRONT PANEL SQUELCH KNOB
U813
REM SQ ENABLE*
SQ ADAPT
U1551D
17646-0
4 OF 4


RX1 AUDIO SAMPLE
.001
C1559
CR1531
J800
RX1 AUDIO
QUAD AUDIO
J804
J803
U8198
QUAD1 AUDIO
J800
QUAD2 AUDIO
J800
C1579
220PF
R1561
(NOTE 4)
CR1528
CR1529
R1562
(NOTE 4)
U1551B
R1563
47K
C1561
.0033
U1551C
R1576
150K
+9.6V
C1562
2.2
VC
R1560
47K
CR1530
R1566
1K
C1560
24PF
U1552B
R1567
6.8K
+5V
R1568
10K
RPTR UNSQ
Q1509
NPNSOT
C1549
220PF
R1535
(NOTE 4)
CR1521
CR1522
R1536
(NOTE 4)
U1550C
VA
R1537
47K
+5V
R8348
10K
CHAN ACT
R1565
1K
Q1508
NPNSOT
R1575
5.6K
C1551
.0033
U1552D
VC
R1540
47K
CR1526
R1553
68K
R1555
10K
+9.6V
R1556
10K
Q1507
NPNSOT
R1554
82K
CR1523
R1546
1K
R1545
68K
C1553
2.2
VD
U1552C
CR1527
R1547
10K
R1548
270K
C1555
24PF
U1552A
R1543
100K
CR1524
R1544
1K
CR1520
C1552
2.2
R1570
1K
R1549
6.8K
+5V
R1550
10K
RX1 UNSQ
Q1510
NPNSOT

SECURE CAPABLE STATION CONTROL BOARD
SCHEMATIC DIAGRAM NOTES

NOTES:

1. Unless otherwise specified, all resistor values are in ohms and capacitor values are in microfarads.
2. An asterisk (*) after or a line over a signal name indicates an active low level signal.
3. Parts may be mounted on circuit board, but circuitry is used for special applications only.
4. Part not included on PC board, but it may be added for special applications.
5. See parts list for component value.

Integrated Circuit Data Chart

Ref. Desig.	Description	13.8 V (pin)	9.6 V (pin)	5 V (pin)	Logic Gnd (pin)	Audio Gnd (pin)
U700	Quad Comparator	3				12
U800	8-Bit MCU			26	1	
U801	ASIC			32,33,74,75	11,12,53,54	
U802	ASIC			32,33,74,75	11,12,53,54	
U803	EPROM			28	14	
U804	8k × 8 RAM			28	14	
U805	Not Used			1,28	14,15	
U806	Quad Operational Amplifier		4			11
U807	Timer			8	1	
U808	EEPROM			8	4	
U810	Analog Mux/Demux		16			8,7,6
U811	Analog Mux/Demux		16			8,7,6
U812	Analog Mux/Demux		16			8,7,6
U813	Converter		16	1	8,13	
U814	Quad Operational Amplifier		4			11
U815	Not Used		13			4
U816	Converter		16	1	8,13	
U817	Quad Bilateral Switch		14			7
U818 thru U821	Quad Operational Amplifier		4			11
U823	Not Used			8	4	
U824	Digital Control Potentiometer			8	4	
U830	1/2 W Audio Amplifier	4				3-5,7,9-13
U831	Digital Control Potentiometer			8	4	
U837	Dual Operational Amplifier		8			4
U838	Dual Operational Amplifier		8			4
U1550	Quad Operational Amplifier		11			7
U1551	Quad Operational Amplifier		11			7
U1552	Quad Operational Amplifier		4			11
U1553	Digital Control Potentiometer			8	4	
U1554	Digital Control Potentiometer			8	4	
U8200	Quad Operational Amplifier		4			11