MOTOROLA INC.

instruction manual revision

GENERAL:

This revision outlines changes that have occurred since the printing of your instruction manual. Use this information to correct your manual.

INSTRUCTION MANUAL AFFECTED:

68P81082E10-O	*MSF 5000* Digital Capable Stations 403-475 MHz; 6, 15, 40, 75, or 110 Watts Continuous Duty
68P81082E25-O	*MSF 5000* Digital Capable Stations 403-475 MHz; 225 Watts Continuous Duty

REVISION DETAILS:

1. Insert new section number 68P81086E04-O, covering new Secure capable Station Control Boards (SSCB) Models TLN3182B, TLN3189B, TLN3204B, and TLN3205B directly behind the SSCB MODULE tab in front of section 68P81083E92-O

2. Replace section number 68P81082E94-O, directly behind the TTRC MODULE tab, with new section 68P81082E94-C, covering Trunked Tone Remote Control (TTRC) modules TLN3112B and TLN3114B

   - Issue C of the section supports version B of the TTRC modules TLN3112 and TLN3114, including: definition of the jumpers used on B-version boards (reference revised Table 8 and new Table 9), revised component location overlays, revised schematics, and revised parts lists.

   - Issue C of the section also includes: — clarification of the source of Failsoft Codeword and Tone Generation on the SSCB board rather than on the TTRC board (paragraph 2.4.4).

3. Replace section number 68P81125E34-A, directly behind the SECURE MODULE tab, with the new section 68P81125E34-B, Option C514 Transparent Operation, Module TLN3045C Secure Module.

ATTACHMENTS:

Secure capable Station Control Boards (SSCB)
Models TLN3182B, TLN3189B, TLN3204B, and TLN3205B 68P81086E04-O

Trunked Tone Remote Control (TTRC) modules
Models TLN3112B and TLN3114B 68P81082E94-C

Option C514 Transparent Operation
Model TLN3045C Secure Module 68P81125E34-B

MOTOROLA INC.

SECURE CAPABLE STATION CONTROL BOARD

MODELS TLN3182B
TLN3189B
TLN3204B
TLN3205B

1. INTRODUCTION

1.1 OVERVIEW

This document describes the operation of the Secure capable Station Control Board (SSCB), which has been designed for use in the Digital *MSF 5000 / MSF 10000* repeater/base stations. The kit number of the SSCB depends upon the frequency band of the station in which the SSCB is used:

TLN3182B - VHF/UHF NB
TLN3189B - VHF/UHF
TLN3204B - 800
TLN3205B - 896

The SSCB is housed in the control tray attached to the top of the RF tray, and is compatible with the Trunked Tone Remote Control (TTRC) board (TLN3112, TLN3114) as well as the optional Secure Module (TLN3045). The SSCB also maintains compatibility with all existing optional expansion modules which can be housed in an expansion tray attached to the top of the control tray.

2. FUNCTIONAL DESCRIPTION

2.1 DC-DC CONVERTER

2.1.1 Operation

The dc-dc converter is a current-mode controlled forward converter operating at 200 kHz. It produces + 5 V for the SSCB and the other connected control tray boards. It also incorporates various self- and system protection features. Input to the converter is the Aux 13.8 V (A+ +) voltage. Reference voltage for the circuit is generated internal to the control chip, U843. System protection features are handled by U842C for overvoltage faults, U842B for under voltage faults, and U842A for insufficient A+ + voltage to protect against over discharge of batteries during battery revert. U842A also provides a test function (Reset_switch*) which allows the converter to run regardless of the input voltage, and concurrently resets the station.

While any of the above fault conditions hold the station reset, only the overvoltage condition will force the converter to shut down. In this case, the converter will turn off and allow the 5 V to discharge down to approximately 2 V before attempting to restart. For a hard fault, the supply will continuously turn off and attempt restart while holding the station in the reset mode. Overcurrent protection for the power supply is provided automatically on a pulse-by-pulse basis due to the current mode control topology (U843-pin 3).

2.1.2 Troubleshooting

In the event of incorrect voltage measured at TP6, Jumper JU12 can be removed to disconnect the station load from the power supply as well as isolating part of the protection circuitry. Before doing this, the type of fault should be determined. If the supply is cycling on and off from approximately 2 V to 6 V, the most likely failure is in the feedback divider network (R2, R7). Either R2 is open or the wrong value, or R7 is shorted or the wrong value. If the fault disappears when the jumper is removed, the problem is in the protection circuit (U842C and associated components).

Overvoltage faults can be caused by any series element from T1 to JU12, as well as feedback divider network errors and failures in the control and driver circuitry on the primary side of the transformer. Overcurrent faults caused by short circuits external to the power supply can be isolated by removal of JU12. Since the supply goes into a fold-back mode during overcurrent, the output voltage drops very rapidly once the current limit threshold value is reached (approximately 1.5 amps). Problems with the station stuck in reset mode with valid + 5 V present at TP6 are most likely caused by circuitry associated with U842B, U842D, Q706, or Q705.

2.2 AUDIO PROCESSING SECTION

The Audio Processing section consists of three parts: receive audio processing, transmit audio processing, and audio routing.

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68P81086E04-O
5/1/92- UP

2.2.1 Receive Audio Processing Section

2.2.1.1 OPERATION

The schematic diagram for this section is on the top left part of Sheet 4. The input to the receive audio processing section is baseband audio, which is demodulated from the RF signal by the receiver in the RF tray.

2.2.1.2 TROUBLESHOOTING

When a strong RF signal is applied to the receiver, the demodulated baseband FM (audio) should be present at RX1 AUDIO (U811–14). For an RF signal with 60% deviation at a 1 kHz modulation frequency, the RX1 AUDIO level should be about 350 mV rms. If this audio is not present, first check the +9.6V supply on TP5 and the VB bias level on U819–12. Next, verify that JU11 is in the proper position. Also check the signal at TP3 QUAD AUDIO, which is not filtered or gated. This signal should have a level of about 300 mV rms. If audio is present at TP3 but not at U811–14, try adjusting the Rx level digital pot U824. If none of these methods works, one of the circuit blocks in the receive audio processing section may have malfunctioned. Each of the following blocks may be checked on an input–to–output basis and repaired if found faulty: PL filter U841, digital pot U824, expander U815, flutter–fighter hybrid HY804, audio gate U811, and op–amps U818 and U819.

2.2.2 Transmit Audio Processing Section

2.2.2.1 OPERATION

The schematic diagram of the transmit audio processing section is shown on the top right part of Sheet 3. The output of this section is TX MOD AUDIO, which is sent to the FM modulator to be impressed upon the RF output of the transmitter, and sent out over the air. This section has several inputs that originate from the SSCB audio routing circuitry.

2.2.2.2 TROUBLESHOOTING

When a large audio signal is applied to the microphone input with a local PTT, the limited and filtered audio signal should be present on TX MOD AUDIO at TP4. If this audio is not present, check the +9.6V supply at TP5 and the VB bias level at U838–5. If the TX MOD AUDIO signal is not found, make sure the mic audio is present at the Tx audio summing amp output U814–1. If this signal is absent, check the Audio Routing Section described in the next paragraph. Also check the signal at U838–7, which should be in full limit (driving the op–amp to its supply rails). Trace the flow of this signal through the splatter filter (U838–7, U838–1, U837–7, U8200–1). The splatter filter output should be similar in peak to peak amplitude to the limiter output, but not so much of a square wave (that is, closer to sinusoidal). If audio is present at U8200–1 but not at TP4, try adjusting the Max Deviation level digital pot, U831. If none of these methods works, one of the circuit blocks in the transmit audio processing section may have malfunctioned. Each of these blocks may be checked on an input to output basis, and any bad ones repaired or replaced.

2.2.3 Audio Routing section

2.2.3.1 OPERATION

Most of the audio routing section is shown on the left half of schematic Sheet 3. Its primary function is to properly distribute audio signals from all sources to all destinations connected to the SSCB. The audio routing section operates on the following audio inputs and outputs, as shown in Tables 1 and 2.

Table 1. Audio Input Description

Inputs	Description
TX AUDIO	Notch filtered audio from TTRC wireline
IN MRTI AUDIO	Audio from MRTI phone patch
LOCAL AUDIO	General purpose audio to/from expansion modules (also common with MIC AUDIO signal)
MIC AUDIO	Audio from local user microphone
RX1 AUDIO	Audio from receive audio processing section
ALERT TONE AUDIO	Audio from alert tone encoder on SSCB
SECURE RX AUDIO	Audio from optional secure board for speaker/wireline
RX2 AUDIO	Processed audio from optional 2nd rcvr board
CODED MOD AUDIO	Audio from optional secure board to be transmitted
TKG MOD AUDIO	TDATA/failsoft from TTRC to be transmitted
SEC ALERT TONES	Tones from option secure board (encode/decode only)
TX DATA AUDIO	General purpose data from expansion modules
GCC DATA AUDIO	1200 or 4800 baud data from optional GCC
RAW TX AUDIO	Unfiltered audio from TTRC wireline
PL ENCODE AUDIO	Audio from PL/connect tone encoder on SSCB
RAC_LN_AUD	Encoder output of optional RAC expansion module

Table 2. Audio Output Description	
Outputs	**Description**
SUMMED TX AUDIO	Audio to transmit audio processing section
LINE AUDIO	Audio to TTRC wireline
SELECT AUDIO	Volume adjusted audio to expansion modules (especially DMP speaker)
OUT MRTI AUDIO	Audio to MRTI phone patch
SPKR AUDIO	Amplified audio to local user speaker
TX AUDIO	Wireline audio to secure board for encryption and to expansion modules
RAW TX AUDIO	Unfiltered wireline audio to optional secure transparent board
LOCAL AUDIO	Local audio to optional secure board for encryption
IN MRTI AUDIO	Audio from MRTI phone patch to secure board for encryption

Some audio inputs are enabled using audio gates, which respond to various PTT and squelch conditions as shown in Table 3. Some other audio inputs are enabled using 3 pin jumpers (see jumper table). TX DATA AUDIO can be summed into the SSCB transmit path before or after the maximum deviation adjust circuit (JU4). GCC DATA AUDIO can be routed through the pre-emphasis/splatter filter path for 1200 baud data or after the maximum deviation adjust for 4800 baud data (JU6).

Table 3. Audio Gate Enabling	
Condition	**Audio Gate**
TX AUDIO	U810A
IN MRTI AUDIO	U817B
LOCAL/MIC AUDIO	U810C
RX1 AUDIO	U810B
ALERT TONE AUDIO	U817C/U817D

2.2.3.2 TROUBLESHOOTING

The routing performed in this section depends on the configuration of the SSCB in the station. This configuration is determined by two factors: code plug programming and jumper settings. If the audio routing section is not performing as expected, one of these two factors is most likely to be the problem. Refer to the jumper table to determine proper jumper settings, and refer to the software description for proper code plug programming. If these two items are found to be correct, and audio routing problems still exist, the circuitry in this section should be checked.

First, check the +9.6V supply at TP5 and the VB bias level at U810–1. If an audio gate does not operate as expected, check the audio gate control input. A high level (about +9.6V) at the control inputs of T-gates U810, U811, and U812 allows audio to pass through the positive gate (no bubble shown at the input) and shuts off the signal from passing through the negative gate (with a bubble). Conversely, a low level on the control input allows audio to pass through the negative gate and shuts off the positive gate. Thus, for audio gate U817, a high level (about +9.6V) at the control input allows audio to pass, and a low level shuts it off. If the control input is correct, but the gate does not respond properly, the audio gate IC is probably bad. If the control input is not as expected, check the level shifters U813 and U816. These ICs shift the 0–5V ASIC control outputs to the 0–9.6V levels required by the audio gates. A low voltage on the input of the level shifter should drive the output low, and a +5V level on the input should drive the output to +9.6V. If that's not what happens, the level shifter IC is probably bad. If none of the foregoing checks isolates the cause of the audio routing problem, check quad summing amp U814. If audio is present on the resistor inputs but not on the outputs, and the +9.6V and VB levels are correct, U814 is probably bad.

2.3 SQUELCH CIRCUITRY

The squelch detection circuitry on the SSCB responds to the signal strength of the incoming receiver audio. The QUAD AUDIO signal from TP3 is routed both to the receiver and to the repeater squelch detectors. These detectors drive control lines to the logic section, which are used in keyup and gating arbitration. For information on PL and DPL coded squelch operation, refer to the logic section of this description.

2.3.1 Troubleshooting

Properly operating squelch detectors should indicate squelch conditions when an RF signal below the adjusted threshold is being received. The detectors should unsquelch as soon as the signal strength goes above the set level. If the squelch circuit malfunctions, first try adjusting the digital pots in the receiver and repeater squelch detection circuits. A relatively easy and quick way to check the operation of the squelch circuitry is to use the ACC DIS switch on the front panel to enable the front panel Squelch control. With no RF input to the station, a noisy signal should appear on TP3 QUAD AUDIO. With the Squelch control fully CW, this noisy input should squelch the receive audio. With the Squelch control full CCW, the detector should not squelch the receiver, and the noisy signal should pass through to the speaker. If the receive channel has PL/DPL connect tone enabled, the PL DIS switch must also be used to hear the signal at the speaker. If these simple checks don't isolate the source of a squelch problem, refer to the squelch troubleshooting chart in the manual.

2.4 LOGIC HARDWARE SECTION

The logic hardware description can be broken down into five broad parts: microprocessor core, data communications circuitry, tone encoders/decoders, general I/O, and reset circuitry.

Many of the functions of the logic section are implemented with Application Specific Integrated Circuits (ASICs). The SSCB uses two of these custom ASICs, which were specifically designed for this product. The ASICs can operate in one of two modes, depending on the state of the MODE pin (18). U801 operates in the standard mode (with MODE pulled high), and serves as a specialized microprocessor support chip, with additional I/O and data communication features. U802 operates in the I/O mode (with MODE pulled low), and serves as an addressable collection of input buffers and output latches.

2.4.1 Microprocessor Core

The schematic diagram of the microprocessor core is located on Sheet 2. Its function is to run the software that controls the station. Most of the core functions are carried out using five integrated circuits.

2.4.2 Data Communications Circuitry

The SSCB logic section communicates with other modules in the station through three primary channels; the IPCB, the MUXbus, and the high speed ring (HSR).

2.4.3 General Input/Output

The SSCB logic section has a great deal of input/output (I/O) capability, which is needed to control station functions and monitor station status. The I/O section also allows a local user to change the state of the station, and to observe station status conditions.

2.4.4 Tone Processing

2.4.4.1 TONE ENCODING AND DECODING

Two 4-bit encoders are included on the SSCB. They are driven by 8-bit latch OL10 from the I/O ASIC. The tone decoding capabilities of the SSCB are complementary to its tone encoding functions. The SSCB detects incoming PL tones or DPL codewords in a conventional coded squelch system, and incoming connect/disconnect tones in a trunked system. These tones and/or codewords are part of the receiver modulation.

2.4.5 Reset Circuitry

The power up reset circuitry is shown on the bottom of schematic Sheet 1. A block diagram of this section is also shown in Figure 1.

DELAYED RESET is inverted by Q822 to form EXPANSION RESET*, which should hold other control tray boards and expansion modules in reset during SSCB self-diagnostics. The microprocessor can also activate EXPANSION RESET* during normal program execution, by turning on Q823 with a general purpose output pin.

2.4.6 Logic Hardware Troubleshooting

The SSCB software is capable of generating several error codes on the front panel seven segment display. Refer to the SSCB software description section for a list of these diagnostic error codes.

If there is a suspected failure in the SSCB logic section first check the + 5V power supply pins on each of the logic devices U800 through U804, and on U807. Next, look at the RESET* line at TP10. This line should be at a steady high, with no superimposed pulses. Also look at the DELAYED RESET line, which should be at a steady low with no superimposed pulses. If the signals on the reset lines are not as expected, check to see that ICs U800 through U804 are all properly seated in their sockets. (Improper seating is especially likely for 28-pin DIP U803.) Also verify that EPROM U803 is programmed with the correct version of the software for the particular SSCB being worked on. (U803 must be compatible with the EEPROM codeplug programming internal to U800, or the system will not work) Next, check to see that the address timing signals (A0–A7) for the demultiplexed low order address bus are present at the relevant outputs of U801 (pins 66–73). If the A0–A7 address timing signals are not found, ASIC U801 is probably bad. If ASIC U801 and EPROM U803 both seem to be OK, and the RESET* line is high, next check microprocessor U800. A properly functioning U800 will drive the E line (U800–5) with a 1.9872 MHz square wave. If all these chips seem to be functioning properly, check ASIC U802 for data bus inputs as well as correct output latch levels.

If an error code indicates that there is a problem with the HSR, first verify that JU1 and JU2 are installed in the correct positions. Next, verify that HSR CLK is an E/2 frequency square wave, and that HSR SYN goes high every 40 HSR CLK cycles. If these signals seem to be correct, but HSR problems still exist, remove the modules from J804 and/or J803, and place JU1/JU2 in the HSR loopback position (JU1 alternate, JU2 normal position). If the error code persists with all other modules disconnected and the HSR looped back by JU1/JU2, then U801 is probably bad.

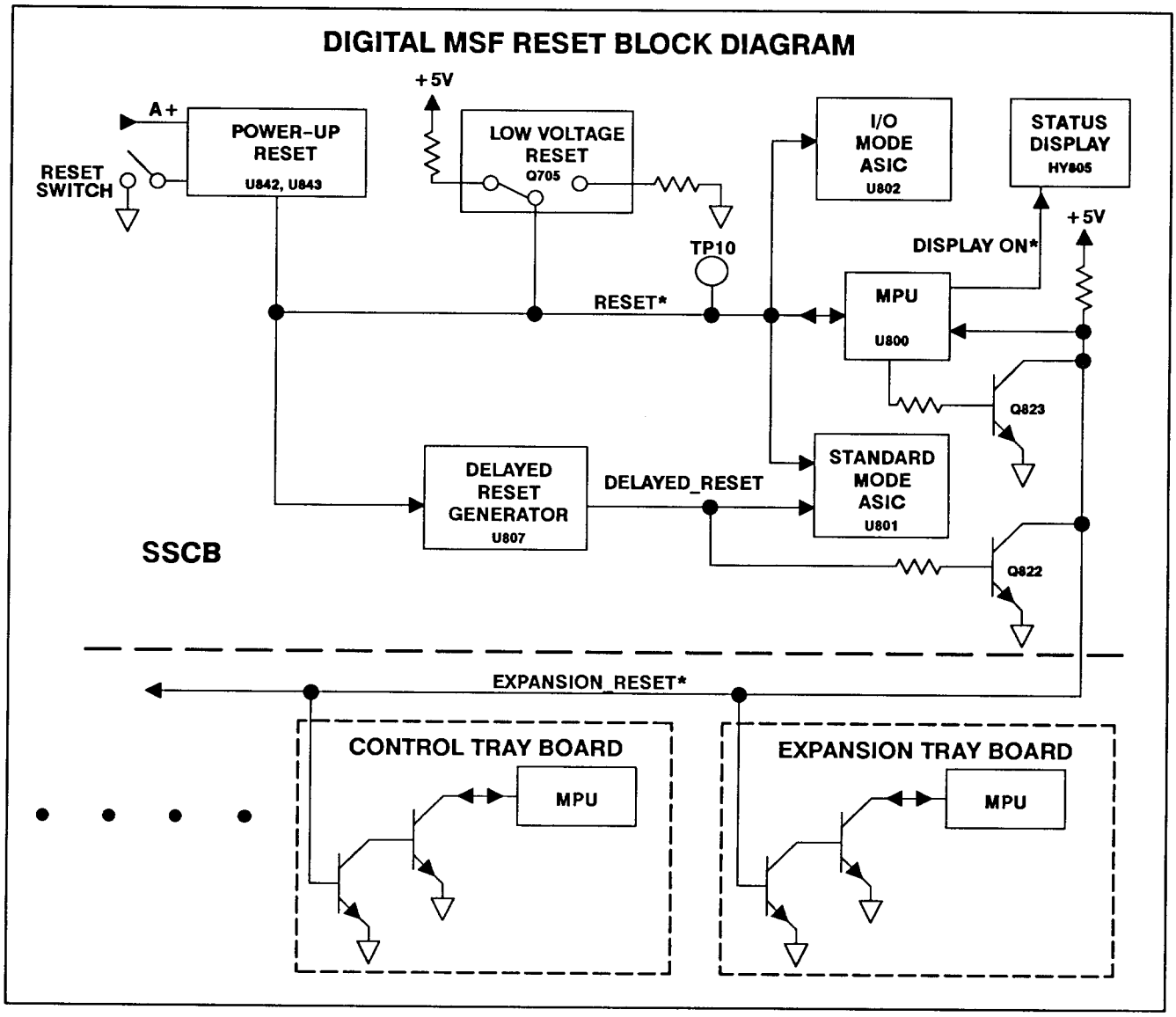


Figure 1. Digital MSF Reset Block Diagram

If problems are encountered with the MUXbus, verify that DS* is a 3105 Hz square wave and that the address lines are being driven. The address nibble BA0–BA3 must be incremented modulo–16 for proper operation. This means that the BA0 line (which toggles at DS*/2 rate = 1553 Hz) should toggle twice as fast as BA1 (DS*/4 = 776 Hz), which is twice as fast as BA2 (DS*/8 = 388 Hz), which is twice as fast as BA3 (DS*/16 = 194 Hz). To verify proper MUXbus data generation, the SSCB can be forced to write to the MUXbus BD0*–BD3* bits. When a MUXbus data bit is set at only one MUXbus address, the signal on the specific MUXbus data pin should be a short low–going pulse from the 5V high level, repeating at a frequency of DS*/16 = 194 Hz. The following chart (Table 4) indicates one way to force the SSCB to drive a MUXbus data bit at only one address: If these signals cannot be verified, ASIC U801 is probably bad.

Table 4. MUXbus Addressing

Signal	Action
BD0* (U801-38)	depress XMIT switch
BD1* (U801-39)	depress XMIT switch
BD2* (U801-40)	ground TP9 (LOC PTT)
BD3* (U801-41)	set to CH1-using ACC DIS, SELECT/CHANGE switch

The procedures for troubleshooting the tone encoders/decoders and wattmeter buffers are similar to those already suggested for troubleshooting the audio sections. Each circuit block can be analyzed on an input to output basis, and any malfunctions isolated and repaired.

When a PL signal is present on the receive audio, the PL DECODE DATA (U800-32) signal should be a 0-5V square wave of the same frequency. An easy way to verify the wattmeter buffer operation is to monitor the buffer outputs (FWD PWR U806-8 and RFL PWR U806-14). The DC levels on these outputs should respond to front panel Po power adjustments while the transmitter is keyed. The tone encoders can be checked by looking at the output of the D/A filters. When an alarm condition is present, an alert tone sine wave burst should be visible at U818-1. Alarm tones can be generated by setting DMP bits at MUXbus address 12. When PL/DPL/connect tones are being generated, a sine wave should be visible at U8200-1. DPL code 031 can be generated by keying the station with a LOC PTT with the station set to channel 1, mode 1.

2.5 SOFTWARE DESCRIPTION

The Station Control board firmware begins execution at the location contained in its RESET vector whenever the station powers-up or is reset. This location is the beginning of the main background routine of the Station Control board firmware. Once initialized, this routine is basically nothing but an endless loop (the background) which calls all of the non-interrupt-driven routines. However, at its beginning, the firmware calls a startup diagnostics module, "sscb_reset_diags.asm," which runs to completion before the background loop begins. As the name implies, this module performs diagnostic tests of the Station Control board. When the diagnostics begin (i.e.: immediately upon station power-up), all segments and digits of the three digit, seven segment Status display LED should light, and stay lit until the circuitry that drives the display has been verified. This indicates that the Station Control board has started its diagnostics.

The sscb_reset_diags.asm routine must initialize some of the registers in the microprocessor before the actual hardware diagnostic tests can start. These registers determine the microprocessor's Computer Operating Properly (COP) watchdog time-out time; set up the Serial Communications Interface (SCI) to communicate at the same baud rate and with the same message protocol as the other boards on the Inter-Processor Communications Bus (IPCB), and set up a service to bypass the flag that normally tells the board to access its EEPROM.

When initialization is complete, the routine sets an output pin to hold the Expansion Reset line active. This prevents the on-board circuitry that activated Expansion Reset immediately upon Station reset or power-up from releasing the line after about 200 milliseconds, which would hold any and all remote boards in reset. The Station Control board diagnostics now begin. Since these tests can yield a number of error conditions, errors are indicated either by flashing the Station Control board's entire Status display or by displaying a formatted error code within the Status window. There are two types of error classes: fatal and non-fatal. Fatal errors are severe enough to prevent proper operation of the Station Control board, and cause the Station Control board to reset. Non-fatal errors, however, are just warnings. They are not severe enough to prevent operation, and should not cause a reset.

Failures of some of the initial diagnostics tests described below are indicated by flashing of the entire Status display. At this point, the operation of the display-driving circuitry, IRQ-interrupts, and external RAM has not yet been verified. The display-driving circuitry and IRQ interrupts are required for displaying error codes within the Status window, and the external RAM is needed to hold the error codes for display. The Status window display cannot be used until those tests have been done.

All failures that flash the entire Status display are fatal errors. For each error of this type that it finds, the sscb_reset_diags.asm routine calls a specific error handler routine, which contains a number peculiar to that error. The error handler flashes the Status display for that specific number of repetitions, to identify the error. It then goes into a wait condition, not servicing the COP timer, which eventually times-out and resets the Station Control board. Failures that display error codes in the status window, on the other hand, may be fatal or non-fatal. When sscb_reset_diags.asm detects an error of that type, it calls a different error handler routine, which writes an error code value to the front-panel Status window. If the error code is fatal, the Station Control firmware displays it for five seconds and then stops servicing its COP timer. Again, COP eventually times-out and resets both the Station Control Board and, via the Expansion Reset line, any board(s) connected to it. If the error code is non-fatal, the Station Control firmware displays it for two seconds and continues without a reset.

If a fatal error is left uncorrected, the test that found it will, of course, fail again, re-display the same error code, and once more reset. This is an endless cycle that will continue until the failure is corrected.

Sscb_reset_diags.asm checks two major sections of the Station Control board hardware: the digital hardware and the audio hardware. Internal digital diagnostic tests are done first, followed by external digital diagnostic tests, followed by audio diagnostic tests. All tests are performed after every Station Control board reset. Internal digital diagnostic tests are tests which verify operation of the Station Control board's digital circuitry as stand-alone hardware. External digital diagnostic tests verify operation of the Station Control board's digital circuitry as part of the overall Station Control Tray. Finally, audio diagnostic tests verify operation of the Station Control board's audio circuitry.

The first internal digital diagnostic test checks that the segment-select lines of the Status display and the internal IRQ signal are working properly. If not, the specific error handler called should flash the entire display twice, then reset the board.

The second internal digital diagnostic test checks that each of the eight bits in every byte of the external RAM can be toggled high and low. After each RAM byte is checked, it is cleared so that all RAM bytes will initially be zero when the diagnostics are complete. If any external RAM byte fails this test, the specific error handler called should flash the entire display four times, then reset the board.

The third internal digital diagnostic test checks that the IRQ (Interrupt Request) is working. The IRQ interrupt should be generated whenever 640 microprocessor E-cycles have been clocked by the MUXbus-driving portion of the standard ASIC. It should occur every 320.061 µsec (640 cycles at 1,987,200 cycles per second). It signals the Station Control board that new MUXbus data is ready to be read, updates the Station Control Software System Timer, and controls the multiplexing of the front-panel display. If this interrupt test fails, the specific error handler called should flash the entire display twice, then reset the board. If it passes, the front-panel display, which should have shown three eights (8.8.8.) up to this point, should become blank.

The fourth internal digital diagnostic test checks that each of the eight bits in every byte of the internal RAM in the microprocessor can be toggled high and low. After each RAM byte is checked, it is cleared so that all RAM bytes will initially be zero when the diagnostics are complete. If any byte fails to pass this test, an error handler routine is called to write the relevant fatal error code to the front-panel Status window. (This and all the following diagnostic tests display their results in the Status window, since at this point the display circuitry has passed its diagnostic tests and is, therefore, available.)

The next section of the sscb_reset_diags.asm routine checks the microprocessor configuration, i.e. checks the information stored in its CONFIG register. If the information is wrong, the routine checks to determine whether or not it can be corrected without total erasure. If so, sscb_reset_diags.asm makes the correction and writes a fatal error code to the Status window. If not, sscb_reset_diags.asm erases the CONFIG register, which erases the entire internal EEPROM, and reprograms CONFIG for the desired features. (Note that erasing the CONFIG register erases the entire internal EEPROM, which is the codeplug.) The routine then writes a different fatal error code to the Status window. In either case, COP will then time-out and reset the system.

Being reset will, of course, restart the diagnostics (i.e.: repeat sscb_reset_diags.asm). However, since the CONFIG register was (ideally) corrected before the system reset, this test should not fail on the second pass. Note, though, that if the internal EEPROM was erased, the Station Control firmware may get caught in a fatal error loop due to some other error.

Unless otherwise specified, failures in all the following tests are fatal errors. When one of these happens, the diagnostics write a fatal error message to the status window, and reset the system. In fact, until the problem is corrected, the system may be expected to continually recycle the diagnostic routines, failing and resetting repeatedly at the same point, which is the "fatal error loop" referred to above.

The diagnostic routine next calculates the single-byte-add checksum of the Station Control firmware. The test fails if this calculated checksum does not match the value stored in the Station Control firmware.

Sscb_reset_diags.asm next tests the Standard and I/O ASICs. The ASIC tests are considered to be internal tests, meaning that each ASIC is tested as a stand-alone device (i.e.: all outputs are looped back to the inputs). (In the external diagnostics section of the routine, the ASICs are tested as part of the overall Station Control Tray.) The first test performed on the Standard ASIC is verification of its Output Latches. The test routine writes a known set of data to the Output Latches; then reads back the corresponding loopback Input Buffers. The test fails if the Output Latches and Input Buffers do not agree.

The second test of the Standard ASIC checks the MUXbus circuitry. The routine first checks MUXbus address cycling. Next, it checks the operation of the the Data Strobe line, verifying that both 1s and 0s can be read at all MUXbus addresses. A discrepancy in either addressing or data integrity is a failure.

The next set of tests on the Standard ASIC is associated with the High Speed Ring (HSR). The first HSR test is an operational check of the Ring Synchronization and Ring Clock lines. The diagnostic routine first reads two watchdog bits (one for Ring Sync and one for Ring Clock), in the Standard ASIC hardware to determine whether or not Ring Sync and Ring Clock are operating properly. Next, it writes a known set of data to the Station Control portion of the HSR, and then reads back the entire HSR. If the data written to and read back from the Station Control portion do not match, or if the Trunked Tone Remote Control and Secure portions are not zero, the HSR fails. (The Station Control board is in internal test mode at this point, and should not be connected to the HSR. Therefore, the Trunked Tone Remote Control and Secure boards should not be able to write to the HSR.) If the test passes, it repeats with an inverted version of the same data set, using the same pass/fail criteria.

The next section of sscb_reset_diags.asm compares various parameters of the Station Control codeplug and the Station Control firmware. The codeplug data must first be read from EEPROM into RAM. (If an external, serially-addressed EEPROM is present on the Station Control board, its data will also be read into RAM. A serially-addressed EEPROM that does not respond to commands is a failure.) After the routine reads the EEPROM(s), it clears the flag that has bypassed EEPROM access prior to this point. The first comparison is between the Module ID stored in the codeplug and the Module ID stored in the

firmware. The second comparison is between the codeplug version and the firmware version. The third comparison is between the single-byte-add checksum of the Station Control codeplug. as calculated by the diagnostic routine, and the checksum value stored in the Station Control codeplug. A mismatch in any of these comparisons is a failure.

The routine next checks to determine whether or nor there was a reset during an EEPROM update. An image of the EEPROM is always kept in RAM. A user can write this RAM image (which he or she may have modified) to the EEPROM by issuing a Write-EEPROM-From-RAM command via the IPCB. This command first erases the entire EEPROM, setting all bytes to hexadecimal value FF. The firmware then does a byte-by-byte copy of the modified RAM image to the EEPROM area, which can take up to 15 seconds. The copy starts at the ***second*** byte in the EEPROM address space. The ***first*** byte, which was previously set to FF hex during the erasure, is not overwritten until the copy has been completed, at which time it is set to 00. If the copy is interrupted by a reset before completion, that doesn't happen. Therefore, if the first byte in the EEPROM address space is non-zero it indicates that the EEPROM may be corrupted, and is a failure.

The routine next checks to determine whether or nor there was a reset during a user area update. What's stored in the user area is dynamically-changeable data that must be preserved between resets, so this area is part of the EEPROM address space. An update of the user-area should reprogram only the bytes in that section of the EEPROM, one of which is a user-area check byte that functions for the user area in the same way that the first byte of the EEPROM functions for the entire EEPROM. That is, the check byte is initially erased to FF hex, and cleared to 00 when the update is completed. Therefore, a non-zero value of the check byte indicates that the user area may be corrupted, and the diagnostics will flag it as a failure.

The last of the internal tests in the diagnostic routine checks the IPCB. The routine writes a test pattern to the IPCB, then checks to determine whether or not the data was received properly.

At this point, the internal Station Control diagnostics are complete. Audio diagnostic tests may now begin. The Disable LED should light to indicate that the digital hardware tests have been completed, and three dashes (- - -) should be displayed in the front-panel Status window to indicate that audio diagnostics are in progress.

The diagnostic routines first check the Analog-to-Digital (A-to-D) Converters of the microprocessor. If any of the A-to-D Converters fail, the diagnostics should send a ***non***-fatal error code to the Status window for display. A non-fatal error that occurs in this section of the diagnostics is handled differently from fatal errors that occurred in the previous section. Once the non-fatal error code is displayed, the operator has two seconds to activate the Acc Dis switch on the front panel of the station. This "freezes" the system at the current stage of the diagnostics, to expedite troubleshooting. (Among its other advantages, this allows audio gating, which may not be possible in normal operation.) If the switch is hit late, freezing the routine at the wrong stage, the operator can simply hit the Reset switch and try again on the next pass.

Failures in all of the remaining tests are non-fatal errors; and should display the appropriate non-fatal error codes in the Status window.

The routine first checks the PL Tone generator circuit. If the192.8 Hz tone is not present at the appropriate A-to-D Converter input when the tone is enabled, the test fails.

The routine next checks the Alert Tone generator. If the 1000 Hz tone is not present at the appropriate A-to-D Converter input when the tone is enabled, the test fails.

The routine next checks the Station Control board for PL signal at the transmitter. If the 192.8 Hz tone is not present at the TP4 A-to-D Converter input when the tone is enabled, the test fails.

The routine next checks the alert tones at the the transmitter. If a 1 KHz test tone shows an unusual characteristic at TP4 while the maximum deviation EEPOT is adjusted, or the test tone is present when it should not be, the test fails.

The routine next checks the receiver audio paths. If a 1 KHz test tone shows an unusual characteristic in the receive path while the receive level EEPOT is adjusted, the test fails.

The routine next uses the alert-tone encoder to apply a 100 Hz tone to the PL-decoder input, and checks for proper waveform at that input. If an unexpected tone period is detected, the test fails.

The routine next tests the receiver and repeater squelch circuits. With loose squelch, the absence of receiver or repeater squelch activity is a failure. With tight squelch, the presence of receiver or repeater squelch activity is a failure. If these tests pass, while retaining the same tight squelch, the diagnostics cause a signal to be looped back to the squelch-detector circuits to simulate receiver quieting. Absence of squelch activity is now a failure.

The routine next checks Line and Receive Audio paths for continuity. A 1000 Hz test tone is used for this purpose, and if it is either there when it shouldn't be, or not there when it should, the test fails. The diagnostics then check the Repeat path in the same way, with the same test tone.

Finally, the diagnostics re-enable the 1000 Hz test tone, and check for it at TP1 (select audio). If it's not there, the test fails. Lastly, the routine disables the tone and checks for it again. This time, the test fails if it is there.

Audio diagnostics are now completed. At this point, the dashes (- - -) should be blanked from the Status window to indicate completion of diagnostics to the operator.

The routine should now attempt to set all EEPOTs to the shadow values kept within EEPROM. If any one EEPOT takes too long to set, that is a fatal error, the relevant fatal error code code will be generated and displayed in the Status window, and the system will reset. This is the last point at which an SSCB error can occur. If that doesn't happen, Expansion Reset is now released, allowing the remote boards to begin their own diagnostics. The routine will indicate this by displaying the version number of the Station Control firmware in the Status window.

When each remote board completes its own internal diagnostics, it waits for an instruction from Station Control. This can be either a "shut up" or a "wake up" command. (The routines that control this on remote boards time-out in 10 seconds. If they receive no commands before time-out, they put their boards into background mode.) At this point in its execution, the diagnostics routine simply orders all remote boards to shut up. If any board refuses to comply, mutiny is assumed and a fatal error results.

While the diagnostic software is attempting to communicate with the remote boards, and also while each remote board is performing its own external diagnostics, the Status window will again display three dashes (- - -), to indicate this condition.

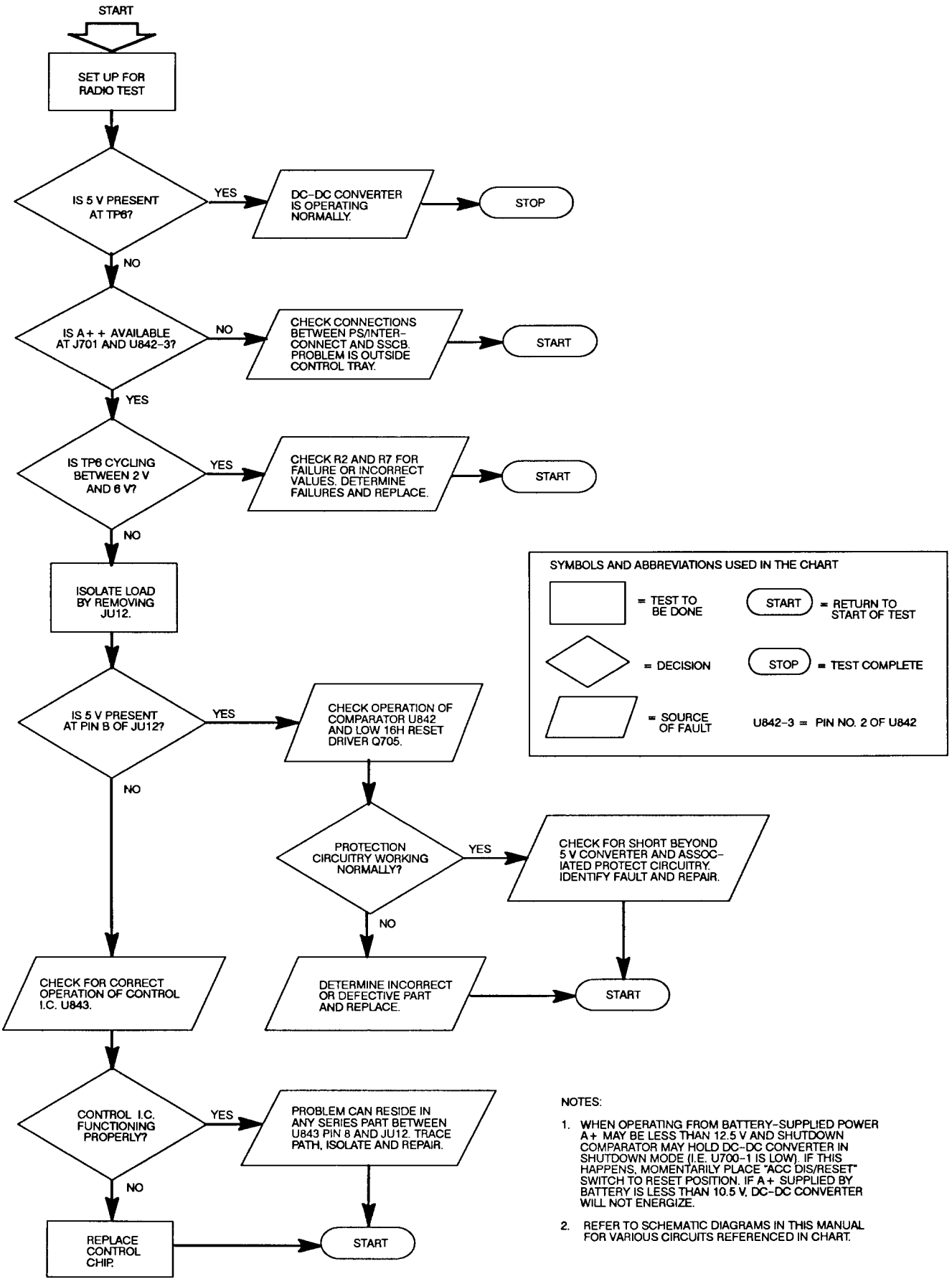
When all boards have agreed to shut up, Station Control asks the first one (TTRC, if present) to wake up and begin its own external diagnostics. The board has five seconds to send something over the IPCB. This can be its own IPCB test message, a fatal or non-fatal error code, or its firmware version number. Error codes received will be displayed in the Status window (fatal ones, of course, will remain in the window for five seconds before the Station Control board resets the entire station.) Reception of a remote board's firmware version number signals the completion of that board's diagnostics. Before displaying the version number, however, Station Control requests the Station Type and System Version bytes from the remote board. If any of those bytes don't match what Station Control has stored within its codeplug as the correct value, that is a fatal error. (This check ensures that only compatible boards can be used within a station). If all bytes match, the version number of the board goes up in the Status window, and the next remote board in line is called up to go through the same procedure. This procedure continues until there are no more remote boards in line. Any remote board that refuses to wake on command is, again, assumed to be in rebellion, and will cause a fatal error.

When the firmware version numbers of all remote boards in the station have been displayed in the Status window of the Station Control board, this means that all boards have run and passed their individual diagnostic routines. Having reached this point, sscb_reset_diags.asm will turn off the Disable LED, and issue a command to each board in turn to enter its background mode. This is the last chance for a remote board to mutiny by refusing the command, creating a fatal error and resetting the system. Assuming that no remote board chooses to do this, Station Control will now clear the Status window, call a variable-initialization routine, and go into its own background processing mode.

Table 5. Secure Station Control Board Jumpers

Jumper #	Description	Normal Position	Alternate Position
JU1	TTRC HSR	TTRC in	TTRC out
JU2	Secure HSR	Secure out	Secure in
JU3	Coded Mod audio	Secure out	Secure in
JU4	post-IDC Tx Data	post-IDC Tx Data out	post-IDC Tx Data in
JU5	Trunking Mod audio	TTRC in	TTRC out
JU6	4800 GCC Data	4800 GCC out	4800 GCC in
JU7	Rx2 Wireline	no Rx2 to wireline	Rx2 to wireline
JU8	Rx2 audio	Rx2 out	Rx2 in
JU9	Secure Alert Tones	Secure out	Secure Enc/Dec in
JU10	Secure Rx audio	Secure out	Secure in
JU11	Rx Diversity audio	no Rx Diversity audio	Rx Diversity audio
JU12	+5V Supply	+5V load in	+5V load out
JU13	rf tray +5V	no +5V to rf tray	+5V to rf tray
JU14	1200 GCC Data	1200 GCC out	1200 GCC in
JU15	pre-IDC Tx Data	pre-IDC Tx Data out	pre-IDC Tx Data in
JU16	Exp Tx audio select	Processed Tx audio to J800	Raw Tx audio to J800
JU17	SAM Line audio	SAM audio not routed to line	SAM audio routed to line
JU18	RX1 gate control	controlled by logic section	controlled by squelch section
JU19	MPT squelch to Exp Conn	Fast key from J800	MPT squelch from J800
JU20 *	Secure coded mod gain	high gain	low gain
JU21 *	Wattmeter A-D resolution	use for high power stations	use for low power stations
JU22 *	Wattmeter A-D resolution	use for high power stations	use for low power stations

* Not present on earlier versions.

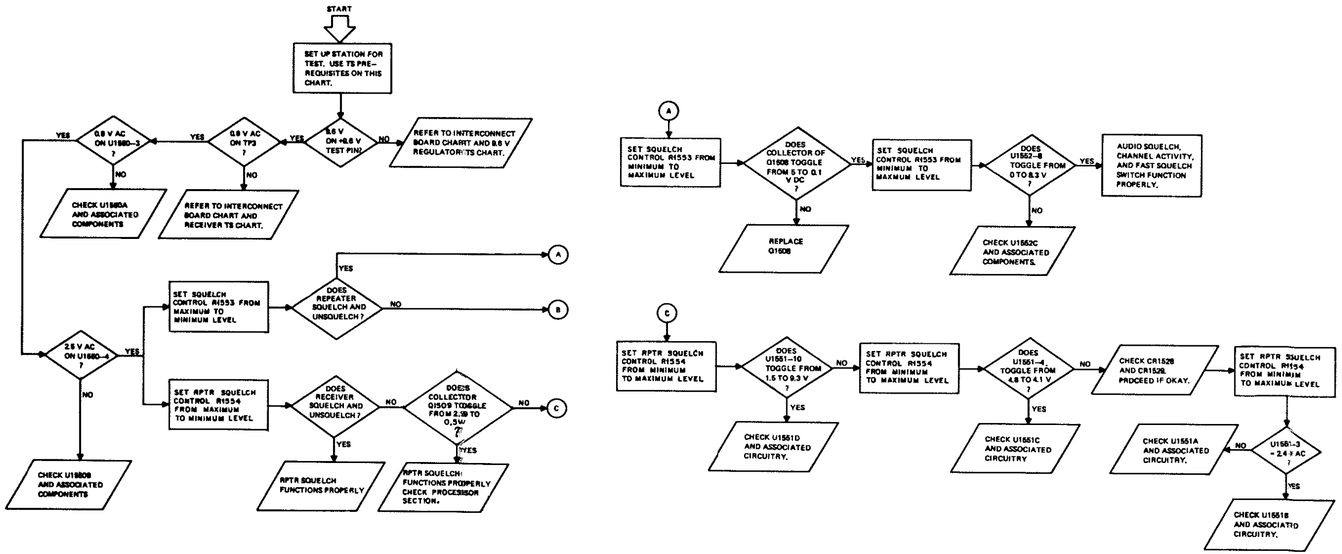


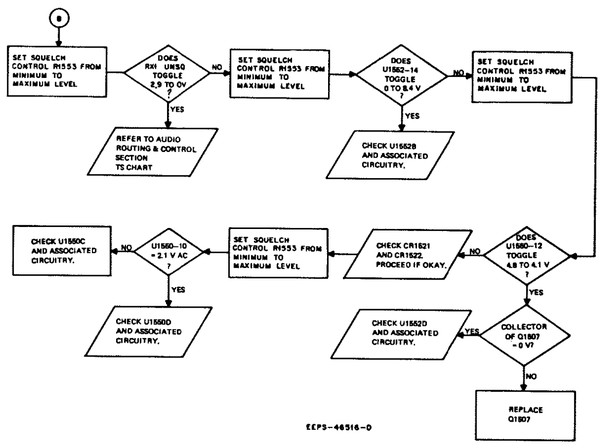
NOTES:

1. WHEN OPERATING FROM BATTERY-SUPPLIED POWER A+ MAY BE LESS THAN 12.5 V AND SHUTDOWN COMPARATOR MAY HOLD DC-DC CONVERTER IN SHUTDOWN MODE (I.E. U700-1 IS LOW). IF THIS HAPPENS, MOMENTARILY PLACE "ACC DIS/RESET" SWITCH TO RESET POSITION. IF A+ SUPPLIED BY BATTERY IS LESS THAN 10.5 V, DC-DC CONVERTER WILL NOT ENERGIZE.
2. REFER TO SCHEMATIC DIAGRAMS IN THIS MANUAL FOR VARIOUS CIRCUITS REFERENCED IN CHART.

SECURE CAPABLE STATION CONTROL BOARD

RECEIVER AUDIO AND SQUELCH CONTROL TROUBLESHOOTING CHART





EEPS-46516-O

SYMBOLS AND ABBREVIATIONS USED IN THE CHART

ALL VOLTAGE MEASUREMENTS ARE DC, UNLESS OTHERWISE STATED. AC VOLTAGES ARE MEASURED WITH AN AVERAGE RESPONDING METER.

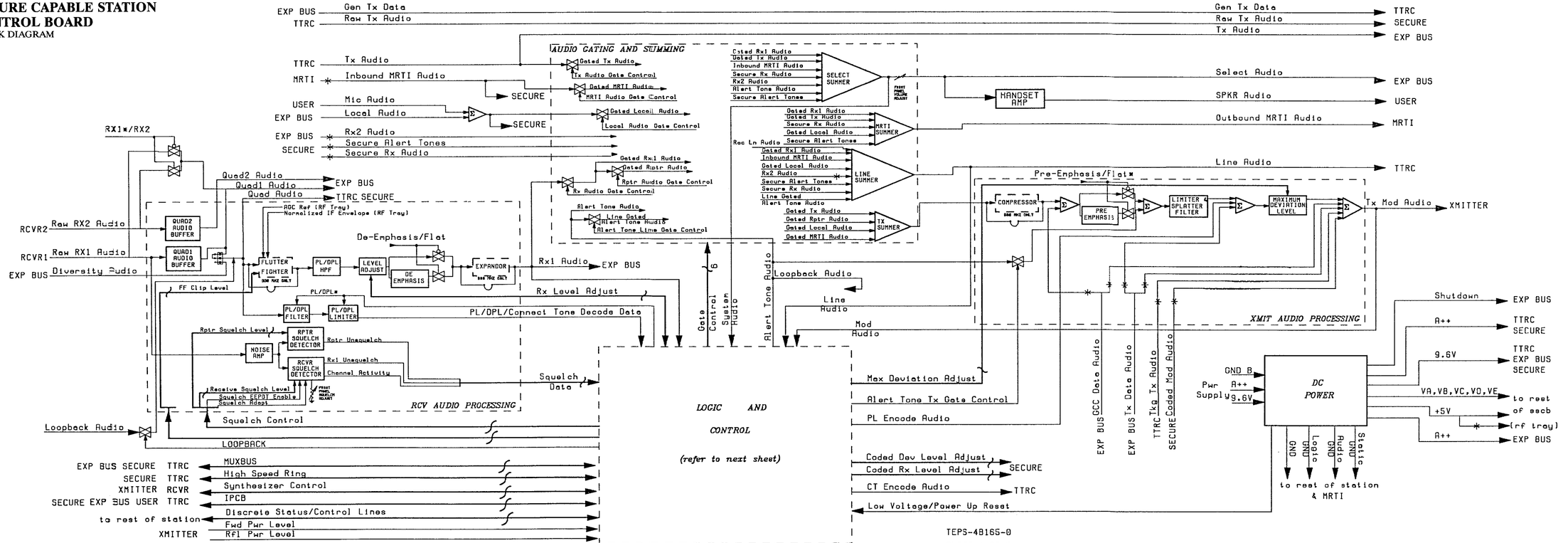
- = TEST TO BE DONE
- = DECISION
- = SOURCE OF FAULT

TS	= TROUBLESHOOTING
U1550-3	= PIN 3 OF U1550
CW	= CLOCKWISE
CCW	= COUNTERCLOCKWISE

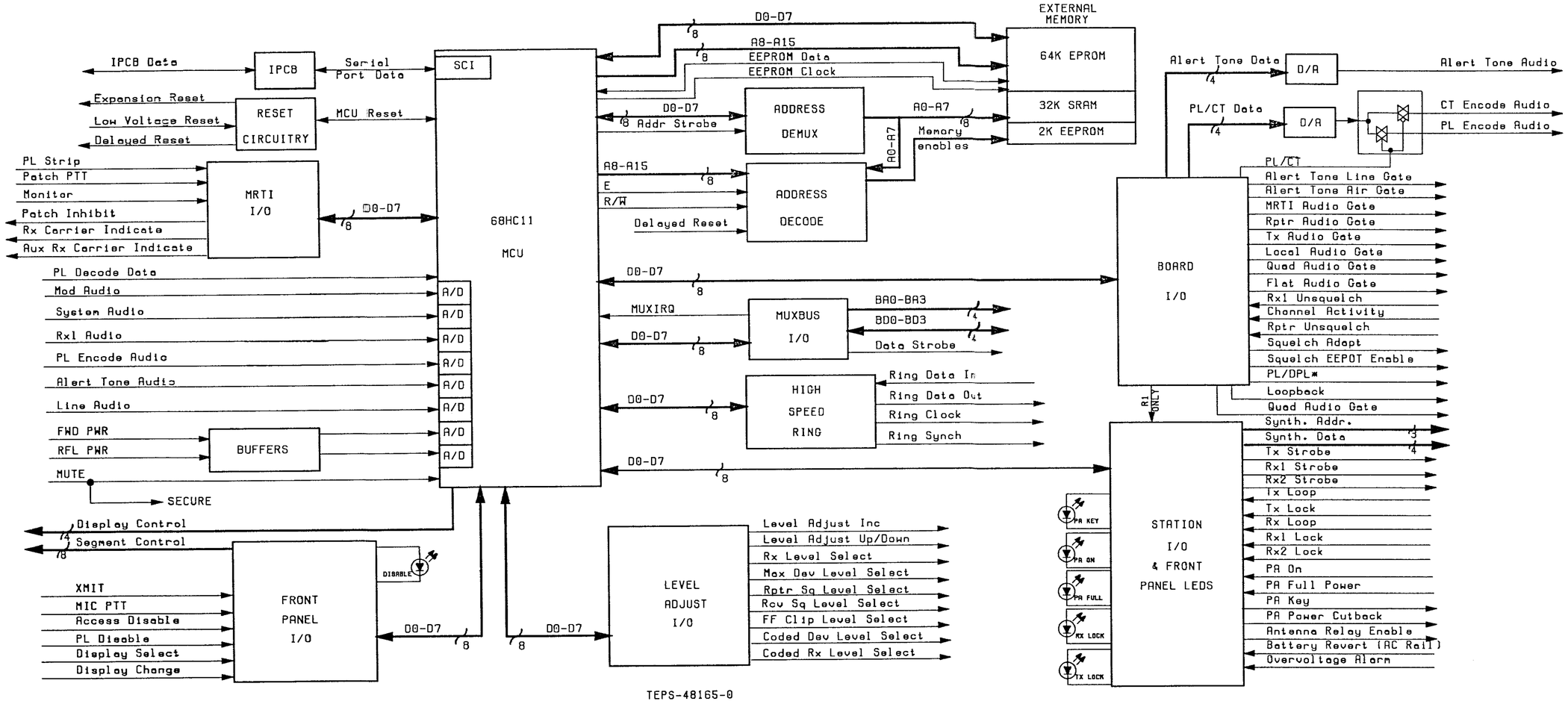
TROUBLESHOOTING PREREQUISITES:

1. ENERGIZE STATION. RECEIVE SYNTHESIZER MUST BE LOCKED (RX LOCK LED LIT). IF NOT, PERFORM RECEIVER TROUBLESHOOTING PROCEDURE.
2. PL DISABLE STATION BY PUTTING SW800 IN THE PL DIS POSITION (UP).
3. ACCESS DISABLE STATION BY PUTTING SW801 IN THE "ACC DIS" POSITION. (UP)
4. PROVIDE A MEANS OF LISTENING TO LOCAL AUDIO. PLUG PORTABLE TEST SET INTO J812.
5. THERE SHOULD BE NO RF SIGNAL PRESENT AT THE RECEIVER INPUT (DISCONNECT ANTENNA).
6. WHEN TROUBLESHOOTING IS COMPLETE, READJUST THE AUDIO AND REPEATER SQUELCH SECTION TO PROPER SYSTEM SPECIFICATIONS.

SECURE CAPABLE STATION CONTROL BOARD
BLOCK DIAGRAM

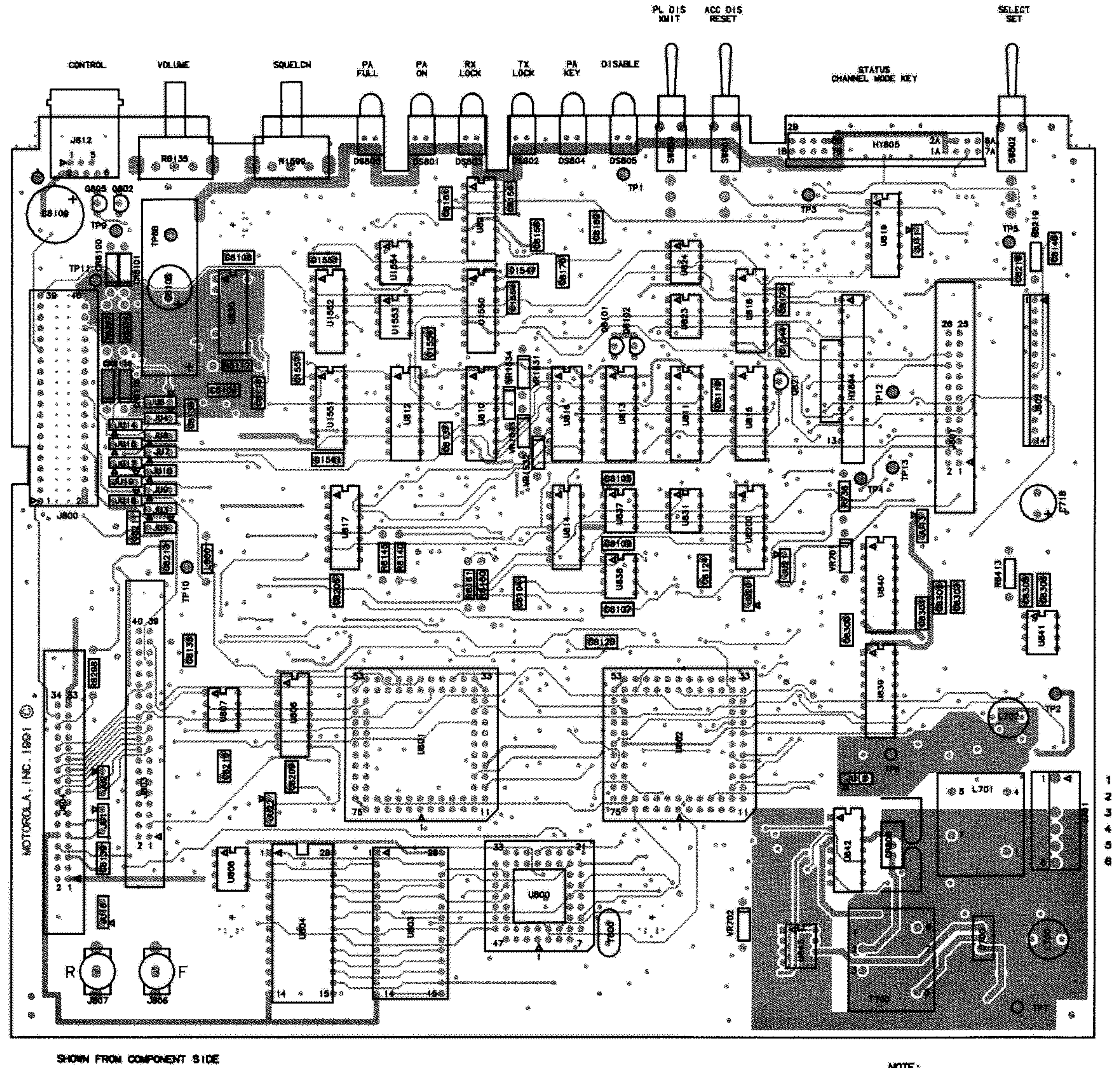


SECURE CAPABLE STATION CONTROL BOARD
BLOCK DIAGRAM



TEPS-48165-0
SHEET 2 OF 2

SECURE CAPABLE STATION CONTROL BOARD
CIRCUIT BOARD DETAIL



SHOWN FROM COMPONENT SIDE

OL - TEPS - 48145-A

BD - TEPS - 48146-A

1 Aux +13.8V (A++)
2
3 Overvoltage Alarm *
4 Battery Revert * (AC Fail*)
5 Gnd B
6 Normalized IF Envelope (800/896 MHz)

NOTE:

AN ASTERISK (*) FOLLOWING A SIGNAL NAME INDICATES AN ACTIVE LOW LEVEL SIGNAL.

J802
PIN OUT DETAIL

Pin	Signal
1	Logic Gnd
2	MRTI PL Strip *
3	Logic Gnd
4	MRTI Monitor *
5	MRTI PTT *
6	Logic Gnd
7	Audio Gnd
8	IN MRTI Audio
9	Logic Gnd
10	Out MRTI Audio
11	MRTI Rx Carrier
12	MRTI Inhibit
13	N.C.
14	MRTI Aux Indicate
15	N.C.
16	A++
17	A++
18	Audio Gnd
19	N.C.
20	N.C.

J800
PIN OUT DETAIL

Signal	Pin	Pin	Signal
Quad 1 Audio	39	40	Audio Ground
Audio Gnd	37	38	Rx1 Audio
Rx2 Audio	35	36	Tx Audio
Local Audio	33	34	Tx Data Audio
QCC/RRAC Data Audio	31	32	Select Audio
Quad 2 Audio	29	30	Diversity Audio
Audio Spare	27	28	Gen Tx Data
Logic Spare	25	26	Audio Spare
Shut Down	23	24	Logic Spare
Logic Gnd	21	22	DS *
BD2 *	19	20	BD3 *
BD0 *	17	18	BD1 *
BA2	15	16	BA3
BA0	13	14	BA1
IPCB	11	12	Expansion Reset *
Audio Gnd	9	10	Audio Gnd
Audio Gnd	7	8	Audio Gnd
A++	5	6	Audio Gnd
A++	3	4	A++
A++	1	2	A++

J801
PIN OUT DETAIL

Signal	Pin	Pin	Signal
Tx Strobe	26	25	Rx1 Strobe
SA0	24	23	SD3
SA1	22	21	SD2
SA2	20	19	SD1
Tx Loop	18	17	SD0
PA Power Cutback *	16	15	Rx1 Lock *
PA Key *	14	13	Rx1 Loop
PA On *	12	11	AGC Ref (800/896)
PA Full Power *	10	9	Rx2 Strobe
Tx Lock *	8	7	Antenna Relay Enable *
Raw Rx2 Audio	6	5	Raw Rx1 Audio
Audio Gnd (Gnd A)	4	3	Tx Mod Audio
Rx2 Lock *	2	1	+9.6V

J803
PIN OUT DETAIL

Signal	Pin	Pin	Signal
Audio Gnd	40	39	+5V
N.C.	38	37	Key Battery Gnd
N.C.	36	35	Coded Rx Level *
Secure Alert Tones	34	33	Expansion Reset *
Coded Mod Level *	32	31	Level Inc
Level U/D *	30	29	IPCB
In MRTI Audio	28	27	Quad Audio
N.C.	26	25	DS *
BA0	24	23	BA1 *
BA2	22	21	BA3 *
BD0 *	20	19	BD1 *
BD2 *	18	17	BD3 *
Logic Gnd	16	15	HSR Syn
Logic Gnd	14	13	HSR Clock
Logic Gnd	12	11	HSR to Secure
Logic Gnd	10	9	HSR In
Local Audio	8	7	Coded Mod Audio
Raw Tx Audio	6	5	Tx Audio
Secure Rx Audio	4	3	+9.6V
Audio Gnd	2	1	Audio Gnd

J804
PIN OUT DETAIL

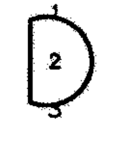
Signal	Pin	Pin	Signal
Audio Gnd	34	33	+5V
A++	32	31	+5V
Gen Tx Data	30	29	Mute
Expansion Reset *	28	27	Connect Tone Audio
IPCB	26	25	DS *
BA0	24	23	BA1
BA2	22	21	BA3
BD0 *	20	19	BD1 *
BD2 *	18	17	BD3 *
Logic Gnd	16	15	HSR Syn
Logic Gnd	14	13	HSR Clock
Logic Gnd	12	11	HSR from TTRC
Logic Gnd	10	9	HSR Out
Quad Audio	8	7	TKG Mod Audio
Raw Tx Audio	6	5	Tx Audio
Line Audio	4	3	9.6V
Audio Gnd	2	1	A++

J812
PIN OUT DETAIL

Signal	Pin	Pin	Signal
IPCB	6	5	Spkr Audio
MIC PTT *	4	3	MIC Audio
Audio Ground	2	1	Logic Ground

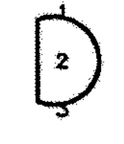
TRANSISTOR DETAILS (TOP VIEW)

4800869642
4800869328
4800869643
4811043C05
4811043C26
4811043C06



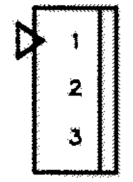
1 -EMITTER
2 -BASE
3 -COLLECTOR

4811043C37
4800869653



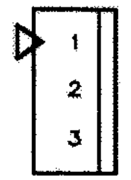
1 -DRAIN
2 -SOURCE
3 -GATE

4800869829

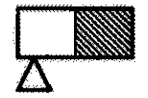


1 -EMITTER
2 -BASE
3 -COLLECTOR

4883875005

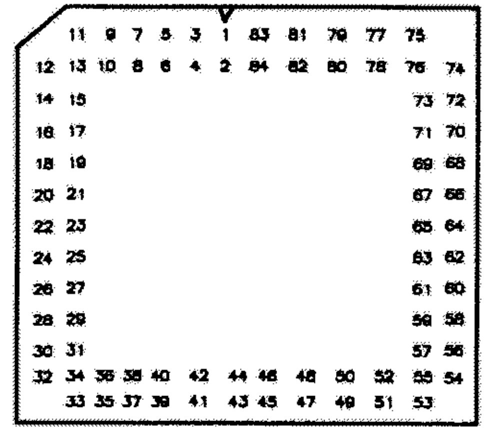


1 -CATHODE
2 -ANODE
3 -GATE

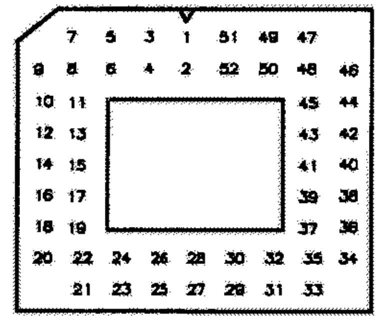


NOTE: SHADED AREA INDICATES DEFAULT JUMPER POSITION.

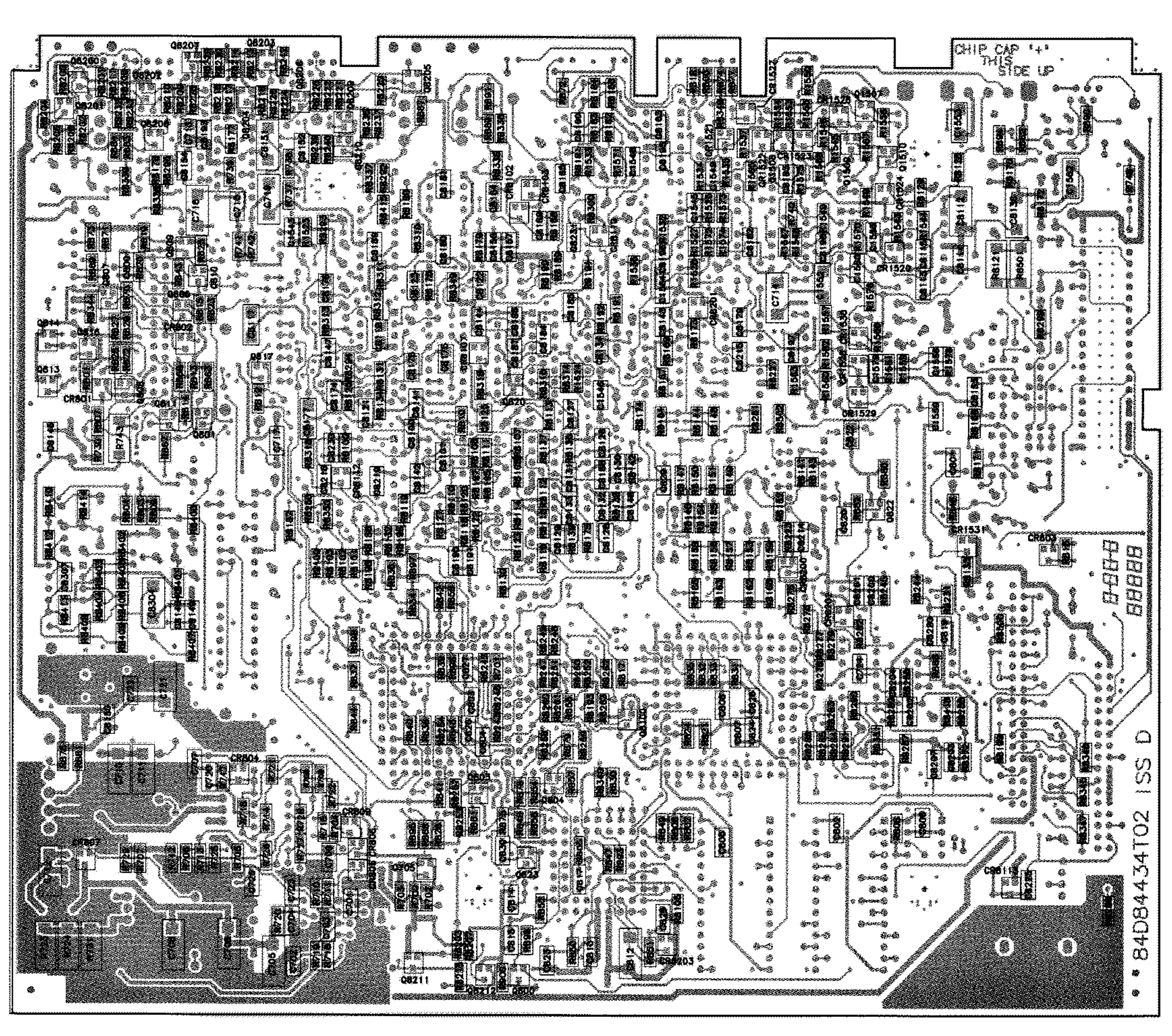
REQ'S BD-TEPS-48146



ASIC SOCKET DETAIL



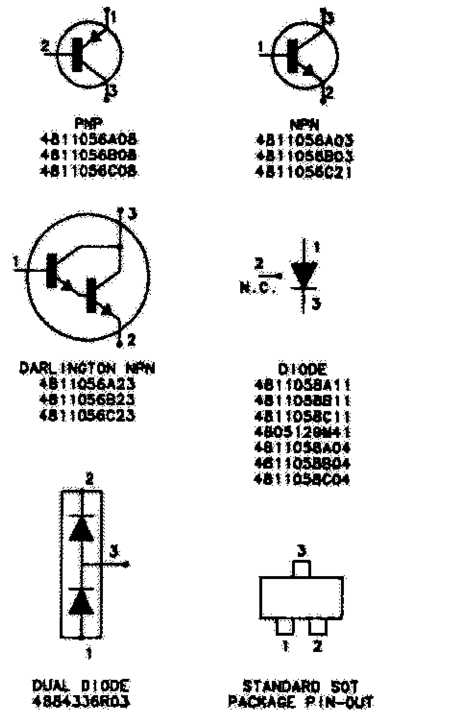
uP SOCKET DETAIL



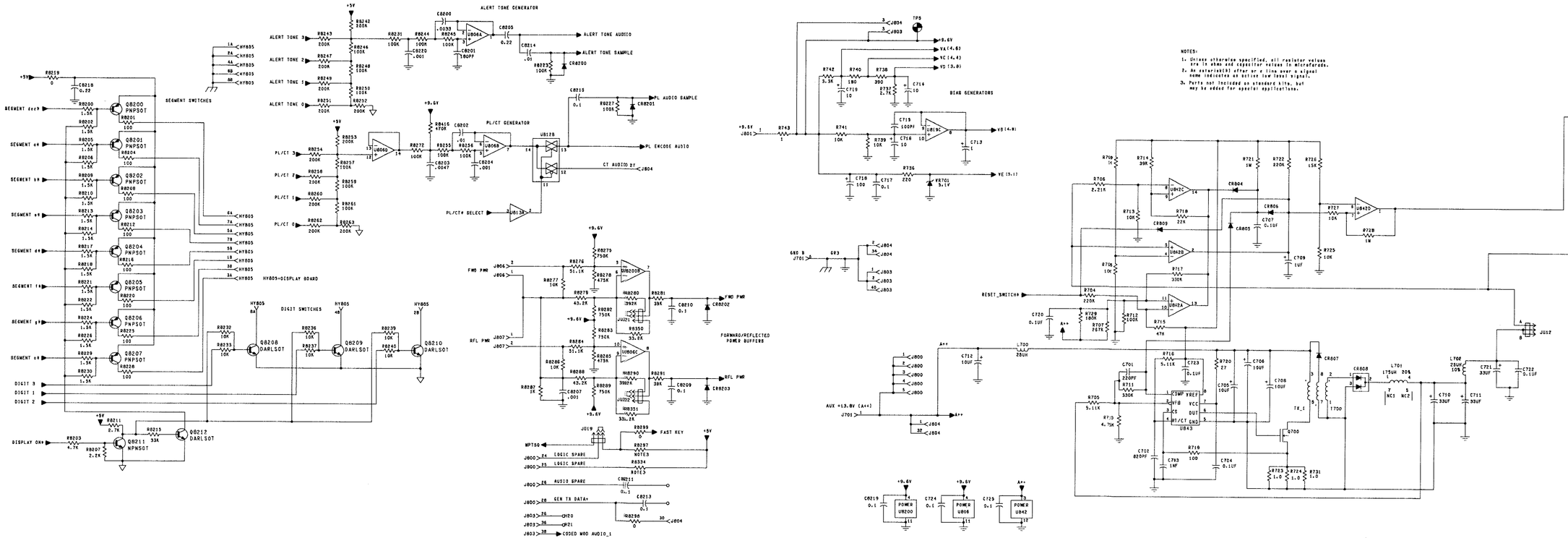
SHOWN FROM SOLDER SIDE

OL - TEPS - 48148-A

BD - TEPS - 48147-A

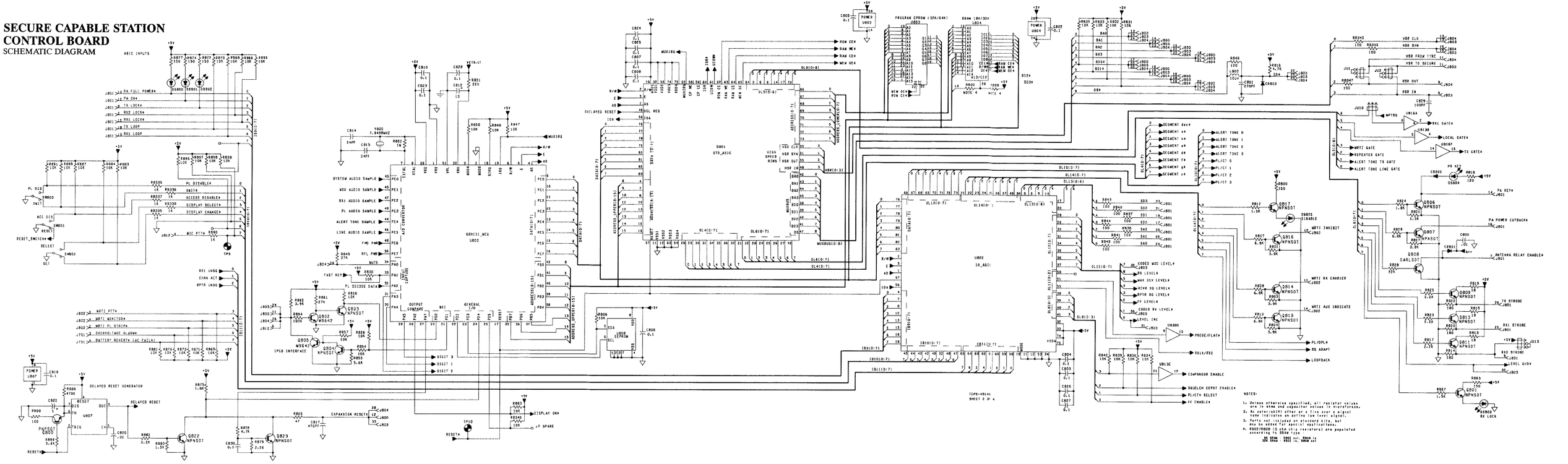


SECURE CAPABLE STATION CONTROL BOARD
SCHEMATIC DIAGRAM

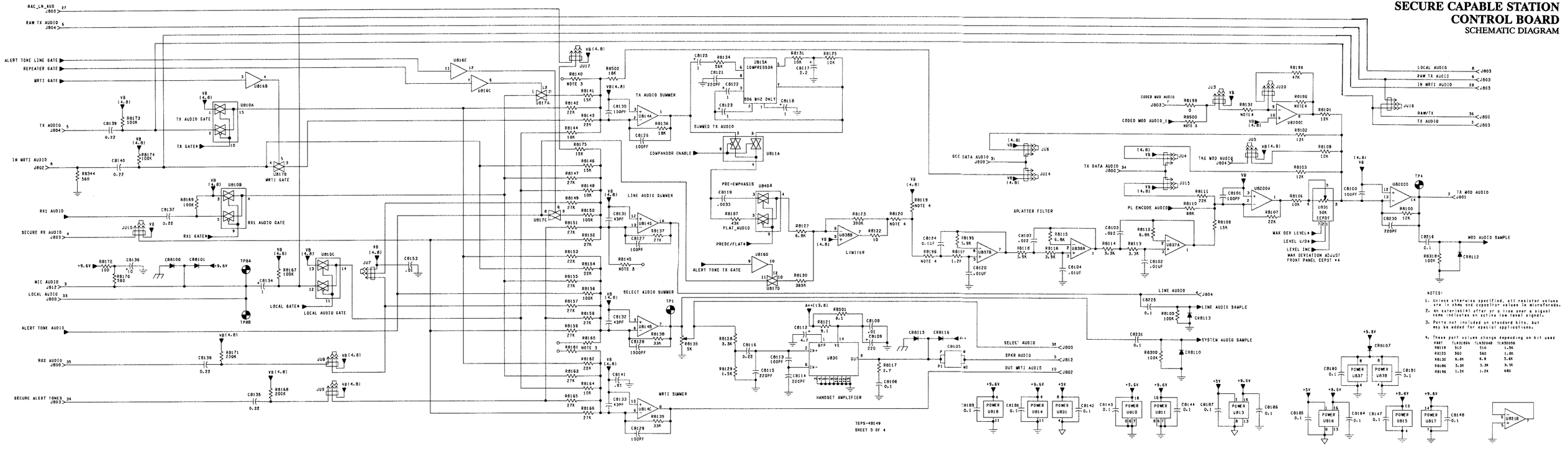


SECURE CAPABLE STATION CONTROL BOARD

SCHEMATIC DIAGRAM



SECURE CAPABLE STATION CONTROL BOARD
SCHEMATIC DIAGRAM

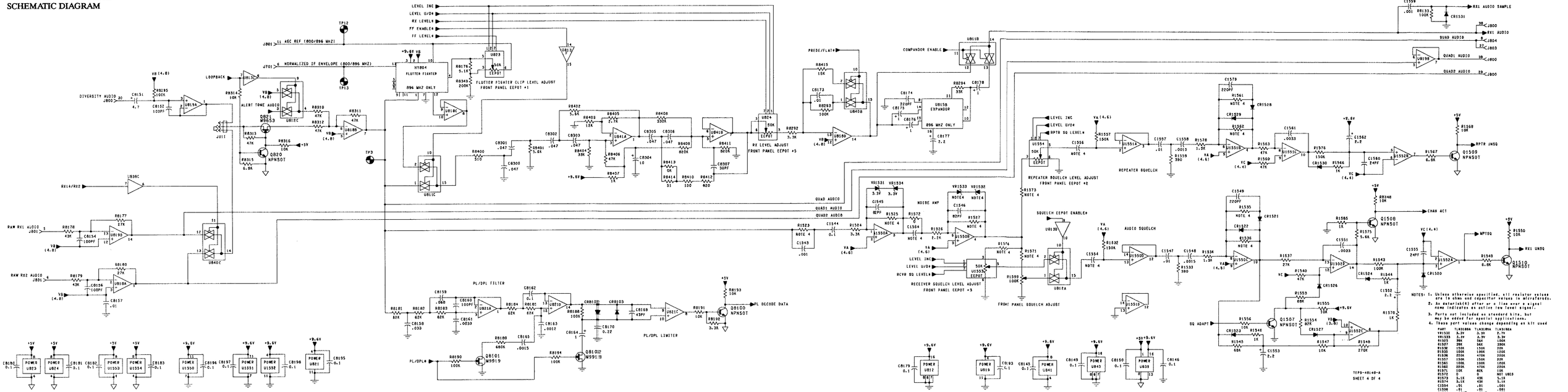


NOTES:

1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but may be added for special applications.
4. These part values change depending on kit used

PART	TLN3089A	TLN3204B	TLN3205B
R8118	510	510	1.5K
R8120	560	560	1.8K
R8132	6.8K	6.8	5.6K
R8186	3.3K	3.3K	3.3K
R8196	1.2K	1.2K	680

SECURE CAPABLE STATION
CONTROL BOARD
SCHEMATIC DIAGRAM



Parts Lists

TRN7352B Vhf/Uhf NB SSCB
TRN7423B 900 Analog Plus SSCB
TRN7604A 800 SSCB
TRN7358B Vhf SSCB

PL-11694-A

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		capacitor, fixed:
C701	2113740B57	220 pF, ±5%; 50V
C702	2113740B71	820 pF, ±5%; 50V
C703	2113740B73	1000 pF, ±5%; 50V
C704	2113741B69	0.1 uF, ±5%; 50V
C705, 706	2311049A19	10 uF, ±10%; 25V
C707	2113741B69	0.1 uF, ±5%; 50V
C708	2311049A19	10 uF, ±10%; 25V
C709	2311049A08	1 uF, ±10%; 35V
C710, 711	2311049A22	33 uF, ±10%; 16V
C712	2311049A19	10 uF, ±10%; 25V
C713	2311049A08	1 uF, ±10%; 35V
C714	2311049A19	10 uF, ±10%; 25V
C715	2113740B49	100 pF, ±5%; 50V
C716	2311049A19	10 uF, ±10%; 25V
C717	2113741B69	0.1 uF, ±5%; 50V
C718	2313748G21	100 uF, ±20%; 16V (TRN7352B, TRN7423B, TRN7604A)
C719	2311049A19	10 uF, ±10%; 25V
C720	2113741B69	0.1 uF, ±5%; 50V
C721	2311049A22	33 uF, ±10%; 16V
C722 thru 725	2113741B69	0.1 uF, ±5%; 50V
C800	2113741B45	0.01 uF, ±5%; 50V
C801	2113740B59	270 pF, ±5%; 50V
C802 thru 808	2113741B69	0.1 uF, ±5%; 50V
C810	2113741B69	0.1 uF, ±5%; 50V
C812	2311049A19	10 uF, ±10%; 25V
C814, 815	2113740B34	24 pF, ±5%; 50V
C817	2113740B65	470 pF, ±5%; 50V
C819	2113741B69	0.1 uF, ±5%; 50V
C820	2113741B45	0.01 uF, ±5%; 50V
C822	2311049A08	1 uF, ±10%; 35V
C823 thru 828	2113741B69	0.1 uF, ±5%; 50V
C829	2113740B49	100 pF, ±5%; 50V
C830	2113741B69	0.1 uF, ±5%; 50V
C1543	2113740B73	1000 pF, ±5%; 50V
C1544	0811051A13	0.1 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C1545, 1546	2113740B47	82 pF, ±5%; 50V
C1547	0811017A08	0.01 uF, ±5%; 50V (TRN7352B, TRN7423B, TRN7604A)
C1548	2113740B76	1500 pF, ±5 pF; 50V
C1549	2113740B57	220 pF, ±5%; 50V
C1551	0811017A05	3300 pF, ±5%; 50V (TRN7352B, TRN7423B, TRN7604A)
C1552, 1553	2311049A10	2.2 uF, ±10%; 35V
C1554	0811017A01	1000 pF, ±5%; 50V (TRN7352B, TRN7423B)
C1554	0811017A08	0.01 uF, ±5%; 50V (TRN7604A)
C1555	2113740B34	24 pF, ±5%; 50V
C1556	0811017A01	1000 pF, ±5%; 50V (TRN7352B, TRN7423B)
C1556	0811017A08	0.01 uF, ±5%; 50V (TRN7604A)
C1557	0811017A08	0.01 uF, ±5%; 50V (TRN7352B, TRN7423B, TRN7604A)

TRN7352B Vhf/Uhf NB SSCB
TRN7423B 900 Analog Plus SSCB
TRN7604A 800 SSCB
TRN7358B Vhf SSCB

PL-11694-A (cont.)

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		capacitor, fixed (cont.):
C1558	2113740B76	1500 pF, ±5 pF; 50V
C1559	2113740B73	1000 pF, ±5%; 50V
C1560	2113740B34	24 pF, ±5%; 50V
C1561	0811017A05	3300 pF, ±5%; 50V (TRN7352B, TRN7423B, TRN7604A)
C1562	2311049A10	2.2 uF, ±10%; 35V
C1564	2113741B21	1000 pF, ±5%; 50V (TRN7352B)
C1564	2113741B37	4700 pF, ±5%; 50V (TRN7604A, TRN7358B)
C1579	2113740B57	220 pF, ±5%; 50V
C8100, 8101	2113740B49	100 pF, ±5%; 50V
C8102	0811017A08	0.01 uF, ±5%; 50V (TRN7352B, TRN7423B, TRN7604A)
C8103	0811051A09	0.022 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8104	0811017A08	0.01 uF, ±5%; 50V (TRN7352B, TRN7423B, TRN7604A)
C8105	2383210A19	500 uF, +100%/-10%; 20V
C8106	0811051A13	0.1 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8107	0811051A09	0.022 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8108	0811017A08	0.01 uF, ±5%; 50V (TRN7352B, TRN7423B, TRN7604A)
C8109	2384665F06	220 uF, +150%/-10%; 25V
C8111	0811017A05	3300 pF, ±5%; 50V (TRN7352B)
C8112	2311049A15	4.7 uF, ±10%; 35V
C8113	2113740B49	100 pF, ±5%; 50V
C8114, 8115	2113740B57	220 pF, ±5%; 50V
C8116	0811051A15	0.22 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8117	2311049A10	2.2 uF, ±10%; 35V
C8118	2311049A08	1 uF, ±10%; 35V
C8119	0811017A05	3300 pF, ±5%; 50V (TRN7352B, TRN7423B, TRN7604A)
C8120	0811017A08	0.01 uF, ±5%; 50V (TRN7352B, TRN7423B, TRN7604A)
C8121	2113740B57	220 pF, ±5%; 50V
C8122, 8123	2311049A08	1 uF, ±10%; 35V
C8124	0811051A13	0.1 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8125	2311049A08	1 uF, ±10%; 35V
C8126 8127	2113740B49	100 pF, ±5%; 50V
C8128	2113740B49	100 pF, ±5%; 50V (TRN7352B, TRN7423B, TRN7604A)
C8128	2113740B76	1500 pF, ±5%; 50V (TRN7604A)
C8129 8130	2113740B49	100 pF, ±5%; 50V
C8131 thru 8133	2113740B40	43 pF, ±5%; 50V
C8134	2311049A08	1 uF, ±10%; 35V
C8135	0811051A15	0.22 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8136	2311049A19	10 uF, ±10%; 25V
C8137 thru 8140	0811051A15	0.22 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8141	2113741B45	0.01 uF, ±5%; 50V

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		capacitor, fixed (cont.):
C8142 thru 8150	2113741B69	0.1 uF, ±5%; 50V
C8151	2311049A15	4.7 uF, ±10%; 35V
C8152	2113740B49	100 pF, ±5%; 50V
C8153	2113741B45	0.01 uF, ±5%; 50V
C8154	2113740B49	100 pF, ±5%; 50V
C8156	2113740B49	100 pF, ±5%; 50V
C8157	2113741B45	0.01 uF, ±5%; 50V
C8158	0811051A10	0.033 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8159	0811051A12	0.068 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8160	2113740B49	100 pF, ±5%; 50V
C8161	0811017A05	3300 pF, ±5%; 50V (TRN7352B, TRN7423B, TRN7604A)
C8162	0811051A13	0.1 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8163	2113740B74	1200 pF, ±5%; 50V
C8164	2311049A08	1 uF, ±10%; 35V
C8165	2113740B76	1500 pF, ±5 pF; 50V
C8169	2113740B40	43 pF, ±5%; 50V
C8170	0811051A15	0.22 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8173	0811017A08	0.01 uF, ±5%; 50V (TRN7352B, TRN7423B, TRN7604A)
C8174	2113740B57	220 pF, ±5%; 50V
C8175, 8176	2311049A08	1 uF, ±10%; 35V
C8177	2311049A10	2.2 uF, ±10%; 35V
C8178	2311049A08	1 uF, ±10%; 35V
C8179 thru 8191	2113741B69	0.1 uF, ±5%; 50V
C8193	2113741B69	0.1 uF, ±5%; 50V
C8195 thru 8198	2113741B69	0.1 uF, ±5%; 50V
C8200	2113741B33	3300 pF, ±5%; 50V
C8201	2113740B55	180 pF, ±5%; 50V
C8202	2113741B45	0.01 uF, ±5%; 50V
C8203	2113741B37	4700 pF, ±5%; 50V
C8204	2113740B73	1000 pF, ±5%; 50V
C8205	0811051A15	0.22 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8207	2113740B73	1000 pF, ±5%; 50V
C8209, 8210	0811051A13	0.1 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8214 thru 8216	2113740B73	1000 pF, ±5%; 50V
C8218	0811051A15	0.22 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8219	2113741B69	0.1 uF, ±5%; 50V
C8220	2113740B73	1000 pF, ±5%; 50V
C8225	2113740B73	1000 pF, ±5%; 50V
C8230	2113740B57	220 pF, ±5%; 50V
C8231	2113740B73	1000 pF, ±5%; 50V
C8300 thru 8303	0811051A11	0.047 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)
C8304	2311049A19	10 uF, ±10%; 25V
C8305, 8306	0811051A11	0.047 uF, ±5%; 63V (TRN7352B, TRN7423B, TRN7604A)

TRN7352B Vhf/Uhf NB SSCB
TRN7423B 900 Analog Plus SSCB
TRN7604A 800 SSCB
TRN7358B Vhf SSCB
PL-11694-A (cont.)

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		capacitor, fixed (cont.):
C8307	2113740B36	30 pF, ±5%; 50V
		diode: (see note)
CR801, 802	4811058A11	silicon
CR803	4805129M41	silicon, type MMBD501 (RH)
CR804 thru 807	4811058A11	silicon
CR808	4884349P01	silicon
CR809	4811058A11	silicon
CR1520 thru 1522	4805129M41	silicon, type MMBD501 (RH)
CR1523,1524	4811058A11	silicon
CR1526,1527	4811058A11	silicon
CR1528,1529	4805129M41	silicon, type MMBD501 (RH)
CR1530	4811058A11	silicon
CR1531	4805129M41	silicon, type MMBD501 (RH)
CR8100,8101	4883654H01	silicon
CR8102,8103	4811058A11	silicon
CR8107	4811058A11	silicon
CR8110	4805129M41	silicon, type MMBD501 (RH)
CR8112,8113	4805129M41	silicon, type MMBD501 (RH)
CR8115,8116	4883654H01	silicon
CR8200 thru 8203	4805129M41	silicon, type MMBD501 (RH)
		light emitting diode: (see note)
DS800 thru 803	4888245C22	green
DS804	4888245C23	yellow
DS805	4888245C24	red
DS8200 thru 8202	482771L03	red (TRN7604A)
		connector:
J701	2882984N13	plug: 6-contact
J800	2882296R34	plug: 40-contact
J801	2882505T03	plug: 26-contact
J802	2884324M16	plug: 14-contact
J803	2882505T05	plug: 40-contact (TRN7352B, TRN7423B, TRN7604A)
J804	2882505T04	plug: 34-contact
J806,807	0984231B03	receptacle: phono jack
J812	0983112N01	receptacle: 6-contact
		jumper:
JU1 thru 20	2880002R03	plug: 3-contact
JU21	2880002R03	plug: 3-contact (TRN7352B, TRN7423B, TRN7604A)
JU22	2880002R03	plug: 3-contact
JU21	0984181L01	SHORTING JUMPER: 2-contact (TRN7423B)
		coil:
L700	2484386T01	25 UH
L701	2484266T01	150 UH
L702	2484386T01	25 UH
L800	2411047A25	10 UH (TRN7352B, TRN7423B, TRN7604A)

TRN7352B Vhf/Uhf NB SSCB
TRN7423B 900 Analog Plus SSCB
TRN7604A 800 SSCB
TRN7358B Vhf SSCB

PL-11694-A (cont.)

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		transistor: (see note)
Q700	4884233T01	type MOSFET
Q705	4811056A08	PNP
Q800	4811056A08	PNP
Q801	4811056A03	NPN
Q802	4800869642	NPN (TRN7352B, TRN7423B, TRN7604A)
Q803, 804	4811056A03	NPN
Q805	4800869642	NPN (TRN7352B, TRN7423B, TRN7604A)
Q806, 807	4811056A03	NPN
Q808	4811056A23	NPN
Q809 thru 811	4813824A10	NPN
Q813, 814	4811056A03	NPN
Q816, 817	4811056A03	NPN
Q820	4811056A03	NPN
Q821	4800869653	type JFET (TRN7352B, TRN7423B, TRN7604A)
Q822, 823	4811056A03	NPN
Q1507 thru 1510	4811056A03	NPN
Q8100	4811056A03	NPN
Q8101, 8102	4800869919	type P-C JFET
Q8200 thru 8207	4811056A08	PNP
Q8208 thru 8210	4811056A23	NPN
Q8211	4811056A03	NPN
Q8212	4811056A23	NPN
		resistor, fixed:
		unless otherwise stated
R700	0611077A98	10K, ±5%; 1/8W
R701	0611077A88	3.9K, ±5%; 1/8W
R702	0611077A50	100 ohms, ±5%; 1/8W
R703	0611077A74	1K, ±5%; 1/8W
R704	0611077B31	220K, ±5%; 1/8W
R705	0611077F63	5.11K, ±1%; 1/8W
R706	0611077F28	2.21K, ±1%; 1/8W
R707	0611077H30	267K, ±1%; 1/8W
R708	0611077F91	10K, ±1%; 1/8W
R709	0611077E94	1K, ±1%; 1/8W
R710	0611077F60	4.75K, ±1%; 1/8W
R711	0611077B35	330K, ±5%; 1/8W
R712	0611077B23	100K, ±5%; 1/8W
R713	0611077F91	10K, ±1%; 1/8W
R714	0611077B13	39K, ±5%; 1/8W
R715	0611077B15	47K, ±5%; 1/8W
R716	0611077F63	5.11K, ±1%; 1/8W
R717	0611077B35	330K, ±5%; 1/8W
R718	0611077B07	22K, ±5%; 1/8W
R719	0611077A50	100 ohms, ±5%; 1/8W
R720	0611077A36	27 ohms, ±5%; 1/8W
R721	0611077B47	1 meg, ±5%; 1/8W
R722	0611077B31	220K, ±5%; 1/8W
R723, 724	0683962T01	1 ohm, ±5%; 1W
R725	0611077F91	10K, ±1%; 1/8W
R726	0611077G09	15K, ±1%; 1/8W
R727	0611077A98	10K, ±5%; 1/8W

TRN7352B Vhf/Uhf NB SSCB
TRN7423B 900 Analog Plus SSCB
TRN7604A 800 SSCB
TRN7358B Vhf SSCB

PL-11694-A (cont.)

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		resistor, fixed: (cont.)
		unless otherwise stated
R728	0611077H85	1 meg, ±1%; 1/8W
R729	0611077B29	180K, ±5%; 1/8W
R730	0611077A01	0 ohm, ±5%; 0W
R731	0683962T01	1 ohm, ±5%; 1W
R736	0611009A33	220 ohms, ±5%; 1/4W (TRN7352B, TRN7423B, TRN7604A)
R737	0611077A84	2.7K, ±5%; 1/8W
R738	0611077A64	390 ohms, ±5%; 1/8W
R739	0611077A98	10K, ±5%; 1/8W
R740	0611077A56	180 ohms, ±5%; 1/8W
R741	0611077A98	10K, ±5%; 1/8W
R742	0611077A86	3.3K, ±5%; 1/8W
R743	0611086A03	1 ohms, ±5%; 1W (TRN7352B, TRN7423B, TRN7604A)
R743	0683962T01	1 ohm, ±5%; 1W (TRN7604A)
R748	0611077A78	1.5K, ±5%; 1/8W
R800	0611077A54	150 ohms, ±5%; 1/8W
R801	0611077A88	3.9K, ±5%; 1/8W
R802	0611077A01	0 ohm, ±5%; 0W
R803, 804	0611077A88	3.9K, ±5%; 1/8W
R805	0611077A42	47 ohms, ±5%; 1/8W
R806	0611077A98	10K, ±5%; 1/8W
R807	0611077A94	6.8K, ±5%; 1/8W
R809, 810	0611077A94	6.8K, ±5%; 1/8W
R812	0611077A78	1.5K, ±5%; 1/8W
R813	0611077A32	18 ohms, ±5%; 1/8W
R814	0611077A56	180 ohms, ±5%; 1/8W
R815	0611077A32	18 ohms, ±5%; 1/8W
R816	0611077A90	4.7K, ±5%; 1/8W
R817	0611077A82	2.2K, ±5%; 1/8W
R818	0611077A52	120 ohms, ±5%; 1/8W
R819	0611077A32	18 ohms, ±5%; 1/8W
R820	0611077A56	180 ohms, ±5%; 1/8W
R821	0611077A78	1.5K, ±5%; 1/8W
R822	0611077A56	180 ohms, ±5%; 1/8W
R823	0611077A82	2.2K, ±5%; 1/8W
R824	0611077A80	1.8K, ±5%; 1/8W
R825	0611077A82	2.2K, ±5%; 1/8W
R826	0611077A98	10K, ±5%; 1/8W
R827	0611077A88	3.9K, ±5%; 1/8W
R828	0611077B07	22K, ±5%; 1/8W
R829	0611077A94	6.8K, ±5%; 1/8W
R830 thru 836	0611077A98	10K, ±5%; 1/8W
R837, 838	0611077A50	100 ohms, ±5%; 1/8W
R839	0611077A98	10K, ±5%; 1/8W
R840, 841	0611077A50	100 ohms, ±5%; 1/8W
R842	0611077A98	10K, ±5%; 1/8W
R843 thru 845	0611077A50	100 ohms, ±5%; 1/8W
R846	0611077A52	120 ohms, ±5%; 1/8W
R847, 848	0611077A98	10K, ±5%; 1/8W
R849	0611077B09	27K, ±5%; 1/8W
R850	0611077A98	10K, ±5%; 1/8W
R851	0611077A58	220 ohms, ±5%; 1/8W
R852	0611077B47	1 meg, ±5%; 1/8W
R854	0611077A98	10K, ±5%; 1/8W

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		resistor, fixed: (cont.)
R855	0611077A92	5.6K, ±5%; 1/8W
R856 thru 858	0611077A98	10K, ±5%; 1/8W
		unless otherwise stated
R861	0611077B09	27K, ±5%; 1/8W
R862	0611077A88	3.9K, ±5%; 1/8W
R863	0611077A54	150 ohms, ±5%; 1/8W
R866	0611077A98	10K, ±5%; 1/8W
R867	0611077A78	1.5K, ±5%; 1/8W
R868 thru 871	0611077A98	10K, ±5%; 1/8W
R872	0611077A54	150 ohms, ±5%; 1/8W
R873	0611077A98	10K, ±5%; 1/8W
R874	0611077A54	150 ohms, ±5%; 1/8W
R875	0611077A80	1.8K, ±5%; 1/8W
R876	0611077A98	10K, ±5%; 1/8W
R877	0611077A54	150 ohms, ±5%; 1/8W
R878	0611077A90	4.7K, ±5%; 1/8W
R879	0611077A82	2.2K, ±5%; 1/8W
R880	0611077A78	1.5K, ±5%; 1/8W
R881	0611077A98	10K, ±5%; 1/8W
R882	0611077A82	2.2K, ±5%; 1/8W
R883, 884	0611077A98	10K, ±5%; 1/8W
R887	0611077A98	10K, ±5%; 1/8W
R888	0611077B39	470K, ±5%; 1/8W
R889	0611077A98	10K, ±5%; 1/8W
R890	0611077A74	1K, ±5%; 1/8W
R891	0611077A98	10K, ±5%; 1/8W
R893	0611077A98	10K, ±5%; 1/8W
R894	0611077B23	100K, ±5%; 1/8W
R895 thru 898	0611077A98	10K, ±5%; 1/8W
R899	0611077A92	5.6K, ±5%; 1/8W (TRN7352B, TRN7423B, TRN7604A)
R900	0611077A50	100 ohms, ±5%; 1/8W
R1523	0611077B15	47K, ±5%; 1/8W (TRN7352B, TRN7423B, TRN7358B)
R1523	0611077B17	56K, ±5%; 1/8W (TRN7604A)
R1524	0611077A86	3.3K, ±5%; 1/8W
R1525	0611077B23	100K, ±5%; 1/8W (TRN7352A)
R1525	0611077B13	39K, ±5%; 1/8W (TRN7423B)
R1525	0611077B11	33K, ±5%; 1/8W (TRN7604A)
R1525	0611077B17	33K, ±5%; 1/8W (TRN7358B)
R1526	0611077A82	2.2K, ±5%; 1/8W
R1527	0611077B35	330K, ±5%; 1/8W (TRN7352B)
R1527	0611077B13	39K, ±5%; 1/8W (TRN7423B)
R1527	0611077B11	33K, ±5%; 1/8W (TRN7604A)
R1527	0611077B17	56K, ±5%; 1/8W (TRN7358B)
R1532	0611077B07	22K, ±5%; 1/8W (TRN7352B)
R1532	0611077B27	150K, ±5%; 1/8W (TRN7358B, TRN7423B, TRN7604A)
R1533	0611077A64	390 ohms, ±5%; 1/8W
R1534	0611077A78	1.5K, ±5%; 1/8W
R1535	0611077B25	120K, ±5%; 1/8W (TRN7352B)
R1535	0611077B15	47K, ±5%; 1/8W (TRN7604A)
R1535	0611077B23	100K, ±5%; 1/8W (TRN7358B)
R1536	0611077B31	220K, ±5%; 1/8W (TRN7352B, TRN7423B, TRN7604A)
R1536	0611077B39	470K, ±5%; 1/8W (TRN7358B)
R1537	0611077B15	47K, ±5%; 1/8W

TRN7352B Vhf/Uhf NB SSCB
TRN7423B 900 Analog Plus SSCB
TRN7604A 800 SSCB
TRN7358B Vhf SSCB
PL-11694-A (cont.)

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		resistor, fixed: (cont.)
		unless otherwise stated
R1540	0611077B15	47K, ±5%; 1/8W
R1543	0611077B23	100K, ±5%; 1/8W
R1544	0611077A74	1K, ±5%; 1/8W
R1545	0611077B19	68K, ±5%; 1/8W
R1546	0611077A74	1K, ±5%; 1/8W
R1547	0611077A98	10K, ±5%; 1/8W
R1548	0611077B33	270K, ±5%; 1/8W
R1549	0611077A94	6.8K, ±5%; 1/8W
R1550	0611077A98	10K, ±5%; 1/8W
R1553	0611077B19	68K, ±5%; 1/8W
R1554	0611077B21	82K, ±5%; 1/8W
R1555, 1556	0611077A98	10K, ±5%; 1/8W
R1557	0611077B07	22K, ±5%; 1/8W (TRN7352B, TRN7423B)
R1557	0611077B27	150K, ±5%; 1/8W (TRN7604A,TRN7358B)
R1559	0611077A64	390 ohms, ±5%; 1/8W
R1560	0611077B15	47K, ±5%; 1/8W (TRN7352B, TRN7604A)
R1561	0611077B25	120K, ±5%; 1/8W (TRN7352B, TRN7423B)
R1561	0611077B15	47K, ±5%; 1/8W (TRN7604A)
R1561	0611077B23	100K, ±5%; 1/8W (TRN7358B)
R1562	0611077B31	220K, ±5%; 1/8W (TRN7352B, TRN7423B, TRN7604A)
R1562	0611077B39	470K, ±5%; 1/8W (TRN7358B)
R1563	0611077B15	47K, ±5%; 1/8W
R1565, 1566	0611077A74	1K, ±5%; 1/8W
R1567	0611077A94	6.8K, ±5%; 1/8W
R1568	0611077A98	10K, ±5%; 1/8W
R1570	0611077A74	1K, ±5%; 1/8W
R1571	0611077A98	10K, ±5%; 1/8W (TRN7352B, TRN7423B, TRN7604A)
R1571	0611077B21	82K, ±5%; 1/8W (TRN7358B)
R1572	0611077A01	0 ohm, ±5%; 0W (TRN7423B, TRN7358B, TRN7604A)
R1573	0611077A91	5.1K, ±5%; 1/8W (TRN7352B, TRN7423B, TRN7604A)
R1573	0611077B14	43K, ±5%; 1/8W (TRN7358B)
R1574	0611077A91	5.1K, ±5%; 1/8W (TRN7352B, TRN7423B, TRN7604A)
R1574	0611077B14	43K, ±5%; 1/8W (TRN7358B)
R1575	0611077A92	5.6K, ±5%; 1/8W
R1576	0611077B27	150K, ±5%; 1/8W
R1578	0611077A78	1.5K, ±5%; 1/8W
R1599	1882787K08	variable: 100K ±20%; 1/4W
R8100 thru 8103	0611077B01	12K, ±5%; 1/8W
R8105	0611077B23	100K, ±5%; 1/8W
R8106	0611077A98	10K, ±5%; 1/8W
R8107	0611077B07	22K, ±5%; 1/8W
R8108	0611077B03	15K, ±5%; 1/8W
R8109	0611077B01	12K, ±5%; 1/8W
R8110	0611077B19	68K, ±5%; 1/8W
R8111	0611077B07	22K, ±5%; 1/8W
R8112	0611077A94	6.8K, ±5%; 1/8W

TRN7352B Vhf/Uhf NB SSCB
TRN7423B 900 Analog Plus SSCB
TRN7604A 800 SSCB
TRN7358B Vhf SSCB

PL-11694-A (cont.)

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		resistor, fixed: (cont.)
		unless otherwise stated
R8113, 8114	0611077A86	3.3K, ±5%; 1/8W
R8115	0611077A94	6.8K, ±5%; 1/8W
R8116	0611077A88	3.9K, ±5%; 1/8W
R8117	0611009B26	2.7 ohms, ±5%; 1/4W (TRN7352B, TRN7423B, TRN7604A)
R8118	0611077A88	3.9K, ±5%; 1/8W
R8119	0611077A67	510 ohms, ±5%; 1/8W (TRN7352B, TRN7358B, TRN7604A)
R8119	0611077A78	1.5K, ±5%; 1/8W (TRN7423B)
R8120	0611077A68	560 ohms, ±5%; 1/8W (TRN7352B, TRN7358B, TRN7604A)
R8120	0611077A80	1.8K, ±5%; 1/8W (TRN7423B)
R8121	0611086A08	4.7 ohms, ±5%; 1W (TRN7352B, TRN7423B, TRN7358B)
R8121	0683962T24	9.1K, ±5%; 1W (TRN7604A)
R8122	0611077A26	10 ohms, ±5%; 1/8W
R8123	0611077B37	390K, ±5%; 1/8W
R8124	0611077A94	6.8K, ±5%; 1/8W (Deleted)
R8125	0611077A98	10K, ±5%; 1/8W
R8127	0611077A94	6.8K, ±5%; 1/8W
R8128	0611077A86	3.3K, ±5%; 1/8W
R8129	0611077A78	1.5K, ±5%; 1/8W
R8130	0611077H43	365K, ±1%; 1/8W
R8131	0611077A98	10K, ±5%; 1/8W
R8132	0611077A92	5.6K, ±5%; 1/8W (TRN7352B, TRN7423B)
R8132	0611077A94	6.8K, ±5%; 1/8W (TRN7604A,TRN7358B)
R8133	0611077B23	100K, ±5%; 1/8W
R8134	0611077B17	56K, ±5%; 1/8W
R8135	1882787K09	variable: 5K ±10%; 1/4W
R8136	0611077B05	18K, ±5%; 1/8W
R8137	0611077B09	27K, ±5%; 1/8W
R8138, 8139	0611077B11	33K, ±5%; 1/8W
R8141	0611077B03	15K, ±5%; 1/8W
R8142, 8143	0611077B07	22K, ±5%; 1/8W
R8144	0611077A98	10K, ±5%; 1/8W
R8146	0611077B03	15K, ±5%; 1/8W
R8147	0611077B09	27K, ±5%; 1/8W
R8148	0611077A98	10K, ±5%; 1/8W
R8149	0611077B09	27K, ±5%; 1/8W
R8150	0611077B23	100K, ±5%; 1/8W
R8151, 8152	0611077B09	27K, ±5%; 1/8W
R8153, 8154	0611077B07	22K, ±5%; 1/8W
R8155	0611077B09	27K, ±5%; 1/8W
R8156	0611077B23	100K, ±5%; 1/8W
R8157 thru 8159	0611077B09	27K, ±5%; 1/8W
R8162	0611077B07	22K, ±5%; 1/8W
R8163	0611077B09	27K, ±5%; 1/8W
R8164	0611077A98	10K, ±5%; 1/8W
R8165, 8166	0611077B09	27K, ±5%; 1/8W
R8167	0611077B23	100K, ±5%; 1/8W
R8168	0611077B30	200K, ±5%; 1/8W
R8169	0611077B23	100K, ±5%; 1/8W

TRN7352B Vhf/Uhf NB SSCB
TRN7423B 900 Analog Plus SSCB
TRN7604A 800 SSCB
TRN7358B Vhf SSCB

PL-11694-A (cont.)

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		resistor, fixed: (cont.)
		unless otherwise stated
R8170	0611077A68	560 ohms, ±5%; 1/8W
R8171	0611077B30	200K, ±5%; 1/8W
R8172	0611077A50	100 ohms, ±5%; 1/8W
R8173, 8174	0611077B23	100K, ±5%; 1/8W
R8175	0611077B03	15K, ±5%; 1/8W
R8176	0611077A91	5.1K, ±5%; 1/8W
R8177	0611077B09	27K, ±5%; 1/8W
R8178, 8179	0611077B14	43K, ±5%; 1/8W
R8180	0611077B09	27K, ±5%; 1/8W
R8181 thru 8185	0611077B18	62K, ±5%; 1/8W
R8186	0611077B15	47K, ±5%; 1/8W (TRN7352B, TRN7423B)
R8186	0611077B05	18K, ±5%; 1/8W (TRN7604A, TRN7358B)
R8187	0611077B14	43K, ±5%; 1/8W
R8188	0611077B23	100K, ±5%; 1/8W
R8189	0611077B43	680K, ±5%; 1/8W
R8190	0611077B23	100K, ±5%; 1/8W
R8191	0611077A98	10K, ±5%; 1/8W
R8192	0611077A86	3.3K, ±5%; 1/8W
R8193	0611077A98	10K, ±5%; 1/8W
R8194	0611077B23	100K, ±5%; 1/8W
R8195	0611077A88	3.9K, ±5%; 1/8W
R8196	0611077A76	1.2K, ±5%; 1/8W (TRN7352B, TRN7604A, TRN7358B)
R8196	0611077A70	680 ohms, ±5%; 1/8W (TRN7423B)
R8197	0611077A76	1.2K, ±5%; 1/8W
R8198	0611077B15	47K, ±5%; 1/8W (TRN7604A)
R8199	0611077A01	0 ohm, ±5%; 0W (TRN7604A)
R8200	0611077A78	1.5K, ±5%; 1/8W
R8201	0611077A50	100 ohms, ±5%; 1/8W
R8202	0611077A78	1.5K, ±5%; 1/8W
R8203	0611077A90	4.7K, ±5%; 1/8W
R8204	0611077A50	100 ohms, ±5%; 1/8W
R8205, 8206	0611077A78	1.5K, ±5%; 1/8W
R8207	0611077A82	2.2K, ±5%; 1/8W
R8208	0611077A50	100 ohms, ±5%; 1/8W
R8209, 8210	0611077A78	1.5K, ±5%; 1/8W
R8211	0611077A84	2.7K, ±5%; 1/8W
R8212	0611077A50	100 ohms, ±5%; 1/8W
R8213, 8214	0611077A78	1.5K, ±5%; 1/8W
R8215	0611077B11	33K, ±5%; 1/8W
R8216	0611077A50	100 ohms, ±5%; 1/8W
R8217, 8218	0611077A78	1.5K, ±5%; 1/8W
R8219	0611009B23	0 ohm, ±5%; 1/4W (TRN7352B, TRN7423B, TRN7604A)
R8220	0611077A50	100 ohms, ±5%; 1/8W
R8221, 8222	0611077A78	1.5K, ±5%; 1/8W
R8223	0611077B23	100K, ±5%; 1/8W
R8224	0611077A78	1.5K, ±5%; 1/8W
R8225	0611077A50	100 ohms, ±5%; 1/8W
R8226	0611077A78	1.5K, ±5%; 1/8W
R8227	0611077B23	100K, ±5%; 1/8W
R8228	0611077A50	100 ohms, ±5%; 1/8W

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		resistor, fixed: (cont.)
		unless otherwise stated
R8229, 8230	0611077A78	1.5K, ±5%; 1/8W
R8231	0611077G88	100K, ±1%; 1/8W
R8232, 8233	0611077A98	10K, ±5%; 1/8W
R8236, 8237	0611077A98	10K, ±5%; 1/8W
R8239, 8240	0611077A98	10K, ±5%; 1/8W
R8242, 8243	0611077H18	200K, ±1%; 1/8W
R8244	0611077G88	100K, ±1%; 1/8W
R8245	0611077B23	100K, ±5%; 1/8W
R8246	0611077G88	100K, ±1%; 1/8W
R8247	0611077H18	200K, ±1%; 1/8W
R8248	0611077G88	100K, ±1%; 1/8W
R8249	0611077H18	200K, ±1%; 1/8W
R8250	0611077G88	100K, ±1%; 1/8W
R8251 thru 8254	0611077H18	200K, ±1%; 1/8W
R8255, 8256	0611077B23	100K, ±5%; 1/8W
R8257	0611077G88	100K, ±1%; 1/8W
R8258	0611077H18	200K, ±1%; 1/8W
R8259	0611077G88	100K, ±1%; 1/8W
R8260	0611077H18	200K, ±1%; 1/8W
R8261	0611077G88	100K, ±1%; 1/8W
R8262, 8263	0611077H18	200K, ±1%; 1/8W
R8272	0611077B25	120K, ±5%; 1/8W
R8275	0611077H46	392K, ±1%; 1/8W (TRN7352B, TRN7423B, TRN7358B)
R8275	0611077H73	740K, ±1%; 1/8W (TRN7604A)
R8276	0611077G60	51.1K, ±1%; 1/8W
R8277	0611077A98	10K, ±5%; 1/8W
R8278	0611077H54	475K, ±1%; 1/8W
R8279	0611077G53	43.2K, ±1%; 1/8W
R8280	0611077H46	392K, ±1%; 1/8W
R8281	0611077B13	39K, ±5%; 1/8W
R8282	0611077H46	392K, ±1%; 1/8W (TRN7352B, TRN7423B, TRN7358B)
R8282	0611077H73	750K, ±1%; 1/8W (TRN7604A)
R8283	0611077H46	392K, ±1%; 1/8W (TRN7358B, TRN7423B)
R8283	0611077H73	750K, ±1%; 1/8W (TRN7604A)
R8284	0611077G60	51.1K, ±1%; 1/8W
R8285	0611077H54	475K, ±1%; 1/8W
R8286	0611077A98	10K, ±5%; 1/8W
R8287	0611077A74	1K, ±5%; 1/8W
R8288	0611077G53	43.2K, ±1%; 1/8W
R8289	0611077H46	392K, ±1%; 1/8W (TRN7352B, TRN7423B, TRN7358B)
R8289	0611077H73	750K, ±1%; 1/8W (TRN7604A)
R8290	0611077H46	392K, ±1%; 1/8W
R8291	0611077B13	39K, ±5%; 1/8W
R8292	0611077A86	3.3K, ±5%; 1/8W
R8293	0611077B23	100K, ±5%; 1/8W
R8294	0611077B11	33K, ±5%; 1/8W
R8295	0611077B23	100K, ±5%; 1/8W
R8299	0611077A01	0 ohm, ±5%; 0W
R8300	0611077B23	100K, ±5%; 1/8W
R8310 thru 8313	0611077B15	47K, ±5%; 1/8W
R8314	0611077A98	10K, ±5%; 1/8W

TRN7352B Vhf/Uhf NB SSCB
TRN7423B 900 Analog Plus SSCB
TRN7604A 800 SSCB
TRN7358B Vhf SSCB
PL-11694-A (cont.)

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		resistor, fixed:
		unless otherwise stated
R8315	0611077A94	6.8K, ±5%; 1/8W
R8316	0611077A98	10K, ±5%; 1/8W
R8318	0611077B23	100K, ±5%; 1/8W
R8335 thru 8339	0611077A74	1K, ±5%; 1/8W
R8340	0611077A98	10K, ±5%; 1/8W
R8344	0611077A68	560 ohms, ±5%; 1/8W
R8345 thru 8347	0611077A50	100 ohms, ±5%; 1/8W
R8348	0611077A98	10K, ±5%; 1/8W
R8349	0611077B30	200K, ±5%; 1/8W
R8350, 8351	0611077G42	33.2K, ±1%; 1/8W
R8400	0611077A67	510 ohms, ±5%; 1/8W
R8401, 8402	0611077A92	5.6K, ±5%; 1/8W
R8403	0611077B01	12K, ±5%; 1/8W
R8404	0611077B11	33K, ±5%; 1/8W
R8405	0611077A84	2.7K, ±5%; 1/8W
R8406	0611077B15	47K, ±5%; 1/8W
R8407	0611077A74	1K, ±5%; 1/8W
R8408	0611077B35	330K, ±5%; 1/8W
R8409	0611077B45	820K, ±5%; 1/8W
R8410	0611077E15	150 ohms, ±1%; 1/8W
R8411	0611077B45	820K, ±5%; 1/8W
R8412	0611077E73	604 ohms, ±1%; 1/8W
R8413	0611009B23	0 ohm, ±5%; 1/4W
R8414	0611077A43	51 ohms, ±5%; 1/8W
R8415	0611077B03	15K, ±5%; 1/8W
R8416	0611077B39	470K, ±5%; 1/8W
R8500	0611077A01	0 ohm, ±5%; 0W (TRN7604A)
R8501	0683962T24	9.1 ohms, ±5%; 1W (TRN7604A)
R8502	0611077B05	18K, ±5%; 1/8W
		switch:
SW800, 801	4083980R12	toggle: sp3t (on-off-mom)
SW802	4083980R11	toggle: sp3t (mom-off-mom)
		transformer:
T700	2584265T01	power
		test point:
TP1	2962998D01	terminal pin
TP2 thru 7	2910271A15	terminal pin (TRN7604A)
TP8, 9	2910271A15	terminal pin
TP10, 11	2910271A15	terminal pin (TRN7604A)
TP12, 13	2910271A15	terminal pin (TRN7423B, TRN7604A)
		integrated circuit: (see note)
U800	5113802A01	A/D w/Switch Control Interface
U801, 802	5184494R03	ASIC Station Control
U804	5184064F76	Static 32Kx8 Bit RAM (TRN7352B, TRN7423B, TRN7604A)
U806	5183222M10	Quad Low Power Operational Amplifier (TRN7352B, TRN7423B, TRN7604A)
U807	5184320A35	Timer (TRN7352B, TRN7423B, TRN7604A)
U810 thru 812	5184887K60	2-Channel Analog Mux/Demux (TRN7352B, TRN7423B, TRN7604A)
U813	5184704M19	Shift Hex Level Log Level Control

TRN7352B Vhf/Uhf NB SSCB
TRN7423B 900 Analog Plus SSCB
TRN7604A 800 SSCB
TRN7358B Vhf SSCB

PL-11694-A (cont.)

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		integrated circuit(cont., see note):
U814	5113819D04	Quad Differential-Input Operational Amplifier (TRN7352B, TRN7423B, TRN7604A)
U815	5184621K86	Dual Gain Control (TRN7423B)
U816	5184704M19	Shift Hex Level Log Level Control (TRN7352B, TRN7423B, TRN7604A)
U817	5184887K73	Quad Bilateral Switch(TRN7352B, TRN7423B, TRN7604A)
U818, 819	5113819D04	Quad Differential-Input Operational Amplifier (TRN7352B, TRN7423B, TRN7604A)
U821	5113819D04	Quad Differential-Input Operational Amplifier (TRN7352B, TRN7423B, TRN7604A)
U823	5182802R24	Digitally Controlled 50K Potentiometer (TRN7423B)
U824	5182802R24	Digitally Controlled 50K Potentiometer (TRN7423B, TRN7352B, TRN7604A)
U830	5184621K33	Operational Amplifierr (TRN7423B, TRN7352B, TRN7604A)
U831	5182802R24	Digitally Controlled 50K Potentiometerr (TRN7423B, TRN7352B, TRN7604A)
U837, 838	5184621K85	Dual Operational Amplifierr (TRN7423B, TRN7352B, TRN7604A)
U839	5184704M19	Shift Hex Level Log Level Controlr (TRN7423B, TRN7352B, TRN7604A)
U840	5184887K60	2-Channel Analog Mux/Demux (TRN7423B, TRN7352B, TRN7604A)
U841	5184621K85	Dual Operational Amplifier (TRN7423B, TRN7352B, TRN7604A)
U842	5113820D02	Quad Single-Supply Comparator (TRN7423B, TRN7352B, TRN7604A)
U843	5184371T01	Single Current Mode Controller
U1550, 1551	5183222M03	Quad Operational Amplifier (TRN7352B, TRN7423B, TRN7604A)
U1552	5183222M10	Quad Operational Amplifier (TRN7352B, TRN7423B, TRN7604A)
U1553, 1554	5182802R24	Digitally Controlled 50K Potentiometer (TRN7352B, TRN7423B, TRN7604A)
U8200	5113819D04	Quad Differential-Input Operational Amplifier (TRN7352B, TRN7423B, TRN7604A)
		voltage regulator: (see note)
VR701	4883461E40	Zener 5.1V (TRN7352B, TRN7423B, TRN7604A)
VR702	4882256C26	Zener 3.3V (TRN7352B, TRN7423B, TRN7604A)
VR1531	4882256C26	Zener 3.3V (TRN7352B, TRN7423B, TRN7604A)
VR1532	4882256C33	Zener 2.7V (TRN7352B)
VR1532	4882256C26	Zener 3.3V (TRN7423B, TRN7604A)

TRN7352B Vhf/Uhf NB SSCB
TRN7423B 900 Analog Plus SSCB
TRN7604A 800 SSCB
TRN7358B Vhf SSCB

PL-11694-A (cont.)

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		voltage regulator: (cont.,see note)
VR1533	4882256C33	Zener 2.7V (TRN7352B)
VR1533	4882256C26	Zener 3.3V (TRN7423B, TRN7604A)
VR1534	4882256C26	Zener 3.3V (TRN7352B, TRN7423B, TRN7604A)
		crystal: (see note)
Y800	4880113K04	7.948 MHZ
		non-referenced items:
	TRN7606A	Display Board
	TRN9837A	Attenuator Flutter Hybrid (TRN7423B)
	0310945A11	SCREW, tapping: P3.12x1.27x8 (2 used with J800)
	0982449T01	SOCKET, IC: 52-contact (used with U800)
	0982449T03	SOCKET, IC: 84-contact (2 used with U801 & U802)
	0982808R02	SOCKET, IC: 8-contact (used with U808)
	0982808R10	SOCKET, IC: 28-contact (used with U803)
	0983729M17	CONNECTOR, receptacle: 20-contact (2 used with J800)
	0984181L01	SHORTING JUMPER: 2-contact (21 used with JU1 thru JU20 &22)
	0984181L01	SHORTING JUMPER: 2-contact (used with JU21) (TRN7352B, TRN7358B, TRN7604A)
	2683373P02	HEAT SINK, transistor (used with CR808)
	4380054K02	SPACER, support (4 used) (TRN7352B, TRN7423B, TRN7604A)
	5483865R01	LABEL, bar code: 1/4" wide, white (TRN7352B, TRN7423B, TRN7604A)
	5484960T01	LABEL, bar code: 6.3x12.7MM, white (TRN7352B, TRN7423B, TRN7604A)
	7505295B01	PAD, crystal (used with Y800)

NOTE: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part number.

TRN7008A Display Board

PL-11223-B

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		light emitting diode: (see note)
DS8200 thru 8202	4882771L03	red
		connector:
J805A	2883547T01	receptacle: 8-contact, right angle
J805B	2883547T01	receptacle: 8-contact, right angle
		non-referenced items:
	5483865R01	LABEL, bar code: 1/4" wide, white
	5484246T01	LABEL, bar code: 6.6x10.2MM

NOTE: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part number.

MOTOROLA INC.

TRUNKED TONE REMOTE CONTROL MODULE

Model TLN3112B
Model TLN3114B

1. FUNCTIONAL DESCRIPTION

1.1 GENERAL

This section describes the operation of the TLN3114B Trunked Tone Remote Control (TTRC) logic kernel board, and the TLN3112B TTRC audio board. These two boards can be operated as a pair only. It is housed alongside the Station Control Board (SSCB) in the control tray attached to the top of the rf tray. The TTRC is compatible only with the SSCB (TLN3189, TLN3204, and TLN3205) and the Secure Module (TLN3045). Note that Secure Module TLN3045 is not applicable for 900 MHz models.

1.2 TONE REMOTE CONTROL

The Tone Remote Control (TRC) section of the TTRC module allows control of a *MSF 5000* station from a remote location, using a non-dc continuous wireline. The input wireline can be Line 1 (4-wire system) or Line 2 (2-wire system), as determined by the position of P422 and P4205. Note that the board is set up for Line 2 as the standard input for TRC, with P422 in its normal position and P4205 in its normal position.

Table 1. TrunkedTone Remote Control (TTRC) Model Complements

Model	Description
TLN3112B	TTRC Audio Circuit Board
TFN6056A	Hybrid Notch Filter, Type 2175
TFN6061A	Hybrid Bandpass Filter (2175)
TRN7273A	TTRC Audio Board
TLN3114B	TTRC Audio Circuit Board
TVN6056A	TTRC Software
TRN7272A	TTRC Logic Board

Control is accomplished by the remote device sending a single tone or a sequence of control tones which are interpreted by the TTRC module. The TTRC module then initiates the station function via the MUXbus, Inter-Processor Communications Bus (IPCB), and High Speed Ring. The MUXbus, IPCB, and High Speed Ring are described in the Logic and Control data communications paragraph.

Figure 1 shows a typical tone remote control signaling format. HLGT is sent as a wake-up tone to the station. The level of this tone is approximately equal to the voice peak levels on the wireline. The HLGT is followed by a Function Tone (FT). FT contains the actual information for the station, as each different function tone corresponds to a different function performed by the station.

The FT level is 10 dB lower than that of the HLGT, and can be followed by a Low-Level Guard Tone (LLGT). The LLGT frequency is equal to that of the HLGT, but is at a 30 dB lower level. In a wireline push-to-talk function, audio to be transmitted is summed onto this signal, and the LLGT is notched out at the station to prevent it from being transmitted. The station remains keyed while the LLGT signal is present; when gone, the station dekeys. Other function tones can be assigned to initiate different functionality. Table 2 provides a list of TRC tones and their uses.

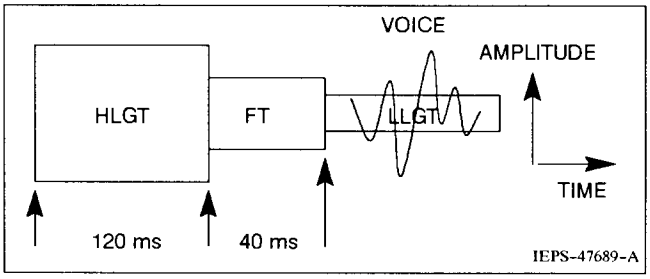


Figure 1. Remote Key-up

1.3 DC REMOTE CONTROL

The dc remote control section on the TTRC module is a software-enabled option that allows control of an *MSF 5000* station from a remote location using a dc continuous wireline pair. The input wireline can be Line 1 or Line 2 as determined by the position of P4226 and P4227. The board is set up for Line 2 as the standard input for dc remote control with P4226 and P4227 in their normal positions. This option may be used instead of the standard TRC remote control, with the TRC decoder being turned off and the dc current decoder turned on. The dc remote control is not compatible with trunking or with any secure-equipped station.

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Table 2. TRC Tone Frequencies and Uses

Function Tone Freq (Hz)	Tone #	Standard Use	Optional Use
2175	F0	MORE	KEY
2050	F1	MON	NULL
1950	F2	CHN 1; KEY	NULL
1850	F3	CHN 2; KEY	TPLOFF; KEY; TPLOFF/NULL
1750	F4	STBYOFF	DVP1/STBYON
1650	F5	STBYON	DVP2/STBYOFF
1550	F6	NULL	RPLON/RPTROFF
1450	F7	NULL	RPLOFF/RPTON
1350	F8	CHN 3; KEY	NULL
1250	F9	CHN 4; KEY	NULL
1150	F10	MORE	ENCRYPTION; MORE/NULL
1050	F11	MORE	ENCRYPTOFF; MORE/NULL
950	F12	SAL A	NULL
850	F13	NULL	LLT/ACK
750	F14	NULL	POLL
650	F15	NULL	NULL

Table 3. DC Currents and Usses

Function Current (mA)	ON/OFF	Standard Use	Optional Use
-12.5	Detect Undetect	CHN 4; KEYON KEYOFF	TPLOFF; KEYON KEYOFF; TLPON
-5.5	Detect Undetect	CHN 3; KEYON KEYOFF	RPLOFF NULL
-2.5	Detect Undetect	MON NULL	NULL NULL
+2.5	Detect Undetect	NULL NULL	NULL NULL
+5.5	Detect Undetect	CHN 1; KEYON KEYOFF	NULL NULL
+12.5	Detect Undetect	CHN 2; KEYON KEYOFF	RPLON NULL

Control is accomplished by the remote device sending a given dc current for each control function which is interpreted by the TTRC module. The TTRC module then initiates the station function via the MUXbus, IPCB, or High Speed Ring. The MUXbus, IPCB, and High Speed Ring are described in the Logic and Control data communications paragraph. Table 3 provides a list of DC currents and their uses.

1.4 TRUNKING CONTROL

The trunking control section on the TTRC module sets up a communications link between the Trunking Central Controller and the *MSF 5000*. The trunking interface connection incorporates inbound transmit audio, outbound receiver audio, and digital control signals. This interface connection originates on connector J2900 on the TTRC logic kernel board which connects to J3 on the station's junction box. The J3 connection on the Junction box is in turn connected to the trunking central controller. The J2900 pinout is provided in paragraph 4.

The state of a trunking system is determined by the central controller. Depending on the state of the system, the station may be performing one of three functions: voice channel, control channel, or failsoft channel. If the control handshaking between the station and central controller is functioning properly, a voice channel or control channel are the only choices. If the control handshaking is interrupted (broken or bad connection, malfunctioning central controller, etc.), a failsoft channel is the only choice.

If the station is in failsoft mode, a subaudible data handshake (failsoft codeword) and an audible tone (failsoft tone) are activated on the station SSCB whenever the repeater goes into failsoft mode. This causes the mobile units to automatically revert to their preassigned failsoft channels and begin conventional repeater operation. The station enters failsoft mode after the loss of handshake form the central controller. This handshake incorporates a tickle pulse sent to the station via Tx Data (+) or the MUTE* line. If the station is in failsoft and a tickle is again detected, the station will resume normal trunking operation based on the central controller.

1.4.1 CONSOLE PRIORITY

Console Priority is a software-enabled option that allows the integration of a console into a trunking system without adding external hardware to the station. This option should not be included in systems that contain a *DIGITAC* comparator or Console Interface Unit (CIU), as they handle the console priority function. This option is intended for use in two separate system types only.

1.4.1.1 TYPE 1 SYSTEMS

A Type 1 System is a Trunked, clear, local area system equipped with a console. In this case, a CIT phone patch is connected to wirelines 3 and 4, and the console is connected to wirelines 1 and 2. Under normal operation CIT audio is mixed with the receiver audio and sent to the transmitter. Detection of HLGT from the console interrupts normal operation and notched console audio is sent to the transmitter until LLGT is lost. Upon loss of LLGT, normal operation resumes. The station always sends its receive audio out on Line 2 and Line 4. Also, the CIT audio is summed onto the console wireline when the console is not accessing the station, and the console audio is summed onto the CIT wireline when the console is accessing the station. This allows the console to monitor both sides of a phone conversation, and the phone user to hear the console operator when he speaks. When the station is in failsoft mode, it sends a HLGT burst on Line 2, followed by LLGT and the receiver audio. This indicates failsoft mode to the console. When the station leaves the failsoft mode, the LLGT is removed.

1.4.1.2 TYPE 2 SYSTEMS

A Type 2 System is a trunked clear system equipped with a receiver, *Spectra-TAC* comparator and console. In this case, the CIT phone patch is replaced with the comparator (operating in the clear mode only). The comparator is connected to wirelines 2 and 3, and the console is connected to wirelines 1 and 4. Under normal operation, comparator audio is mixed with CIT audio at the comparator and the combined audio is sent to the transmitter. Detection of HLGT from the console interrupts normal operation and notched console audio is sent to the transmitter until LLGT is lost. Upon loss of LLGT, normal operation resumes. The station always sends its receive audio on Line 2 and Line 4, the status tone sent out Line 2 when the receiver is squelched. When the station is in failsoft, it sends a HLGT burst out Line 4, followed by LLGT and the receiver audio. This indicates the failsoft mode to the console. When the station leaves the failsoft mode, the LLGT is removed.

1.5 *Spectra-TAC*

The *Spectra-TAC* section of the TTRC module is a software-enabled option that allows the *MSF 5000* station receiver to operate as a receiver-encoder in a wide area coverage system using a *SpectraTAC* analog comparator or *DIGITAC* comparator. The *Spectra-TAC* analog comparator can be used only in clear voice systems, and the *DIGITAC* comparator can be used in either clear voice or coded audio systems.

A clear voice system employs multiple receivers that operate on the same rf frequency over a wide coverage area. One receiver-encoder unit is required at each satellite site. The receiver monitors the rf and amplifies the received audio to be sent to the comparator. The comparator determines which receiver has the best signal and gates that audio to be transmitted. To make sure that audio from each receiver is weighted equally in determining the best signal, an equalization filter is used in the receive audio path of each receiver. The audio between the receivers and comparator are equalized for two reasons: first, the voting process should depend upon the quieting level of the receivers and not on the frequency response of the receiver/comparator connection; second, to improve the intelligibility of the system audio. The equalization filter is fully described in the Receive Audio paragraph.

In coded audio (secure) wide area coverage systems, a *DIGITAC* comparator is used. In this case the equalization filter is not present in the receive audio path during a receive code detect, to preserve the contents of the coded signal. In clear audio systems (no receive code detect), the equalization filter is present.

1.6 SIMULCAST

The simulcast audio section of the TTRC module is a software and hardware enabled option that allows the *MSF 5000* to interface to simulcast systems. Refer to paragraph 4 for a description of hardware jumper positions. In a PL distribution simulcast system, the TTRC typically interfaces with wideband modems (WBM). Voice audio is brought in on Line 1, and PL audio is brought in at GEN TX DATA +/- on J2900 of the TTRC logic kernel. In trunking and secure simulcast systems, the TTRC typically interfaces with a remote delay module (RDM). In this case, all transmit audio is brought in at GEN TX DATA +/-. A more detailed description of the actual circuitry can be found in the Simulcast Mod Audio paragraph.

1.7 INTERFACE

The TTRC module allows the *MSF 5000* to interface in a large number of systems. The interfaces used include a trunking connector (J2901), a systems connector (J2900), and a wireline interface. Both the trunking and systems

connector are presented in paragraph 4. Table 4 provides a detailed outline of the wireline connections for the system types described in the preceding sections.

2. AUDIO SECTION DESCRIPTION

2.1 TRANSMIT AUDIO

2.1.1 OVERVIEW

The Tx Audio section is used to transfer wireline audio originating at a console or other remote device to the station control board (SSCB) for transmission over the air. The transmit audio goes to the SSCB through two paths. Path 1 is RAW TX AUDIO which is sent to the secure module by the SSCB for transparent coded transmissions (secure module not used for 900 MHz models). Path 2 is TX AUDIO for clear transmissions. TX AUDIO is also sent to the secure module by the SSCB for encrypted coded transmissions (only if station is equipped with the secure option). This is accomplished via a wireline interface, an automatic level control (ALC) circuit, a course level adjust circuit, a fine level adjust circuit, and a Tx notch filter. These circuits, described below, are shown on schematic diagram sheet 1.

Table 4. Wireline Interface Matrix

System	Line 1	Line 2	Line 3	Line 4
#1 Conventional Local Area Clear	CONSOLE Routed to: TX Audio, TRC Decoder	CONSOLE Routed from: RCV Audio, TRC Encoder	NOT USED	NOT USED
#2 Conventional Wide Area Clear	COMPARATOR OR CONSOLE Routed to: TX Audio TRC Decoder	COMPARATOR Routed from: RCV Audio Status Encoder	NOT USED	NOT USED
#3 Conventional Local Area Coded	DVM or CIU Routed to: TX audio TRC decoder (new systems) DVM or CIU Routed to: TRC decoder (old systems only)	DVM or CIU Routed from: RCV audio Status encoder (new systems) DVM or CIU Routed from: RCV audio Status encoder (old systems only)	NOT USED (new systems) DVM or CIU Routed to: TX audio (old systems only)	NOT USED
#4 Conventional Wide Area Coded	DVM or *DIGITAC* OR CIU Routed to: TX audio TRC decoder	DVM or *DIGITAC* Routed from: RCV audio Status encoder	NOT USED	NOT USED
#5 Conventional Simulcast Clear	MODEM Routed to: TX audio	COMPARATOR VIA MODEM Routed from: RCV audio Status encoder	NOT USED	NOT USED
#6 w/o CPI Trunked Local Area Clear	CIT PP Routed to: Tx audio	CIT PP Routed from: RCV audio	NOT USED	NOT USED
#7 w/CPI Trunked Local Area Clear	CONSOLE Routed to: TX audio TRC decoder Line 4 output	CONSOLE Routed from: RCV audio TRC encoder Line 3 input	CIT PP Routed to: TX audio	CIT PP Routed from: RCV audio Line 1 input
#8 w/o CPI Trunking Wide Area Clear	COMPARATOR Routed to : TX audio TRC decoder	COMPARATOR Routed from: RCV audio Status encoder	NOT USED	NOT USED

Table 3. Wireline Interface Matrix (Cont'd.)

System	Line 1	Line 2	Line 3	Line 4
#9 w/CPI Trunking Wide Area Clear	CONSOLE Routed to: TX audio TRC decoder	COMPARATOR Routed from: RCV audio Status encoder Line 1 input	COMPARATOR Routed to: TX audio Line 4 output	CONSOLE Routed from: RCV audio TRC encoder Line 3 input
#10 Trunking Local Area Coded	DVM or CIU Routed to: TX audio TRC decoder	DVM or CIU Routed from: RCV audio Status encoder	NOT USED	NOT USED
#11 Trunking Wide Area Coded	DVM or *DIGITAC* Routed to: TX audio TRC decoder	DVM or *DIGITAC* Routed from: RCV audio Status encoder	NOT USED	NOT USED
#12 Trunking AMSS Clear	AUDIO DISTRIBUTOR Routed to: TX audio	COMPARATOR Routed from: RCV audio Status encoder	NOT USED	NOT USED
#13 Trunking AMSS Coded	DVM or *DIGITAC* Routed to: TX audio	DVM or *DIGITAC* Routed from: RCV audio Status encoder	NOT USED	NOT USED
#14 Trunking Simulcast Clear	NOT USED	COMPARATOR VIA MODEM Routed from: RCV audio Status encoder	NOT USED	NOT USED

2.1.2 WIRELINE INTERFACE

The wireline interface network connects the TTRC module (and therefore the station) to the external wirelines. The wireline is connected to the station at the junction box, where lightning protection is provided. Two six-conductor phone wires provide the connection between the junction box and TTRC module. Transformer T4201 (Line 1), transformer T4202 (Line 2), and transformer T4203 (Line 3) match the wireline impedance to that on the TTRC module and provide balanced line inputs to the station. C4239 (Line 1), C4250 (Line 2), and C4238 (Line 3) block any dc currents on the wireline which might otherwise cause T4201, T4202, or T4203 to saturate. P4201 (Line 1), P4217 (Line 2), and P4200 (Line 3) allow the load impedance presented to the wireline to be either high, (10 Kilohms), 900 ohms, or 600 ohms.

T4202 may also be driven by a line driver (described in the Receive Audio paragraph). Therefore, audio on Line 2 may be incoming or outgoing with reference to the station. P4202 must be placed in its normal position and P4205 in its alternate position for a 4-wire setup (Line 1 input). Both P4202 and P4205 must be placed in a configuration opposite to the above for a 2-wire setup (Line 2 input). Input audio leaving JU4202 is then sent to the inverting amplifier (U4200B) where its level is reduced by 4.8 dB before being sent to be transmitted. Line 3 input via T4203 is sent to inverting amplifier U4200A where its level is reduced by 4.8 dB before being sent to be transmitted.

2.1.3 TX LEVEL ADJUST

Wireline audio can take two separate paths before it is sent as TX AUDIO to the SSCB for transmission. Audio leaving U4200B (Line 1 or Line 2 input) is sent to the automatic level control (ALC) circuit, or via U4220B to the course level adjust circuit. Audio leaving U4200A (Line 3 input) is sent via U4220B to the course level adjust circuit. The actual system configuration will determine the wireline input and whether that input will take the ALC or course level adjust path. Refer to Table 4 for the wireline interface matrix.

The course level adjust circuit is a microprocessor-controlled gain stage consisting of analog switches U4218A and U4218B, and inverting amplifier U4200C (EEPOT #E on the front panel status display). The logic state of TX LVL C0 and TX LVL C1 will determine the gain through this amplifier stage. See Table 5 for a description of course gain vs. TX LVL C1 and TX LVL C0.

Table 5. Coarse Gain vs. Logic States of TX LVL C1 and TX LVL C0		
TX LVL C1	**TX LVL C0**	**GAIN (DB)**
Low	Low (0V)	1.7
Low	High (5V)	23.1
High	Low	-8.5
High	High	12.9

The ALC circuit consists of two gain adjust stages. The maximum gain of the first stage (inverting amplifier U4201B) occurs when the effective feedback resistance is highest; that is when FET Q4201 is turned off with a low voltage on its gate. This condition results in about 13.5 dB of gain for the stage. The gain of this stage can be decreased by increasing the gate voltage of the FET (thus lowering the effective feedback resistance of the stage). The lowest gain of this stage is at least -32 dB. The audio signal is next sent to inverting amplifier U4201C, where it is amplified by a constant level of 27 dB. The output of this stage (TP5) drives the tone processing section and is a source for the Tx Audio fine level adjust circuit.

The ALC feedback circuit consists of op amp U4201A, Q4200, and associated circuitry. The audio signal at TP5 is sampled by U4201A and compared to the 5.8 volt reference provided by VR4200. Whenever the peak ac audio signal at TP5 is 1.1 volts higher than the nominal 4.7 volt dc bias, the output of U4201A goes low, turning Q4200 off. Current through R4265 charges C4220, raising the voltage at the gate of FET Q4201. This action lowers the gain of ALC buffer stage U4201B, as well as the average audio signal at TP5. The FET gate voltage continues to rise until the ac audio signal peaks are less than 2.2 Vp-p, or 0 dBm, at TP5. When this occurs, the output of U4201A goes high, turning Q4200 on. The voltage at the FET gate begins to drop as the charge on C4220 bleeds off through R4257. This FET gate voltage drop raises the gain of U4201B until the output of U4201A goes low, turning Q4200 off. This process repeats continuously, resulting in a balanced condition in which ac audio signal peaks at TP5 are always at about 2.2 Vp-p. In addition, the ALC is also under microprocessor control, as described in the TRC Decode Audio paragraph.

The Tx Audio fine level adjust stage following either the ALC or the course level adjust consists of inverting amplifier U4200D and digital potentiometer U4211 (EEPOT #7 on the front panel status display). U4220A determines the source of TX AUDIO. Depending on the setting of U4211, the gain of this stage can vary from -13 dB to -2 dB (ALC as source) or -11 dB to 10 dB (course adjust as source). Refer to Table 6. The nominal audio level expected at the output of the level adjust circuit (TP6) is about 315 mV rms.

2.1.4 ACTIVITY DETECTOR

The input to the activity detector is ALC audio (TP5) which first passes through bandpass filter U4204C. This filter is centered around 1900 Hz with a Q of 1 and a gain of 15 dB. The bandpass filter is followed by a comparator combination of U4204D and Q4233. If the signal entering the activity detector is greater than or equal to -15 dBm around 1900 Hz, the ALC output (TP5) will be considered as activity by the circuit (ACTIVITY* signal is logic low). This voltage level is read by the microprocessor on the logic kernel to detect the presence of audio activity. The main function of this circuit is to support Low Level Guard Tone detection.

2.1.5 TRANSMIT NOTCH FILTER

Audio from the Tx Audio fine level adjust circuit is also sent to Tx Notch Filter Hybrid HY4201A. This hybrid contains an MF10 dual switched-capacitor filter and a dual op amp for summing purposes. Only one of the two filters on the hybrid is being used in the transmit path. The second filter is used in the receive audio path (discussed later). The notch filter is formed by summing together the high-pass and low-pass outputs of the filter IC. The clock that runs the MF10's is derived by the TTRC logic kernel board from the microprocessor E clock via U4233 and U4237. This filter notches out the GT frequency area of the voice spectrum before it is transmitted.

The notch filter has a relatively high Q of 5.8 to remove the GT frequency component but very little voice energy from the transmitted audio signal. Typically, the filter's gain at 1 kHz is 0 dB, and at the notch frequency (usually 2175 Hz) the response is -35 dB relative to 1 kHz. To allow for slight drift of the guard tone frequency (usually due to wireline translation, the filter guarantees 30 dB attenuation at ± 5 Hz from the center frequency. The notch may be removed from the Tx audio path for special applications (such as simulcast) by placing P4204 into its alternate position.

Table 6. Gain Vs. Logic States of TRC LVL C1 and TRC LVL C0		
TX LVL C1	**TX LVL C0**	**GAIN (DB)**
Low	Low (0V)	-20
Low	High (5V)	0
High	Low	-30
High	High	-10

For other applications, Tx audio can be summed into inverting amplifier U4203A (Line 2 Sum) or U4203B (Line 4 Sum) via the Tx notch filter and a line shaping filter. The notch filter can also be removed from this path by placing P4203 into its alternate position . The line shaping filter (U4202A) is a 2 pole low-pass with a -3 dB frequency of 2500 kHz (Q = 0.87).

2.1.6 TROUBLESHOOTING

With a 0 dBm, 1 kHz signal at Line 1 input, a 0 dBm signal should appear at TP5. If not, verify that P4202 is in its normal position and P4205 is in its alternate position (4-wire setup). If P4202 and P4205 are set in an opposite manner, move the wireline input signal to Line 2 (2-wire setup). Assuming a conventional TRC remote control setup, the wireline input signal present at TP6 should be somewhat attenuated. If U4211 is adjusted properly, the level at TP6 should be around 315 mV rms. If there is no signal at TP6, verify that U4220A pin 10 is low. If U4220A pin 10 is high, Tx Audio is not to be sourced from the ALC but from the coarse level adjust stage. If audio is to be sourced from the coarse level adjust stage, verify that U4220B pin 9 is high. If U4220B pin 9 is low, move the input wireline signal to Line 3. The wireline signal should now be present at TP6. If no signal is present, check for the 4.8 V bias and the 9.6 V supply voltages to U4200 and U4201. If no problem exists, check for missing resistors and capacitors along the suspected path. After a signal is verified at TP6, check for its presence at P804 pin 5. If no signal is present at P805 pin 5, verify that P4204 is in either its normal or alternate position. If P4204 is in its alternate position and still no audio is present, look for an open runner between TP6 and P804 pin 5. If P4204 is in its normal position and still no signal is present, check the hybrid filter clock (HY4201 pin 17) for a 0-to-5 volt squarewave at approximately 110.4 kHz. If no clock is present, notch filter hybrid HY4201A may be faulty.

2.2 TRC DECODE AUDIO

2.2.1 OVERVIEW

The TRC decode audio from inverting amplifier U4200B is directed to the automatic level control (ALC) circuit. The output of the ALC is sent to the tone processing section which is the interface for tone decoding between the analog decode audio section and the microprocessor section. This section is responsible for bandpass filtering and limiting the audio signal before passing it to the microprocessor on the TTRC logic kernel board for tone detection.

2.2.2 ALC CONTROL DESCRIPTION

In addition to several analog feedback operations described earlier, the ALC circuit is also controlled by the microprocessor during tone detection and execution of wireline commands.

In its idle state (waiting for HLGT) the LIMIT GAIN* control signal is activated (logic low) and the other control signals are in their de-activated state (ALC RESET* logic high, GAIN UP HOLD logic low, and GAIN DWN HOLD logic low). In this mode, the gain of the ALC is limited so that very low level signals around 2175 Hz (e.g., status tone bleed back in *SpectraTAC* systems) do not provide false indication of HLGT detect. Also in this mode, attack and decay times of the ALC are fast for quick detection of HLGT. The wireline signal could consist of just about anything while searching for HLGT. This condition continues until HLGT is detected by the microprocessor.

When HLGT is detected, LIMIT GAIN* control signal is de-activated (logic high), so that a worst case -35 dBm HLGT signal can be amplified up to 0 dBm at TP5. To help in this amplification (specially in a 2-wire case), ALC RESET* is activated (logic high) for approximately 10 ms to allow C4220 to discharge, causing the ALC gain to increase quickly. After this time, ALC RESET* is de-activated (logic high) and approximately 5 ms is given for the HLGT signal level to adapt to 0 dBm at TP5. When the adapt time has elapsed, GAIN UP HOLD and GAIN DWN HOLD are activated (logic high). This removes the charge and discharge path for C4220. The voltage on the gate of FET Q4201 stays constant (for as long as C4220 can hold it) or until search for HLGT resumes. This action prevents a fast gain-up should wireline activity pause to block "holding on" to noise. This action also prevents any gain-down due to high level noise spikes on the wireline input.

2.2.3 TONE PROCESSING SECTION

The ALC audio from TP5 enters the tone processing section and is bandpass filtered at the guard tone frequency of 2175 Hz by hybrid HY4200. This hybrid contains another MF10 dual switched-capacitor filter IC except this time it uses the bandpass output. Two sections of these bandpass filters, each with a Q of 26, are cascaded. They are used to detect guard tone by attenuating the lower and higher frequency signals which may be higher in level than the guard tone. Remember that while looking for HLGT, high-level voice and receiver noise may be present at the wireline input to the TTRC module in a 2-wire system. The highest level signal tends to capture the limiter, so frequencies other than the guard tone must be attenuated. In spite of this, there is a practical limit on how narrow this filter can be; if it becomes too narrow (high Q), all noise at guard tone frequency as well as guard tone is passed through to the detector, and guard tone falsing is assured. Nominal gain of the bandpass filter is 4 dB while waiting for HLGT. During LLGT detection, U4222C shorts out R4238, making the gain of the filter circuit 15 dB.

After HLGT detection, the bandpass filter is bypassed to allow detection of function tones which usually lie in the range of 650 Hz to 2050 Hz. Detection is accomplished in the microprocessor on the TTRC logic kernel board via U4222A. U4204A and U4204B form a bandpass filter/limiter to attenuate signals outside of the software detec-

tor range, and transform the tone signals into digital ones. This filter is typically 3 dB down at 500 Hz and 4 kHz. The output of this stage is fed to Q4202, which limits and level shifts the signal to CMOS logic levels. The output of Q4202 (TP3) is a square wave which is sent into the microprocessor for analysis.

2.2.4 TROUBLESHOOTING

With a 0 dBm 2175 Hz signal at Line 1 input, a 0 dBm signal should be present at TP5. If no signal is present, verify that P4202 is in its normal position and P4205 in its alternate position (4-wire setup). If P4202 and P4205 are set up in an opposite manner, move the wireline input signal to Line 2 (2-wire setup). After a signal is verified at TP5, check for its presence at TP4. If the signal is present at TP5 but not at TP4, check the hybrid filter clock (HY4200 pin 18) for a 0 to 5 volt squarewave at approximately 110.4 kHz. If no clock is present, HY4200 is probably faulty. After the signal is verified at TP4, check for its presence at TP3. The signal at TP3 should be a squarewave. If no signal is present at TP3, the limiter circuit is probably faulty. First, check U4204A pin 3 for a 3.6V bias. If the bias is proper, check for faulty or missing resistors and capacitors in the limiter circuit.

2.3 RECEIVE AUDIO

2.3.1 OVERVIEW

The Receive Audio section is responsible for transferring LINE AUDIO from the SSCB board to the wireline on Line 2 or Line 4. This section consists of a receive notch filter, summing and level adjust circuits, a *Spectra-TAC* equalizer filter, line drivers, and wireline interfaces. Refer to sheets 2 and 4 of the schematic diagram.

2.3.2 RECEIVE NOTCH FILTER

LINE AUDIO from the SSCB board enters the TTRC module at a level of 325 mV rms (nominal). This Receive Audio is notched at the guard tone frequency by HY4201B in a similar way as described above for the Tx notch filter. Notch depth is the same, but the Q of the Rcv notch filter is slightly lower (3.8), due to the requirement that all of the voice components in the GT frequency range be prevented from reaching the wireline. Without this protection, false guard tone detects by the TTRC module would be inevitable, since audio leaving the TTRC module in a 2-wire system may be up to 20 dB higher than that arriving in order to make up for wireline attenuation. The audio leaving the notch filter next goes through the line shaping filter U4202C before going to the Line 2 or Line 4 summing amps U4203A and U4203B. This line shaping filter is identical to that described in the Tx Audio paragraph.

In secure systems, the receive notch filter and line shaping filter should be bypassed. This is done by switching transmission gate U4221A to its alternate position. This switching is done via the TTRC kernel board microprocessor based on codeplug parameters.

2.3.3 SUMMER/LINE ADJUST

Notched or un-notched Rcv audio from U4221A is sent to the summing amp for Line 2 or Line 4 audio. These stages also sum in tones generated by the TTRC logic kernel board. These encoded tones are usually status (Line 2 only) or guard-tone / function-tone type tones used to signal station status back to a console or remote device. Generation of these tones is described in the logic section of this document.

For Line 2, the audio signal leaving U4203A is sent over two paths, one of which is selected by U4224C. Path 1 goes directly to U4224C and path 2 goes through a *SpectraTAC* equalizer filter, as explained below. Audio leaving U4224C is sent to U4224A which acts as a switch between Line 2 sum audio and audio bias voltage VB. Line 2 sum audio is only passed through U4224A if the LINE MUTE 2 is in a logic low (0 V) state. After passing through U4224A, the audio signal goes to an inverting amplifier adjust stage consisting of U4203C and digital potentiometer U4218 (EEPOT #c on the front panel status display). Depending on the setting of U4218, the gain of this stage can vary from -28 dB to 12 dB.

For Line 4, the audio signal leaving U4203B is sent to U4224B which acts as a switch between Line 4 sum audio and audio bias voltage VB. Line 4 sum audio is only passed through U4224B if the LINE MUTE 4 is in a logic low state. After passing through U4224B, the audio signal goes to an inverting-amplifier adjust stage consisting of U4203D and digital potentiometer U4217 (EEPOT #d on the front panel status display). Depending on the setting of U4217, the gain of this stage can vary from -28 dB to 12 dB.

2.3.4 *Spectra-TAC* EQUALIZER FILTER

The circuit consists of four parts. The first part is inverting amplifier U4210A configured as a bandpass filter with a Q of 3 centered at 400 Hz, followed by digital potentiometer U4215 (EEPOT #A on the front panel status display). The setting of U4215 determines the amount of low end frequency boost, thus directly affecting the intelligibility of the audio. The second part is inverting amplifier U4210C configured as a bandpass filter with a Q of 3 centered at 4 kHz, followed by digital pot U4214 (EEPOT #9 on the front panel display). The setting of U4214 determines the amount of high end frequency boost and is critical to the voting process in a STAC system. To make the voting process independent of the frequency response of the wireline, the audio signal spectrum must be boosted at the higher frequencies to compensate for the high frequency attenuation of the wireline. The critical area of response tends to be between 2 kHz and 4 kHz. The response at the input to the comparator needs to be as flat

as possible between 2 kHz and 4 kHz assuring that the voting process only depends upon the quieting level of the receivers. The third part of the circuit is inverting amplifier U4210B configured as a bandpass filter with -3 dB points at 300 Hz and 3 kHz. The last part is inverting amplifier U4210D, which sums the low-end, midrange, and high-end frequency responses before the audio is sent to the Line 2 level adjust stage.

2.3.5 LINE DRIVER AND CANCELLATION CIRCUIT

The line 2 wireline line driver uses U4209A and U4209B to drive Q4205 and Q4206 in a push-pull arrangement. These transistors drive the secondary winding of T4202. Bias voltage (A+) for the transistors is derived from the center tap of the transformer, allowing a voltage swing on the secondary of about 12 V p-p. This guarantees at least +11 dBm into a 600 ohm load. As mentioned in the Tx audio description, this transformer may be configured for 600 ohm, 900 ohm, or bridged wireline loads.

The cancellation circuit is used only in 2-wire systems when both incoming and outgoing wireline audio is on Line 2. This circuit, consisting of R4300, R4303, R4306, C4253, and C4252 can be disabled by moving P4205 to its alternate position for a 4-wire system. This circuitry couples an out-of-phase sample of the line drivers output back into the decode audio path at U4200B. This helps to decrease the amount of audio in the decode audio path that is only due to the coupling of receive audio back into the decode audio via a 2-wire setup. In this case, receive audio may be up to 20 dB higher than decode audio at the TTRC module due to wireline losses between the station and remote console. The cancellation circuit tends to reduce the amount of this undesired audio in the decode audio path, which enhances the ability of the software algorithm to detect tones.

The line 4 wireline line driver uses U4209C and U4209D to drive Q4207 and Q4208 in a push-pull arrangement. These transistors drive the secondary of T4204. Bias voltage (A+) for the transistors is derived from the center tap of the transformer, allowing a voltage swing on the secondary of about 12 V p-p. This guarantees at least +11 dBm into a 600 ohm load. As mentioned in the Tx audio description, this transformer may be configured for 600 ohm, 900 ohm, or bridged wireline loads.

2.3.6 TROUBLESHOOTING

With a 325 mV rms (nominal), 1 kHz signal at P804 pin 4 (LINE AUDIO), a signal with the same level should be present at TP2. If no signal is present at TP2, check the hybrid filter clock (HY4201 pin 17) for a 0-to-5 volt squarewave at approximately 110.4 kHz. If no clock is present, notch filter hybrid HY4201 may be faulty. Assuming Line 2 as output and a signal at TP2, a signal should also be present at TP11. If the station is hooked up to a comparator or CIU, it is possible a 2175 Hz tone could be present at TP2 and TP11, depending on whether the receiver is squelched or not. If a signal is present at TP2 and TP11 and not at the wireline output, check the supply voltages to U4224, U4216, U4217, U4203, and U4209. If no problem exists, check for faulty or missing resistors and capacitors along the suspected path.

2.4 TRUNKING MOD AND RECEIVE AUDIO

2.4.1 OVERVIEW

Trunking modulation audio (TKG MOD AUDIO) sent to the SSCB board for transmission is sourced from two separate paths. Path 1 is from the trunking central controller via TX DATA (+) and TX DATA (-). The audio on this path comprises either outbound signaling words (3600 baud data) or subaudible digital information (300 baud data). Outbound signaling words are used to direct system users to specific channels. The subaudible digital information (low speed data) is superimposed on all voice communications to unmute the receivers authorized to monitor the communications. Path 2 comprises failsoft codeword and failsoft tone, both of which are generated on the TTRC logic kernel board.

Trunking receive audio (TKG RX AUDIO) is sourced from two separate paths both of which originate on the SSCB. Path 1 is receiver audio (QUAD AUDIO) and path 2 is CONNECT TONE audio. Connect tone audio is used only in coded trunked systems during a receive code detect.

2.4.2 CENTRAL CONTROLLER TRANSMIT INTERFACE

2.4.2.1 DIFFERENTIAL AMPLIFIER

In a non-simulcast trunked system, trunking modulation audio enters the TTRC logic kernel board at J2901 and is passed to the TTRC audio board at J2904 as TX DATA (+) and TX DATA (-). Note that jumpers R4370, R4371, and R4353 must not be present on the TTRC audio board for proper operation in this system. The TX DATA (+/-) level is then reduced by 10 dB and superimposed on the audio bias voltage VB by differential amplifier U4206D. Audio leaving U4206D is next sent to a single-pole double-throw analog switch (U4222B) and is only gated through if the station is not in failsoft. The audio signal leaving U4222B is then sent to the trunking data splatter filter.

2.4.2.2 DATA SPLATTER FILTER

The trunking data splatter filter is a 7-pole bessel low-pass with a -3 dB point of 2.25 kHz. Noninverting-amplifier U4205A comprises the first 3 poles, while U4205B and U4205C comprise the remaining 4 poles. This low-pass filter is required to limit the high frequency content of the audio to be modulated so that sidebands generated as a result of the modulation do not splatter into adjacent channels. Besides attenuating the higher frequencies, this filter has a linear phase response to ensure that no group delay is added in the transmission of data signals.

2.4.2.3 DATA DEVIATION ADJUST STAGE

Audio leaving the data splatter filter is sent to a deviation level adjust stage consisting of inverting amplifier U4205D and digital pot U4213 (EEPOT #b on the front panel status display). Depending on the setting of U4213, the gain of this stage can vary linearly from 0.3 to 1.8. Audio leaving U4205D is sent to U4223B which acts as a switch between trunking modulation audio and audio bias voltage VB. Trunking modulation audio is only passed through U4223B if TKG AUDIO MUTE is in a logic low (0 V) state.

2.4.3 CENTRAL CONTROLLER RECEIVE INTERFACE

Audio from the station's receiver (QUAD AUDIO) is sent back to the trunked central controller in a trunked system. However, depending on the audio signal contents, the path it takes through the TTRC audio board may be different. If the station is assigned as a control channel the receiver audio consists of inbound signaling requests; otherwise the receiver audio consists of normal voice channel activity. If the station is a control channel, CCI ENABLE will be high (5 V) and CT ENABLE will be (0 V). In this case, QUAD AUDIO is routed through the inbound recovery board (IRB) circuit, which consists of noninverting amplifier U4207C. This amplifier boosts the signal level by approximately 8 dB. If the station is a normal voice channel, CCI ENABLE will be low and QUAD AUDIO is routed through the receiver interface board (RIB) filter. This filter consists of the inverting amplifier U4207D. The audio signal level is boosted by approximately 14 dB. Soft limiting is provided at the output of U4207D by VR4215 and VR4214 so the signal level never exceeds + 12 dBm.

In the above discussion, CT ENABLE was always assumed to be in a logic low state. CT ENABLE will only go high if the station is in a coded trunked system and the secure module indicates a receive code detect to the TTRC logic kernel. In a receive code detect state, CONNECT TONE generated on the SSCB board is set to the trunking central controller instead of filtered receive audio.

2.4.4 FAILSOFT CODEWORD AND TONE GENERATION

NOTE

Failsoft codeword and tone, formerly produced on the TTRC Logic board, are now both produced on the Secure Station Control Board (SSCB).

2.4.5 TROUBLESHOOTING

For a trunking setup, first verify the following jumpering before tracing signals through the paths: R4370, R4371, and R4353 should be removed, and R4365, R4366, and R4337 should be present.

With a 1 V rms 150 Hz signal or Low Speed Data at TX DATA (+/–), a somewhat attenuated signal should be present at TP12. If the signal is present but severely distorted, change the polarity on TX DATA (+/–) input. With the signal present at TX DATA (+/–) the station should not be in failsoft, provided that Tx Data (+) is the source for the tickle pulse from the central controller. If the MUTE* line is the source for the tickle pulse, the station may remain in failsoft. Assume that Tx Data (+) is the tickle source. If the signal is removed, the station should go into failsoft. Verify this by checking the failsoft LED; it should be lit. Failsoft codeword should be present at TP12 with a 900 Hz tone burst every 10 seconds. If no signal is present at TP12, check the supply voltages to U4206, U4205, U4220, U4221, U4213, and U4223. If the problem is not cleared, check for faulty or missing resistors and capacitors along the suspected path.

2.5 SIMULCAST MOD AUDIO

2.5.1 OVERVIEW

The simulcast section is used to transfer audio or data originating at a remote delay module (RDM) or wide band modem (WBM) to the station control board (SSCB) for transmission over the air. The contents of the input to this section are different depending on whether a WBM or RDM is the source. In a PL distribution simulcast system, the WBM is typically the source. The contents of the input signal would consist of a PL tone (–10 dBm in level riding on a differential pair with a negative bias voltage). In trunking and secure simulcast systems, the RDM is typically the source. The contents of the input signal would consist of voice audio (–10 dBm in level riding on a differential pair). In either case, R4377, R4378, and R4381 should be removed from the board, and R4370, R4371, and R4378 left in place.

2.5.2 DIFFERENTIAL AMPLIFIER

Simulcast modulation audio enters the TTRC logic kernel board at J2900 and is passed to the TTRC audio board at J2904 as GEN TX DATA (+/–) (600 ohm load). GEN TX DATA (+/–) is then superimposed on the audio bias voltage VB by differential amplifier U4207A. Audio or data leaving U4207A is sent down two paths one of which is selected by U4220C. Path 1 goes directly to U4220C. Path 2 goes through a reverse burst generator circuit explained in the next paragraph. Signals leaving U4220C are sent to the data deviation adjust stage.

2.5.3 REVERSE BURST GENERATOR

Reverse burst is phase shifting of the PL tone signal upon termination of a Line PTT in a PL distribution simulcast station. The phase shift spec is 240 +/– 15 degrees. U4207B, R4358, R4356, R4429, and C4327 form the reverse burst generator. Since the phase shift varies with frequency, R4429 will have the most effect depending on the PL code. R4429 is 16 kilohms, so the above specification is met for PL

codes 4B (146.2 Hz) through 7A (192.8 Hz), since the higher PL codes are used in simulcast systems.

2.5.4 DATA DEVIATION ADJUST STAGE

Audio leaving U4220C is sent to the same deviation level adjust stage described in the trunking mod audio section. The level adjust stage consists of inverting amplifier U4205D and digital pot U4213 (EEPOT #b on the front panel status display). Audio leaving U4205D is sent to U4223B which acts as a switch between simulcast modulation audio and audio bias voltage VB. Simulcast modulation audio is only passed through U4223B if TKG AUDIO MUTE is in a logic low (0 V) state.

2.5.5 TROUBLESHOOTING

For a simulcast system, first verify the following before tracing signals through the paths: R4370, R4371, R4353, and R4337 should be present. R4377, R4378, and R4381 should be removed from the board.

With a -10 dBm PL tone (WBM input) or a 1 kHz tone (RDM input) at GEN TX DATA (+/-), there should be a somewhat attenuated signal at TP12. If no signal is present at TP12, check the supply voltages to U4207, U4220, U4213, and U4205. If the problem is not cleared, check for missing resistors and capacitors along the suspected path.

2.6 DC REMOTE CURRENT DETECTION

The function currents sent from a remote device down the wireline are converted to dc voltage levels by optocouplers U4230, U4231, and associated circuitry. U4230 detects positive line currents and U4231 detects negative line currents. The optocouplers also provide electrical isolation between the wireline and other circuitry on the TTRC module to protect the circuits against lightening hits or high voltage surges.

The voltage levels generated are read by the A-to-D converter on microprocessor (U4231) on the TTRC logic kernel board. The actual current level is determined via a software look-up table and the function initiated.

3. LOGIC SECTION

3.1 LOGIC HARDWARE DESCRIPTION

3.1.1 OVERVIEW

The logic and control hardware are housed on the TTRC logic kernel board (TLN3114A) which is mounted on top of the TTRC audio board (TLN3112A). The two boards are connected via J2904 and J2905. Refer to paragraph 4 for specific pin descriptions.

The logic hardware can be broken down into five broad parts: microprocessor core, data communications circuitry, tone encoders, general I/O, and reset circuitry. Many of the functions performed by the logic section use an Application Specific Integrated Circuit (ASIC). The TTRC kernel uses two of these custom ASICs specifically designed for this product. The ASIC can operate in one of two modes depending on the state of the MODE pin. U4233 operates in the standard mode (with MODE pulled high) and serves as a specialized microprocessor support chip with additional I/O and data communication features. U4234 operates in the I/O mode (with MODE pulled low) and serves as an addressable collection of input buffers and output latches. Refer to Base Stations Technical Report B8804 for more detailed ASIC information not covered in this description.

3.1.2 MICROPROCESSOR CORE

The microprocessor core runs the software program to control the TTRC audio board operations. Most of the core functions use four integrated circuits. Sheet 5 of the schematic diagram shows the microprocessor core circuitry.

U4231 is a Motorola 8-bit single chip microcomputer. During program execution it generates an 8-bit multiplexed data/low-order address bus, AD(0:7)), as well as a high-order address bus, A(8:15). U4231 controls the direction and timing of bus transfers with three signals common to 6800 family devices. U4231-5 is the E signal, and it functions as the primary clock for all bus transfers. U4231 generates the E clock by dividing the external crystal frequency by four (E = 7.9488 MHz /4 = 1.9872 MHz). U4231 controls the direction of bus transfers using the R/W* signal on U4231-6. This signal is high when U4231 needs to read data off the bus and is low when U4231 is writing data to the bus. To allow an external latch in ASIC U4233 to demultiplex the data/low-order address bus, U4231 also generates the AS (address strobe) signal on U4231-4. Thus when AS is high, AD(0:7)) contains the low-order address bus A(0:7), but when AS is low AD(0:7)) contains the data bus D(0:7).

U4231 runs the software program contained in a 32K EPROM (U4235). U4231 also contains 512 bytes of internal EEPROM for operating the parameter storage (code plug). During program execution, U4231 can access 192 bytes of internal RAM as well as an external 8Kx8 SRAM (U4236). U4232 is an optional 2Kx8 serial EEPROM which can be added if additional "code plug" space is required.

Many of the "glue" chips commonly required to complete a microprocessor system are replaced in integrated form by standard mode ASIC U4233. Since U4231 operates with a multiplexed data/low-order address bus AD(0:7)), U4233 contains an address latch to demultiplex this bus. Thus the low-order address bus, A(0:7), is an output of U4233. U4233 also contains all the circuitry required to perform full address decoding using the full 16-bit expanded address bus for the entire 64K memory space. Thus all the required chip select signals are also outputs of

U4233 (refer to software description for memory allocation). The MEM OE* pin drives the output enable pins on EPROM U4235 and SRAM U4236. This signal is active low during every read cycle (E and R/W* both high). The ROM CE* signal drives the chip enable pin on EPROM U4235. This signal is active low whenever the address bus indicates an access in the EPROM memory space. The RAM CE* signal drives the chip enable pin on external SRAM U4236. This signal is active low whenever the address bus indicates an access in the external SRAM memory space. The RAM WE* pin drives the write enable pin on SRAM U4236. This signal is active low during normal write cycles (E high and R/W* low)

3.1.3 DATA COMMUNICATIONS CIRCUITRY

The TTRC logic kernel has three media for communicating with other modules in the station: The IPCB, the MUXbus, and the high speed ring (HSR).

The Inter-Processor Communications Bus (IPCB) is a low speed serial link shared among all the control tray boards and the optional expansion modules. On the TTRC logic kernel, the U4231 interfaces to the IPCB using its serial communications interface (SCI). This link can carry status and control information between modules. The IPCB line is pulled up on the SSCB and is normally high in the idle state until a module begins to write information onto it. The SCI on U4231 has both a receive and a transmit port, and these are buffered by Q4214–Q4217 and wired together before being routed as the IPCB line to the required connectors.

The MUXbus is a time-multiplexed address and data bus capable of carrying 64 bits of control and status information between station modules. The TTRC acts as a MUXbus slave, and all the circuitry interfacing to the MUXbus is contained in ASIC U4233. The SSCB acts as the master and is responsible for driving the data strobe and address lines. The MUXbus consists of 16 4-bit data nibbles for a total of 64 bits. The address bits BA0–BA3 are continually changed to consecutively access each 4-bit data nibble. The 4-bit data nibble is represented by MUXbus data bits BD0*–BD3*. U4233 also asserts the MUXIRQ* signal at every address increment to signal U4231 to service the MUXbus data. All multiplexing timing uses the DS* (data strobe) signal generated on the SSCB. The data strobe signal is generated by dividing the E clock signal by 640 (DS* = 109872 MHz/640 = 3105 Hz).

The High Speed Ring (HSR) is a unique multiprocessor communication mechanism. All the circuitry to implement the HSR is contained in standard mode ASIC U4233. The HSR continually circulates a 40 bit packet between all modules in the ring (SSCB, TTRC, Secure). 16 of these bits can be written to by the TTRC. 16 bits are reserved for writes by the SSCB, and 8 bits are reserved for writes by the optional secure module. All modules can read any of the bits in the 40 bit packet. The SSCB operates as the HSR master and drives the HSR CLK and HSR SYN signals to synchronize all packet transfers. The frequency of the HSR clock is programmable but is normally set to E/2 (0.9936 MHz). The HSR SYN signal is asserted for one bit time at the start of each 40-bit packet. The SSCB sends its HSR OUT data from U801 to the TTRC on J804. Data from the TTRC's HSR is taken on J804 and passed directly to the optional secure module on J803. Data from the optional secure module's HSR is taken from J803 and sent back to U801 as HSR IN to complete the ring.

3.1.4 TONE ENCODERS

Two four-bit tone encoders are included on the TTRC logic kernel. They are driven by 8-bit latch OL12 on U4234. Bits 0–3 of OL12 are used to encode status tone. The status tone encoder frequency can go up to 2500 Hz, but 2175 Hz is the standard. This encoder drives a digital-to-analog converter which uses a common R-2R ladder. The output of the R-2R D/A converter is filtered by two-pole low-pass filter U4238A. This filtering reduces the harmonic noise caused by the limited encoder sample rate. The output of this filter is labeled STAC TONE and is sent to the audio routing section of the TTRC audio board via P2905. Once on the audio board, the tone audio goes through a level adjust stage formed by inverting amplifier U4202D and digital pot U4212. Depending on the setting of U4212 (EEPOT #8 on the front panel status display), the gain through this stage may vary from –46 dB to –6 dB . After being level adjusted, status tone audio is sent to U4203A. Bits 4–7 of OL12 are used to encode TRC tones. TRC tone encoding frequency can go up to 2500 Hz. This encoder drives another digital-to-analog converter which uses a common R-2R ladder. The output of the R-2R D/A converter is filtered by two-pole low-pass filter U4238B. The output of this filter is labeled TRC TONE and is also sent to the audio routing section of the TTRC audio board via P2905. Once on the audio board, this tone audio is sent through a gain stage consisting of analog switches U4218C and U4218D and inverting amplifier U4202B. The logic states of TRC LVL C0 and TRC LVL C1 determines the gain through this amplifier stage (See Table 6).

After being level adjusted, the TRC tone audio is sent to U4221C. If GT LINE 2/4 is set high, the TRC tone is summed into Line 2 audio. This encoder was designed to support HLGT, FT, LLGT tone sequencing.

3.1.5 GENERAL INPUT/OUTPUT

The TTRC logic kernel has a great deal of input/output (I/O) capability to control and monitor remote devices connected to the *MSF 5000* station. The logic section monitors discrete status lines from remote devices using input buffers contained in I/O ASIC U4234. The ASIC has three input buffers:

- IB9 : 8-bit latch from U4234. Bit 0 is used as an audio status signal; bit 1 is used to interface with the system connector; bits 2:3 are spares reserved for future use; and bits 4:7 are not used.

- IB11 : 8-bit latch from U4234. Bits 0:7 are not used.
- IB10 : 8-bit latch from U4234. Bits 0:3 are used to interface with the system connector; and bits 4:7 are used to interface with the trunking central controller.
- ASICs U4233 and U4234 contain general-purpose addressable output latches used for control functions. The following list describes briefly the function of these output latches:
- OL4 : 7-bit latch from U4233. Used for digital pot selection and incrementing.
- OL5 : 7-bit latch from U4233. Bits 0:1 are used to select the divide ratio for the hybrid filter clock generator; bit 2 is used for control; bit 3 is spare for future use; and bits 4:6 are used in LED drive logic.
- OL6 : 8-bit latch from U4233. Bits 0:4,6 are used to control audio gates; bit 5 is used to drive the hybrid clock generator with E/2 clock; and bit 7 is spare for future use.
- OL8 : 4-bit open-drain latch from U4234. Bits 0:2 are used to mute designated audio paths; and bit 3 is used to control audio gating.
- OL10 : 8-bit latch from U4234. Used for controlling the audio gates.
- OL11 : 3-bit latch from U4234. Bit 0 is used to enable loop-back diagnostics; and bits 1:2 are reserved for future use.
- OL12 : 8-bit latch from U4234. Used to drive A/D converters for tone encoding.
- OL13 : 7-bit latch from U4234. Bits 0:2 are used to interface with the system connector; and bits 3:6 are used to control audio routing.
- OL14 : 8-bit latch from U802. Bits 0:2 are used to control audio routing; bits 3:5,7 are used to interface with the system connector; and bit 6 is used to control audio gating.

3.1.6 RESET CIRCUITRY

The reset circuitry resides on the TTRC audio board, and DLYD RESET and RESET* are connected to the TTRC logic kernel via J2904.

The EXPANSION RESET* signal at P804-28 on the TTRC audio board originates on the station control board. This active low signal holds the TTRC logic kernel and audio board in reset whenever the station control or any other module connected on this line pulls it low. The TTRC module cannot generate an EXPANSION RESET* to reset other modules in a system. Internal to the TTRC Module, a RESET* can be generated by either the low voltage reset circuit or U4231 operating properly (COP) reset.

To prevent erroneous writes of the internal EEPROM U4231 during power up, power down or low voltage conditions, RESET* is activated whenever the +5 V supply voltage drops too low. This uses low voltage reset generator Q4220 (shown in schematic diagram sheet 4). This PNP transistor is normally on, pulling up the RESET* line through R4278. When the +5 V line drops too low, Q4220 turns off and provides a passive pulldown on the RESET* line through R4276. This threshold occurs when the +5 V line drops below approximately +3.5 V.

The MCU (U4231) on the logic kernel also contains a COP timer which generates a reset if the COP timer is not periodically serviced by the software routine. This ensures that the TTRC module will restart execution if the program somehow loses proper sequence. The COP circuit generates a short RESET* pulse (~2 E cycles) which forces it to restart at the address indicated by the RESET vector.

The TTRC Module also contains a circuit which inhibits some critical functions while the software performs self-diagnostics. This is achieved using the delayed reset generator U4235. U4235 is a 555 timer which triggers an active high delayed reset line on the standard mode ASIC U4233-46 when the RESET* input goes low. Once the RESET* line is deactivated, the 555 discharges for a time constant defined by C4225 and R4271 (approx. 300 ms) before deactivating the DELAYED RESET line.

3.1.7 TROUBLESHOOTING

If the TTRC logic Kernel is suspect, first check the +5V pins on each of the logic devices U4231-U4237. Next, look at the RESET* line on P2904-40. This line should be high with no pulses on it. Also look at the DELAYED RESET line on P2904-39, which should be low with no pulses on it. If the reset lines are not as expected, verify that U4231, U4233, U4234, and U4235 are properly seated in their sockets (especially 28-pin DIP U4235). Also verify that EPROM U4235 is programmed with the correct version software for this TTRC (U4235 must be compatible with EEPROM codeplug internal to U4231). Also check to see that the A(0:7) demultiplexed bus is being generated on U4231 (pins 66-73). If A(0:7) is not found, then ASIC U4233 is probably faulty. If ASIC U4233 and EPROM U4235 seem OK, and the RESET* line is high, check microprocessor U4231. A properly functioning U4231 will drive the E line (U4231-5) with a 1.9872 MHz square wave. If all these chips are properly functioning, check ASIC U4234 for data bus inputs as well as correct output latch levels.

If the TTRC Module is not responding to commands initiated by the SSCB or secure module, the HSR or MUXbus communication may not be operating properly. Verify that HSR CLK = E/2 (controlled by SSCB) and that the HSR SYN is high every 40 HSR CLK cycles. Also verify that DS* = 3105 Hz square wave and that the address lines are being driven. For proper operation, the address nibble BA0-BA3 should be incremented modulo-16. The SSCB drives both the HSR and MUXbus circuitry; therefore, any problems with the TTRC Module circuitry can be narrowed down to bad connections or open traces between U4233, the inter-board connector P2904, and the inter-module connector P804.

Troubleshoot the tone encoders using procedures similar to those suggested in the audio sections. Circuit blocks can be

analyzed on an input–output basis and fixed if found to be faulty. The tone encoders can be checked by looking at the output of the D/A filters. When a status tone is being generated, a 2175 Hz sine wave should be visible at U4238A–1 on the logic kernel. When TRC tones are being generated, a burst of HLGT (2175 Hz) followed by LLGT should be visible at U4238B–7 on the logic kernel.

3.2 SOFTWARE DIAGNOSTICS DESCRIPTION

When the station powers up or is reset, the station control board holds the TTRC module in reset via Expansion Reset until the station control board finishes its diagnostic tests. When Expansion Reset is deactivated, the TTRC firmware begins execution at the location contained in its RESET vector for Special Test mode. This location is the beginning of the TTRC firmware's main background routine. The main background routine is basically an endless loop (the background loop) which calls all the non–interrupt driven routines. Before entering the background loop, a startup diagnostics routine, "ttrc_reset_diags.asm", is called which performs the TTRC module diagnostic tests of . The TTRC FAIL LED turns on immediately upon station power–up and stays on until the end of the "ttrc_reset_diags.asm" routine. This verifies operation of the FAIL LED and indicates that the TTRC module is performing diagnostics.

The "ttrc_reset_diags.asm" routine mainly performs functionality tests on the TTRC module's hardware circuitry. Before starting the diagnostic tests, however, this routine initializes some microprocessor registers. These registers determine the microprocessor's COP watchdog time–out time and set up the serial communications interface (SCI) to communicate at the same baud rate and message protocol as the other boards on the Inter–Processor Communications Bus (IPCB). This routine also initializes some ASIC registers to their power–up states.

After initialization of the microprocessor, the TRC Encode, Fail Soft and Line PTT LEDs are turned on. This verifies operation of the LEDs and provides a progress indication of the "ttrc_reset_diags.asm" routine.

At this point, the TTRC module diagnostics begin. Diagnostics can yield a number of error conditions; so, in order for the operator to know which diagnostic test has failed, the errors are displayed via either the TTRC module's FAIL LED or the station control board's front panel status display. Two types of error classes exist: fatal and non–fatal. Fatal errors are severe enough to prevent proper operation of the TTRC module; these errors cause the TTRC module to reset. Non–fatal errors, on the other hand, are just warnings and do not prevent operation of the TTRC module; these errors do not cause the TTRC module to reset. Failure of some of the initial diagnostics tests, described below, require that the FAIL LED, as opposed to the front panel display, be used for error display. The FAIL LED must be used because, at this point, the IPCB communications link to the station control board and the TTRC module's external RAM have not been verified. The IPCB must be operating properly because it is required to send the TTRC module's error codes to the station control board; the external RAM is needed to hold the error codes.

All failures which use the TTRC module FAIL LED for display are fatal errors. These errors cause the "ttrc_reset_diags.asm" routine to call an error handler routine with a fixed number. This error handler routine flashes the FAIL LED for that fixed number of times and then waits, not servicing the COP timer. Since the COP timer is not serviced, it will eventually time–out and the TTRC module will reset. Failures which use the front panel display, on the other hand, may be fatal or non–fatal. In this case, when an error is detected, "ttrc_reset_diags.asm" calls a different error handler routine which writes a value, called an error code, to a queue in RAM. Later, after IPCB operation is verified, the "ttrc_reset_diags.asm" routine transmits the error codes one–by–one to the station control board via the IPCB. The station control firmware reads each error code and determines whether it is fatal or non–fatal. If the error code is fatal, the station control firmware displays the error code for five seconds and then stops servicing its COP timer. When the COP timer expires, the station control board resets, activating the Expansion Reset line. Expansion Reset, in turn, resets any board connected to it, which includes the TTRC module. This means that the TTRC module does not reset itself for these fatal errors. If the error code is non–fatal, the station control firmware displays the error for five seconds and continues to service its COP until the next error code is received over the IPCB. Resets do not occur for non–fatal errors.

If a fatal error is left uncorrected, the test which caused the fatal error will fail again, the same error will be displayed, and the firmware will reset again. This sequence will continue until the failure is corrected.

"ttrc_reset_diags.asm" checks two major sections of the TTRC module: the digital hardware and the audio hardware. The "internal" digital diagnostic tests are performed first, followed by the "external" digital diagnostic tests, followed by the audio diagnostic tests. The "internal" digital diagnostic tests verify operation of the TTRC module's digital circuitry as stand–alone hardware. These tests are always done when the TTRC module is reset. The "external" digital diagnostic tests, on the other hand, verify operation of the TTRC module's digital circuitry as part of the overall station control tray. The "external" digital tests are not performed if the TTRC module resets itself; otherwise, the TTRC module, while going through those diagnostics, could adversely affect station operation. Finally, the audio diagnostic tests verify operation of the TTRC module's audio circuitry. These tests are not performed if the TTRC module has reset itself because they also could affect station operation. Before the internal diagnostics are started, the TRC Encode LED is turned off to indicate the start of internal diagnostics.

The first "internal" digital diagnostic test ensures that each RAM byte in the external RAM toggle high and low. After each RAM byte is checked, it is cleared so that all RAM bytes are initially clear. If any external RAM byte fails this test, "ttrc_reset_diags.asm" calls the LED-Flashing error handler routine which uses the TTRC module FAIL LED as the error display. The FAIL LED flashes four times as a result of this error and, as described above, the TTRC module resets because this error handler does not return and does not service the COP.

The next test verifies that the MUXbus_IRQ (IRQ Interrupt) is working. The MUXbus_IRQ interrupt is the result of one byte of MUXbus data written to the ASIC input buffer. This interrupt, when enabled, occurs approx. every 322.1 microseconds. It serves not only to read and write MUXbus data bytes, but also to calculate the data needed for the TRC and STAC encoders, perform two-thirds of the encoder operation, and update the TTRC Software System Timer. If this interrupt fails, "ttrc_reset_diags.asm" calls the LED-Flashing error handler routine, causing the FAIL LED to flash two times.

The next test ensures that each RAM byte internal to the microprocessor can toggle high and low. After each RAM byte is checked, it is cleared so that all RAM bytes are initially clear. If any byte fails to pass this test, "ttrc_reset_diags.asm" writes a fatal error code to the error queue in the external RAM. For this test and all following tests (with the exception of the IPCB test), "ttrc_reset_diags.asm" can put error codes into queue because the external RAM has passed its test. After the internal RAM test, all EEPROM update counters are initialized to their reload values.

The next section of the "ttrc_reset_diags.asm" routine checks the microprocessor configuration, i.e., checks the contents of its CONFIG register. If the CONFIG register is not set up as desired, a check is made to determine if the CONFIG register can be corrected without erasing it. If so, "ttrc_reset_diags.asm" makes the correction and writes a fatal error code to the error queue. If the CONFIG register must be erased in order to correct it, "ttrc_reset_diags.asm" erases the CONFIG register, which erases the entire internal EEPROM, and then reprograms CONFIG for the desired features. Note that erasing the CONFIG register will erase the entire internal EEPROM, which is the codeplug. After making the correction, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

As for all fatal error codes placed into the error queue, these CONFIG re-programmed errors will cause the station control board microprocessor's COP timer to time-out, activating the Expansion Reset and causing the TTRC module to go through a reset. Going through a reset causes the "ttrc_reset_diags.asm" routine to be executed again. However, this test is different in that the "ttrc_reset_diags.asm" routine has previously made a correction before writing a fatal error code to the error queue. So, upon returning to this part of the routine, the CONFIG register should be correct and the firmware should not fail this test again. Note, however, that if the internal EEPROM was erased, the TTRC firmware will get caught in a fatal error loop due to some other error.

At this point, the mode of operation is changed from Special-Test mode to Expanded Multiplexed mode. Next, "ttrc_reset_diags.asm" calculates the single-byte-add double-byte result checksum of the TTRC firmware. If the calculated checksum does not match the value stored in the TTRC firmware, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

The next section of "ttrc_reset_diags.asm" performs tests on the standard mode ASIC and the I/O Mode ASIC. For these first ASIC tests, since "internal" tests are still being performed, the ASIC is put into an "internal" test mode. For the ASIC, "internal" mode means that the ASIC is tested by "ttrc_reset_diags.asm" as a stand-alone device; that is, all outputs are looped back to the inputs. Later, if the "external" diagnostics section of this routine is executed, the ASIC will be tested as part of the overall station control tray.

The first test performed on the standard ASIC is verification of its output latches. Known data is written to the output latches, after which the corresponding loopback input buffers are read. If the output latches and input buffers do not agree, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

Another test of the standard ASIC is a test of the MUXbus circuitry. First, the Data Strobe line is checked. While checking for Data Strobe, the "ttrc_reset_diags.asm" routine also verifies that "0's" can be read at all MUXbus addresses. If that test passes, the "ttrc_reset_diags.asm" routine verifies that "1's" can be read at all MUXbus addresses. These checks verify operation of the MUXbus data and address lines. If any of these tests fail, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

The next standard ASIC tests are associated with the high speed ring (HSR). The first HSR test performed is an operational check of the Ring Synchronization and Ring Clock lines. Two "watchdog" bits (one for Ring Sync and the other for Ring Clock), in the Standard ASIC hardware, are read to determine if Ring Sync and Ring Clock are operating properly. Next "ttrc_reset_diags.asm" writes data to the TTRC portion of the HSR and then reads all portions of the HSR. If the data read from the TTRC portion does not match what was written or if the station control and the secure portions are not zero, the result is an HSR failure. Since the TTRC module is in "internal" test mode, the TTRC module is not connected to the HSR, so the station control and the secure boards could not have written to their portions of the HSR. The inverted version of the data is also written to the TTRC portion of the HSR and the same test is performed. If any of these HSR tests fail, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

The first test performed on the I/O Mode ASIC is verification of its output latches. Known data is written to the output latches, after which the corresponding loopback input buffers are read. If the output latches and input buffers do not agree, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

The next section of "ttrc_reset_diags.asm" compares various parameters between the TTRC codeplug and the TTRC firmware. First, if the module ID stored in the codeplug is not the same as the module ID stored in the firmware, "ttrc_reset_diags.asm" writes a fatal error code to the error queue. Second, if the codeplug version is not equal to the firmware version, "ttrc_reset_diags.asm" writes another fatal error code to the error queue. Finally, "ttrc_reset_diags.asm" calculates the single-byte-add double-byte result checksum of the TTRC codeplug. If this calculated checksum does not match the value stored in the TTRC codeplug, another fatal error code is written to the error queue.

Next, a check is made to determine if a reset occurred during an EEPROM update. In order to understand why this is a problem, the sequence of events to update the EEPROM must be understood. An image of the EEPROM is always kept in RAM; if a user modifies this RAM copy and wishes to make it "permanent" by writing it to the EEPROM, the user must issue a "write-EEPROM- from-RAM" command via the IPCB. This command causes the firmware to first erase the entire EEPROM, causing all bytes to be set to hexadecimal value '$FF'. After erasing the EEPROM, the firmware begins copying the modified RAM image to the EEPROM area byte-by-byte; this copying process can take up to 15 seconds. One byte at the beginning of EEPROM is used as the check byte to determine if all of the RAM image has been copied to the EEPROM. This byte, set to '$FF' by the erase, is set to '00' only after all bytes have been copied from the RAM image to the EEPROM. If a reset occurs before this update is completed, this byte will be '$FF' and "ttrc_reset_diags.asm" will know that the EEPROM is corrupted; a fatal error code is then written to the error queue.

Another check is made to determine if a reset occurred during a "user area" update. The "user area" consists of dynamically changeable data that must be preserved between resets, so the data resides in EEPROM. When an update of the user-area is requested, only the bytes that require changing are reprogrammed; before checking and possibly reprogramming these bytes, the user-area "check byte" is modified to "$FF", and the check byte is programmed to zeroes when the updating process is finished. If a reset occurs before the update is finished, then the check-byte value of "$FF" will be transferred into RAM during the next diagnostic sequence and "ttrc_reset_diags.asm" will then know that the user-area may be corrupted; a unique "user-area corrupt" fatal-error code will then be written to the error queue.

At this point, the "internal" TTRC diagnostics are done and "ttrc_reset_diags.asm" may begin its "external" digital and audio diagnostic tests. To determine whether the "external" tests are to be performed or not, the TTRC firmware must receive a "wake-up" message from the station control board, via the IPCB. However, two conditions can cause the TTRC firmware to wait before it begins looking for the "wake-up"; these conditions are Access Disable being active or reception of a "shut-up" message from the station control board. Access Disable is active if any board in the secure station control fails its audio tests and the operator, wanting to troubleshoot the board, activates the Acc Dis Switch on the front panel. The "shut-up" message comes from the station control board if any part of the station control tray's EEPROM is being updated; any activity which could affect the EEPROM update is therefore inhibited. The "shut-up" message can only be cleared by resetting the station control board. When Access Disable is inactive and the "shut-up" message is not received, the TTRC firmware begins looking for the "wake-up" message. This message tells the TTRC firmware to execute its "external" diagnostic tests. If the wake-up is not present immediately, the TTRC module starts a ten-second timer and waits for the "wake-up". This "wake-up" time allows the station control to finish its "external" diagnostic tests. During this time, EEPROM operations are enabled to allow EEPROM updates; so if the "shut-up" message is received, the timer is stopped. The timer is also stopped if Access Disable is activated during this time. If the "wake-up" does not occur within the "wake-up" time-out time, "ttrc_reset_diags.asm" writes a non-fatal error code to the error queue (this non-fatal error indicates that the TTRC module has reset without Expansion Reset being activated) and the "external" diagnostic tests are bypassed. Whether the TTRC firmware does receive the "wake-up" indication or not, the Fail Soft LED is turned off to indicate that the TTRC module has finished its "internal" digital tests.

The first "external" digital test verifies operation of the MUXbus circuitry; this test is performed only if the TTRC firmware receives the "wake-up" message from the station control board. The reason for this is that the MUXbus should not be manipulated by this test if the TTRC module alone has reset. The tests performed on the MUXbus at this point are identical to the previous MUXbus tests, but now the MUXbus circuitry is interacting with the master MUXbus circuit on the station control board and any other slave MUXbus circuits on other boards. If any of the MUXbus tests described above fail, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

The HSR test, which follows the MUXbus test, is also performed only if the TTRC firmware has received the station control "wake-up" message. The tests performed on the HSR at this point are identical to the previous HSR tests but now the HSR circuitry is interacting with the master HSR circuit on the station control board and any other slave HSR circuits on other boards. If any of the HSR tests described above fail, "ttrc_reset_diags.asm" writes a fatal error code to the error queue.

Up to this point, all the error codes have been entered into an error queue with the intention of sending them to the station control board, via the IPCB. When the station control board receives the error codes, it will display them one-by-one. However, if the IPCB is not working, any errors from the TTRC module can not be displayed. Therefore, the next test verifies operation of the IPCB by sending a known IPCB message to the station control board. If the station control board does not respond or does not respond with the expected response, "ttrc_reset_diags.asm" calls the LED-Flashing error handler routine, causing the FAIL LED to flash 6 times.

Once IPCB operation is verified between the TTRC module and the station control board, the TTRC module can send its error codes via the IPCB for display on the station control board's front panel status display. Since most error codes up to this point have been fatal errors, the first error code received by the station control board will most likely be fatal and therefore cause the station control board to reset. If the station control board does reset, no further error codes will be displayed. The IPCB test is the final "external" digital diagnostic test.

The next tests, checking operation of the TTRC module's audio paths, are also performed only if the TTRC firmware receives the "wake-up" message from the station control board. This will ensure that a TTRC module, which has reset by itself, does not interfere with a normal operating station. Note that for this test and all following tests, "ttrc_reset_diags.asm" no longer needs to put its error codes into a queue because the IPCB has passed its test; instead, the error codes can be sent immediately to the station control board. Also for this test and the audio diagnostics which follow, once the error (always non-fatal) is displayed, the operator will have two seconds to activate the Acc Dis switch on the station's front panel. If the Acc Dis switch is activated within that time, the current diagnostic conditions will "freeze" to allow the operator to troubleshoot the failed circuit. Freezing the current diagnostic test may be desirable because this allows audio gating which may not be possible in normal operation. If the operator misses the time to activate the switch, the station can be reset with the Reset switch and the operator can then wait until the failed diagnostic test is executed again.

If any audio of the following audio tests fail, four seconds are allowed before the next test to permit the station control board time to display the error code.

Control is passed to "ttrc_audio_diags.asm" to perform TTRC audio diagnostics. Before beginning audio diagnostics, the A/D converters of the microprocessor are checked to verify that they are operational. If any of the A/D converters fail, "ttrc_audio_diags.asm" immediately sends a non-fatal error code to the station control board for display.

The first audio circuit to be checked is the TRC encoder including the four-stage gain circuitry. If the 1000 Hz tone is not present at the appropriate A/D converter at the expected level when the tone is enabled or if the 1000 Hz tone is present at the A/D converter when the tone is disabled, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

The next tested audio path is the TRC encoder to Line 4 path. For this test, a 2500 Hz tone from the TRC encoder is gated to Line 4. The corresponding A/D converter is read, with Line 4 Level EEpot set at its minimum, mid-range, and maximum values. If the tone is not present at the corresponding A/D converter at the expected level, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display. Next the Line 4 mute gate is activated. If the tone is still present at the corresponding A/D converter, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

Next, the STAC encoder is tested. For this test, a 1000 Hz tone from the STAC encoder is generated. The corresponding A/D converter is read, with STAC Level EEpot set at its minimum, mid-range, and maximum values. If the tone is not present at the corresponding A/D converter at the expected level, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display. Next, the STAC encoder is turned off. If the tone is still present at the corresponding A/D converter at the expected level, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

The next tested audio path is the STAC encoder to Line 2 path. For this test, a 1000 Hz tone from the STAC encoder is generated. The corresponding A/D converter is read. If the tone is not present at the corresponding A/D converter at the expected level, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

Next, the tone detector path is tested. For this test, a 1000 Hz tone from the STAC encoder is generated and looped back to wireline 1. Input Capture 1 interrupt is enabled to capture the time between edges on wireline 1. The tone detection filter is set to look for function tones. If the period of the edges does not correspond to the expected period for a 1000 Hz tone, an error condition exists. Next, the tone detection filter is set to look for guard tone. If the period of the edges corresponds to the expected period for a 1000 Hz tone, a failure exists. Next, a tone corresponding to the guard tone frequency is generated on wireline 1 via status tone looped back to line 1. If the period of the edges does not correspond to the expected period for guard tone, an error condition exists. For all detected errors, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

Next, the ALC audio path is tested. With a 1000 Hz tone on wireline 1, the corresponding A/D converter is read. If the tone is not present at the expected level, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

Next, the activity detector audio path is tested. For this test, a 1000 Hz tone from the STAC Encoder is generated

and looped back to wireline 1 and then turned off. If the Wireline_Activity bit of the ASIC input buffer does not indicate activity when the tone is present or it indicates activity when the tone is not present, a non-fatal error code is sent to the station control board for display.

Next, the ALC Line 1 Audio to Line 4 Path is tested. For this test, a 1000 Hz tone from the STAC encoder is generated and looped back to wireline 1. First ALC audio is not gated through to Line 4. The corresponding A/D converter is read. Next, the ALC audio is gated through to line 4. The corresponding A/D converter is read, with Tx Level EEpot set at its minimum, mid-range, and maximum values. If the tone is present at the A/D converter when the tone is not gated through or if the tone is not present at the corresponding A/D converter at the expected level when it is gated through, a non-fatal error code is sent to the station control board for display.

Next, the ALC Line 1 Audio to Line 2 Path is tested. The ALC audio is gated through to Line 2. The corresponding A/D converter is read. If the tone is not present at the corresponding A/D converter, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

Next, the Non-ALC Line 1 Audio to Tx Audio Path is tested. For this test, a 1000 Hz tone from the STAC encoder is generated and looped back to wireline 1. Tx Level EEpot is set at its mid-range value. If the 1000 Hz tone is not present for each of the four coarse adjust levels at the A/D converter at the expected level, "ttrc_audio_diags.asm" sends a non-fatal error code to the station control board for display.

Finally, the trunking mod audio path is tested. For this test, a 1000 Hz failsoft tone is generated. The failsoft tone is gated through to trunking mod audio. The corresponding A/D converter is read with Trunking Dev EEpot set at its minimum, mid-range,and maximum values. If the tone is not present at the expected level, an error exists. Next the failsoft tone is turned off and the failsoft codeword is activated with a 150 Hz tone. The corresponding A/D converter is read with Trunking Dev EEpot set at its maximum value. If the tone is not present at the corresponding A/D converter at the expected level, a failure condition exists. Next, the data/failsoft gate is switched from failsoft to data. If the tone is present at the corresponding A/D converter, a failure exists. For all errors discovered, non-fatal error code is sent to the station control board for display.

Note that the audio tests could fail if there are unexpected active inputs to the station from an outside source.

After audio diagnostics, control is returned to "ttrc_reset_diags.asm". Line PTT LED is turned off to indicate completion of audio diagnostics.

Next the EEpots are initialized to their corresponding values stored in EEPROM. If an EEPOT can not be reset to its initial value, "ttrc_reset_diags.asm" sends a fatal error code to station control board for display.

After EEPOT initialization, the "ttrc_reset_diags.asm" tests are completed. At this point, the version number of the TTRC firmware is transmitted to the station control board via the IPCB; the station control firmware displays this version number.

Next, the TTRC module output latches are initialized and the various parameters for the TTRC operation are loaded into the working RAM from the codeplug RAM image. The Output Compare 3 interrupt is enabled to allow tone encoding. Input Capture 1 is set up to capture on rising edges, for wireline tone detection. Input Capture 2 is set up to capture on falling edges, and Input Capture 3 is set up to capture on any edge. Input Captures 2 or 3 are used to detect tickle pulses from the central controller. Input Capture 2 monitors the Tx Data line and Input Capture 3 monitors the MUTE line.

"ttrc_reset_diags.asm", if given the "wake-up" message described earlier, now waits for a "background-enable" message from the station control board, via the IPCB. If the enable occurs, "ttrc_reset_diags.asm" begins execution of the background routines (note that no time-out timer is used while waiting for the "background-enable"). The "background-enable" requirement prevents the TTRC firmware from executing its background before the other remote boards have completed their diagnostics and possibly causing those boards to fail their diagnostic tests due to manipulation of the MUXbus, HSR, and IPCB. If the TTRC firmware did not receive the "wake-up" message earlier in the routine, it is assumed that the TTRC firmware has reset on its own and therefore should not wait for a "background-enable" message from the station control board. In this case, the TTRC firmware immediately begins execution of the background routines. Before beginning execution of the background, for either case above, the TTRC module's FAIL LED is turned off to indicate that the TTRC firmware is executing its background routines.

4. STATION SYSTEM CONNECTOR

The wiring between the TTRC Logic Kernel Board connector, P2900, and the Junction Box 25-pin female D System connector is shown in Table 7.

4.1 DEFINITIONS FOR DESCRIPTION COLUMN OF TABLE 7.

- AG - Indicates audio ground
- $\overline{\text{Site Failsoft}}$ - This is an active low input. In trunking stations, activating this input changes the failsoft mode. It does not cause a failsoft condition, but when the station goes into failsoft (in the normal manner) it causes a "Site Failoft".
- LG - Indicates logic ground.

- Tx Inhibit – This is an active low input. It inhibits all transmitter activity, regardless of the key request.
- Gen Tx Data (+/–) – Data/audio from Remote Diagnostics Module (RDM) or Wide Band Modem (WBM) in trunked simulcast systems.
- RF Relay Control – This is an active high output. The output is switched to the boards A+ line and is capable of supplying up to 300 mA
- Rdstat – This is an active low output. There is no pull-up on the board side. This output is simply a reflection of the RX1ACT MUXbus bit ORed with the RXCDDT MUXbus bit, and therefore indicates the receiver 1 qualified squelch detect OR receiver Code Detect.
- $\overline{\text{Rx Code Detect}}$ – This is an active low output. There is no pull-up on the board side. This output is pulled low whenever the station detects the presence of secure data on receiver 1.
- $\overline{\text{Failsoft Indicate}}$ – This is an active low output. There is no pull-up on the board side. This output is pulled low whenever the station is in local or site failsoft.
- $\overline{\text{Ext PTT}}$ – This is an active low input. By default, this input causes a Line PTT by writing the LINPTT bit on the MUXbus.
- $\overline{\text{Rx Inhibit}}$ – This is an active low input. It prevents the station from driving both outbound phone lines (Line 2 and Line 4) with receiver audio or status tone.
- $\overline{\text{Ext Tx Code Detect}}$ – This is an active low input. It is used to indicate to the station that another secure device (usually a modem or CIU) has detected the presence of secure code.

4.2 TRUNKING CENTRAL CONNECTOR

The wiring between the TTRC Logic Kernel Board connector, J2901, and the Junction Box 25-pin female D Trunking connector is shown in Table 8.

4.3 TTRC JUMPER DESCRIPTIONS

Table 10 shows the various operating modes selected by positioning of the Berg Jumpers or placement of the Resistor Jumpers (either installed or removed from the TTRC module).

Table 7. TTRC Logic Kernel Board Connector (P2900) to Station Junction Box System Connector Wiring

P2900 On TTRC Module Pin NO.	Description/ Wire Color	Junction Box System Connector Pin NO.
1	AG (Green/White)	17
2	Site Failsoft* (Blue/Black)	18
3	LG (Orange/Black)	19
4	TX Inhibit* (Black/White)	5
5	Gen TX Data (–) (Green/Black)	20
6	Gen TX Data (+) (Red/Black)	21
7	RF Relay Control (White/Black)	22
8	Rdstat (Blue)	23
9	Spare Output (Red/White)	9
10	RX Code Detect* (Orange)	11
11	Failsoft Indicate* (Green)	24
12	Ext PTT* (Red)	12
13	Rx Inhibit* (Black)	25
14	Ext Tx Code Detect* (White)	13

Table 8. TTRC Module Trunking Connector (J2901) to Station Junction Box System Connector Wiring

J2901 On Ttrc Module Pin NO.	Description/ Wire Color	Junction Box Trunking Connector Pin NO.
1	LG (Logic Ground)	17
2	LG	18, 19
3	AG (Analog Ground)	20
4	TX Data (-)	21
5	Trunking Rx Audio	22
6	Mute*	23
7	Duplex Enable	9
8	Tkg PTT	11
9	CCI*	24
10	TSTAT	12
11	RSTAT	25
12	Tx Data	13

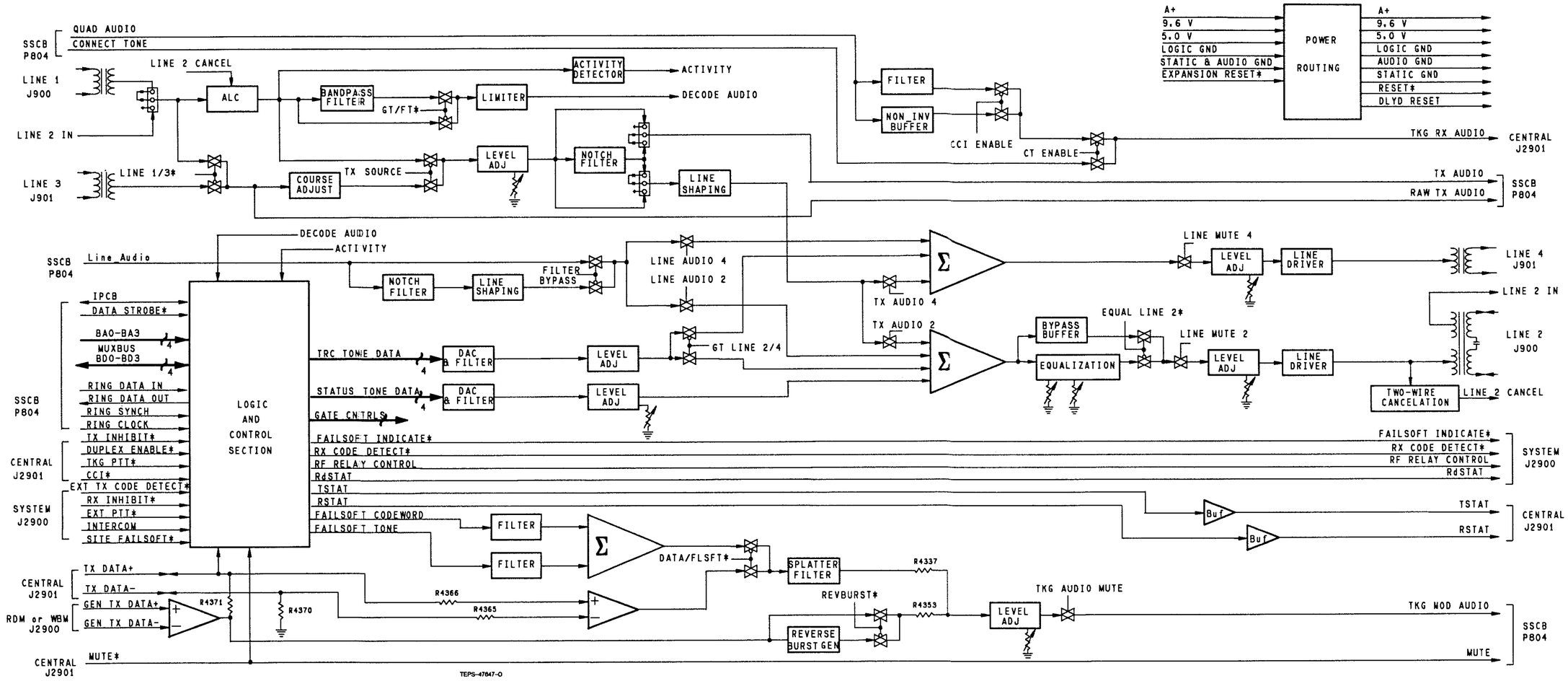
Table 9. TTRC Jumper Description – A Version boards

BERG JUMPERS		
Jumper	**Position**	**Function**
JU4200	Normal Position Alternate Position	600 ohm term. Line 3 900 ohm term. Line 3
JU4201	Normal Position Alternate Position	600 ohm term. Line 1 900 ohm term. Line 1
JU4202	Normal Position Alternate Position	4-Wire audio (for Line 2 or Line 1 input) 2-Wire audio
JU4203	Normal Position Alternate Position	Notched Tx Audio for Lines 2 and 4 Tx Mix Un-notched Tx Audio for Lines 2 and 4 Tx Mix
JU4204	Normal Position Alternate Position	Notched Tx Audio to modulator Un = notched Tx Audio to modulator
JU4205	Normal Position Alternate Position	2-Wire audio (for cancellation circuit) 4-Wire audio
JU4206	Normal Position Alternate Position	4-Wire audio (for DC Remote Control) 2-Wire audio
JU4207	Normal Position Alternate Position	4-Wire audio (for DC Remote Control) 2-Wire audio
JU4217	Normal Position Alternate Position	600 ohm term. Line 2 900 ohm Term. Line 2
JU4218	Normal Position Alternate Position	600 ohm term. Line 4 900 ohm term. Line 4
RESISTOR JUMPERS		
Jumper	**Position**	**Function**
R4353	IN OUT	Stations with simulcast Stations without simulcast
R4370	IN OUT	Stations with simulcast Stations without simulcast
R4371	IN OUT	Stations with simulcast Stations without simulcast
R4377	IN OUT	All standard stations Stations with simulcast
R4378	IN OUT	All standard stations Stations with simulcast
R4381	IN OUT	Special simulcast systems All standard stations

Table 10. Trunked Tone Remote Control Board (TTRC) Jumpers – B Version boards

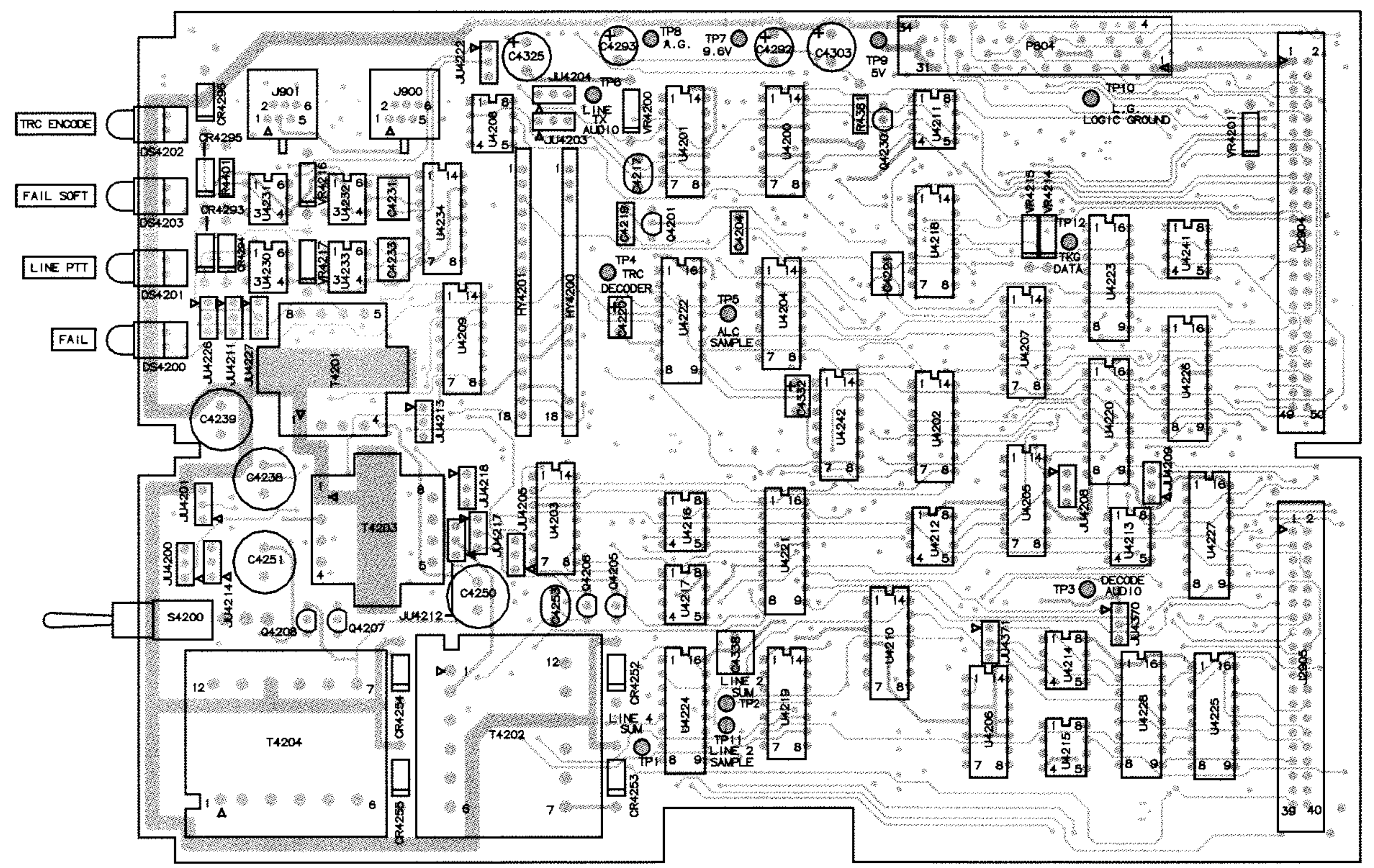
Jumper #	Description	Normal Position	Alternate Position
JU4200	Line 3 termination	600 ohm	900 ohm
JU4201	Line 1 termination	600 ohm	900 ohm
JU4203	Tx Audio Mix notch	notched	un-notched
JU4204	Tx Audio notch	notched	un-notched
JU4205	Line 2 Cancellation circuit	2-wire audio	4-wire audio
JU4208	Trunked Mod audio	Central audio	Gen Tx audio
JU4209	RDM/WBM Simulcast	RDM	WBM
JU4211	Line 1 DC blocking cap	Secure out	Secure in
JU4212	Line 2 DC blocking cap	Secure out	Secure in
JU4213	Line 3 DC blocking cap	Secure out	Secure in
JU4214	Line 4 DC blocking cap	Secure out	Secure in
JU4278	Line 2 termination	600 ohm	900 ohm
JU4218	Line 4 termination	600 ohm	900 ohm
JU4222	Wireline Configuration	2-wire audio	4-wire audio
JU4226	DC control (+) input	2-wire audio	4-wire audio
JU4227	DC control (-) input	2-wire audio	4-wire audio
JU4370	Gen Tx Data Input	Non-simulcast	Simulcast
JU4371	Gen Tx Data Input	Non-simulcast	Simulcast
R4381	0 ohm resistor	out	in for SP Simulcast

TRUNKED TONE REMOTE CONTROL MODULE
BLOCK DIAGRAM



TRUNKED TONE REMOTE CONTROL MODULE

TLN3112B TTRC AUDIO BOARD
CIRCUIT BOARD DETAILS



SHOWN FROM COMPONENT SIDE

BD - TEPS - 47406-A

OL - TEPS - 47407-A

NOTE: AN ASTERICK(*) AFTER OR A LINE OVER A SIGNAL NAME INDICATES AN ACTIVE LOW LEVEL SIGNAL

P804

Signal	Pin	Pin	Signal
5V	33	34	STATIC & AUDIO GND
5V	31	32	A+
MUTE	29	30	GEN TX DATA +
CONNECT TONE	27	28	EXP RESET*
DATA STROBE	25	26	IPCB
BA1	23	24	BA0
BA3	21	22	BA2
BD1*	19	20	BD0*
BD3*	17	18	BD2*
HSR SYNCH	15	16	LOGIC GND
HSR CLK	13	14	LOGIC GND
HSR DATA OUT	11	12	LOGIC GND
HSR DATA IN	9	10	LOGIC GND
TKG MOD AUDIO	7	8	QUAD AUDIO
TX AUDIO	5	6	RAW TX AUDIO
9.6V	3	4	LINE AUDIO
A+	1	2	STATIC & AUDIO GND

J2904

Signal	Pin	Pin	Signal
STATIC & AUDIO GND	50	49	ALC SAMPLE
CURRENT +	48	47	CURRENT -
TRC TONE SAMPLE	46	45	STAC TONE SAMPLE
LINE 2 SAMPLE	44	43	LINE 4 SAMPLE
TKG DATA SAMPLE	42	41	SPARE (HI)
RESET*	40	39	DLYD RESET
TX LVL ADJ CS*	38	37	STAC LVL CS*
HIGH EQUAL CS*	36	35	LOW EQUAL CS*
DATA DEV CS*	34	33	LINE 2 LVL CS*
LINE 4 LVL CS*	32	31	LVL INC*
TX DATA(-)	30	29	TX DATA(+)
GEN TX DATA(-)	28	27	GEN TX DATA(+)
5 V	26	25	5 V
A+	24	23	MUTE
IPCB	22	21	DATA STROBE
BA0	20	19	BA1
BA2	18	17	BA3
BD0*	16	15	BD1*
BD2*	14	13	BD3*
HSR SYNCH	12	11	LOGIC GND
HSR CLK	10	9	LOGIC GND
HSR DATA OUT	8	7	LOGIC GND
HSR DATA IN	6	5	LOGIC GND
TKG RX AUDIO	4	3	9.6V
STATIC & AUDIO GND	2	1	A+

J2905

Signal	Pin	Pin	Signal
ACTIVITY*	40	39	REVBURST
GAIN DOWN HOLD	38	37	ALC RESET*
FILTER CLK	36	35	EQUAL LINE 2*
DATA/FLSFT*	34	33	GAIN UP HOLD
GT LINE 2/4	32	31	FILTER BYPASS
CT ENABLE	30	29	CCI ENABLE
GT/FT*	28	27	LVL U/D*
TX LVL C0	26	25	TX LVL C1
LPTT	24	23	TX AUDIO 4
TRC LVL C0	22	21	TRC LVL C1
STAC TONE	20	19	TRC TONE
LINE MUTE 2	18	17	LINE MUTE 4
TKG AUDIO MUTE	16	15	TX SOURCE
LOOP BACK	14	13	DECODE AUDIO
INTERCOM	12	11	FAILSOFT CODEWORD
FAILSOFT TONE	10	9	FAIL LT
LINE PTT LT	8	7	TRC ENCODE LT
FAILSOFT LT	6	5	LIMIT GAIN*
LINE 1/3*	4	3	LINE AUDIO 2
LINE AUDIO 4	2	1	TX AUDIO 2

J900

Signal	Pin	Pin	Signal
	5	6	LINE 2 +
LINE 1 +	3	4	LINE 2 -
LINE 1 -	1	2	

J901

Signal	Pin	Pin	Signal
	5	6	LINE 4 +
LINE 3 +	3	4	LINE 4 -
LINE 3 -	1	2	

TRANSISTOR DETAILS

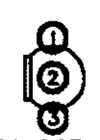
4811043C43

1 -EMITTER
2 -BASE
3 -COLLECTOR

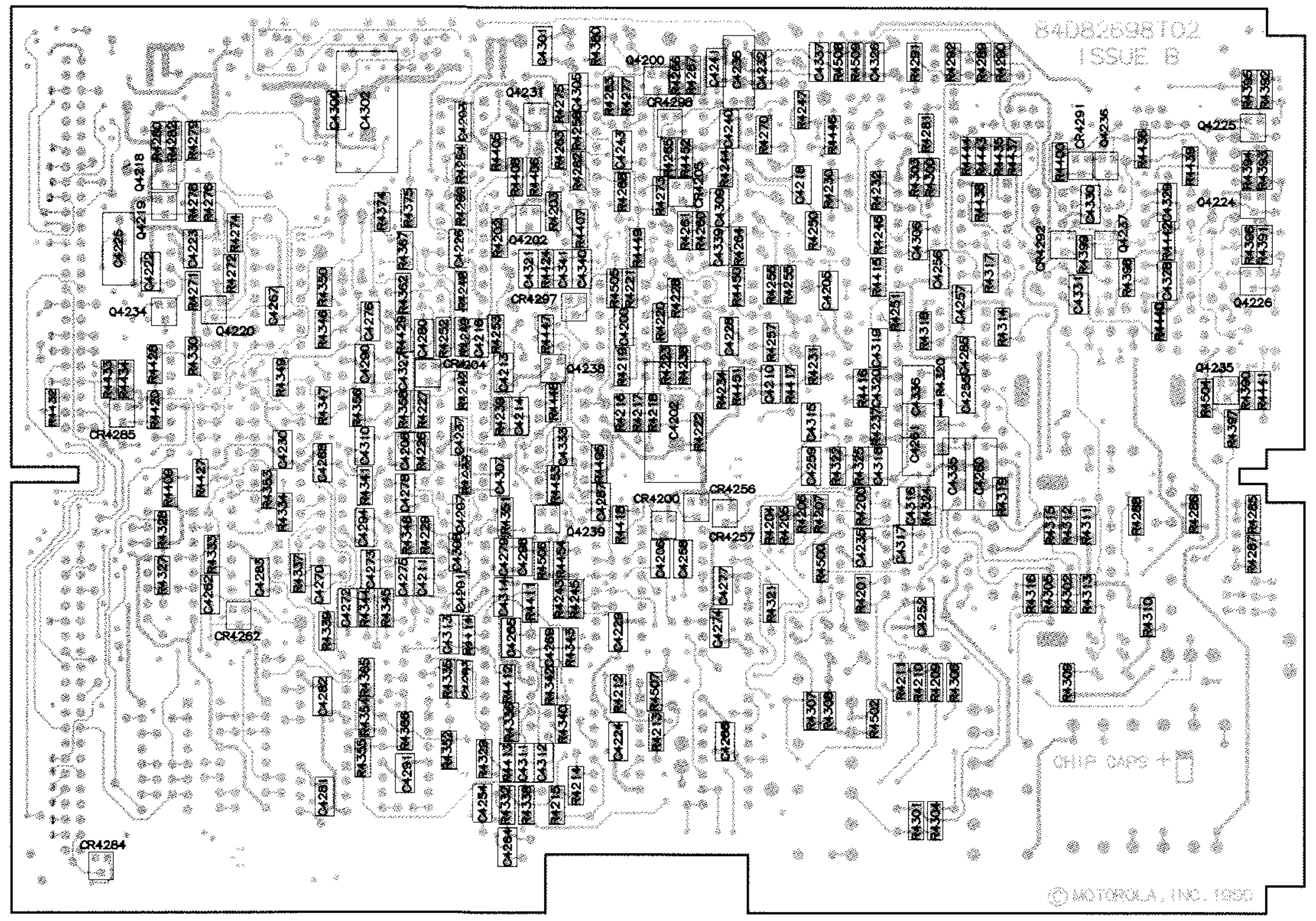
4800869653
4811043C37

1 -DRAIN
2 -SOURCE
3 -GATE

4800869919



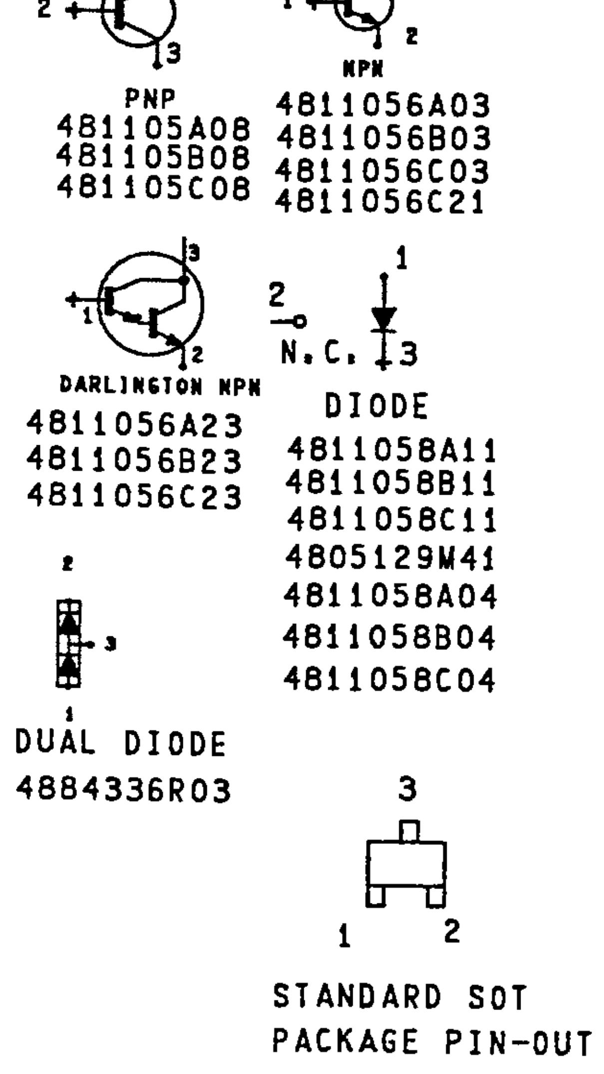
1 -SOURCE
2 -GATE
3 -DRAIN



SHOWN FROM SOLDER SIDE

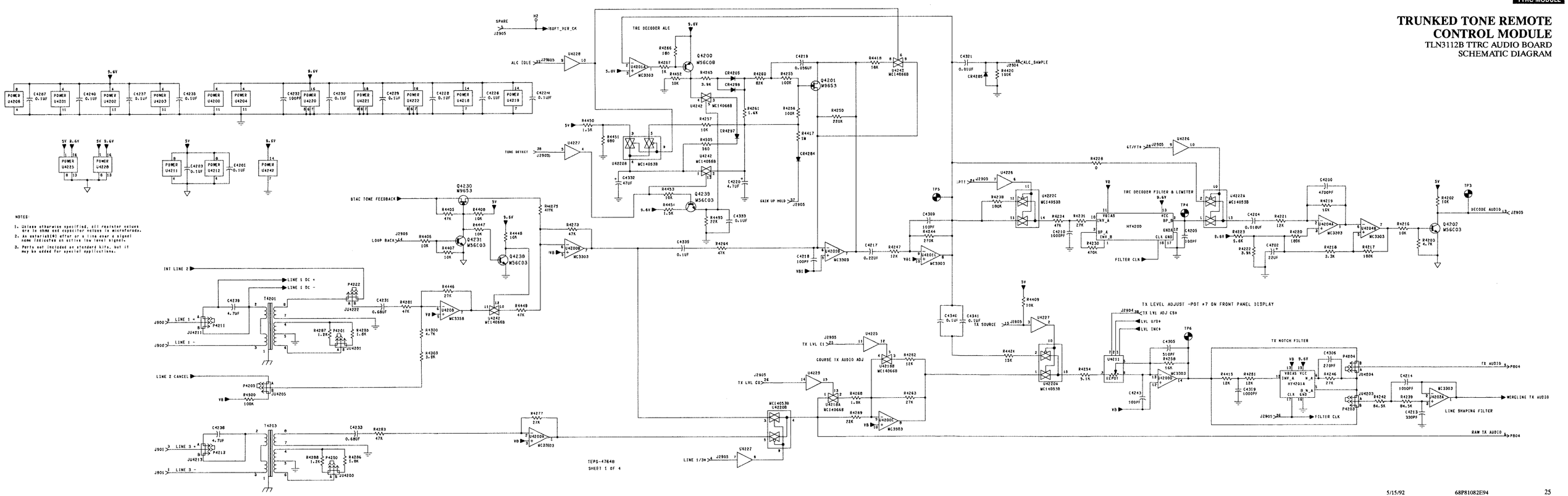
BD - TEPS - 47408-A

OL - TEPS - 47409-A



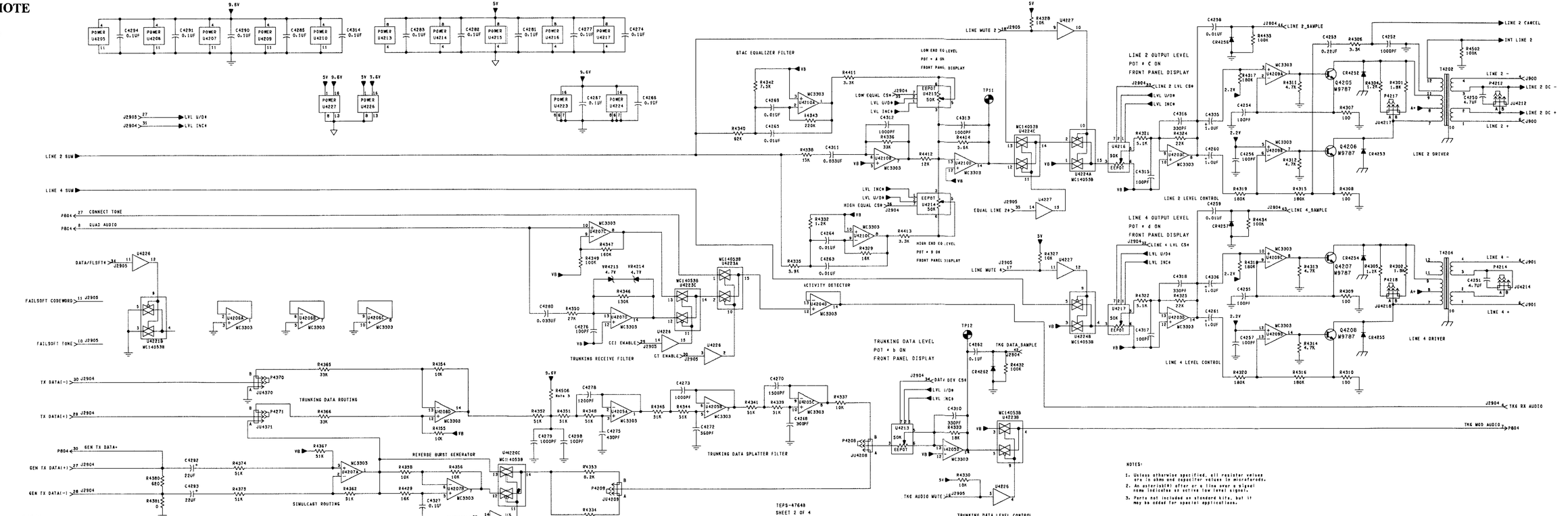
TRUNKED TONE REMOTE CONTROL MODULE

TLN3112B TTRC AUDIO BOARD
SCHEMATIC DIAGRAM



TRUNKED TONE REMOTE CONTROL MODULE

TLN3112B TTRC AUDIO BOARD
SCHEMATIC DIAGRAM

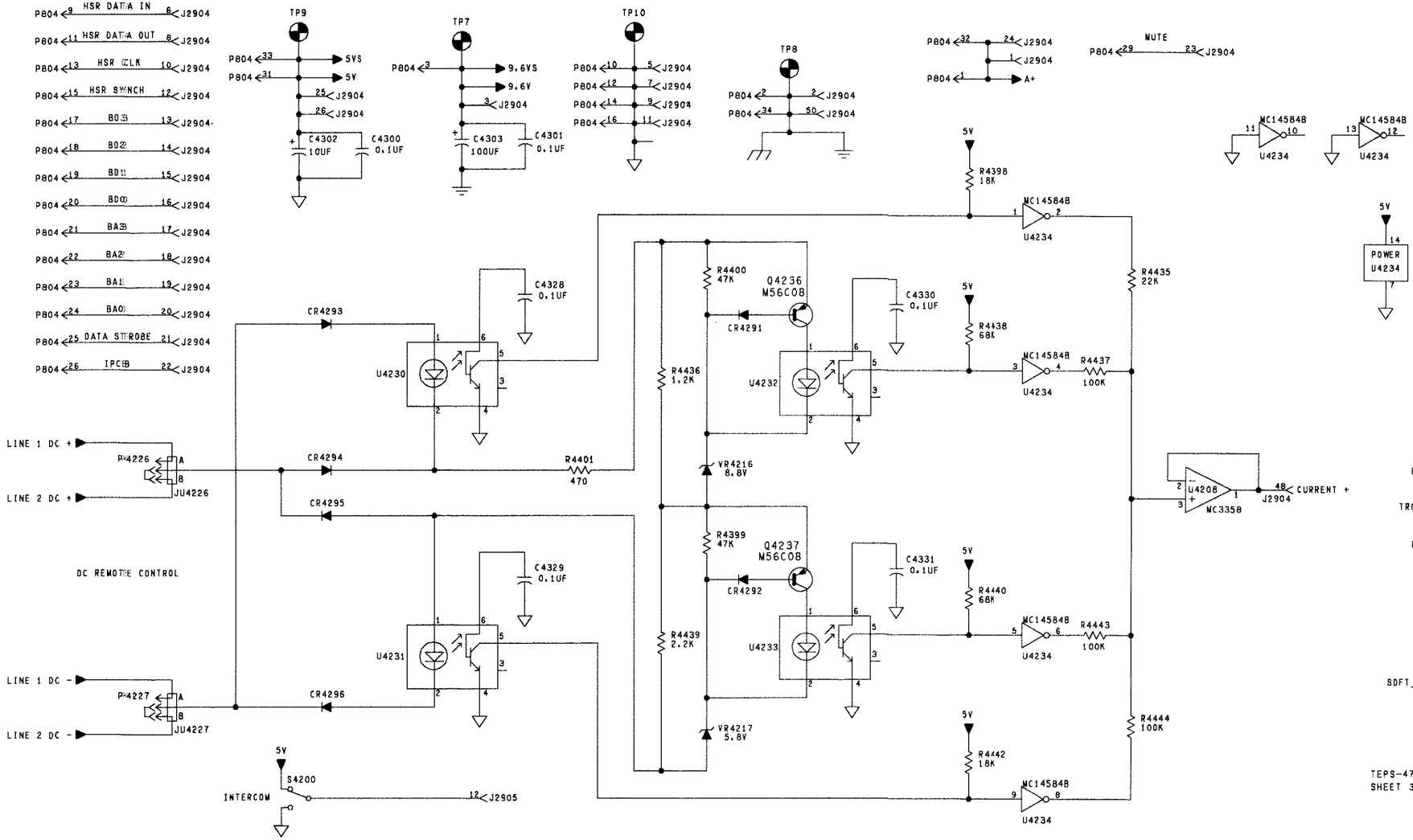


NOTES:

1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but it may be added for special applications.

TRUNKED TONE REMOTE CONTROL MODULE

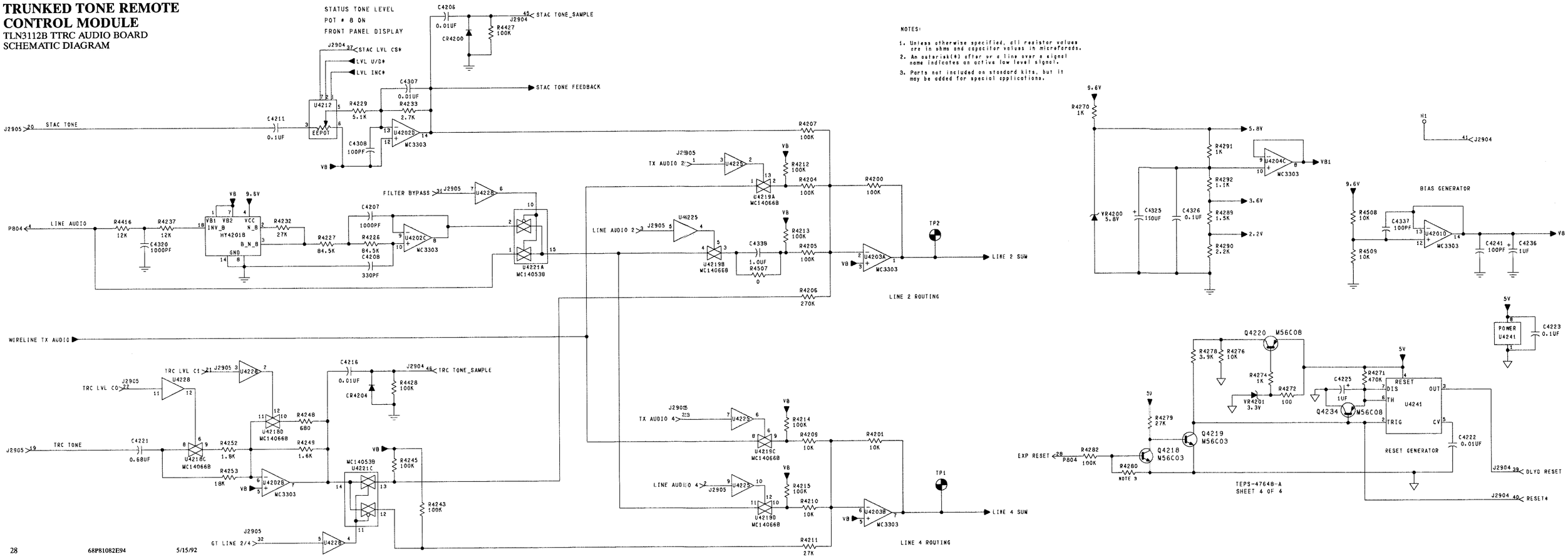
TLN3112B TTRC AUDIO BOARD SCHEMATIC DIAGRAM



TEPS-47648
SHEET 3 OF 4

TRUNKED TONE REMOTE CONTROL MODULE

TLN3112B TTRC AUDIO BOARD
SCHEMATIC DIAGRAM

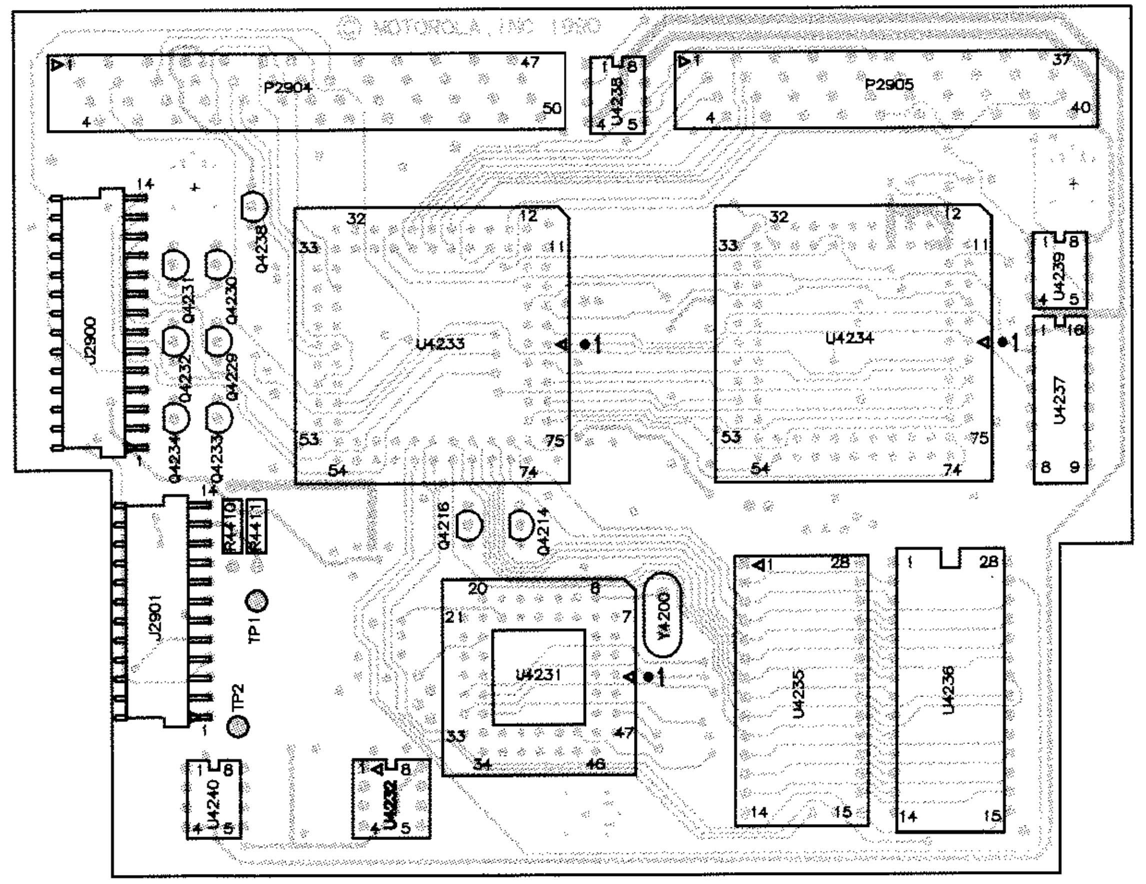


NOTES:

1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but it may be added for special applications.

TRUNKED TONE REMOTE CONTROL MODULE

TLN3114B TTRC LOGIC BOARD CIRCUIT BOARD DETAILS



SHOWN FROM COMPONENT SIDE

BD - TEPS - 47402-A

OL - TEPS - 47403-A

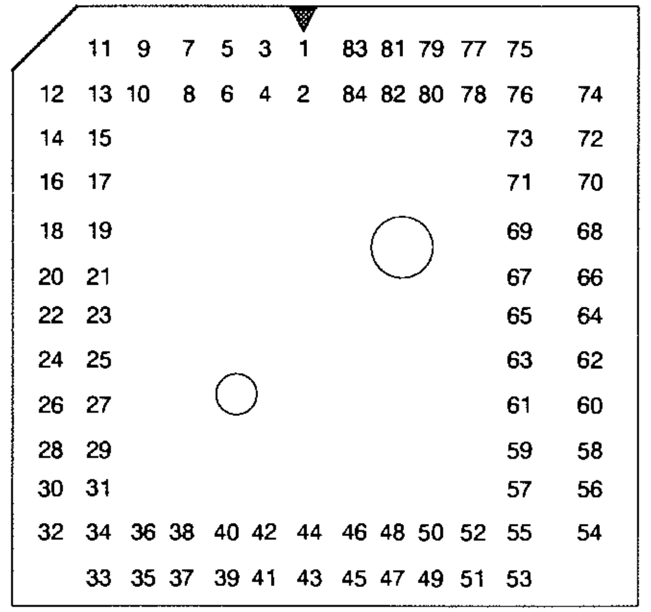
NOTE: AN ASTERISK(*) AFTER OR A LINE OVER A SIGNAL NAME INDICATES AN ACTIVE LOW LEVEL SIGNAL

PIN OUT FOR 50 PIN CABLE (P2904)

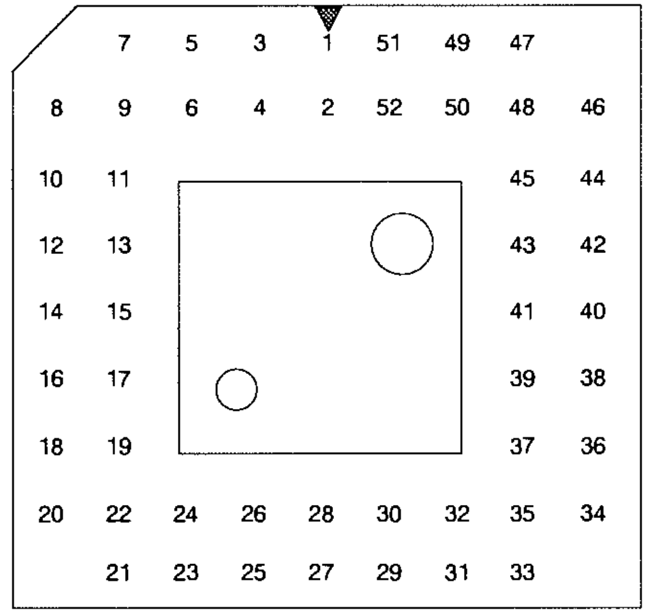
1	A+
2	BOARD GND (STATIC/AUDIO)
3	+9.6V
4	TKG RX AUDIO
5	LOGIC GND
6	HSR DATA IN
7	LOGIC GND
8	HSR DATA OUT
9	LOGIC GND
10	HSR CLOCK
11	LOGIC GND
12	HSR SYNCH
13	BD3*
14	BD2*
15	BD1*
16	BD0*
17	BA3
18	BA2
19	BA1
20	BA0
21	DATA STROBE
22	IPCB
23	MUTE
24	A+
25	+5V
26	+5V
27	GEN TX DATA(+)
28	GEN TX DATA(-)
29	TX DATA(+)
30	TX DATA(-)
31	LVL INC*
32	LINE 4 LVL CS*
33	LINE 2 LVL CS*
34	DATA DEV CS*
35	LOW EQUAL CS*
36	HIGH EQUAL CS*
37	STAC LVL CS*
38	TX LVL ADJ CS*
39	DLYD RESET
40	RESET*
41	SPARE(HI)
42	TKG DATA_SAMPLE
43	LINE 4_SAMPLE
44	LINE 2_SAMPLE
45	STAC TONE_SAMPLE
46	TRC TONE_SAMPLE
47	CURRENT(-)
48	CURRENT(+)
49	ALC_SAMPLE
50	BOARD GND(STATIC & AUDIO)

PIN OUT FOR 40 PIN CABLE (P2905)

1	TX AUDIO 2
2	LINE AUDIO 4
3	LINE AUDIO 2
4	LINE 1/3*
5	LIMIT GAIN*
6	FAILSOFT LT
7	TRC ENCODE LT
8	LINE PTT LT
9	FAIL LT
10	FAILSOFT TONE
11	FAILSOFT CODEWORD
12	INTERCOM
13	DECODE AUDIO
14	LOOP BACK
15	TX SOURCE
16	TKG AUDIO MUTE
17	LINE MUTE 4
18	LINE MUTE 2
19	TRC TONE
20	STAC TONE
21	TRC LVL C1
22	TRC LVL C0
23	TX AUDIO 4
24	LPTT
25	TX LVL C1
26	TX LVL C0
27	LVL U/D*
28	GT/FT*
29	CCI ENABLE
30	CT ENABLE
31	FILTER BYPASS
32	GT LINE 2/4
33	GAIN UP HOLD
34	DATA/FLSFT*
35	EQUAL LINE 2
36	FILTER CLK
37	ALC RESET*
38	GAIN DOWN HOLD
39	REVBURST
40	ACTIVITY*



ASIC SOCKET DETAIL

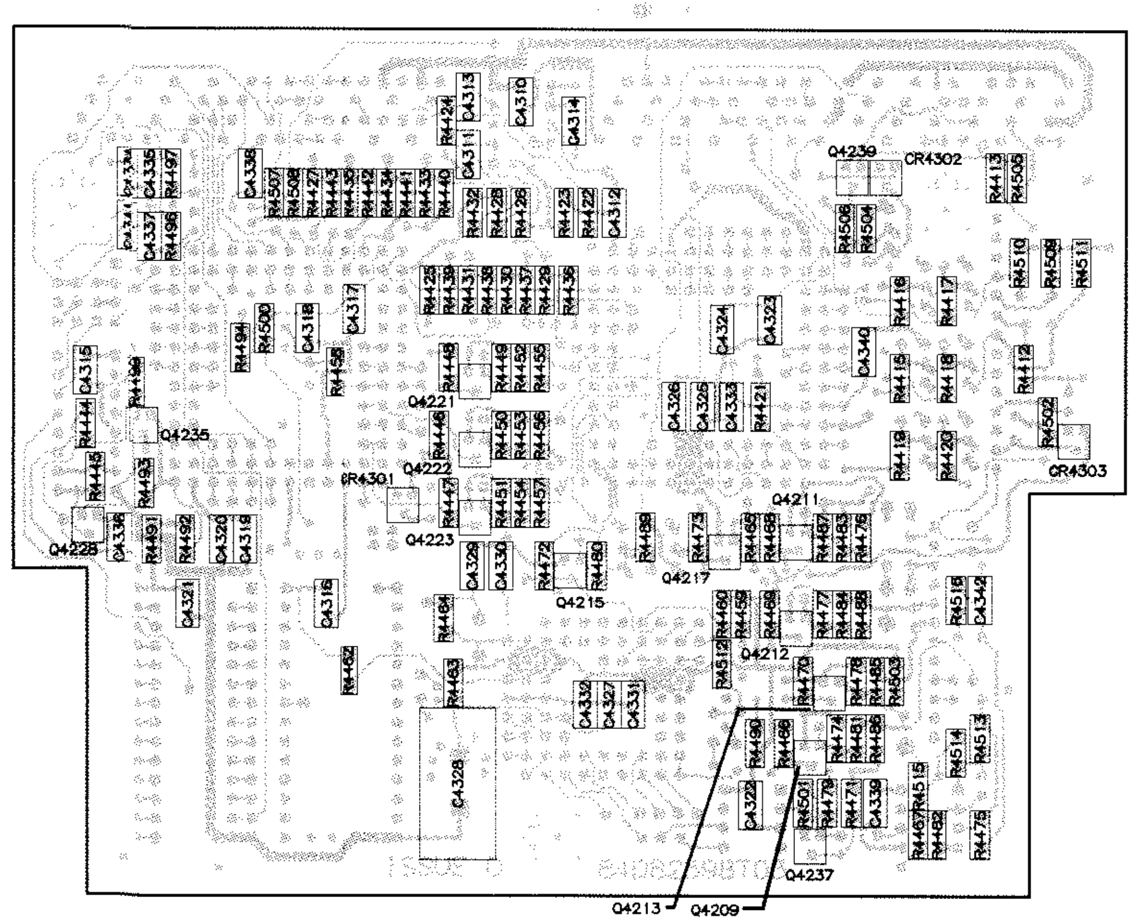


µP SOCKET DETAIL

TRANSISTOR DETAILS
(TOP VIEW)

4811043C05
4811043C20

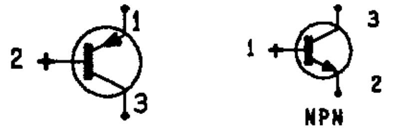
1 -EMITTER
2 -BASE
3 -COLLECTOR



SHOWN FROM SOLDER SIDE

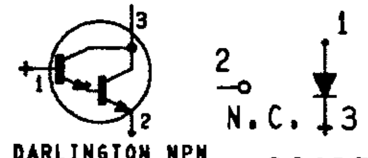
BD - TEPS - 47404-A

OL - TEPS - 47405-A



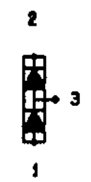
PNP
481105A08
481105B08
481105C08

NPN
4811056A03
4811056B03
4811056C03
4811056C21

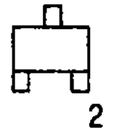


DARLINGTON NPN
4811056A23
4811056B23
4811056C23

DIODE
4811058A11
4811058B11
4811058C11
4805129M41
4811058A04
4811058B04
4811058C04



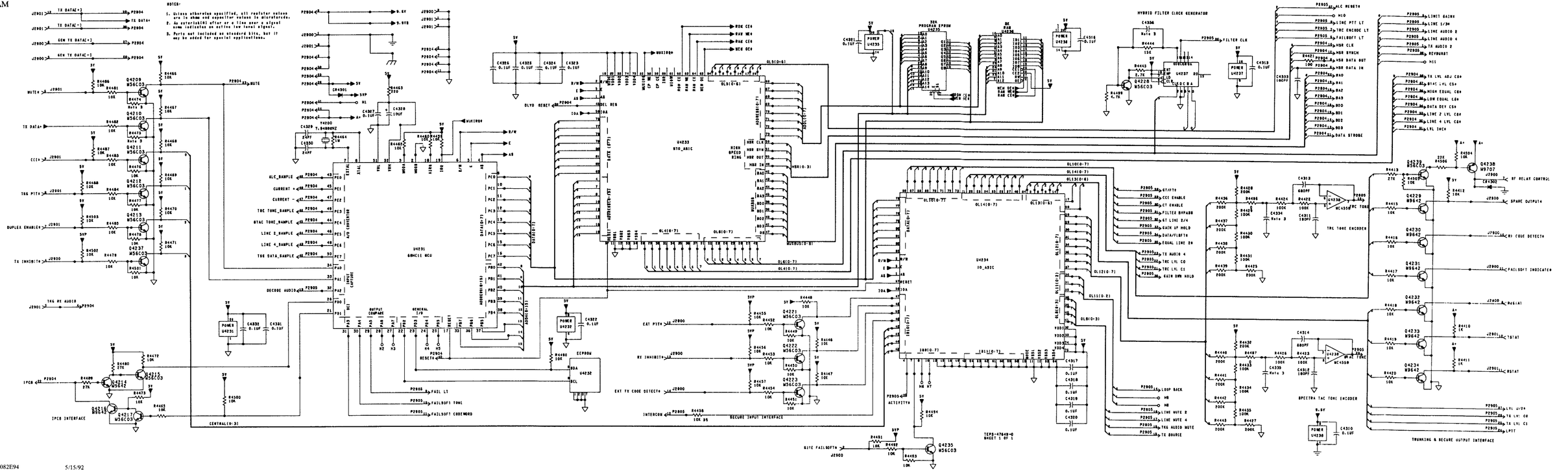
DUAL DIODE
4884336R03



STANDARD SOT PACKAGE PIN-OUT

TRUNKED TONE REMOTE CONTROL MODULE

TLN3114B TTRC LOGIC BOARD
SCHEMATIC DIAGRAM



Parts Lists

TRN7272A TTRC Logic Board PL-11943-O

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		capacitor, fixed:
C4310	2113741B69	0.1 uF, ±5%; 50V
C4311, C4312	2113740B55	180 pF, ±5%; 50V
C4313, C4314	2113740B69	680 pF, ±5%; 50V
C4315 thru C4327	2113741B69	0.1 uF, ±5%; 50V
C4328	2311049A19	10 uF, ±10%; 25V
C4329, C4330	2113740B34	24 pF, ±5%; 50V
C4331, C4332	2113741B69	0.1 uF, ±5%; 50V
C4333	2113740B49	100 pF, ±5%; 50V
C4334, C4335	2113740B59	270 pF, ±5%; 50V
C4336	2113741B69	0.1 uF, ±5%; 50V
C4337, C4338	2113740B71	820 pF, ±5%; 50V
C4339	2113741B69	0.1 uF, ±5%; 50V
C4340	2113740B59	270 pF, ±5%; 50V
C4341, C4342	2113741B69	0.1 uF, ±5%; 50V
		diode: (see note)
CR4301 thru CR4303	4811058A11	silicon
		connector:
J2900	2882041P09	plug: 14-contact
J2901	2882041P08	plug: 12-contact
		connector:
P2904	- -	p/o CABLE ASSEMBLY 3083139N26
P2905	- -	p/o CABLE ASSEMBLY 3083139N25
		transistor: (see note)
Q4209	4811056A03	NPN
Q4211 thru Q4213	4811056A03	NPN
Q4214	4800869642	NPN
Q4215	4811056A03	NPN
Q4216	4800869642	NPN
Q4217	4811056A03	NPN
Q4221 thru Q4223	4811056A03	NPN
Q4228	4811056A03	NPN
Q4229 thru Q4234	4800869642	NPN
Q4235	4811056A03	NPN
Q4237	4811056A03	NPN
Q4238	4800869707	PNP
Q4239	4811056A03	NPN
		resistor, fixed:
R4410, R4411	0611009A49	1K, ±5%; 1/4W
R4412	0611077A98	10K, ±5%; 1/8W
R4413	0611077B09	27K, ±5%; 1/8W
R4415 thru R4420	0611077A98	10K, ±5%; 1/8W
R4421	0611077A50	100 ohms, ±5%; 1/8W
R4422 thru R4424	0611077G88	100K, ±1%; 1/8W

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		resistor, fixed: (cont.)
R4425	0611077H18	200K, ±1%; 1/8W
R4426	0611077G88	100K, ±1%; 1/8W
R4427, R4428	0611077H18	200K, ±1%; 1/8W
R4429 thru R4431	0611077G88	100K, ±1%; 1/8W
R4432	0611077H18	200K, ±1%; 1/8W
R4433 thru R4435	0611077G88	100K, ±1%; 1/8W
R4436 thru R4443	0611077H18	200K, ±1%; 1/8W
R4444	0611077B03	15K, ±5%; 1/8W
R4445	0611077A84	2.7K, ±5%; 1/8W
R4446 thru R4460	0611077A98	10K, ±5%; 1/8W
R4462	0611077A98	10K, ±5%; 1/8W
R4463	0611077A58	220 ohms, ±5%; 1/8W
R4464	0611077B47	1 meg, ±5%; 1/8W
R4465, R4466	0611077A98	10K, ±5%; 1/8W
R4467	0611077B19	68K, ±5%; 1/8W
R4468 thru R4473	0611077A98	10K, ±5%; 1/8W
R4475	0611077A69	620 ohms, ±5%; 1/8W
R4476 thru R4479	0611077A98	10K, ±5%; 1/8W
R4480	0611077B09	27K, ±5%; 1/8W
R4481	0611077A98	10K, ±5%; 1/8W
R4482	0611077A69	620 ohms, ±5%; 1/8W
R4483 thru R4488	0611077A98	10K, ±5%; 1/8W
R4489	0611077B09	27K, ±5%; 1/8W
R4490 thru R4494	0611077A98	10K, ±5%; 1/8W
R4496, R4497	0611077G88	100K, ±1%; 1/8W
R4499	0611077A90	4.7K, ±5%; 1/8W
R4500 thru R4505	0611077A98	10K, ±5%; 1/8W
R4506	0611077B07	22K, ±5%; 1/8W
R4507, R4508	0611077G88	100K, ±1%; 1/8W
R4509 thru R4512	0611077A98	10K, ±5%; 1/8W
R4513	0611077B47	1 meg, ±5%; 1/8W
R4514	0611077A98	10K, ±5%; 1/8W
R4515	0611077B01	12K, ±5%; 1/8W
R4516	0611077A98	10K, ±5%; 1/8W
		integrated circuit: (see note)
U4231	5113802A01	A/D w/Switch Control Interface
U4233, U4234	5184494R03	ASIC Station Control
U4236	5184064F76	Static 32Kx8 Bit RAM
U4237	5103386A02	4-Bit Binary Counter w/clear
U4238 thru U4240	5184621K89	Dual Operational Amplifier
		crystal: (see note)
Y800	4880113K04	7.948 MHZ

TRN7272A TTRC Logic Board (Continued) PL-11943-O

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		non-referenced items:
	0982449T01	SOCKET, IC: 52-contact (used with U4231)
	0982449T03	SOCKET, IC: 84-contact (2 used with U4233 & U234)
	0982808R02	SOCKET, IC: 8-contact (used with U4232)
	0982808R10	SOCKET, IC: 28-contact (used with U4235)
	3083139N25	CABLE ASSEMBLY, flat, 40-conductor: includes connector P2905
	3083139N26	CABLE ASSEMBLY, flat, 50-conductor: includes connector P2904
	4380054K01	SPACER, pcb support (3 used)
	5483865R01	LABEL, bar code: 1/4" wide, white
	5484960T01	LABEL, bar code: 6.3 x 12.7MM, white
	7505295B01	PAD, crystal (used with Y800)

NOTE: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part number.

TFN6056A 2175 Hz Notch Filter PL-11272-A

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		integrated circuit:
U1	5183110T01	Dual Switched Capacitor Active Filter
U2	5113817A11	Operational Amplifier
		non-referenced item:
	2984209P01	TERMINAL, contact: 7.2MM lg (20 used)

NOTE: This hybrid filter is not repairable. If defective, the entire unit must be replaced.

TFN6061A 2175 Hz Bandpass Filter PL-11273-A

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		integrated circuit:
U1	5183110T01	Dual Switched Capacitor Active Filter
		non-referenced item:
	2984209P01	TERMINAL, contact: 7.2MM lg (20 used)

NOTE: This hybrid filter is not repairable. If defective, the entire unit must be replaced.

TVN6056A TTRC Software PL-11221-A

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		integrated circuit: (see note)
U4235	5191012C30	64K x 8 Bit EPROM

NOTE: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part number.

TRN7273A TTRC Audio Board PL-11944-O

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		capacitor, fixed:
C4200	2113741B37	4700 pF, ±5%; 50V
C4201	2113741B69	0.1 uF, ±5%; 50V
C4202	2311049A21	22 uF, ±10%; 20V
C4203	2113741B69	0.1 uF, ±5%; 50V
C4204	0811051A20	0.018 uF, ±5%; 1V
C4205	2113740B49	100 pF, ±5%; 50V
C4206	2113741B45	0.01 uF, ±5%; 50V
C4207	2113740B73	1000 pF, ±5%; 50V
C4208	2113740B61	330 pF, ±5%; 50V
C4210	2113740B73	1000 pF, ±5%; 50V
C4211	2113741B69	0.1 uF, ±5%; 50V
C4213	2113740B61	330 pF, ±5%; 50V
C4214	2113740B73	1000 pF, ±5%; 50V
C4216	2113741B45	0.01 uF, ±5%; 50V
C4217	0811051A15	0.22 uF, ±5%; 63V
C4218	2113740B49	100 pF, ±5%; 50V
C4219	0811051A23	0.056 uF, ±5%; 1V
C4220	2311054H04	4.7 uF, ±10%; 25V
C4221	0811051A18	0.68 uF, ±5%; 63V
C4222	2113741B45	0.01 uF, ±5%; 50V
C4223, C4224	2113741B69	0.1 uF, ±5%; 50V
C4225	2311049A08	1 uF, ±10%; 35V
C4226	2113741B69	0.1 uF, ±5%; 50V
C4228 thru C4230	2113741B69	0.1 uF, ±5%; 50V
C4231	0811051A18	0.68 uF, ±5%; 63V
C4232	2113740B49	100 pF, ±5%; 50V
C4233	0811051A18	0.68 uF, ±5%; 63V
C4235	2113741B69	0.1 uF, ±5%; 50V
C4236	2311049A08	1 uF, ±10%; 35V
C4237	2113741B69	0.1 uF, ±5%; 50V
C4238, C4239	2382028P07	4.7 uF, ±20%; 200V
C4240	2113741B69	0.1 uF, ±5%; 50V
C4241	2113740B49	100 pF, ±5%; 50V
C4243	2113740B49	100 pF, ±5%; 50V
C4250, C4251	2382028P07	4.7 uF, ±20%; 200V
C4252	2113740B73	1000 pF, ±5%; 50V
C4253	0811051A15	0.22 uF, ±5%; 63V
C4254 thru C4257	2113740B49	100 pF, ±5%; 50V
C4258, C4259	2113741B45	0.01 uF, ±5%; 50V
C4260, C4261	2311049A08	1 uF, ±10%; 35V
C4262	2113741B69	0.1 uF, ±5%; 50V
C4263 thru C4265	2113741B45	0.01 uF, ±5%; 50V
C4266, C4267	2113741B69	0.1 uF, ±5%; 50V
C4268	2113740B60	300 pF, ±5%; 50V
C4269	2113741B45	0.01 uF, ±5%; 50V
C4270	2113740B76	1500 pF, ±5 pF; 50V
C4272	2113740B67	560 pF, ±5%; 50V
C4273	2113740B73	1000 pF, ±5%; 50V
C4274	2113741B69	0.1 uF, ±5%; 50V
C4275	2113740B64	430 pF, ±5%; 50V
C4276	2113740B49	100 pF, ±5%; 50V
C4277	2113741B69	0.1 uF, ±5%; 50V
C4278	2113740B74	1200 pF, ±5%; 50V
C4279	2113740B73	1000 pF, ±5%; 50V
C4280	2113741B57	0.033 uF, ±5%; 50V
C4281 thru C4283	2113741B69	0.1 uF, ±5%; 50V

TRN7273A TTRC Audio Board (Continued) PL-11944-O

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		capacitor, fixed: (cont.)
C4285	2113741B69	0.1 uF, ±5%; 50V
C4287	2113741B69	0.1 uF, ±5%; 50V
C4290, C4291	2113741B69	0.1 uF, ±5%; 50V
C4292, C4293	2313748G13	22 uF, ±20%; 25V
C4294	2113741B69	0.1 uF, ±5%; 50V
C4298	2113740B49	100 pF, ±5%; 50V
C4300, C4301	2113741B69	0.1 uF, ±5%; 50V
C4302	2311049A19	10 uF, ±10%; 25V
C4303	2313748G22	100 uF, ±20%; 25V
C4305	2113740B65	470 pF, ±5%; 50V
C4306	2113740B59	270 pF, ±5%; 50V
C4307	2113741B45	0.01 uF, ±5%; 50V
C4308, C4309	2113740B49	100 pF, ±5%; 50V
C4310	2113740B61	330 pF, ±5%; 50V
C4311	2113741B57	0.033 uF, ±5%; 50V
C4312, C4313	2113740B73	1000 pF, ±5%; 50V
C4314	2113741B69	0.1 uF, ±5%; 50V
C4315	2113740B49	100 pF, ±5%; 50V
C4316	2113740B61	330 pF, ±5%; 50V
C4317	2113740B49	100 pF, ±5%; 50V
C4318	2113740B61	330 pF, ±5%; 50V
C4319, C4320	2113740B73	1000 pF, ±5%; 50V
C4321	2113741B45	0.01 uF, ±5%; 50V
C4325	2313748G22	100 uF, ±20%; 25V
C4326 thru C4331	2113741B69	0.1 uF, ±5%; 50V
C4332	2311054A09	47 uF, ±20%; 6V
C4333	2113741B69	0.1 uF, ±5%; 50V
C4335, C4336	2311049A08	1 uF, ±10%; 35V
C4337	2113740B49	100 pF, ±5%; 50V
C4338	0811051A19	1 uF, +5%/-0.5%; 63V
C4339 thru C4341	2113741B69	0.1 uF, ±5%; 50V
		diode: (see note)
CR4200	4805129M41	silicon
CR4204, CR4205	4805129M41	silicon
CR4252 thru CR4255	4882022N05	Unidirectional Transient Voltage Suppressor
CR4256, CR4257	4805129M41	silicon
CR4262	4805129M41	silicon
CR4284, CR4285	4805129M41	silicon
CR4291, CR4292	4811058A11	silicon
CR4293 thru CR4296	4882466H18	silicon
CR4297, CR4298	4805129M41	silicon
		light emitting diode: (see note)
DS4200	4888245C24	red
DS4201 thru DS4203	4888245C23	yellow
		connector:
J900, J901	0984206N01	receptacle: 6-contact
J2904	2883290P11	plug; 50-contact
J2905	2883290P06	plug: 40-contact

TRN7273A TTRC Audio Board (Continued) PL-11944-O

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		jumper, connector:
JU4200, JU4201	2880002R03	plug: 3-contact
JU4203 thru JU4205	2880002R03	plug: 3-contact
JU4208, JU4209	2880002R03	plug: 3-contact
JU4211 thru JU4214	2880002R03	plug: 3-contact
JU4217, JU4218	2880002R03	plug: 3-contact
JU4222	2880002R03	plug: 3-contact
JU4226, JU4227	2880002R03	plug: 3-contact
JU4370, JU4371	2880002R03	plug: 3-contact
		connector:
P804	- -	p/o CABLE ASSEMBLY 3083139N22
		transistor: (see note)
Q4200	4811056A08	PNP
Q4201	4800869653	type JFET
Q4202	4811056A03	NPN
Q4205 thru Q4208	4800869787	NPN
Q4218, Q4219	4811056A03	NPN
Q4220	4811056A08	PNP
Q4224 thru Q4226	4811056A03	NPN
Q4230	4800869653	type JFET
Q4231	4811056A03	NPN
Q4234 thru Q4237	4811056A08	PNP
Q4238, Q4239	4811056A03	NPN
		resistor, fixed:
R4200	0611077B23	100K, ±5%; 1/8W
R4201, R4202	0611077A98	10K, ±5%; 1/8W
R4203	0611077A90	4.7K, ±5%; 1/8W
R4204, R4205	0611077B23	100K, ±5%; 1/8W
R4206	0611077B33	270K, ±5%; 1/8W
R4207	0611077B23	100K, ±5%; 1/8W
R4209, R4210	0611077A98	10K, ±5%; 1/8W
R4211	0611077B09	27K, ±5%; 1/8W
R4212 thru R4215	0611077B23	100K, ±5%; 1/8W
R4216	0611077A98	10K, ±5%; 1/8W
R4217	0611077B29	180K, ±5%; 1/8W
R4218	0611077A86	3.3K, ±5%; 1/8W
R4219	0611077B04	16K, ±5%; 1/8W
R4220	0611077B29	180K, ±5%; 1/8W
R4221	0611077B01	12K, ±5%; 1/8W
R4222	0611077A88	3.9K, ±5%; 1/8W
R4223	0611077A92	5.6K, ±5%; 1/8W
R4226, R4227	0611077G81	84.5K, ±1%; 1/8W
R4228	0611077A01	0 ohm, ±5%; 0W
R4229	0611077A91	5.1K, ±5%; 1/8W
R4230	0611077B39	470K, ±5%; 1/8W
R4231, R4232	0611077B09	27K, ±5%; 1/8W
R4233	0611077A84	2.7K, ±5%; 1/8W

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		resistor, fixed: (cont.)
R4234	0611077B15	47K, ±5%; 1/8W
R4237	0611077B01	12K, ±5%; 1/8W
R4238	0611077B29	180K, ±5%; 1/8W
R4239	0611077G81	84.5K, ±1%; 1/8W
R4242	0611077G81	84.5K, ±1%; 1/8W
R4243	0611077B23	100K, ±5%; 1/8W
R4244	0611077B33	270K, ±5%; 1/8W
R4245	0611077B23	100K, ±5%; 1/8W
R4246	0611077B09	27K, ±5%; 1/8W
R4247	0611077B01	12K, ±5%; 1/8W
R4248	0611077A70	680 ohms, ±5%; 1/8W
R4249	0611077A79	1.6K, ±5%; 1/8W
R4250	0611077B31	220K, ±5%; 1/8W
R4251	0611077B01	12K, ±5%; 1/8W
R4252	0611077A80	1.8K, ±5%; 1/8W
R4253	0611077B05	18K, ±5%; 1/8W
R4254	0611077A91	5.1K, ±5%; 1/8W
R4255, R4256	0611077B23	100K, ±5%; 1/8W
R4257	0611077A98	10K, ±5%; 1/8W
R4258	0611077B04	16K, ±5%; 1/8W
R4260	0611077B21	82K, ±5%; 1/8W
R4261	0611077A79	1.6K, ±5%; 1/8W
R4262	0611077B01	12K, ±5%; 1/8W
R4263	0611077B09	27K, ±5%; 1/8W
R4264	0611077B15	47K, ±5%; 1/8W
R4265	0611077A88	3.9K, ±5%; 1/8W
R4266	0611077A56	180 ohms, ±5%; 1/8W
R4267	0611077A74	1K, ±5%; 1/8W
R4268	0611077A80	1.8K, ±5%; 1/8W
R4269	0611077B07	22K, ±5%; 1/8W
R4270	0611077A74	1K, ±5%; 1/8W
R4271	0611077B39	470K, ±5%; 1/8W
R4272	0611077A50	100 ohms, ±5%; 1/8W
R4273	0611077B15	47K, ±5%; 1/8W
R4274	0611077A74	1K, ±5%; 1/8W
R4275	0611077B15	47K, ±5%; 1/8W
R4276	0611077A98	10K, ±5%; 1/8W
R4277	0611077B09	27K, ±5%; 1/8W
R4278	0611077A88	3.9K, ±5%; 1/8W
R4279, R4280	0611077B09	27K, ±5%; 1/8W
R4281	0611077B15	47K, ±5%; 1/8W
R4282	0611077B19	68K, ±5%; 1/8W
R4283	0611077B15	47K, ±5%; 1/8W
R4285, R4286	0611077A80	1.8K, ±5%; 1/8W
R4287, R4288	0611077A76	1.2K, ±5%; 1/8W
R4289	0611077A78	1.5K, ±5%; 1/8W
R4290	0611077A82	2.2K, ±5%; 1/8W
R4291	0611077A74	1K, ±5%; 1/8W
R4292	0611077A75	1.1K, ±5%; 1/8W
R4300	0611077A90	4.7K, ±5%; 1/8W
R4301, R4302	0611077A80	1.8K, ±5%; 1/8W
R4303	0611077A88	3.9K, ±5%; 1/8W
R4304, R4305	0611077A76	1.2K, ±5%; 1/8W
R4306	0611077A86	3.3K, ±5%; 1/8W
R4307 thru R4310	0611077A50	100 ohms, ±5%; 1/8W
R4311 thru R4314	0611077A90	4.7K, ±5%; 1/8W
R4315 thru R4320	0611077B29	180K, ±5%; 1/8W

TRN7273A TTRC Audio Board (Continued) PL-11944-O

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		resistor, fixed: (cont.)
R4321, R4322	0611077A91	5.1K, ±5%; 1/8W
R4324, R4325	0611077B07	22K, ±5%; 1/8W
R4327, R4328	0611077A98	10K, ±5%; 1/8W
R4329	0611077B04	16K, ±5%; 1/8W
R4330	0611077A98	10K, ±5%; 1/8W
R4332	0611077A76	1.2K, ±5%; 1/8W
R4333	0611077B05	18K, ±5%; 1/8W
R4334	0611077A78	1.5K, ±5%; 1/8W
R4335	0611077A88	3.9K, ±5%; 1/8W
R4336	0611077B11	33K, ±5%; 1/8W
R4337	0611077A98	10K, ±5%; 1/8W
R4338	0611077B03	15K, ±5%; 1/8W
R4339	0611077B16	51K, ±5%; 1/8W
R4340	0611077B18	62K, ±5%; 1/8W
R4341	0611077B16	51K, ±5%; 1/8W
R4342	0611077A95	7.5K, ±5%; 1/8W
R4343	0611077B31	220K, ±5%; 1/8W
R4344, R4345	0611077B16	51K, ±5%; 1/8W
R4346	0611077B26	130K, ±5%; 1/8W
R4347	0611077B28	160K, ±5%; 1/8W
R4348	0611077B16	51K, ±5%; 1/8W
R4349	0611077B23	100K, ±5%; 1/8W
R4350	0611077B09	27K, ±5%; 1/8W
R4351, R4352	0611077B16	51K, ±5%; 1/8W
R4353	0611077A94	6.8K, ±5%; 1/8W
R4354 thru R4356	0611077A98	10K, ±5%; 1/8W
R4358	0611077A98	10K, ±5%; 1/8W
R4362	0611077B16	51K, ±5%; 1/8W
R4365, R4366	0611077B11	33K, ±5%; 1/8W
R4367	0611077B16	51K, ±5%; 1/8W
R4374, R4375	0611077B16	51K, ±5%; 1/8W
R4380	0611077A69	620 ohms, ±5%; 1/8W
R4381	0611009B23	0 ohm, ±5%; 1/4W
R4390	0611077A82	2.2K, ±5%; 1/8W
R4391 thru R4393	0611077A56	180 ohms, ±5%; 1/8W
R4394 thru R4397	0611077A91	5.1K, ±5%; 1/8W
R4398	0611077B05	18K, ±5%; 1/8W
R4399, R4400	0611077B15	47K, ±5%; 1/8W
R4401	0611009A41	470 ohms, ±5%; 1/4W
R4405	0611077B15	47K, ±5%; 1/8W
R4406 thru R4409	0611077A98	10K, ±5%; 1/8W
R4411	0611077A86	3.3K, ±5%; 1/8W
R4412	0611077B01	12K, ±5%; 1/8W
R4413	0611077A86	3.3K, ±5%; 1/8W
R4414	0611077A92	5.6K, ±5%; 1/8W
R4415, R4416	0611077B01	12K, ±5%; 1/8W
R4417	0611077B47	1 meg, ±5%; 1/8W
R4418	0611077B05	18K, ±5%; 1/8W
R4420	0611077B23	100K, ±5%; 1/8W
R4424	0611077B03	15K, ±5%; 1/8W
R4427, R4428	0611077B23	100K, ±5%; 1/8W
R4429	0611077B04	16K, ±5%; 1/8W
R4432 thru R4434	0611077B23	100K, ±5%; 1/8W
R4435	0611077B07	22K, ±5%; 1/8W
R4436	0611077A76	1.2K, ±5%; 1/8W

TRN7273A TTRC Audio Board (Continued) PL-11944-O

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		resistor, fixed: (cont.)
R4437	0611077B23	100K, ±5%; 1/8W
R4438	0611077B19	68K, ±5%; 1/8W
R4439	0611077A82	2.2K, ±5%; 1/8W
R4440	0611077B19	68K, ±5%; 1/8W
R4441	0611077A54	150 ohms, ±5%; 1/8W
R4442	0611077B05	18K, ±5%; 1/8W
R4443, R4444	0611077B23	100K, ±5%; 1/8W
R4446	0611077B09	27K, ±5%; 1/8W
R4447, R4448	0611077A98	10K, ±5%; 1/8W
R4449	0611077B15	47K, ±5%; 1/8W
R4450	0611077A78	1.5K, ±5%; 1/8W
R4451	0611077A70	680 ohms, ±5%; 1/8W
R4452, R4453	0611077A98	10K, ±5%; 1/8W
R4454	0611077A78	1.5K, ±5%; 1/8W
R4495	0611077B07	22K, ±5%; 1/8W
R4500	0611077B23	100K, ±5%; 1/8W
R4502	0611077B23	100K, ±5%; 1/8W
R4504	0611077A91	5.1K, ±5%; 1/8W
R4505	0611077A68	560 ohms, ±5%; 1/8W
R4507	0611077A01	0 ohm, ±5%; 0W
R4508, R4509	0611077A98	10K, ±5%; 1/8W
		switch:
S4200	4083980R08	toggle: spdt
		transformer:
T4201	2584202A02	Audio Frequency
T4202	2583036L01	Audio Frequency
T4203	2584202A02	Audio Frequency
T4204	2583036L01	Audio Frequency
		integrated cirucit: (see note)
U4200 thru U4207	5113819D04	Quad Differential-Input Operational Amplifier
U4208	5184621K89	Dual Operational Amplifier
U4209, U4210	5113819D04	Quad Differential-Input Operational Amplifier
U4211 thru U4217	5182802R24	Digitally Controlled 50K Potentiometer
U4218, U4219	5184887K73	Quad Bilateral Switch
U4220 thru U4224	5184887K60	Triple 2-Channel Analog Mux/Demux
U4225 thru U4228	5184704M19	Shift Hex Level Log Level Control
U4230 thru U4233	5184621K34	Optical Isolator
U4234	5184887K52	Hex Schmitt Trigger
U4241	5184320A35	Timer
U4242	5184887K73	Quad Bilateral Switch
		voltage regulator: (see note)
VR4200	4882256C61	Zener 5.8V
VR4201	4882256C26	Zener 3.3V
VR4214 VR4215	4882256C03	Zener 4.7V
VR4216	4882256C56	Zener 8.8V
VR4217	4882256C61	Zener 5.8V

TRN7273A TTRC Audio Board (Continued) PL-11944-O

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		non-referenced items:
	TFN6056A	2175 Hz Notch Filter
	TFN6061A	2175 Hz Bandpass Filter
	0984181L01	SHORTING JUMPER: 2-contact (18 used with JU4200,4201,4203 thru 4205,4208,4209,4211 thru 4214,4217,4218,4222,4226, 4227,4370,4371)
	3083139N22	CABLE ASSEMBLY, flat, 34-conductor: includes connector P804
	4380054K02	SPACER, support (3 used)
	5483865R01	LABEL, bar code: 1/4" wide, white
	5484960T01	LABEL, bar code: 6.3x12.7MM, white

NOTE: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part number.

MOTOROLA INC.

OPTION C514
TRANSPARENT OPERATION
MODEL TLN3045C SECURE MODULE

1. FUNCTIONAL DESCRIPTION

This document describes the operation of the TLN3045C Secure Module. The module consists of a TRN9999C Secure Board and a TVN6057A Secure EEPROM. The secure module is designed to interface directly with the TLN3189 and TLN3204 series of Secure Capable Station Control Modules (SSCB), for use in *MSF 5000* and *MSF 10000* Digital Control Stations. The secure board is mounted into the station as a stand-off daughter board to the station control board. Table 1 lists the Secure Hybrid options available for the secure board.

Table 1. Secure Hybrid Options

Option	Description
C331	Secure Encryption
C388	DES Encryption
C794	DVPE Encryption
C795	DES-XL Encryption
C797	DVP-XLE Encryption

The secure board has two basic modes of operation. The first is the transparent mode, in which secure code is simply passed through the station. In this mode, the secure board monitors the receiver and the wireline signals until valid secure code (12 kBit/Sec data) is detected, generating an Rx or Tx Code Detect. During a code detect, audio paths on the station control board are switched so that the secure data is routed through the secure board for reclocking, buffering, and filtering; before being transmitted and/or sent down the wireline. A Console Interface Unit (CIU) can be interfaced to the station via the wireline to provide the encrypt/decrypt capability.

The second mode of operation is the encrypt/decrypt mode. When one of the secure hybrid options is specified, the secure board operates in this mode, which provides encryption and decryption of audio signals in either half or full duplex. For transmission, audio is analog to digital (A-to-D) converted into a 12 kBit/Sec digital bit stream, and then encrypted. The resultant bit stream is splatter filtered and transmitted. During reception, the process is reversed. The received encrypted signal is filtered, limited, and reclocked to produce a digital bit stream. This bit stream is then decrypted to produce a digital signal, which is then D-to-A converted back into audio. The C332 Full Duplex Wireline option, in conjunction with one of the Secure Hybrid options, allows simultaneous encrypt and decrypt operation.

The encryption/decryption process is performed by one of several different hybrids, as specified by the desired encryption algorithm. Each hybrid can be loaded with a different key variable, making it different from any other hybrid. The loading process requires a Key Variable Loader (KVL), which interfaces to the secure board through two cables. The station internal TKN8597A Secure Interface cable connects between J4001 (on the secure board) and a connector on either the RF tray front panel or the station junction box. The station external TKN8531B KVL cable connects between the KVL and the station. When the board is in half duplex operation, up to eight hybrids with different key variables can be selected to perform the encrypt/decrypt function. In full duplex operation, the hybrids are combined in pairs to provide up to four different encryption/decryption keys.

2. AUDIO SECTION

2.1 TRANSMIT AUDIO CIRCUITRY DESCRIPTION

The transmit processing section is divided into two sections which provide the two different modes of station control operation; transparent operation, and transmit audio encryption. The schematic diagrams for these control modes are located on the diagram sheet titled "Secure Audio," at the end of this section.

2.1.1 Transmit Transparent Operation

2.1.1.1 CIRCUIT DESCRIPTION

The input to the transmit audio circuitry is at P803-6. The signal is RAW TX AUDIO, and consists of either audio

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or filtered data coming from the wireline. This signal is processed by a three-pole lowpass linear phase active filter, using op-amp U4002C. It is a noise filter, the purpose of which is to band-limit the line data, thus removing the high frequency noise components from the transmission channel. Left in, these could cause spurious code "detections."

The filtered signal is then limited by comparator U4019B, to transform the signal into discrete logic level data. A single pole lowpass filter is used to determine the average DC value of the input signal, and provide a bias which is used to set the comparator threshold. The frequency of the pole (which determines the cutoff frequency of the filter) may take on one of two values. A higher cutoff frequency is implemented by turning audio gate U4015A on, which puts R4081 in parallel with R4080. This cutoff frequency is used while the code detector is searching for code, while a lower cutoff frequency (U4015A turned off) is used once code has been detected. Hysteresis is provided by R4073, to make the comparator less sensitive to noise.

The data at the output of the comparator is at a 9.6 V logic level. This is changed to a 5 V logic level by transistor Q4002, and routed to pin 46 of the Application Specific Integrated Circuit (ASIC) U4007. (Refer to paragraph 5 for a description of this chip.) The ASIC contains an on-chip 12 kHz clock circuit, which phase locks to the incoming data stream by detecting data transitions and adjusting the clock phase until the falling edges of the clock pulses occur in sync with the data transitions. The clock is then used by a serial-to-parallel converter to decode the incoming serial data stream into eight bit bytes, which can be buffered and analyzed by the microprocessor to determine whether or not the data stream possesses the characteristics unique to encrypted data. The data is also checked for a Beginning-Of-Message (BOM) or an End-Of-Message (EOM) bit stream, consisting of alternating one-zero patterns which are used to signal the beginning or end of encrypted messages. Whenever valid 12 kBit/Sec transmit code, or a BOM, or an EOM is detected, the SSCB front panel **Tx CD** (transmit code detect) LED DS4002 should light.

The RAW TX AUDIO signal is continually reclocked, serial-to-parallel converted, buffered, and finally parallel-to-serial converted by the on-chip circuitry of the secure ASIC. Once valid code is detected, the serial transmit data at the output of the secure ASIC (U4007-45) is sent to the splatter filter. The splatter filter consists of a five pole linear phase lowpass switched capacitor filter, using U4019. This lowpass filter is used to band-limit the data to 6 kHz, eliminating the higher frequency noise which could otherwise cause interference on adjacent channels.

In addition to U4019, a 6 dB/octave anti-aliasing filter formed by R4008, R4027, R4001 and C4006 attenuates high frequency components above 50 kHz. This circuit also limits the peak-to-peak voltage of the data signal to 2.5 V. A two-pole lowpass filter using U4004D as its active element is used to filter out switching noise at the output of U4019, and change the DC bias of the signal from 2.5 V to 4.8 V.

The clock frequency supplied by the secure ASIC to the switched capacitor filter is nominally set to 341.3 kHz.

The output level of the splatter filter is level-adjusted by digital pot U4018 (EEPOT No. 6 on the front panel Status display) to set the coded deviation level. The secure EEPOTs are controlled directly by the SSCB, via connector P803.

The CODED MOD AUDIO output of the secure board at P803-7 is sent to the SSCB to be routed to the modulator. For 25 kHz channel spacing, secure data should have a deviation of 4 kHz $\pm$200 Hz. An internal 1 kHz square-wave generator is used to set the coded deviation level at 3.9 kHz $\pm$200 Hz. This level correlates to secure data with a 4 kHz deviation.

2.1.1.2 TROUBLESHOOTING TRANSMIT TRANSPARENT OPERATION

With valid secure code applied to P803-6, a data stream at 5 V logic level should be present at TP3. If there is no data at TP3, check the DC bias level of the incoming signal, which should be 4.8 V. Next, check the 9.6 V supply voltages at U4002 and U4019. If the foregoing does not isolate the problem, check for missing chip resistors and capacitors along the transmit data path. If data is present at TP3 and a Tx Code Detect (*DVP* SEL or TX CD DT on the MUXbus) is not being generated, refer to paragraph 5.2 for troubleshooting information.

If a Tx Code Detect is generated (Tx Coded PTT in the High Speed Ring signal), there should be a filtered data stream (eye pattern) at TP1. Refer to the HSR signal description in paragraph 5.1.2. If this is not the case, check for the presence of a 341.3 kHz clock at U4019-10 and/or missing chip components along this path.

2.1.2 Transmit Audio Encryption Operation

2.1.2.1 CIRCUIT DESCRIPTION

Audio to be encrypted and transmitted can originate from the TX AUDIO (P803-5), LOCAL AUDIO (P803-8), or INBOUND MRTI (P803-28) inputs to the secure board. The selected audio source is amplified, pre-emphasized and lowpass filtered by op-amps U4003C and U4003D, and routed to the Continuously Varying Slope Delta (CVSD) devices U4005 and U4006 to be digitized. When jumper JU4003 is in its alternate position, INBOUND MRTI audio is always summed with the selected encryption audio source.

SECURENET equipment uses a CVSD modulation technique to convert an analog waveform into a continuous stream of binary digits. In a full duplex station, U4006

is a dedicated A-to-D converter, and U4005 is a dedicated D-to-A converter. In a half duplex station, U4006 is not present, and U4005 performs both the A-to-D and D-to-A conversions, but not simultaneously. The operation of the CVSD devices is controlled by the RECEIVE_CTRL signal at U4005-12, and the TRANSMIT_CTRL signal at U4005-11. Both of these signals are active high, with 9.6 V logic levels. The audio signal is sampled and digitized into a serial 12 kBit/Sec data stream, which is then routed to pin 17 of all the encryption hybrids.

All secure hybrids operating in the transmit mode will encrypt this data stream. In half duplex operation, any one of eight hybrids can be selected to encrypt. In full duplex operation, only hybrids located in sockets HY4001A through HY4004A can be selected to encrypt. (Refer to paragraph 3 for details.) The encrypted data from pin 14 of the encryption hybrids is sent to the secure ASIC TX CIPHER signal inputs, where an on-chip 8:1 multiplexer selects the appropriate TX CIPHER signal, based on software key selection. This signal is then First-In-First-Out (FIFO) buffered, splatter filtered, level adjusted, and routed to the modulator.

Depending on the system and the type of encryption hybrids being used, a secure coded message may be preceded by a Beginning-Of-Message (BOM) bit stream and/or followed by an End-Of-Message (EOM) bit stream. The EOM and BOM bit streams consist of a variable length alternating 12 KHz bit pattern (i.e. 101010.....) which is generated by the secure board software.

2.1.2.2 TROUBLESHOOTING TRANSMIT AUDIO ENCRYPTION OPERATION

With an audio signal applied to one of the three audio inputs (P803-5, -8, or -28), verify that the station is configured to encrypt (MUXbus ENCRYPT bit is set) and verify that the proper audio gate is open. If INBOUND MRTI P803-28 is being used, jumper JU4003 should be in its alternate position. Then check the XMIT_OD output of the transmit CVSD (U4005-9 for half duplex, U4006-9 for full duplex). If a fixed 6 kHz square wave is present at this output, either the input signal level is too low or the signal path is being interrupted prior to the CVSD. A 12 kBit/Sec data output indicates that a signal is being digitized. This same signal should be present at pin 17 of each of the encryption hybrids.

Check the TX CIPHER signal output (pin 14) of the selected transmit (encryption) hybrid. If the output is not pseudo-random 12 kBit/Sec data, the hybrid has lost its key or the hybrid control lines are in the wrong state. Also, check for the same pseudo-random data output at U4007-45. If the data is not present, it is most likely that the desired encryption hybrid is not being selected by the software, or that the encryption hybrid is in the wrong socket.

2.2 RECEIVE AUDIO CIRCUITRY DESCRIPTION

The receive processing section is divided into two sections which provide the two different modes of operation; transparent operation and receive audio decryption. The schematic diagrams for these sections are located on the diagram sheet titled "Secure Audio," at the end of this section.

2.2.1 Receive Transparent Operation

2.2.1.1 CIRCUIT DESCRIPTION

The input to the receive audio circuitry is at P803-27. The signal is QUAD AUDIO and consists of the demodulated signal from the receiver, which has been buffered by the station control board and routed to the secure board equalizer filter. The equalizer filter utilizes two op-amps which form a two pole, one zero functional block, with a magnitude response which increases monotonically from DC to 6 kHz, and decreases monotonically at frequencies higher than 6 kHz, while maintaining a linear phase response. This equalizer filter is needed to compensate for attenuation of critical frequency components introduced by the station receiver.

NOTE

For special applications, the equalizer filter can by bypassed by placing jumper JU4004 in its alternate position.

The filtered signal is digitized by comparator U4019A to translate the signal into discrete logic level data. A single pole lowpass filter is used to determine the average DC value of the input signal, and provide a bias which is used to set the comparator threshold. The frequency of the pole (which determines the cutoff frequency of the filter) may take on one of two values. A higher cutoff frequency is implemented by turning audio gate U4017D on, which puts R4069 in parallel with R4068. This cutoff frequency is used while the code detector is searching for code, while a lower cutoff frequency (U4017D turned off) is used once code has been detected. Hysteresis is provided by R4060 to make the comparator less sensitive to noise.

The data at the output of the comparator is at a 9.6 V logic level. This is changed to a 5 V logic level by transistor Q4001, and then routed to pin 4 of the secure ASIC, U4007. An Rx Code Detect test (similar to the Tx Code Detect test discussed in the Transmit section) is performed on the data stream. Whenever valid 12 kBit/Sec code, or a BOM, or an EOM is detected, the SSCB front panel **Rx CD** (receive code detect) LED (DS4003) should light.

The on-chip circuitry of the secure ASIC can route the reclocked and buffered received data to the transmit splatter filter, and/or out to the wireline, depending on the station type. In a conventional base station, the received data is routed to pin 43 of secure ASIC U4007, where the data is

pulled up to a 4.8 V DC bias, attenuated, and filtered by a three pole lowpass linear phase filter using op-amp U4004A. This filter is used to band-limit the signal to 6 kHz for the wireline. When the wireline is in close proximity to other conductors, eliminating the higher frequencies with this filter reduces the potential for crosstalk.

The output of this filter is sent to the station control board via P803-4, Secure_Rx_Audio, where it is summed with other signals to be sent down the wireline. If the station is configured as a transparent repeater, the reclocked received data will be routed to the transmit path via U4007-45, as well as to the wireline.

2.2.1.2 TROUBLESHOOTING RECEIVE TRANSPARENT OPERATION

With valid secure code applied to P803-27, a 5 V data stream should be present at TP2. If there is no data at TP2, check the DC bias level of the incoming signal, which should be 4.8 V. Next, check the 9.6 V supply voltages for the op-amps and U4019. Also check for missing chip resistors and capacitors along the receive data path. If data is present at TP2, but an Rx Code Detect (R1 SQ LV on the MUXbus) is not being generated, refer to paragraph 5.2 for the troubleshooting procedure.

If an Rx Code Detect is generated, there should be a filtered data stream eye pattern present at P803-4. If there is no eye pattern, or the eye appears badly distorted, check for missing component chips along this path.

2.2.2 Receive Audio Decryption Operation

2.2.2.1 CIRCUIT DESCRIPTION

Audio to be decrypted originates at the station receiver, and enters the secure board at the QUAD AUDIO input P803-27. This signal is reclocked, buffered, and routed to pin 9 of all the secure hybrids for decryption. The recovered clock is also present at U4007-69 and -70, to clock the rest of the circuitry processing the signal. Any secure hybrid operating in the receive mode will attempt to decrypt the received signal.

In half duplex operation, any one of eight secure hybrids can be selected to decrypt. In full duplex operation, only secure hybrids located in sockets HY4001B through HY4004B can be selected to decrypt (Refer to paragraph 3 for details.) The decrypted data output from pin 15 of each of the decrypt hybrids is sent to the secure ASIC RX DATA inputs, where on-chip 8:1 multiplexers in each ASIC select the appropriate RX DATA signal based on software key selection.

The selected RX DATA signal, DECRYPT AUDIO, is sent to CVSD1 for D-to-A conversion, which reproduces the original audio signal. The D-to-A conversion is performed by U4005 for both half and full duplex operation. Decrypted data input to the CVSD is at pin 10, and recovered audio output is at pin 15. The CVSD device also performs the "proper code detect" function. This function indicates whether the coded transmission being received used the same encryption key as that stored in the secure board encryption hybrid. The output of the detector, at U4005-14, is an active high signal.

The recovered audio output is routed through an active bandpass filter utilizing op-amp U4004C, to improve audio quality and remove out-of-band quantization noise. This signal may be amplified or attenuated $\pm$10 dB by adjusting the gain stage (op-amp U4004B) with digital pot U4020 (EEPOT No. 0 on the front panel Status display). Normally, the level of the decrypted audio should be set 4 dB higher than clear audio. Finally, the signal is gated by U4016A and sent to the station control board via P803-4, where it is summed with other signals to be sent down the wireline.

2.2.2.2 TROUBLESHOOTING RECEIVE AUDIO DECRYPTION OPERATION

If an Rx Code Detect is not being generated, refer to paragraph 2.2.1.2 for troubleshooting information. The reclocked RX CIPHER signal should be present at pin 9 of every decryption hybrid. Check the RX DATA output (pin 15) of the selected receive (decryption) hybrid. If the output is not 12 kBit/Sec data, the hybrid has lost its key or the hybrid control lines are in the wrong state. Also check for the same pseudo-random data output at U4007-41. If the data is not present, the desired decryption hybrid is probably not being selected by the software, or the decryption hybrid may be installed in the wrong socket.

The recovered audio signal should be available between U4005-15 and P803-4. If the signal drops out anywhere along this path, check level adjust pot U4020 to see if it is properly adjusted, and make sure audio gate U4016A is open (U4016A-5 should be at approximately 9 V).

3. SECURE HYBRIDS

3.1 DESCRIPTION

In the encrypt/decrypt mode of operation, the secure board can support up to eight hybrids. A single hybrid can operate in either the encrypt (transmit) or decrypt (receive) mode, but not in both modes at the same time. Pins 10 and 13 of hybrids HY4001A through HY4004A are controlled in common by U4014 to configure the hybrids to either encrypt or decrypt. During full duplex operation, the "A" hybrids are configured to encrypt. These hybrids are physically located in the upper half of the hybrid sockets. The lower portions of the sockets (closest to the PC board) contain hybrids HY4001B through HY4004B. The "B" hybrids share common control lines for pins 10 and 13, which operate independently of the "A" hybrids.

The "B" hybrids are configured to decrypt during full duplex operation. Pin 10 on the hybrids is held low for encryption, and pulled high (to 5 V) for decryption. Pin 13 is normally pulled high during encryption; if pulled low while pin 10 is high, the hybrid will generate an EOM signal at pin 14, instead of encrypted data. For decryption, pin 13 is pulled low.

The secure board currently supports the following hybrids: DES, DES-XL, *DVP*, *DVP-XL*, and DVI-XL. Hybrid pin 5, common to all of the secure hybrids, controls different functions, depending on the hybrid type. It is normally held low. DES-XL, *DVP-XL*, and DVI-XL hybrids operate in the synchronous Range Extension (REX) mode when pin 5 is low, and in the asynchronous Cipher Feedback mode when pin 5 is high. The *DVP* hybrid uses pin 5 to select between Code 1 or Code 2, where Code 2 is a modified version of the encryption key (Code 1) stored in the hybrid. The DES hybrid has no internal connection to pin 5.

Hybrid selection is accomplished under software control, based on information provided by the High Speed Ring signal. (Refer to the HSR signal description in paragraph 4.1.2.) The hybrid selection originates with user definable function tones on the station wireline; or locally, via the station control front panel **Select/Set** switch, when the station is in access disable.

The current hybrid selection is displayed on the "Key" digit of the SSCB front panel display. "Key" selection, under local control from the station control front panel, selects hybrids as shown in Table 2 (refer to paragraph 4.1 for "Key" Insertion/loading information.

Table 2. Local Control Key/Hybrid Selection

Front Panel Status Display	Half Duplex Operation	Full Duplex Operation	
Key Digit	Encrypt & Decrypt	Encrypt	Decrypt
1	HY4001A	HY4001A	HY4001B
2	HY4002A	HY4002A	HY4002B
3	HY4003A	HY4003A	HY4003B
4	HY4004A	HY4004A	HY4004B
5	HY4001B	HY4001A	HY4001B
6	HY4002B	HY4002A	HY4002B
7	HY4003B	HY4003A	HY4003B
8	HY4004B	HY4004A	HY4004B

3.2 ALERT TONES

Any of six types of codeplug selectable (field re-programmable) alert tone sequences can be generated by the secure board to alert the user of conditions in an encrypt/decrypt station. Normally, all six types are enabled by the factory. All tones have a frequency of 750 Hz, but are of varying duration. These tones will be gated to the wireline and local speaker, but not over-the-air.

The 750 Hz tone is generated by the secure ASIC and routed to U4007-40. The 750 Hz square wave is level adjusted and filtered by a two pole lowpass active filter, using op-amp U4003B. The tone is passed to the station control board via P803-34, where it is summed with the outbound wireline audio signal. The six types of alert tones are as follows.

- CLEAR XMIT: If enabled, a single 87 ms beep will be encoded at the start of any clear line or local PTT. This serves as a warning to the operator that the transmission is not secure.
- CLEAR RECEIVE: If enabled, a single 87 ms beep will be encoded at the start of any clear receive activity. This serves to notify the console operator that the transmission is in the clear mode.
- CROSS-MODE: If enabled, a single 87 ms beep will be encoded at the start of any clear receive activity ONLY if the wireline mode is coded.
- KEY RESET ALERT: If enabled, the 750 Hz tone will be encoded as long as the Key Erase signal is active.
- XMIT KEY FAIL: If enabled, the 750 Hz tone is encoded with an 87 ms on/87 ms off duty cycle, if a coded Line/Local PTT occurs AND the selected hybrid has a corrupted/erased key (see NOTE). This tone sequence is only generated while the PTT is active (and the key is lost).

NOTE

A secure hybrid indicates a corrupted key by pulling its KEY line, pin 8, low whenever the PTT and Transmit (encrypt) states are active (pin 13 high and pin 10 low). The secure ASIC monitors the KEY lines to check for corrupted and/or erased keys among the hybrids. The C794 *DVP* CFB Secure Hybrid option (TRN6777B) does not provide this key fail indication.

- RCV KEY FAIL: If enabled, the 750 Hz tone is encoded with an 87 ms on by 87 ms off duty cycle, if coded receive activity occurs when the receive decryption hybrid has lost its key. The tone sequence is generated as long as these two conditions exist.

4. KEY VARIABLE LOADER OPERATION

4.1 KEY INSERTION

A Key Variable Loader (KVL) is a device used to transfer encryption keys from its own memory into other *SECURENET* equipment containing secure hybrids. A KVL will only load a hybrid of the same type as that specified on the back of the KVL unit. The station internal TKN8597A Secure Interface cable connects between J4001 (on the

secure board) and a connector on either the RF tray front panel or the station junction box. The station external TKN8531B KVL cable connects between the KVL and the station. Pins 1 and 2 of J4001 are signal lines, and the rest of the connector pins are control lines.

When a KVL is connected to the station, the CI_GND pin (J4001–4) is grounded, placing the station in access disable.

IMPORTANT
The SSCB front panel **Acc Dis** switch must be in its center (off) position.

The SSCB front panel **Select/Set** switch can be used to select the desired hybrid for key loading. During the key loading process, the front panel entry will always select individual hybrids as if the station were in half duplex mode (see Table 2). In a Full Duplex station, the hybrids that are grouped in encrypt/decrypt pairs are normally loaded with the same encryption key. For example, to keyload a full duplex station with two hybrids, use the following procedure.

NOTE
The key selection process allows selection of any of the eight possible hybrid installation positions, even if fewer than eight hybrids are installed.

Step 1. Plug the TKN8531B KVL cable into the station. Verify that the station is in access disable (the SSCB front panel **Disable** LED should be lit).

Step 2. Select KEY 1 with the **Select/Set** switch on the SSCB front panel.

Step 3. Depress the **PROGRAM** switch on the KVL. Verify successful key transfer (the KVL display should show "PASS").

Step 4. Select KEY 4 with the **Select/Set** toggle switch on the SSCB front panel.

Step 5. Depress the **PROGRAM** switch on the KVL. Verify successful key transfer (the KVL display should show "PASS").

Step 6. Disconnect the TKN8531B KVL cable. The SSCB front panel **Disable** LED should turn off.

The CI_KEY line is a bi-directional signal line, utilizing analog multiplexer U4021 to connect J4001-1 to the currently selected hybrid. The Code Insert Write Enable (CI_WE) and Key Insert Data (KID) signals are routed to the selected hybrid through an on-chip multiplexer in secure ASIC U4007. When key bits are being transferred to the KEY line (pin 8) of the hybrid, the $\overline{WE}$ line (pin 4) must go low to enable the write process. During that period, the clock to the hybrid must be synchronized with the clock in the KVL. To accomplish this, a synchronized clock signal (the KVL clock synchronization signal) is generated by the secure ASIC and phase locked to the KID signal. After all of the keys have been loaded, the KVL connector must be disconnected to take the station out of access disable.

NOTE
A successful Key transfer is indicated in the readouts of the KVL display for all hybrid types, except for the C794 *DVP* Hybrid option (TRN6777B).

A Key Variable backup battery is provided with all secure hybrid options, in order to allow the hybrid(s) to retain their encryption keys if the station loses power. If the +5 V supply drops out, the V_{CS} supply to the hybrids must be maintained above +2 V for key data retention. The 3.6 V lithium battery BT4001 should provide a minimum of 4 years of key retention time for eight hybrid installations, and up to 10 years of key retention time for two hybrid installations.

4.2 KEY CLEARING

The Key Reset ($\overline{KR}$) line, Pin 7 of the secure hybrids, provides a means for erasing all of the hybrid keys simultaneously, which prevents any further encryption or decryption.

NOTE
This function is not available with the C794 *DVP* Hybrid option (TRN6777B).

The secure board provides two methods with which to generate the $\overline{KR}$ active low signal and clear the keys.

- The first method uses the External Key Reset ($\overline{EXT\_KR}$) pin, J4001–5. This interface is provided to allow the Key Reset line to be activated by switches or push buttons that may be located on or near the station.
- The second method is controlled by microprocessor U4013. With jumper JU4002 in its alternate position, via the C683 option, an active high Key Reset signal from secure ASIC U4007–13 turns on transistor Q4003, grounding the $\overline{KR}$ signal line. The source of the key reset request is commonly a wireline function tone, which is communicated to the secure board via the HSR signal.

5. LOGIC SECTION

5.1 LOGIC CIRCUITRY DESCRIPTION

The logic circuitry can be broken down into four broad areas. They are:

- The Microprocessor Core Circuitry,
- The Data Communication Circuitry,
- The Secure Data Processing Circuitry
- The Reset Circuitry.

NOTE

The schematic diagrams for these areas are located on the diagram sheet titled "Logic and Control" at the end of this section.

Many of the functions carried out by the logic section are implemented with ASICs. The secure board uses two ASICs specifically designed for the application. U4010 is the station control ASIC operating in the standard mode. This ASIC serves as a specialized microprocessor support chip, with additional I/O lines and data communication features. U4007 is the secure ASIC designed to facilitate half or full duplex encrypted data processing, in either a transparent mode or an encrypt/decrypt mode.

5.1.1 Microprocessor Core Circuitry

The function of the microprocessor core circuitry is to run the software program controlling secure board operation. Most of the core circuitry functions are carried out using four integrated circuits.

U4013 is a Motorola 68HC11 8-bit microprocessor. During program execution, it generates an 8-bit multiplexed low-order address/data bus A/D(0-7), as well as a high-order address bus A(8-15). U4013 controls the direction and timing of bus transfers with the three signals (E, RW, AS) that are common to the Motorola 6800 family of devices.

Pin U4013-5 provides the E signal, which functions as the primary clock for all bus transfers. U4013 generates the E clock by dividing the external crystal frequency by four, thus E = 7.9488 MHz/4 = 1.9872 MHz. U4013 controls the direction of bus transfers, using the R/$\overline{W}$ signal at pin U4013-6. This signal is high when U4013 needs to read data off the bus, and is low when U4013 is writing data to the bus. In order to allow an external latch in ASIC U4014 to demultiplex the low-order address/data bus, U4013 also generates the AS (Address Strobe) timing signal on pin U4013-4. Thus, when the AS signal is high, A/D(0-7) contains the low order address bus A(0-7). But, when the AS signal is low, A/D(0-7) contains the data bus D(0-7).

The software to control U4013 is provided as "firmware," which is code stored in a 32K CMOS EPROM (U4009). U4013 itself also contains 512 bytes of on-chip EPROM for station parameter codeplug storage. During program execution, U4013 can access 192 bytes of internal RAM, as well as the 8k x 8 external RAM (U4010).

Many of the "glue" chips commonly required to complete a microprocessor system are replaced by on-chip logic circuitry included in standard mode ASIC U4014. Since U4013 operates with a multiplexed low-order address/data bus A/D(0-7), U4014 contains an address latch to demultiplex that bus. Thus, the low-order address bus A(0-7) is an output of U4014. U4014 also contains all the circuitry required to perform full address decoding, using the 16-bit expanded address bus for the entire 64k memory space. Therefore, all required chip select signals are also outputs of U4014.

The $\overline{\text{MEM OE}}$ pin drives the output enable pins on EPROM U4009. This signal is active low during every read cycle (E and R/$\overline{W}$ both high). The ROM $\overline{CE}$ signal drives the chip enable pin on EPROM U4009. This signal is active low whenever the address bus indicates an access in the EPROM memory space. The RAM $\overline{WE}$ pin is active low during normal write cycles (E high and R/$\overline{W}$ low).

5.1.2 Data Communications Circuitry

The secure board logic section has three methods with which to communicate with other modules in the station: The IPCB, the MUXbus, and the High Speed Ring (HSR) signals.

The IPCB (Inter-Processor Communication Bus) is a low speed serial link shared among all the station control tray boards, as well as optional expansion modules. On the secure board, U4013 interfaces to the IPCB using its SCI (Serial Communications Interface). This link can carry status and control information between modules. The IPCB line is pulled up on the station control board, and is normally high in the idle state until a module begins to write information onto it. The SCI from U4013 has both a receive and a transmit port, which are buffered by Q4008-Q4010, and then wired-ORed together, before being routed as the IPCB line to the required connectors.

The MUXbus is a time-multiplexed address and data bus capable of carrying 64 bits of control and status information between station modules. The secure board serves as a MUXbus slave (the SSCB drives the MUXbus). All the circuitry needed to interface to the MUXbus is contained in ASIC U4014.

The SSCB, as the master, is responsible for driving the data strobe and address lines. The MUXbus consists of 16 4-bit data nibbles, for a total of 64-bits. Address bits BA0-BA3 are continually cycled, to access each 4-bit data nibble in a consecutive fashion. The 4-bit data nibble is represented by MUXbus data bits $\overline{BD0}$-$\overline{BD3}$. U4014 signals U4013 to service the MUXbus data at each address,

via the active low $\overline{\text{MUXIRQ}}$ signal. All multiplex timing is done using the $\overline{\text{DS}}$ (data strobe) signal generated on the SSCB. The data strobe signal is generated by dividing the E clock signal by 640 ($\overline{\text{DS}}$ = 1.9872 MHz/640 = 3105 Hz).

The HSR signal is a unique multiprocessor communication method. All the circuitry to implement the HSR signal is on-chip in ASIC U4014. The HSR signal continually circulates a 40-bit packet between all modules (SSCB, TTRC, and secure) in its ring. Of these 40 bits, 16 can be written to by the SSCB, 16 are reserved for writes from the Trunked Tone Remote Control (TTRC) board, and 8 are reserved for writes from the secure board. All three boards can read any of the bits in the 40-bit packet.

The SSCB, as the HSR master, provides the HSR CLK and HSR SYN signals used to synchronize all packet transfers. The frequency of the HSR clock is programmable, but is normally set to E/2 (0.9936 MHz). The HSR SYN signal is asserted, for 1-bit time, at the start of each 40-bit packet.

The SSCB outputs its HSR OUT data from U801 to the TTRC, via J804. Data from the TTRC HSR signal is taken in via J804, and passed directly to U4014-48 on the secure board via P803-11. Data from the secure board HSR signal is taken in via J803-9, and sent back to U801 as HSR IN, to complete the ring.

NOTE

To complete the ring, JU2 (the SSCB secure HSR jumper) should be in its alternate position when a secure board is installed.

5.1.3 Secure Data Processing Circuitry

Secure ASIC U4007 performs most of the time-intensive data processing tasks required on the secure board, freeing up the microprocessor to perform data detection and other pertinent tasks. U4007 uses a separate 3.072 MHz crystal oscillator to generate many of the internal clocks needed for secure data applications. Functions performed by U4007 include the following.

- Address Decoding

Secure ASIC U4007 acts as a microprocessor support component in conjunction with the station control ASIC U4010, providing seven on-chip 8-bit output latches and eight on-chip 8-bit read buffers. The output latches are used primarily for gating and control internal to U4007, and also provide external control signals for the secure hybrids. The input buffers are used primarily for internal data collection, while also monitoring external hybrid KEY/$\overline{\text{FAIL}}$ lines for a key failure indication.

- Clock Recovery (transmit and receive)

The clock recovery circuits generate the 12 kHz clock signals, which are phase locked to the incoming transmit and receive data. The ASIC contains an on-chip 12 kHz clock circuit, which phase locks to the incoming data stream by detecting data transitions and adjusting the clock phase until the falling edges of the clock pulses occur in sync with the data transitions. The 12 kHz clock signals are used on-chip to clock the 12 kBit/Sec data circuitry, and are used externally to clock the secure hybrids and CVSDs. The clock recovery circuits can also be configured to provide a fixed 12 kHz clock signal, for use when encrypting.

- Phase Lock Detection (transmit and receive)

The phase lock detectors determine whether or not the recovered clock is phase-locked to the incoming data. A hardware count is generated by comparing incoming data transitions to the falling clock edge. The software monitors the count and determines whether or not the signal is valid data.

- Serial-to-Parallel Conversion (transmit and receive)

The 12 kBit/Sec data is shifted into an 8-bit serial-in/parallel-out shift register by the recovered clock. After eight bits have been shifted in, the serial-to-parallel converter generates an interrupt to U4013. The RX_IRQ and TX_IRQ interrupt lines are connected to the serial-to-parallel converters in U4007, and to the input capture ports of U4013. The software services the interrupt by reading the serial-to-parallel register before the next bit is shifted in. Interrupts are active high 83.3 µs pulses, occurring at 667 µs intervals.

- Parallel-to-Serial Conversion (transmit and receive)

After the parallel data has been First-In-First-Out (FIFO) buffered and analyzed, it is converted back into a 12 kBit/Sec data stream. During RX_IRQ or TX_IRQ interrupt servicing, while the serial-to-parallel converter interrupt signal is high, the parallel data is automatically loaded into an 8-bit shift register at the rising edge of the recovered clock. The data is shifted out with each of the next eight rising clock edges.

- Alert Tone Generation

A 750 Hz internally generated square wave can be gated to the Key Alert Tone pin, U4007-40. It is used in encode/decode stations to provide an audible indication of Key Variable status and coded/clear operation to the remote operator.

- Splatter Filter Clock Generation

A clock output is provided at U4007-50 to clock a switched capacitor filter, which is used in the splatter filter on the secure board. The clock frequency can be software selected as either 341.3 kHz (XTAL/9) or 307.2 kHz (XTAL/10).

- Key Reset Generation/Protection

A key reset generator is provided to clear the encryption hybrid key variables via a software command. To protect against accidental resets, two monostable timers must be activated simultaneously in order to generate a reset pulse output at U4007–13. The reset pulse is an active high signal, with a pulse width of 9.3 ms to 10.67 ms.

- Multi–Key Signal Multiplexing/Demutiplexing

U4007 supports up to eight key variables and hybrids in an encode/decode station configuration. Several multiplexers incorporated in U4007 handle the routing of the following signals: WE, KEY, RX DATA, TX CIPHER, and TX DATA. Three control lines are also provided to control an external 8–bit multiplexer via U4007–51, 52, and 55. These control an 8:1 analog multiplexer, which provides bi–directional gating for the CI_KEY line between the secure hybrids and a key loader.

- Alignment Mode Test Tone Generation

A 1 kHz clock can be routed to the Coded Mod output, U4007–45, to provide a 1 kHz square wave for transmit deviation alignment.

- Key Fail Input Buffer

The KEY inputs on U4007 allow the software to poll the KEY/$\overline{\text{FAIL}}$ lines on the secure hybrids for a key fail status by momentarily activating the R/$\overline{\text{T}}$ and PTT pins. The Key Fail input buffer can be used to determine which of the eight hybrids has lost its key.

5.1.4 Reset Circuitry

The $\overline{\text{EXPANSION RESET}}$ signal at P803–33 originates on the SSCB. This active low signal will hold the secure board in reset whenever the SSCB pulls it low. This signal is used to hold all modules connected to this line in reset for a period of time after power up, during which the SSCB performs self diagnostics.

NOTE

The secure board does NOT generate an $\overline{\text{EXPANSION RESET}}$ signal to reset other modules in a system.

A $\overline{\text{RESET}}$ signal can be generated on the secure board either by the low voltage reset circuit, or by a U4013 Computer Operating Properly (COP) reset.

To prevent erroneous writes to the on–chip EEPROM of U4013 during power up, power down, or low voltage conditions; it is essential to activate $\overline{\text{RESET}}$ whenever the +5 V supply voltage drops too low. This is accomplished by using low voltage reset generator Q4022. This PNP transistor is normally on, pulling up the $\overline{\text{RESET}}$ line through R4125. When the +5 V line drops too low, Q4022 will turn off and provide a passive pulldown on the $\overline{\text{RESET}}$ line through R4124. This occurs when the +5 V line drops below approximately +3.5 V.

Microprocessor U4013 contains a Computer Operating Properly (COP) timer, which will generate a reset if the COP timer is not periodically serviced by the software. This is to ensure that the secure board will restart execution if the program somehow loses proper sequence. The COP circuit generates a short $\overline{\text{RESET}}$ pulse (approx. 2 E cycles), which forces the program to restart execution at the address indicated by the RESET vector.

The secure board contains a circuit which holds the MUXbus data lines inactive, to prevent any undesired writes to the MUXbus while the software performs self–diagnostics. This is implemented with the Delayed Reset Generator (DRG) circuit. U4008 is a 555–type timing device, which triggers an active high delayed reset at U4014–46 when the $\overline{\text{RESET}}$ input goes low. Once the $\overline{\text{RESET}}$ line is deactivated, the DRG circuit will wait for a period of time determined by the time constant of C4092 and R4120 before deactivating the delayed reset line. The length of the period should be about 500 ms.

5.2 LOGIC CIRCUITRY TROUBLESHOOTING

If the a failure in the secure board logic section is suspected, first check the +5 V supply pins on each of the logic devices U4007 through U4014. Next, look at the $\overline{\text{RESET}}$ line at TP6. This line should be pulled high with no pulses on it. A 2 µs pulse occurring every 16 ms on the $\overline{\text{RESET}}$ line identifies a COP reset, which occurs when the software is not functioning properly. If the reset occurs continuously, EPROM U4009 may be improperly programmed, damaged, or improperly inserted. Also look at the DELAYED RESET line, which should be low with no pulses on it. A properly functioning microprocessor will drive the E line (U4013–5) with a 1.9872 MHz square wave. Also check ASIC U4014 for proper logic levels on all of the data bus inputs, address lines, and output latch outputs.

If the secure board is not responding to external commands such as a $\overline{\text{KEY RESET}}$ or EXTERNAL CODE DETECT, the HSR or MUXbus communication may not be operating properly. Verify that HSR CLK = E/2 (controlled by the SSCB) and that HSR SYN is high every 40 HSR CLK cycles. Also verify that $\overline{\text{DS}}$ = station control 3105 Hz square wave, and that the address lines are being driven. For proper operation, the address nibble BA0–BA3 should be incremented modulo–16. The SSCB drives both the HSR and MUXbus circuitry, therefore it is best to check for proper connections between these two boards and for correct jumper positions on the SSCB.

Secure ASIC U4007 functionality can be checked by examining its clock outputs. A 12 kHz square wave should always be present at U4007–35 through –38. The 341.3 kHz (or 307.2 kHz) splatter filter clock should always be present at pin U4007–50. If it's not there, verify that there is a 3.072 MHz oscillation at U4007–1 and –2. Also check

the logic levels of the data and clock lines coming from U4013. If valid code is present at either the RAW RX or TX data lines and a code detect is not being generated, make sure the interrupt signals are being generated and routed to the microprocessor at U4013-32 and -33. The interrupt signals are active high 83.3 ms pulses, occurring at 667 ms intervals.

6. SOFTWARE DIAGNOSTICS

6.1 GENERAL

When the station powers-up or is reset, the SSCB holds the secure board in reset via the Expansion Reset signal until the SSCB finishes its diagnostic tests. When the Expansion Reset signal is deactivated, the secure firmware begins execution at the location contained in its RESET vector. This location is the beginning of the secure firmware's main background routine. The main background routine is basically an endless loop, the background loop, which calls all routines which are not interrupt-driven. Before entering the background loop, a startup diagnostics routine, named Secure_Reset_Diags_Asm (SRDA), is called, which performs diagnostic tests of the secure board.

NOTE

The SSCB **Secure Fail** LED should light immediately upon station power-up, and remain lit until the end of the SRDA routine. This verifies the operation of the SSCB **Secure Fail** LED, and indicates that the on-board diagnostics are in the process of being performed.

The SRDA routine mainly performs functionality tests on the secure board circuitry. However, before beginning the diagnostic tests, the routine initializes some microprocessor registers. These registers determine the microprocessor's Computer Operating Properly (COP) watchdog time-out time, and set up the Serial Communications Interface (SCI) to communicate at the same baud rate and message protocol as the other boards on the Inter-Processor Communications Bus (IPCB).

When initialization of the microprocessor has been completed, the transmit code detect (**Tx CD**) and receive code detect (**Rx CD**) LEDs should light. This verifies operation of the **Tx CD** and **Rx CD** LEDs, as well as providing a progress indication for the SRDA routine.

At this point, the actual secure board diagnostic tests begin. The diagnostic tests can yield a number of error conditions. To identify which diagnostic test failed, the errors are displayed via either the SSCB **Secure Fail** LED, or the front panel **Status** display.

6.2 TYPES OF ERRORS

Two types of error classes exist: fatal and non-fatal. Fatal errors are errors which are severe enough to prevent proper operation of the secure board. Fatal errors will cause the secure board to reset. Non-fatal errors are warnings, and do not prevent operation of the secure board. Non-fatal errors do not cause the secure board to reset.

Failure of some of the initial diagnostics tests require that the SSCB **Secure Fail** LED, as opposed to the front panel **Status** display, be used for error display. The **Secure Fail** LED is used because the IPCB communications links to the SSCB and the secure board external RAM have not yet been verified. To use the front panel display the IPCB must be operating properly, because it is needed to send the secure board error codes to the SSCB, and the external RAM is needed to hold the error codes.

IMPORTANT

All failures which use the secure board **Secure Fail** LED for display are fatal errors.

Those fatal errors which use the **Secure Fail** LED cause the SRDA routine to call an error handler routine with a fixed number. The error handler routine then flashes the **Secure Fail** LED for that fixed number of times and then waits, not servicing the COP timer. Since the COP timer is not serviced, it will eventually time-out and the secure board will reset.

Failures which use the front panel **Status** display may be either fatal or non-fatal errors. In this case, when an error is detected, the SRDA routine calls a different error handling routine which writes a value, called an error code, to a queue in RAM. Later, after IPCB operation is verified, the SRDA routine transmits the error codes, one-by-one, to the SSCB via the IPCB.

The station control firmware reads each error code and determines whether it is fatal or non-fatal. If the error code is fatal, the station control firmware will display the error code for five seconds, and then stop servicing its COP timer. When the COP timer expires, the SSCB resets, activating the Expansion Reset line. The Expansion Reset signal, in turn, resets any board connected to it, which includes the secure board.

IMPORTANT

The secure board does NOT reset itself for fatal errors.

If the error code is non-fatal, the station control firmware displays the error for five seconds, and continues to service its COP until the next error code is received over the IPCB. Resets do not occur for non-fatal errors.

In the case of a fatal error left uncorrected, the test which caused the fatal error will fail again. The same error will

be displayed, and the firmware will reset again. This sequence will continue until the failure is corrected.

6.3 TYPES OF TESTS

The SRDA routine checks two major sections of the secure board, the digital circuitry and the audio circuitry. Internal digital diagnostic tests are performed first, followed by external digital diagnostic tests, followed by audio diagnostic tests. Internal digital diagnostic tests refer to tests which verify the operation of the secure board digital circuitry as stand-alone hardware. These tests only run when the secure board is reset.

External digital diagnostic tests verify the operation of the secure board digital circuitry as part of the overall station control tray. The external digital diagnostic tests are not performed if the secure board has reset itself. This is to prevent the secure board from adversely affecting station operation while going through those external digital diagnostic tests.

Finally, the audio diagnostic tests verify operation of the secure board audio circuitry. These tests are also not performed if the secure board has reset itself, because they also could affect station operation.

7. INTERNAL DIGITAL DIAGNOSTICS

7.1 EXTERNAL RAM TEST

The first digital diagnostic self-test performs a high and low toggle on each of the eight bits in every byte of the external RAM. After each RAM byte is checked, it is cleared to all zeros (lows) so that all RAM bytes are initially clear. If any external RAM byte fails this test, the SRDA routine calls the LED-Flashing error handler routine, which uses the secure board **Secure Fail** LED as the error display. The **Secure Fail** LED flashes four times as a result of this error, and the secure board resets because the error handling routine does not return, and does not service the COP.

7.2 INTERRUPT TEST

The next test verifies that the RX_IRQ (Input Capture 1 Interrupt) and TX_IRQ (Input Capture 2 Interrupt) are working. The RX_IRQ interrupt is the result of eight 12 kBit/sec data bits having been clocked into the receive serial-to-parallel converter of secure ASIC U4007. This interrupt, when enabled, will occur approximately every 667 μs (8 bits @ 12 kBit/Sec = 667 μs). It serves both to initiate operation of the receive code detector and to update the secure software system timer; and also polls the Synchronous Communications Interface (SCI) interrupt to see if any Inter-Processor Communications Bus (IPCB) activity exists.

The TX_IRQ interrupt is the result of eight 12 kBit data bits having been clocked into the transmit serial-to-parallel converter of secure ASIC U4007. This interrupt, which also occurs approximately every 667 μs, initiates operation of the transmit code detector and also allows the MUXbus to be read.

NOTE
The secure board does not write to the MUXbus because of timing restrictions.

If either of the two interrupts fail, the SRDA routine calls the LED-Flashing error handler routine, causing the **Secure Fail** LED to flash two times.

7.3 INTERNAL RAM TEST

The next test performs a high and low toggle on each of the eight bits in every byte of the on-chip RAM in microprocessor U4013. After each RAM byte is checked, it is cleared to all zeros (lows) so that all RAM bytes are initially clear. If any byte fails to pass this test, the SRDA routine writes a fatal error code to the error queue in external RAM.

IMPORTANT
For this test, and all following tests (with the exception of the IPCB test), the SRDA routine can put error codes into the queue because the external RAM has passed its test.

7.4 MICROPROCESSOR CONFIGURATION TEST

The next test the SRDA routine makes checks to see how the microprocessor is configured, i.e., examines what is contained in its CONFIG register. If the CONFIG register is not set up as desired, a check is made to determine if the CONFIG register can be corrected without erasing it. If so, the SRDA routine makes the correction and writes a fatal error to the error queue.

If the CONFIG register must be erased in order to correct it, the SRDA routine erases it, which erases the entire internal EEPROM, and then reprograms the CONFIG register with the desired features. After making the correction, the SRDA routine writes a fatal error to the error queue. Erasing the CONFIG register will cause the entire internal EEPROM, which is the codeplug, to be erased.

As with all fatal error codes placed into the error queue, the CONFIG re-programmed errors cause the SSCB microprocessor COP timer to time-out, which activates the Expansion Reset signal, causing the secure board to go through a reset cycle. Going through a reset cycle causes the SRDA routine to be executed again. However, this test is somewhat different, because the SRDA routine had previously made a correction before writing a fatal error code to the error queue. Therefore, upon returning to this part of the routine, the CONFIG register should be cor-

rect and the firmware should not fail this test again. If the internal EEPROM was erased, the secure firmware will get caught in a fatal error loop due to some other error.

7.5 CHECKSUM TEST

The next SRDA routine calculates the single-byte-add checksum of the secure firmware. If this calculated checksum does not match the value stored in the secure firmware, the SRDA routine writes a fatal error to the error queue.

7.6 ASIC TESTS

7.6.1 Secure ASIC U4007 Tests

The next section of the SRDA routine performs tests on Secure ASIC U4007. These tests perform operational examinations of the serial-to-parallel and parallel-to-serial converter circuits and the phase lock detector circuits.

7.6.1.1 PARALLEL-TO-SERIAL and SERIAL-TO-PARALLEL CONVERTER TESTS

In these tests, both the transmit and receive parallel-to-serial converters are loaded with known values. After a period of time long enough to allow those bits to be shifted from the parallel-to-serial converter into the serial-to-parallel converter, the data is read from the corresponding serial-to-parallel converter.

If the value read from the serial-to-parallel converter does not match the value originally put into the parallel-to-serial converter, the test has failed. The SRDA routine then writes a fatal error to the error queue, for whichever parallel to serial/serial to parallel converter combination failed. The same test is then performed using an inverted version of the known value written into the parallel-to-serial converters.

7.6.1.2 PHASE LOCK DETECTOR TESTS

The next test performed is to check the operation of the receive and transmit phase lock detector circuits. These tests verify correct operation of the phase lock detector circuits for a variety of conditions. For example, the phase lock detector circuits are tested to verify that a known data input causes their counters to count up to a known value (within some range). The phase lock detector circuits are also tested to insure that a count is NOT produced without input data present.

In the process of these tests, the operation of the control lines for the phase lock detector circuits is verified. If the phase lock detector circuits fail any of these tests, the SRDA routine writes a fatal error to the error queue for the failed phase lock detector circuit(s).

7.6.2 Standard ASIC U4014 Tests

After all secure ASIC tests are complete, the SRDA routine tests standard ASIC U4014. During the first standard ASIC tests, since internal testing is being performed, U4014 is put into an internal test mode. For the ASIC, internal mode means that the U4014 is tested by the SRDA routine as a stand-alone device. That is, all outputs are looped back to the inputs. Later, if the external diagnostics section of the SRDA routine is executed, the U4014 is tested as part of the overall station control tray.

7.6.2.1 OUTPUT LATCH TEST

The first test performed on U4014 is verification of its output latches. Known data is written to the output latches, then the corresponding loopback input buffers are read. If the output latches and input buffers do not agree, the SRDA routine writes a fatal error to the error queue.

7.6.2.2 MUXbus TESTS

The next test of U4014 examines the MUXbus circuitry. Since the secure firmware cannot write to the MUXbus due to timing restrictions, only the read portion of the hardware is tested. First, the Data Strobe line is checked. While checking for Data Strobe, the SRDA routine also verifies that 0s can be read at all MUXbus addresses. If that test passes, the SRDA routine verifies that 1s can be read at all MUXbus addresses. These tests verify operation of the MUXbus data and address lines. If any of these tests fail, the SRDA routine writes a fatal error to the error queue.

7.6.2.3 HIGH SPEED RING TESTS

The next U4014 tests are associated with the High Speed Ring (HSR) signal. The first HSR test performed is an operational check of the ring synchronization and ring clock lines. Two watchdog bits in U4014 hardware (one for ring sync and one for ring clock) are read to determine if the ring sync and ring clock signals are operating properly.

Next, the SRDA routine writes data to only the secure portion of the HSR signal. Then it reads all portions of the HSR signal. If the data read from the secure portion does not match what was written, or if the SSCB and the TTRC portions of the signal are not zero, the result is an HSR signal failure.

NOTE

Since the secure board is in its internal test mode, it should be disconnected from the HSR signalling ring. Therefore neither the SSCB nor the TTRC boards should be able to write to their portions of the HSR signal.

Next, an inverted version of the data is written to the secure portion of the HSR signal, and the same test is performed again. If any of these HSR signal tests fail, the SRDA routine writes a fatal error to the error queue.

7.7 PARAMETER TESTS

The next section of the SRDA routine compares various parameters between the secure codeplug and the secure firmware.

- Module ID – If the Module ID stored in the codeplug is not the same as the Module ID stored in the firmware, the SRDA routine writes a fatal error to the error queue.
- Codeplug Version – If the codeplug version is not the same as the firmware version, the SRDA routine writes a fatal error to the error queue.
- Checksum – The SRDA routine calculates the single-byte-add checksum of the secure codeplug. If this calculated checksum does not match the value stored in the secure codeplug, a fatal error is written to the error queue.

7.8 EEPROM TESTS

The next section of the SRDA routine checks to determine if a reset occurred during an EEPROM update. The proper sequence of events that should occur while updating the EEPROM is as follows. An image of the EEPROM is always kept in RAM. If a user modifies that RAM copy, and wishes to make it permanent by writing it to the EEPROM, the user must issue a write-EEPROM-from-RAM command, via the IPCB. That command causes the firmware to erase the entire EEPROM, causing all bytes to be set to hexadecimal value FF.

After erasing the EEPROM, the firmware begins copying the modified RAM image to the EEPROM, byte-by-byte. The copying process can take up to 15 seconds. One byte at the beginning of EEPROM is used as the check byte, which is used to determine if all of the RAM image has been copied to the EEPROM. This byte, which is set to FF by the erase, is set to 00 only after all bytes have been copied from the RAM image to the EEPROM.

If a reset occurs before this update is completed, this byte will be FF and the SRDA routine will know that the EEPROM is corrupted. A fatal error is then written to the error queue.

A similar check is made on the user-area section of the EEPROM to insure that it was not being updated when a reset occurred. However, since the secure firmware does not use the user-area for any storage, this fatal error should never occur.

8. EXTERNAL DIGITAL DIAGNOSTICS

8.1 WAKE-UP MESSAGE TEST

At this point, the internal digital diagnostics are completed, and the SRDA routine may begin the external digital diagnostics and audio diagnostics. In order to determine whether the external tests are to be performed or not, the secure firmware must receive a wake-up message from the SSCB, via the IPCB. However, two conditions can cause the secure firmware to wait before it begins looking for the wake-up message. The conditions are an active access disable signal and the receipt of a shut-up message from the SSCB.

The access disable signal could be active if any board in the station control tray failed its audio tests and the user, wanting to troubleshoot the board, activated the **Acc Dis** switch on the SSCB front panel. The shut-up message comes from the SSCB if any portion of the station control tray EEPROM is being updated. Any activity which could affect an EEPROM update is therefore inhibited. The shut-up message can be cleared only by resetting the SSCB.

When the access disable signal is inactive and a shut-up message has not been received, the secure firmware begins looking for a wake-up message. The receipt of this message tells the secure firmware to execute its external digital diagnostic tests. If the wakeup message is not immediately present, the secure board will start a ten second time-out timer, and wait for the wake-up message. The wake-up time-out period allows the SSCB and TTRC modules to finish their external digital diagnostic tests. During the wake-up message time-out time, EEPROM operations are enabled, allowing EEPROM updates. Therefore, if a shut-up message is received, the wake-up time-out timer is halted. The timer is also halted if the access disable signal is activated during that time.

If the wake-up message does not occur within the wake-up time-out time, the SRDA routine writes a non-fatal error to the error queue, and the external digital diagnostic tests are bypassed. The non-fatal error indicates that the secure board was most likely reset without $\overline{\text{Expansion Reset}}$ being activated..

IMPORTANT

Whether or not the secure firmware receives the wake-up message, the **Rx CD** LED is then turned off, indicating that the secure board has finished its internal digital tests.

8.2 MUXbus TEST

The first external digital diagnostic test verifies operation of the MUXbus circuitry. The test will be performed only if the secure firmware has received a wake-up message from the SSCB. The reason for this is that the MUXbus should not be manipulated by this test if the secure board has reset.

The tests performed on the MUXbus at this point are identical to the previous internal MUXbus tests (refer to paragraph 7.6.2.2), but now the MUXbus circuitry is interacting with the master MUXbus circuit on the SSCB, and any other slave MUXbus circuits on other boards. If any of the MUXbus tests described previously fail, the SRDA routine writes a fatal error to the error queue.

8.3 HIGH SPEED RING TESTS

The HSR test is also performed only if the secure firmware has received a wake-up message from the SSCB. The tests performed on the HSR at this point are identical to the previous internal HSR tests (refer to paragraph 7.6.2.3), but now the HSR circuitry is interacting with the master HSR circuit on the SSCB, and any other slave HSR circuits on other boards. If any of the HSR tests described previously fail, the SRDA routine writes a fatal error to the error queue.

8.4 IPCB TEST

Up to this point, all errors have been entered into an error queue, with the intention of sending them to the SSCB, via the IPCB. When the SSCB receives the errors, it will display them one-by-one on the SSCB front panel **Status** display. If the IPCB is not working, errors from the secure board cannot be displayed. Therefore, the next test verifies operation of the IPCB by sending a known IPCB message to the SSCB. If it does not respond, or does not respond with the expected response, the SRDA routine calls the LED-flashing error handler routine, causing the **Secure Fail** LED to flash 6 times.

Once IPCB operation is verified between the secure board and the SSCB, the secure board can send its errors, via the IPCB, for display on the SSCB front panel **Status** display. Since most errors up to this point have been fatal errors, the first error code received by the SSCB will most likely be fatal and cause the SSCB to reset. If it does reset, no further errors will be displayed.

NOTE

The IPCB test is the final external digital diagnostic test.

9. AUDIO DIAGNOSTICS

9.1 GENERAL

The next SRDA tests check the operation of the secure board audio paths. They are performed only if the secure firmware has received a wake-up message from the SSCB. This insures that a secure board which has reset by itself does not interfere with a normal operating station.

Before beginning the audio diagnostics, the analog-to-digital (A-to-D) converters of the microprocessor are checked to verify that they are operational. If any of the A-to-D converters fail, the SRDA routine immediately sends a non-fatal error to the SSCB for display. Since the IPCB has passed its examination when it reaches this point; for this test and the following audio diagnostic tests the SRDA routine no longer needs to put its errors into a queue. Instead, the errors can be immediately sent to the SSCB for **Status** display.

During this test, and the following audio diagnostic tests, once the error (always non-fatal) is displayed, the user will have two seconds to activate the **Acc Dis** switch on the SSCB front panel. If the **Acc Dis** switch is activated within that time, the current diagnostic conditions will freeze, allowing the user to troubleshoot the failed circuit. Freezing the current diagnostic test may be desirable because it allows audio gating, which may not be possible in normal operation. If the operator misses the time to activate the switch, the station can be reset with the SSCB **Reset** switch, and the user can then wait until the failed diagnostic test is executed again.

NOTE

If any of the following audio tests fails, four seconds are allowed before the reset test, in order to give the SSCB enough time to display the error.

9.2 ALERT TONE GENERATOR TEST

The first audio circuit checked is the alert tone generator circuit. If a 750 Hz tone is not present at the appropriate A-to-D converter when the tone is enabled, or if the 750 Hz tone is present at the A-to-D converter when the tone is disabled, the SRDA routine sends a non-fatal error to the SSCB for display.

9.3 MODULATOR PATH TEST

The next audio circuit tested is the modulator path going to SSCB connector P803. For this test, a 1 kHz test tone from secure ASIC U4007 is enabled, but initially is not gated to the corresponding A-to-D converter. If the test tone is present at the A-to-D converter, the SRDA routine sends a non-fatal error to the SSCB for display. Next, the test tone is gated to the A-to-D converter. If the test tone is not present at the A-to-D converter, the SRDA routine sends a different non-fatal error to the SSCB for display.

9.4 RECEIVE PATH TEST

The next audio circuit to be tested is the receive wireline path going to SSCB connector P803. An EOM is generated by the SRDA routine, and gated to an A-to-D converter. If the EOM is not present at the A-to-D converter, the SRDA routine sends a non-fatal error to the SSCB for display. Next, the CODED_GATE signal on the secure board is disabled. If the EOM is present at the A-to-D converter, the SRDA routine sends a different non-fatal error to the SSCB for display.

NOTE
The receive path test is the final audio diagnostic test.

10. SECURE MODULE ENABLING

After performing the audio diagnostics, the SRDA routine is finished with all of its testing. To provide the user with an indication of this, the version number of the secure firmware is transmitted to the SSCB, via the IPCB, for display.

Next, the secure board output latches are initialized, and the various parameters for secure data detection are loaded into RAM from the codeplug. The two secure board interrupts, RX_IRQ and TX_IRQ, are then enabled, and other variables are initialized.

At this time, the **Tx CD** LED is turned off, to indicate to the user that the SRDA routine has completed all of its tests and that the secure firmware is ready to begin execution of its background routines. The SRDA routine, if provided a wake-up message as described in paragraph 9.1, now waits to receive a background enable message from the SSCB, via the IPCB. When the background enable occurs, the SRDA routine begins execution of the station background routines. A time-out timer is NOT used while waiting for the background-enable message.

Requiring a background-enable message prevents the secure firmware from executing its background routines before other remote boards have completed their diagnostics. It is necessary to prevent this condition, because the execution of the background routines by one board while other boards are still in their diagnostic mode could cause spurious failures of some of the diagnostic tests, due to manipulation of the MUXbus, HSR, and IPCB signals and/or messages.

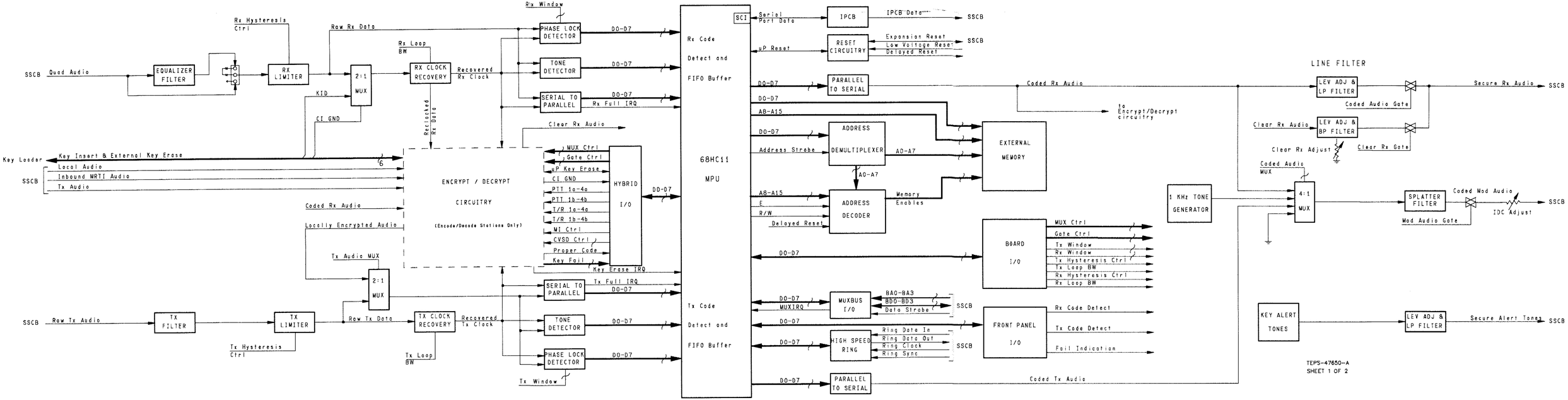
If the secure firmware did not receive the wake-up message earlier in the routine, it is assumed that the secure firmware reset on its own, and therefore should not wait for a background-enable message from the SSCB. In this case, the secure firmware immediately begins execution of the station background routines.

NOTE
Before beginning execution of the station background routines, the SSCB **Secure Fail** LED is turned off, indicated that the secure firmware is executing the station background routines.

Table 3. Secure Board Jumpers

Jumper Number	Description	Normal Position	Alternate Position
JU4002	Remote Key Reset	Disabled	Enabled
JU4003	MRTI audio	no MRTI audio	MRTI audio
JU4004	Receive Equalizer Filter	Filter in	Filter out

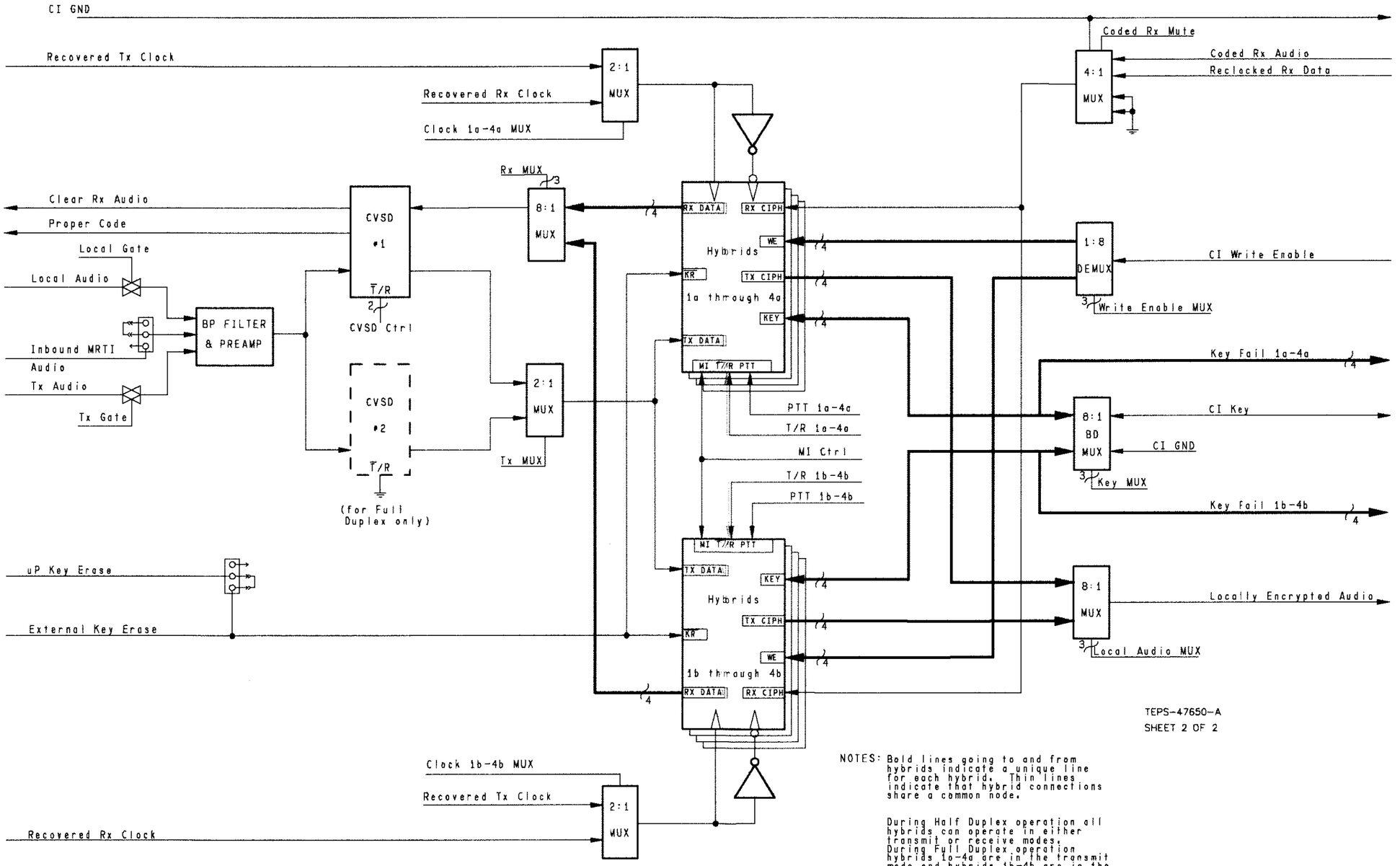
SECURE MODULE
MODEL TLN3045C
OVERALL BLOCK DIAGRAM



TEPS-47650-A
SHEET 1 OF 2

SECURE MODULE

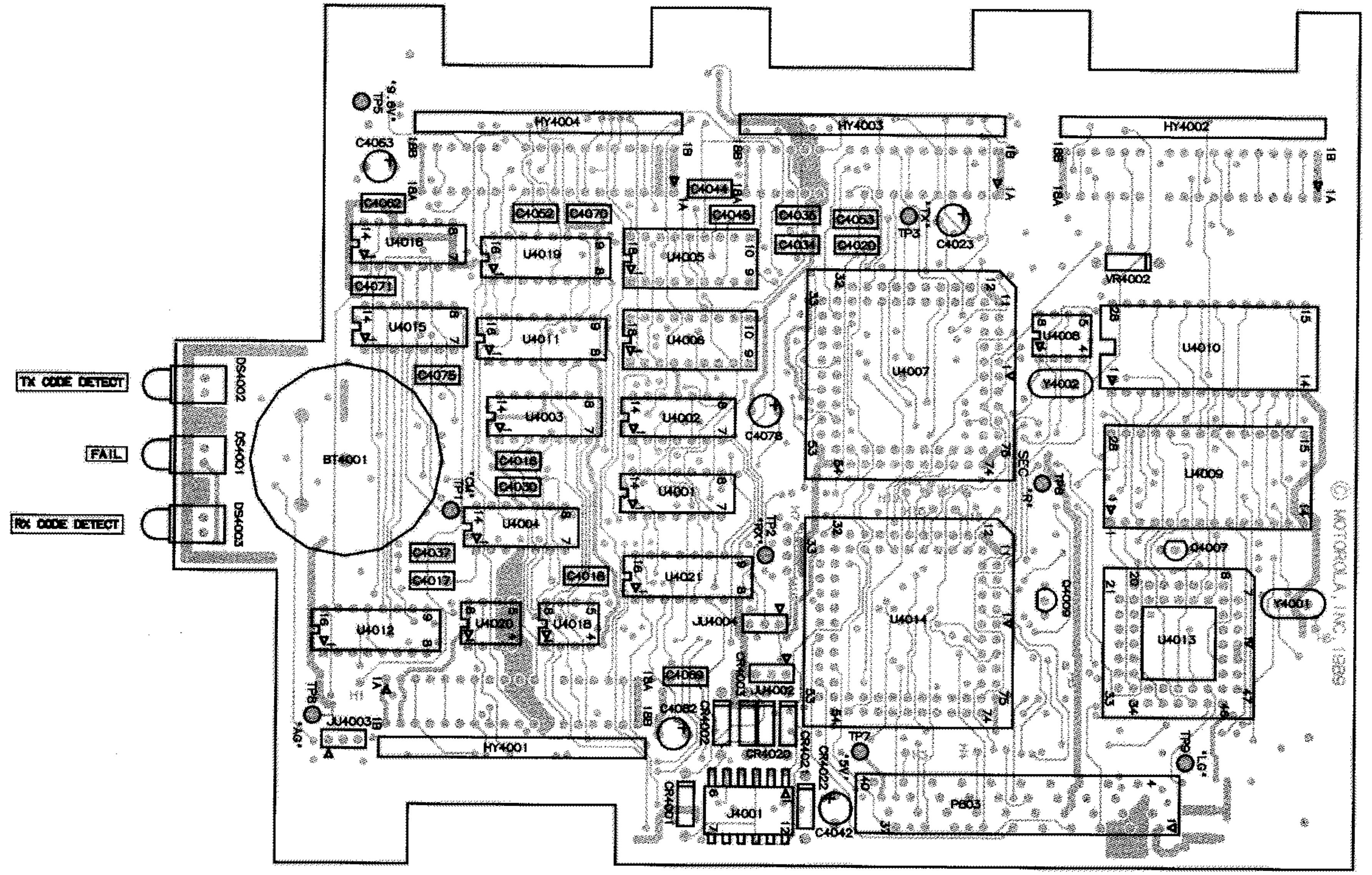
MODEL TLN3045C
ENCRYPT/DECRYPT CIRCUITRY
BLOCK DIAGRAM



TEPS-47650-A
SHEET 2 OF 2

NOTES: Bold lines going to and from hybrids indicate a unique line for each hybrid. Thin lines indicate that hybrid connections share a common node.

During Half Duplex operation all hybrids can operate in either transmit or receive modes. During Full Duplex operation hybrids 1a-4a are in the transmit mode and hybrids 1b-4b are in the receive mode.



SHOWN FROM COMPONENT SIDE

BD-TEPS-47410-A

OL-TEPS-47411-A

NOTE: SHADED AREA INDICATES DEFAULT JUMPER POSITION.

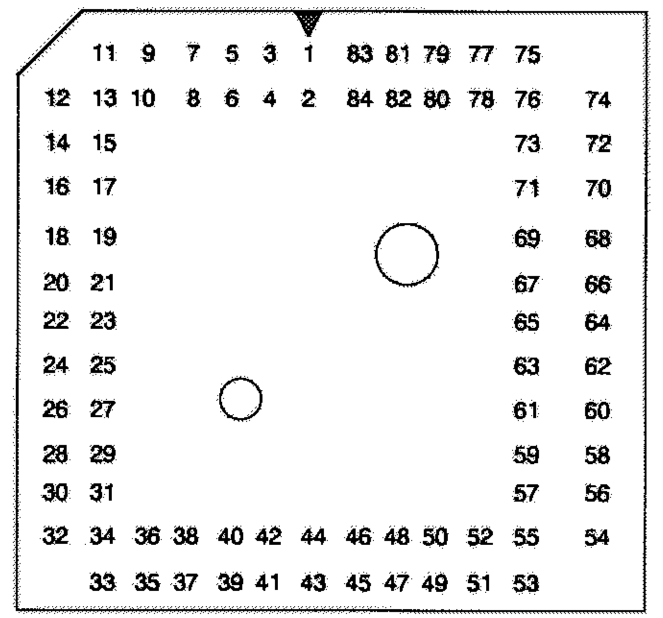
P803

1 SYSTEM GND (AUDIO GND)
2 SYSTEM GND (AUDIO GND)
3 +9.6V
4 SECURE RX AUDIO
5 TX AUDIO
6 RAW TX AUDIO
7 CODED MOD AUDIO
8 LOCAL AUDIO
9 HSR OUT
10 LOGIC GND
11 HSR IN
12 LOGIC GND
13 HSR CLK
14 LOGIC GND
15 HSR SYNC
16 LOGIC GND
17 BD3*
18 BD2*
19 BD1*
20 BD0*
21 BA3
22 BA2
23 BA1
24 BA0
25 DS*
26 SPARE
27 QUAD AUDIO
28 INBOUND MRTI
29 IPCB
30 U/D*
31 INC*
32 CODED MOD CS*
33 EXPANSION RESET*
34 SECURE ALERT TONES
35 SECURE RX CS*
36 SPARE
37 BATTERY GND
38 SPARE
39 +5V
40 SYSTEM GND (AUDIO GND)

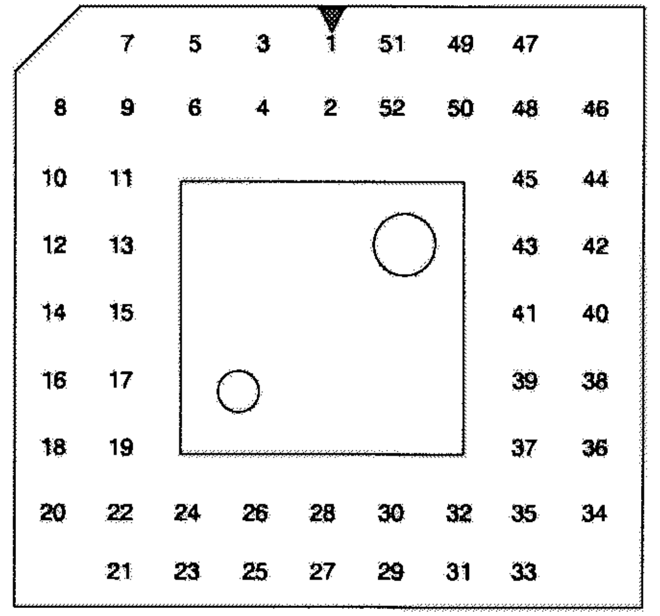
J4001

1 CI KEY
2 KID
3 CI WE*
4 CI GND*
5 EXT KR*
6 GND

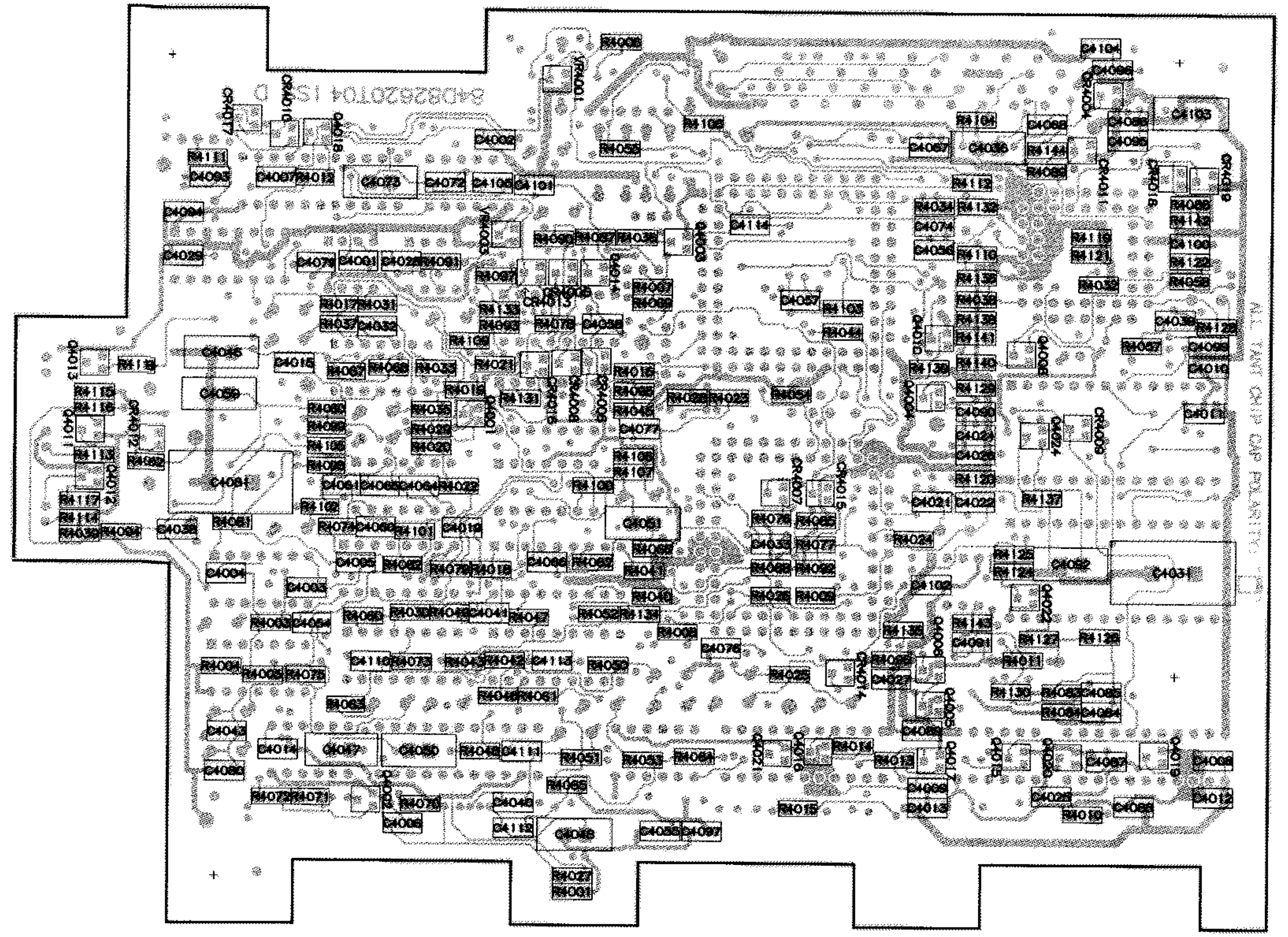
ASTERISK (*) INDICATES ACTIVE LOW STATE



ASIC SOCKET DETAIL



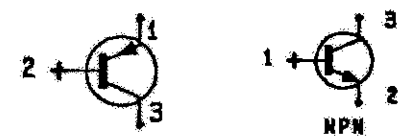
µP SOCKET DETAIL



SHOWN FROM SOLDER SIDE

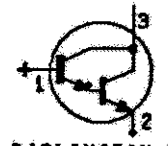
BD-TEPS-47412-A

OL-TEPS-47413-A

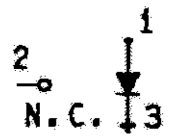


PNP
481105A08
481105B08
481105C08

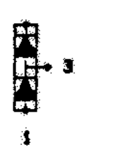
NPN
4811056A03
4811056B03
4811056C03
4811056C21



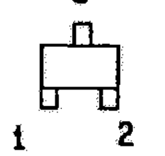
DARLINGTON NPN
4811056A23
4811056B23
4811056C23



DIODE
4811058A11
4811058B11
4811058C11
4805129M41
4811058A04
4811058B04
4811058C04



DUAL DIODE
4884336R03

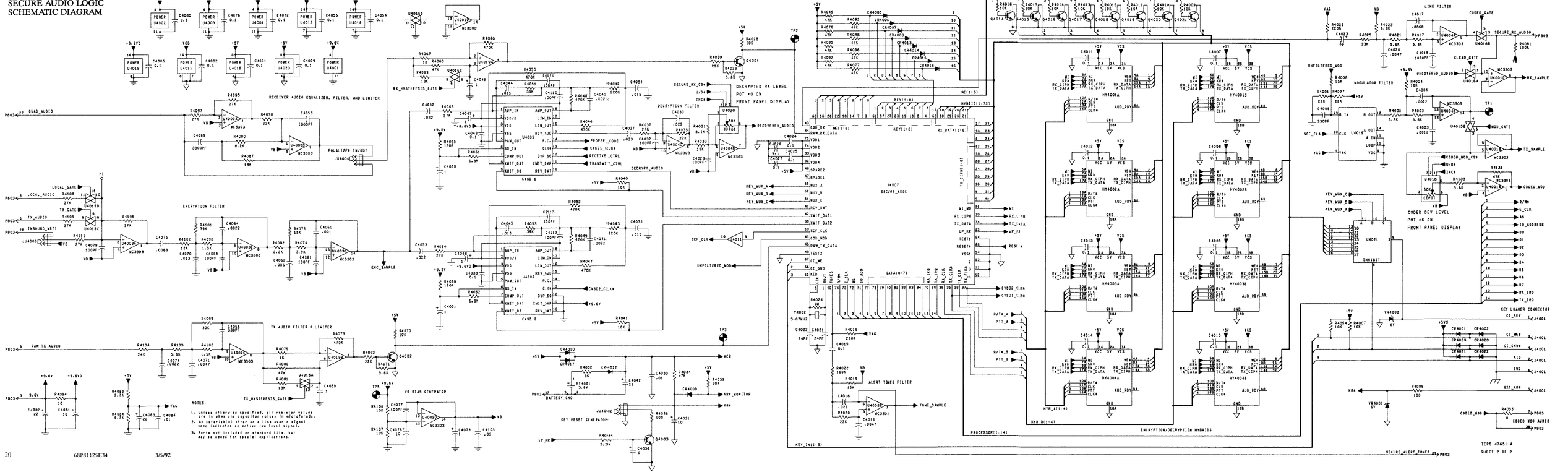


STANDARD SOT PACKAGE PIN-OUT

SECURE AUDIO SCHEMATIC DIAGRAM ON NEXT PAGE

SECURE MODULE

MODEL TLN3045C
SECURE AUDIO LOGIC
SCHEMATIC DIAGRAM



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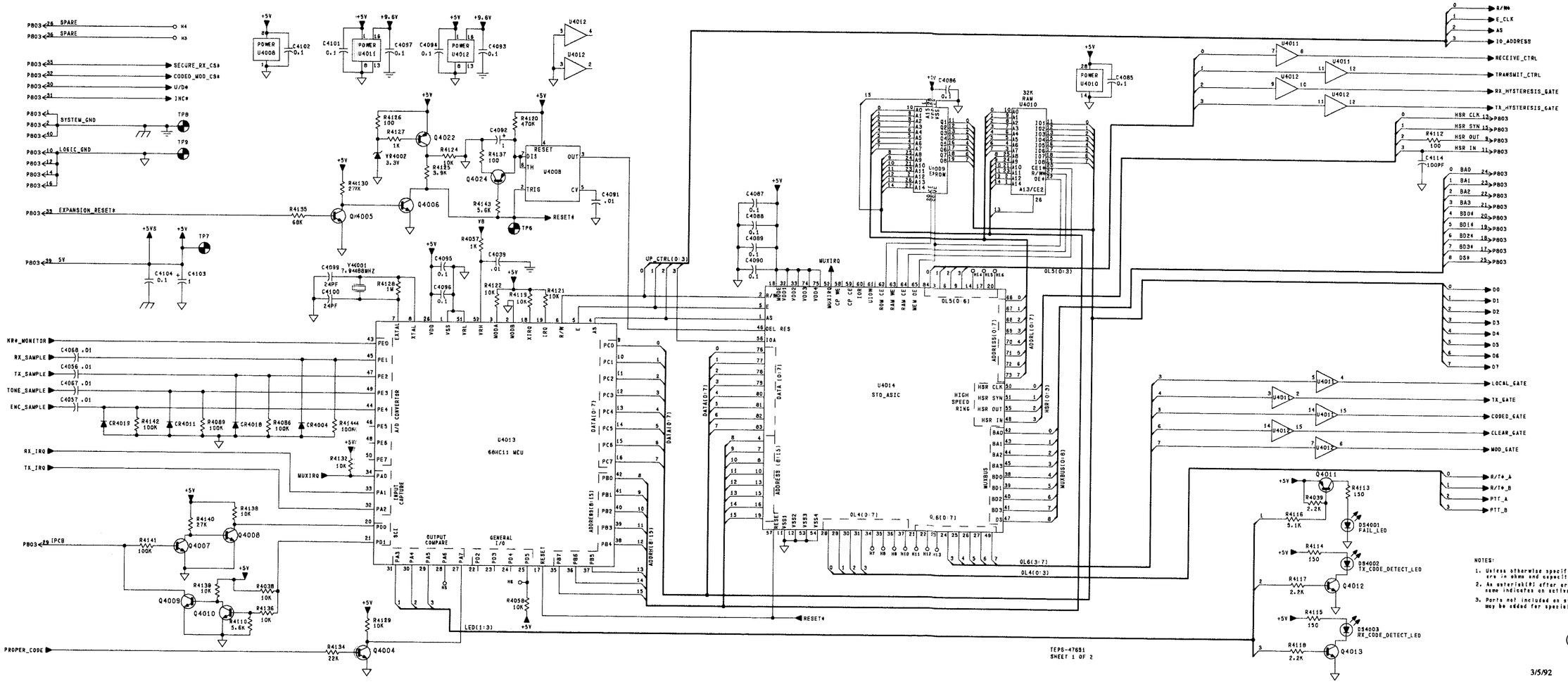
SECURE MODULE
MODEL TLN3045C
SECURE AUDIO LOGIC
SCHEMATIC DIAGRAM



NOTES:
1. Unless otherwise specified, all resistor values are in ohms and capacitor values in microfarads.
2. An asterisk(*) after or a line over a signal name indicates an active low level signal.
3. Parts not included on standard kits, but may be added for special applications.

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(Page 22 is blank)

TRN9999A Secure Board PL-11219-B

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		capacitor, fixed
C4001, C4002	2113741B69	0.1 uF, ±5%; 50V
C4003	2113740B74	1200 pF, ±5%; 50V
C4004	2113740B80	2200 pF, ±5%; 50V
C4005	2113741B69	0.1 uF, ±5%; 50V
C4006	2113740B61	330 pF, ±5%; 50V
C4007 thru 4014	2113741B69	0.1 uF, ±5%; 50V
C4015	2113740B73	1000 pF, ±5%; 50V
C4016	0811017A06	470 pF, ±5%; 50V
C4017	0811017A07	6800 pF, ±5%; 50V
C4018	0811051A09	0.022 uF, ±5%; 63V
C4019	2113741B69	0.1 uF, ±5%; 50V
C4020	0811017A06	470 pF, ±5%; 50V
C4021, C4022	2113740B34	24 pF, ±5%; 50V
C4023	2313748G13	22 uF, ±20%; 25V
C4024 thru 4027	2113741B69	0.1 uF, ±5%; 50V
C4028	2113740B49	100 pF, ±5%; 50V
C4029	2113741B69	0.1 uF, ±5%; 50V
C4030	0811051A09	0.022 uF, ±5%; 63V
C4031	2311049A19	10 uF, ±10%; 25V
C4032	2113740B49	100 pF, ±5%; 50V
C4033	2113741B69	0.1 uF, ±5%; 50V
C4034, C4035	0811051A08	0.015 uF, ±5%; 63V
C4036	2311049A08	1 uF, ±10%; 35V
C4037	0811051A10	0.033 uF, ±5%; 63V
C4038	2113741B69	0.1 uF, ±5%; 50V
C4040,4041	2113740B80	2200 pF, ±5%; 50V
C4042	2313748G13	22 uF, ±20%; 25V
C4043	2113741B69	0.1 uF, ±5%; 50V
C4044, C4045	0811051A08	0.015 uF, ±5%; 63V
C4046 thru 4048	2311049A08	1 uF, ±10%; 35V
C4050, C4051	2311049A08	1 uF, ±10%; 35V
C4052, C4053	0811051A09	0.022 uF, ±5%; 63V
C4054, C4055	2113741B69	0.1 uF, ±5%; 50V
C4056, C4057	2113741B45	0.01 uF, ±5%; 50V
C4058	2113740B73	1000 pF, ±5%; 50V
C4059	2311049A08	1 uF, ±10%; 35V
C4060	2113740B73	1000 pF, ±5%; 50V
C4061	2113740B49	100 pF, ±5%; 50V
C4062	0811051A23	0.056 uF, ±5%; 1V
C4063	2311049A08	1 uF, ±10%; 35V
C4064	2113740B80	2200 pF, ±5%; 50V
C4065	2113740B49	100 pF, ±5%; 50V
C4066	2113740B61	330 pF, ±5%; 50V
C4067, C4068	2113741B45	0.01 uF, ±5%; 50V
C4069	0811017A05	3300 pF, ±5%; 50V
C4070	0811051A10	0.033 uF, ±5%; 63V
C4071	0811017A06	470 pF, ±5%; 50V
C4072	2113741B69	0.1 uF, ±5%; 50V
C4073	2311049A08	1 uF, ±10%; 35V
C4074	2113740B80	2200 pF, ±5%; 50V
C4075	0811017A07	6800 pF, ±5%; 50V
C4076	2113741B69	0.1 uF, ±5%; 50V
C4077	2113740B49	100 pF, ±5%; 50V
C4078	2311049A19	10 uF, ±10%; 25V
C4079	2113740B49	100 pF, ±5%; 50V

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		capacitor, fixed: (cont.)
C4080	2113741B69	0.1 uF, ±5%; 50V
C4081	2311049A19	10 uF, ±10%; 25V
C4082	2313748G13	22 uF, ±20%; 25V
C4084 thru 4090	2113741B69	0.1 uF, ±5%; 50V
C4091	2113741B45	0.01 uF, ±5%; 50V
C4092	2311049A08	1 uF, ±10%; 35V
C4093 thru 4097	2113741B69	0.1 uF, ±5%; 50V
C4099, C4100	2113740B34	24 pF, ±5%; 50V
C4101, C4102	2113741B69	0.1 uF, ±5%; 50V
C4103	2311049A08	1 uF, ±10%; 35V
C4104, C4105	2113741B69	0.1 uF, ±5%; 50V
C4110 thru 4114	2113740B49	100 pF, ±5%; 50V
		diode: (see note)
CR4004 thru 4019	4805129M41	silicon
		light emitting diode: (see note)
DS4001	4888245C24	red
DS4002, DS4003	4888245C23	yellow
		connector:
J4001	2882041P01	plug: 6-contact
		connector:
P803	- -	plug: 40-contact (p/o Cable Assembly 3083139N23)
		jumper:
JU4002 thru 4004	2880002R03	plug: 3-contact
		transistor: (see note)
Q4001 thru 4010	4811056A03	NPN
Q4011	4811056A08	PNP
Q4012 thru 4021	4811056A03	NPN
Q4022	4811056A08	PNP
Q4024	4811056A08	PNP
		resistor, fixed:
R4001	0611077B07	22K, ±5%; 1/8W
R4002	0611077A74	1K, ±5%; 1/8W
R4003	0611077A92	5.6K, ±5%; 1/8W
R4004	0611077B05	18K, ±5%; 1/8W
R4005	0611077A96	8.2K, ±5%; 1/8W
R4006	0611077A50	100 ohms, ±5%; 1/8W
R4007	0611077A98	10K, ±5%; 1/8W
R4008	0611077B03	15K, ±5%; 1/8W
R4009 thru 4016	0611077A98	10K, ±5%; 1/8W
R4017	0611077A92	5.6K, ±5%; 1/8W
R4018	0611077B31	220K, ±5%; 1/8W
R4019	0611077B03	15K, ±5%; 1/8W
R4020	0611077B07	22K, ±5%; 1/8W
R4021	0611077A92	5.6K, ±5%; 1/8W
R4022	0611077B23	100K, ±5%; 1/8W
R4023	0611077A94	6.8K, ±5%; 1/8W
R4024	0611077B47	1 meg, ±5%; 1/8W
R4025	0611077B11	33K, ±5%; 1/8W
R4026	0611077B31	220K, ±5%; 1/8W

TRN9999A Secure Board PL-11219-B

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		resistor, fixed: (cont.)
R4027	0611077B07	22K, ±5%; 1/8W
R4028	0611077A98	10K, ±5%; 1/8W
R4029	0611077A92	5.6K, ±5%; 1/8W
R4030	0611077B07	22K, ±5%; 1/8W
R4031	0611077A91	5.1K, ±5%; 1/8W
R4032	0611077A98	10K, ±5%; 1/8W
R4033	0611077B03	15K, ±5%; 1/8W
R4034	0611077B15	47K, ±5%; 1/8W
R4035	0611077B07	22K, ±5%; 1/8W
R4036	0611077A50	100 ohms, ±5%; 1/8W
R4037	0611077B07	22K, ±5%; 1/8W
R4038	0611077A98	10K, ±5%; 1/8W
R4039	0611077A82	2.2K, ±5%; 1/8W
R4040, R4041	0611077A98	10K, ±5%; 1/8W
R4042, R4043	0611077B31	220K, ±5%; 1/8W
R4044	0611077A82	2.2K, ±5%; 1/8W
R4045	0611077B15	47K, ±5%; 1/8W
R4046 thru 4050	0611077B39	470K, ±5%; 1/8W
R4051	0611077B13	39K, ±5%; 1/8W
R4052	0611077B39	470K, ±5%; 1/8W
R4053	0611077B13	39K, ±5%; 1/8W
R4054	0611077A98	10K, ±5%; 1/8W
R4060	0611077B39	470K, ±5%; 1/8W
R4061, R4062	0611077A94	6.8K, ±5%; 1/8W
R4063, R4064	0611077B09	27K, ±5%; 1/8W
R4065, R4066	0611077B25	120K, ±5%; 1/8W
R4067	0611077A74	1K, ±5%; 1/8W
R4068	0611077B15	47K, ±5%; 1/8W
R4069	0611077B02	13K, ±5%; 1/8W
R4070	0611077A98	10K, ±5%; 1/8W
R4071	0611077A92	5.6K, ±5%; 1/8W
R4072	0611077B07	22K, ±5%; 1/8W
R4073	0611077B39	470K, ±5%; 1/8W
R4074	0611077A88	3.9K, ±5%; 1/8W
R4075	0611077B03	15K, ±5%; 1/8W
R4076, R4077	0611077B15	47K, ±5%; 1/8W
R4078	0611077B07	22K, ±5%; 1/8W
R4079	0611077A74	1K, ±5%; 1/8W
R4080	0611077B15	47K, ±5%; 1/8W
R4081	0611077B02	13K, ±5%; 1/8W
R4082	0611077A82	2.2K, ±5%; 1/8W
R4083, R4084	0611077A92	5.6K, ±5%; 1/8W
R4085	0611077B15	47K, ±5%; 1/8W
R4086	0611077B23	100K, ±5%; 1/8W
R4087	0611077B05	18K, ±5%; 1/8W
R4088	0611077B15	47K, ±5%; 1/8W
R4089	0611077B23	100K, ±5%; 1/8W
R4090	0611077A96	8.2K, ±5%; 1/8W
R4091	0611077B23	100K, ±5%; 1/8W
R4092	0611077B15	47K, ±5%; 1/8W
R4093	0611077B09	27K, ±5%; 1/8W
R4094	0611077A26	10 ohms, ±5%; 1/8W
R4095, R4096	0611077B15	47K, ±5%; 1/8W
R4097	0611077B09	27K, ±5%; 1/8W
R4098	0611077A78	1.5K, ±5%; 1/8W
R4099	0611077B10	30K, ±5%; 1/8W

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		resistor, fixed: (cont.)
R4100	0611077A78	1.5K, ±5%; 1/8W
R4101	0611077B13	39K, ±5%; 1/8W
R4102	0611077B01	12K, ±5%; 1/8W
R4103	0611077A92	5.6K, ±5%; 1/8W
R4104	0611077B08	24K, ±5%; 1/8W
R4105	0611077B09	27K, ±5%; 1/8W
R4106, R4107	0611077A98	10K, ±5%; 1/8W
R4108, R4109	0611077B09	27K, ±5%; 1/8W
R4110	0611077A92	5.6K, ±5%; 1/8W
R4111	0611077B09	27K, ±5%; 1/8W
R4112	0611077A50	100 ohms, ±5%; 1/8W
R4113 thru 4115	0611077A54	150 ohms, ±5%; 1/8W
R4116	0611077A91	5.1K, ±5%; 1/8W
R4117, R4118	0611077A82	2.2K, ±5%; 1/8W
R4119	0611077A98	10K, ±5%; 1/8W
R4120	0611077B39	470K, ±5%; 1/8W
R4121, R4122	0611077A98	10K, ±5%; 1/8W
R4124	0611077A98	10K, ±5%; 1/8W
R4125	0611077A88	3.9K, ±5%; 1/8W
R4126	0611077A50	100 ohms, ±5%; 1/8W
R4127	0611077A74	1K, ±5%; 1/8W
R4128	0611077B47	1 meg, ±5%; 1/8W
R4129	0611077A98	10K, ±5%; 1/8W
R4130	0611077B09	27K, ±5%; 1/8W
R4132	0611077A98	10K, ±5%; 1/8W
R4134	0611077B07	22K, ±5%; 1/8W
R4135	0611077B19	68K, ±5%; 1/8W
R4136	0611077A98	10K, ±5%; 1/8W
R4138, R4139	0611077A98	10K, ±5%; 1/8W
R4140	0611077B09	27K, ±5%; 1/8W
R4141, R4142	0611077B23	100K, ±5%; 1/8W
R4144	0611077B23	100K, ±5%; 1/8W
		test point:
TP1 thru TP3	2910271A15	terminal pin
TP5 thru TP9	2910271A15	terminal pin
		integrated circuit: (see note)
U4002 thru 4004	5113819D04	type MC3303P
U4007	5184494R04	ASIC Encryption
U4008	5184320A35	Timer
U4010	5184944N51	RAM 8Kx8 Bit
U4011, U4012	5184704M19	Shift Hex Level Log Level Control
U4013	5113802A01	A/D w/Switch Control Interface
U4014	5184494R03	ASIC Station Control
U4015, U4016	5184887K73	Quad Bilateral Switch
U4018	5182802R24	Digitally Controlled 50K Potentiometer
U4019	5183977M42	Capacitor Switched Filter
U4020	5182802R24	Digitally Controlled 50K Potentiometer
U4021	5184887K26	Analog Mux/Demux
		voltage regulator: (see note)
VR4001	4811058A04	Zener 6V
VR4002	4882256C26	Zener 3.3V

TRN9999A Secure Board PL-11219-B

REFERENCE SYMBOL	PART NUMBER	DESCRIPTION
		voltage regulator: (see note)(cont.)
VR4003	4811058A04	Zener 6V
		crystal: (see note)
Y4001	4880113K04	7.948 MHZ
Y4002	4882611M12	oscillator: 3.072 MHZ
		non-referenced items:
	0980082P05	SOCKET, IC: 18-contact (2 used with U4005 & U4006)
	0982449T01	SOCKET, IC: 52-contact (used with U4013)
	0982449T03	SOCKET, IC: 84-contact (2 used with U4007 & U4014)
	0982483T01	SOCKET, IC: 18-contact (4 used with HY4001 thru HY4004)
	0982483T02	SOCKET, IC: 16-contact (4 used with HT4001 thru HT4004)
	0982808R10	SOCKET, IC: 28-contact (used with U4009)
	0983662T01	SOCKET, contact (3 used)
	0984181L01	SHORTING JUMPER: 2-contact (3 used with JU4002 thru JU4004)
	3083139N23	CABLE ASSEMBLY, flat, 40-conductor: includes connector P803
	4380054K01	SPACER, pcb support (4 used)
	5483865R01	LABEL, bar code: 1/4" wide, white
	5484960T01	LABEL, bar code: 6.3x12.7MM, white
	7505295B01	PAD, crystal (2 used with Y4001 & Y4002)

NOTE: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part number.

END OF DOCUMENT