TX/RX FREQUENCY SYNTHESIS

1. INTRODUCTION

1.1 GENERAL INFORMATION

The TRN7006A uniboard contains the transmit and receive frequency synthesizers. These synthesizers are of the same basic design but have some unique differences. Since the transmit synthesizer is the more complicated of the two, it will be used for operational explanation. The major difference between the two synthesizers is that the transmit synthesizer contains the modulation circuitry. Sections which are required for modulation capabilities will be marked as TX ONLY. When a transmit synthesizer or VCO component is designated, the corresponding receive synthesizer or VCO component can be found in Tables 1 and 2.

1.2 DESCRIPTION

The *MSF 5000/MSF 10000* frequency synthesizers generate the transmit carrier and receive injection signals. Each synthesizer employs a phase-locked loop (PLL) to lock a voltage controlled oscillator (VCO) to a precision reference frequency to produce the desired frequency. The major functional blocks which are located on the uniboard are the programmable dividers, phase detector, and adaptive loop filter. The transmit and receive VCOs are separate assemblies which are located in the rf tray.

2. THEORY OF OPERATION

2.1 PHASE-LOCKED LOOP OPERATION

Various output frequencies are generated by the synthesizer using a single negative feedback loop. The phase difference between two signals at the phase detector input is used to control the VCO output frequency. The input waveforms compared are the same reference frequency. The input waveforms compared are the reference frequency signal and the loop pulse signal.

Table 1. TX Synthesizer Reference Designations to RX Synthesizer Reference Designations Cross-Reference

Transmit Synthesizer	Receive Synthesizer
C343	C283
C346	C286
C348	C288
C352	C292
C353	C293
C354	C294
C360	C306
C361	C307
C362	C308
Q322	Q262
Q324	Q264
Q325	Q265
Q326	–
U322	U262
U323	U263
U324	U264
U325	U265

Table 2. TX VCO Reference Designations to RX VCO Reference Designations Cross-Reference

Transmit VCO	Receive VCO
A26	A51
C29	C53
C32	C54
C33	–
CR28	CR53
CR29	CR54
J323	J263
P323	P263
P324	P264
Q30	Q53
Q31	Q54
W104	W101
W106	W103

technical writing services
1301 E. Algonquin Road, Schaumburg, IL 60196

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The stable 14.4 MHz reference signal is generated by the KXN1096A Crystal Oscillator Element. The reference frequency divider, U322, divides the 14.4 MHz signal down to a 6.25 kHz square wave. The loop pulse signal is the negative feedback signal of the PLL which is created by dividing the VCO output frequency by the programmable loop divide number, N.

Both the loop and reference signals are applied to the phase detector, which generates a dc control voltage proportional to the phase difference between the loop and reference frequencies. The phase detector output is passed through the adaptive loop filter, which damps the loop transient response and attenuates noise and spurs, to drive the VCO steering line. The steering line increases or decreases the VCO output frequency as its voltage level rises or falls. If, for instance, the VCO output frequency increases, the loop signal frequency also increases, causing a phase change at the phase detector. The phase detector then drops its dc output in accordance with the phase slippage, and the steering line moves the VCO frequency back down.

2.2 DIVIDER

The 14.4 MHz signal produced by the reference synthesizer is divided by the programmable reference divider in U322. The internal bits R_1 and R_2 in U322 determine the reference signal frequency (6.25 kHz).

The VCO output frequency is divided by the programmable loop divider to produce the loop pulse signal. The dual modulus divider divides by 63 or 64 and is located with the reference divider, in U322. Divide-by-64 is started with the rising edge of the loop pulse and continues until the internal "A" counter reaches zero. The loop pulse is then sent low and the divider divides by 63 until the internal "B" counter goes to zero. The loop pulse then goes high and another cycle begins.

2.3 SYNTHESIZER PROGRAMMING FROM MICROPROCESSOR

For data loading into divider U322, the microprocessor reads data from the code plug on the station control board, and multiplexes the information into six 4-bit words. Each word is loaded into U322 as four lines of data (SD_0 through SD_3) and a corresponding three lines of address (SA_0 through SA_2), so that the words are properly de-multiplexed in U322.

The received data bits inform divider U322 of the appropriate numbers for the "A" and "B" counters for the desired PLL output frequency.

2.4 PHASE DETECTOR

Phase detector U323 generates a dc output signal proportional to the phase difference between the reference and loop pulse signals sent from divider U322. The phase difference is measured by the phase detector. It turns ramp current source Q322 on when the reference signal goes high and switches Q322 off at the leading edge of the loop pulse signal. The current generated during this interval charges C348, forming a voltage ramp.

The ramp voltage is then held constant for a time interval determined by C343, allowing hold capacitor C346 to charge to the ramp voltage level. Ramp capacitor C348 is discharged at the end of the hold interval in preparation for another ramp sequence that begins with the next reference signal leading edge.

The hold capacitor is discharged through a push-pull output transistor pair via a high-to-low impedance output buffer. This creates the phase detector output signal.

When the reference-to-loop-pulse phase slippage is too great for the ramp capability, the ramp remains at a high or low limit. The VCO cannot be steered to the intended frequency and an unlocked state occurs. The phase detector then issues an "adapt" signal (on the ADAPT and $\overline{\text{ADAPT}}$ lines). The ADAPT line control voltage switches the analog gates in the adaptive filter to the "normal " mode or "adapt" mode, as well as forcing lock indicator Q234 into a no-lock, open-collector condition The "adapt" mode is automatically attained whenever the phase detector encounters a "change frequency" positive pulse from U322. The duration of a single adapt duration is 12 msec, which is hard-wire controllable at the phase detector. Adapt cycles continue until reference and loop pulse signals are again locked in frequency.

2.5 ADAPTIVE LOOP FILTER

The adaptive loop filter is used for effective loop lock. When the PLL is unlocked, or when a "change frequency" pulse is sent to the synthesizer from control, the ADAPT and $\overline{\text{ADAPT}}$ lines are sent high and low, respectively, by the phase detector. Analog gates U324A, B, and C are switched closed, shorting the phase detector output to the steering line, keeping C352 uncharged, and charging C353 quickly to the new steering voltage. Gate U324D is switched open, detaching the loop filter output from the steering line. In this mode, the loop filter is essentially out of the PLL, and fast lock (due to reduced damping) is possible.

When the loop reaches its new frequency, (at the end of the last adapt cycle, ADAPT goes low and $\overline{\text{ADAPT}}$ goes high. Analog gates U324A, B, and C are then switched open., returning the loop filter to its normal connection to the output of U323 and breaking the direct connection between this output and the steering line. Gate U324D re-connects the loop filter output to the steering line. During this switching, C354 remains charged to the new phase detector output voltage, keeping the VCO tuned to the new frequency.

The transmit loop filter, when in normal operation, has a natural frequency of 15 Hz Tx or 75 Hz Rx and a third

order Integral-Times-Absolute-Value-of-Error response, a method for minimizing transients. The filter damps steering line excursion due to voltage increments of the phase detector output and attenuates reference signal spurs and noise.

2.6 SUPER FILTER

Because the VCO requires a very pure dc supply voltage, an ultra-low-pass filter U325 is used to provide the VCO with a very low noise supply output voltage. Any ripple or noise present on the +9.6 V supply line is removed by the filter, preventing unwanted modulation of the VCO. A 1 V drop occurs across the filter. The U325 output voltage is +8.6 V.

The super filter consists of a low-pass filter, an error amplifier, and external series-pass transistor Q325. The +9.6 V supply is connected to U325-1 as well as to the emitter of Q325. Internally, the input from U325-1 passes through a low-pass filter to the non-inverting input of the error amplifier. Capacitor C360, connected to U325-2, forms part of the low-pass filter. The output line (also connected to the collector of Q325) is fed back to the inverting input of the error amplifier through U325-4. The error amplifier output is connected to the base of Q325-4. The error amplifier output is connected to the base of Q325 via U325-3 and is used to control the conduction of this transistor. These connections enable the super filter to compare the output line voltage with the filtered input line voltage and to increase or decrease the conduction of Q325 to remove any ripple or noise present on the VCO supply line. The super filter output itself is filtered by C361 and C362 before being routed from the synthesizer to the VCO.

2.7 ISOLATION BUFFER (TX ONLY)

The isolation buffer stage applies the transmit VCO rf signal to the first stage of the intermediate power amplifier (IPA). The buffer stage consists of input and output matching circuits and an active device Q326, biased for class A operation. The buffer ensures isolation between the VCO output and the IPA, and prevents pulling of the VCO output frequency during transmitter key-up.

2.8 DPL MODULATION COMPENSATION (TX ONLY)

The DPL modulation compensation circuit of the transmit sysnthesizer enables low-frequency modulation (DPL) to be transmitted without being "tracked out" by the loop. When the VCO is modulated by DPL, the modulation appears as an error signal at the phase detector, after it is divided down and compared to the reference signal. Unless compensated, this error signal passes through the loop filter and modulates the steering line, distorting the intended DPL modulation.

The dpl modulation compensation circuit sends a cancellation signal to the phase detector output buffer summing point U323-11. This cancellation signal is the original low-frequency DPL signal after being integrated, delayed, and inverted. Thus, DPL modulation of the VCO results without loop tracking interference.

2.9 VOLTAGE CONTROLLED OSCILLATOR (VCO)

Each *MSF 5000/MSF 10000* radio contains a transmit and receive VCO. The transmit VCO operates from 146-174 MHz (132-158 MHz with C367 option) and produces the frequency modulated (FM) exciter frequencies. The receiver VCO operates from 135.3-163.3 MHz (121.3-147.3 MHz with C367 option) and produces the receiver injection frequencies.

2.9.1 Oscillator Circuit

The VCO uses a grounded-gate Colpitts oscillator with a FET (Q30) as the amplifying element. A PIN diode band shift switch and varactor diode tuning network allows the VCO to electrically tune the entire operating frequency range in two sub-bands. A feedback network composed of a transmission line and capacitors provide the correct phase and amplitude response to sustain oscillations. A bipolar buffer transistor (Q31) is lightly coupled to the oscillator circuit to provide a feedback signal to the PLL and the load pull buffer amp on the uniboard via a coaxial cable W106.

2.9.2 Steering Line Circuit

The steering line circuit determines the VCO operating frequency within a given sub-band. The steering line is driven by the phase detector (U323) and is coupled to the VCO via the adaptive loop filter. The phase detector generates a dc voltage which steers the VCO to the desired operating frequency. The steering line is coupled from the uniboard via P324A-6 of VCO interconnect cable W104 to the VCO feed-through plate A26. This plate contains rf filters that de-couple the VCO circuits from the uniboard circuits. The steering line voltage determines the capacitance of the tuning varactor (CR28,29) which electronically control the oscillator frequency. An increase in steering line voltage decreases varactor capacitance which results in an increase in the oscillator frequency. Conversely, decreasing the steering line voltage decreases the oscillator frequency.

2.9.3 Bandshift Switch Circuit

The bandshift switch circuit utilizes a PIN diode to electronically vary the effective length of the main transmission line. This is accomplished by switching C29 and C32 in parallel with the transmission line. This provides two frequency sub-bands. A control voltage generated by the divider IC (U322-20) is applied to a high impedance transistor driver network to bias the PIN diode on or off depending on the desired sub-band. When the PIN is forward biased, the oscillator operates in the lower sub-band

and when the PIN is reverse-biased the oscillator operates in the upper sub-band.

2.9.4 Modulation Line (TX Only)

The VCO is directly frequency modulated by the transmit audio signal at TP4 on the station control board. The modulation signal is applied to CR27 via P324A-4 of the VCO interconnect cable W104. C33 couples the modulation circuit to the steering line circuit which maintains the modulation constant as the steering line voltage is changed for different operating frequencies.

3. SYNTHESIZER TROUBLESHOOTING PROCEDURE

3.1 GENERAL

Refer to the Frequency Synthesizer Troubleshooting Chart at the end of this section for a comprehensive procedure for troubleshooting the transit or receive frequency synthesizers.

The major problems that may occur in the transmit frequency synthesizer are:

- synthesizer does not lock
- synthesizer locks on wrong frequency
- excessive reference frequency feed-through (spurs)
- noisy frequency lock
- slow switching response

A summary of the problems and possible causes in the frequency synthesizer is provided in Table 2. Also refer to the other tables that provide pin connections and voltages for the phase detector, divider, pre-scaler, and super filter. Tabular reference designations are shown for components in the Tx Synthesizer. Corresponding reference designations for the Rx Synthesizer can be found in Table 1.

3.2 OPEN LOOP TEST

For this test, the following test equipment is required: frequency counter, signal generator, digital voltmeter, power meter and dual trace oscilloscope. The maintenance and troubleshooting section of this manual has a list of recommended test equipment. These tests are designed to be performed in sequence.

The open loop test consists of the following procedures:

- Loop and reference waveform tests
- Phase detector test
- Adaptive filter test
- VCO frequency test

3.2.1 Loop and Reference Waveform Tests

Remove P323 from the VCO. Connect a signal generator to P323 and set the amplitude of the signal generator to + 10 dBm. Connect one channel of a dual trace scope to REF OUT(U322-5) and the other channel to LOOP PULSE (U322-9). Adjust the oscilloscope such that it triggers on the REF OUT waveform. The oscilloscope trace should be in the chop mode.

Observe the REF OUT waveform and verify that the period is 160 µsec. The waveform should not exhibit any jitter.

Observe the LOOP PULSE waveform as the frequency of the generator is varied from 110–180 MHz. The waveform should move smoothly across the screen without any jitter. The period of the LOOP PULSE should be greater than the REF OUT waveform at 110 MHz and less than the REF OUT waveform at 180 MHz.

If the divider does not pass the above tests, check the divider programming as outlined in the Control Section of this manual. If the divider programming is correct, then check the divider (U322) and the associated circuitry.

3.2.2 Phase Detector Test

Remove P323 from the VCO. Connect a signal generator to P323 and set the amplitude of the signal generator to + 10 dBm. Set the frequency of the generator 30 Mhz below the frequency of the channel selected by station control. Check that the steering line voltage (U323-15) $\geq$ 8.0 V dc. Set the generator frequency to 30 MHz above the programmed frequency. Check that the steering line voltage (U323-15) $\leq$ 1.5 V dc. If the phase detector does not change state, check the phase detector and associated circuitry.

3.2.3 Adaptive Loop Filter Test

Remove P324A from the VCO. Repeat the phase detector test for Vsl $\geq$ 8.0 V dc. The voltage at P324A-6 should be the same as U323-15. If the voltages do not match, check the adaptive loop filter, loop filter control lines (U323-7, 10) and W106.

3.2.4 VCO Frequency Test

Remove P323 from the VCO. Connect a signal generator to P323 and set the amplitude of the signal generator to + 10 dBm. Set the frequency of the generator 30 MHz below the frequency of the channel selected by station control. Check that the steering line voltage (P324A-6) $\geq$ 8.0 V dc. Measure the frequency and power out of the VCO at J323 (verify that P324A is connected to VCO). Refer to Figure 2. For the steering line voltage measured at P324A-6, the measured VCO frequency should be within + 2MHz of the value on the graph for the selected bandshift. Change the generator frequency to 30 MHz above the programmed frequency. Check that the steer-

ing line voltage (P324A-6) $\leq$ 1.5 V dc. Verify the VCO frequency per Figure 2 for the selected bandshift. For each steering line voltage the output power at J323 should be $\geq$ + 7 dBm. If the VCO frequency is not within the limits specified per Figure 1 or the output power is < + 7 dBm, it is defective and must be replaced

WARNING

The signal at P101 is dc coupled. 13.8 V dc is present at P101. When checking the receive synthesizer output take the necessary precautions to prevent damage to test equipment due to the dc voltage.

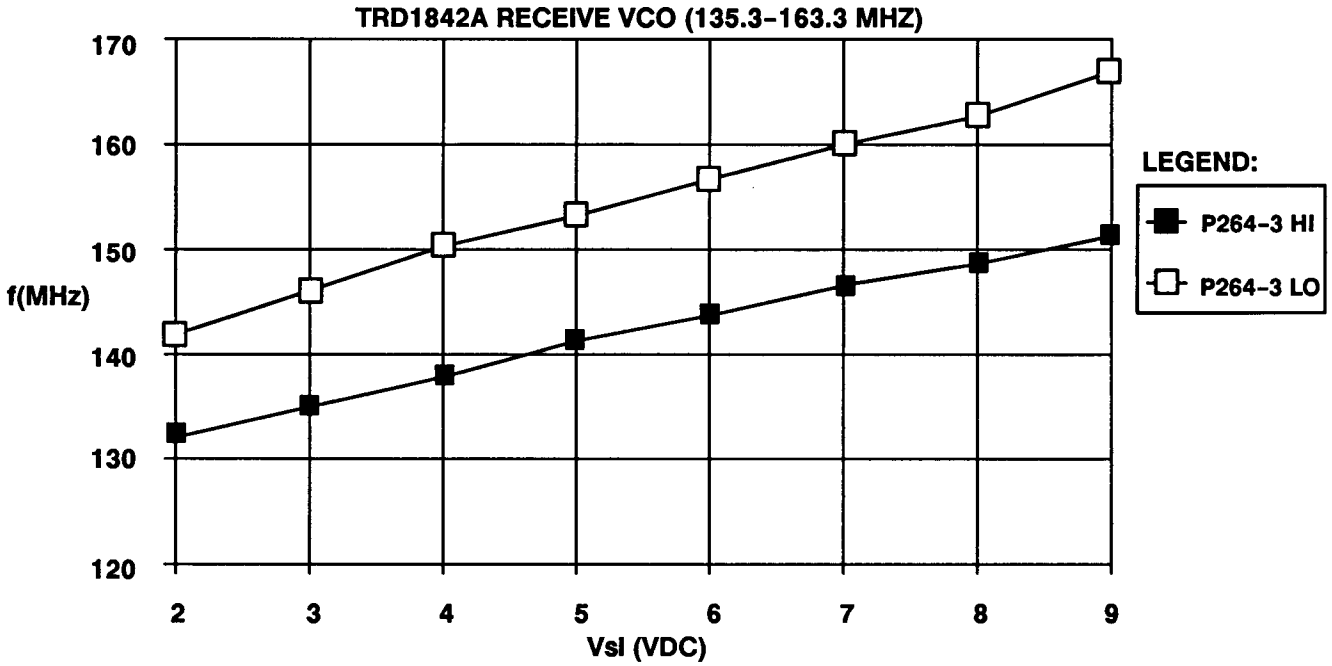


Figure 1. Receive VCO Frequency Chart

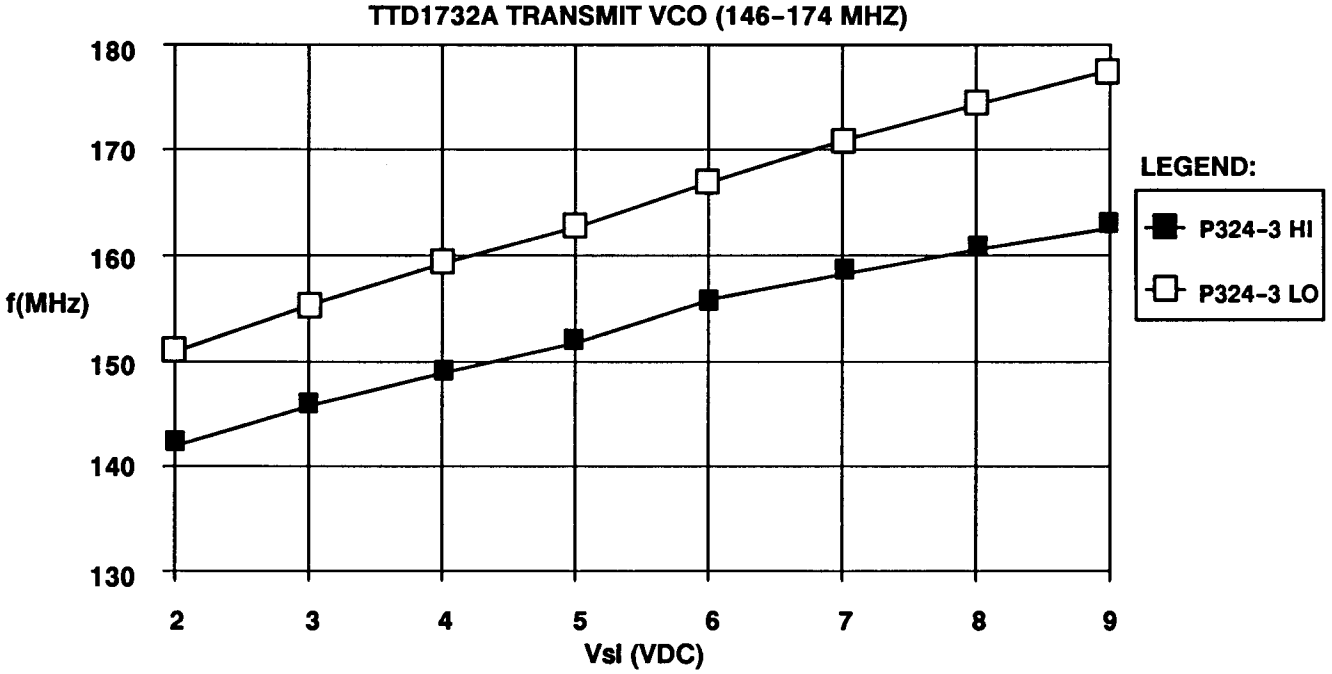


Figure 2. Transmit VCO Frequency Chart

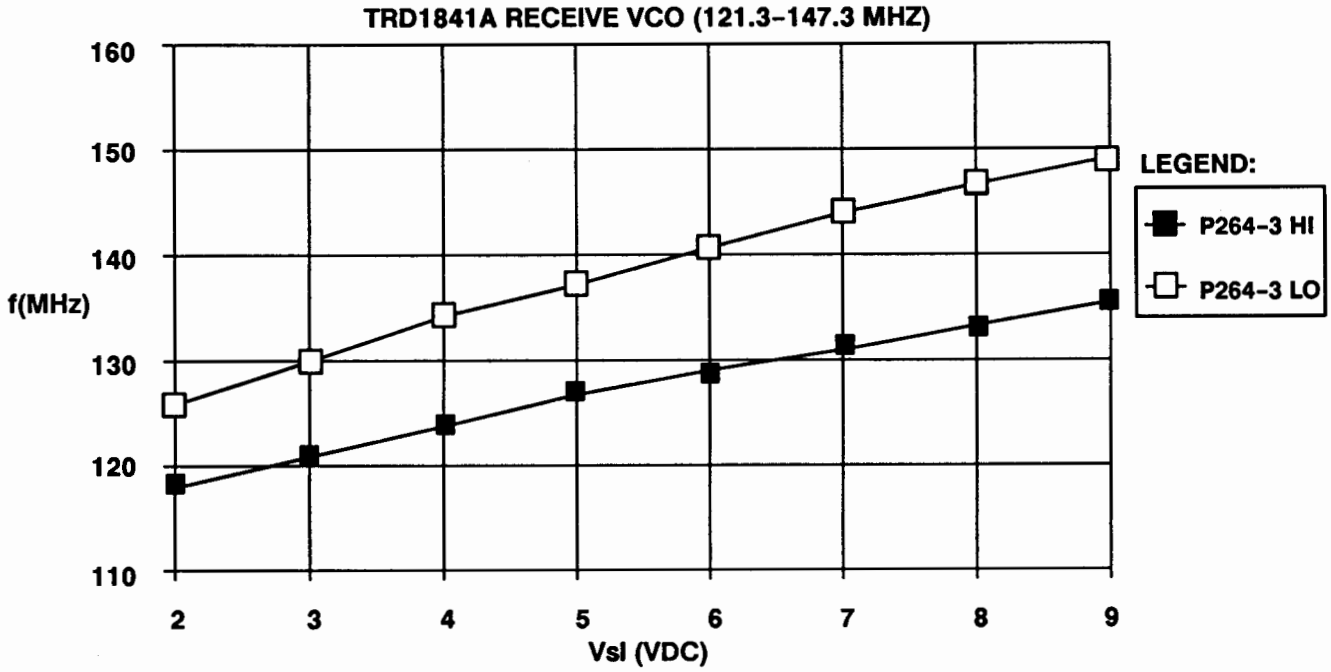


Figure 3. Receive VCO Frequency Chart

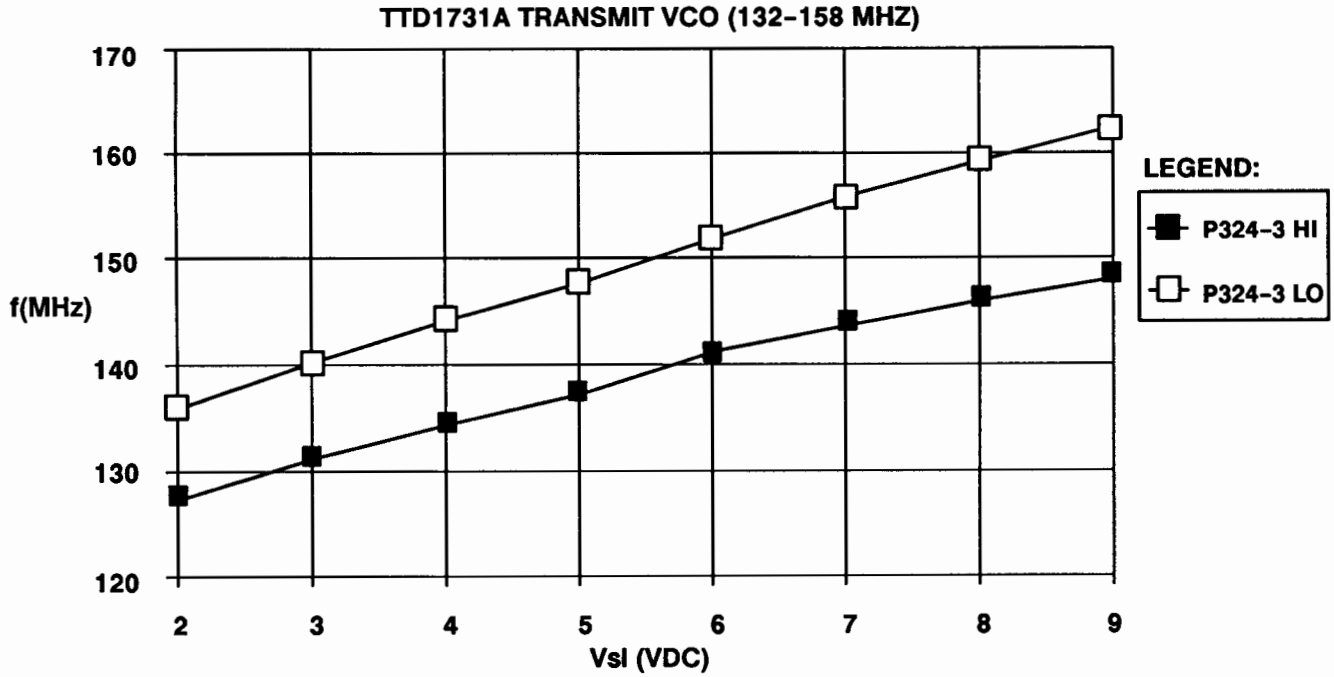


Figure 4. Transmit VCO Frequency Chart

Table 3. Problems and Possible Causes for MSF 5000 Synthesizers

Problem	Possible Source of Trouble
Synthesizer does not lock	Refer to Synthesizer Troubleshooting Chart
Synthesizer does not lock all channels	Refer to Synthesizer Troubleshooting Chart
Synthesizer locks on wrong frequency	Refer to Synthesizer Troubleshooting Chart
Excessive reference frequency feedthru (spurs)	Defective hold capacitors (open or leaky), C346
	Defective ramp capacitor C348
	Defective phase detector U323
	Adaptive filter in ADAPT mode or shorted input to output; guard band shorted to VCO steering line or other adaptive filter mode
Noisy frequency lock	Leaky VCO varactor diodes
	Marginal input level to loop divider U322–25 or reference divider U322
	Loose connection, cold solder joints, or faulty component
	Noisy Q322
	Defective phase detector U323
	Defective reference divider U322 (jittery)
	Noisy +5 V or +9.6 V supplies, noisy super filter output
	Defective adaptive filter (open capacitors)
Slow frequency switching response	Malfuntioning adaptive filter, check U324
	Phase detector U323 gain too low (overdamped response) or too high (underdamped response); check R336, R337, R338, RT321, Q322
	Check ramp slope at U323–24
	Leaky adaptive filter capacitors or transmission gates; check C353, C352, C354, U324
	Leaky VCO varactor diodes

Table 4. Phase Detector U323 Pin Connections and Voltages

Pin No.	Function	To / From	Nominal Voltage
1	high current ground	–	0 V dc
2	REFERENCE IN	from U322–5	0 to 4.3 V square wave (160 µsec period); U323–17, 5 V dc transmit
3	adapt select	–	0 V dc
4	SYNTHESIZER SYNC	to microcomputer	60 µsec positive pulse, 0–5 V at loop pulse rate; equal to pin 2 if pin 7 is low
5	FREQUENCY CHANGE	from U322–18	0.5 V, 11.1 µsec when frequency changes
6	N.C.	–	–
7	ADAPT	to lock transistor via R339	9.6 to 0.6 V single pulse; 12 msec
8	N.C.	–	–
9	N.C.	–	–
10	ADAPT	to adaptive filter	0 to 9 V single pulse; 12 msec
11	mod input	from R369 (U323 only)	3.0 to 6.0 V dc (use high impedance)
12	N.C.	–	–
13	HOLD 2	to C346	1.4 to 8 V dc (use high impedance voltmeter)
14	A+	–	9.6 V dc
15	PHASE DET OUTPUT	to adaptive filter	1.2 to 9.5 V dc (depending on loop output frequency)
16	low current ground	–	0 V dc
17	EXT PNP BASE	to Q232 base	8.9 V dc
18	V_{cc}	from regulator	9.6 V dc
19	RAMP BASE	to Q322 base (ramp generator)	9.1 V dc
20	FILTERED 9.1 V	to R336, RT321, R337, C344	9.1 V dc
21	ramp resistor	to R338, Q322 emitter	8 to 8.7 V dc rectangular wave at reference rate
22	SAMPLE TIMING CAP	to C343	0 to 2 V sawtooth wave at loop pulse rate
23	LOOP IN PULSE	from U322–9 via C340	1.4 V pulse riding oon 1.6 V dc (160 µsec, typical period)
24	RAMP CAP	from C348 and ramp Q322 collector	flat top ramp waveform at reference rate, top voltage 1.4 to 7 V (depending on loop output frequency)

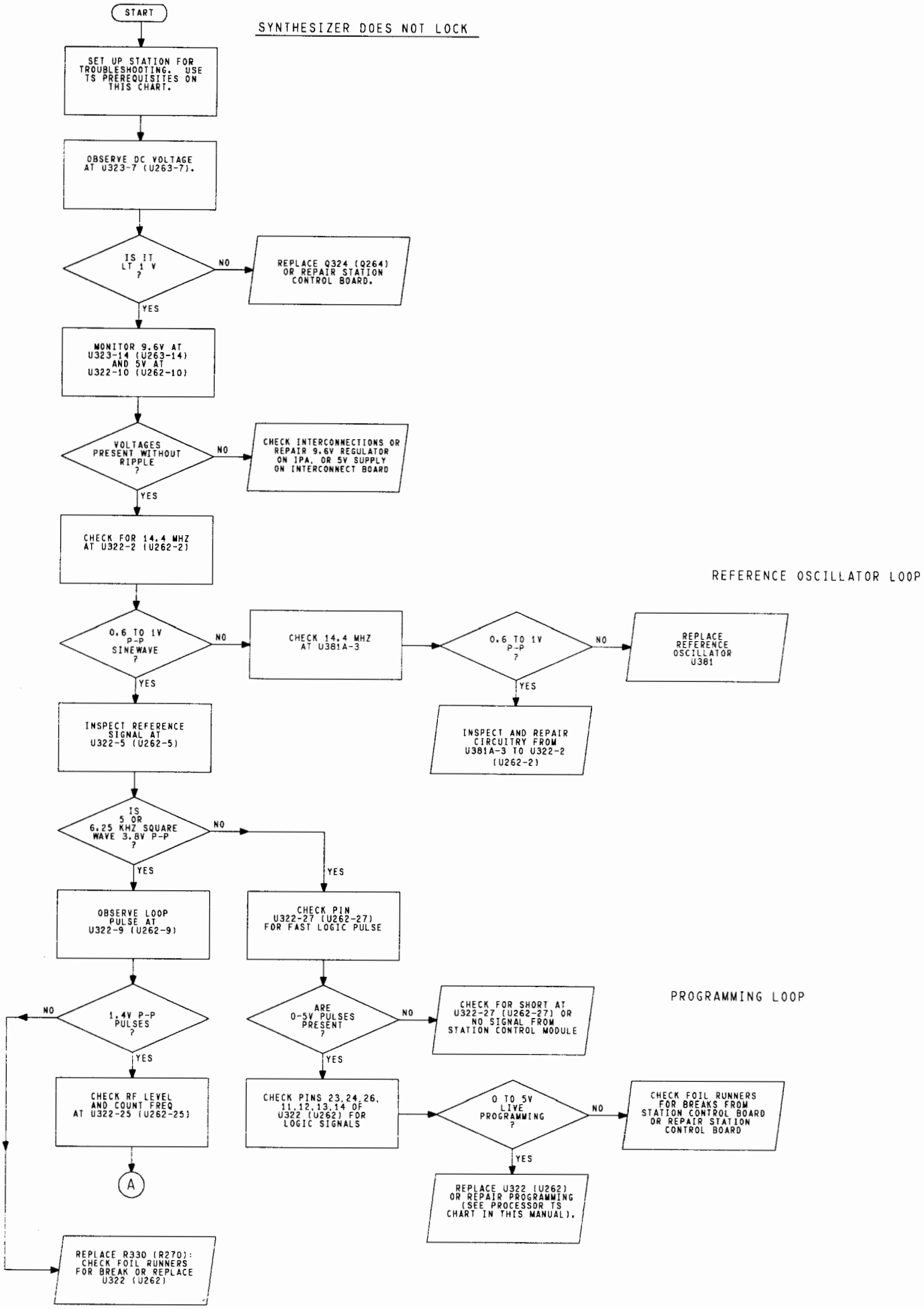
Table 5. Divider U322 Pin Connections and Voltages

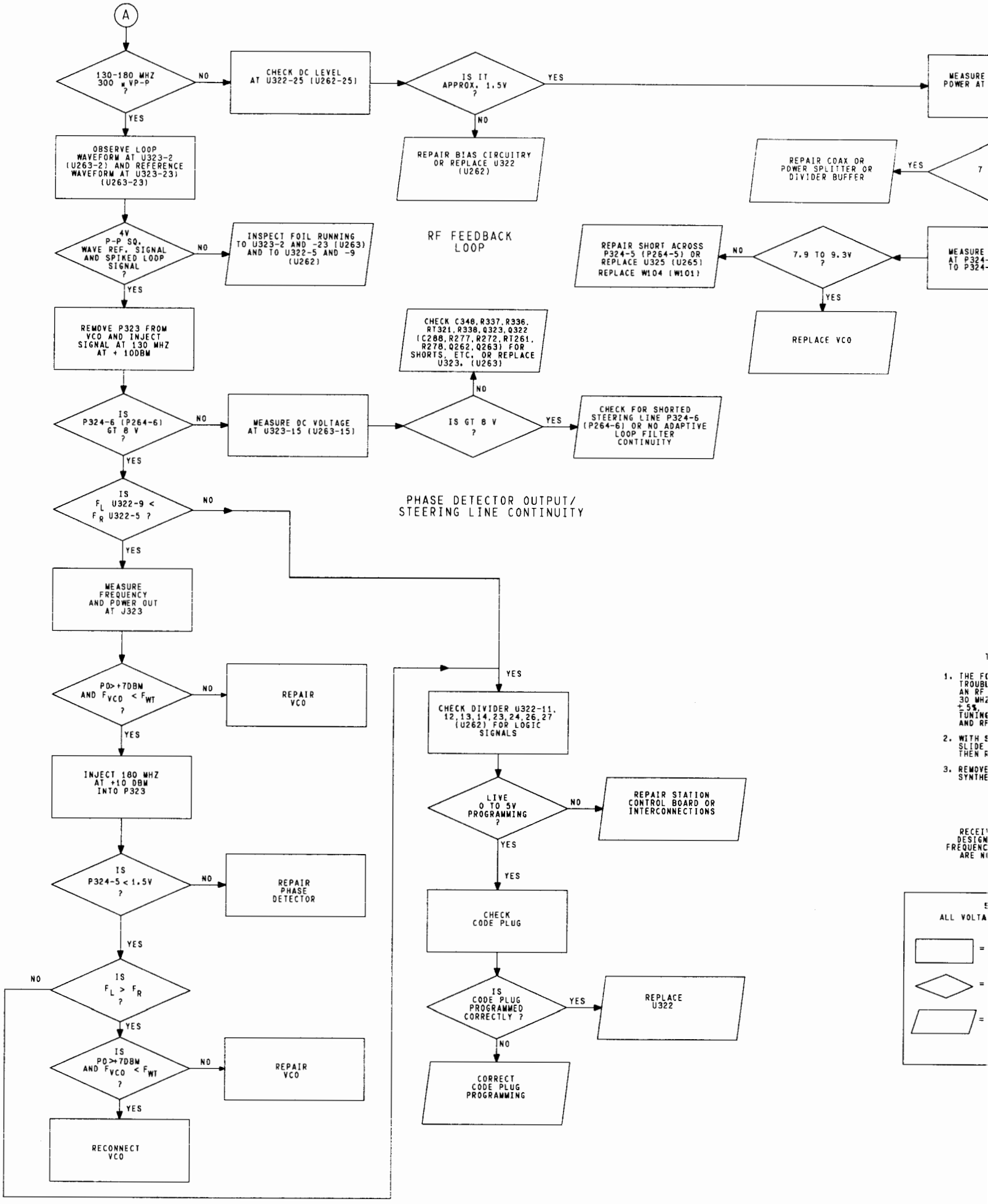
Pin No.	Function	To / From	Nominal Voltage
1*	GND	–	0 V dc
2	REF IN	from J381 (reference oscillator)	1.5 V dc + 0.6 V pp ac (14.4 MHz)
3	N.C.	–	–
4	N.C.	–	–
5*	REFERENCE OUT	to U323–2 (phase detector)	0 to 4.3 V square wave (5.0 kHz to 6.25 kHz)
6	N.C.	–	–
7	N.C.	–	–
8	N.C.	–	–
9*	LOOP OUT	to phase detector	2.9 V to 4.3 V narrow pulse (1.4 V_{pp}, 160 µsec nominal period)
10*	V_{cc}	from regulator	5 V dc
11	D0	from microcomputer	0 to 5 V pulse train
12	D1	from microcomputer	0 to 5 V pulse train
13	D2	from microcomputer	0 to 5 V pulse train
14	D3	from microcomputer	0 to 5 V pulse train
15	N.C.	–	–
16	N.C.	–	–
17	VCO3	to Q327 gate (Tx only)	0 to 5 V dc
18	FREQ CHANGE	to phase detector U323–5	o to 5 V dc
19	VCO1	N.C.	–
20	VCO2	to J324C–2	0.1 or 8.6 V dc
21	N.C.	–	–
22	V_{BB}	R331, C337, R271, C277	1.5 V dc
23	A0	from microcomputer	0 to 5 V pulse train
24	A1	from microcomputer	0 to 5 V pulse train
25	F_{IN}	from divider buffer	+0.7 V_{PP} ac (approx. 150 MHz)
26	A2	from microcomputer	0 to 5 V pulse train
27*	STROBE	from microcomputer	0 to 5 V pulse train

* should be checked first

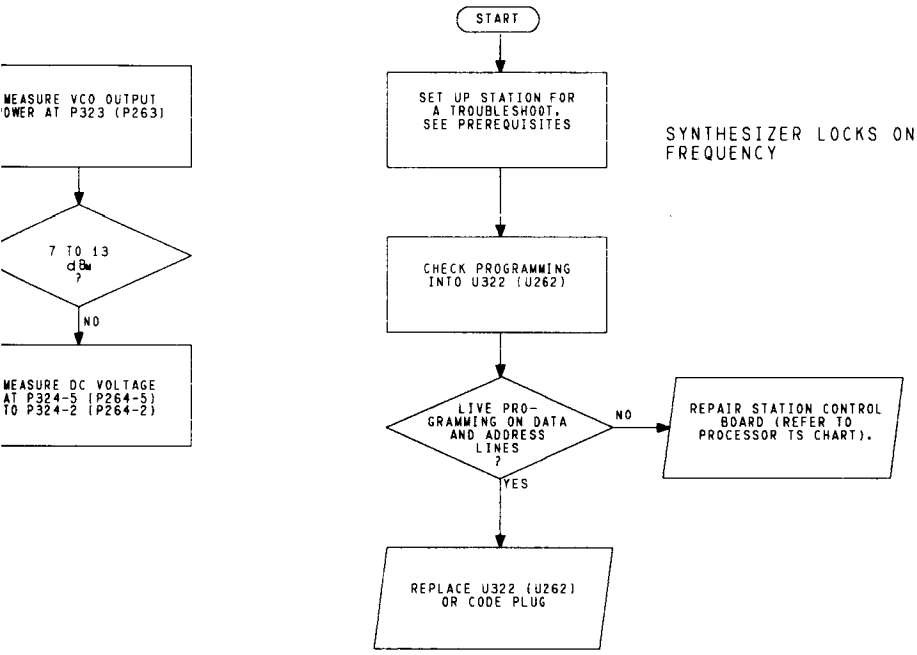
Table 6. Super U325 Filter Pin Connections and Voltages

Pin No.	Function	To / From	Nominal Voltage
1	V_{CC}	from 9.6 V regulator	9.6 V dc
2	FILTER CAP	C360	7.1 V dc
3	EXT DRIVER CONTROL	Q325	8.9 V dc
4	8.6 V OUT	to VCO	8.9 V dc
5	Ground (internal NPN emitter)	from regulator	0 V dc
6	N.C.	–	–
7	N.C.	–	–
8	N.C.	–	–


SYNTHESIZER DOES NOT LOCK
START
SET UP STATION FOR TROUBLESHOOTING. USE TS PREREQUISITES ON THIS CHART.
OBSERVE DC VOLTAGE AT U323-7 (U263-7).
IS IT LT 1 V ?
NO
REPLACE Q324 (Q264) OR REPAIR STATION CONTROL BOARD.
YES
MONITOR 9.6V AT U323-14 (U263-14) AND 5V AT U322-10 (U262-10)
VOLTAGES PRESENT WITHOUT RIPPLE ?
NO
CHECK INTERCONNECTIONS OR REPAIR 9.6V REGULATOR ON IPA, OR 5V SUPPLY ON INTERCONNECT BOARD
YES
CHECK FOR 14.4 MHZ AT U322-2 (U262-2)
REFERENCE OSCILLATOR LOOP
0.6 TO 1V P-P SINEWAVE ?
NO
CHECK 14.4 MHZ AT U381A-3
0.6 TO 1V P-P ?
NO
REPLACE REFERENCE OSCILLATOR U381
YES
INSPECT AND REPAIR CIRCUITRY FROM U381A-3 TO U322-2 (U262-2)
YES
INSPECT REFERENCE SIGNAL AT U322-5 (U262-5)
IS 5 OR 6.25 MHZ SQUARE WAVE 3.8V P-P ?
NO
YES
YES
OBSERVE LOOP PULSE AT U322-9 (U262-9)
CHECK PIN U322-27 (U262-27) FOR FAST LOGIC PULSE
PROGRAMMING LOOP
1.4V P-P PULSES ?
NO
YES
ARE 0-5V PULSES PRESENT ?
NO
CHECK FOR SHORT AT U322-27 (U262-27) OR NO SIGNAL FROM STATION CONTROL MODULE
YES
CHECK RF LEVEL AND COUNT FREQ AT U322-25 (U262-25)
CHECK PINS 23,24,26, 11,12,13,14 OF U322 (U262) FOR LOGIC SIGNALS
0 TO 5V LIVE PROGRAMMING ?
NO
CHECK FOIL RUNNERS FOR BREAKS FROM STATION CONTROL BOARD OR REPAIR STATION CONTROL BOARD
YES
REPLACE U322 (U262) OR REPAIR PROGRAMMING (SEE PROCESSOR TS CHART IN THIS MANUAL).
A
REPLACE R330 (R270): CHECK FOIL RUNNERS FOR BREAK OR REPLACE U322 (U262)


A
130-180 MHZ 300 mVP-P ?
NO
CHECK DC LEVEL AT U322-25 (U262-25)
IS IT APPROX. 1.5V ?
YES
NO
REPAIR BIAS CIRCUITRY OR REPLACE U322 (U262)
YES
OBSERVE LOOP WAVEFORM AT U323-2 (U263-2) AND REFERENCE WAVEFORM AT U323-23) (U263-23)
4V P-P SQ. WAVE REF. SIGNAL AND SPIKED LOOP SIGNAL ?
NO
INSPECT FOIL RUNNING TO U323-2 AND -23 (U263) AND TO U322-5 AND -9 (U262)
YES
RF FEEDBACK LOOP
REMOVE P323 FROM VCO AND INJECT SIGNAL AT 130 MHZ AT + 10DBM
IS P324-6 (P264-6) GT 8 V ?
NO
MEASURE DC VOLTAGE AT U323-15 (U263-15)
IS GT 8 V ?
NO
CHECK C348, R337, R336, RT321, R338, Q323, Q322 (C288, R277, R272, RT261, R278, Q262, Q263) FOR SHORTS, ETC. OR REPLACE U323, (U263)
YES
CHECK FOR SHORTED STEERING LINE P324-6 (P264-6) OR NO ADAPTIVE LOOP FILTER CONTINUITY
YES
IS F_L U322-9 < F_R U322-5 ?
NO
PHASE DETECTOR OUTPUT/ STEERING LINE CONTINUITY
YES
MEASURE FREQUENCY AND POWER OUT AT J323
PO>+7DBM AND $F_{VCO} < F_{WT}$?
NO
REPAIR VCO
YES
INJECT 180 MHZ AT +10 DBM INTO P323
IS P324-5 < 1.5V ?
NO
REPAIR PHASE DETECTOR
YES
IS $F_L > F_R$?
NO
YES
IS PO>+7DBM AND $F_{VCO} < F_{WT}$?
NO
REPAIR VCO
YES
RECONNECT VCO
YES
CHECK DIVIDER U322-11, 12, 13, 14, 23, 24, 26, 27 (U262) FOR LOGIC SIGNALS
LIVE 0 TO 5V PROGRAMMING ?
NO
REPAIR STATION CONTROL BOARD OR INTERCONNECTIONS
YES
YES
CHECK CODE PLUG
IS CODE PLUG PROGRAMMED CORRECTLY ?
YES
REPLACE U322
NO
CORRECT CODE PLUG PROGRAMMING
REPAIR COAX OR POWER SPLITTER OR DIVIDER BUFFER
YES
7
REPAIR SHORT ACROSS P324-5 (P264-5) OR REPLACE U325 (U265) REPLACE W104 (W101)
NO
7.9 TO 9.3V ?
YES
REPLACE VCO
MEASURE POWER AT
MEASURE AT P324- TO P324-
1. THE FO TROUBL AN RF 30 MHZ + 5%, TUNING AND RF
2. WITH S SLIDE THEN R
3. REMOVE SYNTHE
RECEI DESIGN FREQUENC ARE NO
5
ALL VOLTA
=
=
=

TROUBLESHOOTING CHART



TROUBLESHOOTING PREREQUISITES:

1. THE FOLLOWING TEST EQUIPMENT IS REQUIRED FOR TROUBLESHOOTING THE SYNTHESIZER CIRCUITS: AN RF FREQUENCY COUNTER, RF PROBE, DC VOLTMETER, 30 MHZ BANDWIDTH OSCILLOSCOPE, OHM METER, 270 OHM ± 5%, 1 4W RESISTOR (MOTOROLA NO. 6-11009C35), VCO TUNING TOOL, REFERENCE OSCILLATOR TUNING TOOL, AND RF POWER METER
2. WITH STATION POWERED AND DE-KEYED, UNLATCH AND SLIDE RF TRAY OUT, TILT UP STATION CONROL TRAY, AND THEN REMOVE RF TRAY COVER.
3. REMOVE SOLDER SIDE SHIELDS FROM MALFUNCTIONING SYNTHESIZER CIRCUIT AREA ON UNIBOARD.

IMPORTANT

RECEIVE FREQUENCY SYNTHESIZER CIRCUITRY REFERENCE DESIGNATIONS ARE ENCLOSED IN PARENTHESIS. TRANSMIT FREQUENCY SYNTHESIZER CIRCUITRY REFERENCE DESIGNATIONS ARE NOT. IN EITHER CASE, THE APPROPRIATE TEST IS THE SAME.

SYMBOLS AND ABBREVIATIONS USED THE CHART

LL VOLTAGE MEASUREMENTS ARE DC, UNLESS OTHERWISE STATED.

= TEST TO BE DONE

= DECISION

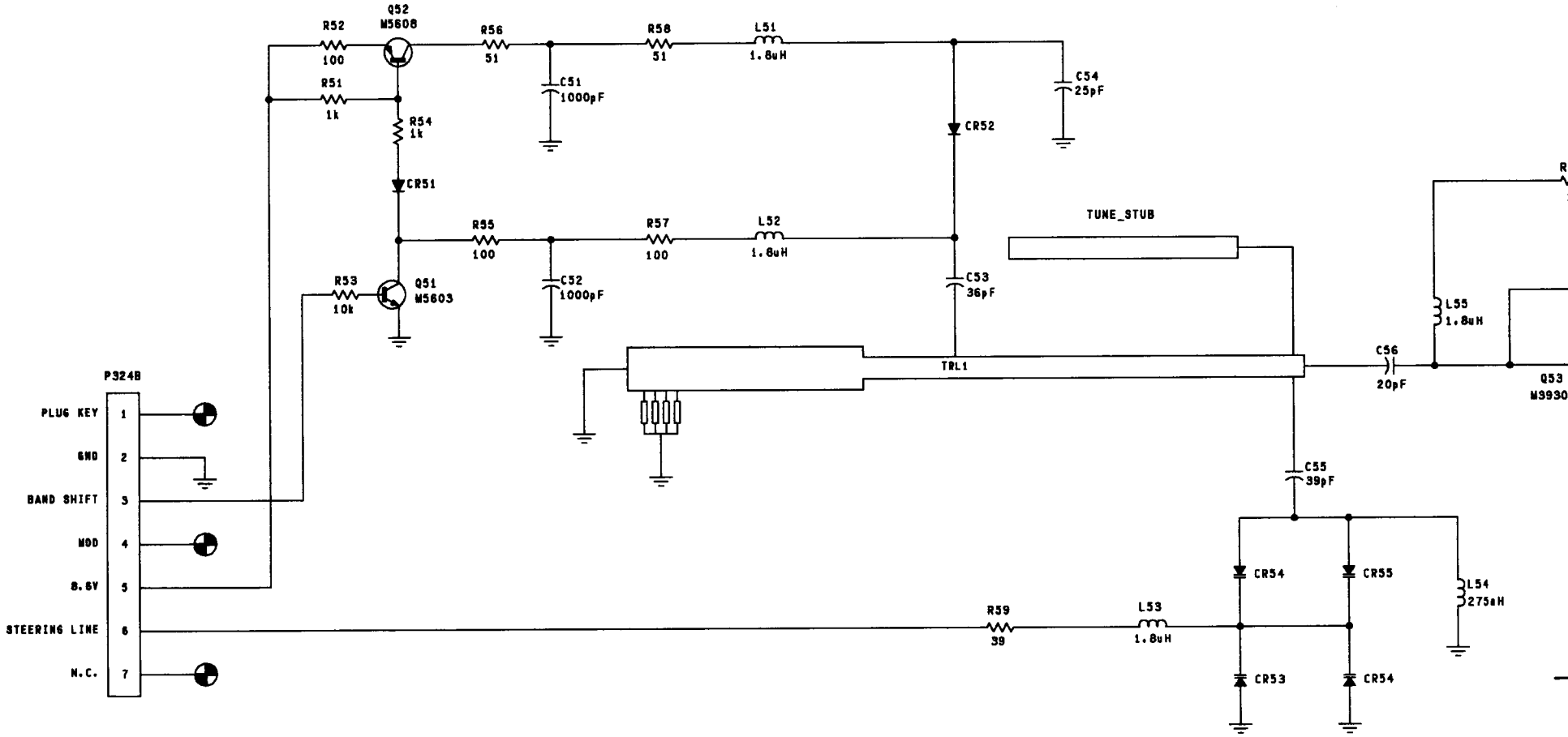
= SOURCE OR FAULT

U323-7	= PIN NO. 7 OF U323
P-P	= PEAK-TO-PEAK
F_{VCO}	= VCO OUTPUT FREQUENCY
F_{INT}	= INTENDED FREQUENCY
F_L	= LOOP PULSE FREQUENCY
F_R	= REFERENCE FREQUENCY
PCB	= PRINTED-CIRCUIT BOARD
GT	= GREATER THAN
LT	= LESS THAN
TS	= TROUBLESHOOTING
PLL	= PHASE-LOCK LOOP

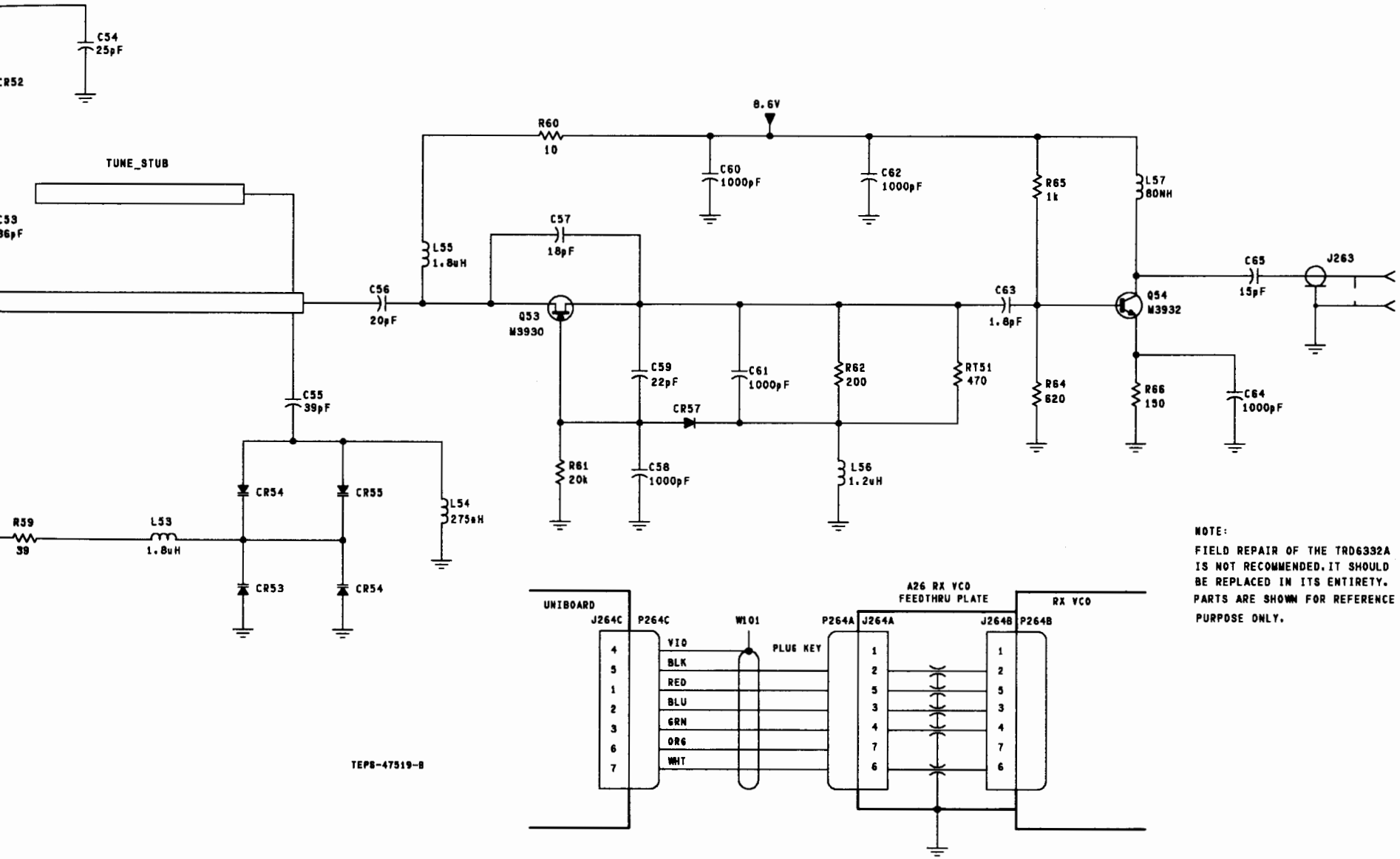
RECEIVE FREQUENCY VCO CIRCUIT BOARD DETAIL, SCHEMATIC DIAGRAM, AND PARTS LIST ON NEXT PAGE

XEPS-47674-0

A RECEIVE VCO (135.3-163.3 MHz)

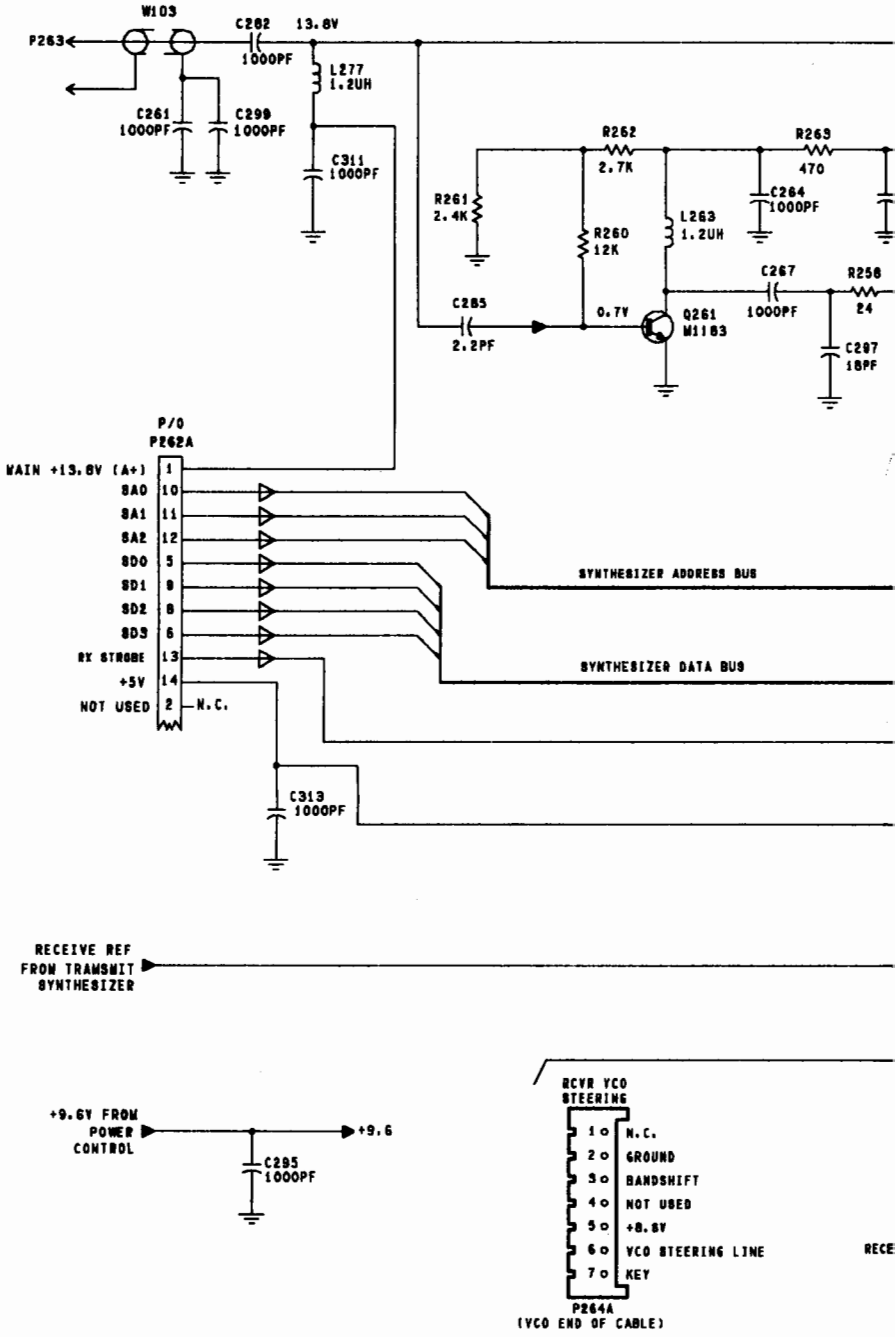


TEPS-47519-B

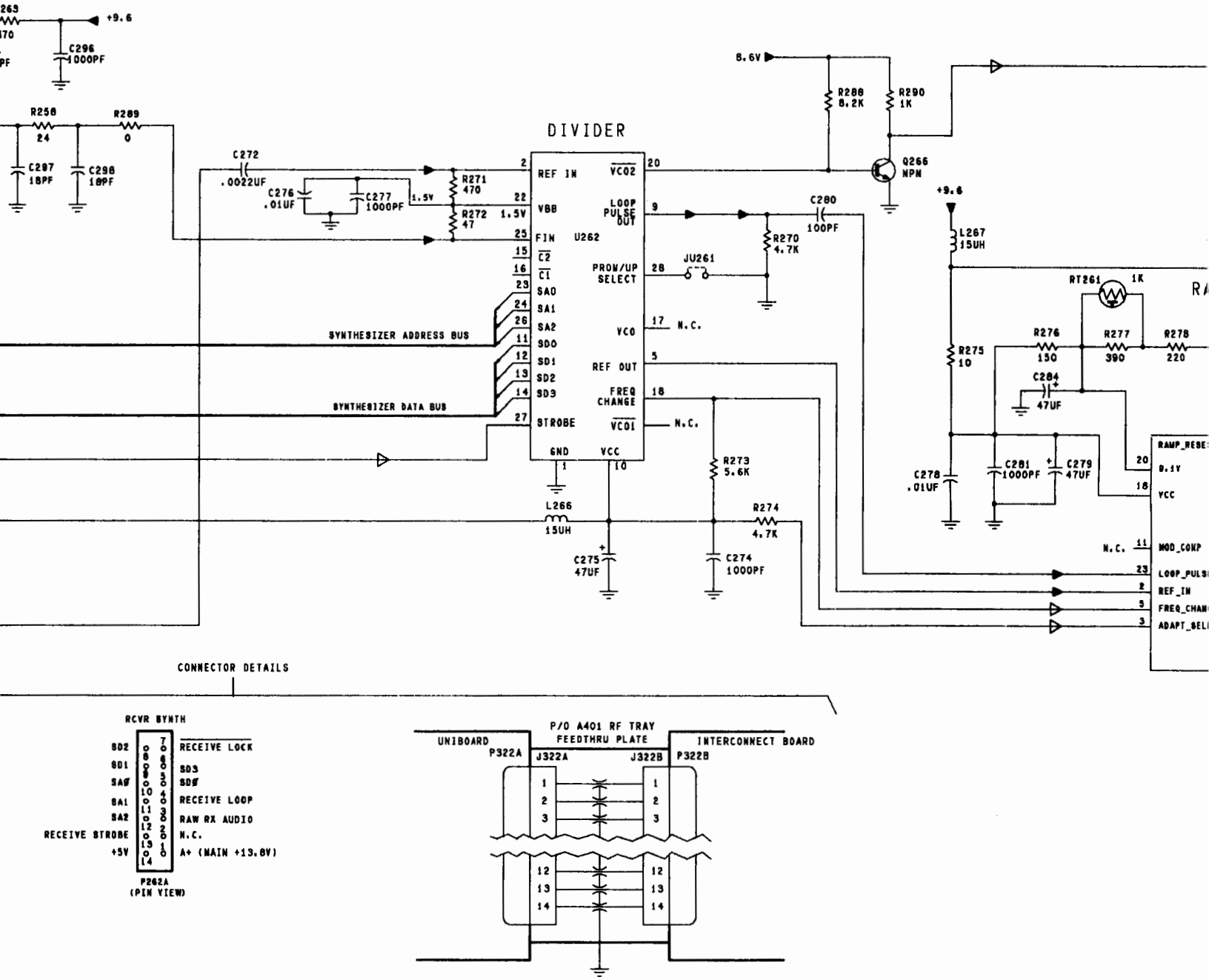

C54
25pF
CR52
TUNE_STUB
C53
36pF
8.6V
R60
10
C60
1000pF
C62
1000pF
R65
1k
L57
80NH
C57
18pF
L55
1.8uH
C56
20pF
Q53
M3930
C63
1.8pF
Q54
M3932
C65
15pF
J263
C59
22pF
C61
1000pF
R62
200
RT51
470
R64
620
R66
150
C64
1000pF
C55
39pF
CR57
R61
20k
C58
1000pF
L56
1.2uH
CR54
CR55
L54
275nH
R59
39
L53
1.8uH
CR53
CR54
TEPS-47519-8
UNIBOARD
J264C
P264C
W101
PLUG KEY
P264A
J264A
A26 RX VCO
FEEDTHRU PLATE
J264B
P264B
RX VCO
VIO
BLK
RED
BLU
GRN
ORG
WHT
4
5
1
2
3
6
7
1
2
5
3
4
7
6
NOTE:
FIELD REPAIR OF THE TRD6332A IS NOT RECOMMENDED. IT SHOULD BE REPLACED IN ITS ENTIRETY. PARTS ARE SHOWN FOR REFERENCE PURPOSE ONLY.

TRN7006A RECEIVE FREQUENCY SYNTHESIZER

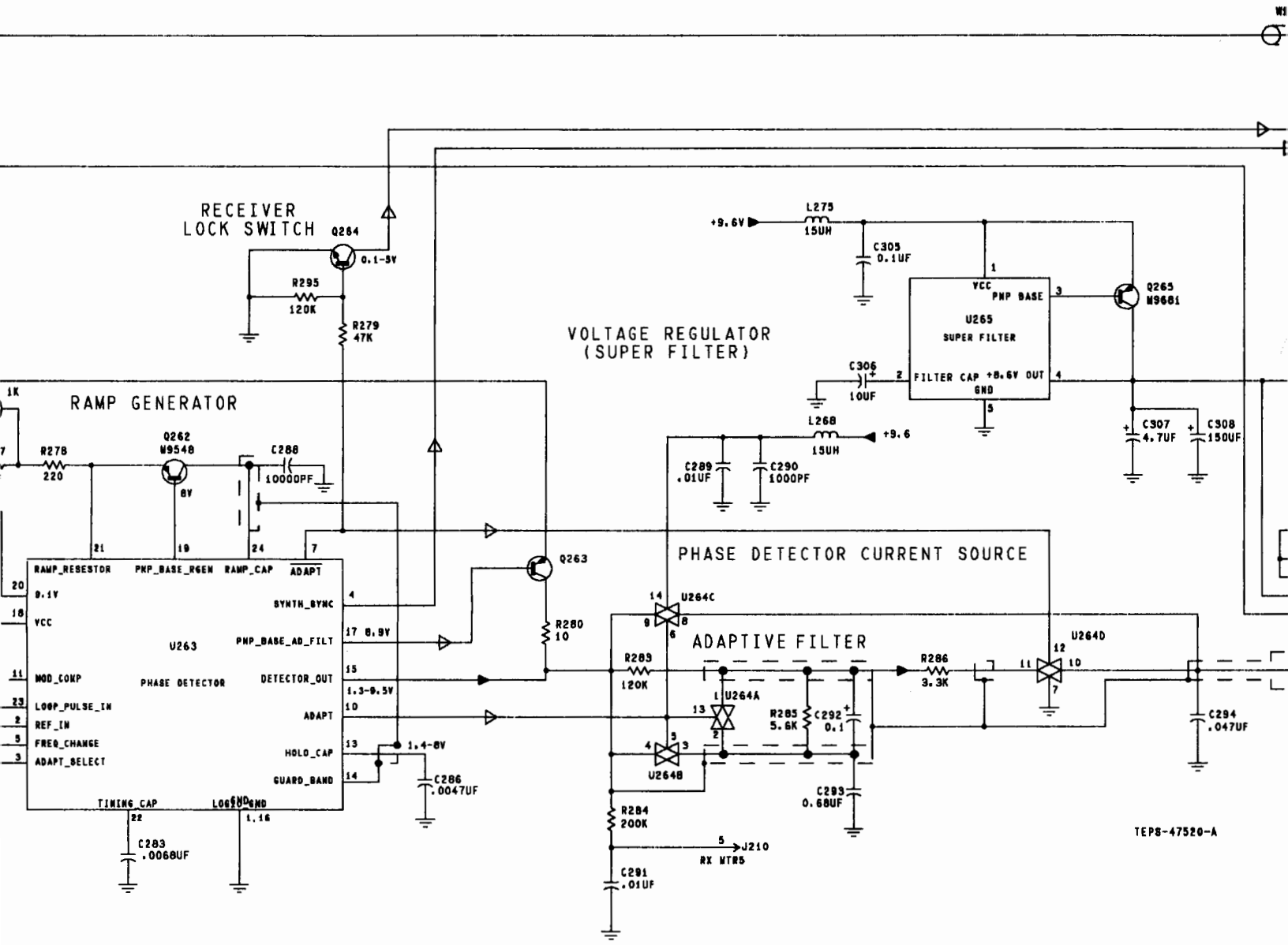
(p/o UNIBOARD)
SCHEMATIC DIAGRAM

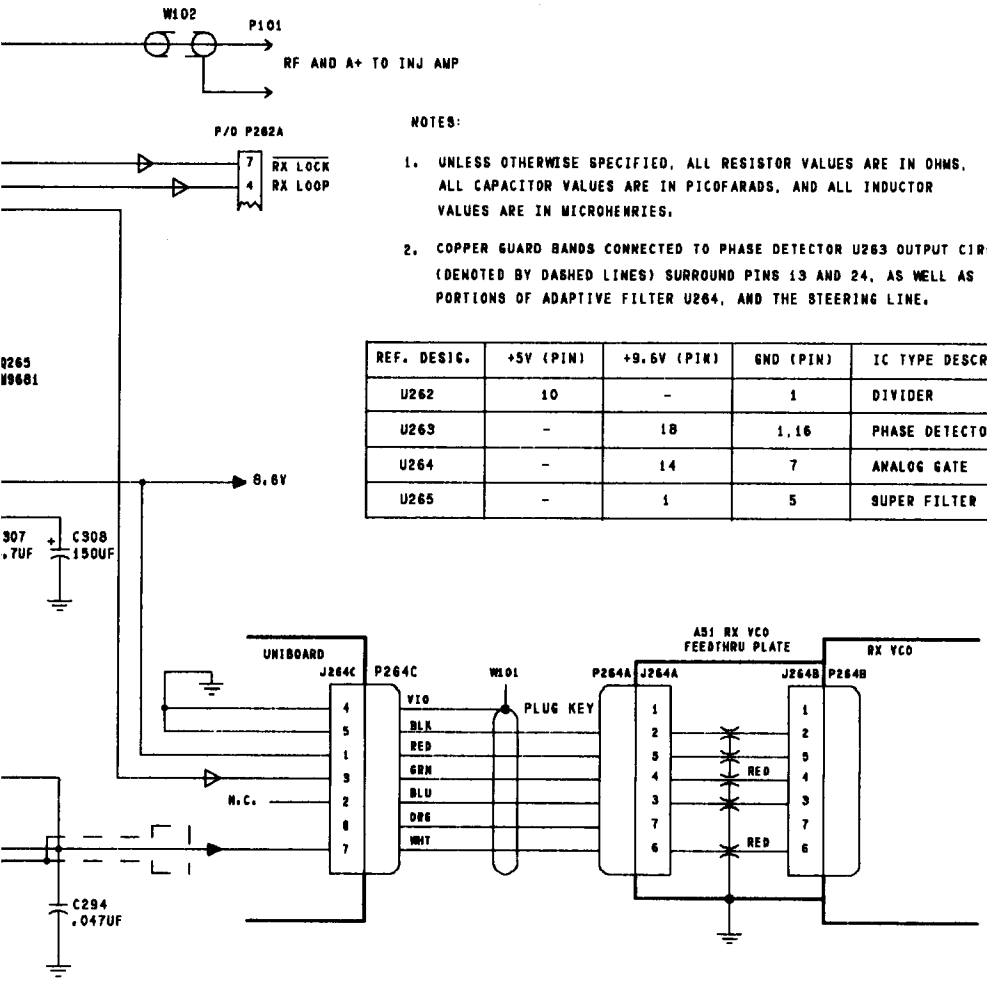


TRANSMIT FREQUENCY VCO CIRCUIT BOARD DETAIL, SCHEMATIC DIAGRAM, AND PARTS LIST ON NEXT PAGE



CONNECTOR DETAILS


RECEIVER
LOCK SWITCH
Q264
0.1-3V
R295
120K
R279
47K
VOLTAGE REGULATOR
(SUPER FILTER)
+9.6V
L275
15UH
C305
0.1UF
U265
SUPER FILTER
VCC
PNP BASE
FILTER CAP +8.6V OUT
GND
Q265
M9681
C306
10UF
L268
15UH
+9.6
C289
.01UF
C290
1000PF
C307
4.7UF
C308
150UF
RAMP GENERATOR
R278
220
Q262
M9548
8V
C288
10000PF
PHASE DETECTOR CURRENT SOURCE
Q263
R280
10
U263
PHASE DETECTOR
RAMP_RESISTOR
PNP_BASE_RGEN
RAMP_CAP
ADAPT
9.1V
VCC
SYNTH_SYNC
PNP_BASE_AD_FILT
8.9V
MOD_COMP
LOOP_PULSE_IN
REF_IN
FREQ_CHANGE
ADAPT_SELECT
DETECTOR_OUT
1.3-9.5V
ADAPT
HOLD_CAP
GUARD_BAND
1.4-8V
TIMING_CAP
LOGIC GND
GND
1.16
C283
.0068UF
C286
.0047UF
U264C
ADAPTIVE FILTER
U264D
U264A
U264B
R283
120K
R285
5.6K
C292
0.1
R286
3.3K
C293
0.68UF
C294
.047UF
R284
200K
C291
.01UF
J210
RX MTR5
TEPS-47520-A



NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTOR VALUES ARE IN OHMS, ALL CAPACITOR VALUES ARE IN PICOFARADS, AND ALL INDUCTOR VALUES ARE IN MICROHENRIES.
2. COPPER GUARD BANDS CONNECTED TO PHASE DETECTOR U263 OUTPUT CIRCUIT (DENOTED BY DASHED LINES) SURROUND PINS 13 AND 24, AS WELL AS PORTIONS OF ADAPTIVE FILTER U264, AND THE STEERING LINE.

REF. DESIG.	+5V (PIN)	+9.6V (PIN)	GND (PIN)	IC TYPE DESCRIPTION
U262	10	-	1	DIVIDER
U263	-	18	1,16	PHASE DETECTOR
U264	-	14	7	ANALOG GATE
U265	-	1	5	SUPER FILTER