MOTOROLA

RECEIVER MODULE

INCLUDES MODELS:
TRD6361A-F Receiver Board(132–154 MHZ)
TFD6511A Preselector Filter (132–154 MHZ)
TRD6362A-F Receiver Board (150–174 MHZ)
TFD6512A Preselector Filter (150–174 MHZ)

1 DESCRIPTION

The *Quantar*/*Quantro* VHF High Band Receiver Modules are described in this section. A general description, identification of controls, indicators, and inputs/outputs, a functional block diagram, and functional theory of operation are provided. The information provided is sufficient to give service personnel a functional understanding of the module, allowing maintenance and troubleshooting to the module level. (Refer also to the Maintenance and Troubleshooting section of this manual for detailed troubleshooting procedures for all modules in the station.)

General Description

The Receiver Module provides the receiver functions for the *Quantar* VHF station. Each receiver module is comprised of a Preselector Filter Assembly and a Receiver Board, all contained within a slide–in module housing. The receiver module performs highly selective bandpass filtering and dual down conversion of the station receive rf signal. A custom receiver IC then performs an analog to digital conversion of the received signal and outputs a differential data signal to the Station Control Module.

The Models TFD6511/TFD6512 Preselector Filter Assemblies and the TRD6361/TRD6362 Receiver Boards differ only in the range of operation. Models TFD6511/TRD6361 operate in VHF Range 1 (132–154MHz); Models TFD6512/TRD6362 operate in VHF Range 2 (150–174MHz). Unless otherwise noted, the information provided in this section applies to all models.

Overview of Circuitry

The receiver module contains the following circuitry:

- Frequency Synthesizer Circuitry— consisting of a phase–locked loop and VCO, generates the 1st LO injection signal
- Preselector Filter Assembly — provides 5–pole bandpass filtering of the station receive rf input
- Receiver Front End Circuitry — performs filtering, amplification, and the 1st down conversion of the receive rf signal
- Custom Receiver IC Circuitry — consists of a custom IC which performs the 2nd down conversion, filtering, amplification, and analog to digital conversion of the receive signal
- Address Decode & A/D Converter Circuitry — performs address decoding to provide board and chip select signals; also converts analog status signals to digital format for transfer to Station Control Module
- Local Power Supply Regulation — accepts +14.2V dc input and outputs +10V and +5V dc operating voltages

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2 CONTROLS, INDICATORS, AND INPUTS/OUTPUTS

Figure 1 shows the receiver module controls, indicators, and all input and output external connections.

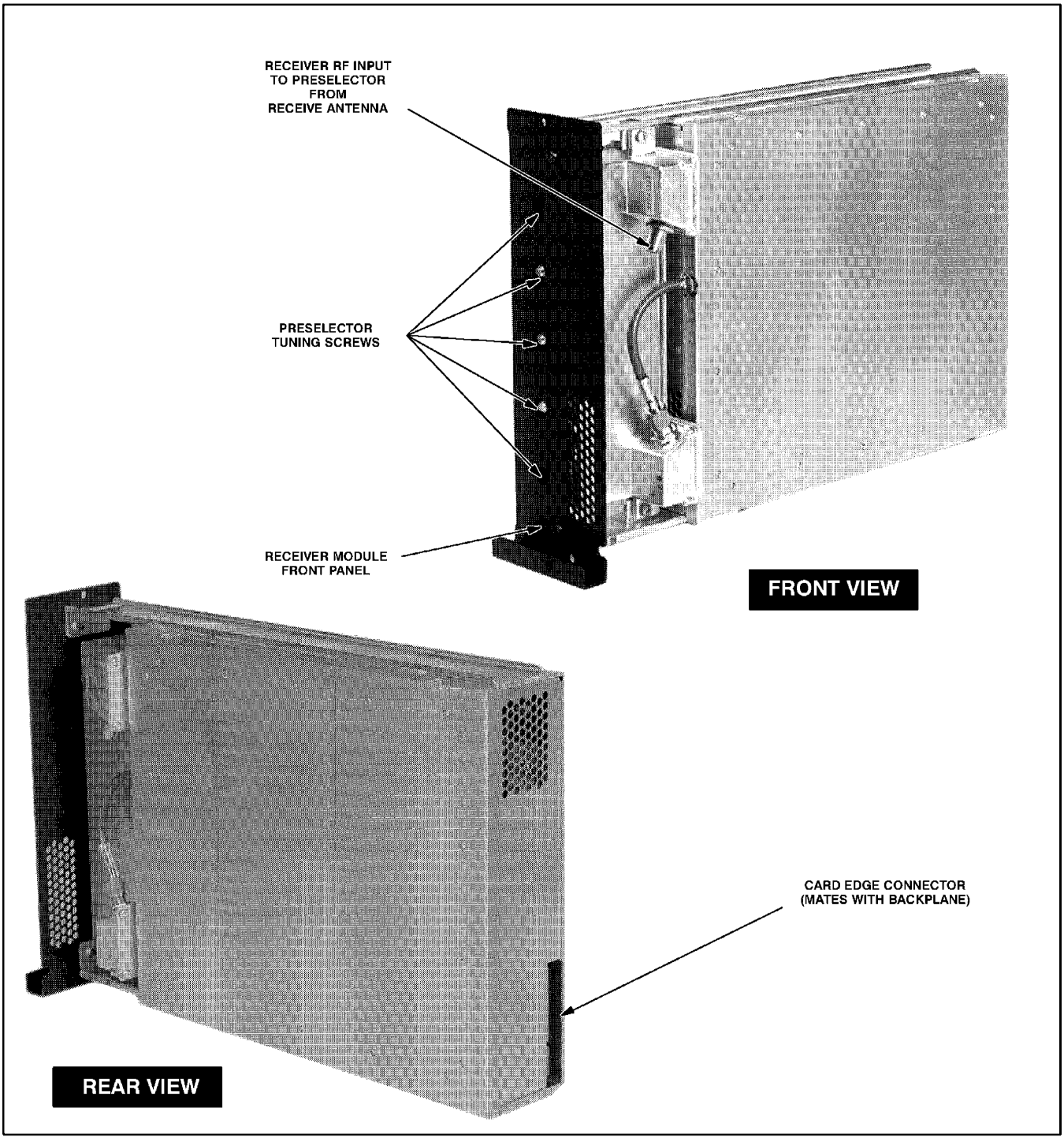

Figure 1. *Quantar/Quantro* VHF Receiver Module Controls, Indicators, and Inputs/Outputs

3 FUNCTIONAL THEORY OF OPERATION

The following theory of operation describes the operation of the receiver circuitry at a functional level. The information is presented to give the service technician a basic understanding of the functions performed by the module in order to facilitate maintenance and troubleshooting to the module level. Refer to Figure 2 for a block diagram of the receiver module.

Synthesizer and VCO Circuitry

Introduction

The synthesizer and VCO circuitry generate the 1st LO injection signal for the 1st mixer in the receiver front end circuitry. Functional operation of these circuits is as follows.

Phase–Locked Loop

The phase–locked loop (PLL) IC receives frequency selection data from the Station Control Module microprocessor. Once programmed, the PLL IC compares a 2.1 MHz reference signal (from the Station Control Module) with a feedback sample of the VCO output. Depending on whether the feedback signal is higher or lower in frequency than the 2.1 MHz reference, correction pulses are generated. (The width of these correction pulses is dependent on the amount of difference between the 2.1 MHz reference and the VCO feedback.)

The up/down pulses from the PLL IC are fed to a charge pump which outputs a dc voltage proportional to the pulse widths. This dc voltage is then low–pass filtered and fed to the VCO as the *CONTROL VOLTAGE*. (Note that if a frequency change is requested by the microprocessor, the low–pass loop filter is momentarily bypassed to accelerate the frequency change.)

VCO

The dc control voltage from the synthesizer is fed to dual VCOs which generate the 1st LO injection signal. Within each band (Range 1 and Range 2), one VCO generates signals in the upper half of the band, while the other VCO generates signals in the lower half of the band. Only one VCO is active at a time. Selection of the active VCO is provided by a *BANDSHIFT* signal from the PLL IC.

The active VCO responds to the dc control voltage and generates the appropriate rf signal. This signal is fed through a buffer ampifier and impedance matching and output to the 1st LO injection amplifier in the receiver front end circuitry. A sample of the injection signal is returned to the PLL IC (via a feedback buffer) to serve as a VCO feedback signal.

Preselector Filter Assembly

The preselector filter assembly provides 5 poles of bandpass filtering for the station receive rf input signal. The filter assembly is mounted to the front of the receiver module housing and provides mini–UHF connectors for input from the receive antenna and output to the receiver board. Tuning screws are provided for filter tuning. (Refer to the *Troubleshooting* section in this manual for instructions on tuning the preselector assembly.)

Receiver Front End Circuitry

The receive rf input is fed from the antenna through the 5–pole preselector assembly to the receiver board. The signal is low–pass filtered, amplified, image filtered, and fed to one input of the 1st mixer. The signal is mixed with the 1st LO injection signal (generated by the synthesizer/VCO circuitry) to produce a 21.45 MHz 1st i–f signal.

The 1st i–f signal is 2–pole bandpass filtered and fed to an amplifier. The amplifier gain (high or low) is determined by an AGC switch circuit that is controlled by an AGC select signal from the Station Control Board. The amplified 1st i–f signal is then 4–pole bandpass filtered and fed to the rf input of the custom receiver IC.

Custom Receiver IC Circuitry

The custom receiver IC provides additional amplification, filtering, a second down conversion, and finally analog to digital conversion of the 2nd i–f signal. The digital receive signal is then output via differential driver circuitry to the Station Control Board. This data signal contains the necessary I and Q quadrature information, AGC information, and other data transfer information required by the Station Control Board to process the receive signal. (Note that the recovered audio signal is in digital format throughout the station circuitry, resulting in a more noise–free, linear receiver. Analog audio is present only in the external speaker driver circuitry on the Station Control Board and on the Wireline Interface Board at the phone line connections to and from the station.)

The remainder of the custom receiver IC circuitry consists of timing and tank circuits to support the internal oscillator, 2nd LO synthesizer circuitry, and 2nd i–f circuitry.

A serial bus allows data communications between the custom receiver IC and the DSP ASIC located on the Station Control Board. This bus allows the DSP ASIC to control various current and gain settings, establish the data bus clock rate, program the 2nd LO, and perform other control functions.

Address Decode and A/D Converter Circuitry

Address Decode Circuitry

The address decode circuitry allows the Station Control Board to use the address bus to select a specific device on a specific station board for control or data communications purposes (via the SPI bus). If the board select circuitry decodes address lines A2 thru A5 as the receiver module address, it enables the chip select circuitry. The chip select circuitry then decodes address lines A0 and A1 and generates chip select signals for the PLL and A/D converter and the *SYNTH ADAPT* signal to control the loop filter bypass switch in the synthesizer circuitry.

A/D Converter Circuitry

Analog signals from various strategic operating points throughout the receiver board are fed to the A/D converter, which converts them to a digital signal and, upon request by the Station Control Board, outputs the signal to the Station Control Board via the SPI bus.

Voltage Regulator Circuitry

The voltage regulator circuitry consists of +10V and two +5V regulators. The +10V regulator accepts a +14.2V dc input and generates a +10V dc operating voltage for the receiver board circuitry.

The +10V regulator output also feeds two +5V regulators which output Custom Analog +5V and Custom Digital +5V dc operating voltages to supply the custom receiver IC. In addition, a +5V dc operating voltage is input at the backplane (from the station power supply) to supply Digital +5V to the remainder of the receiver board circuitry.

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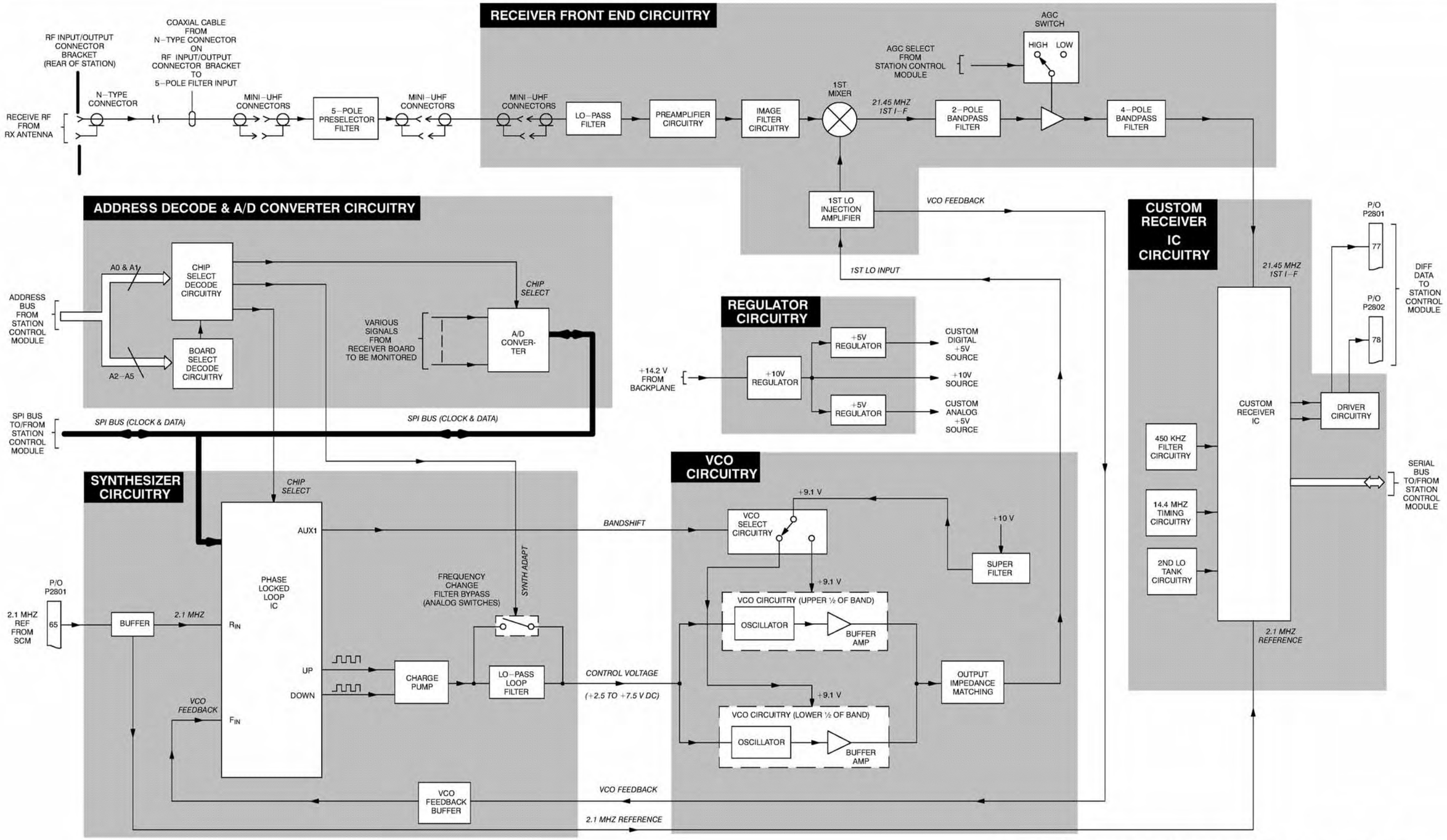

Figure 2. VHF Ranges 1 and 2 Receiver Module Functional Block Diagram

MOTOROLA

RECEIVER MODULE

INCLUDES MODELS:

CRX4022A Receiver Board/CRX4001A Preselector (380–433 MHZ)
TRE6281A–E Receiver Board/TLE5991A Preselector (403–433 MHZ)
TRE6282A–E Receiver Board/TLE5992A Preselector (438–470 MHZ)
TRE6283A–E Receiver Board/TLE5993A Preselector (470–494 MHZ)
TRE6284A–E Receiver Board/TLE5993A Preselector (494–520 MHZ)

1 DESCRIPTION

The *Quantar*/*Quantro* UHF Receiver Modules (ranges 0 thru 4) are described in this section. A general description, identification of controls, indicators, and inputs/outputs, a functional block diagram, and functional theory of operation are provided. The information provided is sufficient to give service personnel a functional understanding of the module, allowing maintenance and troubleshooting to the module level. (Refer also to the Maintenance and Troubleshooting section of this manual for detailed troubleshooting procedures for all equipment modules.)

General Description

The Receiver Module provides the receiver functions for the *Quantar*/*Quantro* communications equipment. Each receiver module is comprised of a Preselector Filter Assembly and a Receiver Board, all contained within a slide-in module housing. The receiver module performs highly selective bandpass filtering and dual down conversion of the receive rf signal. A custom receiver IC then performs an analog to digital conversion of the received signal and outputs a differential data signal to the Station Control Module.

The preselector and receiver board models differ only in the range of operation. Unless otherwise noted, the information provided in this section applies to all models.

Overview of Circuitry

The receiver module contains the following circuitry:

- Frequency Synthesizer Circuitry— consisting of a phase–locked loop and VCO, generates the 1st LO injection signal
- Preselector Filter Assembly — provides 3–pole bandpass filtering of the receive rf input
- Receiver Front End Circuitry — performs filtering, amplification, and the 1st down conversion of the receive rf signal
- Custom Receiver IC Circuitry — consists of a custom IC which performs the 2nd down conversion, filtering, amplification, and analog to digital conversion of the receive signal
- Address Decode & A/D Converter Circuitry — performs address decoding to provide board and chip select signals; also converts analog status signals to digital format for transfer to Station Control Module
- Local Power Supply Regulation — accepts +14.2 V dc input and outputs +10V and +5V dc operating voltages

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2 CONTROLS, INDICATORS, AND INPUTS/OUTPUTS

Figure 1 shows the receiver module controls, indicators, and all input and output external connections.

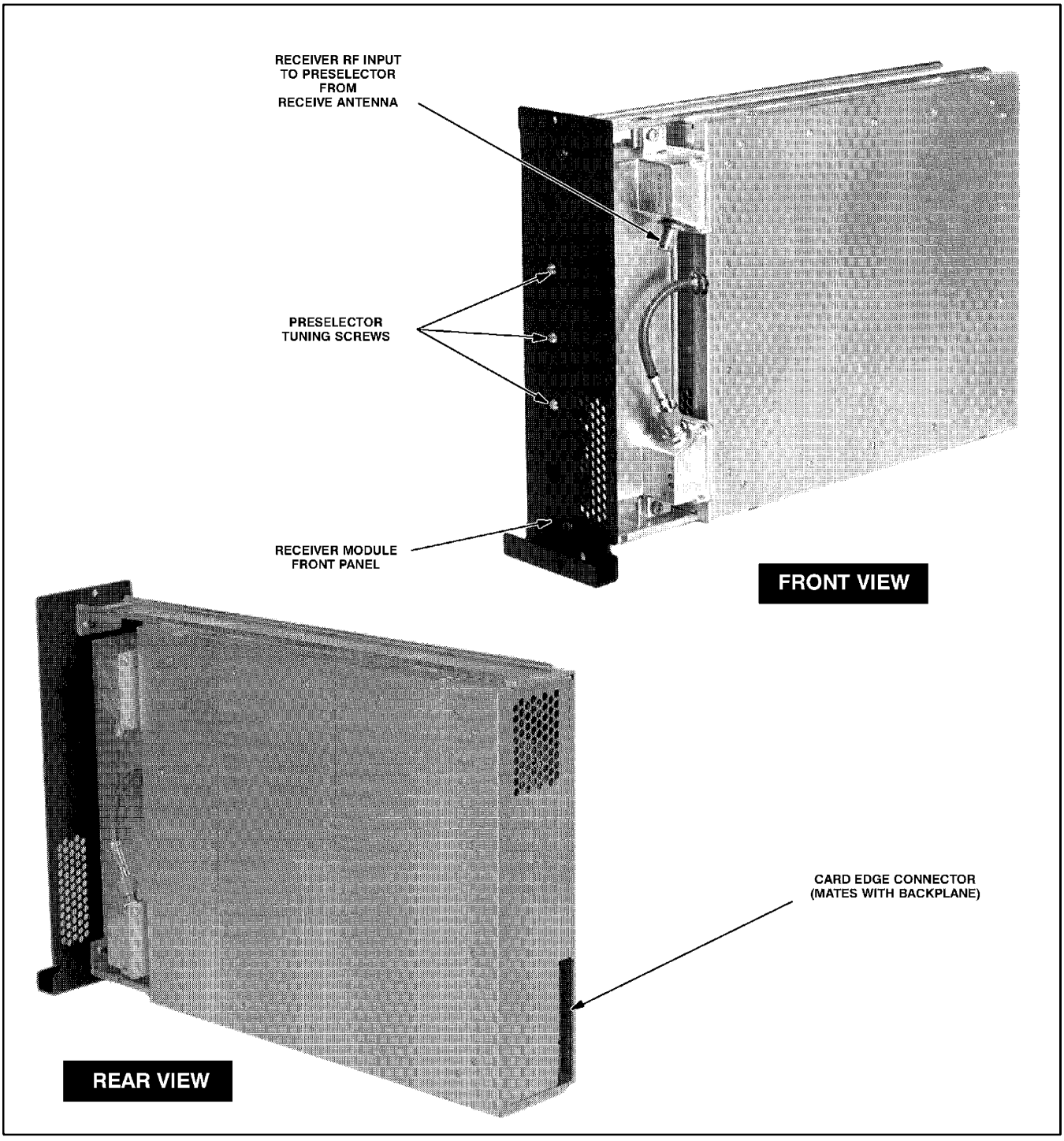

Figure 1. UHF Receiver Module Controls, Indicators, and Inputs/Outputs

3 FUNCTIONAL THEORY OF OPERATION

The following theory of operation describes the operation of the receiver circuitry at a functional level. The information is presented to give the service technician a basic understanding of the functions performed by the module in order to facilitate maintenance and troubleshooting to the module level. Refer to Figure 2 for a block diagram of the receiver module.

Synthesizer and VCO Circuitry

Introduction

The synthesizer and VCO circuitry generate the 1st LO injection signal for the 1st mixer in the receiver front end circuitry. Functional operation of these circuits is as follows.

Phase–Locked Loop

The phase–locked loop (PLL) IC receives frequency selection data from the Station Control Module microprocessor. Once programmed, the PLL IC compares a 2.1 MHz reference signal (from the Station Control Module) with a feedback sample of the VCO output. Depending on whether the feedback signal is higher or lower in frequency than the 2.1 MHz reference, correction pulses are generated. (The width of these correction pulses is dependent on the amount of difference between the 2.1 MHz reference and the VCO feedback.)

The up/down pulses from the PLL IC are fed to a charge pump which outputs a dc voltage proportional to the pulse widths. This dc voltage is then low–pass filtered and fed to the VCO as the *CONTROL VOLTAGE*. (Note that if a frequency change is requested by the microprocessor, the low–pass loop filter is momentarily bypassed to accelerate the frequency change.)

VCO

The dc control voltage from the synthesizer is fed to dual VCOs which generate the 1st LO injection signal. Within each band (Ranges 0 thru 4), one VCO generates signals in the upper half of the band, while the other VCO generates signals in the lower half of the band. Only one VCO is active at a time. Selection of the active VCO is provided by a *BANDSHIFT* signal from the PLL IC.

The active VCO responds to the dc control voltage and generates the appropriate rf signal. This signal is fed through a buffer amplifier and impedance matching and output to the 1st LO injection amplifier in the receiver front end circuitry. A sample of the injection signal is returned to the PLL IC (via a feedback buffer) to serve as a VCO feedback signal.

Preselector Filter Assembly

The preselector filter assembly provides 3 poles of bandpass filtering for the receive rf input signal. The filter assembly is mounted to the front of the receiver module housing and provides mini–UHF connectors for input from the receive antenna and output to the receiver board. Tuning screws are provided for filter tuning. (Refer to the *Troubleshooting* section in this manual for instructions on tuning the preselector assembly.)

Receiver Front End Circuitry

The receive rf input is fed from the antenna through the 3–pole preselector assembly to the receiver board. The signal is low–pass filtered, amplified, image filtered, and fed to one input of the 1st mixer. The signal is mixed with the 1st LO injection signal (generated by the synthesizer/VCO circuitry) to produce a 73.35 MHz 1st i–f signal.

The 1st i–f signal is 2–pole bandpass filtered and fed to an amplifier. The amplifier gain (high or low) is determined by an AGC switch circuit that is controlled by an AGC select signal from the Station Control Module. The amplified 1st i–f signal is then 4–pole bandpass filtered and fed to the rf input of the custom receiver IC.

Custom Receiver IC Circuitry

The custom receiver IC provides additional amplification, filtering, a second down conversion, and finally analog to digital conversion of the 2nd i–f signal. The digital receive signal is then output via differential driver circuitry to the Station Control Board. This data signal contains the necessary I and Q quadrature information, AGC information, and other data transfer information required by the Station Control Module to process the receive signal. (Note that the recovered audio signal is in digital format throughout the equipment circuitry, resulting in a more noise–free, linear receiver. Analog audio is present only in the external speaker driver circuitry on the Station Control Board and on the Wireline Interface Board at the phone line connections to and from the equipment.)

The remainder of the custom receiver IC circuitry consists of 2nd LO VCO circuitry and timing and tank circuits to support internal circuitry.

A serial bus allows data communications between the custom receiver IC and the DSP ASIC located on the Station Control Board. This bus allows the DSP ASIC to control various current and gain settings, establish the data bus clock rate, program the 2nd LO, and perform other control functions.

Address Decode and A/D Converter Circuitry

Address Decode Circuitry

The address decode circuitry allows the Station Control Board to use the address bus to select a specific device on a specific station board for control or data communications purposes (via the SPI bus). If the board select circuitry decodes address lines A2 thru A5 as the receiver module address, it enables the chip select circuitry. The chip select circuitry then decodes address lines A0 and A1 and generates chip select signals for the PLL and A/D converter and the *SYNTH ADAPT* signal to control the loop filter bypass switch in the synthesizer circuitry.

A/D Converter Circuitry

Analog signals from various strategic operating points throughout the receiver board are fed to the A/D converter, which converts them to a digital signal and, upon request by the Station Control Module, outputs the signal to the Station Control Module via the SPI bus.

Voltage Regulator Circuitry

The voltage regulator circuitry consists of +10V and three +5V regulators. The +10V regulator accepts a +14.2V dc input and generates a +10V dc operating voltage for the receiver board circuitry.

The +10V regulator output also feeds three +5V regulators. Two of the regulators provide Custom Analog +5V and Custom Digital +5V dc operating voltages to supply the custom receiver IC. The third regulator provides Synth +5V to supply the synthesizer circuitry.

In addition, a +5V dc operating voltage is input at the backplane (from the station power supply) to supply Digital +5V to the remainder of the receiver board circuitry.

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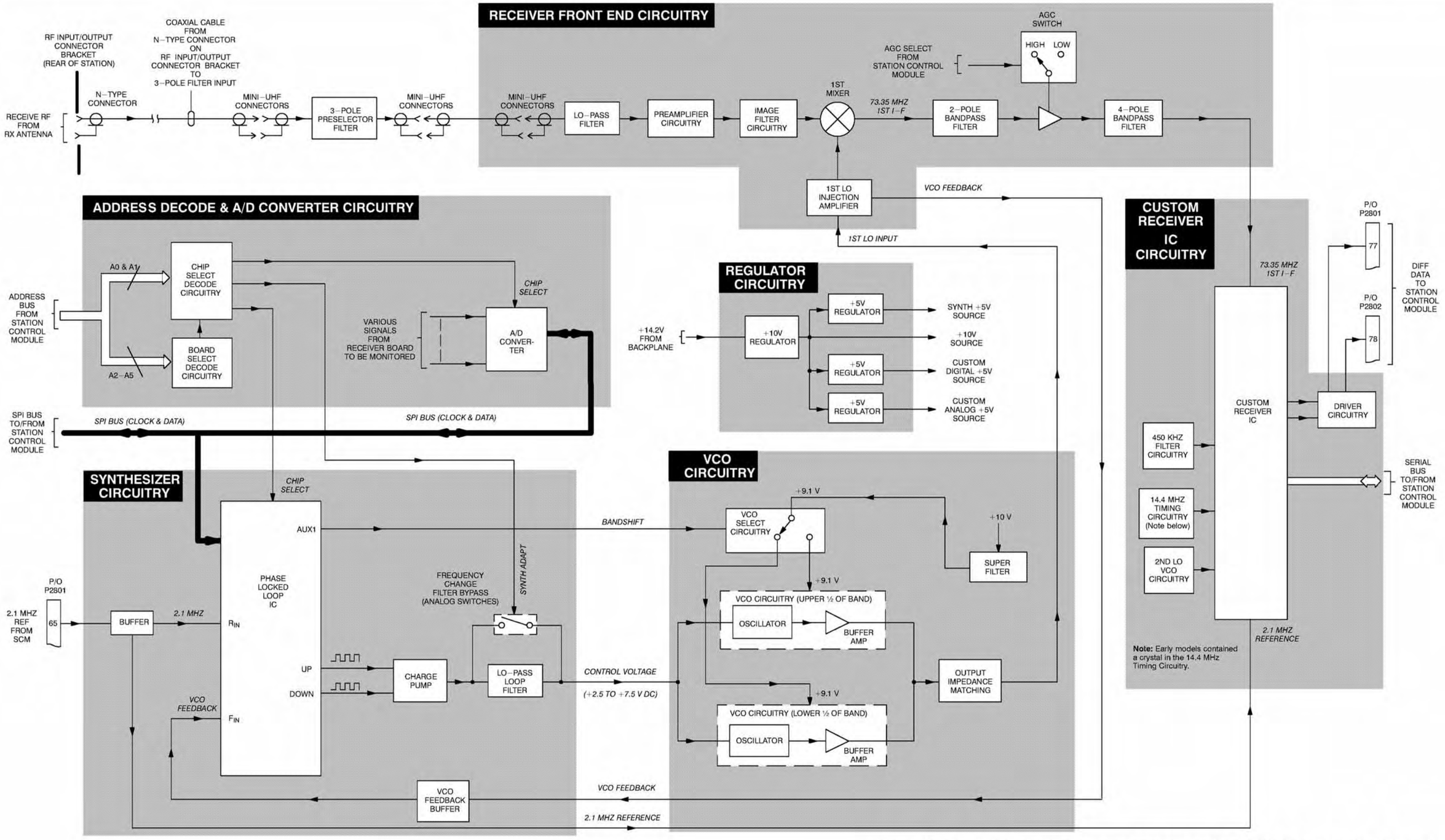

Figure 2. *Quantar/Quantro* UHF (Ranges 0 thru 4) Receiver Module Functional Block Diagram

MOTOROLA

RECEIVER MODULE

Includes TRF6551G Receiver Board

1 DESCRIPTION

The *Quantro/Quantar* 800 MHz Receiver Module is described in this section. A general description, identification of controls, indicators, and inputs/outputs, a functional block diagram, and functional theory of operation are provided. The information provided is sufficient to give service personnel a functional understanding of the module, allowing maintenance and troubleshooting to the module level. (Refer also to the Maintenance and Troubleshooting section of this manual for detailed troubleshooting procedures for all modules in the station.)

General Description

The Receiver Module provides the receiver functions for the *Quantro/Quantar* 800 MHz station. The receiver module is comprised of a Receiver Board and a ceramic preselector (mounted on board), all contained within a slide–in module housing. The receiver module performs highly selective bandpass filtering and dual down conversion of the station receive rf signal. A custom receiver IC then performs an analog to digital conversion of the received signal and outputs a differential data signal to the Station Control Module.

Overview of Circuitry

The receiver module contains the following circuitry:

- Frequency Synthesizer Circuitry— consisting of a phase–locked loop and VCO, generates the 1st LO injection signal
- Ceramic Preselector Filter — provides 7–pole bandpass filtering of the station receive rf input
- Receiver Front End Circuitry — performs filtering, amplification, and the 1st down conversion of the receive rf signal
- Custom Receiver IC Circuitry — consists of a custom IC which performs the 2nd down conversion, filtering, amplification, and analog to digital conversion of the receive signal
- Address Decode & A/D Converter Circuitry — performs address decoding to provide board and chip select signals; also converts analog status signals to digital format for transfer to Station Control Module
- Local Power Supply Regulation — accepts +14.2V dc input and outputs +10V and +5V dc operating voltages

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2 CONTROLS, INDICATORS, AND INPUTS/OUTPUTS

Figure 1 shows the receiver module controls, indicators, and all input and output external connections.

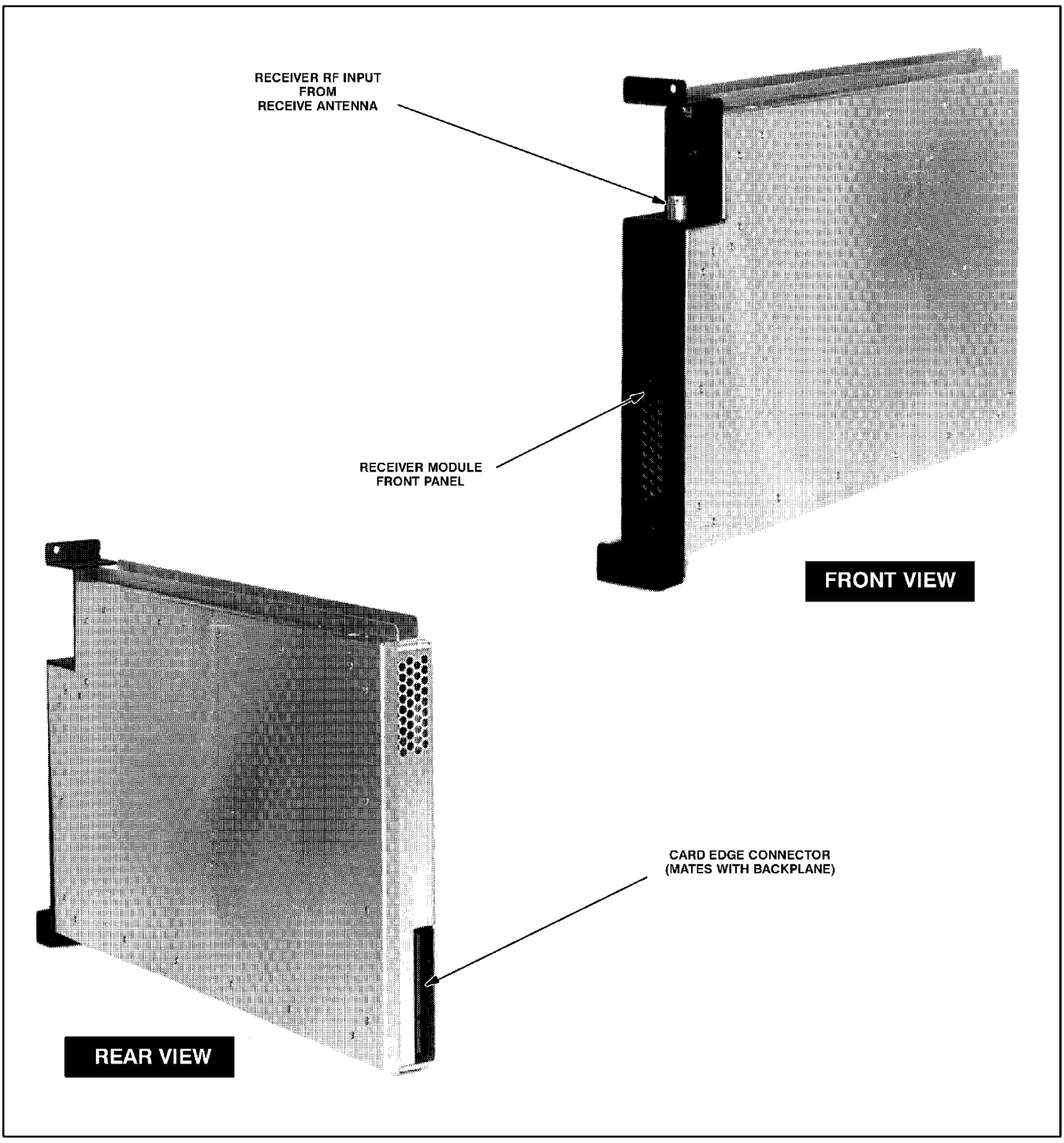

Figure 1. *Quantro/Quantar* 800 MHz Receiver Module Controls, Indicators, and Inputs/Outputs

3 FUNCTIONAL THEORY OF OPERATION

The following theory of operation describes the operation of the receiver circuitry at a functional level. The information is presented to give the service technician a basic understanding of the functions performed by the module in order to facilitate maintenance and troubleshooting to the module level. Refer to Figure 2 for a block diagram of the receiver module.

Synthesizer and VCO Circuitry

Introduction

The synthesizer and VCO circuitry generate the 1st LO injection signal for the 1st mixer in the receiver front end circuitry. Functional operation of these circuits is as follows.

Phase–Locked Loop

The phase–locked loop (PLL) IC receives frequency selection data from the Station Control Module microprocessor. Once programmed, the PLL IC compares a 2.1 MHz reference signal (from the Station Control Module) with a feedback sample of the VCO output. Depending on whether the feedback signal is higher or lower in frequency than the 2.1 MHz reference, correction pulses are generated. (The width of these correction pulses is dependent on the amount of difference between the 2.1 MHz reference and the VCO feedback.)

The up/down pulses from the PLL IC are fed to a charge pump which outputs a dc voltage proportional to the pulse widths. This dc voltage is then low–pass filtered and fed to the VCO as the *CONTROL VOLTAGE*. (Note that if a frequency change is requested by the microprocessor, the low–pass loop filter is momentarily bypassed to accelerate the frequency change.)

VCO

The dc control voltage from the synthesizer is fed to a VCO which generates the 1st LO injection signal. The VCO responds to the dc control voltage and generates the appropriate rf signal. This signal is fed through a buffer amplifier and impedance matching and output to the 1st LO injection amplifier in the receiver front end circuitry. A sample of the injection signal is returned to the PLL IC (via a feedback buffer) to serve as a VCO feedback signal.

Receiver Front End Circuitry

The receive rf input is fed from the antenna through a low−pass filter to a 7−pole ceramic preselector filter which provides highly selective bandpass filtering. The output of the preselector filter is then amplified, image filtered, and fed to one input of the 1st mixer. The signal is mixed with the 1st LO injection signal (generated by the synthesizer/VCO circuitry) to produce a 73.35 MHz 1st i−f signal.

The 1st i−f signal is 2−pole bandpass filtered and fed to an amplifier. The amplifier gain (high or low) is determined by an AGC switch circuit that is controlled by an AGC select signal from the Station Control Module. The amplified 1st i−f signal is then 4−pole bandpass filtered and fed to the rf input of the custom receiver IC.

Custom Receiver IC Circuitry

The custom receiver IC provides additional amplification, filtering, a second down conversion, and finally analog to digital conversion of the 2nd i−f signal. The digital receive signal is then sent via differential driver circuitry to the Station Control Board. This data signal contains the necessary I and Q quadrature information, AGC information, and other data transfer information required by the Station Control Module to process the receive signal. (Note that the recovered audio signal is in digital format throughout the station circuitry, resulting in a more noise−free, linear receiver. Analog audio is present only in the external speaker driver circuitry on the Station Control Board and on the Wireline Interface Board at the phone line connections to and from the station.)

The remainder of the custom receiver IC circuitry consists of timing and tank circuits to support the internal oscillator, 2nd LO synthesizer circuitry, and 2nd i−f circuitry.

A serial bus allows data communications between the custom receiver IC and the DSP ASIC located on the Station Control Board. This bus allows the DSP ASIC to control various current and gain settings, establish the data bus clock rate, program the 2nd LO, and perform other control functions.

Address Decode and A/D Converter Circuitry

Address Decode Circuitry

The address decode circuitry allows the Station Control Board to use the address bus to select a specific device on a specific station board for control or data communications purposes (via the SPI bus). If the board select circuitry decodes address lines A2 thru A5 as the receiver module address, it enables the chip select circuitry. The chip select circuitry then decodes address lines A0 and A1 and generates chip select signals for the PLL and A/D converter and the *SYNTH ADAPT* signal to control the loop filter bypass switch in the synthesizer circuitry.

A/D Converter Circuitry

Analog signals from various strategic operating points throughout the receiver board are fed to the A/D converter, which converts them to a digital signal and, upon request by the Station Control Module, outputs the signal to the Station Control Module via the SPI bus.

Voltage Regulator Circuitry

The voltage regulator circuitry consists of +10V and two +5V regulators. The +10V regulator accepts a +14.2V dc input and generates a +10V dc operating voltage for the receiver board circuitry.

The +10V regulator output also feeds two +5V regulators which output Custom Analog +5V and Custom Digital +5V dc operating voltages to supply the custom receiver IC and Synthesizer IC. In addition, a +5V dc operating voltage is input at the backplane (from the station power supply) to supply Digital +5V to the remainder of the receiver board circuitry.

RECEIVER FRONT END CIRCUITRY
RF INPUT/OUTPUT CONNECTOR BRACKET (REAR OF STATION)
COAXIAL CABLE FROM N–TYPE CONNECTOR ON RF INPUT/OUTPUT CONNECTOR BRACKET TO LO–PASS FILTER
N–TYPE CONNECTOR
MINI–UHF CONNECTORS
RECEIVE RF FROM RX ANTENNA
LO–PASS FILTER
7–POLE CERAMIC PRESELECTOR FILTER
PREAMPLIFIER CIRCUITRY
IMAGE FILTER CIRCUITRY
1ST MIXER
73.35 MHZ 1ST I–F
AGC SELECT FROM STATION CONTROL MODULE
AGC SWITCH
HIGH
LOW
2–POLE BANDPASS FILTER
4–POLE BANDPASS FILTER
INJECTION FILTER
1ST LO INJECTION AMPLIFIER
VCO FEEDBACK
1ST LO INPUT
ADDRESS DECODE & A/D CONVERTER CIRCUITRY
ADDRESS BUS FROM STATION CONTROL MODULE
A0 & A1
A2–A5
CHIP SELECT DECODE CIRCUITRY
BOARD SELECT DECODE CIRCUITRY
CHIP SELECT
VARIOUS SIGNALS FROM RECEIVER BOARD TO BE MONITORED
A/D CONVERTER
SPI BUS TO/FROM STATION CONTROL MODULE
SPI BUS (CLOCK & DATA)
SPI BUS (CLOCK & DATA)
SPI BUS (CLOCK & DATA)
REGULATOR CIRCUITRY
+14.2V FROM BACKPLANE
+10V REGULATOR
+5V REGULATOR
+5V REGULATOR
CUSTOM/SYNTH DIGITAL +5V SOURCE
+10V SOURCE
CUSTOM ANALOG +5V SOURCE
CUSTOM RECEIVER IC CIRCUITRY
73.35 MHZ 1ST I–F
P/O P2801
77
P/O P2802
78
DIFF DATA TO STATION CONTROL MODULE
CUSTOM RECEIVER IC
DRIVER CIRCUITRY
450 KHZ FILTER CIRCUITRY
14.4 MHZ TIMING CIRCUITRY
2ND LO VCO CIRCUITRY
SERIAL BUS TO/FROM STATION CONTROL MODULE
2.1 MHZ REFERENCE
SYNTHESIZER CIRCUITRY
CHIP SELECT
P/O P2801
2.1 MHZ REF FROM SCM
65
BUFFER
2.1 MHZ
PHASE LOCKED LOOP IC
R_{IN}
F_{IN}
UP
DOWN
VCO FEEDBACK
FREQUENCY CHANGE FILTER BYPASS (ANALOG SWITCHES)
SYNTH ADAPT
CHARGE PUMP
LO–PASS LOOP FILTER
CONTROL VOLTAGE
(+2.5 TO +7.5 V DC)
VCO FEEDBACK BUFFER
VCO FEEDBACK
2.1 MHZ REFERENCE
VCO CIRCUITRY
+10 V
SUPER FILTER
+9.1 V
OSCILLATOR
BUFFER AMP
OUTPUT IMPEDANCE MATCHING

Figure 2. *Quantro/Quantar* 800 MHz Receiver Module Functional Block Diagram

MOTOROLA

RECEIVER MODULE

Includes TRF6552G Receiver Board

1 DESCRIPTION

The *Quantar/Quantro* 900 MHz Receiver Module is described in this section. A general description, identification of controls, indicators, and inputs/outputs, a functional block diagram, and functional theory of operation are provided. The information provided is sufficient to give service personnel a functional understanding of the module, allowing maintenance and troubleshooting to the module level. (Refer also to the Maintenance and Troubleshooting section of this manual for detailed troubleshooting procedures for all modules in the station.)

General Description

The Receiver Module provides the receiver functions for the *Quantar/Quantro* 900 MHz station. The receiver module is comprised of a Receiver Board and a ceramic preselector (mounted on board), all contained within a slide−in module housing. The receiver module performs highly selective bandpass filtering and dual down conversion of the station receive rf signal. A custom receiver IC then performs an analog to digital conversion of the received signal and outputs a differential data signal to the Station Control Module.

Overview of Circuitry

The receiver module contains the following circuitry:

- Frequency Synthesizer Circuitry— consisting of a phase−locked loop and VCO, generates the 1st LO injection signal
- Ceramic Preselector Filter — provides 7−pole bandpass filtering of the station receive rf input
- Receiver Front End Circuitry — performs filtering, amplification, and the 1st down conversion of the receive rf signal
- Custom Receiver IC Circuitry — consists of a custom IC which performs the 2nd down conversion, filtering, amplification, and analog to digital conversion of the receive signal
- Address Decode & A/D Converter Circuitry — performs address decoding to provide board and chip select signals; also converts analog status signals to digital format for transfer to Station Control Module
- Local Power Supply Regulation — accepts +14.2V dc input and outputs +10V and +5V dc operating voltages

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2 CONTROLS, INDICATORS, AND INPUTS/OUTPUTS

Figure 1 shows the receiver module controls, indicators, and all input and output external connections.

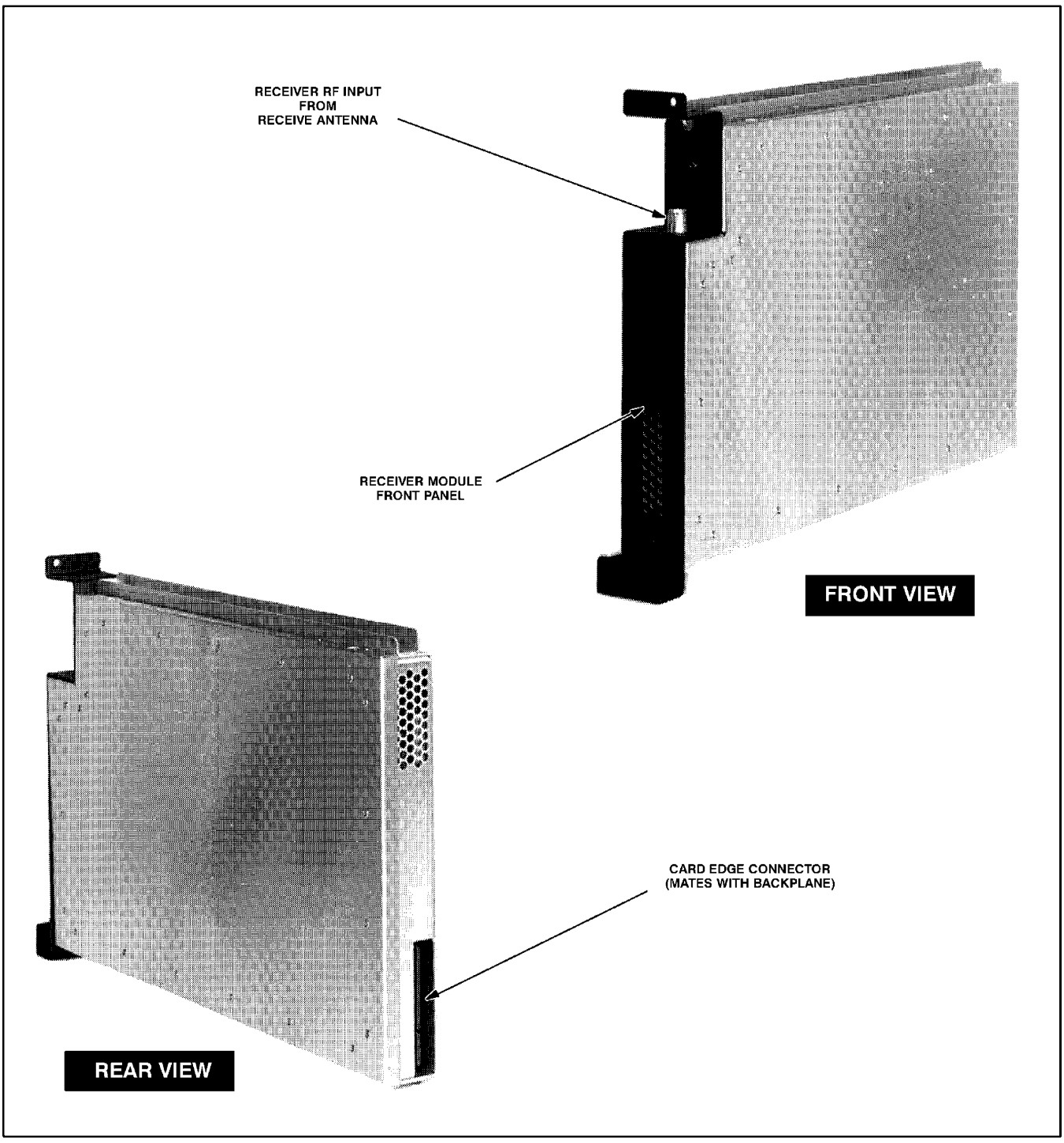

Figure 1. *Quantar/Quantro* 900 MHz Receiver Module Controls, Indicators, and Inputs/Outputs

3 FUNCTIONAL THEORY OF OPERATION

The following theory of operation describes the operation of the receiver circuitry at a functional level. The information is presented to give the service technician a basic understanding of the functions performed by the module in order to facilitate maintenance and troubleshooting to the module level. Refer to Figure 2 for a block diagram of the receiver module.

Synthesizer and VCO Circuitry

Introduction

The synthesizer and VCO circuitry generate the 1st LO injection signal for the 1st mixer in the receiver front end circuitry. Functional operation of these circuits is as follows.

Phase–Locked Loop

The phase–locked loop (PLL) IC receives frequency selection data from the Station Control Module microprocessor. Once programmed, the PLL IC compares a 2.1 MHz reference signal (from the Station Control Module) with a feedback sample of the VCO output. Depending on whether the feedback signal is higher or lower in frequency than the 2.1 MHz reference, correction pulses are generated. (The width of these correction pulses is dependent on the amount of difference between the 2.1 MHz reference and the VCO feedback.)

The up/down pulses from the PLL IC are fed to a charge pump which outputs a dc voltage proportional to the pulse widths. This dc voltage is then low–pass filtered and fed to the VCO as the *CONTROL VOLTAGE*. (Note that if a frequency change is requested by the microprocessor, the low–pass loop filter is momentarily bypassed to accelerate the frequency change.)

VCO

The dc control voltage from the synthesizer is fed to a VCO which generates the 1st LO injection signal. The VCO responds to the dc control voltage and generates the appropriate rf signal. This signal is fed through a buffer amplifier and impedance matching and output to the 1st LO injection amplifier in the receiver front end circuitry. A sample of the injection signal is returned to the PLL IC (via a feedback buffer) to serve as a VCO feedback signal.

Receiver Front End Circuitry

The receive rf input is fed from the antenna through a low−pass filter to a 7−pole ceramic preselector filter which provides highly selective bandpass filtering. The output of the preselector filter is then amplified, image filtered, and fed to one input of the 1st mixer. The signal is mixed with the 1st LO injection signal (generated by the synthesizer/VCO circuitry) to produce a 73.35 MHz 1st i−f signal.

The 1st i−f signal is 2−pole bandpass filtered and fed to an amplifier. The amplifier gain (high or low) is determined by an AGC switch circuit that is controlled by an AGC select signal from the Station Control Module. The amplified 1st i−f signal is then 4−pole bandpass filtered and fed to the rf input of the custom receiver IC.

Custom Receiver IC Circuitry

The custom receiver IC provides additional amplification, filtering, a second down conversion, and finally analog to digital conversion of the 2nd i−f signal. The digital receive signal is then sent via differential driver circuitry to the Station Control Board. This data signal contains the necessary I and Q quadrature information, AGC information, and other data transfer information required by the Station Control Module to process the receive signal. (Note that the recovered audio signal is in digital format throughout the station circuitry, resulting in a more noise−free, linear receiver. Analog audio is present only in the external speaker driver circuitry on the Station Control Board and on the Wireline Interface Board at the phone line connections to and from the station.)

The remainder of the custom receiver IC circuitry consists of timing and tank circuits to support the internal oscillator, 2nd LO synthesizer circuitry, and 2nd i−f circuitry.

A serial bus allows data communications between the custom receiver IC and the DSP ASIC located on the Station Control Board. This bus allows the DSP ASIC to control various current and gain settings, establish the data bus clock rate, program the 2nd LO, and perform other control functions.

Address Decode and A/D Converter Circuitry

Address Decode Circuitry

The address decode circuitry allows the Station Control Board to use the address bus to select a specific device on a specific station board for control or data communications purposes (via the SPI bus). If the board select circuitry decodes address lines A2 thru A5 as the receiver module address, it enables the chip select circuitry. The chip select circuitry then decodes address lines A0 and A1 and generates chip select signals for the PLL and A/D converter and the *SYNTH ADAPT* signal to control the loop filter bypass switch in the synthesizer circuitry.

A/D Converter Circuitry

Analog signals from various strategic operating points throughout the receiver board are fed to the A/D converter, which converts them to a digital signal and, upon request by the Station Control Module, outputs the signal to the Station Control Module via the SPI bus.

Voltage Regulator Circuitry

The voltage regulator circuitry consists of +10V and two +5V regulators. The +10V regulator accepts a +14.2V dc input and generates a +10V dc operating voltage for the receiver board circuitry.

The +10V regulator output also feeds two +5V regulators which output Custom Analog +5V and Custom Digital +5V dc operating voltages to supply the custom receiver IC and Synthesizer IC. In addition, a +5V dc operating voltage is input at the backplane (from the station power supply) to supply Digital +5V to the remainder of the receiver board circuitry.

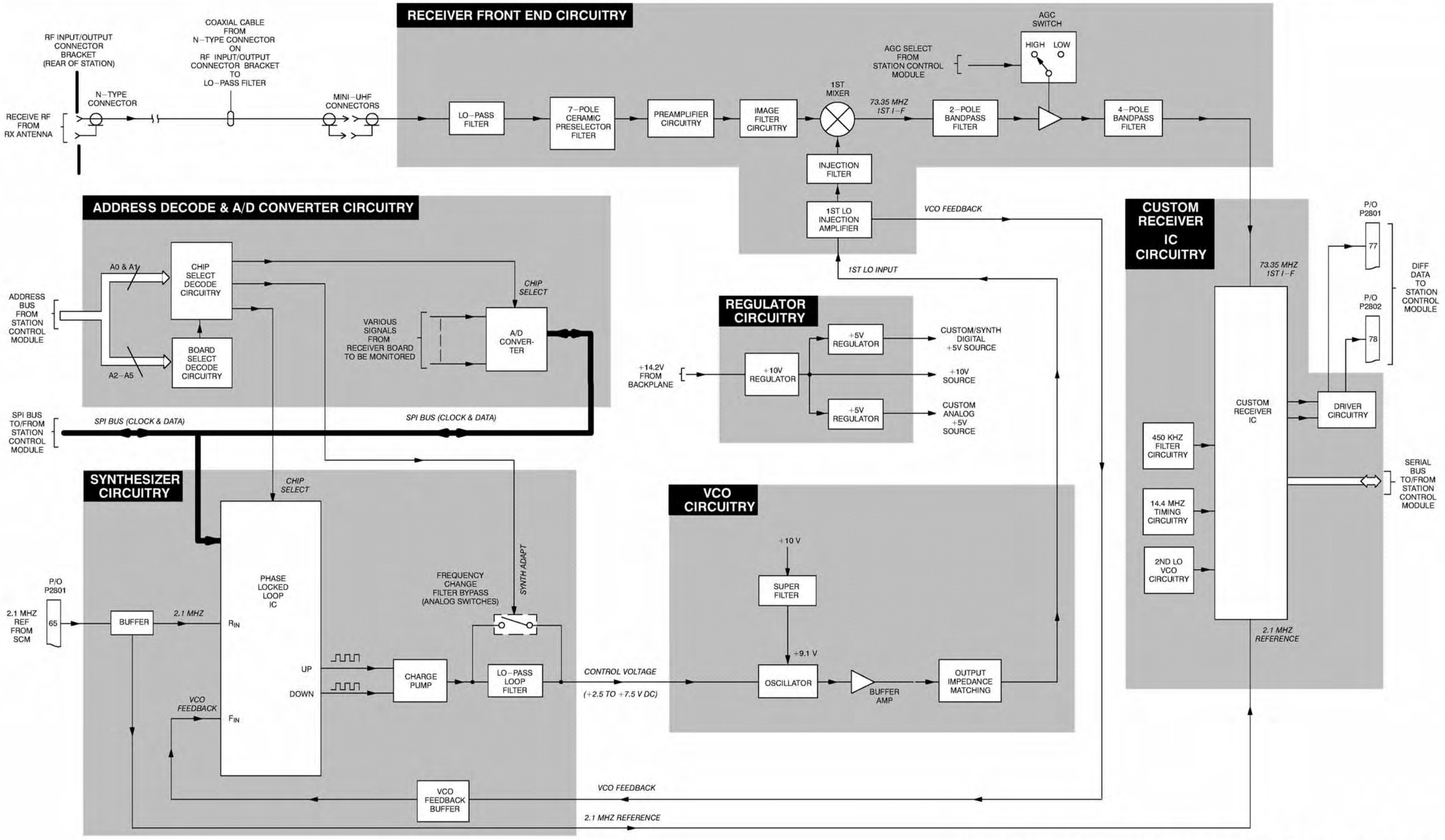

Figure 2. *Quantar/Quantro* 900 MHz Receiver Module Functional Block Diagram

END OF PART 5