MOTOROLA

STATION CONTROL MODULE

MODELS CLN6960E
CLN6961E
CLN1614C

1 DESCRIPTION

The Models CLN6960E, CLN6961E, and CLN1614C station control modules (SCM) are described in this section. A general description, identification of controls, indicators, and inputs/outputs, a functional block diagram, and functional theory of operation are provided. The information provided is sufficient to give service personnel a functional understanding of the module, allowing maintenance and troubleshooting to the module level. (Refer also to the *Maintenance and Troubleshooting* section of this manual for detailed troubleshooting procedures for all modules in the station.)

General Description

The SCM serves as the main controller for the station. The SCM board contains a 68EN360 microprocessor, a 56002 digital signal processor (DSP), and support circuitry which combine to provide signal processing and operational control over the other station modules. The SCM also contains the station operating software (stored in FLASH memory) and codeplug which define the personality of the station, including system capabilities (ASTRO, IntelliRepeater, etc.) and operating parameters such as output power and operating frequency.

The CLN6961 and CLN1614 provide conventional operation along with MRTI and 6809 trunking capabilities. The CLN6960 is a full-featured model and is required for use in IntelliRepeater applications. Specific differences between the models are shown throughout the functional block diagram (Figure 2).

Overview of Circuitry

The SCM contains the following circuitry:

- **Host Microprocessor** (µP)— The 68EN360 µP is the central controller of the SCM and station
- **Non-Volatile Memory** — consists of a FLASH SIMM module that contains the station operating software and data, and an EEPROM that contains the station codeplug data
- **DRAM Memory** — Dynamic RAM into which station software is downloaded and executed

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- **External Line Interface Circuitry** — provides interface between the SCM and external devices such as IntelliRepeater DLAN ports, RSS port, an Ethernet port, and miscellaneous backplane connectors
- **Digital Signal Processor (DSP) and DSP ASIC Circuitry** — performs high-speed processing of audio and signaling data signals
- **Station Reference Circuitry** — generates the 2.1 MHz reference signal used throughout the station
- **HDLC Bus Control Circuitry** — provides bus control to allow host communications port SCC1 to communicate with the wireline interface board (WIB) and other optional modules via the HDLC interprocessor communications bus
- **Audio Interface Circuitry** — routes the various audio input signals (such as microphone, wireline, and receiver audio) to output devices (such as external speaker, built-in local speaker, and exciter modulation inputs)
- **Input/Output Ports Circuitry** — two 32-line output buses allow miscellaneous control signals to be sent to various circuits throughout the station; two 32-line input buses allow miscellaneous inputs to be received from throughout the station
- **Front Panel LEDs and Switches** — general purpose input/output ports control eight status LEDs and accept inputs from four momentary switches, all located on the SCM front panel
- **Supply Voltage Circuitry** — contains filtering and regulator circuitry which accepts +14.2 V and +5 V from backplane and generates the operating voltages required by the SCM circuitry

2 CONTROLS, INDICATORS, AND INPUTS/OUTPUTS

Figure 1 shows the SCM controls, indicators, and all input and output external connections.

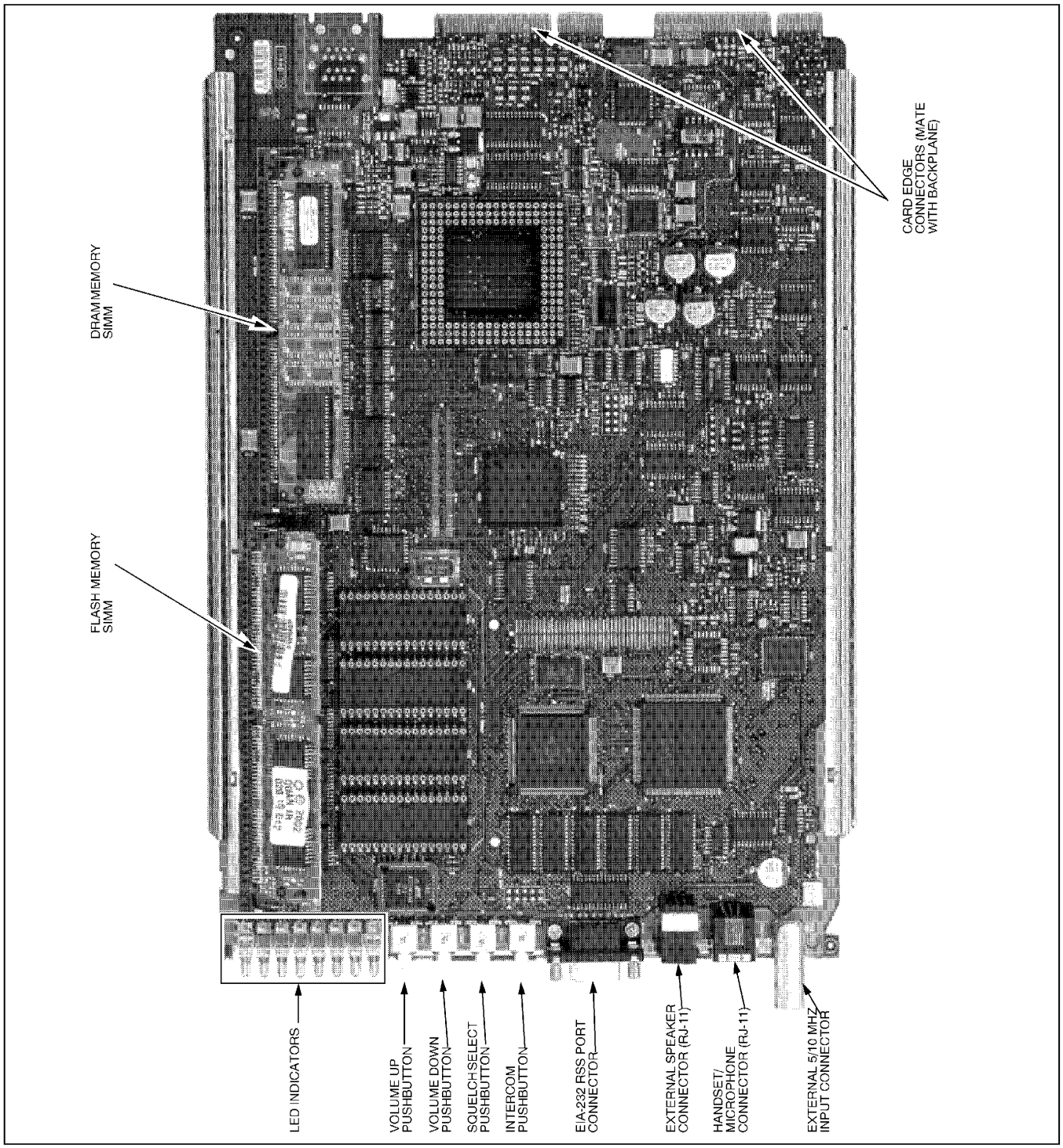

Figure 1 Station Control Module Controls, Indicators, and Inputs/Outputs (CLN6960E shown)

3 FUNCTIONAL THEORY OF OPERATION

The following theory of operation describes the operation of the SCM circuitry at a functional level. The information is presented to give the service technician a basic understanding of the functions performed by the module in order to facilitate maintenance and troubleshooting to the module level. Refer to Figure 2 for a block diagram of the SCM.

Host Microprocessor

Overview

The host µP serves as the main controller for the SCM (and station). The host µP, an MC68EN360 running at a clock speed of 25 MHz, controls the operation of the station as determined by the station software (contained in a FLASH SIMM module) and the station codeplug (EEPROM).

Communications Buses

The host µP provides six general-purpose serial communications buses, as follows:

- **SCC1** — Used as Ethernet port for high-speed communications,either to connect to the Ethernet local network of an IntelliRepeater trunking site or to allow station software to be downloaded from a local PC into the FLASH memory
- **SCC2** — Used as communications port to allow the station to connect into the local network of an IntelliRepeater trunking site; external connections are provided by a 9-pin D-type connector (#19) located on backplane
- **SCC3** — Used as the interprocessor communications bus (HDLC protocol) to allow the host µP to communicate with the WIB and other optional modules
- **SCC4** — Used as RS-232 port for connections to external equipment, such as a modem
- **SMC1** — Used as RS-232 port for RSS communications (9-pin D-type connector #20 on backplane)
- **SMC2** — Used as RS-232 port for RSS communications (9-pin D-type connector located on SCM front panel)

Address and Data Buses

The µP is equipped with a 28-line address bus used to access the non-volatile memory, DRAM memory, and provide control (via memory mapping) for other circuitry in the SCM. A 32-line data bus (buffered for the non-volatile memory) is used to transfer data to/from the SCM memory, as well as other SCM circuitry.

SPI Bus

The host µP also controls the SPI bus, a general-purpose communications bus that allows the host µP to communicate with other modules in the station.

DRAM Controller

The host μP provides signals necessary to access and refresh the DRAM memory.

25 MHz Clock Circuitry

A crystal-controlled 25 MHz clock circuit and buffer provide the 25 MHz clock signal to the host μP.

Non-Volatile Memory

Station Software FLASH Memory

The station software resides in a FLASH SIMM module (1M x 32 for CLN6960E, 512k x 32 for CLN6961E and CLN1614C). The FLASH SIMM is accessed by the host μP via the 28-line host buffered address bus and the 32-line host buffered data bus.

Codeplug EEPROM

The data which determines the station personality resides in an 8K x 8 codeplug EEPROM. Stations are shipped from the factory with generic default data programmed into the codeplug EEPROM. Field programming is performed during installation using the Radio Service Software (RSS) program to enter additional customer-specific data, such as site output power, time-out timer settings, etc.

DRAM Memory

Each SCM contains a 2MX32 DRAM SIMM into which the station software code is downloaded and run. The DRAM also provides short-term storage for data generated/required during normal operation. Read and write operations are performed using the host buffered address and host buffered data buses.

The DRAM memory locations are sequentially refreshed by the column and row signals from the host μP.

External Line Interface Circuitry

IntelliRepeater DLAN Network Port

A DLAN port is provided on the station backplane to allow the station to connect into the local network of an IntelliRepeater trunking site. This DLAN port is provided by host μP serial communication bus SCC2.

SCC2 communicates with an RS-485 bus transceiver, which provides DLAN+ and DLAN– signals. These signals are connected to a 9-pin D-type connector (#19) located on the station backplane, which typically mates with a PhoneNET adapter module connected into the IntelliRepeater local network.

Ethernet Port

An Ethernet port is provided via a BNC connector on the station backplane which allows the station to connect into the Ethernet local network of an IntelliRepeater trunking site. The Ethernet port may also be used to allow station software to be downloaded from a local PC into the FLASH SIMM module. This Ethernet port is provided by host µP serial communication bus SCC1.

General Purpose RS232 Serial Port

A general purpose RS-232 communications port is provided by host µP serial communication bus SCC4. This port is available at a DB-25 connector (#15) located on the station backplane, and may be used to connect external equipment such as an external modem.

RSS Port (Backplane)

A 9-pin D-type connector (#20) is provided on the station backplane to allow service personnel to connect a PC loaded with the Radio Service Software (RSS) and perform programming and maintenance tasks. The RSS port may also be used to allow station software to be downloaded from a local PC into the FLASH SIMM module. This RSS port is provided by host µP serial communication bus SMC1 which communicates with the RSS terminal via EIA-232 Bus Receivers/ Drivers.

RSS Port (Front Panel)

A 9-pin D-type connector is provided on the SCM front panel to allow service personnel to connect a PC loaded with the Radio Service Software (RSS) and perform programming and maintenance tasks. The RSS port may also be used to allow station software to be downloaded from a local PC into the FLASH SIMM module. This RSS port is provided by host µP serial communication bus SMC2 which communicates with the RSS terminal via EIA-232 Bus Receivers/ Drivers.

Digital Signal Processor (DSP) and DSP ASIC Circuitry

General

All station transmit and receive audio/data is processed by the DSP and related circuitry. This circuitry includes the DSP IC, the DSP ASIC, and the DSP ASIC interface circuitry. All audio signals in to and out of the DSP are in digitized format.

Inputs to the DSP circuitry are:

- Digitized receive signals from the receiver module
- Audio from handset or microphone connected to appropriate SCM front panel connector; signal is digitized by CODEC IC (p/o audio interface circuitry) before being sent to DSP via audio interface bus
- Digitized voice audio/data from WIB and other optional modules via TDM bus

- ASTRO modem data from WIB via HDLC bus
- 6809/MRTI transmit audio

Outputs from the DSP circuitry are:

- Digitized voice audio/data from DSP to WIB and other optional modules via TDM bus
- Digitized voice audio from DSP to external speaker, built-in speaker, or handset earpiece via audio interface bus and audio interface circuitry
- Digitized voice audio/data from DSP to exciter module (modulation signals) via audio interface bus and audio interface circuitry
- 6809/MRTI transmit audio

Digital Signal Processor (DSP)

The DSP, a 56002 operating at an internal clock speed of 60 MHz, accepts and transmits digitized audio to/from the various modules in the station. The DSP provides address and data buses to receive/transmit digitized audio (via the DSP ASIC) and to access the DSP program and signal processing algorithms contained in three 32K x 8 SRAM ICs.

Three additional 32K x 8 SRAM ICs are provided for data storage.

DSP ASIC

The DSP ASIC operates under control of the DSP to provide a number of functions, as follows:

- Interfaces with the DSP via the DSP address and data buses
- Accepts 16.8 MHz signal from Station Reference Circuitry and outputs a 2.1 MHz reference signal used throughout the station
- Provides interfaces for the HDLC bus, TDM bus, and serial bus used to communicate with the Receiver Module
- Accepts digitized data from Receiver Module via DSP ASIC Interface Circuitry
- Provides interfaces for several A/D and D/A converters

Station Reference Circuitry

Note: *Two BNC connectors (one 50 Ω input located on SCM front panel, one high impedance input located on the station backplane) are provided to allow an external 5/10 MHz source to be connected to the OSC_{in} input to the PLL to perform frequency netting. Refer to the Maintenance section in this manual for recommended intervals and procedures for netting the station reference.*

The station reference circuitry consists of a phase-locked loop (PLL) comprised of a high-stability VCO and a PLL IC. The output of the VCO is a 16.8 MHz signal which is fed to the DSP ASIC. The ASIC divides the signal by 8 and outputs a 2.1 MHz signal which is separated and buffered by a splitter and output to the Exciter Module and Receiver Module as 2.1 MHz REF.

The Station Reference Circuitry may operate in one of three modes:

- **Normal Mode** — In this mode, the control voltage is turned off (via control voltage enable switch) and the high-stability VCO operates in an open loop mode; stability of the VCO in this mode is 1 PPM per year.

- **Manual Netting Mode** — Periodically, an external 5/10 MHz source is required to fine tune, or "net", the 16.8 MHz reference signal. In this mode, the PLL compares the 5/10 MHz reference and a sample of the 16.8 MHz VCO output and generates up/down pulses. The host μP reads the pulses (via SPI bus) and sends correction signals (via SPI bus) to the VCO to adjust the output frequency to 16.8 Mhz ±0.3 ppm.
- **High-Stability Mode** — For some systems, such as simulcast systems, the free-running stability of the VCO is unacceptable for optimum system performance. Therefore, an external 5/10 MHz source is connected permanently to one of the BNC connectors. In this mode, the PLL compares the 5/10 MHz reference and a sample of the 16.8 MHz VCO output and generates a dc correction voltage. The control voltage enable switch is closed, allowing the control voltage from the PLL to adjust the high-stability VCO frequency to 16.8 MHz ±0.3 ppm. The VCO operates in this closed loop mode and is continually being frequency controlled by the control voltage from the PLL.

HDLC Bus Control Circuitry

The HDLC bus control circuitry provides high-impedance buffering and data routing for the interprocessor communications bus (a serial data bus implementing HDLC protocol). This bus allows the host μP to communicate with the host μP located on the WIB and other optional modules via an interprocessor communications bus.

Audio Interface Circuitry

General

The audio interface circuitry interfaces external analog audio inputs and outputs with the DSP circuitry.

External Audio Sources

A multiplexer, under control of the host μP, is used to select one of eight possible external audio input sources (four for diagnostic loopback signals, two for future use, one for 6809/MRTI transmit audio, and one for handset or microphone audio). The selected audio source signal is converted to a digital signal by the A/D portion of the CODEC IC and sent to the DSP ASIC via the audio interface bus. The DSP circuitry processes the signal and routes it to the desired destination.

External Audio Destinations

Digitized audio from the DSP circuitry is applied to the D/A portion of the CODEC IC and is then sent to one of four external devices:

- External Speaker — connects to RJ-11 jack (||) located on SCM front panel
- Handset Earpiece/Microphone — connects to RJ-11 jack ( ) located on SCM front panel

- Local Built-In Speaker — internal speaker and ½ W audio amplifier; may be switched on/off and volume controlled by using volume up ( ) and down ( ) buttons on SCM front panel
- J14 on Station Backplane — 6809/MRTI receive audio output to external MRTI Module

Exciter Modulation Signals

Digitized audio/data intended to be transmitted from the station is sent from the DSP circuitry to a D/A converter via the TX/Voice Audio signal (part of the serial synchronous interface bus, connected between the DSP and the DSP ASIC). The digitized signal is converted to analog, level shifted and amplified, and fed to a 0-6 kHz filter. The output of the filter is then fed to one of the inputs of a multiplexer. The output of the multiplexer is fed to two individual digitally controlled potentiometers (each of which is adjusted by the host μP via the SPI Bus) and applied to the exciter module as modulation signals VCO MOD AUDIO and REF MOD AUDIO.

Input/Output Ports

Input Ports

Two general-purpose 32-line input ports are provided to allow various input signals from the SCM and station circuitry to be accepted and sent to the host μP. The two ports (I/O Port P0 In and I/O Port P1 In) are each comprised of 32 lines which come from circuitry in the SCM as well as other modules in the station via the backplane. The buses are received by buffers which make the data available to the host μP via the host buffered data bus. Typical inputs include the pushbutton switches located on the SCM front panel and the MIC PTT signal from the handset/microphone.

Output Ports

Two general-purpose 32-line output ports are provided to allow various control signals from the host μP to be output to the SCM and station circuitry via the backplane. The two ports (I/O Port P0 Out and I/O Port P1 Out) are each comprised of 32 lines which come from the host buffered data bus via latches. Typical output control signals include the control lines for the eight LEDs located on the SCM front panel and the local speaker enable signal.

6809/MRTI Interface Circuitry

6809 Trunking Interface

TX DATA from the 6809 trunking controller is received by the station via J14 on the station backplane. The signal is routed through nominal filtering on the 6809/MRTI interface circuitry and fed to the audio interface circuitry. The T DATA signal is then waveshaped/filtered and fed to an A/D converter, which outputs a digital signal to the DSP via the audio interface bus.

6809 RX AUDIO is output from the DSP to the local audio circuitry via the audio interface bus. The signal is amplified, filtered, buffered, and output through nominal filtering on the 6809/MRTI interface circuitry to the 6809 trunking controller via J14 on the station backplane.

MRTI Interface

MRTI AUDIO from an external MRTI module is received by the station via J14 on the station backplane. The signal is routed through the 6809/MRTI interface circuitry and fed to one input of an 8-to-1 multiplexer. If selected, the MRTI TX AUDIO signal is converted to a digital signal by the A/D portion of the CODEC IC and sent to the DSP ASIC via the audio interface bus.

MRTI RX AUDIO is output from the DSP to the local audio circuitry via the audio interface bus. The signal is amplified, filtered, buffered, and output through the 6809/MRTI interface circuitry to the external MRTI module via J14 on the station backplane.

Front Panel LEDs and Switches

LEDs

Note: *Refer to the Troubleshooting section of this manual for complete details on the interpretation of the LEDs.*

Eight status LEDs on the SCM front panel provide visual indications of various station operating conditions.The LEDs are controlled by eight lines from I/O Port P0 Out.

Switches

Note: *Refer to the Operation section of this manual for complete details on the use of the pushbutton switches.*

Four momentary contact pushbutton switches are provided on the SCM front panel to allow various station functions to be selected. Pressing a pushbutton causes a high to be sent to the host µP via I/O Port P0 In.

Supply Voltages Circuitry

The SCM contains on-board regulator and filtering circuitry to generate the various operating voltages required by the SCM circuitry. +14.2 V and +5V from the backplane are used as sources for the following supply voltage circuits:

- **+10V Regulator Circuitry** — provides +10 V dc and a +5 V reference voltage (½ of +10V) for the audio interface circuitry in the SCM.
- **VCCA Supply Circuitry** — provides VCCA (+5V) and a +2.5 V reference voltage (½ of VCCA) for the audio interface circuitry in the SCM.
- **Filtering Circuitry** — filters the +14.2 V and +5V from the backplane to provide A+ and VCC, respectively, for the SCM digital circuitry.

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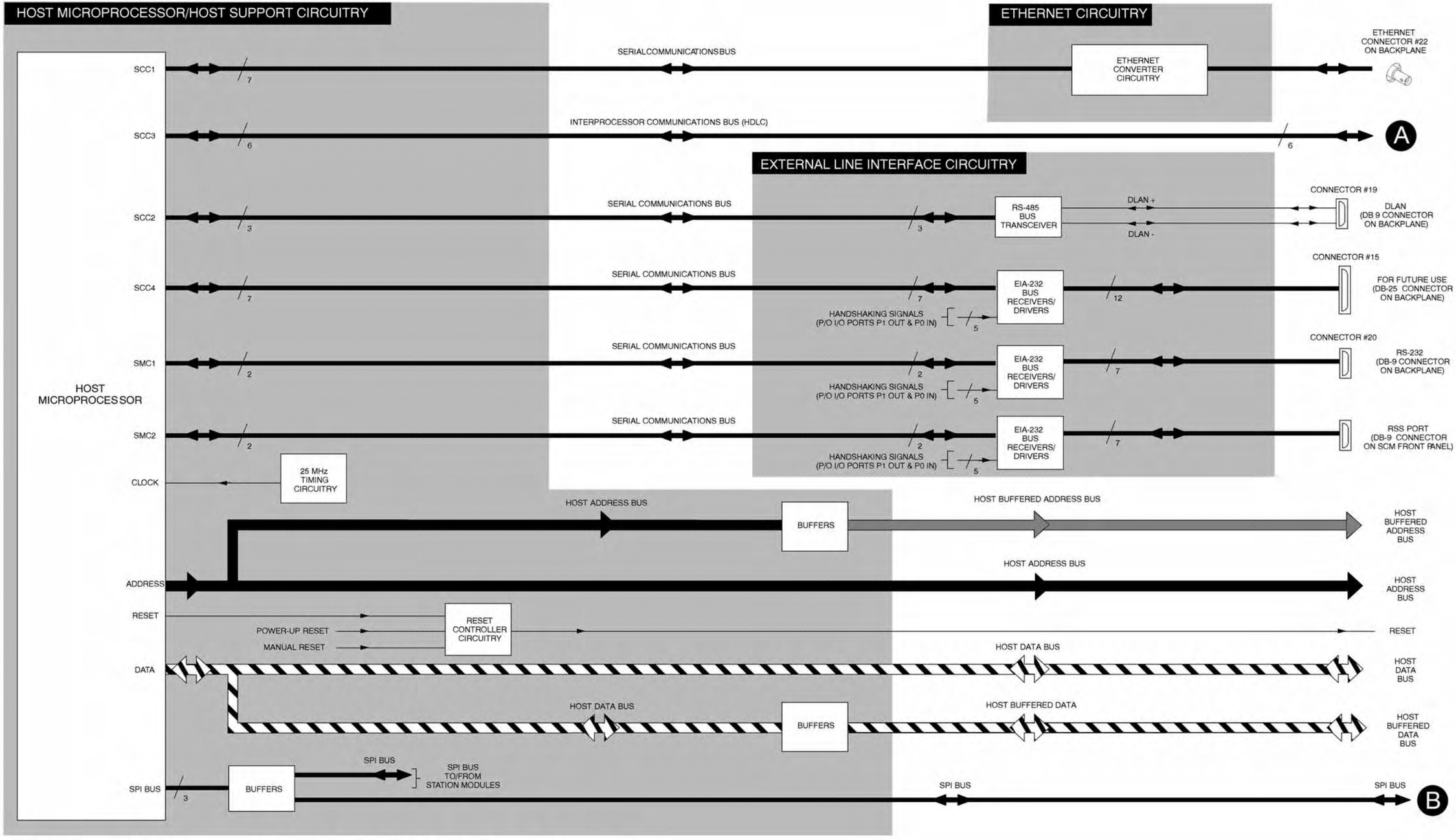


Figure 2 CLN6960E, CLN6961E, and CLN1614C Station Control Module Functional Block Diagram (1 of 5)

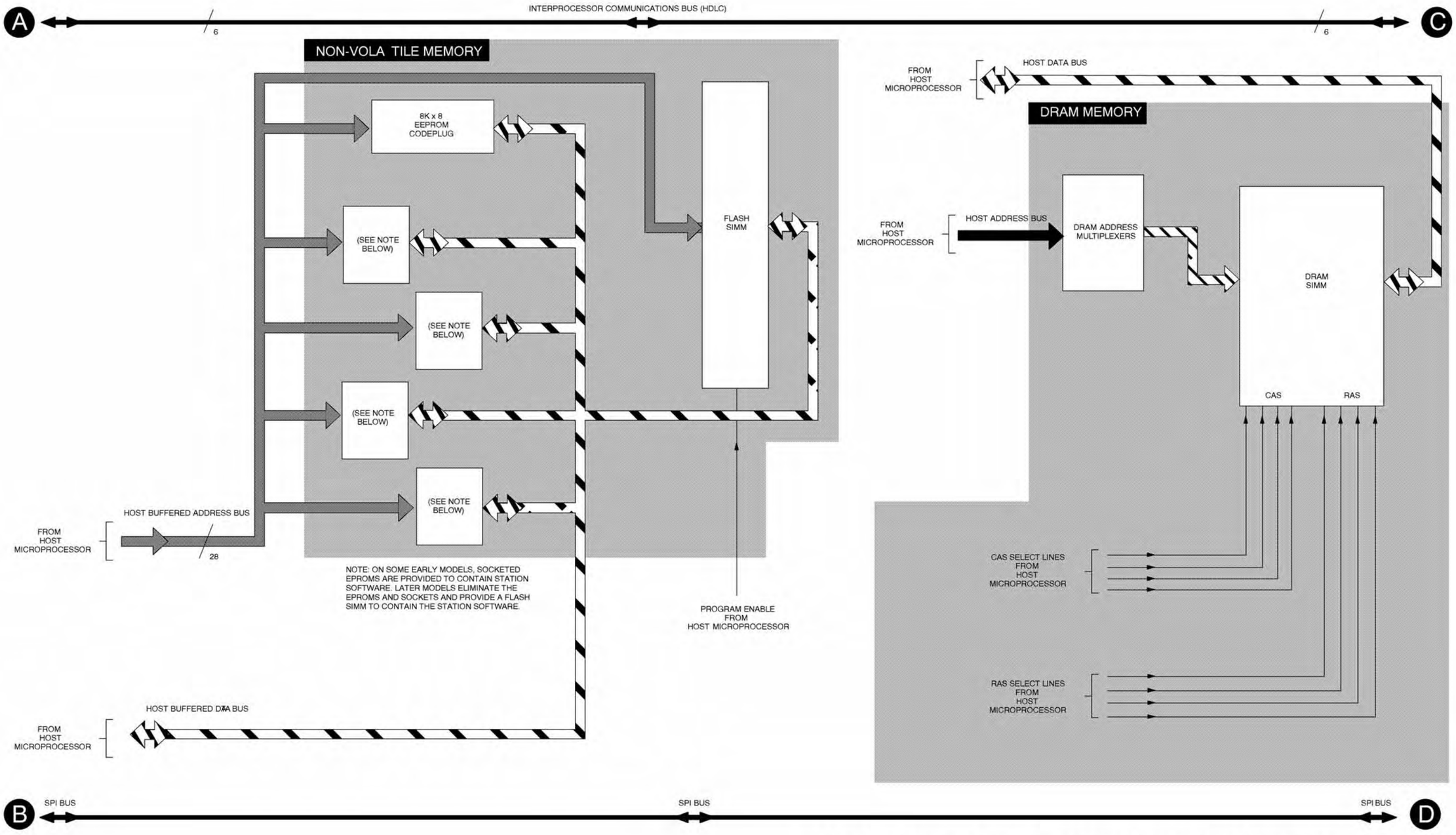


Figure 2 CLN6960E, CLN6961E, and CLN1614C Station Control Module Functional Block Diagram (2 of 5)

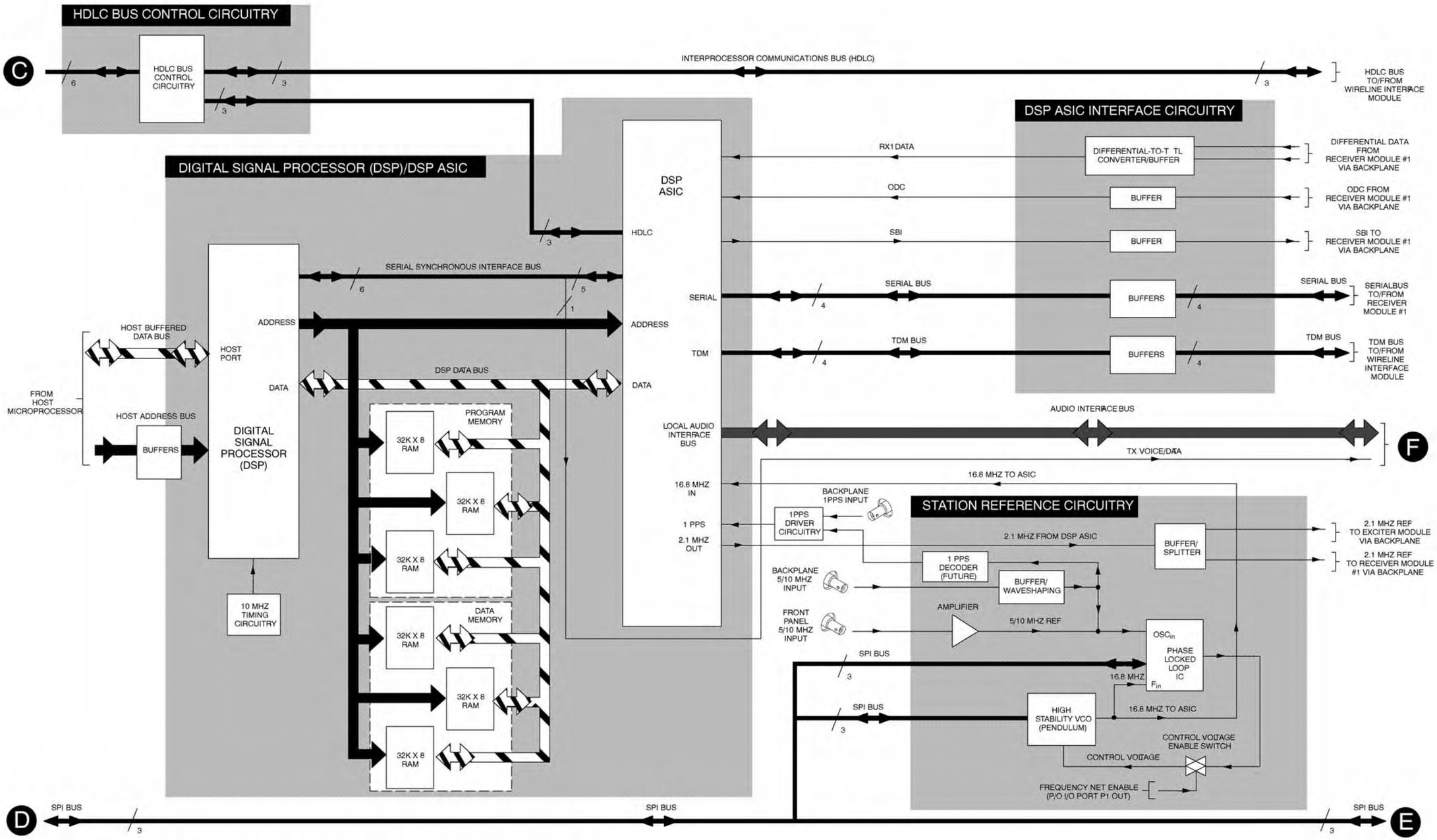


Figure 2 CLN6960E, CLN6961E, and CLN1614C Station Control Module Functional Block Diagram (3 of 5)

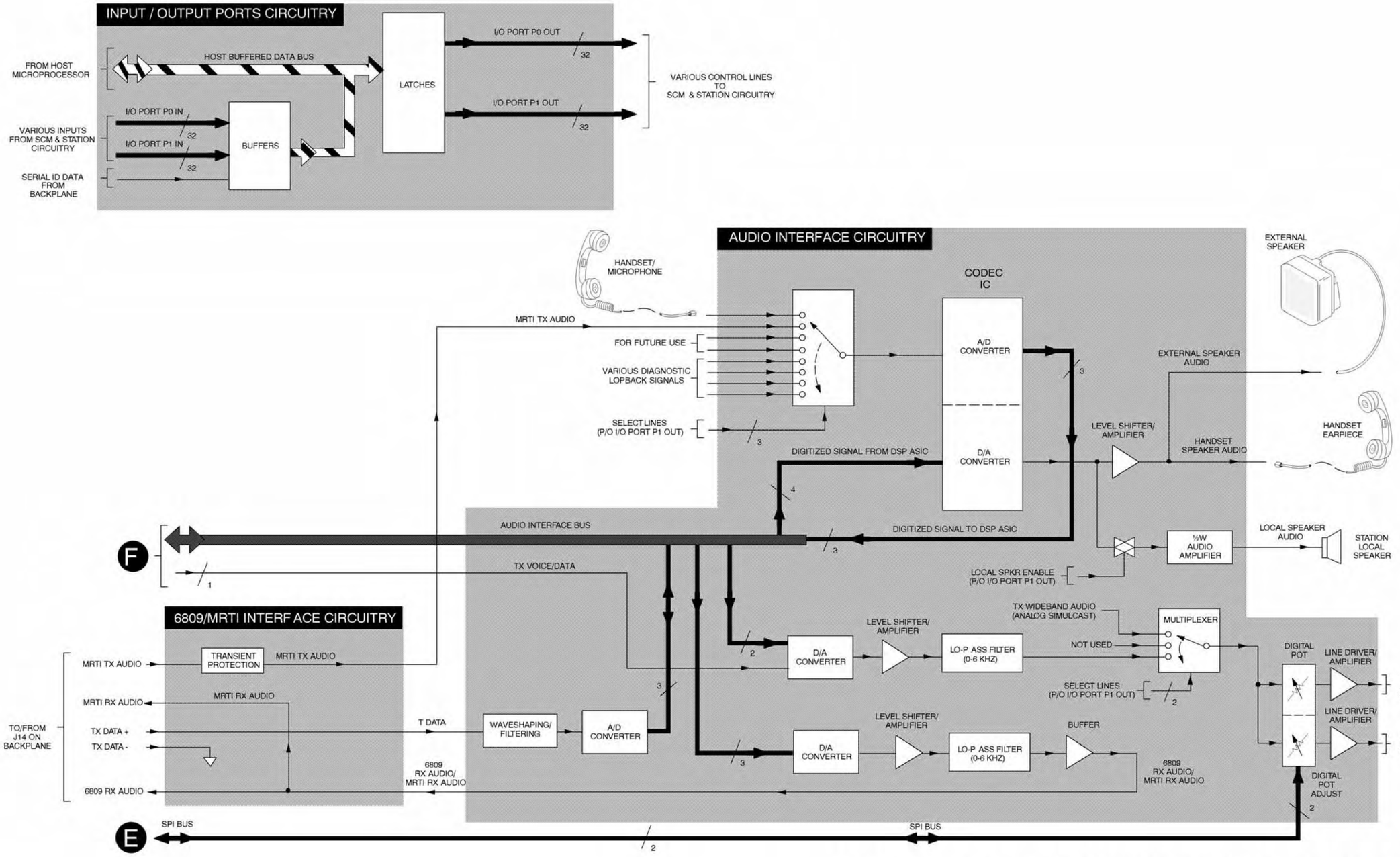
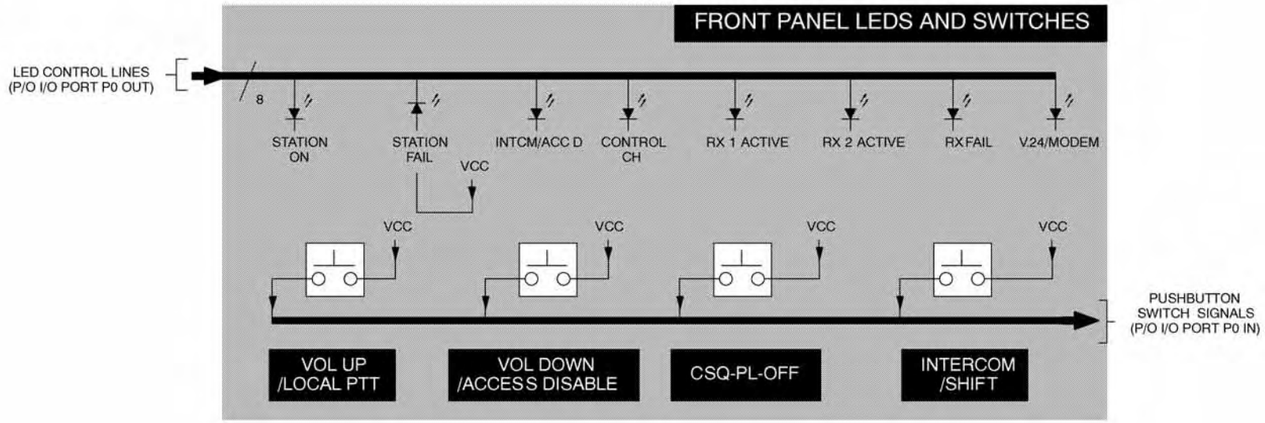


Figure 2 CLN6960E, CLN6961E, and CLN1614C Station Control Module Functional Block Diagram (4 of 5)



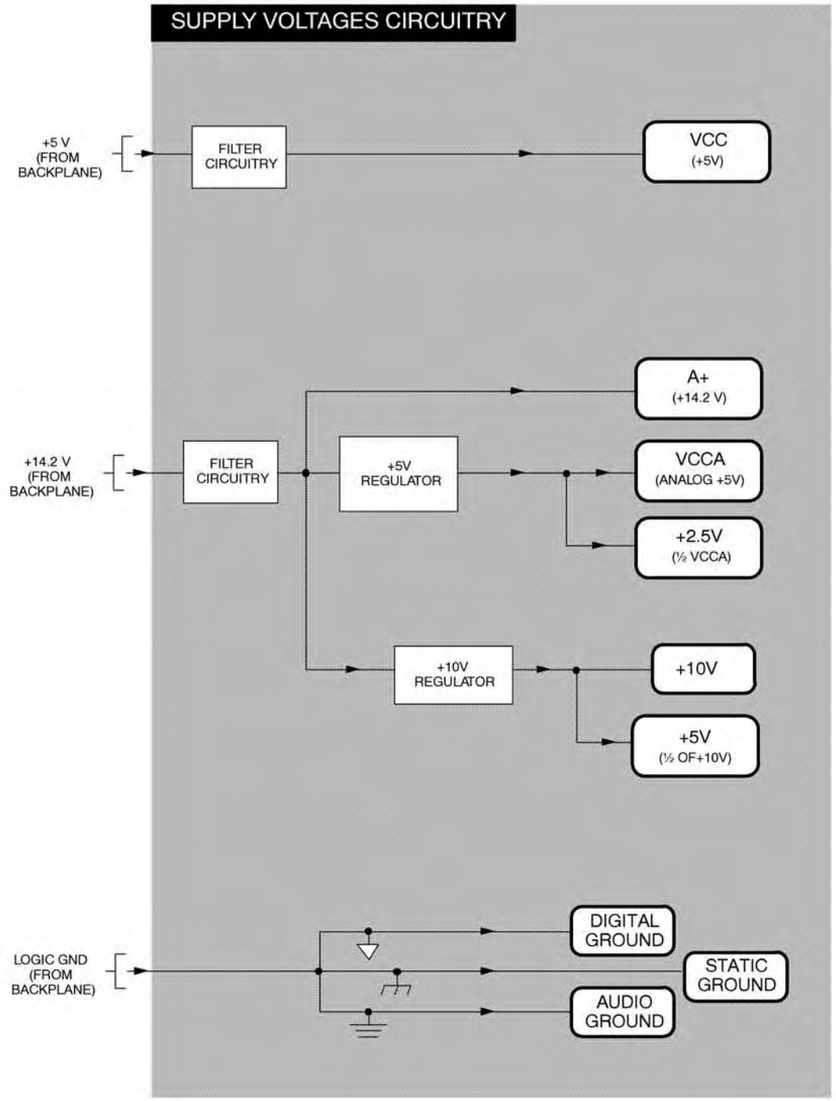


Figure 2 CLN6960E, CLN6961E, and CLN1614C Station Control Module Functional Block Diagram (5 of 5)

MOTOROLA

STATION CONTROL MODULE

MODELS CLN1614A
CLN1614B

1 DESCRIPTION

The Model CLN1614A and CLN1614B Station Control Module (SCM) is described in this section. A general description, identification of controls, indicators, and inputs/outputs, a functional block diagram, and functional theory of operation are provided. The information provided is sufficient to give service personnel a functional understanding of the module, allowing maintenance and troubleshooting to the module level. (Refer also to the Maintenance and Troubleshooting section of this manual for detailed troubleshooting procedures for all modules in the station.)

General Description

The SCM serves as the main controller for the station. Each SCM is comprised of two circuit boards (Control Board and LED Board), contained in a single slide-in housing. The two boards are connected via a multi-conductor ribbon cable.

The Control Board contains a 68EN360 microprocessor, a 56002 Digital Signal Processor, and support circuitry which combine to provide signal processing and operational control over the other station modules. The SCM also contains the station operating software (stored in FLASH memory) and codeplug which define the personality of the station, including system capabilities (*ASTRO*, *SECURENET*, etc.) and operating parameters such as output power and operating frequency.

The CLN1614A/B SCM provides conventional operation along with MRTI and 6809 trunking capabilities for use in *Quantar* and *Quantro* stations.

Note: *The CLN1614A uses tantalum capacitors and the CLN1614B uses ceramic capacitors. Otherwise, the two models are identical.*

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Overview of Circuitry

The SCM is comprised of two circuit boards, connected together via a multi-conductor ribbon cable. These boards contain circuitry as follows:

Control Board (CLN7060A)

- **Host Microprocessor** — 68EN360 µP which comprises the central controller of the SCM and station
- **Non–Volatile Memory** — consists of a FLASH SIMM module that contains the station operating software and data, and an EEPROM that contains the station codeplug data
- **DRAM Memory** — Dynamic RAM into which station software is downloaded and executed
- **External Line Interface Circuitry** — provides interface between the SCM and external devices such as the RSS port, an Ethernet port, and miscellaneous backplane connectors
- **Digital Signal Processor (DSP) and DSP ASIC Circuitry**— performs high-speed processing of audio and signaling data signals
- **Station Reference Circuitry** — generates the 2.1 MHz reference signal used throughout the station
- **HDLC Bus Control Circuitry** — provides bus control to allow Host Microprocessor communications port SCC1 to communicate with the Wireline Interface Board and other optional modules via the HDLC interprocessor communications bus
- **Audio Interface Circuitry** — Comprised of a Local Audio ASIC that routes the various audio input signals (such as microphone, wireline, and receiver audio) to output devices (such as external speaker, built–in local speaker, and exciter modulation inputs)
- **Input / Output Ports Circuitry** — two multi–line output buses allow miscellaneous control signals to be sent to various circuits throughout the station; two multi–line input buses allow miscellaneous inputs to be received from throughout the station
- **Supply Voltages Circuitry** — contains filtering and regulator circuitry which accepts +14.2 V and +5 V from backplane and generates the operating voltages required by the SCM circuitry

LED Board (CLN7098A)

- **Front Panel LEDs and Switches** — general purpose input/output ports control eight status LEDs and accept inputs from four momentary switches, all located on the SCM front panel
- **Front Panel Connectors** — four connectors (RSS Port DB-9, External Speaker RJ-11, Handset/Microphone RJ-11, and 5/10 MHz External Input BNC) are mounted on the front panel for interface with external equipment

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2 CONTROLS, INDICATORS, AND INPUTS/OUTPUTS

Figure 1 and Figure 2 show the SCM controls, indicators, and all input and output external connections.

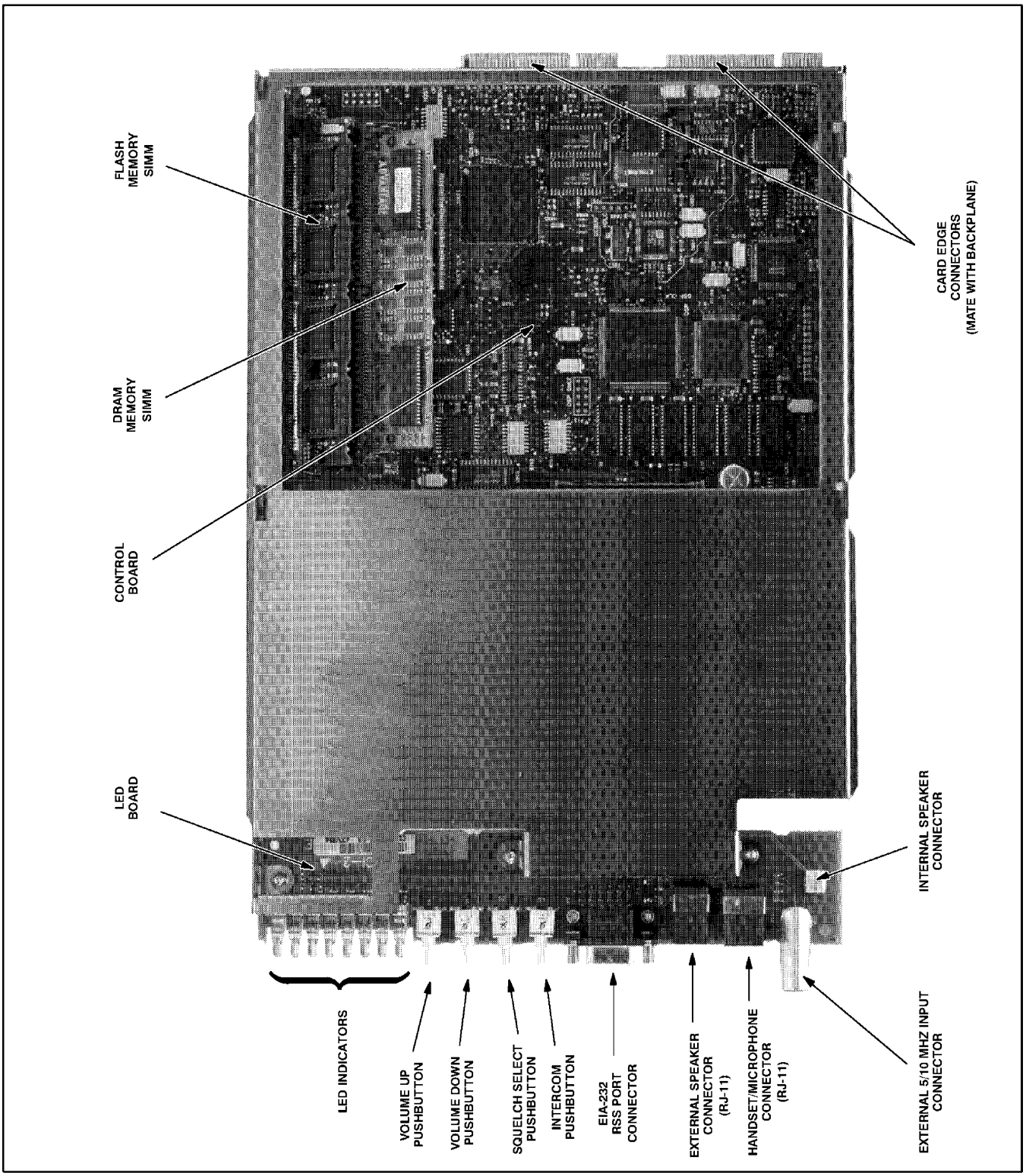

Figure 1. Station Control Module Controls, Indicators, and Inputs/Outputs (Front View)

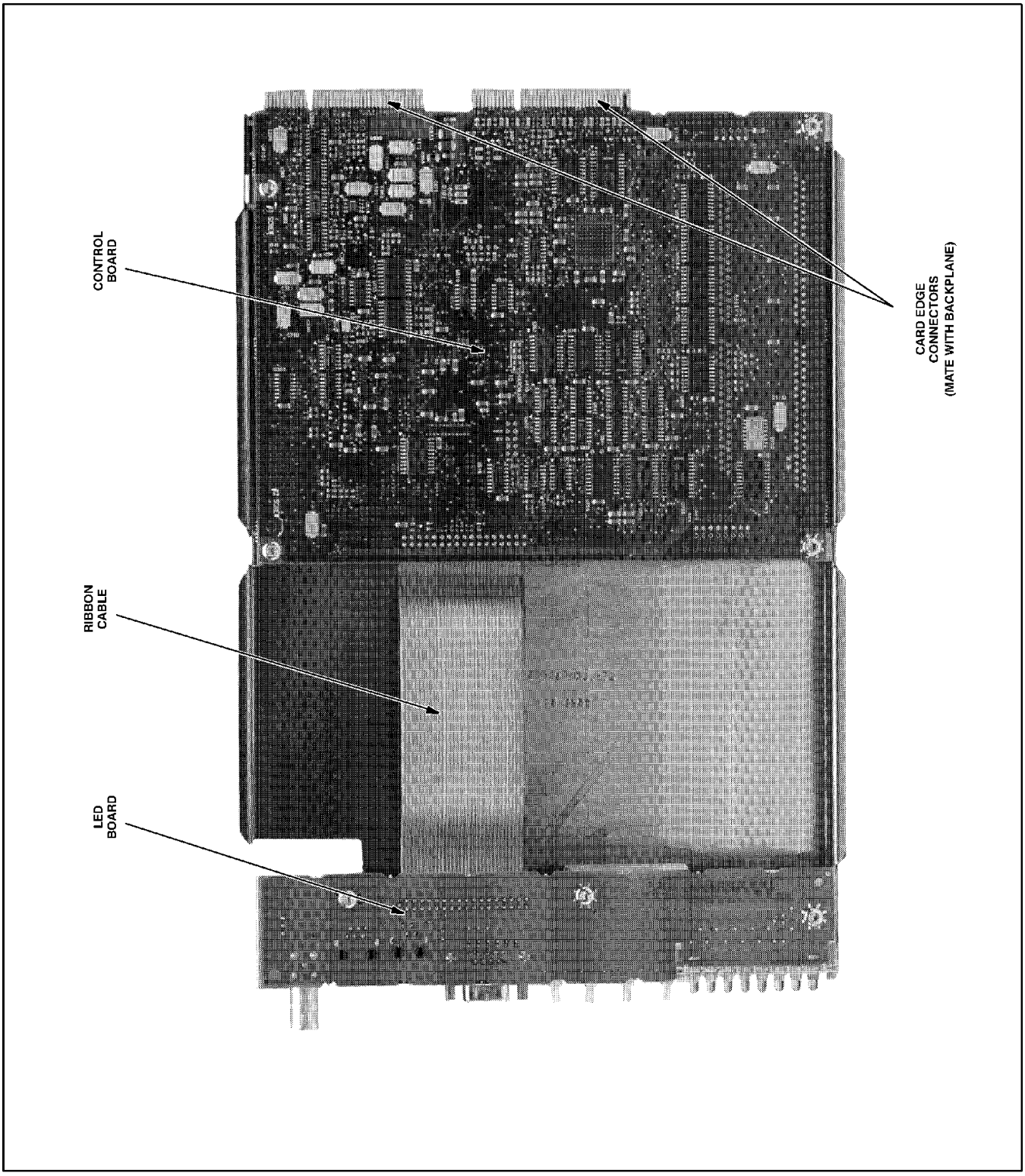

Figure 2. Station Control Module Controls, Indicators, and Inputs/Outputs (Rear View)

3 FUNCTIONAL THEORY OF OPERATION (CLN7060A Control Board; Tantalum Capacitors) (CLN7558A Control Board; Ceramic Capacitors)

The following theory of operation describes the operation of the CLN7060A/CLN7558A Control Board circuitry at a functional level. The information is presented to give the service technician a basic understanding of the functions performed by the module in order to facilitate maintenance and troubleshooting to the module level. Refer to Figure 3 for a block diagram of the CLN7060A/CLN7558A Control Board.

Host Microprocessor

Overview

The Host Microprocessor (μP) serves as the main controller for the SCM (and station). The μP, an MC68EN360 running at a clock speed of 25 MHz, controls the operation of the station as determined by the station software (contained in a FLASH SIMM module) and the station codeplug (EEPROM).

Communications Buses

The Host μP provides five general−purpose serial communications buses, as follows:

- **SCC1** — Used as Ethernet port for high-speed communications, either to allow station software to be downloaded from a local PC into the FLASH memory
- **SCC3** — Used as the Interprocessor Communications Bus (HDLC protocol) to allow the Host μP to communicate with the Wireline Interface Board and other optional modules
- **SCC4** — Used as RS−232 port for connections to external equipment, such as a modem
- **SMC1** — Used as RS−232 port for RSS communications (9-pin D-type connector #20 on backplane)
- **SMC2** — Used as RS−232 port for RSS communications (9-pin D-type connector located on SCM front panel)

Address and Data Buses

The μP is equipped with a 28−line address bus used to access the non−volatile memory, DRAM memory, and provide control (via memory mapping) for other circuitry in the SCM. A 32−line data bus (buffered for the non−volatile memory) is used to transfer data to/from the SCM memory, as well as other SCM circuitry.

SPI Bus

The Host μP also controls the SPI bus, a general−purpose communications bus that allows the Host μP to communicate with other modules in the station.

(continued)

Host Microprocessor (Continued)

DRAM Controller

The Host μP provides signals necessary to access and refresh the DRAM memory.

25 MHz Clock Circuitry

A crystal–controlled 25 MHz clock circuit and buffer provide the 25 MHz clock signal to the Host μP.

Non–Volatile Memory

Station Software FLASH Memory

The station software resides in a 512k x 32 FLASH SIMM module. The FLASH SIMM is accessed by the Host μP via the 28–line Host Buffered Address Bus and the 32–line Host Buffered Data Bus.

Codeplug EEPROM

The data which determines the station personality resides in an 8K x 8 codeplug EEPROM. Stations are shipped from the factory with generic default data programmed into the codeplug EEPROM. Field programming is performed during installation using the Radio Service Software (RSS) program to enter additional customer–specific data, such as site output power, time–out timer settings, etc.

DRAM Memory

Each SCM contains a 2M x 32 DRAM SIMM into which the station software code is downloaded and run. The DRAM also provides short–term storage for data generated/required during normal operation. Read and write operations are performed using the Host Buffered Address and Host Buffered Data buses.

The DRAM memory locations are sequentially refreshed by the column and row signals from the Host μP.

External Line Interface Circuitry

Ethernet Port

An Ethernet port is provided via a BNC connector on the station backplane which allows the station to connect into the Ethernet local network of an *IntelliRepeater* trunking site. The Ethernet port may also be used to allow station software to be downloaded from a local PC into the FLASH SIMM module. This Ethernet port is provided by Host μP serial communication bus SCC1 (which supports 10Base-2 architecture).

General Purpose RS232 Serial Port

A general purpose RS−232 communications port is provided by Host μP serial communication bus SCC4. This port is available at a DB-25 connector (#15) located on the station backplane, and may be used to connect external equipment (e.g., an external modem).

RSS Port (Backplane)

A 9−pin D−type connector (#20) is provided on the station backplane to allow service personnel to connect a PC loaded with the Radio Service Software (RSS) and perform programming and maintenance tasks. The RSS port may also be used to allow station software to be downloaded from a local PC into the FLASH SIMM module. This RSS port is provided by Host μP serial communication bus SMC1 which communicates with the RSS terminal via EIA−232 Bus Receivers/Drivers.

RSS Port (Front Panel)

A 9−pin D−type connector is provided on the SCM front panel to allow service personnel to connect a PC loaded with the Radio Service Software (RSS) and perform programming and maintenance tasks. The RSS port may also be used to allow station software to be downloaded from a local PC into the FLASH SIMM module. This RSS port is provided by Host μP serial communication bus SMC2 which communicates with the RSS terminal via EIA−232 Bus Receivers/Drivers.

Digital Signal Processor (DSP) and DSP ASIC Circuitry

General

All station transmit and receive audio/data is processed by the DSP and related circuitry. This circuitry includes the DSP IC, the DSP ASIC, and the DSP ASIC Interface Circuitry. All audio signals input to or output from the DSP are in digitized format.

Inputs to the DSP circuitry are:

- Digitized receive signals from the Receiver Module
- Audio from handset or microphone connected to appropriate SCM front panel connector; signal is digitized by CODEC (p/o Audio Interface Circuitry) before being sent to DSP via Audio Interface Bus
- Digitized voice audio/data from Wireline Interface Board and other optional modules via TDM bus
- ASTRO modem data from Wireline Interface Board via HDLC bus
- *SECURENET* modem data from Wireline Interface Board via HDLC bus
- 6809/MRTI transmit audio

Outputs from the DSP circuitry are:

- Digitized voice audio/data from DSP to Wireline Interface Board and other optional modules via TDM bus
- Digitized voice audio from DSP to external speaker, built–in speaker, or handset earpiece via Audio Interface Bus and Audio Interface Circuitry
- Digitized voice audio/data from DSP to Exciter Module (modulation signals) via Audio Interface Bus and Audio Interface Circuitry
- 6809/MRTI transmit audio

Digital Signal Processor (DSP)

The DSP, a 56002 operating at an internal clock speed of 60 MHz, accepts and transmits digitized audio to/from the various modules in the station. The DSP provides address and data buses to receive/transmit digitized audio (via the DSP ASIC) and to access the DSP program and signal processing algorithms contained in three 32K x 8 SRAM ICs. Three additional 32K x 8 SRAM ICs are provided for data storage.

DSP ASIC

The DSP ASIC operates under control of the DSP to provide a number of functions, as follows:

- Interfaces with the DSP via the DSP address and data buses
- Accepts 16.8 MHz signal from Station Reference Circuitry and outputs a 2.1 MHz reference signal used throughout the station
- Provides interfaces for the HDLC bus, TDM bus, and serial bus used to communicate with the Receiver Module,
- Accepts digitized data from Receiver Module via DSP ASIC Interface Circuitry
- Provides interfaces for several A/D and D/A converters

Station Reference Circuitry

The Station Reference Circuitry consists of a phase-locked loop comprised of a high-stability VCO and a PLL IC. The output of the VCO is a 16.8 MHz signal which is fed to the DSP ASIC. The ASIC divides the signal by 8 and outputs a 2.1 MHz signal which is separated and buffered by a splitter and output to the Exciter Module and Receiver Module as 2.1 MHz REF.

The Station Reference Circuitry may operate in one of three modes:

- **Normal Mode** — In this mode, the control voltage is turned off (via control voltage enable switch) and the high−stability VCO operates in an open loop mode; stability of the VCO in this mode is 1 PPM per year.
- **Manual Netting Mode** — Periodically, an external 5/10 MHz source is required to fine tune, or "net", the 16.8 MHz reference signal. In this mode, the PLL compares the 5/10 MHz reference and a sample of the 16.8 MHz VCO output and generates up/down pulses. The Host μP reads the pulses (via SPI bus) and sends correction signals (via SPI bus) to the VCO to adjust the output frequency to 16.8 Mhz ±0.3 ppm.
- **High-Stability Mode** — For some systems (e.g., Simulcast systems), the free−running stability of the VCO is unacceptable for optimum system performance. Therefore, an external 5/10 MHz source is connected permanently to one of the BNC connectors. In this mode, the PLL compares the 5/10 MHz reference and a sample of the 16.8 MHz VCO output and generates a dc correction voltage. The control voltage enable switch is closed, allowing the control voltage from the PLL to adjust the high-stability VCO frequency to 16.8 Mhz ±0.3 ppm. The VCO operates in this closed loop mode and is continually being frequency controlled by the control voltage from the PLL.

Note:
Two BNC connectors (one 50 Ω input located on SCM front panel, one high impedance input located on the station backplane) are provided to allow an external 5/10 MHz source to be input to the OSC_{in} input to the PLL to perform frequency netting. Refer to the Maintenance section in this manual for recommended intervals and procedures for netting the station reference.

HDLC Bus Control Circuitry

The HDLC Bus Control Circuitry provides high-impedance buffering and data routing for the Interprocessor Communications Bus (a serial data bus implementing HDLC protocol). This bus allows the Host μP to communicate with the microprocessor located on the Wireline Interface Board and other optional modules via an interprocessor communications bus.

Audio Interface Circuitry

General

The Audio Interface Circuitry interfaces external analog audio inputs and outputs with the DSP circuitry. Most of the local audio processing is performed by a custom Local Audio ASIC.

External Audio Sources

A multiplexer, under control of the Host µP, is used to select one of six possible external audio input sources (four for diagnostic loopback signals, one for 6809/MRTI transmit audio, and one for handset or microphone audio). The selected audio source signal is converted to a digital signal by the A/D portion of the CODEC circuit and sent to the DSP ASIC via the Audio Interface Bus. The DSP circuitry processes the signal and routes it to the desired destination.

External Audio Destinations

Digitized audio from the DSP circuitry is input to the D/A portion of the CODEC IC and is output to one of four external devices:

- External Speaker — connects to RJ−11 jack () located on SCM front panel
- Handset Earpiece/Microphone — connects to RJ−11 jack () located on SCM front panel
- Local Built−In Speaker — internal speaker and ½ W audio amplifier; may be switched on/off and volume controlled by using volume up ( ) and down ( ) buttons on SCM front panel
- J14 on Station Backplane — 6809/MRTI receive audio output to external MRTI Module

Exciter Modulation Signals

Digitized audio/data intended to be transmitted from the station is output from the DSP circuitry to a D/A converter (internal to the Local Audio ASIC) via the TX/Voice Audio signal (p/o the Serial Synchronous Interface bus, connected between the DSP and the DSP ASIC). The digitized signal is converted to analog, level shifted and amplified, and fed to a 0−6 kHz filter. The output of the filter is then fed to one of the inputs of a multiplexer. The output of the multiplexer is fed to two individual digitally controlled potentiometers (each of which is adjusted by the Host µP via the SPI Bus) and output to the Exciter Module as modulation signals VCO MOD AUDIO and REF MOD AUDIO.

Input/Output Ports

Input Ports

Two general–purpose multi–line input ports are provided to allow various input signals from the SCM and station circuitry to be accepted and sent to the Host μP. The two ports (I/O Port P0 In and I/O Port P1 In) are comprised of 32 and 24 lines, respectively, which come from circuitry in the SCM as well as other modules in the station via the backplane. The buses are input to buffers which make the data available to the Host μP via the Host Buffered Data Bus. Typical inputs include the pushbutton switches located on the SCM front panel and the MIC PTT signal from the handset/microphone.

Output Ports

Two general–purpose multi–line output ports are provided to allow various control signals from the Host μP to be output to the SCM and station circuitry via the backplane. The two ports (I/O Port P0 Out and I/O Port P1 Out) are comprised of 32 and 8 lines, respectively, which come from the Host Buffered Data Bus via latches. Typical output control signals include the control lines for the eight LEDs located on the SCM front panel and the local speaker enable signal.

6809/MRTI Interface Circuitry

6809 Trunking Interface

TX DATA from the 6809 Trunking Controller is input to the station via J14 on the station backplane. The signal is routed thru nominal filtering on the 6809/MRTI Interface Circuitry and fed to the Audio Interface Circuitry. The T DATA signal is then waveshaped/filtered and fed to an A/D converter (internal to the Local Audio ASIC), which outputs a digital signal to the DSP via the Audio Interface Bus.

6809 RX AUDIO is output from the DSP to the Local Audio Circuitry via the Audio Interface Bus. The signal is amplified, filtered, buffered, and output thru nominal filtering on the 6809/MRTI Interface Circuitry to the 6809 Trunking Controller via J14 on the station backplane.

MRTI Interface

MRTI TX AUDIO from an external MRTI module is input to the station via J14 on the station backplane. The signal is routed thru the 6809/MRTI Interface Circuitry and fed to one input of an 6–to–1 multiplexer. If selected, the MRTI TX AUDIO signal is converted to a digital signal by a CODEC (internal to the Local Audio ASIC) and sent to the DSP ASIC via the Audio Interface Bus.

MRTI RX AUDIO is output from the DSP to the Local Audio ASIC via the Audio Interface Bus. The signal is amplified, filtered, buffered, and output thru the 6809/MRTI Interface Circuitry to the external MRTI Module via J14 on the station backplane.

Supply Voltages Circuitry

The SCM contains on−board regulator and filtering circuitry to generate the various operating voltages required by the SCM circuitry. +14.2 V and +5V from the backplane are used as sources for the following supply voltage circuits:

- **VCCA Supply Circuitry** — provides VCCA (+5V) for the Audio Interface Circuitry in the SCM.
- **Filtering Circuitry** — filters the +14.2 V and +5V from the backplane to provide A+ and VCC, respectively, for the SCM digital circuitry.

4 FUNCTIONAL THEORY OF OPERATION (CLN7098A LED Board)

The following theory of operation describes the operation of the CLN7098A LED Board circuitry at a functional level. The information is presented to give the service technician a basic understanding of the functions performed by the module in order to facilitate maintenance and troubleshooting to the module level. Refer to Figure 4 for a block diagram of the CLN7098A LED Board.

Front Panel LEDs and Switches

Note:
Refer to the Troubleshooting section of this manual for complete details on the interpretation of the LEDs.

Note:
Refer to the Operation section of this manual for complete details on the use of the pushbutton switches.

LEDs

Eight status LEDs are provided on the SCM front panel to provide visual indications of various station operating conditions.The LEDs are controlled by eight lines from I/O Port P0 Out.

Switches

Four momentary contact pushbutton switches are provided on the SCM front panel to allow various station functions to be selected. Depressing a pushbutton causes a high to be sent to the Host µP via I/O Port P0 In.

Front Panel Connectors

Four connectors are provided on the SCM front panel to interface with external equipment:

- **RSS Port** — DB-9 connector used for connection to a PC loaded with Radio Service Software (RSS) for configuring/servicing the station
- **External Speaker Connector** — RJ-11 connector used for connection to an external speaker (Model HSN1000)
- **External Handset/Microphone** — RJ-11 connector used for connection to an external handset (Model TMN6164) or microphone (Model HMN1001)
- **5/10 MHz Input** — BNC connector used for connection to an external source of 5 or 10 MHz to be used as a station reference

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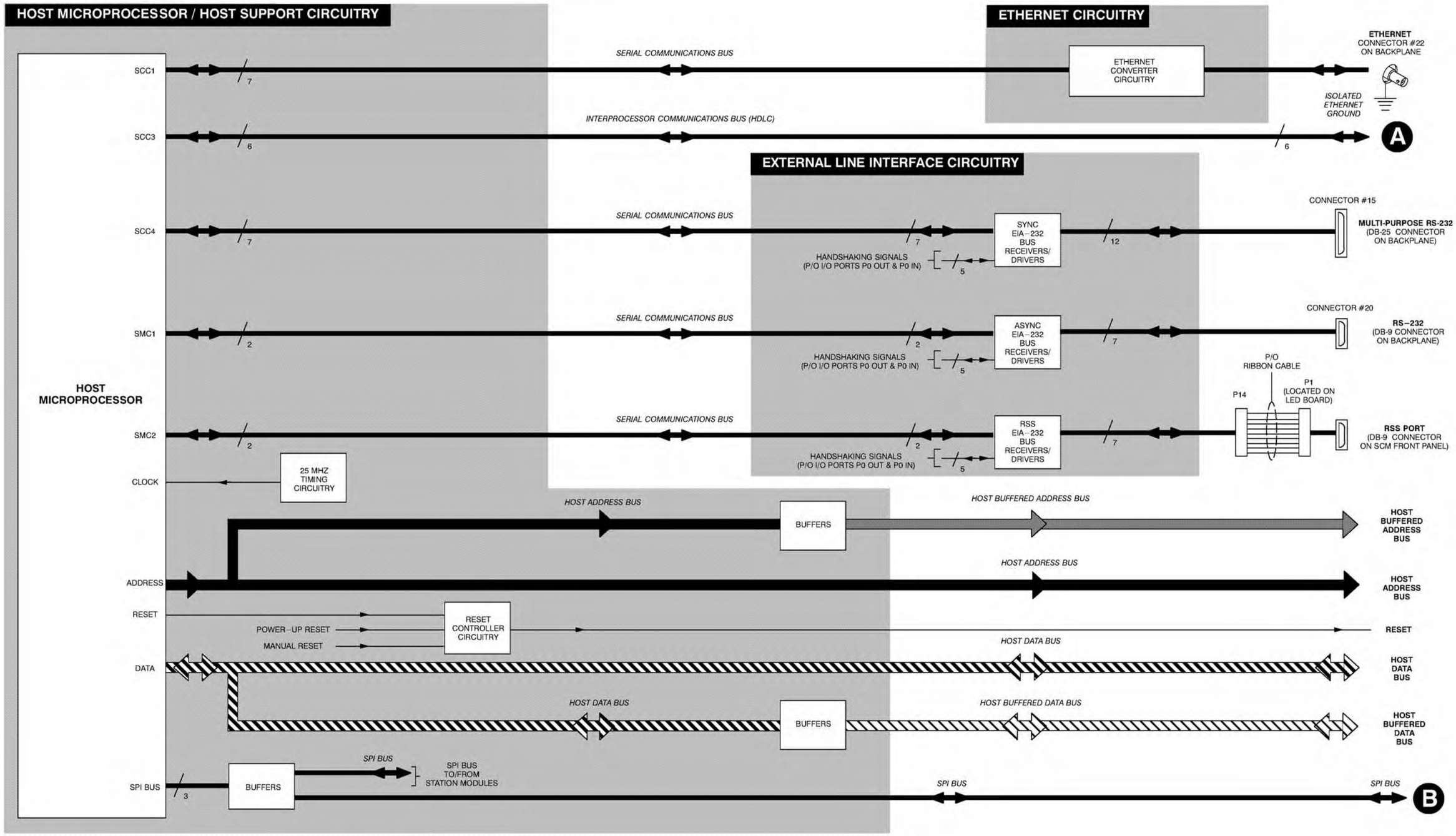


Figure 3. CLN7060A/CLN7558AStation Control Board Functional Block Diagram (1 of 5)

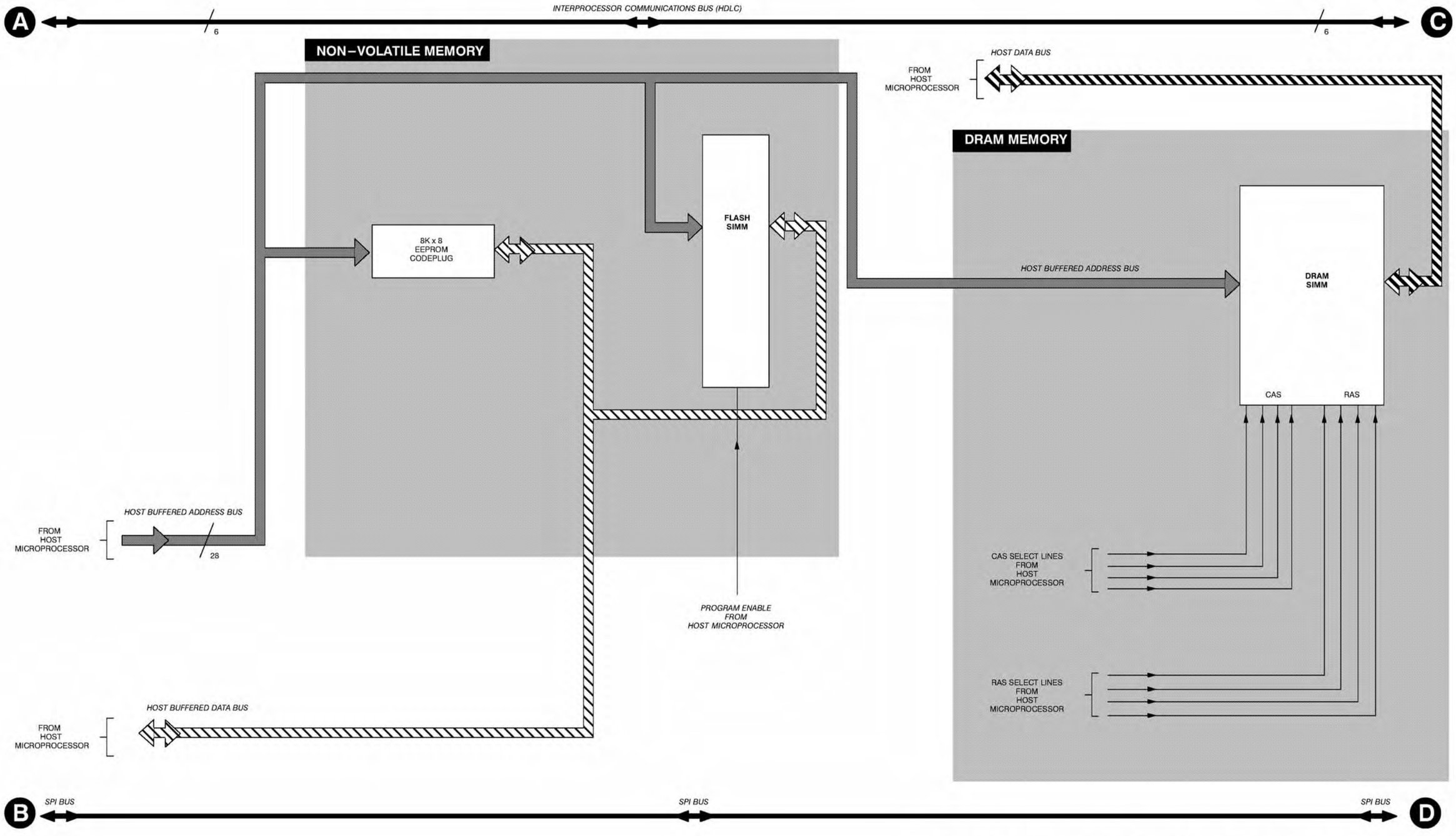


Figure 3. CLN7060A/CLN7558A Station Control Board Functional Block Diagram (2 of 5)

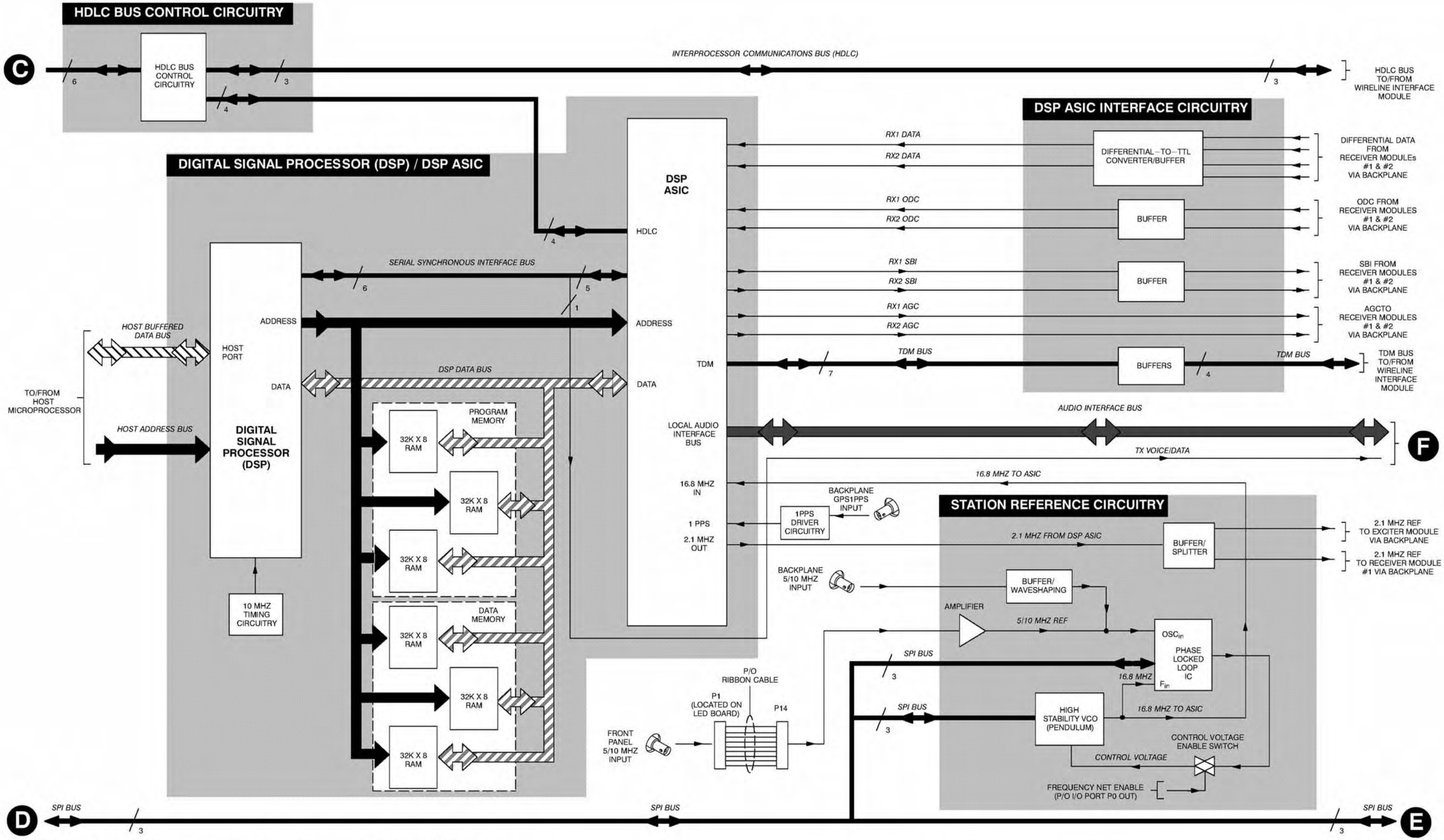


Figure 3. CLN7060A/CLN7558A Station Control Board Functional Block Diagram (3 of 5)

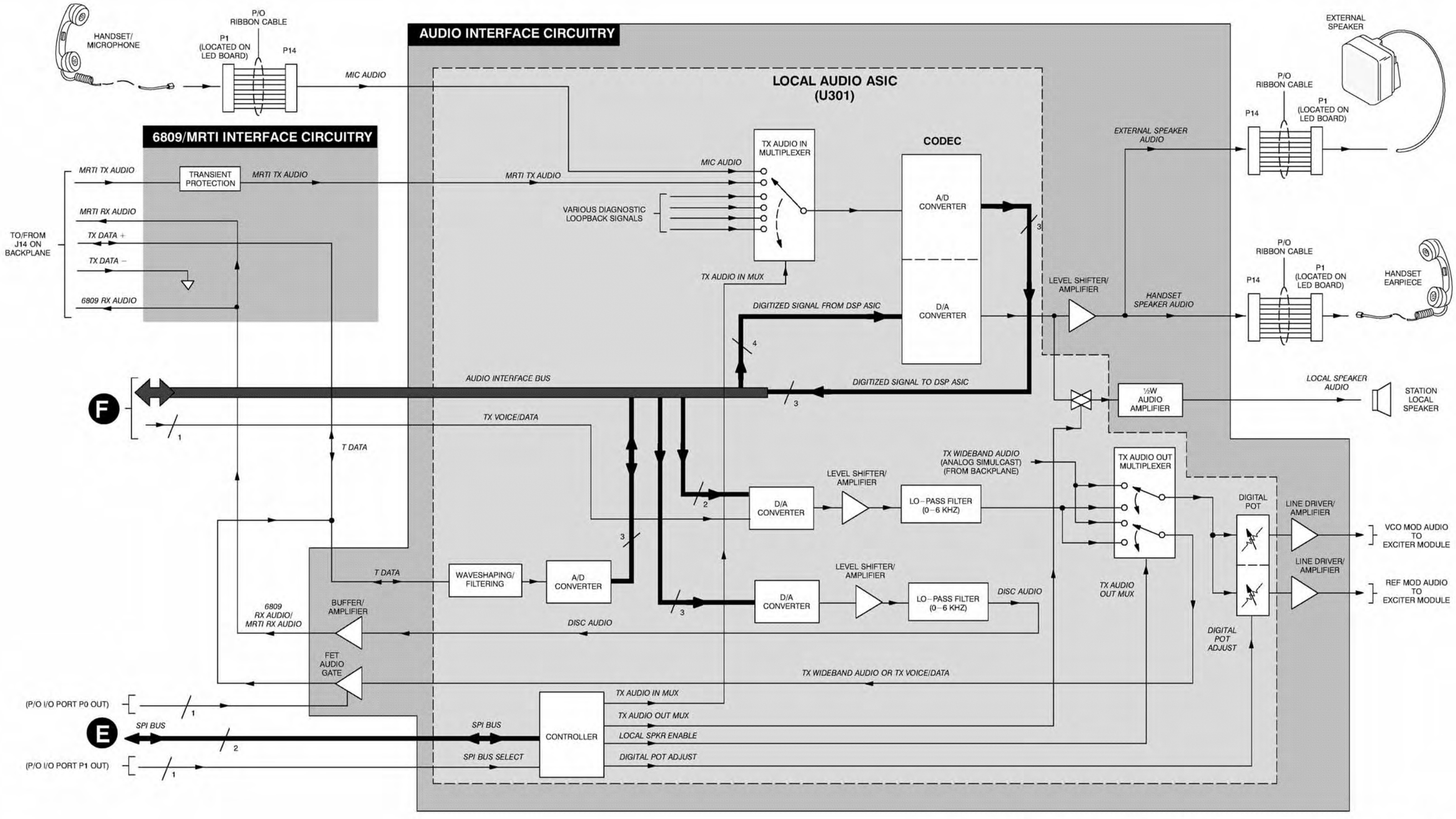
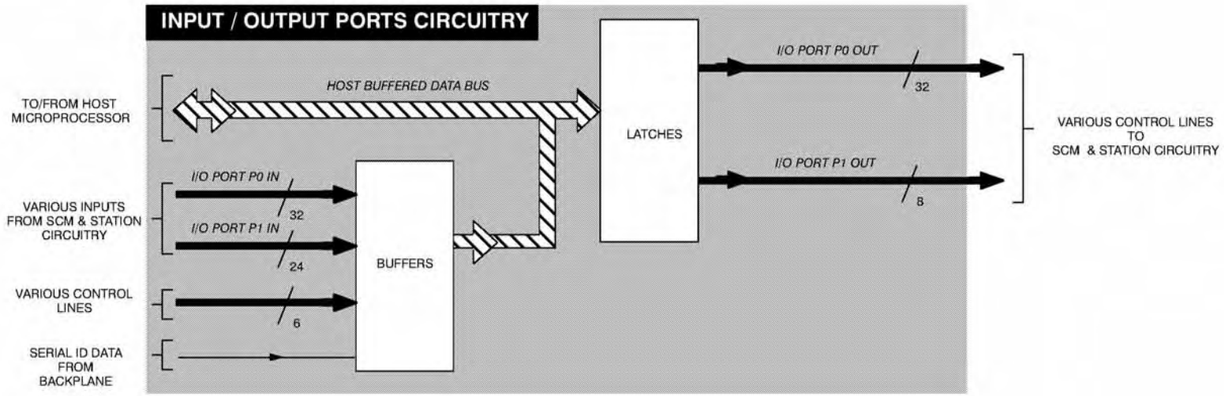


Figure 3. CLN7060A/CLN7558A Station Control Board Functional Block Diagram (4 of 5)



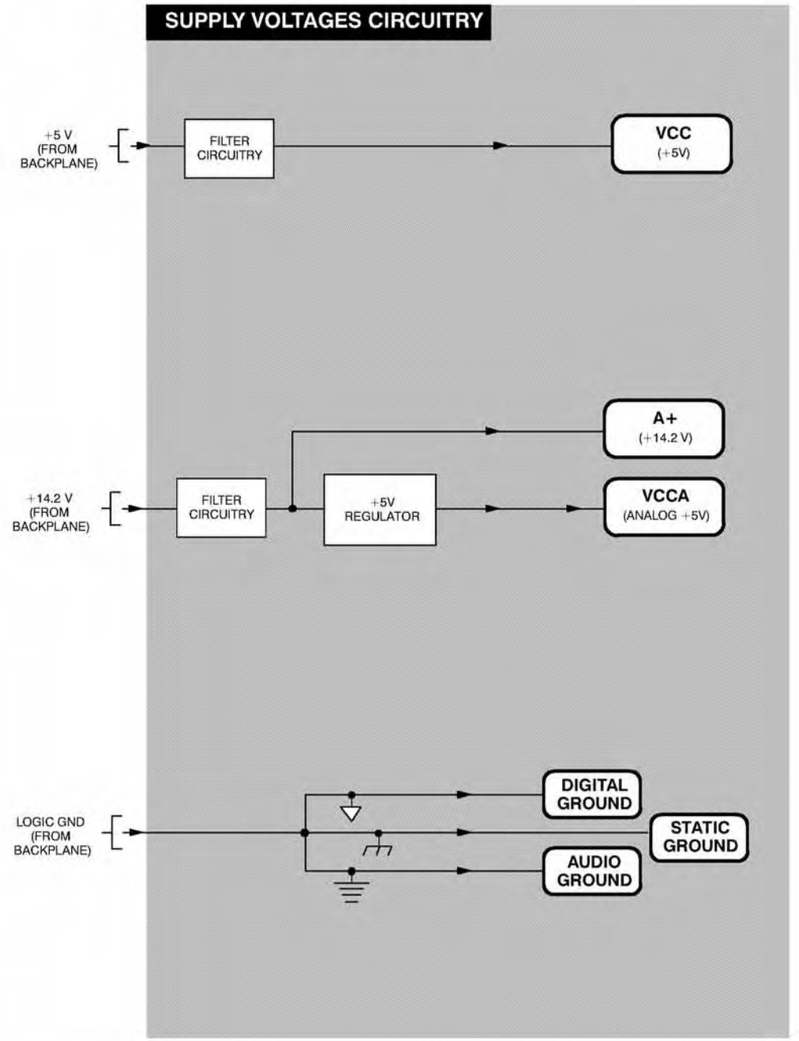


Figure 3. CLN7060A/CLN7558A Station Control Board Functional Block Diagram (5 of 5)

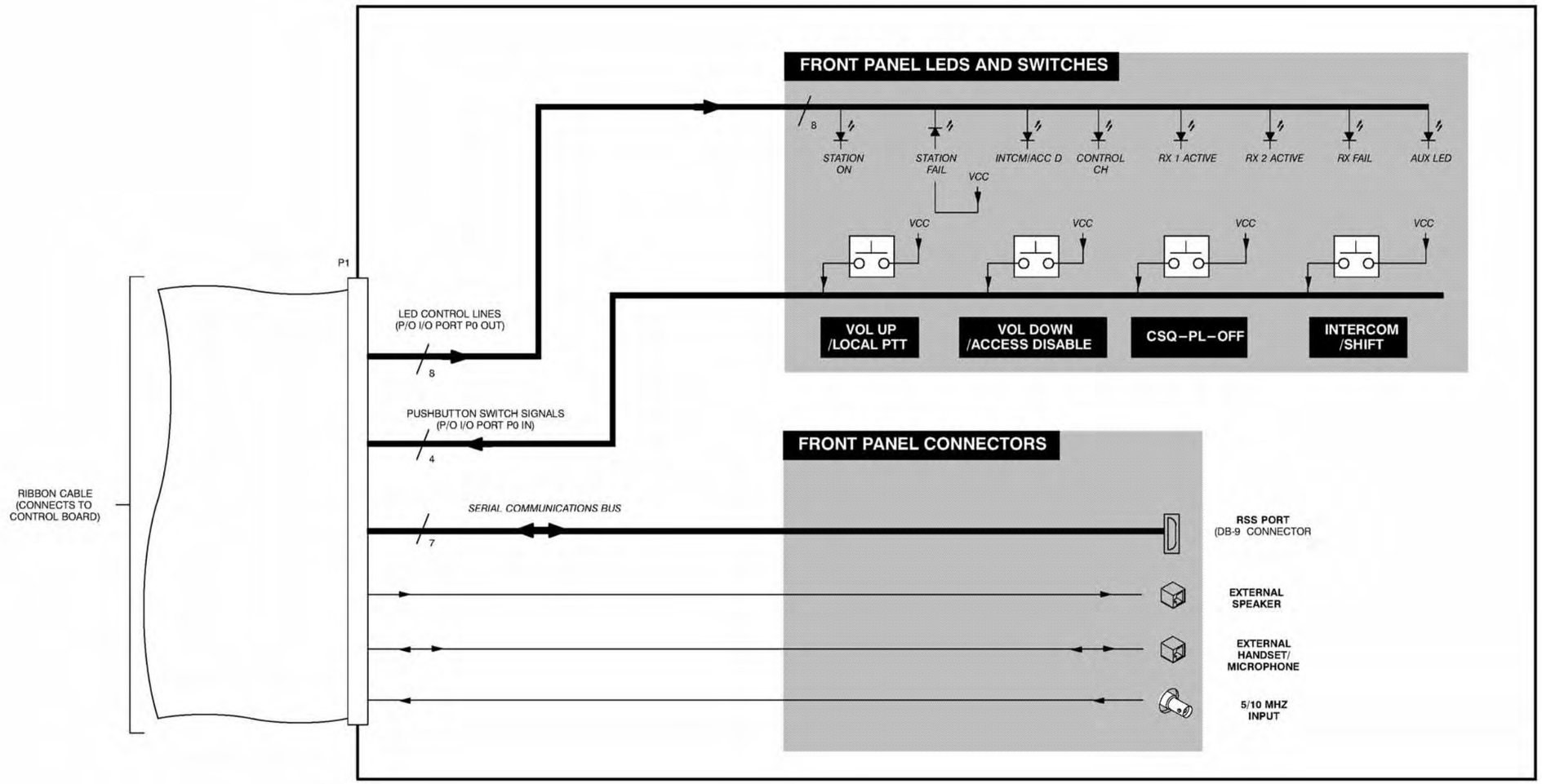


Figure 4. CLN7098A LED Board Functional Block Diagram

1 DESCRIPTION

The model CLN7692 station control module (SCM) is described in this section. A general description, identification of controls, indicators, and inputs/outputs, a functional block diagram, and functional theory of operation are provided. The information provided is sufficient to give service personnel a functional understanding of the module, allowing maintenance and troubleshooting to the module level. (Refer also to the *Maintenance and Troubleshooting* section of this manual for detailed troubleshooting procedures for all modules in the station.)

General Description

The SCM serves as the main controller for the station. The SCM board contains a MPC860EN host microprocessor (host μP), a DSP56311 digital signal processor (DSP), and support circuitry, which combine to provide signal processing and operational control over the other station modules. The SCM also contains the station operating software and parameters that define the personality of the station, including system capabilities and operating variables such as output power and operating frequency.

The CLN7692 SCM consists of the Enhanced Performance Integrated Control (EPIC) IV module which supports general station control, communications, and signal processing functions, as well as certain system specific functions. Several versions of the module are available to support various applications including conventional, 6809 trunking, IntelliRepeater, data base stations and wireless data.

Overview of Circuitry

The SCM contains the following circuitry:

- **Host Microprocessor** — MPC860EN 50MHz PowerPC based central processor of the SCM with 32-bit wide data bus, 4 GB address space and background debug mode
- **SDRAM Memory** — consists of SDRAM into which station software is loaded and executed with a bus width of 32 bits, and a bus speed of 50MHz.
- **Non-Volatile Memory** — consists of FLASH with a bus width of 32 bits that contains the station operating software and data. There is

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an additional FLASH with a bus width of 16 bits that contains boot and test code, and station codeplug data.

- **HDLC Bus Control Circuitry** — provides bus control to allow the host µP communications port SCC3 to communicate with the Wireline Interface Board and other optional modules via the HDLC interprocessor communications bus
- **Serial Peripheral Interface (SPI)** — Bus supports EPIC IV and other SCMs
- **External Line Interface Circuitry** — consists of two RS-232 asynchronous serial ports (one on front panel and one on back panel), one RS-232 synchronous serial port (back panel), and one external 10BaseT Ethernet port (connectors on backplane).
- **Digital Signal Processor (DSP) and DSP ASIC Circuitry** — DSP56311 processor operating at a core frequency of 100MHz performs high-speed processing of audio and signaling data signals.
- **Station Reference Circuitry** — 16.8MHz temperature compensated crystal oscillator capable of 1ppm performance and software enhanced fault tolerant control used to generate the reference signals throughout the station.
- **Audio Interface Circuitry** — consists of the DSP, DSP ASIC, local audio ASIC that process and route the various audio input signals (such as microphone, MRTI, receiver, or the wireline audio) to output devices (such as the local speaker, MRTI, exciter modulation, or the wireline audio inputs, when enabled).
- **Input / Output Ports Circuitry** — consists of general inputs and outputs on the CPLD, DSP ASIC and the host µP. The input and output signals are used to control and monitor station functions.
- **Front Panel LEDs and Switches** — general purpose input/output ports control eight status LEDs and accept inputs from four pushbutton switches, all located on the front panel.
- **Supply Voltage Circuitry** — contains filtering and regulator circuitry that accepts +14.2 V and +5 V from the backplane and generates the operating voltages required by the SCM circuitry.

2 CONTROLS, INDICATORS AND INPUTS/OUTPUTS

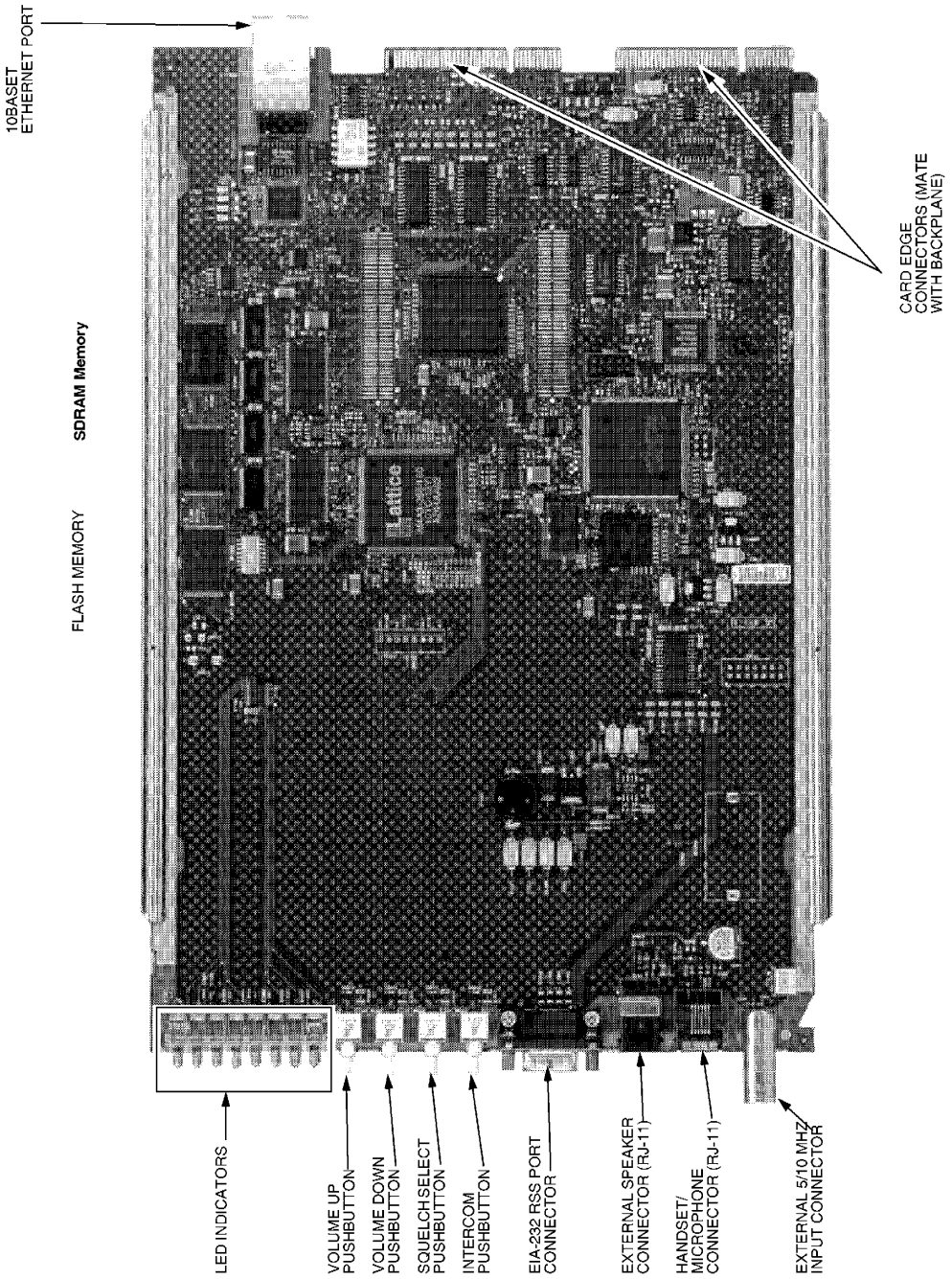


Figure 1 EPIC IV

3 FUNCTIONAL THEORY OF OPERATION

The following theory of operation describes the operation of the SCM circuitry at a functional level. The information is presented to give the service technician a basic understanding of the functions performed by the module in order to facilitate maintenance and troubleshooting to the module level.

Host Microprocessor (See Figure 2, Sheet 1 of 5)

Overview

The host µP serves as the main controller for the SCM and therefore the station. The µP runs at a clock speed of 50 MHz and controls the operation of the station as determined by the station software contained in the FLASH.

Communications Buses

The Host µP provides six general-purpose serial communications buses, as follows:

- **SCC1** — Used as Ethernet port for high speed communications, either to connect to the Ethernet local network of an IntelliRepeater trunking site or to allow station software to be downloaded from a local PC into the FLASH memory.
- **SCC2** — Used as communications port to allow the station to connect to the local network of an IntelliRepeater trunking site; a 9-pin D-type connector located on the backplane provides external connections.
- **SCC3** — Used as the interprocessor communications bus (HDLC protocol) to allow the Host µP to communicate with other optional modules.
- **SCC4** — Used as miscellaneous general purpose I/O.
- **SMC1** — Used as RS-232 port for RSS communications (9-pin D-type connector on the backplane.)
- **SMC2** — Used as RS-232 port for RSS communications (9-pin D-type connector located on SCM front panel.)

Address and Data Buses

The µP has a 32-line address bus used to access the non-volatile memory, SDRAM memory, and provide control (via memory mapping) for other circuitry in the SCM. A 32-line data bus (buffered for the non-volatile memory) is used to transfer data to/from the SCM memory, as well as other SCM circuitry.

SPI Bus

The host µP also controls the SPI bus, a general-purpose communications bus that allows the host µP to communicate with other modules in the station.

SDRAM Controller

The host µP provides signals necessary to access and refresh the SDRAM memory.

25 MHz Clock Circuitry

A crystal-controlled 25 MHz clock circuit and buffer provide the 25 MHz clock signal to the host µP. This clock is internally multiplied in the µP, allowing an operational frequency of 50MHz.

Non-Volatile Memory (See Figure 3, Sheet 2 of 5)

Station Software FLASH Memory

The station software resides in 16 MB of FLASH memory with a 32 bit bus. The host processor accesses the FLASH via the 32-line host buffered address bus and the 32-line host buffered data bus.

Station Boot and Configuration FLASH Memory

The station boot and configuration software resides in 4 MB of FLASH memory utilizing 16 bits of a 32 bit bus. The FLASH memory is accessed by the host µP via the 32-line host buffered address bus and the 32-line host buffered data bus.

SDRAM Memory

Each SCM contains a minimum of 32 MB of SDRAM memory with a 32 bit bus into which the station software code is downloaded and executed. This SDRAM memory is comprised of two banks. The SDRAM also provides short-term storage for data generated or required during normal operation. Read and write operations are performed using the host address and data buses.

The SDRAM memory locations are sequentially refreshed by the column and row signals from the host µP.

External Line Interface Circuitry

CSS Port (Front Panel)

This asynchronous serial port is provided by SMC2 of the host µP, configured as a universal asynchronous receiver-transmitter (UART). Only the TX and RX signals are supported by the SMC. Optional handshake signals may be provided, under software control, via the host input/output ports. A 9-pin, female D-type connector (P1) is provided at the front panel edge of the LED board.

General Purpose Backplane Asynchronous RS-232 Port

This serial port is provided by SMC1 of the host µP, configured as a UART. Only the TX and RX signals are supported by the SMC. Optional

handshake signals may be provided, under software control, via the host input/output ports. The signals for this port are routed (via RS232 drivers/receivers) to a 9-pin, female D-type connector located on the backplane (Connector 20).

General Purpose Backplane Synchronous RS-232 Port

This serial port provides for future enhancement. This port interfaces to SCC2 of the host μP and supports both asynchronous and synchronous UART protocols. In addition to TX and RX, the clock signals and standard handshake signals are handled directly by the host μP. Optional handshake signals may be provided, under software control, via the host input/output ports. The signals for this port are routed (via RS232 drivers/receivers) to a 25-pin, female D-type connector located on the backplane (connector 15).

Ethernet

Ethernet (10baseT) is a standard feature of the EPIC IV module. External Ethernet signaling is controlled by SCC1 of the host μP SCC1 interfaces to the SIA, which performs the Manchester encoder/decoder function via the host μP signals. The isolation transformers and the SIA provide signal conditioning and translation. The physical Ethernet 10baseT port is located on the station backplane.

Digital Signal Processor (DSP) and DSP ASIC and Local Audio ASIC (See Figure 4, Sheet 3 of 5)

General

All station transmit and receive audio/data is processed by the DSP, DSP ASIC, local audio ASIC, and related circuitry. All audio signals handled by the DSP are in digitized format.

Inputs to the DSP circuitry are:

- Digitized receive signals from the receiver module
- When enabled, audio from handset or microphone connected to appropriate SCM front panel connector; signal is digitized by the audio interface circuitry, local audio ASIC and DSP ASIC before being sent to the DSP.
- When enabled, digitized voice audio/data from wireline interface board and other optional modules via time division multiplexing (TDM) bus to the, local audio ASIC and DSP ASIC before being sent to the DSP.
- When enabled, ASTRO modem data from wireline interface board via HDLC bus to the local audio ASIC and DSP ASIC before being sent to the DSP
- 6809/MRTI transmit audio to the local audio ASIC and DSP ASIC before being sent to the DSP

Outputs from the DSP circuitry are:

- When enabled, digitized voice audio/data from DSP to DSP ASIC and via the local audio ASIC to the wireline interface board and other optional modules via TDM bus
- When enabled, digitized voice audio from DSP to DSP ASIC and via the local audio ASIC to the external speaker, built-in speaker, or handset earpiece via audio interface circuitry
- Digitized voice audio/data from DSP to DSP ASIC and via the local audio ASIC to the exciter module (modulation signals) via the audio interface circuitry
- Digitized voice audio/data from DSP to DSP ASIC and via the local audio ASIC to the 6809/MRTI transmit audio

Digital Signal Processor (DSP) Circuitry

The DSP56311 provides performance enhancements over those used on other SCMs. Features include:

- Up to150MIPS with 150MHz clock, 100MIPs available with implementation of a 100MHz core clock.
- 100% object code compatible with the 56K Core
- Fully pipelined 24x24 parallel multiplier-accumulator
- 16 bit arithmetic support
- On-chip phase lock loop (PLL)
- On-chip emulator (OnCE)
- 128Kx24 bit on-chip SRAM
- Glueless interface to SRAMs and SSRAMs
- Enhanced filter co-processor (EFCOP)
- Two enhanced synchronous serial interfaces (ESSI)
- Up to 34 programmable general purpose I/O pins (GPIO) (depends on peripherals used)
- Very low power design
- 3.3VDC I/O, 1.8VDC core

The DSP is hardware configured to enter the bootstrap through HI08 bus mode on power up. This allows the DSP to receive its program information upon power up from the host µP's memory bus, through its host interface port. The program code is then loaded into internal program RAM that allows zero wait state execution.

DSP ASIC (DSP Glue ASIC)

The DSP ASIC, also known as the DSP glue ASIC for FDMA systems (DGA4F), was designed to replace the DGA3F. The DSP ASIC operates under the control of the DSP to provide the following functions:

- DGA4F is a field programmable gate array (FPGA) instead of a gate array.
- DGA4F utilizes 3.3V I/O with a 2.5V core.
- The DGA4F interfaces to the host µP through the memory bus and the receive SSI. For the memory bus interface, it utilizes the uppermost 16 data bits for data transfers.

- Provides a serial receive data input from the station receiver that is translated and output to the DSP (SSI)
- When enabled, provides a HDLC interface with the host μP that is translated to a TDM interface to other modules
- Provides a digital to analog interface to the local audio ASIC
- When enabled, provides a Wireline Board interface to the local audio ASIC
- Provides a CODEC interface to the local audio ASIC
- Provides site timing through a 1PPS input
- Accepts a 16.8MHz signal from the station reference circuitry and outputs a 2.1 MHz reference signal used throughout the station
- The FPGA is programmed in slave parallel mode by the DSP via the host μP. The FPGA data is stored in FLASH memory then transferred to the DSP which then programs the FPGA. After the FPGA has been programmed its reset signal is driven high by the DSP.

Host Interface

Interfacing the DSP to the host μP is done through the host interface port. The DSP code is downloaded from the host μP through this port as well as transfer of control information. The DSP is treated as a memory-mapped peripheral by the host μP.

Receiver Interface

The station receiver audio path originates from the receiver module. The receive audio is converted into digital I and Q samples by the ABACUS IC and then sent over the backplane to the SCM. The digital I and Q samples are received by DSP ASIC and then re-clocked to the DSP. The data samples can also be made available to the DSP via memory-mapped locations. If a second receiver is in use, its receive data is only available to the DSP as memory-mapped locations. The DSP then performs audio processing on the received data.

General Purpose I/O

The FPGA supports six bidirectional general purpose I/O lines. This port can be accessed by the DSP through the DSP ASIC.

Station Reference

The 16.8MHz station reference is generated by a temperature compensated crystal oscillator capable of 1ppm performance. When the 5MHz reference frequency is present the oscillator is steered by a PLL frequency synthesizer. When the PLL is locked the steering voltage is recorded by the host μP. When the host detects that the 5MHz is not present it switches the steering voltage path from the PLL to a digital to analog convertor (DAC) that generates the steering voltage that was previously recorded. The 5MHz reference signal has an input swing (sine or square-wave) at the SCM of at least 3.0Vp-p and a constant duty cycle of 25-75%.

HDLC Bus Control Circuitry

The HDLC bus control circuitry provides high-impedance buffering and data routing for the Inter-processor communications bus (a serial data bus implementing HDLC protocol). This bus allows the host µP to communicate with the host µP located on the wireline interface board and other optional modules via an interprocessor communications bus.

Audio Interface Circuitry (See Figure 5, Sheet 4 of 5)

General

The audio interface circuitry interfaces external analog audio inputs and outputs with the DSP circuitry.

External Audio Sources

A multiplexer, under control of the host µP, is used to select one of eight possible external audio input sources:

- Four for diagnostic loopback signals that include loopback MRTI audio, loopback VCO audio and loopback ref mod audio
- Two for future use
- One for 6809/MRTI transmit audio
- One for handset or microphone audio and for future use

The selected audio source signal is converted to a digital signal by the CODEC A/D portion of the local audio ASIC and sent to the DSP ASIC via the audio interface bus. The DSP circuitry processes the signal and routes it to the desired destination.

External Audio Destinations

Digitized audio from the DSP circuitry is input to the CODEC D/A portion of the local audio ASIC via the audio interface bus and is output to one of four external devices:

- External speaker connects to RJ-11 jack ( ) located on SCM front panel, when enabled.
- Handset earpiece/microphone connects to RJ-11 jack ( ) located on SCM front panel, when enabled.
- Local built-in speaker internal speaker and ½ W audio amplifier; may be switched on/off and volume controlled by using volume up ( ) and down ( ) buttons on SCM front panel, when enabled.
- J14 on station backplane - 6809/MRTI receive audio output to external MRTI Module

Exciter Modulation Signals

Outbound audio to be transmitted over the air is written to the FPGA memory-mapped locations from the DSP. The DSP ASIC clocks the audio samples out to a 12 bit linear D/A in the local audio ASIC. The audio is then digitally filtered by a low pass filter within the local audio

ASIC and is sent out the backplane, destined for the exciter module as VCO MOD and REF audio. Audio can also be sent out a second similar path via the wideband Rx D/A converter in Epsilon to the MRTI port. (What is Epsilon?)

Input/Output Ports and Reset Circuitry (See Figure 6, Sheet 5 of 5)

General

The input, output, 5MHz detect, and reset circuitry are implemented in a CPLD that provides most of the external glue logic functionality. Most of the CPLD functions are controlled and accessed by the host μP. The following list summarizes the supported host μP CPLD functions:

Input Ports

Two memory-mapped general-purpose input ports (40 bits total) are available to read various inputs from SCM and station circuitry. These input are in host addressable space for reading.

Output Ports

One memory-mapped general-purpose 32-bit registered output port is available to drive various control lines to the SCM and station circuitry. The output register is in Host addressable space for reading.

5MHz Detection

If the 5Mhz signal is lost the information is sent to the output port register and is accessable to the host μP via the host buffered data bus.

Reset

Various reset inputs from SCM and station circuitry that includes power-up reset from the power monitor, manual reset from the front panel (via the RESET switch on the front panel), software reset (via a set breakpoint) from the host μP, SRESET from the host μP, and the bidirectional HRESET. Reset states are in host μP addressable space for reading.

Host Interrupt

Interrupts the host via the IRQ TO HOST signal when P0_IN inputs 5MHz_Act, DAC_Voltage_Status, 16.8MHz_Act, Pend_Lock, Tx_Host_Reqx, 16.8MHz_Clk, Link_Integrity, or Exp_Host_Reqx are active. These interrupts are maskable and resetable. The DAC_Voltage_Status signal can also be programmed to be active on the rising or falling edge.

Serial Identification

The station serial identification number is read and stored in a register that is host μP addressable for read access.

Interrupts (IRQs)

An interrupt is generated to the host via the IRQ-TO-HOST signal when the various inputs from SCM and station circuitry inputs 5MHz_Act,

DAC_Voltage_Status, 16.8MHz_Act, Pend_Lock, Tx_Host_Reqx, 16.8MHz_Clk, Link_Integrity, or Exp_Host_Reqx are active. These interrupts are maskable and resetable. The DAC_Voltage_Status signal can also be programmed to be active on the rising or falling edge.

6809/MRTI Interface Circuitry (See Figure 5, Sheet 4 of 5)

6809 Trunking Interface

TX data from the 6809 trunking controller is input to the station via J14 on the station backplane. The signal is routed through nominal filtering on the 6809/MRTI interface circuitry and fed to the audio interface circuitry. The T DATA signal is then wave shaped/filtered and fed to an A/D converter, which outputs a digital signal to the DSP via the audio interface bus.

6809 RX audio is output from the DSP to the DSP ASIC and sent out the local audio interface bus via the audio interface bus to the audio interface circuitry. Here the digital signal is converted to analog, level shifted and amplified, filtered, buffered, and output through the 6809/MRTI interface circuitry to the 6809 trunking controller via J14 on the station backplane.

MRTI Interface

MRTI audio from an external MRTI module is input to the station via J14 on the station backplane. The signal is routed through the 6809/MRTI interface circuitry and fed to one input of an 8-to-1 multiplexer. If selected, the MRTI TX AUDIO signal is converted to a digital signal by the A/D portion of the CODEC IC and sent to the DSP ASIC via the audio interface bus.

MRTI RX audio is output from the DSP to the DSP ASIC and sent out the local audio interface bus via the audio interface bus to the audio interface circuitry. Here the digital signal is converted to analog, level shifted and amplified, filtered, buffered, and output through the 6809/MRTI interface circuitry to the 6809 trunking controller via J14 on the station backplane.

Front Panel LEDs and Switches (See Figure 7)

Front Panel LEDs

Eight status LEDs are provided on the SCM front panel to provide visual indications of various station operating conditions. The LEDs are controlled by eight lines from I/O port P0 Out.

LED Addresses and "ON" States

The hardware addresses, "ON" states, and initial states for the LEDs are presented in the table below.

Table 1: *LED Addresses and States*

Control On	P0_OUT, bit 7	Logic '1'	OFF
Control Fail	P0_OUT, bit 6	Logic '0'	ON
Intercom	P0_OUT, bit 5	Logic '1'	OFF
Control Channel	P0_OUT, bit 4	Logic '1'	OFF
RX1 Active	P0_OUT, bit 3	Logic '1'	OFF
RX2 Active	P0_OUT, bit 2	Logic '1'	OFF
RX Fail	P0_OUT, bit 1	Logic '1'	OFF
Aux LED	P0_OUT, bit 0	Logic '1'	OFF

Power Up and Reset Operation

After power up and reset all LEDs momentarily illuminate to demonstrate functionality then turn off for at least 1 second before they display the actual state of their labeled function.

Normal Operation

The normal operation of the LEDs is defined below:

Table 2: *Normal LED Operation*

Control On	Green	On	Control Module fully functional.
		Flashing	Front panel switch press detected or 5MHz NET in process.
		Off	Control Module malfunction.
Control Fail	Red	On	Control Module failure or reset.
		Flashing	Station is in failsoft mode. (trunking systems only).
		Off	Control Module fully functional.
Intercom	Yellow	On	Station is in intercom mode.
		Flashing	Station is in access disable mode.
		Off	Station is not in intercom mode.
Control Channel	Green	On	Station is control channel (trunking systems only).
		Flashing	Flashes each time an ISW is decoded (trunking systems only).
		Off	Station is not control channel (trunking systems only).

Table 2: *Normal LED Operation*

RX1 Active	Green	On	Receiver 1 is active.
		Off	Receiver 1 is Inactive.
RX2 Active	Green	On	Receiver 2 is active.
		Off	Receiver 2 is inactive.
RX Fail	Red	On	Neither receiver is functional.
		Flashing	Receiver 1 is not functional. (1 blink per second)
		Flashing	Receiver 2 is not functional. (2 blinks per second)
Aux LED	Green	Off	Both receivers are fully functional.
		On	Per customer requirement.
		Off	Per customer requirement.

Front Panel Switches

Four momentary contact pushbutton switches are provided on the SCM front panel to allow station functions to be selected. Pressing a push button causes a high signal to be sent to the host µP via I/O port P0 In.

The switches may be accessed and interpreted per the table below when enabled.

Table 3: *Front Panel Switch Addresses and Logic States*

Volume Up	0	PO_IN, bit 7	Switch Depressed	0
Volume Down	1	PO_IN, bit 6	Switch Depressed	0
Squelch Mode	2	PO_IN, bit 5	Switch Depressed	0
Intercom	3	PO_IN, bit 4	Switch Depressed	0

Normal Switch Function Operation

The switch function, except for the intercom switch, occurs after a valid low-to-high transition (button pressed). The intercom switch function occurs after a valid low-to-high then high-to-low transition (button pressed then released). The normal switch functions are described in the table below, when enabled.

Note: *Each volume down button press lowers volume one step. Pressing and holding the volume down button for 2 seconds shuts off the local speaker. Therefore, pressing and holding the volume down button for 2 seconds has the effect of reducing the volume by one step and shutting off the local speaker. Pressing the volume up button raises the volume one step and turns on the local speaker at the same volume at which it was shut off. Thus repeatedly switching the speaker on and off leaves the volume level unchanged.*

Table 4: *Normal Switch Functions*

Volume Up	Increment speaker volume one of 16 steps. Turn on local speaker, if off.	Step 10
Volume Down	Decrement speaker volume one of 16 steps.	Step 10
Volume Down (Hold 2 sec, see side note)	Turn off local speaker.	Speaker off
Squelch Mode	Step to next squelch state: (Off, CSQ, PL, Off)	CSQ
Intercom	Toggle intercom mode: (Off, On, Off)	Off

Note: *Speaker on/off affects internal speaker only. Volume affects internal speaker, external speaker and handset.*

Volume Control

The volume control for the local speaker, external speaker, and handset speaker can be performed by the DSP or by the wideband Rx D/A converter in Epsilon. The DSP-based volume steps are defined on a logarithmic scale.

Supply Voltages Circuitry

The SCM contains on-board regulator and filtering circuitry to generate the various operating voltages required by the SCM circuitry. +14.2 V and +5V from the backplane are used as sources for the following supply voltage circuits:

- +14.2 Vdc provides VCCA (+5V) for the analog circuitry
- + 5 V VCC C1809 Regulatory Circuit provides:
  - +3.3Vdc by means of a high efficiency DC to DC converter to power most of the digital logic on the board,
  - +2.5V U1801-4 reference voltage (½ of VCC) for the Audio Interface Circuitry in the SCM
  - +1.8Vdc for the DSP core circuitry.

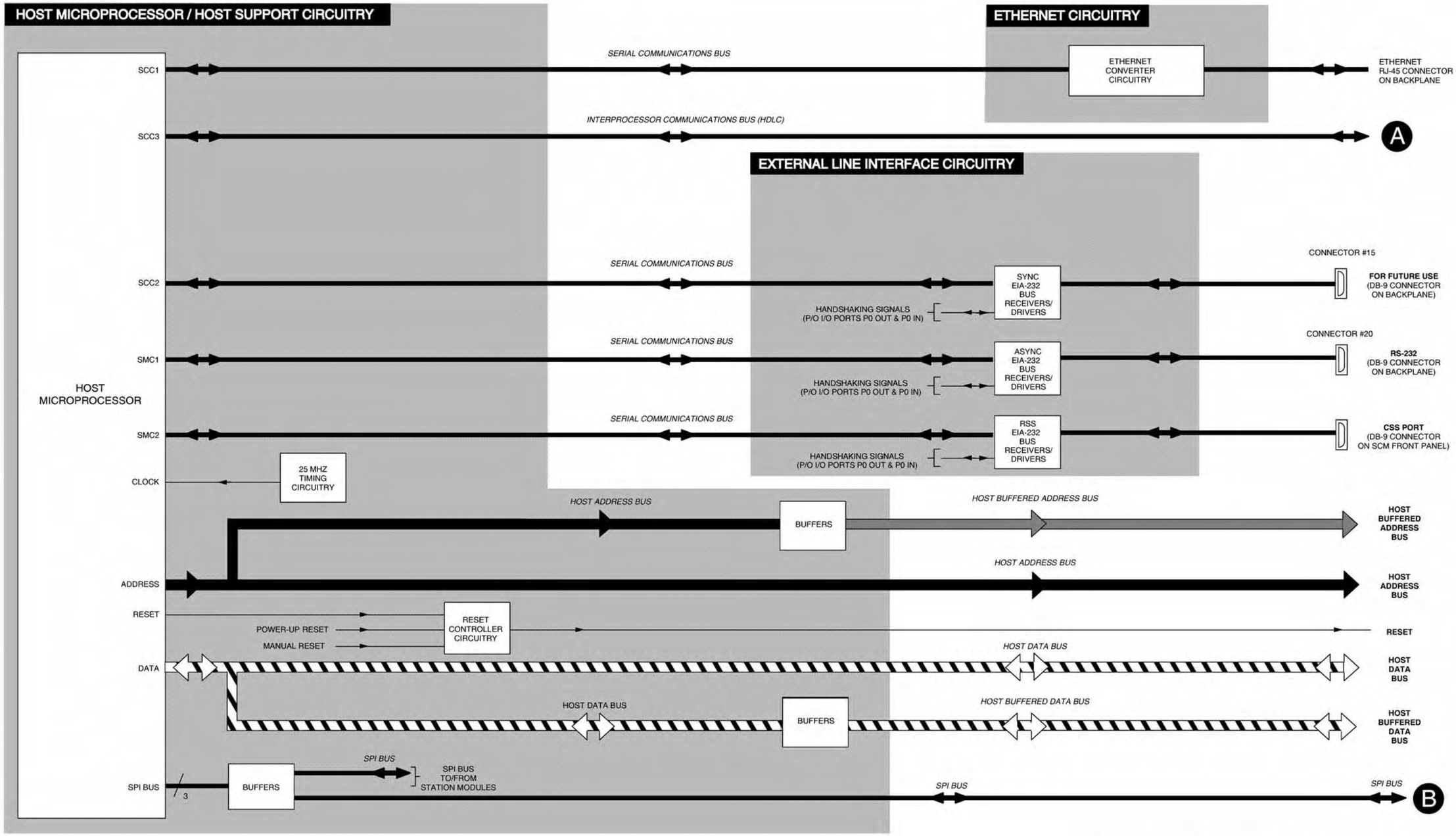


Figure 2 Station Control Board Functional Block Diagram (Sheet 1 of 5)

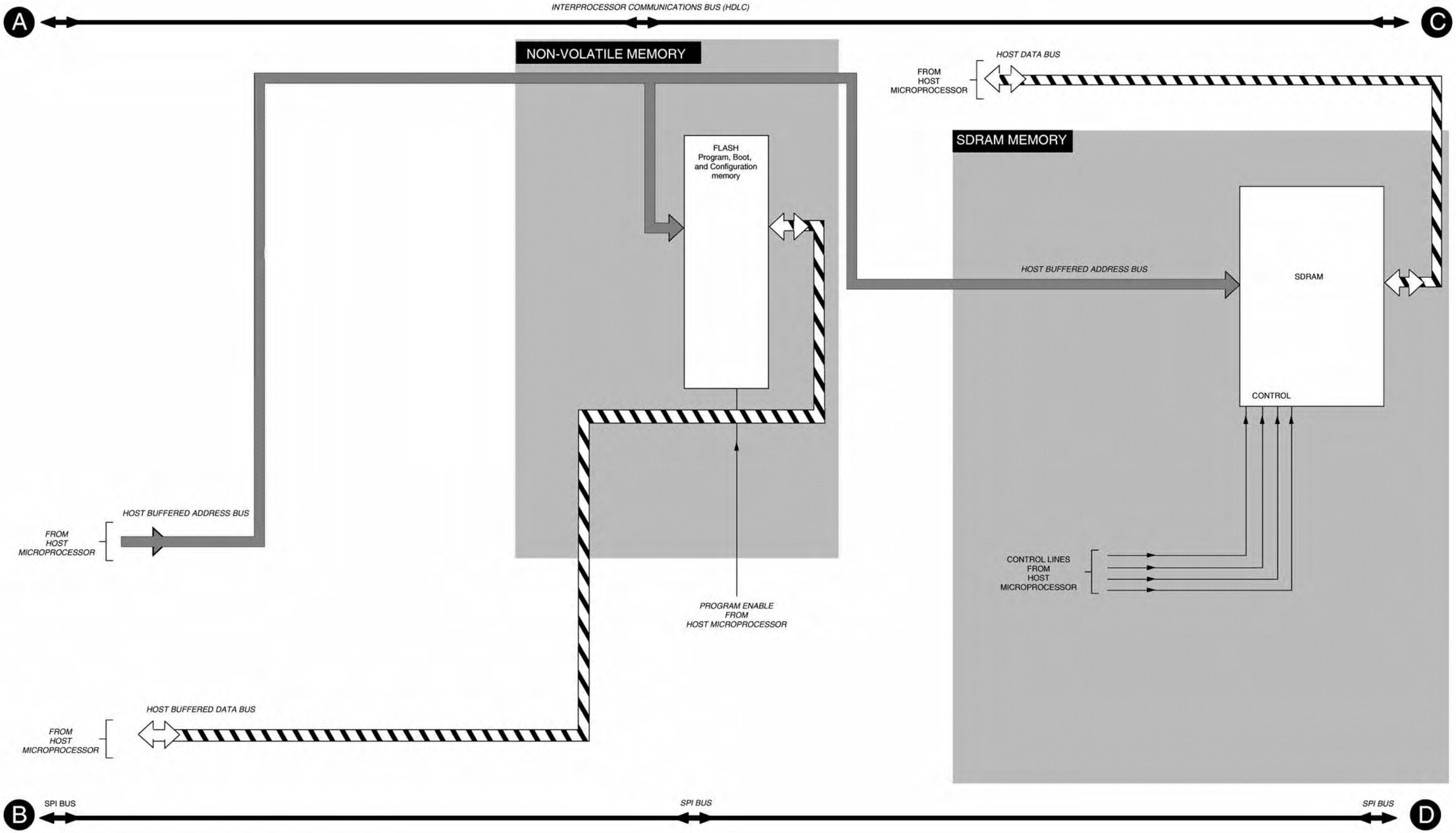


Figure 3 Station Control Board Functional Block Diagram (Sheet 2 of 5)

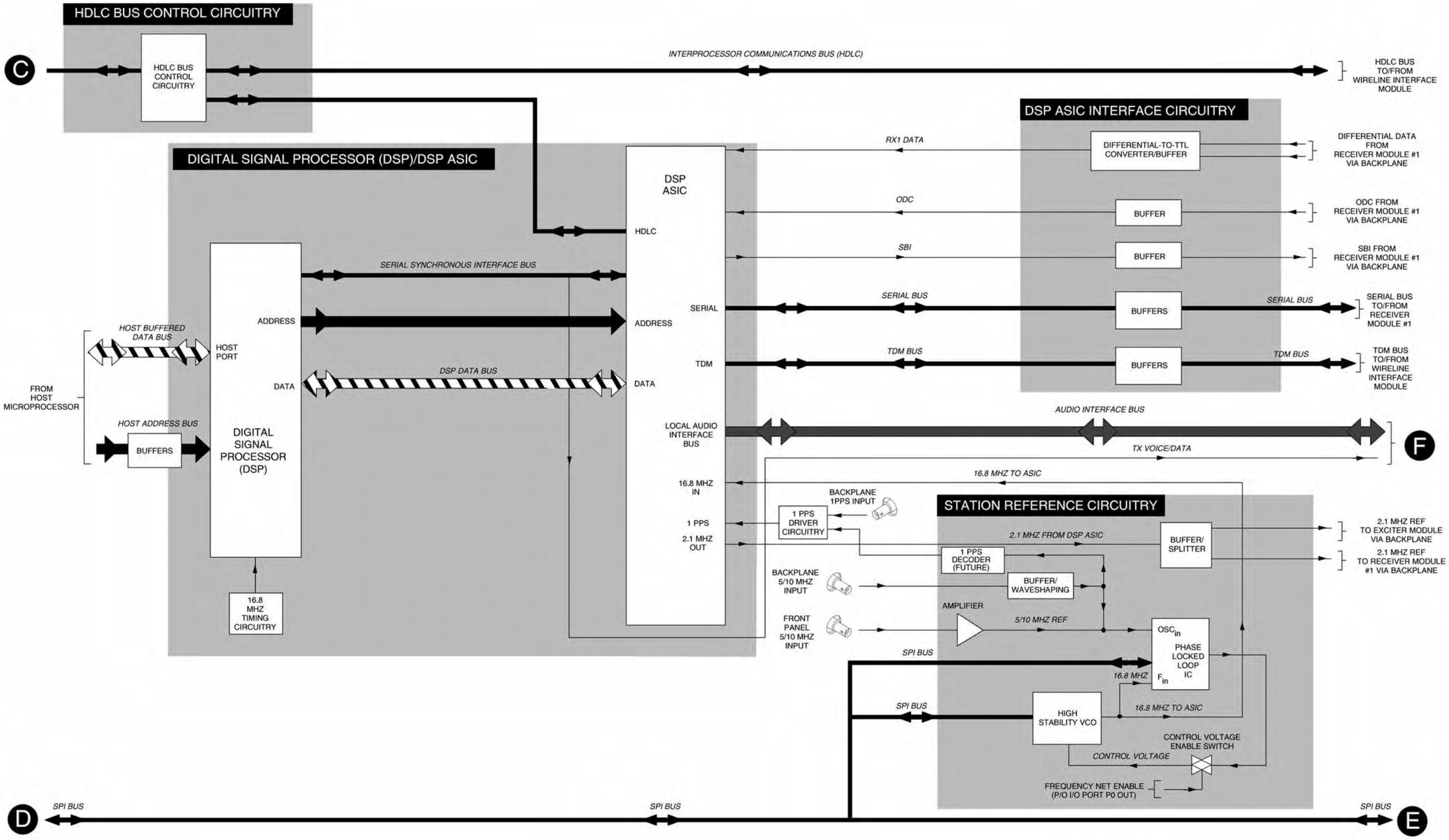


Figure 4 Station Control Board Functional Block Diagram (Sheet 3 of 5)

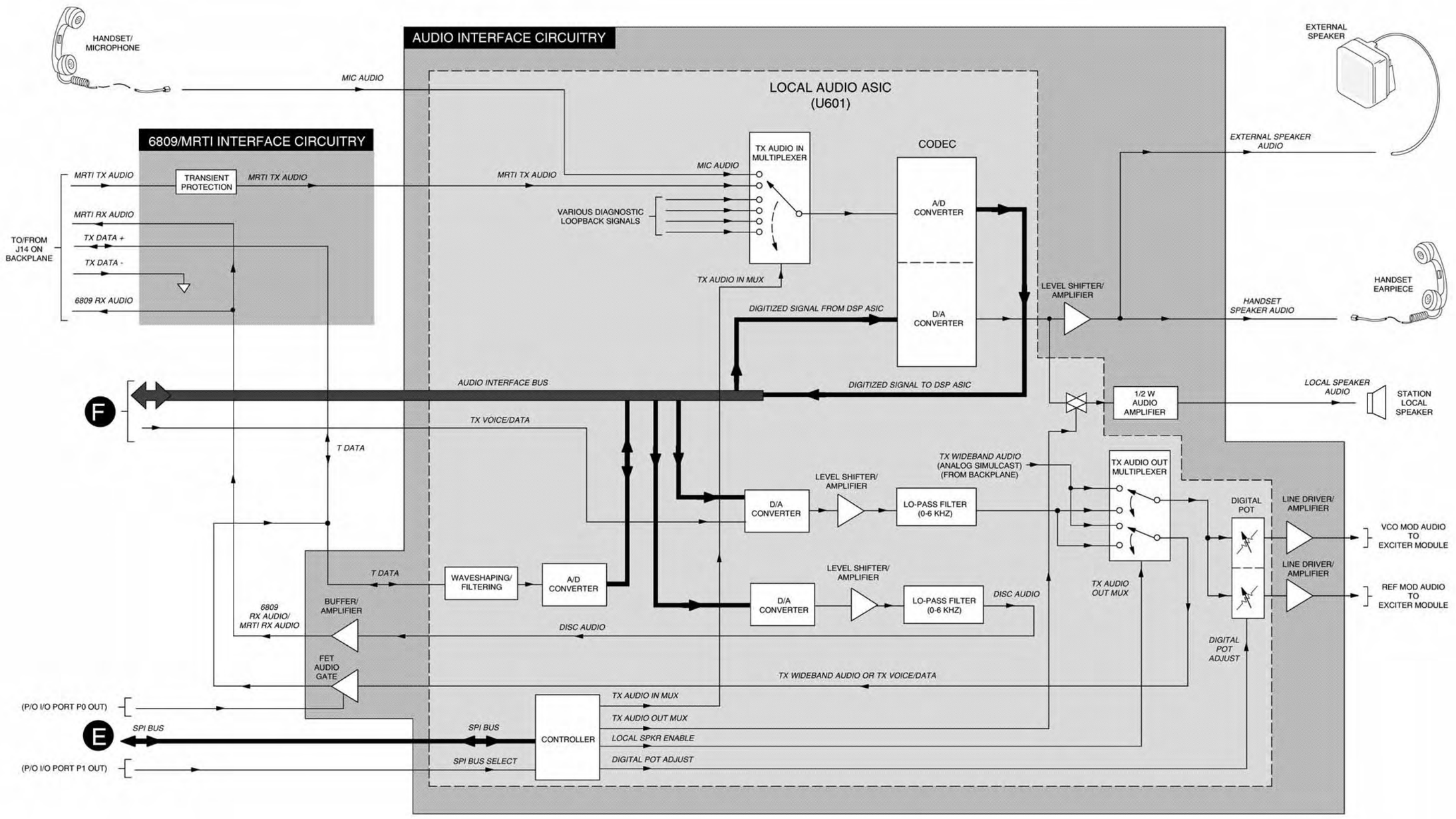
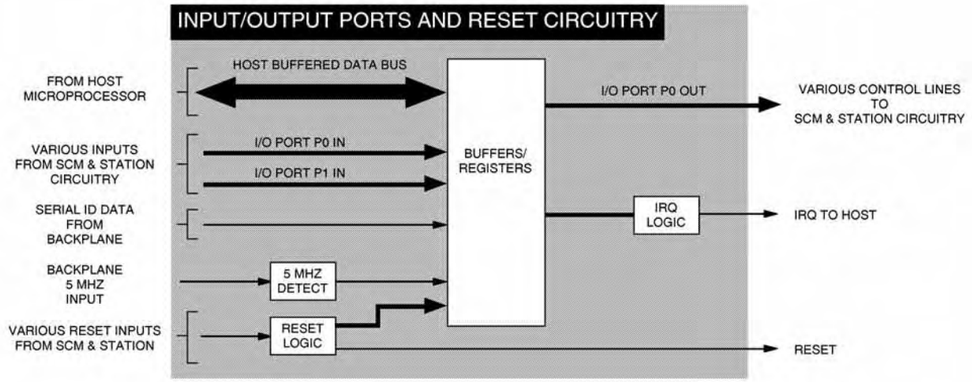


Figure 5 Station Control Board Functional Block Diagram (Sheet 4 of 5)



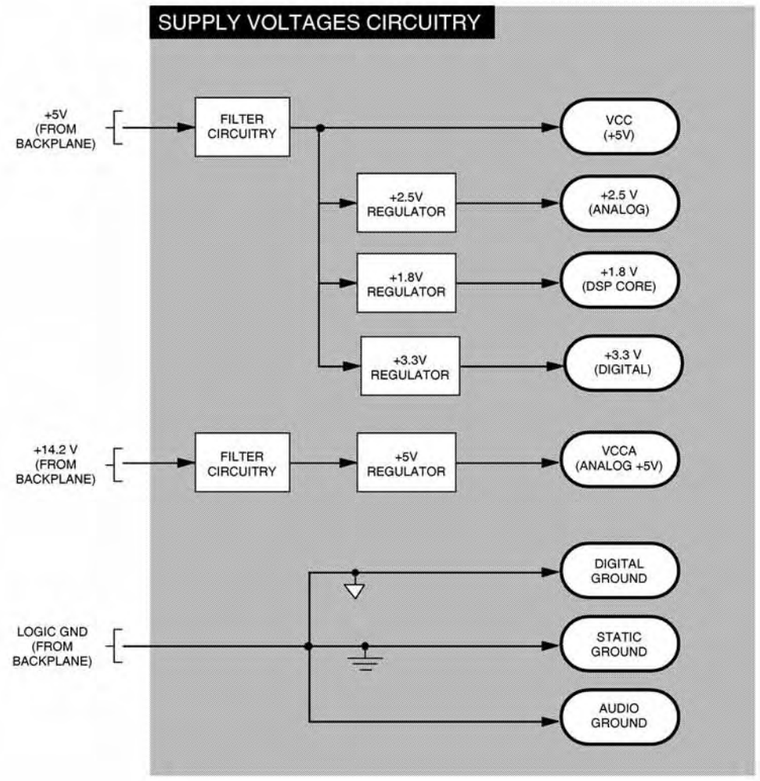


Figure 6 Station Control Board Functional Block Diagram (Sheet 5 of 5)

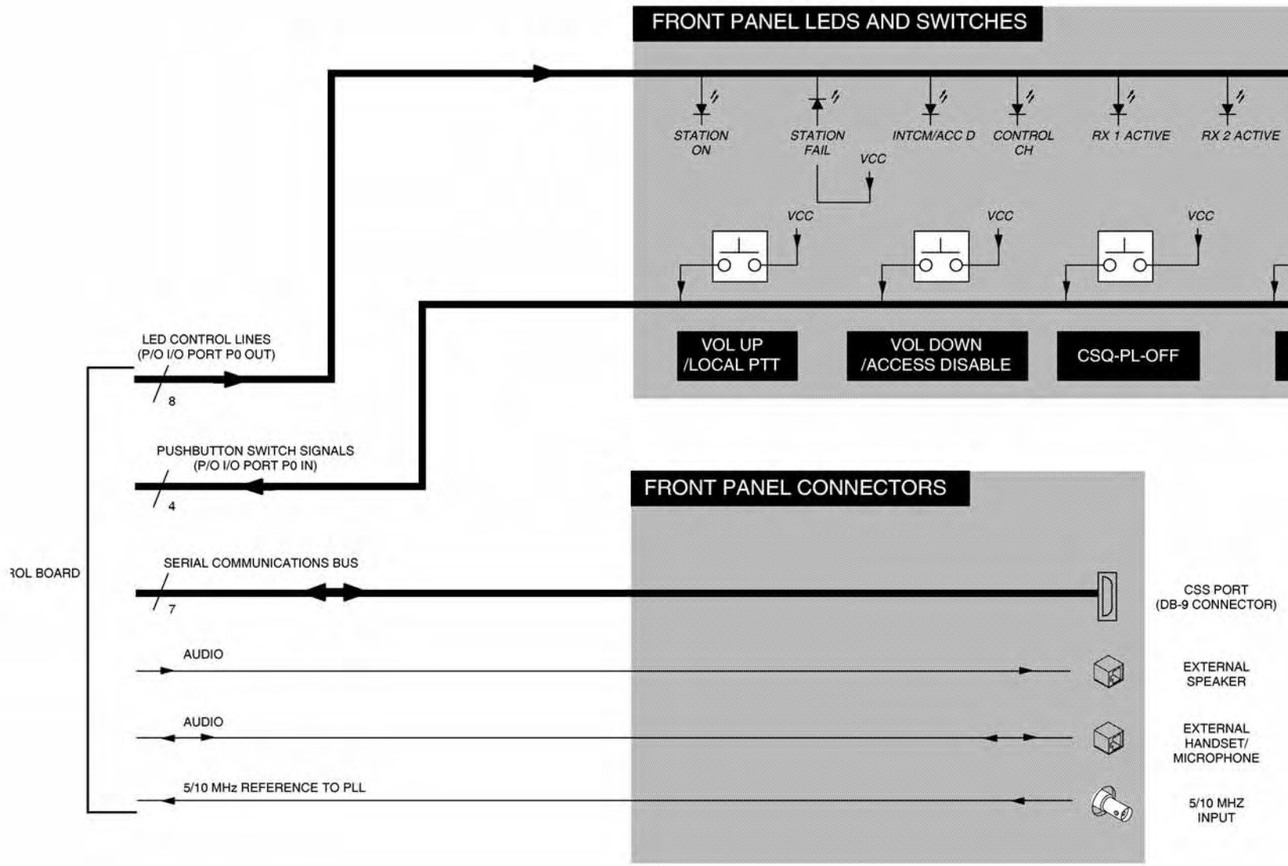


Figure 7 Front Panel LEDs and Switches

END OF PART 7