THEORY OF OPERATION

1. INTRODUCTION

1.1 This section describes the Theory of Operation of the *DVP MCX100* Radio Set. To help the serviceman more readily understand the discussion, the material is presented in three distinct levels: General Description, Functional Description, and Detailed Description.

- General Description — For ease of discussion, the circuits comprising the radio set are organized into seven functional groups. The General Description introduces the serviceman to these functional groups and gives a brief description of each. An accompanying block diagram outlines the functional groups, shows the relationship and signal flow between the groups, and the signal flow through the groups (where applicable).

- Functional Description — This description further details the operation of each functional group. A supporting functional block diagram accompanies each description to show the circuits, signals, and interconnections that go to make up the group.

- Detailed Description — The detailed description gives complete circuit descriptions for each functional group. In this description, the schematic diagrams in the diagrams section are used as references.

1.2 As an additional aid, an overall functional interconnection diagram of the radio set is provided in the manual.

2. GENERAL DESCRIPTION
(Refer to Figure 1)

2.1 The Front Mount Radio Set operates in the VHF frequency range of 136 to 174 MHz, and, depending on the model used, can provide rf power output of either 10 or 30 watts in systems employing minimum channel spacing of either 25 or 30 kHz. Models allowing use of up to 32 channels are available.

2.2 The seven functional groups that make up the *DVP MCX100* radio set are: receiver circuits, transmitter circuits, frequency synthesizer circuits, *DVP* (Digital Voice Protection) circuits, PL/DPL (*Private-Line/Digital Private-Line*) circuits, time-out timer circuits, and power distribution circuits. A brief description of each functional group is given in the following paragraphs.

2.3 RECEIVER CIRCUITS

2.3.1 The receiver circuits in the standard radio set use a single front end that utilizes FETs (field-effect transistors) for rf amplification, mixing, and i-f input stages for high sensitivity and low noise; crystal filters for i-f selectivity; and integrated circuits for amplication, limiting, and detection. The standard, single front end provides a receive bandwidth of 4 MHz.

2.3.2 An optional widespaced dual front end allows a total receive bandwidth of 12 MHz; it provides two 6 MHz "windows" which may be independently tuned anywhere within the 136 to 162 or 146 to 174 MHz bands. Tuning within each band is accomplished by two 6 MHz-wide tuneable helical filters. Selection of either the low range or high range 6 MHz filter is under the control of the frequency synthesizer circuits (front end select signal).

2.3.3 The receive rf from the antenna and the receive injection signal from the frequency synthesizer circuits are mixed in the single front end (or optional widespaced dual front end) to produce the 21.4 MHz i-f frequency. The i-f signal is amplified, filtered, and applied to a limiter/quadrature detector to recover the audio from the frequency-modulated carrier. The recovered audio is processed by low level audio and muting circuits. The receiver audio is then amplified by the audio amplifier and applied to the speaker.

2.3.4 The low level audio and muting circuits also process the sidetone/alert tone from the *DVP* circuits, the PL/DPL circuits (or optional time-out timer circuits) and the PL filtered audio (from the PL/DPL

circuits). The audio muting circuits mute the receiver audio in response to control signals from the receiver squelch circuits (when no on-channel carrier is present); the transmitter circuits (when PTT is keyed); the frequency synthesizer circuits (when out-of-lock); the *DVP* circuits; or the PL/DPL circuits (when a valid tone-coded or binary-coded signal is not received). The *DVP* circuits, optional time-out timer circuit, or PL/DPL circuits can also gate audio to the speaker to allow insertion of sidetones or alert tones into the audio path.

2.3.5 The low level audio circuit also supplies an option receive audio signal to the *DVP* circuits for code detection and audio recovery. If the signal is not coded, the audio is routed either back to the low level audio circuits, or to the PL/DPL board (in radios so equipped) for tone decoding and filtering before being returned to the low level audio circuits. If the signal is coded, the *DVP* recovered audio is routed back to the low level audio circuits.

2.3.6 The squelch circuit incorporates a high-speed, variable closing-time constant that provides optimum squelch performance for both weak and strong signals. Pushing in the squelch pushbutton on the front panel defeats the carrier squelch circuits, unsquelching the receiver audio.

2.3.7 A front panel BUSY light is used in PL/DPL squelch or *Select 5* signaling models to indicate channel activity.

2.4 TRANSMITTER CIRCUITS

2.4.1 The transmitter circuits amplify the frequency-modulated low level rf output (transmit injection signal) from the frequency synthesizer circuits for radiation by the antenna. The transmit injection signal is applied to the low level amplifier (exciter), which supplies the rf drive for the 10 watt power amplifier. The final rf is applied through a harmonic filter/antenna switch to the antenna. In 30 watt models, the 10 watt power amplifier supplies the rf drive for the higher-powered amplifier.

2.4.2 A transmit power and level control circuit monitors the control voltage supplied by a directional coupler, located on the harmonic filter/antenna switch hybrid, to maintain the radiated rf output at a relatively constant level regardless of operating frequency, battery voltage, or temperature. A control circuit shuts down the transmitter if the synthesizer frequency goes out-of-lock (lock detect signal), or reduces output power to prevent damage to the rf final amplifier if a fault occurs in the antenna system.

2.4.3 PTT signals from the microphone, (which are processed by the *DVP* circuits, the PL/DPL circuits, or the optional time-out timer circuits, if present) are applied to a PTT logic circuit to control transmitter keying. A transmitter audio/IDC (instantaneous deviation control) circuit processes the microphone audio to produce the IDC audio. The microphone audio is also pre-emphasized in the transmit audio/IDC circuitry. If the radio is transmitting in the private mode, this audio is digitized and then encrypted by the *DVP* circuits. The encrypted bits are then used to modulate the VCO (voltage controlled oscillator), and the 14.4 MHz reference oscillator in the frequency synthesizer. If the radio is transmitting in the clear mode, the IDC audio directly modulates the VCO. In DPL radios, the PL/DPL circuits also generate a reference modulation signal which modulates the 14.4 MHz reference oscillator. By modulating the reference oscillator, the low frequency modulation capability of the radio is extended nearly to dc, a requirement for both *DVP* and DPL.

2.5 FREQUENCY SYNTHESIZER CIRCUITS

2.5.1 The frequency synthesizer circuits generate the low side receive injection frequency and the transmit injection signal. In the receive mode, the frequency synthesizer locks on a frequency that is 21.4 MHz (i-f frequency) lower than the desired receive frequency. In the transmit mode, the frequency synthesizer locks on the transmit output frequency. The frequency synthesizer is set to the transmit mode by the +9.6T keying voltage generated by the transmitter circuits.

2.5.2 The frequency synthesizer employs a phase-locked-loop that maintains a constant VCO frequency (limited only by the frequency stability of the 14.4 MHz reference oscillator). Logic circuitry controls the operating frequency of the phase-locked VCO. Frequency select data from the front panel channel selector switch is applied to a plug-in PROM (programmable read-only memory) module. The PROM is factory-programmed or field-programmed with customer-specified data that determines the transmit and receive frequencies for each position of the channel selector switch. Channels can be added or changed by simply changing the PROM.

2.6 *DVP* CIRCUITS

2.6.1 The Digital Voice Protection (*DVP*) circuitry interfaces with the radio's audio circuits to add a high security scrambled voice mode. Microphone audio is digitized, transformed into cipher, and applied to the transmitter circuits. Similarly, received cipher is transformed into audio and applied to the speaker. Logic circuits and audio switches allow operation in either the private (coded) mode or the standard (clear) mode.

2.6.2 The private mode employs a digital non-linear coding scheme. Microphone audio is digitized by a Continuously Variable Slope Delta modulator (CVSD) whose output is applied to a non-linear digital

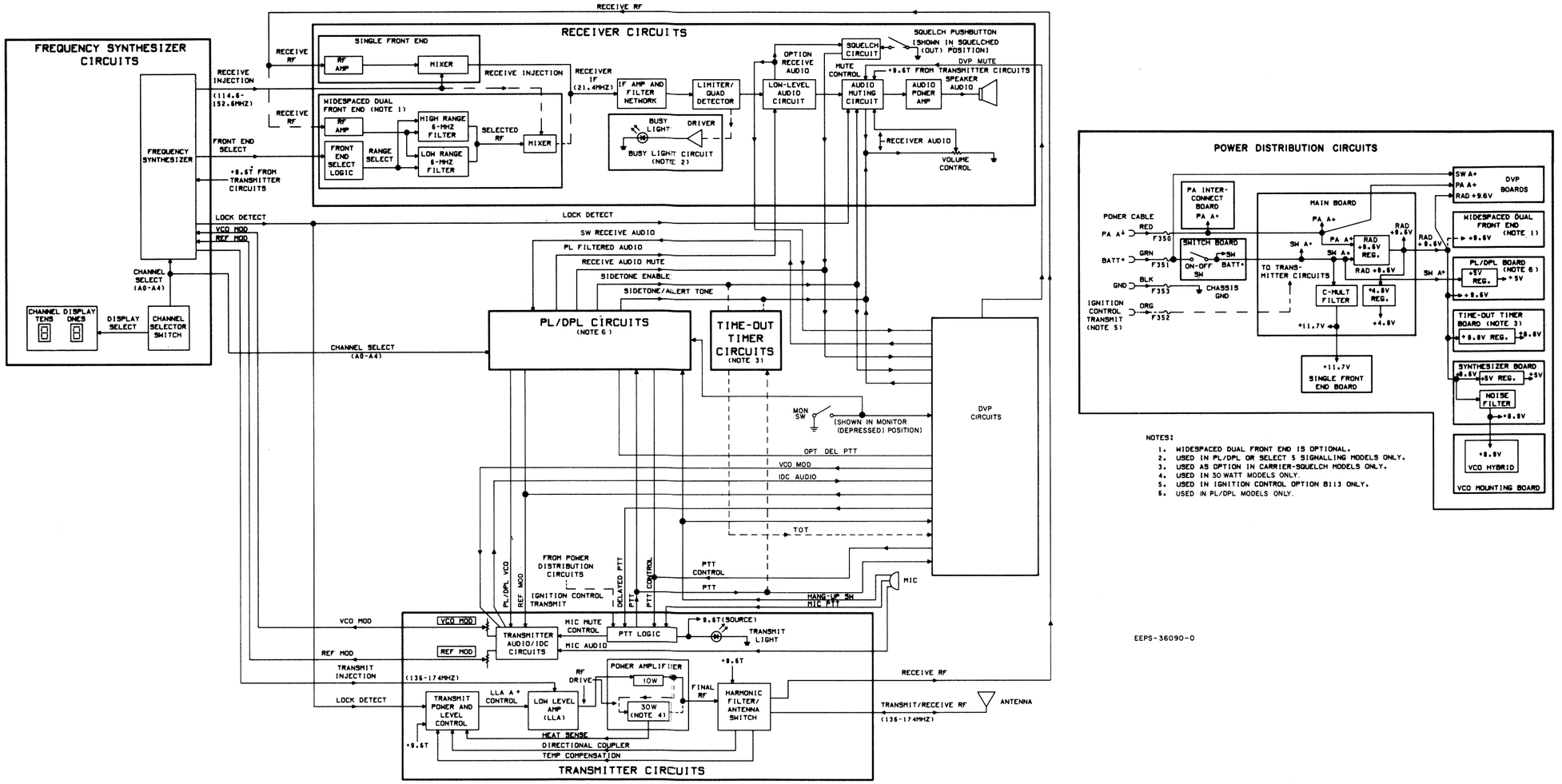
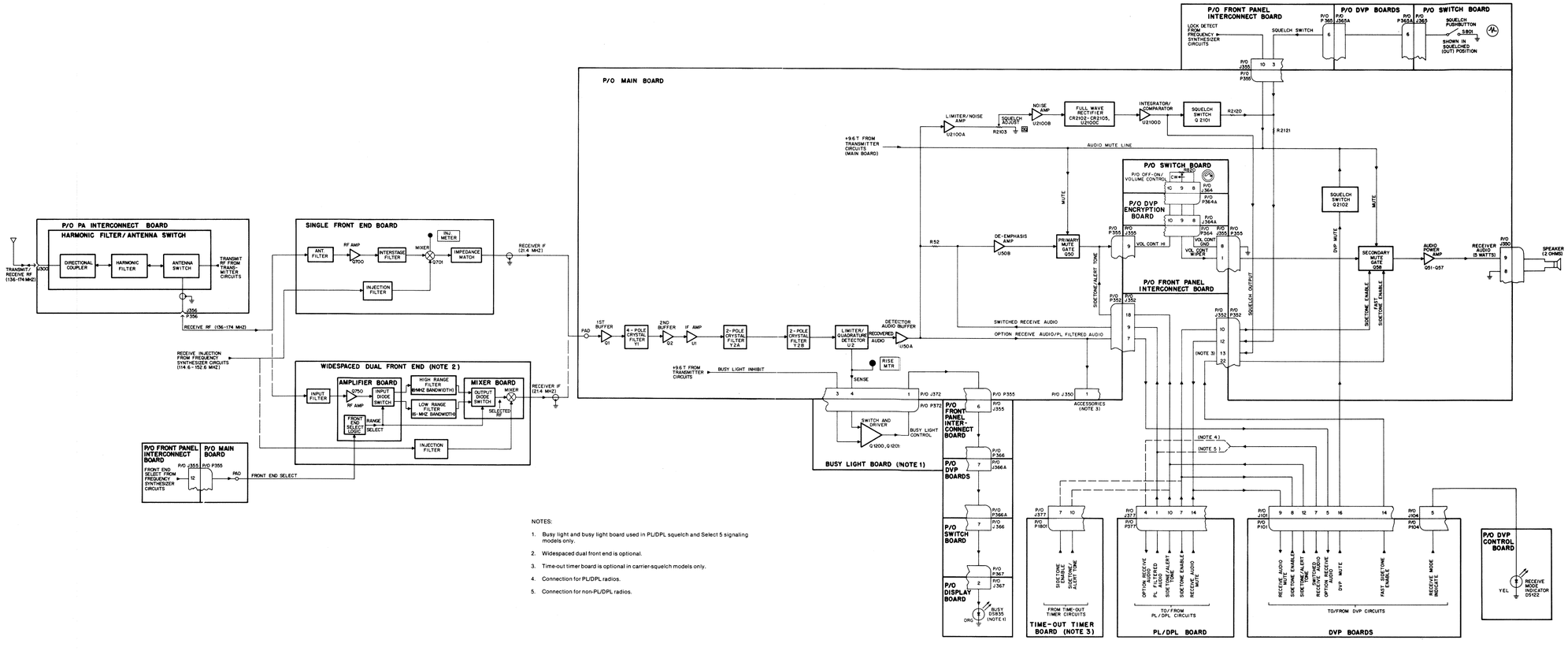


*Figure 1. **DVP MCX100** Front Mount Radio Set, Functional Block Diagram*



NOTES:

1. Busy light and busy light board used in PL/DPL squelch and Select 5 signaling models only.
2. Widespaced dual front end is optional.
3. Time-out timer board is optional in carrier-squelch models only.
4. Connection for PL/DPL radios.
5. Connection for non-PL/DPL radios.

Figure 2. Receiver Circuits, Functional Block Diagram

EEPS-35713-O

encryption circuit. The encrypted data is then filtered and used to modulate the synthesizer. In the receive mode, cipher from the discriminator is applied to a decoder whose digital output is converted to an analog signal by the CVSD. A filter shapes the received audio before it is applied to the speaker amplifier circuit.

2.6.3 All Motorola *DVP* system components (base stations, mobiles, and portables) utilize a self synchronizing non-linear digital voice scrambling scheme with a capacity for 2.36×10^{21} unique orthogonal codes. Once loaded the chosen code is internally stored and completely unreadable. A single electronic key inserter (with appropriate interconnect cable) allows easy code insertion on any desired schedule. Selection of either private or standard transmissions may be made at the front panel by the operator.

2.6.4 Additional features are included to ensure operator convenience and flexibility.

- Fully automatic selection and front panel indication of private receive mode.
- Audible alert to remind the operator that he is initiating a standard transmission.

2.6.5 Optional functions are also available to expand the radio's capabilities. These are dual code capability and proper code detect circuitry.

2.7 PL/DPL CIRCUITS

2.7.1 The PL/DPL circuits encode (during transmit) and decode (during receive) the sub-audible *Private-Line* and *Digital Private-Line* squelch signals for compatibly-equipped radios. The *Private-Line* or *Digital Private-Line* coded squelch information is programmed into a code plug (used in single-code PL/DPL configurations), or a personality ROM (read-only-memory) used in multiple-code PL/DPL configurations. The *Private-Line* squelch eliminates annoying co-channel message reception by accepting only those signals with the proper, predetermined tone code. The *Digital Private-Line* squelch allows only those calls that use the proper system code to be heard. A front panel Monitor pushbutton, when pushed in, defeats the PL/DPL decoder circuits, allowing all activity on the channel to be monitored. The PL/DPL decoder circuits are also automatically defeated when the microphone is removed from its hang-up clip.

2.7.2 The PL/DPL circuits are controlled by a microcomputer which accomplishes all tone (or code) generation and detection digitally, eliminating all mechanical reed assemblies. The circuits also incorporate a time-out timer function that unkeys the transmitter after a predetermined interval. This prevents accidental (or intentional) repeater lock-up, or tying up a channel by prolonged transmitter keying. A sidetone/alert tone, audible in the speaker, warns the operator that the timer is shutting off the transmitter. The timer is reset instantly when the PTT button on the microphone is released.

2.8 TIME-OUT TIMER CIRCUITS

The time-out timer circuits are an option used in carrier squelch models. The circuits perform the same function as the time-out timer previously described in the PL/DPL circuit description.

2.9 POWER DISTRIBUTION CIRCUITS

The power distribution circuits supply and distribute all the necessary dc power required to operate the radio set. The radio set is designed for use in 12 V dc negative ground systems only. Power inverters are available for use in systems having different voltages or polarity. Input power is applied to the radio set via a three-wire fused power cable. A fourth fused wire is connected to the vehicle ignition switch in radios employing ignition control option B113. The Off-on/Volume switch on the front panel controls the application of power to the radio set.

3. FUNCTIONAL DESCRIPTION

3.1 RECEIVER CIRCUITS
(Refer to Figure 2)

The receiver circuits are functionally arranged into the single front end, the optional widespaced dual front end, and the main board receiver circuits.

3.1.1 Single Front End

The standard single front end is located on the single front end board. The single front end generates the receiver i-f signal using the receiver rf signal from the antenna switch in the transmitter circuits and the receiver injection signal from the frequency synthesizer circuits. The receiver rf is filtered by an antenna filter, amplified by rf amplifier Q700, filtered again by an interstage filter, and finally applied to mixer Q701. The receiver injection signal is also applied to the mixer, via an injection filter. The mixer combines the two signals to produce the 21.4 MHz receiver i-f signal which is applied through an impedance matching network to the receiver circuits on the main board.

3.1.2 Widespaced Dual Front End

3.1.2.1 The optional widespaced dual front end is housed in a metal casting that is mounted to the main board. Except for the helical filters, circuit components are mounted on an amplifier board and a mixer board, located inside the casting. The widespaced dual front end provides extended frequency coverage by switching the receiver rf between two, 6 MHz-wide,

tuneable helical filters. Each filter can be tuned to any desired 6 MHz-wide frequency band within the frequency range of the radio. Switching between ranges is controlled by the front end select signal supplied by frequency synthesizer circuits. As in the single front end, the widespaced dual front end generates the receiver i-f signal using the receiver rf signal from the antenna switch in the transmitter circuits and the receiver injection signal from the frequency synthesizer circuits. The receiver rf is filtered by an input filter, amplified by rf amplifier Q750, and applied to an input diode switch. The input diode switch, together with an output diode switch, determine which rf frequency range is selected.

3.1.2.2 Frequency range selection is determined by the logic state of the front end select signal applied to the front end logic circuit. When the front end select signal is high, the front end logic circuit switches the input and output diode switches to a high-range condition. This routes the output from the rf amplifier through the high range filter to the mixer. When the front end select signal is low, amplified rf is switched to the mixer via the low range filter. Also applied to the mixer, via an injection filter, is the receiver injection signal. The mixer combines the two signals to produce the 21.4 MHz receiver i-f signal that is applied to the receiver circuits on the main board.

3.1.3 Main Board Receiver Circuits

The remainder of the receiver circuits are located on the main board and are functionally arranged into the following circuits: an i-f circuit, a limiter/quadrature detector, a low-level audio circuit, a audio muting circuit, an audio power amplifier, and a squelch circuit. Additionally, in PL/DPL squelch or *Select 5* signaling models, a busy light circuit is included.

3.1.3.1 I-F Circuit

The i-f circuit consists of two buffers, an i-f amplifier, and a series of crystal filters cut to a fundamental frequency of 21.4 MHz. The receiver i-f signal from the single front end (or the optional widespaced dual front end) is applied through first buffer Q1 to four-pole crystal filter Y1. The filtered i-f output from Y1 is buffered again by Q2, amplified by U1, and further filtered by two-pole crystal filters Y2A and Y2B. The amplified and filtered i-f output from Y2B is applied to limiter/quadrature detector U2.

3.1.3.2 Limiter/Quadrature Detector U2

Limiter/quadrature detector U2 is an integrated circuit that recovers the audio from the frequency-modulated carrier. The limiter/quadrature detector buffers the recovered audio and applies it to the low-level audio circuit. In PL/DPL or *Select 5* signaling models, it also supplies a sense signal to the busy light circuit to control the busy light on the front panel.

3.1.3.3 Low-Level Audio Circuit

The low-level audio circuit consists of detector audio buffer U50A and de-emphasis amplifier U50B. The recovered audio from the limiter/quadrature detector is applied through U50A to U50B. The recovered audio from U50A is also applied as the optional receive audio to the *DVP* circuits, and to accessories connector J350-1. If this is a *DVP* signal, the re-constructed audio is switched back into the low level audio path. If it is not a *DVP* signal, then it is routed, unchanged, back into the low level audio path. If the radio is equipped with PL/DPL the audio is then routed to the PL/DPL board. The PL/DPL circuits, in turn, inject the PL filtered audio signal into the recovered audio path between U50A and U50B. The recovered audio is amplified and de-emphasized by U50B and is applied to primary mute gate Q50 in the audio muting circuit.

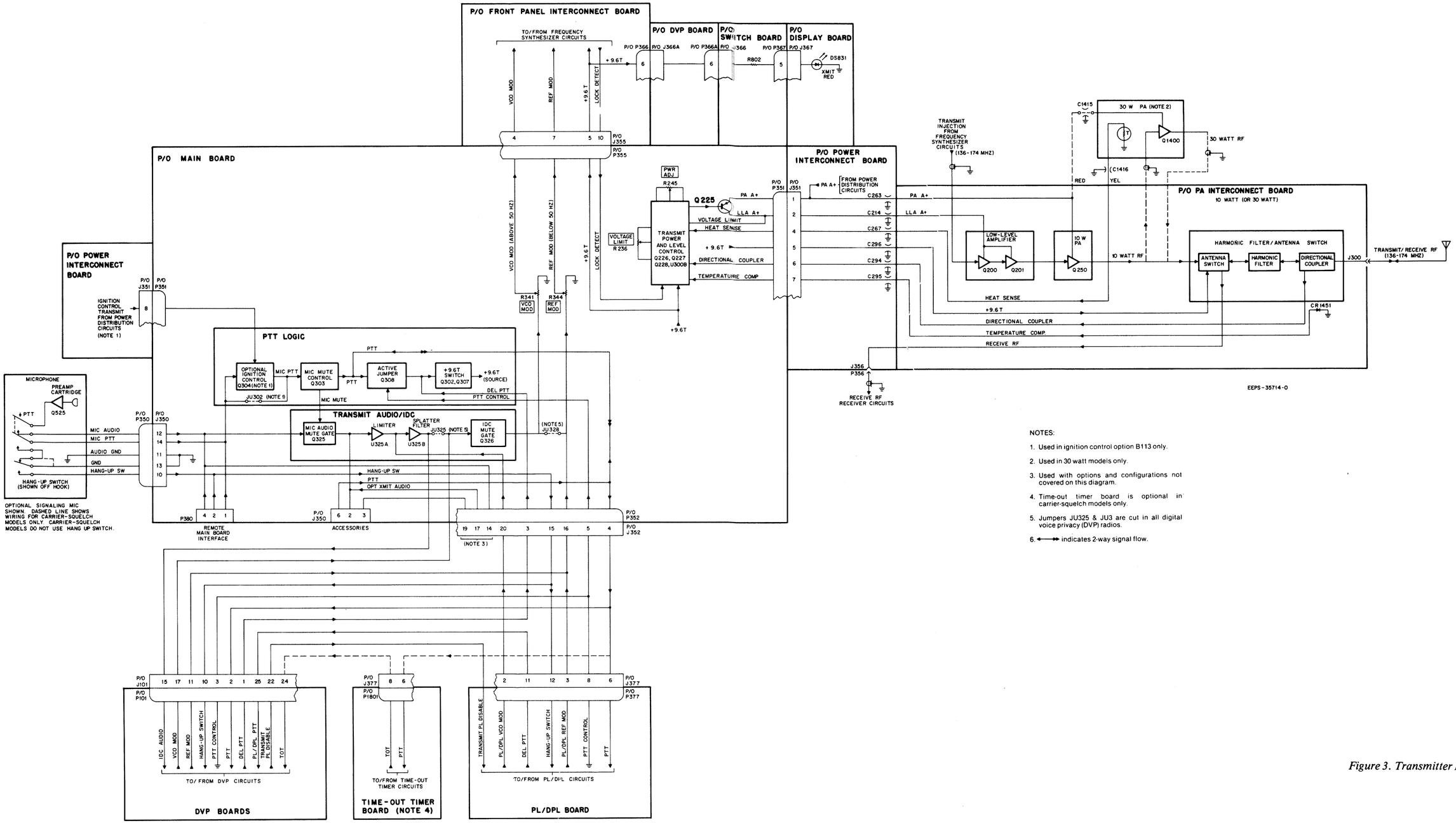
3.1.3.4 Audio Muting Circuit

3.1.3.4.1 Primary mute gate Q50 and secondary mute gate Q58 form the audio muting circuit. Audio inputs to the circuit are the recovered audio from the low-level audio circuit and the sidetone/alert tone from the *DVP* or PL/DPL circuits (or the time-out timer or *Select 5* signaling circuits). The sidetone/alert tone is inserted into the circuit, via the volume control, which is between Q50 and Q58.

3.1.3.4.2 The audio muting circuit gates the receiver audio on and off in response to four signals:

- the high lock detector (VCO lock) signal from the frequency synthesizer circuits;
- the +9.6T keying voltage from the transmitter PTT logic circuit;
- the sidetone enable signal from the *DVP*, PL/DPL, time-out timer, or *Select 5* circuits;
- the *DVP* mute signal which is a combination of *DVP* muting functions and the receive audio mute signal from the PL/DPL or *Select 5* circuits, and the squelch signal developed by the receiver squelch circuit.

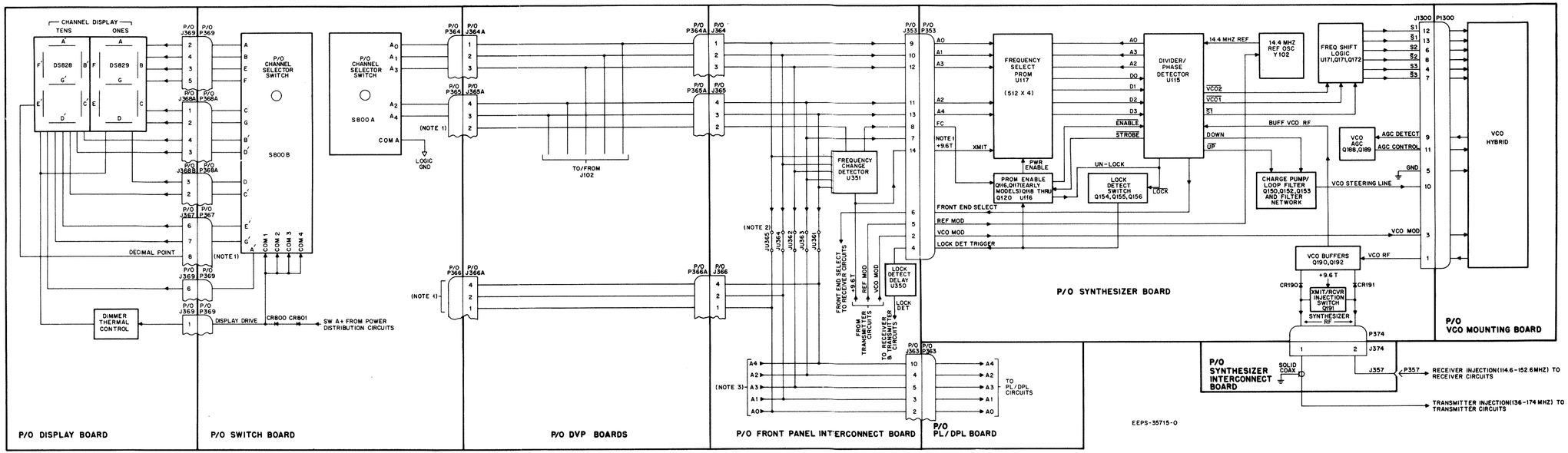
3.1.3.4.3 When no mute signal is applied to the audio mute line, series mute gate Q50 is on and shunt mute gate Q58 is off. This allows receiver audio from the low-level audio circuit to be applied through the volume control to the audio power amplifier. If the audio mute line is driven high, the audio is muted. This occurs when the synthesizer frequency is out-of-lock, the transmitter is keyed, the *DVP* circuitry has not detected a coded message, the PL/DPL circuit (or *Select 5* signaling circuits) have not decoded a correct signal, or the receiver quieting level is insufficient to open the squelch circuit.



NOTES:

1. Used in ignition control option B113 only.
2. Used in 30 watt models only.
3. Used with options and configurations not covered on this diagram.
4. Time-out timer board is optional in carrier-squelch models only.
5. Jumpers JU325 & JU3 are cut in all digital voice privacy (DVP) radios.
6. ⟷ indicates 2-way signal flow.

Figure 3. Transmitter Functional Diagram



NOTES:

1. Used with options and configurations not covered on this diagram.
2. Jumper JU361 used for multi-PL/DPL models only. Jumpers JU361-JU365 are removed in selectable PL/DPL option only.
3. In selectable PL/DPL option only, channel select address A0-A4 initiated by selectable PL/DPL board.

Figure 4. Frequency Synthesizer Functional Diagram

3.1.3.4.4 To allow the sidetone/alert tone to be inserted into the audio path when the recovered audio is muted, the sidetone enable signal is activated (goes low). This allows the sidetone/alert tone to be routed through the volume control to the audio power amplifier.

3.1.3.5 Audio Power Amplifier

The audio power amplifier consists of transistors Q51 through Q57. It supplies up to five watts of audio power to the speaker. A discrete design is used for low noise, high alternator whine rejection, and maximum possible audio output swing.

3.1.3.6 Squelch Circuit

3.1.3.6.1 The squelch circuit consists of four operational amplifiers, a full-wave rectifier, two squelch switch transistors, a variable time-constant stage, and the front panel squelch pushbutton. The recovered audio output from detector buffer U50A in the low-level audio circuit is applied to audio-captured limiter/noise amplifier U2100A. The output from U2100A is applied through SQ (squelch adjust) potentiometer R2103 (which adjusts the noise quieting level at which the squelch operates) to a second amplifier, U2100B. The amplified output from U2100B is detected by a full-wave rectifier to produce an average dc voltage at the output of the third amplifier, U2100C. The output voltage at U2100C is proportional to the receiver quieting level. This dc quieting level voltage is then compared to a fixed dc reference voltage by integrator/comparator U2100D. When the quieting level dc voltage is below the reference voltage (carrier signal absent), U2100D turns on squelch switch Q2101. This drives the receive audio mute line high. The receive audio mute line goes to the *DVP* board which then outputs a high on the *DVP* mute line. This turns on squelch buffer Q2102 which mutes the receiver. When the quieting level rises above the reference voltage (carrier signal present), squelch switch Q2101 and Q2102 turns off, putting a low on the receive audio mute line. This signal then goes to the *DVP* board, which puts a low on the *DVP* mute line, turning off Q2102 and unmuting the receiver. If the squelch pushbutton is pushed in (unsquelch position) the output at current driver Q2101 is grounded, preventing the squelch signal going to the *DVP* board from indicating a squelch condition, regardless of the noise quieting level.

3.1.3.6.2 The receive audio mute signal is also controlled by the PL/DPL (or *Select 5*) circuits. When a proper PL/DPL code is not received the receive audio mute signal goes high, causing the *DVP* board to put a high on the *DVP* mute line, muting the radio. When a valid PL/DPL code is detected, the PL/DPL circuits provide an active low on the receive audio mute line. This causes the *DVP* board to unmute the radio. The PL/DPL circuitry can prevent Q2101 from muting the receive audio, even though the level of noise quieting is below the squelch circuit opening threshold.

3.1.3.6.3 Variable time constant stage Q2100 (not shown in block diagram) provides a high speed closing time constant for strong signals, eliminating the noise bursts normally heard at the end of a transmission. The time constant increases during very weak signal conditions to eliminate the chatter that is often heard when signals fade. The variable time constant is controlled by the dc quieting level voltage from U2100C.

3.1.3.7 Busy Light Circuit

The busy light circuit controls the lighting of the front panel busy light in PL/DPL squelch or *Select 5* signaling models. The circuit is contained on the busy light board, which is mounted on the main board. The circuit consists of level detector Q1200 and driver Q1201, and uses the sense signal developed by limiter/quadrature detector U2, and the squelch output from U2100D to light the busy light, indicating channel activity.

3.2 TRANSMITTER CIRCUITS (Refer to Figure 3)

3.2.1 Circuit Boards

3.2.1.1 The transmitter circuits are arranged into functional groups that are mounted on the main board and the PA interconnect board. Two PA interconnect boards can be used, depending on the transmitter power output. In 10 watt models, a 10 watt PA interconnect board is used. In 30 watt models, a 30 watt interconnect board is used.

3.2.1.2 The main board contains part of the PTT logic circuit, the transmit audio/IDC (instantaneous deviation control) circuit, and the transmit power level and control circuit. The 10 watt PA interconnect board contains the low level amplifier, the 10 watt power amplifier, and the harmonic filter/antenna switch. The 30 watt PA interconnect board contains the same three functional groups just mentioned; in addition, the 30 watt power amplifier, mounted in the external heat sink, is added. In this high-power version, the 10 watt power amplifier drives the 30 watt power amplifier.

3.2.2 PTT Logic Circuit

3.2.2.1 The PTT logic circuit supplies the +9.6T keying voltage to the transmitter and mutes the microphone audio during receive and unmutes the audio during transmit. The 9.6T keying voltage also switches the frequency synthesizer circuits to the transmit mode, mutes the receiver audio circuits, and lights the transmit indicator on the front panel to indicate that the radio set is transmitting.

3.2.2.2 The PTT logic circuit can be controlled from any of several sources:

- the microphone,
- the *DVP* circuits,
- the PL/DPL circuits,
- the time-out timer circuits (used as an option in carrier squelch models only),
- the vehicle ignition switch (with ignition control option B113 only),
- and external accessories connected at the rear of the radio, using J350 pins 1 through 7.

Mic audio transmissions are inhibited while a PTT is being generated by a *Select 5* signaling option or externally connected accessory. This prevents microphone noise from being inserted into the transmitter audio path when data (or optional *Select 5* signaling) transmissions are being made.

3.2.2.3 Pressing the push-to-talk button on the microphone supplies a mic PTT signal (via J350-14 in front-mount radios, or via P380-1 in remote mount radios), through jumper JU302, to mic mute control stage Q303. This enables Q303, which activates in turn, two signals. One signal is the mic mute enabling signal which is routed to mic audio mute gate Q325 in the transmit audio/IDC circuit. The gate allows microphone audio to be applied to the transmitter audio circuits. The second signal is the PTT enabling signal that tells the *DVP*, PL/DPL and time-out timer circuits that the radio is being keyed. The *DVP* board will then pull the delayed PTT line low. This is the signal which actually enables the +9.6T switches Q302 and Q307. When these switches are enabled, the +9.6T keying voltage is generated.

3.2.2.4 In radios having the ignition control option, jumper JU302 is cut and Q304 is added, allowing the vehicle switched ignition voltage to control the PTT logic circuit, via ignition control stage Q304. Ignition voltage is supplied to the radio via an additional (orange) wire.

3.2.3 Transmit Audio/IDC Circuit

3.2.3.1 The transmit audio/IDC circuit processes the microphone audio to ensure that the proper level of audio drive is supplied to the VCO hybrid in the frequency synthesizer circuits. When the radio is transmitting clear mode, the IDC audio directly modulates the VCO. In PL/DPL radios the low frequency PL/DPL encode (tone) signal from the PL/DPL circuits is combined with the microphone audio and is routed, via IDC deviation control and compensation circuits, to the VCO hybrid. A second modulation signal is routed to the 14.4 MHz reference oscillator in the frequency synthesizer to obtain low frequency transmit response. When the radio is transmitting in private mode, the IDC audio is routed to the *DVP* board, and converted to a digital signal which is then encrypted. This signal is splatter filtered and then modulates both the VCO and the 14.4 MHz reference oscillator.

3.2.3.2 Microphone audio is applied to mic mute gate Q325, via connector P350-12 in front mount radios, or via connector J380-4 in remote mount radios. The mic mute gate applies the audio to limiter U325A, via a pre-emphasis network. Transmit audio from options or accessories can also be injected into the input path of U325A, without pre-emphasis, via connectors J350-2 or P352-17. The output from U325A is applied to the input of splatter filter U325B. Inserted into this audio path is the PL/DPL VCO-modulation tone input from the PL/DPL circuits.

3.2.3.3 The output from the splatter filter is sent to the *DVP* board. If the radio is transmitting in clear mode, the audio is routed back to IDC mute gate Q326, which is open in the receive mode. The deviation level of the clear mode transmit audio is adjusted by VCO MOD potentiometer R341. The IDC audio then continues to the frequency synthesizer circuits to drive the VCO hybrid. If the radio is transmitting in private mode, the IDC audio is converted by U103 (on the *DVP* board) to a digital waveform. This digital waveform is then encrypted by HY101 and splatter filtered by U102. The deviation level of the transmitted *DVP* data is adjusted by potentiometer R158. From R158 the *DVP* data is sent back into the transmit path at IDC mute gate Q326, and from there on to the frequency synthesizer VCO hybrid. The VCO allows transmissions which carry information above 50 Hz.

3.2.3.4 Both *DVP* and DPL signals modulate the 14.4 MHz reference oscillator. The reference oscillator allows transmissions which carry information below 50 Hz. The level of the DPL modulation signal is adjusted by potentiometer R344 before being routed to the reference oscillator. The level of the *DVP* modulation signal is adjusted by potentiometer R159 on the *DVP* board. The *DVP* signal then gets routed to the reference oscillator.

3.2.4 Transmit Power and Level Control Circuit

3.2.4.1 The control circuit provides power leveling and protection for the final power amplifier circuits in the transmitter. The circuit acts as a control loop to protect the power amplifier against possible damage due to excessive temperature (in 30 watt models) or excessive reflected rf output power. If a possible excessive temperature condition should occur, or if the rf output power exceeds a preset level, or if excessive antenna mismatch is present, the circuit reduces the gain of the low level amplifier, hence the rf drive level to the final power amplifier. The circuit also disables the rf drive (by removing the LLA A+ source voltage) if the frequency synthesizer goes out-of-lock. Short circuit protection removes the LLA voltage if a short circuit occurs on the LLA A+ line.

3.2.4.2 The transmit power and level control circuit consists of transistors Q225, Q226, Q227, Q228, and differential amplifier U300B. The

temperature sensing signals supplied to the control circuit are the temperature compensation and heat sense monitoring signals. The temperature compensation monitoring signal is developed by negative-coefficient diode CR1451, mounted near the directional coupler. The heat sense signal is developed by a thermistor located in the 30 watt power amplifier only. The rf output power is monitored at the directional coupler. The directional coupler signal is a dc voltage that represents the weighted sum of the forward and reflected power. If any of these signals indicate a fault, the voltage variation on the directional coupler signal line is compared by differential amplifier U300B to a fixed dc reference. The amplifier then causes the control circuit to reduce the LLA A+ voltage, hence the rf output power, until the fault is stabilized. PWR ADJ potentiometer R245 presets the rf output level by setting a dc reference voltage for the differential amplifier. Voltage limit potentiometer R236 sets an upper limit on the LLA A+ voltage available to the LLA, to prevent damage to the 10 watt PA due to overdrive from the LLA.

3.2.5 Low Level Amplifier

The low level amplifier is a two-stage, non-linear amplifier that supplies the rf drive for the 10 watt power amplifier. The input to the low level amplifier is the 136 to 174 MHz transmit injection signal from the frequency synthesizer circuits. The signal is amplified by amplifiers Q200 and Q201 to produce the rf drive output. The gain of the amplifiers is controlled by the LLA A+ operating voltage supplied and regulated by the transmit power level and control circuit. By controlling the gain, hence the rf drive, the rf output power is maintained within prescribed limits.

3.2.6 10 Watt Power Amplifier

The 10 watt power amplifier consists of a single, non-linear stage Q250 that supplies the final rf output for low power transmitters. Operating power for the amplifier is the PA A+ voltage supplied by the power distribution circuits. The rf output from the power amplifier is applied to the input of the harmonic filter/antenna switch. In models using the 30 watt power amplifier, the rf output serves as the final rf drive for the high power amplifier.

3.2.7 30 Watt Power Amplifier

This power amplifier provides the final rf output for high power transmitters. The amplifier consists of a single, non-linear stage, Q1400. The PA A+ voltage is supplied by the power distribution circuits. Temperature protection is provided by a thermistor located near the amplifier. A temperature in excess of 120°C, monitored by the heat sense signal, causes the power level and control circuit to reduce the rf output power to bring the temperature within safe limits. The final rf output from the amplifier is applied to the harmonic filter/antenna switch.

3.2.8 Harmonic Filter/Antenna Switch

3.2.8.1 The harmonic filter/antenna switch attenuates harmonics of the assigned transmit frequency during transmit mode, and helps attenuate higher-frequency spurious responses of the receiver during receive mode. It also switches the antenna between the transmit signal path and receive signal path.

3.2.8.2 When the transmitter is in the transmit mode, the final rf output is routed through the transmit port of the antenna switch, the harmonic filter, and directional coupler to the antenna. In the receive mode, the receive rf from the antenna is directed through the directional coupler and harmonic filter to the receive port of the antenna switch. The receive rf is then routed to the front end of the receiver. The directional coupler signal monitors the forward versus reflected power allowing the transmit power level and control circuit to keep the rf output power level within the preset level.

3.3 STANDARD-LOCK FREQUENCY SYNTHESIZER CIRCUITS (Refer to Figure 4)

The frequency synthesizer circuits are functionally arranged into the channel selection and display circuits, the synthesizer board circuits, and the VCO hybrid circuits.

3.3.1 Channel Selection and Display Circuits

3.3.1.1 The channel selection and display circuits consist of the front panel channel selector switch and the channel display. The channel selector switch is located on the switch board and the channel display is located on the display board. The channel display consists of two, seven-segment LED displays. A dimmer/thermal control circuit on the display board automatically adjusts the LED's intensity to suit ambient light conditions. The circuit is powered by the SW A+ voltage supplied by the power distribution circuits. The SW A+ voltage is applied to the dimmer/thermal control circuit via diodes CR800 and CR801 on the switch board.

3.3.1.2 The channel selector switch encodes the selected channel in five binary bits and supplies the data on address lines A0 through A4 to frequency select PROM U117 on the synthesizer board. The five address lines are also fed to the PL/DPL circuits for encoding the information on the selected channel for transmisison. In selectable PL/DPL options only, the encoded address data for the PL/DPL circuits is generated by a selectable PL/DPL board. In this option, jumpers JU361 through JU365 on the front panel interconnect board are removed to disconnect the channel selctor switch from the PL/DPL circuits.

3.3.2 Synthesizer Board Circuits

The synthesizer board circuits include nine circuits: a 14.4 MHz reference oscillator, frequency select PROM U117, divider/phase detector U115, a PROM enable circuit, a lock detect switch circuit, a charge pump and loop filter circuit, a frequency shift logic circuit, the VCO buffers and transmit/receive injection switch, and a VCO AGC circuit.

3.3.2.1 14.4 MHz Reference Oscillator

The 14.4 MHz reference oscillator is a high-accuracy, temperature compensated crystal reference oscillator. The output of the reference oscillator is applied to divider/phase detector U115 to generate the reference frequency used to control the VCO frequency. The reference modulation signal from the transmitter circuits modulate the oscillator.

3.3.2.2 Frequency Select PROM, U117

3.3.2.2.1 Frequency select PROM (programmable read-only memory) U117 is a plug-in memory device that stores information regarding transmit and receive frequencies as well as filter selection for dual front end. Changes in any of the parameters can easily be affected by simply replacing the PROM with another factory-programmed PROM having the required information.

3.3.2.2.2 Addressing for the PROM is applied on address lines A0 through A4 by the channel selector switch, and by the +9.6T keying voltage from the transmitter circuits. When the +9.6T keying voltage is high, the data transferred out of the PROM contains transmit frequency information. The data is applied to divider/phase detector U115 via a four-bit data bus, D0 through D3. The data for each channel consists of six 4-bit words. The PROM only applies the data to U115 when a power enable voltage (+5 V dc) is applied to the PROM by the PROM enable circuit.

3.3.2.3 Divider/Phase Detector U115

3.3.2.3.1 Divider/phase detector U115 contains the negative feedback, phase-locked-loop circuitry that controls the VCO frequency. The divider/phase detector contains a reference divider, a loop divider, and a phase detector. The reference dividier divides down in frequency the 14.4 MHz reference oscillator signal and applies it as the reference frequency input to the phase detector. The loop divider divides down (in frequency) the negative feedback input, which is the buffered VCO rf signal originating at the VCO in the VCO hybrid. This signal is applied as the loop frequency input to the phase detector. The phase detector compares the phase difference between the two frequencies and generates error pulses on the $\overline{UP}$ and DOWN output lines that are proportional to any phase difference. (Phase is used as the controlling variable since small phase errors may exist in the locked-loop but frequency errors cannot.) The $\overline{UP}$ and DOWN error pulses are applied, via the charge pump and loop filter circuit, to the VCO steering line (which controls the VCO frequency) to complete the feedback loop.

3.3.2.3.2 The action of the negative feedback loop can be explained as follows. If the output frequency goes high, the loop frequency output also goes high, thus causing a leading phase displacement on the phase detector loop input. Since the reference signal phase does not change, the phase detector detects this condition and cause the generation of error pulses on the DOWN line. This is reflected on the VCO steering line to cause a reduction in frequency, thus compensating for the original frequency difference. The divider/phase detector also supplies a monitoring $\overline{LOCK}$ signal to the lock detect switch to indicate if the synthesizer frequency is, or is not, locked onto the correct frequency.

3.3.2.3.3 The divider/phase detector also supplies data outputs S1, $\overline{VCO1}$, and $\overline{VCO2}$ to the frequency shift logic circuit. These data lines are used to select the VCO band shift "window", which is the VCO sub-range frequency required by the selected operating frequency. The divider/phase detector also feeds a front end select signal to the optional widespaced dual front end in the receiver circuits. The front end select signal activates the correct frequency-range filter in the widespaced dual front end depending on the receive frequency of the selected channel.

3.3.2.4 PROM Enable Circuit

The PROM enable circuit and frequency change detector, consisting of ICs U116 and U351, allows divider/phase detector U115 to address the PROM. A pulse on the FC line from frequency change detector U351 on the front panel interconnect board causes the PROM to be addressed by U115. The PROM is addressed when any of the following occur.

- The transmitter is keyed (+9.6T at U351 causes FC pulse to occur).
- The frequency is changed (sensed by a change of state on any (A0-A4) address line applied to U351).
- The synthesizer goes out-of-lock (active lock detector output from lock detector switch circuit).

When one of these conditions occur, the PROM enable circuit applies an enable signal to U115, and U115 responds by returning a $\overline{STROBE}$ signal. The $\overline{STROBE}$ signal activates the PROM enable circuit, and the PROM enable circuit activates the PROM by applying +5 V dc operating power to its Vcc input. The PROM enable circuit also sends a synthesizer out-of-lock signal to the lock detect switch circuit. This ensures that the circuit develops an active lock detector output if

only the transmitter is keyed or if the frequency is changed.

3.3.2.5 Lock Detect Switch Circuit

The lock detect switch circuit consists of transistors Q154, Q155, Q156 on the synthesizer board and of U350 and Q350 on the Front Panel Interconnect Board (identified as lock detect delay). The circuit generates an active lock detector output signal that disables the receiver (in the receive mode) or the transmitter (in the transmit mode) if the synthesizer frequency goes out-of-lock. The circuit disables the receiver (or transmitter) when an un-lock condition is sensed by divider/phase detector U115, or if the un-lock condition is forced by the PROM enable circuit.

3.3.2.6 Charge Pump and Loop Filter Circuit

The charge pump and loop filter circuit consists of transistors Q150, Q152, and Q153 and an associated filter network. The circuit changes the $\overline{\text{UP}}$ or DOWN error pulses from divider/phase detector U115 to a corresponding dc voltage. The dc voltage is then filtered to become the VCO steering line voltage used to control the frequency of the VCO. As part of the negative feedback phase-locked-loop, the charge pump and loop filter circuit control the closed-loop response and removes noise from the divider/phase detector output.

3.3.2.7 Frequency Shift Logic Circuit

The frequency shift logic circuit consists of transistors Q171 and Q172, and IC U171. The circuit controls the switching of the VCO to the sub-range frequencies at which it operates for a selected channel. These sub-range frequencies, or band shift "windows", are encoded in the PROM, read-out to divider/phase detector U115, applied from U115 on the $\overline{\text{S1}}$, $\overline{\text{VCO1}}$, and $\overline{\text{VCO2}}$ data lines, and are applied to the frequency shift logic circuit. The circuit then supplies six outputs to PIN (diode) switches in the VCO hybrid. Depending on the logic states of the six outputs (S1 and $\overline{\text{S1}}$; S2 and $\overline{\text{S2}}$; and S3 and $\overline{\text{S3}}$), the PIN diodes switch the VCO to the correct sub-range frequency.

3.3.2.8 VCO Buffers and Transmit/Receive Injection Switch

The VCO buffers consist of transistors Q190 and Q192. The transmit/receive switch consists of transistor Q191. The buffers receive the VCO rf feedback signal from the VCO. The buffered signal is applied to the loop divider in divider/phase detector U115 to generate the loop frequency used to control the VCO frequency. The buffers also feed the VCO rf feedback signal to either the transmit or receive injection ports on the synthesizer interconnect board. Transmission along either port is controlled by the +9.6T keying voltage applied to the transmit/receive injection switch. A high +9.6T keying voltage (transmit mode) causes the injection switch to forward bias diode CR190, routing the VCO rf to the transmit injection port at connector P344-1. From the port, the signal is fed, via a coaxial cable, to the low level amplifier in the transmitter. A low +9.6T keying voltage (receive mode) forward biases diode CR191, thus routing the VCO rf to the receive injection port at connector J357. From the port, the signal is fed as the receiver injection signal to the mixer in the receiver.

3.3.2.9 VCO AGC Circuit

The VCO AGC circuit consists of transistors Q188 and Q189. The circuit stabilizes the VCO gain by maintaining a constant rf level in the VCO tank circuit. A dc sample of the VCO rf output is applied to the VCO AGC circuit as the AGC detect signal. If the signal varies, the circuit feeds an AGC control signal back to the VCO tank circuit to maintain a constant VCO rf output.

3.4 *FAST-LOK* FREQUENCY SYNTHESIZER CIRCUITS (Refer to Figure 5.)

The frequency synthesizer circuits are functionally arranged into the channel selection and display circuits, the synthesizer board circuits, the VCO hybrid circuits and the synthesizer rf amplifier circuit.

3.4.1 Channel Selection and Display Circuits

The channel selection and display circuits used with the *Fast-Lok* synthesizer are the same as the circuits used with the standard lock synthesizer. Refer to the channel selection and display circuits paragraphs in the standard lock frequency synthesizer section.

3.4.2 Synthesizer Board Circuits

The synthesizer board circuits include eight circuits; a 14.4 MHz reference oscillator, frequency select PROM U116, divider U115, phase detector U140, an adaptive loop filter, a PROM enable circuit, a frequency shift logic circuit, and a VCO AGC circuit.

3.4.2.1 14.4 MHz Reference Oscillator

The 14.4 MHz reference oscillator U101 is a 2 ppm, temperature-compensated crystal oscillator. The output of the reference oscillator is applied to divider U115 to generate the reference frequency used to control the VCO frequency. The reference modulation signal from the transmitter circuits modulates the oscillator.

3.4.2.2 Frequency Select PROM, U116

3.4.2.2.1 Frequency select PROM (programmable read-only memory) U116 is a plug-in memory device that stores information regarding

transmit and receive frequencies as well as filter selection for optional dual front end. Changes in any of the parameters can easily be affected by simply replacing the PROM with another factory-programmed PROM having the required information.

3.4.2.2.2 Addressing for the PROM is applied on address lines A0 through A4 by the channel selector switch, and by the 9.6T keying voltage from the transmitter circuits. When the 9.6T keying voltage is high, the data transferred out of the PROM contains transmit frequency information. The data is applied to divider/phase detector U115 via a four-bit data bus, D0 through D3. The data for each channel consists of six 4-bit words. The PROM only applies the data to U115 when a power enable voltage (+5 V dc) is applied to the PROM by the PROM enable circuit.

3.4.2.3 PROM Enable/Frequency Change Detector

The PROM enable circuit and frequency change detector, consisting of U116, U351, Q115, Q117 and Q118 allow divider U115 to address the PROM. A pulse on the FC line from frequency change detector U351 on the front panel interconnect board causes the PROM to be addressed by U115. The PROM is addressed when any of the following occur.

- The transmitter is keyed (+9.6T at U351 causes FC pulse to occur)
- The frequency is changed (sensed by a change of state on any (A0-A4) address line applied to U351).
- The synthesizer goes out-of-lock (sensed by phase detector U140 internal lock detect circuit).

When one of these conditions occur, phase detector ADAPT output U140-10 goes high. This applies an $\overline{\text{ENABLE}}$ signal to U115-28 via Q117, and U115 responds by returning a $\overline{\text{STROBE}}$ signal. The $\overline{\text{STROBE}}$ signal activates the PROM enable circuit, and the PROM enable circuit activates the PROM by applying +5 V dc operating power to its Vcc input.

3.4.2.4 Divider U115

3.4.2.4.1 The divider circuit contains two programmable dividers and control circuitry. The reference divider acts upon the 14.4 MHz reference oscillator input. This divider is set by the PROM input data to divide the input frequency down to a reference frequency of 4.167 kHz, 5.00 kHz, or 6.25 kHz. The loop divider is set by the PROM input data to divide the desired VCO feedback frequency down to the reference frequency. The loop (divided VCO) signal and the reference signal are then coupled to the phase detector circuit.

3.4.2.4.2 The divider also supplies data outputs $\overline{\text{SO}}$, $\overline{\text{VCO1}}$, and $\overline{\text{VCO2}}$ to the frequency shift logic circuit. The $\overline{\text{SO}}$ output is routed through a synchronizing "D" flip-flop on phase detector U140. These data lines are used to select the VCO band shift "window", which is the VCO sub-range frequency required by the selected operating frequency. The divider also feeds a front end select signal ($\overline{\text{S1}}$) to the optional widespaced dual front end in the receiver circuits. The front end select signal activates the correct frequency-range filter in the widespaced dual front end depending on the receive frequency of the selected channel.

3.4.2.5 Phase Detector U140

3.4.2.5.1 Phase detector U140 compares the reference and loop frequency outputs of the divider circuit and uses this information to generate a dc control signal that is coupled through the adaptive loop filter to tune the VCO.

3.4.2.5.2 The phase detector also monitors the status of the frequency change (FC) line (P353-8) and uses this information to generate the control signal for the adaptive loop filter. A "D" flip-flop (U140-11, 6) synchronizes the divider $\overline{\text{SO}}$ output to the rising edge of the loop (divided VCO) pulse.

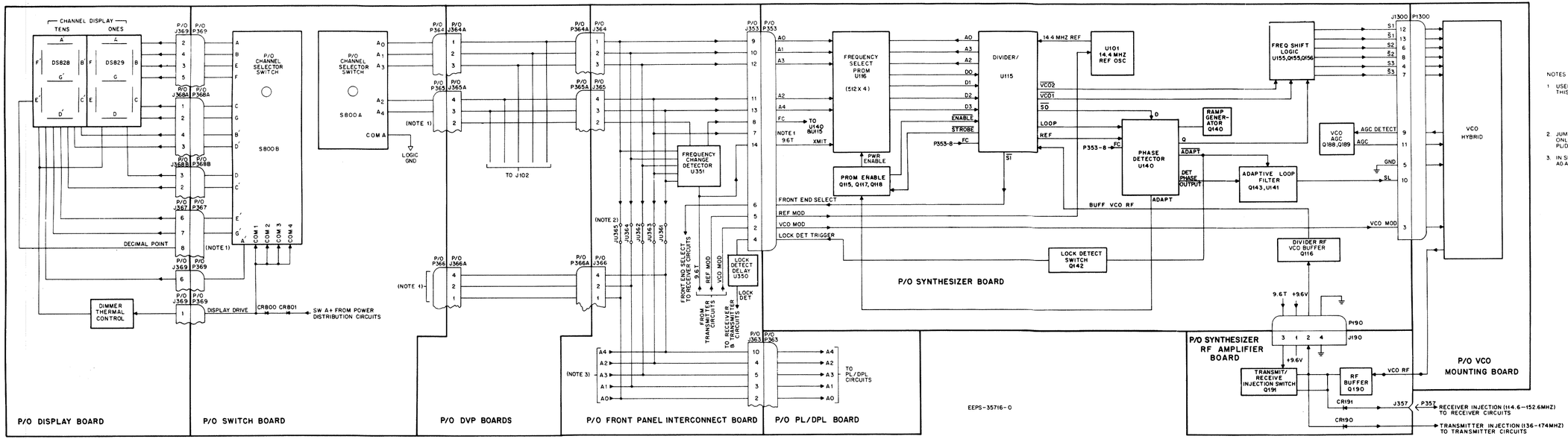
3.4.2.6 Adaptive Loop Filter

3.4.2.6.1 The adaptive loop filter is a low-pass filter in the steering line between the phase detector and the VCO. This filter removes noise and variations in the steering line level to prevent unwanted modulation of the VCO.

3.4.2.6.2 The adaptive loop filter, which is connected to the phase detector output line (U140-15), is controlled by the phase detector to operate in either of two modes, either the Adapt or the Receive/Transmit mode is selected depending upon the state of the synthesizer at a given time. The Receive/Transmit mode is selected for transmitting and receiving while the Adapt mode is entered during any period when the synthesizer changes frequency.

3.4.2.7 Frequency Shift Logic Circuit

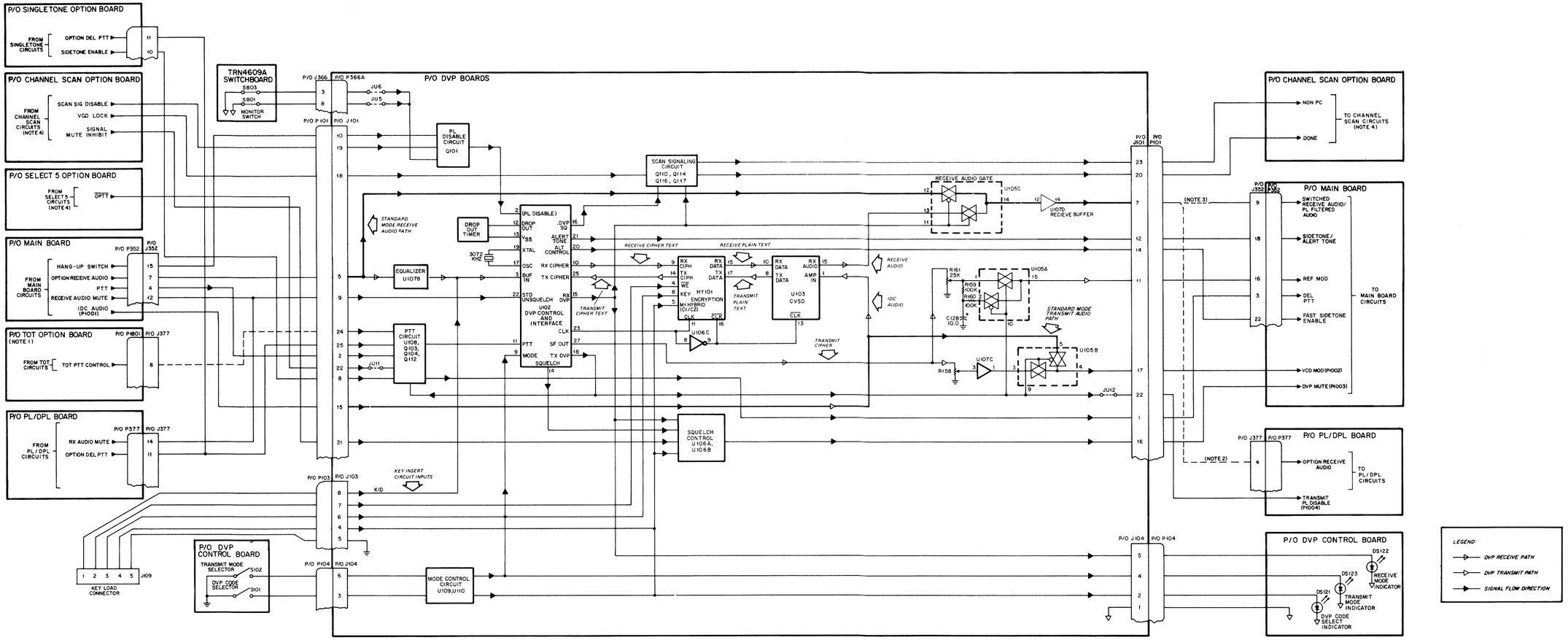
The frequency shift logic circuit consists of transistors Q155 and Q156, and IC U155. The circuit controls the switching of the VCO to the sub-range frequencies at which it operates for a selected channel. These sub-range frequencies, or band shift "windows", are encoded in the PROM, read-out to divider U115, applied from U115 on the $\overline{\text{SO}}$, (via U140) $\overline{\text{VCO1}}$, and $\overline{\text{VCO2}}$ data lines, and are applied to the frequency shift logic circuit. The circuit then supplies six outputs to PIN (diode) switches in the VCO hybrid. Depending on the logic states of the six outputs (S1 and $\overline{\text{S1}}$; S2 and



NOTES

1. USED WITH OPTIONS AND CONFIGURATIONS NOT COVERED ON THIS DIAGRAM.
2. JUMPER JU361 USED FOR 32-CHANNEL MULTI-PL/DPL MODELS ONLY. JUMPERS JU361-JU365 ARE REMOVED IN SELECTABLE PL/DPL OPTION ONLY.
3. IN SELECTABLE PL/DPL OPTION ONLY, CHANNEL SELECT ADDRESS A0-A4 INITIATED BY SELECTABLE PL/DPL BOARD.

Figure 5. Fast-Lok Synthesizer Functional Block Diagram



NOTES:

1. Time-out timer board is optional in carrier squelch models only.
2. Connection for PL/DPL radios.
3. Connection for non PL/DPL radios.
4. Option not covered in this manual.

Figure 6. Digital Voice Protection Circuits Functional Block Diagram

$\overline{S2}$; and S3 and $\overline{S3}$), the PIN diodes switch the VCO to the correct sub-range frequency.

3.4.2.8 VCO AGC Circuit

The VCO AGC circuit consists of transistors Q170, Q171 and Q1300. The circuit stabilizes the VCO gain by maintaining a constant rf level in the VCO tank circuit. A dc sample of the VCO rf output is applied to the VCO AGC circuit as the AGC DETECT signal. If the signal varies, the circuit feeds an AGC control signal back to the VCO tank circuit to maintain a constant VCO rf output.

3.4.3 Synthesizer RF Amplifier Board

RF buffer Q190 raises the VCO rf output level, feeding the transmit/receive injection switch as well as providing the VCO frequency feedback signal to divider U115 via buffer transistor Q116 on the synthesizer board. The transmit/receive injection switch consists of PIN diodes CR190 and CR191 and transmit/receive injection switch Q191. Transmission along either port is controlled by the 9.6T keying voltage applied to Q191. A high 9.6T keying voltage (transmit mode) forward biases CR191, routing the VCO rf to the transmit injection port at connector P374-1. From the port, the signal is fed, via a coaxial cable, to the low level amplifier in the transmiter. A low 9.6T keying voltage (receive mode) turns on transistor Q191, forward biasing CR190, routing the VCO rf to the receive injection port at connector J357. From the port, the signal is fed as the receiver injection signal to the mixer in the receiver.

3.4.4 Voltage Controlled Oscillator

The voltage controlled oscillator (VCO) used with the *Fast-Lok* synthesizer is the same as the VCO utilized with the standard lock synthesizer with the addition of a feedthrough capacitor/filter wall. Refer to the VCO description paragraphs in the standard lock synthesizer section for operation information.

3.5 *DVP* CIRCUITS
(Refer to Figure 6.)

The *DVP* circuitry is contained on two boards located within the radio housing just behind the front panel circuitry. The boards use CMOS integrated circuits to perform the audio switching and control functions which are necessary to control the *MCX100* radio. A 5-pin connector at the side of the radio allows loading an electronic encryption key into the *DVP* circuitry. Switches and indicators necessary to control the *DVP* circuitry are conveniently located on the radio front panel.

3.5.1 *DVP* Definitions

The following is a definition of some of the terminology used in explaining *DVP* operation and circuitry.

- ALERT TONE is sounded at the speaker when the operator transmits in the standard mode. The tone alerts the operator that the transmission is not encrypted. The alert consists of a 750 Hz tone for about 80 milliseconds.
- CIPHER TEXT refers to the digital waveform which represents the encrypted audio.
- CODE is the word sometimes used in place of the correct term which is key (see key).
- CODE INSERTER is an electronic device used to load an electronic encryption key into *DVP* equipped radios.
- CROSSOVER JITTER is the ratio of crossover time (X) to whole bit time (T). See Figure 7. For example, with X equal to 0.55cm and T equal to 3.5cm, the crossover jitter is 15.7%.

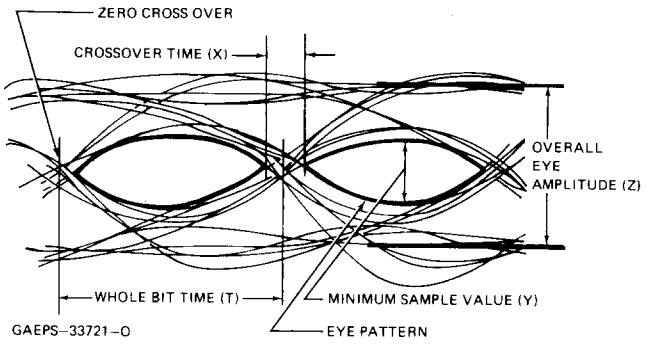


Figure 7. Cipher Text Waveform

- DECRYPTION converts cipher text to plain text.
- DUAL CODE is a second key capability. The key is stored in the Code 1 position. The Code 2 position electronically alters the stored key. An operator control selects either Code 1 or Code 2.
- ENCRYPTED VOICE COMMUNICATION is called private mode, secure mode, cipher, or cipher text depending on the context in which the term is used. In this mode, the audio signal is converted to a digital signal and encrypted before transmission. At the receiver, the receiver signal is decrypted, and the resulting digital signal is used to reconstruct the audio waveform.
- ENCRYPTION converts plain text to cipher text.
- END-OF-MESSAGE (EOM) signal is a short burst of 6 kHz sine wave transmitted at the end of a private mode message by a *DVP* radio. EOM lasts for the interval usually used for the PL reverse burst signal which is about 180 milliseconds. The EOM signal functions as a squelch closure.

- EYE OPENING is the ratio of the minimum sample value to the overall eye amplitude expressed as a percentage. See Figure 7. For example, with Y equal to 1.0cm and Z equal to 2.5cm, the eye opening is 40.0%.

- EYE PATTERN is transmit cipher text converted by the splatter filter. See Figure 7. The term eye pattern is used because the oscilloscope trace vaguely resembles the shape of the human eye.

- KEY consists of a sequence of bits that are electronically stored in the encryption module. The key is transferred to the module through the 5-pin connector on the side of the radio. The key is sometimes referred to as the electronic key to distinguish it from a physical key such as a car key. The key is sometimes casually referred to as a code.

- PLAIN TEXT refers to the digital waveform which represents the non-encrypted audio.

- QUALITY OF RECEIVED SIGNAL is expressed by an error rate or probability of error. This number expresses the probability that any bit that is recovered by the receiver is in error. The error rate measures the quality of a private mode signal in much the same way that quieting or SINAD measure the quality of a standard mode signal. For *DVP* radios the error rate is usually measured for plain text rather than cipher text since it is easier to measure. For plain text messages to be intelligible in the *DVP MCX100*, the error rate should be less than 5%.

- SPLATTER FILTER converts the transmit cipher text signal to an eye pattern signal.

- STANDARD VOICE COMMUNICATION is called standard mode, clear mode, bypass mode, or plain text depending on the context in which the term is used. In this mode of operation, the audio signal is transmitted exactly like an FM two-way radio normally transmits an audio signal.

- TURN-OFF-CODE (TOC) is the term sometimes used instead of end-of-message (EOM).

- ZERO CROSSOVER corresponds to the transition point between bits. See Figure 7.

3.5.2 *DVP* Signal Routing

3.5.2.1 The *DVP* circuitry controls both the receive and transmit portions of the *DVP MCX100* radio. When the radio is receiving, the *DVP* circuitry checks the signal. If the signal is coded, decrypted audio is routed to the radio speaker. If the signal is not coded, discriminator audio is routed to the radio speaker. When the radio is transmitting, the *DVP* circuitry will route either IDC audio or *DVP* cipher to the radio modulating circuitry, depending upon the front panel mode setting.

3.5.2.2 Buffered discriminator output is routed to the *DVP* circuitry for code detection and audio reconstruction. It first goes through an equalizer and is then applied to U102. If the signal is *DVP* code, U102 reclocks the signal to recover the cipher text. The cipher text then goes to the encryption hybrid where it is decrypted to produce the plain text. The plain text is then routed to the CVSD, where the audio is reconstructed. U102 will then switch U105C so that decrypted audio is routed back into the radio low level audio path. If the incoming signal is not *DVP* code, U102 does not switch U105C and the buffered discriminator signal is routed back into the low level audio path.

3.5.2.3 IDC audio is routed to the *DVP* circuitry to be digitized by the CVSD. The output of the CVSD (the plain text) goes to the encryption hybrid. The hybrid encrypts the plain text to produce cipher text. From the hybrid, the cipher text passes through a splatter filter on U102 and then goes to the deviation adjustment potentiometers, R158 and R161. The *DVP* signal then goes to analog switches U105A and U105B. If the radio is set for coded transmission, and the *DVP* circuitry has received an active PTT signal, U105A and U105B will be switched so that the *DVP* signal is passed back into the radio transmit circuitry. If the radio is set for clear transmission, the IDC audio will be passed back into the radio transmit circuitry by U105A.

3.6 PL/DPL CIRCUITS
(Refer to Figure 8)

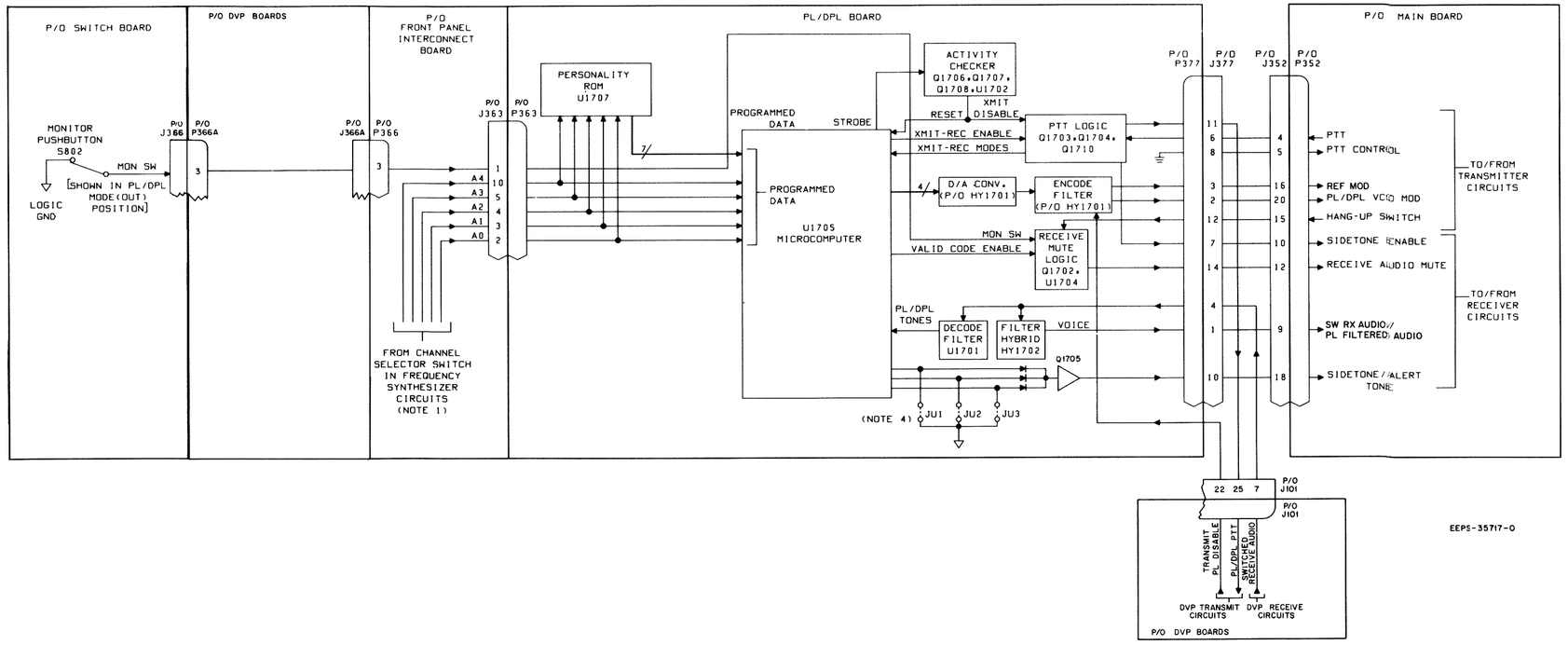
3.6.1 Squelch Code Systems

3.6.1.1 The PL/DPL (*Private-Line/Digital Private-Line*) circuits greatly improve the privacy of communications for a number of private users that may be sharing an rf channel. The circuits encode (transmit) and decode (receive) PL (tone coded) and DPL (binary-coded) squelch signals to unsquelch compatably-equipped radios. The use of a personality ROM (read only memory), allows PL and DPL signaling tones to be mixed (transmit in one code scheme and receive in another on the same channel).

3.6.1.2 The PL/DPL coded squelch circuits unsquelch the receiver upon receipt of a properly coded signal. In the PL mode, a sub-audible tone frequency is detected, whereas in the DPL circuits, a 23-bit binary code word is detected. In either case, the code is transmitted continuously during the transmit mode, to unsquelch the receiver. Other receivers operating on the same rf channel but not compatable with the code signal remain squelched. In both systems, the code signal frequency is below the 300 to 3000 Hz audio band and is therefore not heard in the speaker.

3.6.2 Microcomputer and Memory

3.6.2.1 An 8-bit, 40-pin microcomputer and a personality ROM control the PL/DPL decoding



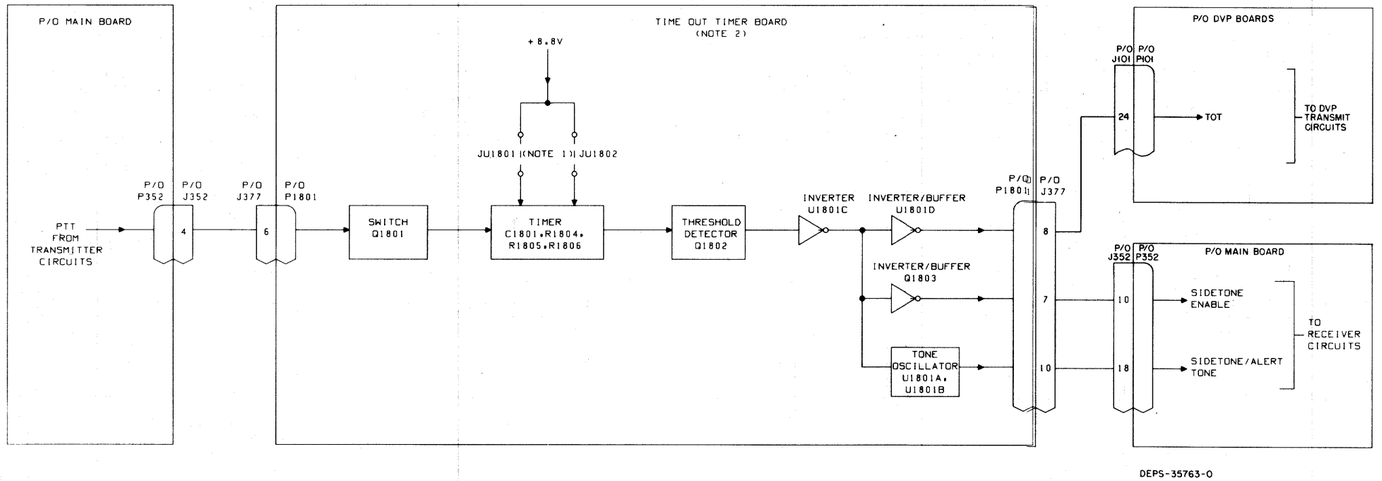
NOTES:

1. IN SELECTABLE PL/DPL OPTION ONLY, ADDRESS A0-A4 INITIATED BY SELECTABLE PL/DPL BOARD INSTEAD OF CHANNEL SELECTOR SWITCH.

2. JUMPERS JU1, JU2, & JU3 DETERMINE TIME-OUT TIME, AS FOLLOWS:

JUMPERS			TIME-OUT
JU1	JU2	JU3	TIME
IN	OUT	OUT	15 SEC
OUT	OUT	OUT	30 SEC
OUT	IN	OUT	60 SEC
IN	IN	OUT	90 SEC
OUT	OUT	IN	2-1/2 MIN
IN	OUT	IN	5 MIN
OUT	IN	IN	NONE

Figure 8. PL/DPL Circuits, Functional Diagram



DEPS-35763-O

NOTES:

1. JUMPERS JU1801 AND JU1802 DETERMINE TIME-OUT TIME, AS FOLLOWS:

JUMPER		TIME-OUT
JU1801	JU1802	TIME (SEC)
IN	IN	15
OUT	IN	30
OUT	OUT	60

2. TIME-OUT TIMER BOARD IS OPTIONAL IN CARRIER-SQUELCH MODELS ONLY.

Figure 9. Time-Out Timer Circuits, Functional Diagram

and encoding functions. The personality ROM is factory-programmed with user-specified operating parameters. For single and multi-code operation, changing codes is accomplished by removing the personality ROM and inserting another ROM.

3.6.2.2 The microcomputer accesses the personality ROM whenever it requires information to control its operation. Software programming within the microcomputer then directs the decoding and encoding processes. In multiple PL/DPL squelch models, channel selection data is applied to the personality ROM on five address lines (A0-A4) encoded by the channel select switch on the front panel. In selectable PL/DPL squelch models only, the five address lines are encoded by a selectable PL/DPL board.

3.6.3 Decoding

3.6.3.1 An inactive PTT signal from the microphone initiates the decode process. The inactive signal causes PTT logic circuit Q1703 to set the microcomputer to the receive mode. The option receive audio from the receiver circuits is applied to the microcomputer, via low pass decode filter U1701. This allows only the PL or DPL tones (or codes) to be applied to the microcomputer for decoding. The PL or DPL tones (or codes) are removed from the optional receive audio by high pass filter hybrid HY1702. The filtered output, containing voice only, is the PL filtered audio that is inserted into the receiver low level audio stages.

3.6.3.2 When the microcomputer is set to the receive mode, and a valid PL or DPL code is decoded, the microcomputer enables receive mute logic circuit Q1702 and U1704. The circuit then supplies an active low receive audio mute signal to the receiver circuits to unmute the audio. The decoder circuits can be bypassed to allow all signals on the channel to be monitored. This permits a check of a selected channel to see if it is in use before transmitting. Pushing in the Monitor pushbutton on the front panel disables the PL/DPL decoder circuits. This allows the receiver carrier squelch circuit to control the receiver audio. Leaving the microphone off-hook performs the same function, via the hang-up switch signal applied to the receive mute logic circuit.

3.6.4 Encoding

3.6.4.1 An active microphone PTT signal applied to the PTT logic circuit activates the encoding process. The circuit applies a signal to the microcomputer, setting it to the transmit mode. The microcomputer responds by applying a delayed PTT signal to the *DVP* PTT logic circuits on the *DVP* board, keying the transmitter. When microphone PTT is released, the delayed PTT signal remains low for a preprogrammed time interval, during which the "reverse-burst" or turn-off code is transmitted. At the end of this interval, the transmitter dekeys.

3.6.4.2 During encoding, the microcomputer begins timing the duration of the transmission, and times out (dekeys the transmitter automatically) at the end of a user-specified interval. Up to seven time-out intervals can be selected for the time-out-timer, depending on the inclusion or exclusion of jumpers JU1, JU2, and JU3 in the circuit. When time-out occurs, the sidetone enable signal is activated, and the sidetone/alert tone is heard in the speaker.

3.6.4.3 The microcomputer applies PL or DPL signaling information on four digital data lines. For PL tone transmission, the digital data is converted to an analog signal by a D/A (digital-to-analog) converter in hybrid HY1701. The PL/DPL signal is filtered by a low-pass encode filter, also part of hybrid HY1701. The PL or DPL signal produced is then applied to the transmitter audio/IDC curcuits and also to the reference oscillator/IDC circuit. The levels at these two points are controlled by potentiometers.

3.6.5 Activity Checker

This circuit resets the microcomputer if a microcomputer fault occurs. During normal operation, the microcomputer applies strobe pulses to activity checker Q1707 and U1702. If strobe pulses are not generated for 15 milliseconds, indicating a microcomputer fault, the activity checker generates a reset pulse to reset the microcomputer. The reset pulse is also applied to the PTT logic circuit to unkey the transmitter during the microcomputer fault. The reset pulse is disabled when the microcomputer is again operating properly.

3.7 TIME-OUT TIMER CIRCUITS
(Refer to Figure 9)

3.7.1 The time-out timer circuit is used as an option in carrier-squelch models. The circuit dekeys the transmitter after a predetermined period of time and allows the sidetone/alert tone signal to be heard in the speaker. The time-out timer circuit consists essentially of a 33 Hz clock generator, a 775 Hz tone oscillator, and a counter to count the clock pulses.

3.7.2 The time-out timer circuits produce three output signals: the TOT control signal that unkeys the transmitter; the sidetone enable signal that unmutes the receiver audio; and the sidetone/alert tone signal that is inserted into the receiver audio line when the receiver is unmuted. The circuits are controlled by the PTT signal generated by PTT logic in the transmitter circuits.

3.7.3 When the transmitter is not being keyed, the PTT signal is high and the time-out timer circuits are in the reset condition. In this state, the outputs from the circuits allow the transmitter to be keyed while preventing the sidetone/alert tone from being heard in the speaker. As soon as the transmitter is keyed, the PTT signal goes low, taking the counter (U1802) out of

reset. U1802 then counts the clock pulses generated by U1801C. When the selected output of U1802 goes high, the clock oscillator (U1801C and U1801D) is inhibited and stops clocking the counter. The high output of the counter enables the 775 Hz tone oscillator, causing the tone to be inserted into the receiver sidetone path. The output high of the counter also drives the sidetone enable buffer (Q1803), and the TOT PTT control buffer (Q1802). Q1803 pulls the sidetone enable signal low, allowing the 775 Hz tone to be heard in the speaker, and Q1802 applies a low TOT PTT control signal to the *DVP* PTT circuitry, causing the radio to stop transmitting.

3.7.4 The time-out timer circuits remain in this state until the PTT signal goes high again (microphone dekeyed). This resets the counter, causing its output to go low again. This enables the clock generator, disables the tone oscillator and the transistor drivers, and allows the transmitter to be keyed again.

3.8 REMOTE MOUNT CIRCUITS (Refer to Figure 10.)

3.8.1 Functions

3.8.1.1 Most of the control head functions in the remote mount models operate in the same manner as the front panel functions do in front mount models. The only difference is that these functions are performed through a 36-conductor interconnect cable. The following functions operate identically in both front mount and remote mount radios.

- *DVP* control
- Channel select lines
- Monitor, or Secondary Call/External Alarm pushbutton
- Call Pushbutton
- Call light indicator
- 10/100 Call or Selectable PL/DPL Code Select pushbuttons
- *Select 5* signaling thumbwheel switches.

3.8.1.2 The following functions operate differently in remote mount models.

- Power on-off
- Monitor pushbutton
- Busy light indicator
- Transmit indicator
- PTT (when used with control head microphone)
- Volume

The above functions require processing by the remote interface board for operation. Refer to Figure 8. Three wires in the interconnect cable (marked A, B, and C) perform multiple functions. The functions they perform are determined by the dc voltage level on the lines.

3.8.1.3 Lines A and C use comparators on the interface board to decode the function to be performed. Comparators on the interface board are biased such that the voltage on the line determines if the comparator output is in the high state (approximately 11.5 V dc) or low state (approximately 1.4 V dc).

3.8.1.4 Line B sources current (transmit mode) to the control head or sinks current (busy mode) from the control head, depending on the state of the 9.6 T line and busy line from the radio.

Line	Functions
A	Power On-off/Squelch
B	Transmit/Busy Indicators
C	PTT/Microphone Audio

3.8.2 Power On-Off/Squelch

3.8.2.1 Refer to the remote mount functional diagram and function chart (Figure 8). When the control head on-off switch (part of Off-on/Volume control) is closed, 4.8 V is present on line A which activates the on-off comparator, Q2201 and Q2203, on the remote interface board. The output of the comparator drives Q2202 into saturation, turning on the radio. Note that the + BATT return for the control head is provided through the ground wire in the 36-conductor interconnect cable. If this cable is not connected to the transceiver, the contol head is inactive.

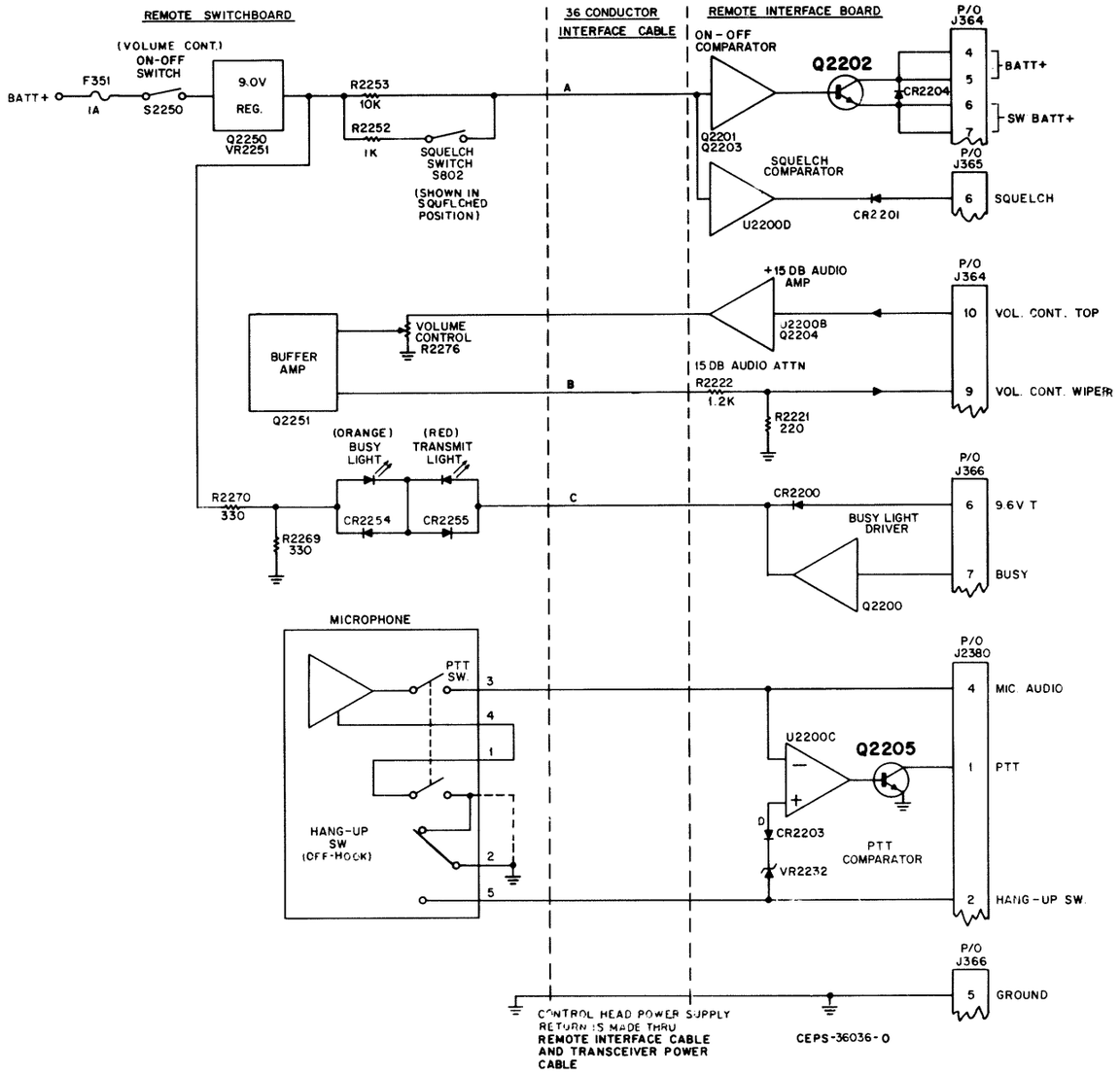
3.8.2.2 With the Squelch push button out (radio squelched) the output of the squelch comparator, U2200D, is high. Pushing the squelch button in (radio unsquelched) raises the voltage on line A to 8.3 V dc and causes the output of U2200D to go low. The on-off comparator is not effected by the Squelch pushbutton.

3.8.3 Busy/Transmit Indicators

In the transmit mode, 9.6 T is applied to line B through CR2200 on the remote interface board. This causes the Transmit LED in the control head to become forward biased (ON) and the Busy indicator reverse biased (OFF). In the busy mode, line B is pulled low by Q2200, causing the Busy indicator LED to become forward biased and the Transmit indicator LED reverse biased. When the radio is not in the transmit mode, or the channel is not busy, both diodes are off, CR2200 is reverse biased and Q2200 is in cutoff, preventing current from flowing through the LEDs. Both the Transmit and Busy indicator LEDs cannot be on at the same time.

3.8.4 PTT/Microphone Audio

3.8.4.1 The microphone in the control head controls the PTT line via the PTT comparator,



REMOTE FUNCTIONAL CHART

	SIGNAL LEVEL	FUNCTION
A	4.8V POWER ON, SQUELCHED 8.3V POWER ON, UNSQUELCHED 0V POWER OFF	ON-OFF/SQUELCH
B	8.3V TRANSMIT LED ON 0.6V BUSY LED ON 3.0V BOTH LED'S OFF	BUSY/TRANSMIT INDICATORS
C	9.6V PTT LINE HIGH (REC.) 5.75V PTT LINE LOW (XMIT)	PTT/MIC AUDIO
D	7.1V MIC OFF HOOK 3.0V MIC ON HOOK	HANG-UP

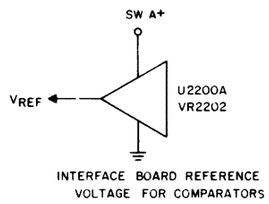


Figure 10. Remote Mount Circuits Functional Diagram

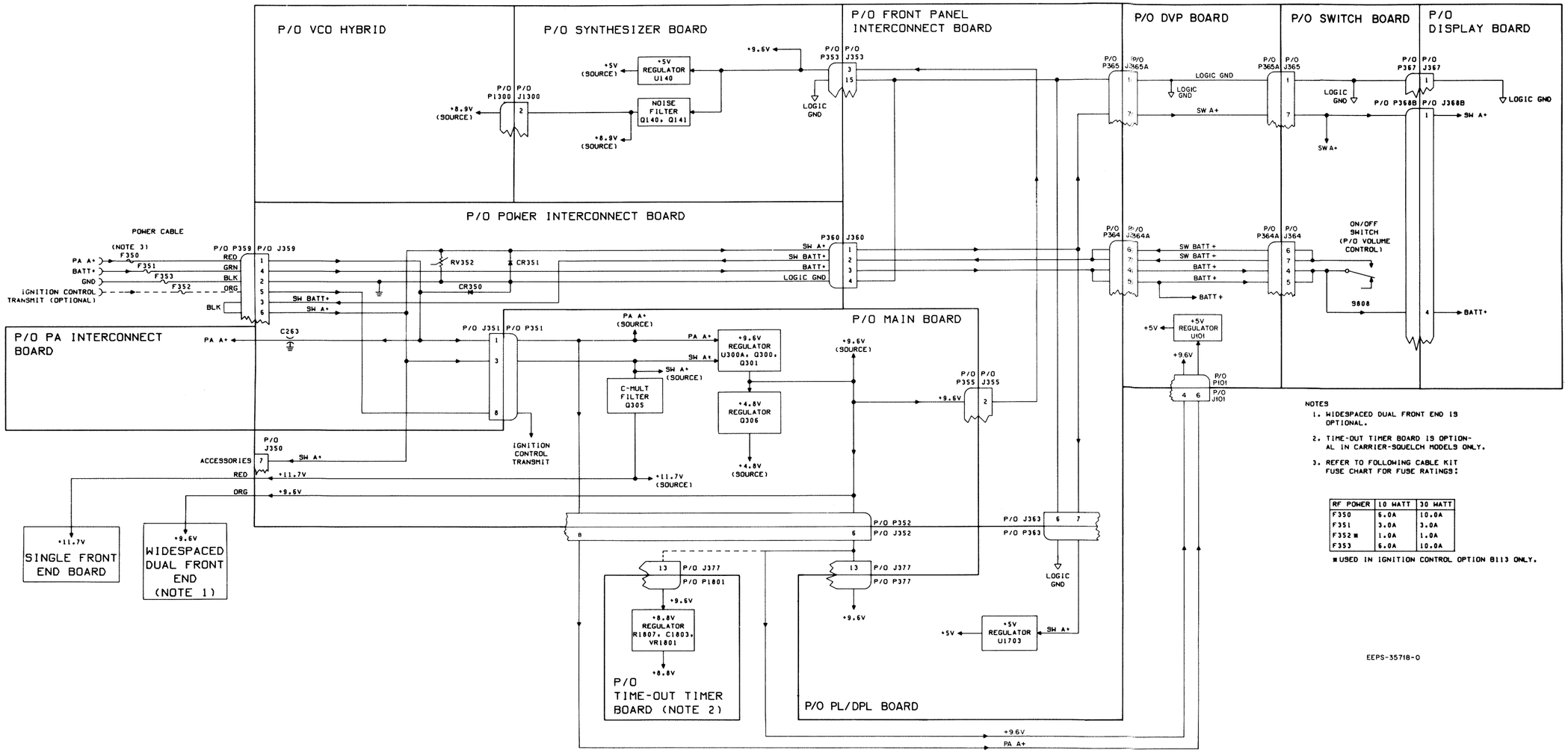


Figure 11. Power Distribution Circuits Functional Diagram

U2200C, and Q2205 on the remote interface board. The PTT comparator senses the dc voltage on line C in the functional diagram. If the microphone is off-hook and the PTT switch is pressed, the voltage on line C drops from 9.6 V to 5.8 V causing the output of U2200C to go high, saturating Q2205. Q2205 pulls the PTT line low which keys the transmitter. While transmitting, line C also carries the microphone audio to the radio IDC circuitry.

3.8.4.2 If the control head has a signaling microphone and is on-hook, the microphone ground is broken by the hang-up switch, prventing line C from dropping in voltage when the microphone PTT switch is pressed. The output of U2200C remains low, preventing the transmitter from keying up.

3.8.4.3 The diode network on the non-inverting input of U2200C permits a signaling microphone to be connected at the radio instead of at the control head. With a signaling microphone connected at the radio, the voltage on line C goes low (5.8 V) when the microphone PTT switch is pressed, regardless of if the microphone is on-hook or off-hook. To prevent the transmitter from keying on-hook, the non-inverting input of U2200C is pulled low (lower than the inverting input) through CR2203, VR2232 and the hang up switch. The output of U2200C remains low, preventing the transmitter from keying.

3.8.5 Volume Control

To minimize noise pick-up in the interconnect cable, the receiver audio is amplified 15 dB and buffered by U2200B and Q2204 on the interface board before being applied to the volume control in the control head. The volume control applies the audio signal to an emitter follower, Q2251, which returns the signal to a 15 dB attenuator on the interface board.

3.9 POWER DISTRIBUTION CIRCUITS (Refer to Figure 11.)

3.9.1 General

3.9.1.1 The power distribution circuits supply the necessary dc power to the boards that make up the *DVP MCX100* radio set. Regulators and filters on various boards are provided to supply regulated and filtered voltages, where necessary.

3.9.1.2 Primary input power from the vehicle in the form of BATT+ (green wire), PA A+ (red wire), and ground (black wire) is applied to connector J359. The wires are in a power input cable; J359 is on the power interconnect board. Ignition control option B113 uses a fourth wire (orange) for "ignition control of transmit". Each wire is fused. Refer to the Installation section of this manual for power lead connections.

3.9.1.3 The BATT+ voltage is routed through the power interconnect board and front panel interconnect board to the front panel power on/off switch. The BATT+ voltage is also routed through the switch board to the display board to provide power to multiple-code memory circuits. When the power switch is set to the on position, the BATT+ voltage is applied to the SW BATT+ line. This voltage is applied through the front panel interconnect board and power interconnect board to connector P359. A small wire jumper on plug P359 applies the SW BATT+ voltage to the SW A+ line. The SW A+ voltage, in turn, is routed along several paths.

3.9.1.4 One SW A+ path is through connector J351 to the main board. On the main board, the SW A+ voltage is also applied to accessories connector J350-7 for equipment connected to this jack. A second path for the SW A + voltage is through the power interconnect board to the front panel interconnect board where it is again distributed. One path is through the *DVP* encryption board to the switch board and display board. Another path is to the PL/DPL board, or other option boards mounted in the same location.

3.9.1.5 The PA A+ voltage is routed, via the power interconnect board, to the PA interconnect board through feedthrough-capacitor C263, where it supplies operating voltage to the 10 watt PA and, in 30 watt models, the high-power PA mounted in the external heat sink. PA A+ voltage is also supplied, through J351, to the main board, where it serves as the voltage source for the 9.6 volt regulator, the transmitter power control circuit, and the receiver audio power amplifier. PA A+ also goes to J352 where it gets routed to the *DVP* boards.

3.9.1.6 Reverse polarity and transient voltage protection is provided by diodes CR350 and CR351, and varistor RV352. The black ground lead is connected directly to the chassis via the power interconnect board. A separate logic ground (for digital circuitry in the radio) is connected to the chassis at the same point.

3.9.1.7 The optional ignition control of transmit input is supplied to circuitry on the main board via J351.

3.9.2 Main Board Regulators and Filter

3.9.2.1 A +9.6 V regulator, a +4.8 V regulator, and a C-multiplier filter are located on the main board. The +9.6 V regulator regulates the PA A+ input voltage and is turned on by the SW A+ input voltage. The regulator consists of U300A, Q300, and Q301. It supplies regulated +9.6 V dc to the main board, the synthesizer board, the optional widespaced dual front end, the *DVP* boards and the optional PL/DPL or time-out timer boards.

3.9.2.2 The +4.8 V regulator, Q306, converts the regulated +9.6 V dc to a regulated +4.8 V dc. The regulator provides a temperature-compensated, low-impedance bias supply for IC's in the audio and squelch stages of the receiver and transmitter circuits on the main board, and *DVP* boards.

3.9.2.3 The C-multiplier filter consists of transistor Q305. It filters and reduces the SW A+ voltage to +11.7 V dc and supplies it to the receiver i-f circuits on the main board, and to circuits on the single front end board.

3.9.3 Synthesizer Board Regulator and Filter

A +5 V IC regulator and a noise filter are located on the synthesizer board. The +5 V regulator, U140, provides regulated +5 V dc to the logic circuits on the board. The noise filter, including transistors Q140 and Q141, reduces the +9.6 V dc to 8.9 V dc and supplies it to the VCO and to various circuits on the synthesizer board.

3.9.4 *DVP* Board Regulator

Regulator U101 is a regulator which supplies +5 V dc to some of the logic circuits on the *DVP* boards.

3.9.5 PL/DPL Time-Out Timer Board Regulator

Regulator U1703 is an IC that provides regulated +5 V dc to logic circuits on the board.

3.9.6 Time-Out Timer Board

The +8.8 V regulator on this board consists simply of Zener diode VR1801, resistor R1807, and capacitor C1803. The circuit provides regulated and filtered +8.8 V dc to circuits on the board.

4. DETAILED DESCRIPTION

NOTE

The schematic diagrams referenced in the Detailed Description are located in the Diagrams section of this manual.

4.1 RECEIVER CIRCUITS

4.1.1 Single Front End

(Refer to Single Front End schematic diagram)

4.1.1.1 The standard single front end is located on the single front end board. The single front end consists of an antenna filter, an rf amplifier, an interstage filter, an injection filter, and a mixer. Depending on the kit used, the single front end provides a 4 MHz receive bandwidth, tuneable within the 136 to 162 MHz (TRD6161B) or 146 to 174 MHz (TRD6162B) band.

4.1.1.2 Receiver rf from the receive port of the antenna switch in the transmitter circuits is routed to the input of the antenna filter. The antenna filter is tuned by coils RF1 (L700) and RF2 (L701). The rf output from the filter is amplified approximately 10 dB by rf amplifier Q700 before being applied to the interstage filter. This filter is tuned by coils RF3 (L703), RF4 (L704), and RF5 (L705). The filtered rf output is applied to the gate of N-channel JFET (junction field-effect transistor) mixer Q701. A second input to the mixer is the low side receiver injection signal generated by the frequency synthesizer circuits in the receive mode. The receiver injection signal is applied to the mixer via the injection filter. Coils LO1 (L710), LO2 (L709), and LO3 (L708) tune this filter. The INJ METER point provides a dc voltage (typically between 2.1 to 3.5 V dc) that is proportional to the mixer source current flowing through resistor R703. The INJ METER point is used to tune the receiver injection filter for maximum injection drive to the mixer.

4.1.1.3 The receiver injection signal output from the injection filter is applied to the source of mixer Q701. The mixer combines the receiver rf and the receiver injection signal to produce the 21.4 MHz receiver i-f signal. The i-f output from the mixer drain is applied through a 50-ohm impedance matching network to the input of the receiver i-f circuit on the main board. The mixer characteristics are optimized to produce excellent intermodulation immunity.

4.1.2 Widespaced Dual Front End

(Refer to Widespaced Dual Front End schematic diagram)

4.1.2.1 The optional widespaced dual front end is housed in a metal casting that contains the amplifier board, the mixer board, and the tuneable helical filter coils. Depending on the kit used, the widespaced dual front end provides extended frequency coverage, consisting of two 6 MHz-wide "windows" tuneable anywhere within the range of 136 to 162 MHz (Range I) or 146 to 174 MHz (Range II). The extended coverage is provided by low-range and high-range three-cell helical filters, each 6 MHz wide, that can be tuned to any desired center frequency within one of these ranges. Selection of the appropriate (low-range or high-range) filter is made by the front end select signal generated by the frequency synthesizer circuit in the receive mode. Figure 12 illustrates two examples of the tuning capability of the widespaced dual front end. One example illustrates tuning for continuous 12 MHz coverage, and the other illustrates tuning for two 6 MHz "windows".

4.1.2.2 Receiver rf from the antenna switch is applied to the input filter. The input filter is approximately 30 MHz wide and is factory-tuned by coils

L701, L702, and L703. The filtered rf output is amplified approximately 12 dB by wideband rf amplifier Q750. Diode CR751 protects Q750 against high level rf signals or transients. The rf output from Q750 is then switched to either the high-range or low-range filter, depending on the biasing of the input PIN didoe switch (CR752 through CR755) and the output PIN diode switch (CR761 and CR762). Biasing, in turn, is controlled by the front end select signal.

4.1.2.3 The front end select signal is applied to the front end select logic circuit consisting of differential amplifiers U750A and U750B. When the front end select signal is low (typically 0.2 V dc), the output from U750A is also low (2.7 V dc), and the output from U750B is high (5.8 V dc). This combination of voltage levels turns on diodes CR753 and CR755 in the input diode switch, and diode CR762 in the output diode switch. (The remaining diodes in the input and output diode switches are reverse biased, and are therefore turned off.) When CR753 and CR762 are turned on, CR753 switches the rf output from Q750 to the low-range filter, and CR762 applies the filtered output to the mixer. When CR755 turns on, it switches the input of the high-range filter to rf ground through capacitor C756, further isolating the two filters. Low-range filter coils L704, L705, and L706 tune the filter, and the low-range test point serves as the rf monitoring port while tuning.

4.1.2.4 When the front end select signal is high (typically 6.9 V dc), the front end select logic circuit changes state. This turns on diodes CR752 and CR754 in the input diode switch, and diode CR761 in the output diode switch. In this condition, CR752 switches the rf output from Q750 to the high-range filter, and CR761 transfers the filtered output to the mixer. Diode CR754 switches the input of the low-range filter to rf ground. The high-range filter is tuned by coils L707, L708, and L709. The high-range test point serves as the monitoring port for the filter.

4.1.2.5 The mixer is configured as a broadband, double-balanced mixer. It consists of matched quad diode CR760 and transformers T760 and T761. Transformer T760 couples the selected rf signal to the mixer network while T761 couples the receiver injection signal to the mixer network. The receiver injection signal, which is generated by the frequency synthesizer circuits in the receive mode, is applied to the mixer, via the injection filter. The injection filter is approximately 30 MHz wide and is factory-tuned by coils L710, L711, and L712. The filtered injection signal is applied to the mixer network to produce the 21.4 MHz receiver i-f that is applied to the receiver i-f circuit on the main board.

4.1.3 Main Board Receiver Circuits

(Refer to Main Board and Power Interconnect Board schematic diagrams)

4.1.3.1 I-F Circuit

Several stages of filtering and amplification are provided by the i-f circuit. Selective i-f filtering is accomplished using dual-resonator, mode-coupled, monolithic crystals cut to a fundamental frequency of 21.4 MHz. Each crystal filter, consisting of two poles, is mounted in a single i-f can. Due to the inherent piezoelectric properties of the crystal material, input signals selectively produce mechanical vibrations that propagate through the device. At the output, the same piezoelectric property selectively converts the mechanical vibrations into the i-f electrical signal.

4.1.3.1.1 Figure 13 is a simplified diagram showing the coupling effect of the piezoelectric properties. The figure shows that the high "Q" of the crystals create steep skirts that result in excellent on-channel intelligibility and off-channel signal rejection. The i-f circuit requires no tuning and makes extensive use of shielding to minimize unwanted pick-up by the high-gain stages.

4.1.3.1.2 The 21.4 MHz signal from the single front end (or optional widespaced dual front end) is applied to first buffer Q1. The buffer provides a constant 50-ohm impedance match between the mixer and four-pole crystal filters Y1A and Y1B. This impedance match is maintained even though the crystal filter impedance varies widely for only a few kHz deviation from the i-f frequency. Capacitors C24 and C25, across Y1A and Y1B, improve the adjacent channel selectivity.

4.1.3.1.3 The output from the crystal filters is applied to second buffer Q2. The buffer, together with resistor R3, serves as an impedance termination for the crystal filters, and improves the system noise figure. The i-f signal is amplified by wideband integrated circuit amplifier U1, and is further filtered by two-pole crystal filters Y2A and Y2B. The filtered output is applied through an r-c matching network to integrated circuit limiter/quadrature detector U2.

4.1.3.2 Limiter/Quadrature Detector

4.1.3.2.1 Limiter/quadrature detector U2 is a 16-pin, monolithic integrated circuit that includes three stages of i-f amplification, a quadrature fm detector that recovers the audio from the frequency-modulated carrier, and an audio preamplifier. The limiter/quadrature detector includes approximately

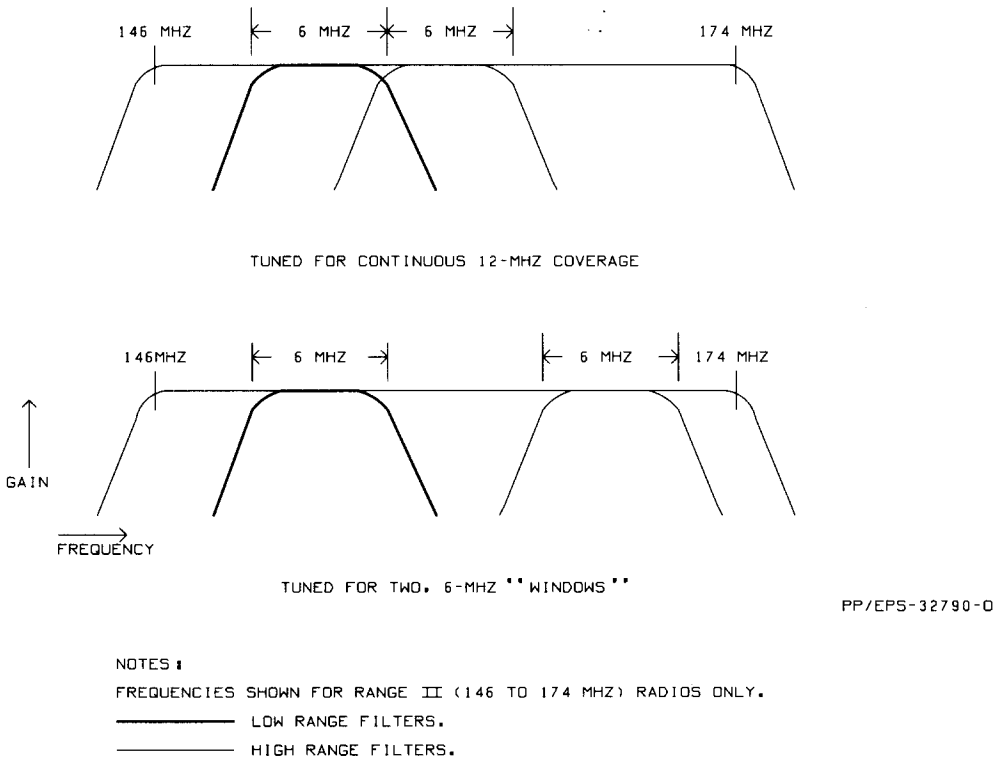


Figure 12. Widespaced Dual Front End Tuning Capability

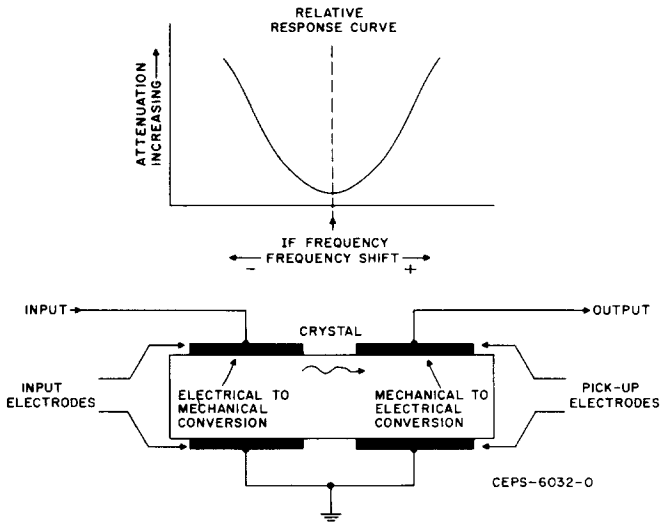


Figure 13. Simplified Piezoelectric Coupling Diagram

85 dB of i-f gain, and produces a recovered audio output level of 16 mV rms per one kHz deviation. The polarity of the output is positive, producing an increasing positive voltage for increasing frequency. The recovered audio output level is adjusted for maximum output by quad coil L5.

4.1.3.2.2 The limiter/quadrature detector also develops a dc output voltage that is proportional to the rf input. This voltage is monitored at the RISE METER point for receiver alignment. For PL/DPL squelch or *Select 5* singaling models, the dc output voltage also serves as the carrier level sense signal that lights the BUSY light on the front panel. (Refer to the paragraph that describes Busy light circuit.) The recovered audio output from the limiter/quadrature detector is applied to detector buffer U50A in the low-level audio circuit.

4.1.3.3 Low-Level Audio Circuit

4.1.3.3.1 Detector buffer U50A serves as an audio operational amplifier whose gain is flat from 0.1 Hz to 100 kHz. The gain is determined by selected resistor R50 and feedback resistor R51. The audio output from U50A is applied to second operational amplifier U50B, which serves as a de-emphasis amplifier. The audio output from U50A is also applied as the option receive audio signal to the *DVP* circuitry, the PL/DPL circuit, accessory connector J350-1, and the squelch circuit. If the *DVP* circuitry detects a coded transmission, it switches decoded audio back into the audio path. If the *DVP* circuitry does not detect code, it passes the low level audio untouched. From the *DVP* board, the audio routing depends on whether or not the

radio is equipped with PL/DPL. If the radio has the PL/DPL option, the audio from the *DVP* board is routed to the PL/DPL board for tone decoding and filtering. The PL filtered audio is then injected back into the low-level audio path at the input of U50B (junction of R52 and R53). If the radio is not equipped with PL/DPL, the audio from the *DVP* board is injected back into the low-level audio path at the same junction (U50B, R52 and R53). In either case, R52 is effectively an open circuit because of the low output impedance of either the PL filter or the *DVP* buffer.

4.1.3.3.2 The de-emphasis network is formed by resistor R55 and capacitor C55. Capacitor C53 attenuates frequencies beyond 3 kHz, and C54 reduces low frequency noise that may appear on the receiver injection signal inserted into the front end by the frequency synthesizer circuits. Capacitor C54 also helps eliminate PL tones that may appear on the PL filtered audio line when a PL channel is in use. The audio output from U50B is applied to primary mute gate Q50 in the audio muting circuit.

4.1.3.4 Audio Muting Circuit

4.1.3.4.1 Primary mute gate Q50 and secondary mute gate Q58 form the main components of the audio muting circuit. The circuit can be gated on (unmuted) and off (muted) by four signals.

- The high lock detector (VCO lock) signal from the frequency synthesizer circuits;
- The +9.6T keying voltage from the transmitter PTT logic circuit;
- The *DVP* muting signal which is a combination of *DVP* muting functions, the receive audio mute signal from the PL/DPL or *Select 5* circuits, and the squelch mute signal developed by the receiver;
- The sidetone enable signal from the *DVP* circuits, the PL/DPL, time-out timer, or *Select 5* circuits;

If a mute signal is not supplied by the frequency synthesizer, transmitter, or *DVP* circuitry, the audio path is gated on as follows.

4.1.3.4.2 De-emphasis Amplifier

U50B supplies a low-impedance, +4.8 V dc source voltage to the emitter of Q50. The base current for Q50 flows through resistor R56 to ground, saturating Q50. Therefore, the audio applied to the emitter of Q50 also appears at the collector of Q50. The base voltage of Q50 is applied, via resistor R76 and Zener diode VR54, to the base of Q58, but because the base voltage of Q50 is lower than the breakdown voltage of VR54, Q58 is cut off. This allows audio from the collector of Q50 to pass through the volume control and, via capacitors C64 and C59, to the audio power amplifier.

4.1.3.4.3 If the synthesizer frequency is out-of-lock, a high voltage is applied to the base of Q50 via diode CR302. Since the emitter of Q50 is maintained at +4.8 V dc by U50B, Q50 is cut off. The high voltage at the base of Q50B is also applied, via R76 and VR54, to the base of Q58. Since VR54 is now conducting, Q58 becomes saturated. The combined attenuation of cut-off series gate Q50, and saturated shunt gate Q58, is in excess of 100 dB.

NOTE

Refer to the "TP9 Mute Voltage Chart" on the schematic diagram for voltage levels at test point 9.

4.1.3.4.4 In a similar manner to that just described, muting also occurs under the following conditions.

- During transmit, the 9.6T keying voltage from the transmitter circuits is applied to the base of Q50B, via diode CR303.
- With no on-channel carrier and the squelch pushbutton at the front panel in the squelched (out) position, the squelch circuit supplies a high voltage (+8.4 V) to Q50, via Q2101, the *DVP* muting circuitry and Q2102 in the squelch circuitry.
- In PL/DPL squelch or *Select 5* signaling models, audio is muted in the signaling squelch mode of operation by a high receive audio mute signal applied from the signaling board. This signal goes to the *DVP* muting circuitry, via P352-12, which puts a high on Q2102, muting the receive audio.

4.1.3.4.5 To allow sidetone to be inserted into the audio path when the receiver audio is muted, the sidetone enable signal goes to ground. This turns off Q58 and allows the sidetone/alert tone from the *DVP*, the PL/DPL, time-out timer, or *Select 5* signaling circuits to be inserted through the volume control to the audio power amplifier. The sidetone level is automatically reduced if the receiver is suddenly unsquelched due to an on-channel signal; as Q50 turns on to unmute the receiver audio, the resistive combination of R60 and 2,000 ohm volume control R819 is effectively reduced to approximately 440 ohms, thus lowering the sidetone level supplied to the volume control.

4.1.3.5 Audio Power Amplifier

4.1.3.5.1 The receiver audio is amplified by the audio power amplifier, which is composed of transistors Q51 through Q57. The amplifier residual noise level is at least 40 dB lower than that of currently available integrated circuit amplifiers and supplies five watts of power to the 2 ohm speaker.

4.1.3.5.2 Transistor Q52 is a current source used to provide a constant base biasing current to

the output stages as the A+ supply voltage varies between +10.8 and +16.5 V dc. Resistors R61 and R62, and capacitors C57 and C58 attenuate noise and alternator whine present on the SW A+ voltage source used to bias Q51. This achieves an alternator whine rejection considerably greater than that obtainable with integrated circuit power amplifiers.

4.1.3.5.3 Capacitors C64 and C59, and resistor R73 form a two-pole, active high-pass filter using the audio power amplifier as the gain element. This configuration achieves rapid attenuation of noise, hum, and PL tones below 300 Hz without affecting response above 300 Hz.

4.1.3.6 Squelch Circuit

4.1.3.6.1 The squelch circuit consists essentially of an integrated circuit containing four operational amplifiers, a full-wave rectifier, a variable time constant circuit, and two current drivers. The audio output from detector buffer U50A is coupled through capacitor C51 to first amplifier U2100A. This amplifier operates as an audio-captured limiter that reduces high frequency modulation noise. The output from U2100A is adjusted by SQ (squelch adjust) potentiometer R2103, which controls the noise queting level at which the squelch operates. The audio is then applied to second amplifier U2100B. Amplifier U2100B amplifies squelch noise above 12 kHz, and also acts as a temperature-compensated stage whose gain varies with temperature to track changes in characteristics of diodes CR2102 through CR2105. These diodes form the full-wave rectifier that increases the operating speed of the squelch circuit by detecting both positive and negative noise spikes. This produces a dc output from third operational amplifier U2100C that is proportional to the receiver quieting level.

4.1.3.6.2 Operational amplifier U2100D integrates the dc output from U2100C using resistor R2111 and capacitor C2107 and compares the dc average with a fixed reference voltage at pin 13 of U2100D. The reference voltage is determined by resistors R2113 and R2114. When the carrier signal is absent, the dc voltage at pin 3 is below the reference voltage, causing the output from U2100D to go high. This turns on current driver Q2101, which applies a high to the *DVP* muting circuitry, via P352-12. This causes the *DVP* circuitry to put a high on the base of Q2102, supplying a high voltage to Q50, and muting the receive audio. When the carrier signal is present and quieting occurs, the dc voltage at pin 3 rises above the reference voltage. This drives the output of U2100D low, turning off Q2101 and applying a low to the *DVP* muting circuitry. The *DVP* muting circuitry then applies a low to the base of Q2102, unmuting the receive audio. The squelch circuit is defeated by pushing the squelch pushbutton in. This prevents Q2101 from applying a high to the *DVP* board, thus keeping the audio unmuted.

4.1.3.6.3 The receiver audio can also be muted or unmuted by the receive audio mute signal supplied by the PL/DPL Squelch or *Select 5* signaling circuits. When a valid PL/DPL code is not detected, the receive audio mute signal at connector P352-12 is high. This applies a high to the *DVP* muting circuitry, which responds by putting a high voltage on the base of Q2102, muting the receiver.

4.1.3.6.4 In PL/DPL radios, the PL/DPL decoder circuit unmutes the audio by supplying an active low receive audio mute signal to the *DVP* mute circuitry, via connector P352-12. For weak signals, the squelch circuit would otherwise mute the audio with a high voltage from the emitter of Q2101. This enables reception of weak signals that are below the squelch circuit threshold of 10 dBq, but are above the decode threshold of the PL/DPL decoder circuit (approximately 6 dBq.).

4.1.3.6.5 Transistor Q2100 reduces squelch closing time depending on the strength of the carrier signal. The closing time is determined by the charging time (r-c time constant) of resistor R2116 and capacitor C2109. For weak carrier signals, a longer time constant is produced (approximately 200 milliseconds); for stronger signals, a faster time constant is produced (approximately 0.1 milliseconds). As the carrier level increases, the dc output from U2100C increases proportionally. This turns on Q2100, reducing the charge through C2109 and allowing the base of Q2101 to follow the output of U2100D. For dekey of strong signals, sudden negative-going spikes at the output of U2100C rapidly turn off Q2100 via diode CR2106. This causes positive pulses at the base of Q2101, muting the audio fast enough that no squelch tail is heard. The base of Q2101 is maintained high by the output of U2100D, via resistor R2116.

4.1.3.7 Busy Light Circuit
(Refer to Main Board and Power Interconnect Board)

4.1.3.7.1 The Busy light circuit is mounted on the Busy light board and is used in PL/DPL squelch or *Select 5* signaling models. The circuit controls the Busy liht on the front panel. The Busy light is an orange LED that lights to indicate that a channel is in use.

4.1.3.7.2 The Busy light circuit is controlled by the sense signal developed by limiter/quadrature detector U2, the squelch output of U2100D, and the 9.6T keying voltage. The sense signal is a dc voltage that varies in proportion to the signal level present in the receiver i-f. In single front end receivers, the sense signal varies from approximately 2.1 V dc (no receiver i-f signal) to 4.6 V dc (strong receiver i-f signal). In widespaced dual front end receivers, the no-signal voltage is approximately 1.5 V dc.

4.1.3.7.3 In the absense of an on-channel signal, the sense voltage of the base of switch Q1200 is below the reference voltage at its emitter. The reference voltage is determined by BUSY LIGHT ADJ potentiometer R1202. A clockwise adjustment reduces the threshold sensitivity. The reference voltage keeps switch Q1200, current driver Q1201, and the Busy light off. When a signal is present in the receiver i-f, the increased sense voltage turns on switch Q1200. This turns on current driver Q1201, supplying current to the LED via resistors R1206 and R1207, causing it to illuminate. The emitter of Q1200 is returned to the 9.6T keying voltage rather than to ground to prevent the Busy light from turning on due to transmitter sideband noise present in the receiver i-f during transmit.

4.1.3.7.4 The squelch output of U2100D is used to insure that the Busy LED does not turn on unless the squelch circuitry has also determined that carrier is present. This prevents the LED from turning on when the radio is in a very noisy rf environment where the sense signal would rise high enough to turn on the LED, even though the radio is not receiving a transmission. The collector of Q2103 forces the busy light control signal low (LED off) unless the squelch circuit detects carrier.

4.2 TRANSMITTER CIRCUITS

4.2.1 PTT Logic Circuit

(Refer to Main Board and Power Interconnect Board)

4.2.1.1 The PTT logic circuit generates the 9.6T voltage (keyed +9.6 V dc) used to key the transmitter. The circuit also mutes the microphone audio supplied to the transmit audio/IDC circuit during receive and unmutes the audio during transmit.

4.2.1.2 The PTT logic consists of ignition control stage Q304 (used in models with ignition control option B113 only), mic mute control Q303, active jumper Q308, and 9.6T switch Q302 and Q307. The 9.6T keying voltage is generated at the common collectors of Q302 and Q307. In the receive mode, Q302 is held off and Q307 is held on due to voltage divider network R310, R311, R316, and R317. The 9.6T keying voltage is, therefore, low (near ground potential).

4.2.1.3 The PTT logic circuit can be controlled by any of six sources.

- The microphone, via J350-14 in front mount radios or P380-1 in remote mount radios,
- The *DVP* circuitry,
- The PL/DPL squelch or *Select 5* signaling circuits,
- The time-out timer circuits (when used as an option in carrier-squelch models only),
- The vehicle's ignition switch (in ignition control option B113 only), or
- Accessories connected externally via J350-6.

4.2.1.4 Pressing the microphone push-to-talk button supplies a mic PTT ground signal, via J350-14 and jumper JU302, to mic mute control Q303. (In remote mount radios, the mic PTT signal from connector P380-1 is also applied to Q303 along this path.) Transistor Q303 turns on due to the base-emitter current flowing through it, and supplies a low mic mute signal to turn on mic audio mute gate Q325 via R327 in the transmit audio/IDC circuit. Turning on Q325 allows microphone audio to be passed to the audio circuits. With the ignition control option, jumper JU302 is cut, R313 and Q304 are added, and Q303 is controlled by ignition control transistor Q304. In this option, the positive voltage from the vehicle's ignition switch, routed to the radio via an additional orange wire, supplies current to the base of Q304 via R313. This allows the mic PTT signal to key Q303, via the saturated stage Q304.

4.2.1.5 In carrier-squelch radios, when Q303 is keyed via a low mic PTT signal at the emitter (TP44), the base voltage (TP43) goes low. This supplies a low PTT signal to the *DVP* PTT circuitry via P352-4. The *DVP* PTT circuitry grounds P352-5, the base of Q308. This allows the *DVP* circuitry to control the 9.6T generating transistors, Q302 and Q307 via P352-3 (TP41). When PTT goes low, the *DVP* circuitry puts a low on the base of Q302 and Q307, providing the 9.6T keying voltage (actually 9.5 V dc due to Q302's saturation voltage) at the collector of Q302 (TP39).

4.2.1.6 In carrier-squelch models with the time-out timer option, operation is similar to above, except that the time-out timer also has an input to the *DVP* PTT circuitry. The time-out timer monitors the voltage at TP43, low with the microphone keyed, via P352-4. At time-out, the timer circuit puts a low on the TOT line (J101-24) going to the *DVP* PTT circuitry. This causes the *DVP* circuitry to remove the low on the base of Q302 and Q307, removing the 9.6T keying voltage.

4.2.1.7 In PL/DPL squelch models, the PL/DPL circuits monitor mic PTT status via P352-4. When the mic PTT signal goes low, the PL/DPL circuitry then supplies an option delayed PTT low signal to the *DVP* PTT circuitry, via J101-25. The *DVP* circuitry then controls the 9.6T keying voltage via J352-3.

4.2.1.8 Radios with *Select 5* signaling or with external accessories connected via J350 key the transmitter by supplying a low at TP43 via P352-4 (*Select 5)* or J350-6 (accessories). This keys the transmitter via a low PTT signal to the *DVP* PTT circuitry. Also, because Q303 base is grounded, this stage as well

as Q325 cannot turn on, muting microphone audio during transmissions initiated by *Select 5* signaling or accessory circuits.

4.2.2 Transmit Audio/IDC Circuit

(Refer to the Main Board and Power Interconnect Board)

4.2.2.1 The transmit audio/IDC circuit consists of mic audio mute gate Q325, operational amplifier/limiter U325A, splatter filter U325B, *DVP* audio switch U105A and B and IDC mute gate Q326.

4.2.2.2 Audio is applied to mic audio mute gate Q325 from the microphone, via connector P350-12 (front mount radios), or connector P380-4 (remote mount radios). When Q325 is turned on by the low mic mute signal from the PTT logic circuit (Q303), the audio output from Q325 is applied through pre-emphasis network C326 and R328 to operational amplifier/limiter U325A. Transmit audio from options or accessories can also be inserted into the audio path via connectors J350-2 and P352-17. Resistor R329 and capacitor C327 provide a flat response for the option transmit audio. Diode CR325 limits the audio output from U325A to a symmetrical waveshape centered at approximately 4.8 V dc. Resistors R331, R332, and R333 form a 6 dB attenuation pad that prevents the full-limited output of U325A from causing clipping in the output of splatter filter U325B. Capacitor C333 and inductor L325 reduce adjacent channel splatter by filtering harmonics above the audio passband.

4.2.2.3 The PL/DPL signals from the PL/DPL circuits are inserted into the audio input of the splatter filter, via connector P352-20, at the junction of resistors R331 through R334. PL/DPL insertion after the limiter maintains constant PL deviation regardless of the degree of limiting.

4.2.2.4 The output from the splatter filter goes to the *DVP* circuitry via J1001 (IDC AUDIO) and J101-15. If it is a coded transmission the audio is converted to a digital waveform by U103, encrypted by HY101, and splatter filtered by U102. The signal then goes to potentiometers R158 and R161. R158 adjusts the level of *DVP* signal sent back into the VCO modulation path to Q326, via J101-17 and J1002 (VCO MOD). R161 adjusts the level of *DVP* signal sent to the 14.4 MHz reference oscillator via J352-16. If the transmission is in a clear mode, the audio comes back unaltered from the *DVP* circuitry to Q326, via J101-17 and J1002 (VCO MOD). IDC mute gate Q326 is cut off in the receive mode due to the absence of the 9.6T keying voltage at its base. When cut off, Q326 prevents noise in the IDC stages from modulating the VCO. During transmit, the gate is turned on as the 9.6T keying voltage is applied to its base via R337. The output from the gate is coupled through capacitor C331 to VCO MOD potentiometer R341, which adjusts the deviation level of the VCO modulation. The output from the potentiometer is the VCO modulation signal used to drive the VCO hybrid in the frequency synthesizer circuits. If the radio has the PL/DPL option, the PL/DPL circuitry will also modulate the 14.4 MHz reference oscillator. The reference modulation signal is sent from the PL/DPL circuitry via J352-16 to the REF MOD level-adjust potentiometer R344, and from there to the 14.4 MHz oscillator in the frequency synthesizer circuitry.

4.2.2.5 The two modulating signals carry information at different frequencies. The VCO modulation line carries information above 50 Hz and the reference modulation line carries information below 50 Hz. Two IDC outputs are used because, due to the nature of the frequency synthesizer correction loop, the VCO cannot be modulated below 50 Hz without the loop tracking out the signal, resulting in no modulation of the synthesizer VCO. However, by modulating the reference oscillator with frequencies below 50 Hz, the synthesizer correction loop can track frequency changes down to nearly 0 Hz. This technique, called "dual port modulation", allows modulation to take place over a very wide range of frequencies, while maintaining practical amounts of loop filtering and reasonable lock times.

4.2.3 Transmit Power and Level Control Circuit

(Refer to Main Board and Power Interconnect Board)

4.2.3.1 The transmit power and level control circuit consists of differential amplifier U300B and transistors Q225 through Q228. The circuits form a control loop that reduces or inhibits the rf drive, therefore the transmitter rf output power, if any of the following occurs.

- LLA (low level amplifier) A+ voltage, which controls rf drive available from the low level amplifier, exceeds a preset maximum limit;
- Short-circuit in LLA A+ line;
- RF output power becomes excessive;
- Load mismatch becomes excessive;
- Overtemperature conditions exists (25/30 watt power amplifier only);
- Synthesizer goes out-of-lock.

4.2.3.2 The directional coupler signal monitors the rf output power, the temperature compensation signal monitors the directional coupler temperature, the heat sense signal monitors the temperature of the 30 watt power amplifier, and the lock detect signal monitors synthesizer lock condition.

4.2.3.3 Transistor Q225 utilizes the PA A + voltage to supply the regulated LLA A + voltage to the low level amplifier. Differential amplifier U300B compares any parameter changes to a fixed dc reference voltage and develops a correction signal that adjusts the LLA A + voltage, to offset the changes. The fixed dc reference voltage determined by resistor network R238, R239, R240 and voltage limit potentiometer R236, is applied to the positive input of U300B. The sensing voltage appears at the negative input of U300B. The dc level at this input is determined by the voltage divider circuit of R243, R244, and R246, and PWR ADJ potentiometer R245. The PWR ADJ potentiometer sets the rf output power level of the transmitter. Once set, the loop maintains this output power. During normal operation, the voltage levels at both the positive and negative inputs of U300B is approximately + 5 V dc.

4.2.3.4 If the rf output power increases, the directional coupler monitoring signal decreases. This lowers the dc level at the negative input of U300B, causing the output from U300B to increase. This decreases the current through Q227, causing the output from series-pass transistors Q225 and Q226 to decrease. This lowers the LLA A + voltage, reducing the gain of the low level amplifier. With lowered gain, the rf drive is reduced, causing the rf output power to be reduced to the desired level. As a result, a constant power level independent of frequency and temperature is maintained.

4.2.3.5 In the 30 watt power amplifier only, the negative input of U300B also samples the heat sense monitoring signal developed by the thermistor (RT1401) mounted near the power transistor. If the temperature rises above 120 °C the heat sense monitoring voltage decreases. This causes diode CR227 to conduct, reducing the voltage at the negative input of U300B. This, in turn, causes the correction loop to reduce the LLA A + voltage until the temperature is stabilized.

4.2.3.6 The LLA + voltage is made self-limiting by voltage limit adjust potentiometer R236, resistor R237, and diode CR226. If the LLA A + voltage rises above the level set by potentiometer R236, diode CR226 conducts, increasing the voltage at the positive input of U300B. This increases the output from U300B, causing the correction loop to reduce the LLA A + voltage to the preset level. The positive input of U300B is also controlled by the temperature compensation monitoring signal developed by a temperature- sensitive diode (CR1451) located near the directional coupler. Increased temperature at the directional coupler causes the correction loop to reduce the LLA A + voltage.

4.2.3.7 The LLA A + voltage is disabled if the synthesizer goes out-of-lock. Normally, the lock detect signal from the frequency synthesizer circuits is low. This keeps Q228 switched off, which keeps the LLA A + voltage on. If the synthesizer goes out-of-lock, the lock detect signal goes high. This switches on Q228, which applies a ground to the base of Q226. This turns off Q225 and Q226, disabling the LLA A + voltage.

4.2.3.8 The LLA A + voltage is also turned off if the LLA A + line is short-circuited to ground. Diode CR225 becomes forward biased at this time, turning off Q225 and Q226.

4.2.3.9 The LLA A + voltage is disabled during receive mode. Because the 9.6T keying voltage is absent, the negative input of U300B is forced low, causing the output from U300B to rise towards the PA A + supply voltage. This effectively removes the drive from the base of Q226, allowing the PA A + voltage, via resistor R225, to keep Q225 off.

4.2.4 Low Level Amplifier

(Refer to Power Amplifier schematic diagram)

The low level amplifier supplies the rf drive for the 10 watt power amplifier. The 136 to 174 MHz transmit injection signal from the frequency synthesizer circuits is applied through a 3 dB resistor pad to the input of the low level amplifier. The pad, comprised of resistors R1451, R1452, and R1453, attenuates and isolates the synthesizer from low level amplifier input impedance variations. The injection signal is passed through a high pass filter network to remove low frequency spurious signals before being applied to the two-stage, non-linear amplifiers Q200 and Q201. Collector power for the two stages is the LLA A + voltage supplied by the transmitter power and level control circuit, via feedthrough capacitor C214 on the feedthrough plate. The LLA A + voltage controls the gain of the low level amplifier and is precisely regulated to maintain the rf output power level at the preset level. The 2.2 watt output from the amplifier is applied through an attenuation network composed of resistors R1454 through R1457, to the input of the 10 watt power amplifier. The attenuation is 2.3 dB in 10 watt transmitters; 1 dB in 30 watt transmitters. The pad isolates the low level amplifier from input variations of the power amplifier.

4.2.5 10 Watt Power Amplifier

(Refer to Power Amplifier schematic diagram)

4.2.5.1 The 10 watt power amplifier consists of a single non-linear amplifier stage, Q250. The power amplifier produces the final rf output for the low power *DVP MCX100* radio set. In radio sets that use the 30 watt power amplifier, the 10 watt unit is used to drive this high power amplifier. Operating voltage for the power amplifier is the PA A + voltage suppied by the power distribution circuit. The voltage is applied via feedthrough capacitor C263 on the feedthrough plate.

4.2.5.2 The rf output from the 10 watt power amplifier is applied along a microstrip transmission line to the harmonic filter/antenna switch. The length of the microstrip is selected to maximize the attenuation of second harmonics.

4.2.6 30 Watt Power Amplifier

(Refer to Power Amplifier schematic diagram)

4.2.6.1 The 30 watt power amplifier is driven by the 10 watt power amplifier via a coaxial cable. The 30 watt power amplifier uses a single, non-linear power transistor, Q1400. The PA A+ voltage from the power distribution circuits supplies the operating voltage for the power amplifier. Thermistor RT1400 is mounted near the power transistor. RT1400 controls the output power of the transmitter to keep the temperature within safe limits.

4.2.6.2 The temperature of Q1400 is monitored by the heat sense signal returned to the transmit power and level control circuit via feedthrough capacitors C1416 (on the 30 watt power amplifier) and C267 (on the feedthrough plate). If the temperature reaches 120 °C, the resistance of RT1400 decreases. This is reflected on the heat sense monitoring signal to cause the control circuit to reduce the output power until the temperature is stabilized. The final rf output from the power amplifier is routed to the harmonic filter/antenna switch hybrid on the PA interconnect board.

4.2.7 Harmonic Filter/Antenna Switch

(Refer to Power Amplifier schematic diagram)

4.2.7.1 The 10 watt rf signal (or the 30 watt rf signal) is applied to the input port of the antenna switch. The antenna switch is controlled by the 9.6T keying signal generated by the PTT logic circuit. The signal is supplied via feedthrough capacitor C296 on the feedthrough plate.

4.2.7.2 With the radio set in the transmit mode, the 9.6T keying signal is enabled. The antenna switch directs the rf signal through the transmit port of the switch, through the harmonic filter and directional coupler to the antenna. In the receive mode, the 9.6T keying signal is grounded. Incoming receive rf is then reflected back through the directional coupler and harmonic filter, and through the receive port of the antenna switch to the input of the receiver front end. The harmonic filter removes spurious signals generated by the power amplifiers and the antenna switch by presenting a high VSWR (voltage standing wave ratio) load to all frequencies above the VHF range.

4.2.7.3 The directional coupler is a microstrip that senses forward and reflected power in the rf output line. The forward and reflected ports of the coupler are directed to their respective detector circuits where the signals are filtered, rectified, weighted, and summed to produce a dc voltage that is proportional to the sum of the forward and reflected power. This dc voltage, which decreases with increased power, is the directional coupler monitoring signal that is returned to the transmit power and level control circuit, via feedthrough capacitor C294 on the feedthrough plate. If the rf output power increases to a level that could damage the power amplifier circuits, the directional coupler monitoring signal causes the control circuit to reduce the rf output power to a safe level.

4.2.7.4 The temperature of the directional coupler is monitored by diode CR1451. The diode sends a temperature compensation monitoring signal to the transmit power and level control circuit via feedthrough capacitor C295 on the feedthrough plate. As directional coupler temperature varies, due to ambient conditions or dissipation, the changing forward voltage drop of CR1451 is sensed by the transmit power and level control circuit. The changing voltage drop acts to offset the rf output power variations which would otherwise occur due to temperature-induced changing characteristics of the directional coupler.

4.3 FREQUENCY SYNTHESIZER CIRCUITS

The frequency synthesizer consists of the channel selection and display circuits, the synthesizer board circuits, and the VCO hybrid circuits. The channel selection and display circuits, which include the front panel channel selector switch and LED display, are covered in the functional description of the frequency synthesizer circuits and are not detailed here.

4.3.1 Synthesizer Board Circuits

NOTE

Except for the divider/phase detector (U115) circuit description, the following descriptions refer to the schematic diagrams in the Synthesizer section.

4.3.1.1 14.4 MHz Reference Oscillator

The 14.4 MHz reference oscillator provides a stable reference for the frequency synthesizer. The oscillator is completely self-contained and non-serviceable. During transmit operation, low frequency (below 50 Hz) *DVP* and DPL signals are routed directly to the reference oscillator. This is required because divider/phase detector U115 can track low frequency modulation, and prevent direct low frequency audio (frequencies required for *DVP* and DPL) from modulating the VCO.

4.3.1.2 Frequency Select PROM

Frequency selection data (factory or field programmed) in the PROM is addressed by five binary bits from the channel selector switch via five address lines, A0 through A4. The five bits comprise the channel select word.

NOTE

On the synthesizer schematic diagram, use the address line designations on the outside of the U117 symbol. The designations inside the symbol do not correspond to the channel select address lines.

Frequency selection in the PROM is further determined by the presence or absence of transmitter keying signal, 9.6T, at pin 5 of the PROM as follows:

- Presence of 9.6T: data words specify transmit frequency
- Absence of 9.6T: data words specify receive frequency.

Data words transfer from PROM U117, to divider U115, when a +5 volt enable signal at pin 15 (VCC) coincides with arrival of a word select signal (three address bits, A0-A2) from the divider. Frequency data is transferred to the divider by six 4-bit words on data lines D0 through D3.

4.3.1.3 PROM Enable Circuit

4.3.1.3.1 The PROM enable circuit allows divider/phase detector U115 to address the PROM for either of three conditions:

- The transmitter is keyed.
- The frequency is changed.
- The synthesizer goes out-of-lock.

When the transmitter is keyed the PROM enable circuit is controlled by the 9.6T keying voltage, either directly or via U351, depending on the model. When the frequency is changed the circuit is controlled by the A0 address line from the channel selector switch, or by the output (FC) of frequency change detector U351, depending on the model. If the synthesizer goes out-of-lock, the circuit is controlled by the lock detect switch.

4.3.1.3.2 The PROM enable circuit used with the TRN5243A synthesizer consists of IC U116 and output inverters Q118, Q119, and Q120. The 9.6T keying voltage or a change in frequency is sensed by frequency change detector U351. U351 produces a positive going pulse on the FC line for every change in an input line (A0-A4 or 9.6T). The positive pulse sets flip-flop U116A and U116B, causing the output to go high. This turns on Q118, driving Q118 output low.

4.3.1.3.3 The output of Q118 is connected to the $\overline{\text{LOCK}}$ output line of divider U115. The output of Q118 is driven low and forces the lock detector switch into an out-of-lock condition. This causes the lock detect switch to generate a high lock detect signal that is fed back to series-connected NOR gates U116C and U116D. The high output from NOR gate U116D turns on Q120, driving its output low, and resets flip-flop U116A and B. The low output of Q120 is the read enable signal applied to the enable input of U115. With the enable input activated, U115 outputs a 10 microsecond low $\overline{\text{STROBE}}$ signal that reoccurs every 200 microseconds. The low $\overline{\text{STROBE}}$ signal turns on Q119. When Q119 turns on, it turns on Q115, and when Q115 turns on, it supplies +5 V dc enabling voltage to the VCC pin of the PROM. With the PROM enabled, frequency data is read from the PROM to the divider U115.

4.3.1.3.4 When the synthesizer locks onto the correct frequency, the $\overline{\text{LOCK}}$ output from U115 goes high. This disables the enable input to U115, disabling in turn the $\overline{\text{STROBE}}$ output from U115. With the $\overline{\text{STROBE}}$ output disabled, power is removed from the PROM, and the PROM enable circuit reverts to its initial condition.

4.3.1.4 Divider/Phase Detector

(Refer to Synthesizer section 68P81045E88, in the service manual.) The divider/phase detector contains the following circuits:

- multiplex control
- six 4-bit latches
- loop divider (programmable)
- phase detector
- reference divider (programmable)

4.3.1.4.1 Multiplex Control

The multiplex control circuit performs three functions:

- Three address bits on lines A0 through A2 select 4-bit words in the PROM. The selected 4-bit words containing frequency data are transferred from the PROM to the six 4-bit latches.
- An ENABLE signal initiates generation of 10 microsecond $\overline{\text{STROBE}}$ signals that reoccur every 200 microseconds.
- Produces a LATCH CONTROL signal that determines which data words are stored in each of the six latch registers.

4.3.1.4.2 Latch Circuits

4.3.1.4.2.1 The six 4-bit latches are activated when the multiplex control circuit receives the active (low) enable signal from the PROM enable circuit. The multiplex control circuit also applies a latch control to the six 4-bit latches.

4.3.1.4.2.2 The information stored in the six 4-bit latches determines the values (A and B) for the counters in the loop divider. The stored information

also determines the output levels of the S1, $\overline{VCO1}$, and $\overline{VCO2}$ signals appearing at pins 17, 19, and 20, respectively, of U115. These signals are applied to the frequency shift logic circuit to determine at which sub-range the VCO operates.

4.3.1.4.2.3 The $\overline{S0}$ signal from the latch registers, appearing at pin 18, is used only with dual front end receiver models. The signal is used to select one of two 6 MHz filters at the front end of the receiver. When the $\overline{S0}$ signal is low, the low range 6 MHz filter is switched into the rf signal path. When the $\overline{S0}$ signal is high, the high range 6 MHz filter is switched into the rf signal path.

4.3.1.4.3 Loop Divider

The loop divider contains a double-programmable dual modulus counter. The counter acts as a programmable divider for the VCO rf feedback signal from the VCO output by dividing by 64 for a programmable number of (A) cycles, and then by 63 for another programmable number of (B) cycles. Divider rf buffer Q192 isolates the VCO rf feedback signal from the divider. The loop divider divides the VCO feedback signal by 64 "A" times and by 63 "B" times. The output of the loop divider counters is the loop frequency signal that is applied as the second input to the phase detector. The loop frequency signal is the VCO output signal frequency divided by (64A and 63B). The loop frequency is applied to one input of the phase detector.

4.3.1.4.4 Reference Divider

The reference divider divides the 14.4 MHz signal from the reference oscillator to any of three reference frequencies: 4.166 kHz, 5.0 kHz, or 6.25 kHz. These frequencies are determined by the channel spacing of the *DVP MCX100* radio set. The reference frequency is applied as one input to the phase detector.

4.3.1.4.5 Phase Detector

The phase detector compares the reference and loop frequency outputs from the two dividers for frequency and phase. The phase detector uses the frequency and phase relationships to produce pulses for the $\overline{UP}$ and DOWN output lines. If the loop frequency is lower than the reference frequency, the phase detector produces a number of $\overline{UP}$ error pulses that is proportional to the amount of error. If the loop frequency is higher than the reference frequency, the phase detector produces DOWN error pulses. The $\overline{UP}$ and DOWN error pulses are applied to the charge pump and loop filter circuit to affect the output frequency of the VCO. The output of the phase detector continues to adjust the VCO output frequency until the loop frequency equals the reference frequency. The synthesizer is then "locked" on frequency and a logic high is generated at the $\overline{LOCK}$ output of the phase detector. The logic high is applied to the lock detect switch. The lock detect switch controls the various transmitter and receiver circuits that are disabled when the synthesizer is out of lock.

4.3.1.5 Lock Detect Switch Circuit

4.3.1.5.1 The lock detect switch monitors the $\overline{LOCK}$ output from divider/phase detector U115. When the $\overline{LOCK}$ output is high, the synthesizer is locked onto the correct frequency, and when it is low, the synthesizer is out-of-lock. When the synthesizer goes out-of-lock, the lock detect switch supplies a high LOCK DET signal to disable the transmitter (during the transmit mode) or to disable the receiver (during the receiver mode). The high LOCK DET TRIGGER output is also applied to the PROM enable circuit to energize the PROM.

4.3.1.5.2 The lock detect switch consists of Schmitt trigger Q154 and Q155, and inverter Q156. The LOCK DET TRIGGER signal is developed at the collector of Q156. When the $\overline{LOCK}$ output from U115 is high (synthesizer in-lock), the high output keeps Q154 on and Q155 off. When Q155 is off, Q156 is also off, thus keeping its collector output low.

4.3.1.5.3 When the $\overline{LOCK}$ output from U115 goes low (synthesizer frequency out-of-lock), the low error pulses are filtered by integrator network R159 and C156. When the pulses are wide enough, the dc voltage at the junction of R159 and C156 falls below the threshold voltage of the Schmitt trigger, causing it to change state. This turns on Q156, driving its output high, thus activating the LOCK DET TRIGGER signal. The Schmitt trigger returns to its original state when the charge on capacitor C156 is sufficiently high to turn on Q154.

4.3.1.5.4 Radios using the TRN5243A Synthesizer Board and TRN5241A/TRN5244A Front Panel Interconnect Board also contain lock detect delay IC U350. U350 outputs a pulse of longer duration than the lock detect pulse, to make sure that the synthesizer in radios equipped with the *Channel Scan* monitor option is locked before squelch status is checked.

4.3.1.6 Charge Pump And Loop Filter Circuit

4.3.1.6.1 The charge pump and loop filter circuit converts the $\overline{UP}$ and DOWN pulses generated by divider/phase detector U115 to the dc VCO steering line voltage. The VCO steering line voltage determines the operating frequency of the VCO. Pulses on the $\overline{UP}$ line increase the VCO steering line voltage (increasing the VCO operating frequency), whereas pulses on the DOWN line decrease the VCO steering line voltage (decreasing the VCO operating frequency).

4.3.1.6.2 The VCO steering line voltage is developed by transistors Q150, Q152, and Q153. Transistors Q152 and Q153 comprise the charge pump that serves as the current source to increase or decrease the

amount of charge on loop filter capacitor C150. Capacitor C150 and resistor R156 form the loop filter that controls the stability and response of the VCO feedback loop. Transistor Q150 serves to limit the voltage on the U115 $\overline{UP}$ line to 5 V dc.

4.3.1.6.3 The dc output from the charge pump is filtered by reisistors R157 and R158; capacitors C151 and C152; and inductor L127. The filter removes undesireable noise and variations from divider/phase detector U115 that would otherwise modulate the VCO. The filtered dc VCO steering line voltage is applied to the VCO to adjust its frequency.

4.3.1.7 Frequency Shift Logic Circuit

4.3.1.7.1 The *DVP MCX100* radio set provides extended frequency coverage in two ranges: 136 to 162 MHz (Range I) and 146 to 174 MHz (Range II). To allow the VCO to operate within this wide frequency band, the two frequency ranges are divided into two sub-ranges. For Range I, the VCO operating sub-range is 114.6 to 162.0 MHz. For Range II, the VCO operating sub-range is 124.6 to 174.0 MHz. To select the proper VCO sub-range, the frequency shift logic circuit develops 16 discrete switching conditions on six data lines. The data lines control PIN (diode) switches in the VCO hybrid that switch (shift) the VCO to the proper sub-range frequency. The VCO is shifted up or down in increments of 6.2 MHz, 12.4 MHz, or 24.8 MHz.

4.3.1.7.2 The frequency shift logic circuit consists of transistors Q171 and Q172, and IC U171. The circuit is controlled by the $\overline{VCO1}$, $\overline{VCO2}$, and $\overline{S1}$ data outputs from divider/phase detector U115, the frequency and shift information is initially stored in the PROM and is transferred into U115 as a four-bit word.

4.3.1.7.3 The $\overline{VCO1}$, $\overline{VCO2}$, and $\overline{S1}$ data outputs from U115 develop corresponding frequency range shift signals, designated S3, S2, and S1, respectively, used to control the frequency shift. Each frequency range switch signal, in turn, consists of complimentary logic outputs. Logic outputs S3, and $\overline{S3}$ control the 6 MHz shift. Logic outputs S2 and $\overline{S2}$ control the 12 MHz shift, and logic outputs S1 and $\overline{S1}$ control the 24.8 MHz shift. Transistors Q171 and Q172 generate the S3 and $\overline{S3}$ logic outputs, whereas U171 generates the remaining logic outputs. When a logic output is high, it is at +8 V dc. When it is low, it is at ground. The logic outputs are applied on the six data lines to the PIN switching decodes to shift the VCO to the proper sub-range frequency.

4.3.1.7.4 Depending on the frequency shift selected, the dc voltage on the VCO steering line (between +3 and + 8 V dc) is shifted up or down by 5 V dc. Since the voltage level on the VCO steering line determines the VCO operating frequency within the sub-range, the frequency shift changes the VCO operating frequency accordingly. An increase in the VCO steering line voltage increases the VCO operating frequency. Conversely, a decrease in the VCO steering line voltage decreases the VCO operating frequency.

4.3.1.7.5 Table 1 tabulates the eight descrete switching conductors outputted by the frequency shift logic circuit. For each switching condition, the table shows the logic states of the S1, S2, and S3 frequency range select signals, and the sub-range frequency at which the VCO is operating.

Table 1.
Frequency Shifting of VCO Sub-Range Frequencies

Switching Condition	Frequency Range Select Signals S1	S2	S3	VCO Sub-Range Range I	Range II
1	0	0	1	114.6 to 120.595	124.6 to 130.595
2	0	0	0	120.6 to 126.595	130.6 to 136.795
3	0	1	1	126.6 to 132.495	136.8 to 142.995
4	0	1	0	132.5 to 138.395	143.0 to 149.195
5	1	0	1	138.4 to 144.295	149.2 to 155.395
6	1	0	0	144.3 to 150.195	155.4 to 161.595
7	1	1	1	150.2 to 156.095	161.6 to 167.795
8	1	1	0	156.1 to 162.0	167.8 to 174.0

4.3.1.8 VCO Buffers And Transmit/Receive Injection Switch

4.3.1.8.1 The VCO Buffers and transmit/receive injection switch route the rf output from the VCO to either the transmit or receive injection ports on the synthesizer board. The VCO buffers isolate the VCO tank circuits from varying loads and noise generated by the transmit/receive switch.

4.3.1.8.2 The VCO buffers consist of transmit/receive buffer Q190 and divider rf buffer Q192. The rf output from the VCO is applied to the base of Q190. The amplified VCO rf is then applied to the anodes of PIN diodes CR190 and CR191. Diode CR190 is in the transmit injection line and diode CR191 is in the receive injection line. Depending on the biasing of the diodes, amplified VCO rf is switched to either the transmit or receive injection line.

4.3.1.8.3 The biasing of the diodes is controlled by transmit/receive injection switch Q191. When the transmitter is keyed, the 9.6T keying voltage is applied to the cathode of CR190 and to the base of Q191. The 9.6T applied to CR190 forward biases the diode, switching the amplified VCO rf to the transmit injection port. From this port, the signal is applied as the 136 to 174 MHz transmitter injection signal to the low level amplifier in the transmitter. The 9.6T voltage applied to Q191 turns on Q190, effectively reverse-biasing CR191. In the absence of the 9.6T keying voltage (signal low) the reverse action takes place. Diode CR191 becomes forward biased, switching amplified VCO rf to the receive injection port. The output is the 114.4 to 152.6 MHz receive injection signal that is routed to the mixer in the receiver.

4.3.1.8.4 The amplified VCO rf output from Q191 is also applied to divider rf buffer Q192. The

output from Q192 is a buffered VCO rf signal that is applied to the loop divider in divider/phase detector U115 to generate the loop frequency signal.

4.3.1.9 VCO AGC Circuit

The VCO AGC circuit provides a constant rf level in the VCO tank circuit. The VCO AGC circuit consists of transistors Q188 and Q189. A rectified dc sample of the VCO rf output is applied as the AGC detect signal to the base of Q189. If the level of the signal increases, indicating a rise in the VCO rf output, Q189 conducts more, causing a corresponding decrease in the current flow through current driver Q188. Since the collector output of Q188 is the AGC control signal coupled to the source of the VCO FET, the decreased AGC control curent reduces the VCO tank voltage to offset the increased rf output. Conversely, a corresponding decrease in the VCO rf level would cause the AGC control signal to rise, increasing the VCO tank voltage and raising the VCO rf level.

4.3.2 VCO Hybrid Circuits

(Refer to Synthesizer schematic diagram)

The VCO hybrid circuits are functionaly arranged into the VCO steering line, the PIN (diode) switches, the VCO modulator, and the VCO.

4.3.2.1 VCO Steering Line

4.3.2.1.1 The dc voltage on the VCO steering line determines the operating frequency of the VCO within the sub-range selected by the frequency shift logic circuit. The steering line output is determined by the $\overline{UP}$ and DOWN pulses generated by divider/phase detector U115 (on the synthesizer board), and which is converted and filtered to a dc voltage by the charge pump and loop filter circuit (also on the synthesizer board). The dc voltage is applied to the network of varactor diodes that control the frequency of the VCO. When the VCO frequency is not equal to the desired frequency, the dc voltage on the VCO steering line steps to another level to change the VCO operating frequency. When the VCO locks to the desired frequency, the VCO steering line maintains a constant voltage level.

4.3.2.1.2 The varactor diode network consists of CR1301 through CR1304. Capacitor C1307 couples the varactor network to the VCO tank circuit, via the VCO transmission line. The varactor network is configured to prevent high level rf from the VCO transmission line from being rectified by the varactor diodes. This eliminates noise that might otherwise modulate the VCO.

4.3.2.1.3 The capacitance of the varactor diodes determines the reactance of the VCO tank circuit, and therefore the operating frequency. The dc voltage level present on the VCO steering line determines the capacitance of the varactor diodes. Variations in their capacitance therefore change the VCO tank circuit reactance, varying the VCO operating frequency. The range of levels present on the VCO steering line extends from +3 to +8 V dc. An increase in VCO steering line voltage causes the capacitance of the varactor diodes to decrease and the VCO frequency to increase. Conversely, a decrease in VCO steering line voltage causes an increase in the capacitance of the varactor diodes and a reduction of the VCO frequency.

4.3.2.2 PIN (Diode) Switches

4.3.2.2.1 The PIN diodes switch the VCO to the proper sub-range operating frequency by removing or inserting capacitive or inductive elements of the VCO tank circuit, via the transmission line. When the PIN diodes are off (reverse biased), they effectively create an rf open circuit between the capacitive or inductive elements and the transmission line. When the PIN diodes are on (forward biased), they effectively create an rf short circuit to the transmission line, inserting the capacitive or inductive elements into the VCO tank circuit. Inserting capacitive elements decreases the VCO operating frequency. Inserting inductive elements increases the VCO operating frequency.

4.3.2.2.2 The PIN diodes are controlled by the 6.2 MHz, 12.4 MHz, and 24.8 MHz frequency range shift signals generated by the frequency shift logic circuit on the synthesizer board. The 6.2 MHz shift is initiated by the S3 frequency range shift signals S3 and $\overline{S3}$. When the S3 line is low (ground) and the $\overline{S3}$ line is high (+8 V dc), PIN diode CR1306 is reverse biased. This effectively uncouples capacitor C1300 from the VCO tank circuit. When the logic states of the S3 and $\overline{S3}$ lines change, CR1306 becomes forward biased, effectively inserting C1300 into the VCO tank circuit. This decreased capacitance causes the VCO frequency to shift upwards by 6.2 MHz.

4.3.2.2.3 PIN diode CR1320 controls the 12.4 MHz shift by removing or inserting inductor L1309 and a short, series-connected transmission line to the VCO tank circuit. The 12.4 MHz shift is initiated by the S2 frequency range shift signals S2 and $\overline{S2}$. When the S2 line is high and the $\overline{S2}$ line is low, inductor L1309 and the short transmission line (an inductive element) are inserted into the VCO tank circuit. This parallel inductance shifts the VCO frequency up by 12.4 MHz.

4.3.2.2.4 PIN diodes CR1340 and CR1341 control the 24.8 MHz shift, which is initiated by the S1 frequency range shift signals S1 and $\overline{S1}$. Before the 24.8 MHz shift is initiated, the S1 line is low and the $\overline{S1}$ line is high. This turns on CR1340, effectively short circuiting a second VCO transmission line to rf ground, via capacitor C1340 and C1325. This removes the second VCO transmission line from the VCO tank circuit, and prevents it from resonating due to stray capacitance to prevent noise from being introduced into the VCO tank circuit. When the 24.8 MHz frequency shift is activated,

the S1 line goes high and the $\overline{S1}$ line goes low. This turns on diode CR1341, connecting the two VCO transmission lines together, via capacitors C1340 and C1341. This effectively shortens the VCO transmission line, decreasing the inductance of the VCO tank circuit, and thus shifting the VCO frequency up by 24.8 Hz.

4.3.2.2.5 Because of coupling losses between the VCO tank circuit and shifting elements during shifts (approximately 6 MHz), compensation must be provided. To reduce the coupling loss when the 12.4 MHz shift is initiated while a 28.4 MHz shift is in effect, compensating diode CR1312 is provided. When the S1 line controlling the 24.8 MHz shift is high and the $\overline{S1}$ line is low, diode CR1312 is turned on. This effectively disconnects the short transmission line from inductor L1309.

4.3.2.2.6 Capacitor C1302 provides steering line compensation for S1 shift. The varactor diodes and capacitor C1307 are connected to one side of the transmission line. Sensitivity of the varactor diodes is reduced when the S1 transmission line is added to the VCO tank. With capacitor C1300 in parallel with C1307, the sensitivity of the varactors to the VCO is maintained.

4.3.2.3 VCO Modulator

4.3.2.3.1 The VCO is modulated by the VCO modulation signal (transmit audio signal) supplied by the transmitter circuits. The VCO modulation signal carries microphone audio (and PL or DPL signals, if present) whose frequencies are above 50 Hz. (Frequencies below 50 Hz are on the VCO reference signal supplied only to the 2 PPM 14.4 MHz reference oscillator on the synthesizer board.) The VCO is modulated with the VCO modulation signal by varactor diode CR1300. The VCO modulation signal increases and decreases the capacitance of CR1300, thus changing the frequency of the VCO (direct frequency modulation).

4.3.2.3.2 Because the VCO can operate over a wide range of frequencies, the sensitivity of the VCO is subject to slight drifting. This is due to changes in the VCO steering line voltage, or to coupling losses that occur in the VCO tank circuit when the PIN diode switches shift the VCO to a new sub-range frequency. To compensate for this drift, and to maintain the modulation level constant throughout the range of the VCO frequencies, compensation is provided for the VCO steering line voltage and for frequency shifts. To compensate for changes in the VCO steering line voltage, a second varactor is used. This varactor CR1305, is connected in series with varactor CR1300 and the VCO steering line. As the VCO steering line voltage changes, the capacitance of CR1305 changes, thus altering the capacitance in the VCO tank circuit.

4.3.2.3.3 To compensate for frequency shifts, the dc bias on varactor CR1300 is varied. This is accomplished by a modulation compensation network composed of resistors R1310, R1311, and R1312; and diodes CR1307, CR1308, and CR1309. The network is controlled by the S1, S2, and $\overline{S3}$ frequency range shift signals. Depending on the logic states of these signals, the dc bias on CR1300 changes, changing the varactor sensitivity to audio levels.

4.3.2.4 VCO

4.3.2.4.1 The VCO generates frequency modulated transmit injection and stable receive injection frequencies. The operating frequency range of the VCO extends from 21.4 MHz below the radio operating frequency (to provide low-side receiver injection at the lowest radio operating frequency) continuously to the highest radio operating frequency. The VCO also provides a feedback signal at the injection frequency that is used by divider/phase detector U115 on the synthesizer board to generate the loop frequency signal.

4.3.2.4.2 Transistor Q1300 is the amplifying element of a grounded-gate oscillator. The oscillator operates in the VHF frequency band at the desired injection frequency. The drain of Q1300 is coupled to a microstrip transmission line through capacitor C1308.

4.3.2.4.3 The VCO tank circuit is composed of capacitors C1309, C1313, and C1327; the transmission line; and the capacitive and inductive elements inserted into, or removed from, the VCO tank circuit by the PIN switching diodes. The transmission line serves as the inductive component of the VCO tank circuit. Microstrip plates attached to the tranmsission line act as tuning capacitors on the VCO tank circuit. Factory-tuned tuning jumpers R1 and R2 are also attached to the transmission line to tune the VCO tank circuit.

4.3.2.4.4 The VCO rf output signal from the tank circuit is coupled through capacitor C1308 to the transmission line. The rf passes through the transmission line and is coupled into the VCO output buffer Q1330, via capacitor C1330. The output buffer feeds the VCO rf signal to the transmit/receive rf buffer on the synthesizer board. The rf signal present at this point is either a low-side receiver injection signal 21.4 MHz below the receiver operating frequency, or a transmitter injection signal at the desired transmitter operating frequency.

4.3.2.4.5 An AGC circuit is used to maintain constant rf levels in the VCO tank circuit to ensure consistent sideband noise characteristics across the entire frequency band. A sample of the VCO rf signal is rectified by diode CR1310 to provide a dc voltage with level proportional to the VCO rf level. The rectified dc voltage is applied to the AGC circuit on the synthesizer board. the AGC circuit returns a dc control voltage that maintains the VCO tank voltage constant (approximately 3 V rms).

4.4 *FAST-LOK* FREQUENCY SYNTHESIZER CIRCUIT

The *Fast-Lok* frequency synthesizer consists of the channel selection and display circuits, the synthesizer board circuits, the synthesizer output amplifier circuit, and the VCO hybrid circuits. The channel selection and display circuits, which include the front panel channel selector switch and LED display, are covered in the functional description of the standard lock frequency synthesizer circuits and are not detailed here.

4.4.1 Synthesizer Board Circuits

NOTE

Except for the divider U115 and phase detector U140 circuit descriptions, the following descriptions refer to the schematic diagrams in the *Fast-Lok* Frequency Synthesizer section.

4.4.1.1 14.4 MHz Reference Oscillator

The 14.4 MHz reference oscillator provides a stable (±2 ppm) reference for the frequency synthesizer. The oscillator is completely self contained and non-servicable. During transmit operation, low frequency (below 50 Hz) *DVP* or DPL signals (ref mod) are routed directly to the oscillator. This is required because the divider/phase detector (U115/U140) can track low-frequency modulation, to prevent direct low-frequency audio (used in *DVP* and DPL signaling) from modulating the VCO.

4.4.1.2 Frequency Select PROM

Frequency selection data (factory or field programmed) in the PROM is addressed by five binary bits from the channel selector switch via five address lines, A0 through A4. The five bits comprise the channel select word.

NOTE

On the synthesizer schematic diagram, use the address line designations on the outside of the U116 symbol. The designations inside the symbol do not correspond to the channel select address lines.

Frequency selection in the PROM is further determined by the presence or absence of transmitter keying signal, 9.6T, at pin 5 of the PROM as follows:

- Presence of 9.6T: data words specify transmit frequency
- Absence of 9.6T: data words specify receive frequency

Data words transfer from PROM U116 to divider U115, when a +5 volt enable signal at pin 16 (VCC) coincides with arrival of a word select signal (three address bits, A0-A2) from the divider. Frequency data is transferred to the divider by six 4-bit words on data lines D0 through D3.

4.4.1.3 PROM Enable Circuit

4.4.1.3.1 The PROM enable circuit allows divider U115 to address the PROM when any of the following occur:

- The transmitter is keyed.
- The frequency is changed.
- The synthesizer goes out of lock.

If the transmitter is keyed or the frequency is changed, frequency change detector U351 on the front panel interconnect board emits a positive going pulse of approximately 5 usec duration. This pulse is sensed at phase detector U140-5 and causes the phase detector ADAPT output (U140-10) to go high. If the synthesizer goes out of lock, circuitry within phase detector U140 senses the out-of-lock condition and causes the $\overline{\text{ADAPT}}$ output (U140-7) to go low.

4.4.1.3.2 The PROM enable circuit consists of a portion of phase detector U140 as well as transistors Q115, Q117 and Q118. Transmit PTT, frequency change, or synthesizer out-of-lock causes phase detector ADAPT output U140-10 to go high. This turns on Q117, providing low $\overline{\text{READ ENABLE}}$ signal to divider U115-28. With the $\overline{\text{READ ENABLE}}$ input activated, U115 applies a 10 microsecond low $\overline{\text{STROBE}}$ signal that recurs every 200 microseconds. The low $\overline{\text{STROBE}}$ signal turns on Q118. When Q118 turns on, it turns on Q115, and when Q115 turns on, it supplies +5 V dc enabling voltage to the Vcc pin of the PROM. With the PROM enabled, frequency data is read from the PROM to the divider U115.

4.4.1.3.3 At the end of the three millisecond adapt interval the phase detector ADAPT output goes low. This turns off Q117, disabling the $\overline{\text{READ ENABLE}}$ input to U115. With the $\overline{\text{STROBE}}$ output disabled, power is removed from the PROM.

4.4.1.4 Lock Detect Switch Circuit

4.4.1.4.1 The lock detect switch monitors the $\overline{\text{ADAPT}}$ output from phase detector U140. When the $\overline{\text{ADAPT}}$ output is high, the synthesizer is locked onto the correct frequency, and when it is low, the synthesizer is out-of-lock. When the synthesizer goes out-of-lock, the lock detect switch supplies a high LOCK DETECT signal to disable the transmitter (during the transmit mode) or to disable the receiver (during the transmit mode) or to disable the receiver (during the receive mode).

4.4.1.4.2 The lock detect switch consists of inverter Q142. The LOCK DET TRIGGER signal is

developed at the collector of Q142. The LOCK DET TRIGGER signal is routed through CR351 to become the LOCK DET signal for the radio set.

4.4.1.5 Divider

(Refer to functional diagram in Synthesizer section.) The divider contains the following circuits:

- multiplex control
- six 4-bit latches
- loop divider (programmable)
- reference divider (programmable)

4.4.1.5.1 Multiplex Control

The multiplex control circuit performs three functions:

- Three address bits on lines AO through A2 select 4-bit words in the PROM. The selected 4-bit words containing frequency data are transferred from the PROM to the six 4-bit latches.

- An ENABLE signal initiates generation of 10 microsecond $\overline{\text{STROBE}}$ signals that reoccur every 200 microseconds.

- Produces a LATCH CONTROL signal that determines which data words are stored in each of the six latch registers.

4.4.1.5.2 Latch Circuits

4.4.1.5.2.1 The six 4-bit latches are activated by a latch control when the multiplex control circuit receives the active (low) enable signal from the PROM enable circuit.

4.4.1.5.2.2 The information stored in the six 4-bit latches determines the values (A and B) for the counters in the loop divider. The stored information also determines the output levels of the $\overline{\text{SO}}$, $\overline{\text{VCO1}}$, and $\overline{\text{VCO2}}$ signals appearing at pins 17, 19, and 20, respectively, of U115. These signals are applied to the frequency shift logic circuit to determine at which sub-range the VCO operates.

4.4.1.5.2.3 The $\overline{\text{S1}}$ signal from the latch registers, appearing at pin 18, is used only with dual front end receiver models. The signal is used to select one of two 6 MHz filters at the front end of the receiver. When the $\overline{\text{S1}}$ signal is low, the low range 6 MHz filter is switched into the rf signal path. When the $\overline{\text{S1}}$ signal is high, the high range 6 MHz filter is switched into the rf signal path.

4.4.1.5.3 Loop Divider

The loop divider contains a double-programmable dual modulus counter. The counter acts as a programmable divider for the VCO rf feedback signal from the VCO output by dividing by 64 for a programmable number of (A) cycles, and then by 63 for another programmable number of (B) cycles. Divider rf buffer Q116 isolates the VCO rf feedback signal from the divider. The loop divider divides the VCO feedback signal by 64 "A" times and by 63 "B" times. The output of the loop divider counters is the loop frequency signal that is applied as the second input to the phase detector. The loop frequency signal is the VCO output signal frequency divided by (64A plus 63B).

4.4.1.5.4 Reference Divider

The reference divider divides the 14.4 MHz signal from the reference oscillator to any of three reference frequencies: 4.166 kHz, 5.0 kHz, or 6.25 kHz. These frequencies are determined by the channel spacing of the *DVP MCX100* radio set. The reference frequency is applied as one input to the phase detector.

4.4.1.6 Phase Detector
(Refer to functional diagram)

4.4.1.6.1 Phase detector U140 compares the reference and loop frequency outputs of the divider circuit and uses this information to generate a dc output signal that controls the VCO frequency. The phase detector also monitors the frequency change (FC) line and uses this information to generate control signals for the adaptive filter.

4.4.1.6.2 The phase detector output signal level is controlled by the length of time between the positive transition of the reference signal and the positive transition of the loop signal. When the reference signal goes high (at U140-2), the ramp generator (Q140) turns on, maintaining a constant current through C142. This constant current generates a linear rise (ramp) in the voltage at U140-24. The rise of the ramp voltage halts when the LOOP signal (at U140-23) switches to a high level, causing Q140 to turn off.

4.4.1.6.3 The positive transition of the loop signal, in addition to halting the ramp generator, resets an internal sample timing circuit. The ramp voltage is held constant for a period of time determined by the sample timing capacitor, C141. During this time, the two hold capacitors (C143 and C144) are charged to a level determined by the ramp voltage. At the end of the sample time, ramp capacitor C142 is discharged in preparation for the next cycle.

4.4.1.6.4 The accumulated charge on the hold capacitors is used to control the conduction of a push-pull output driver. The output driver consists of an internal NPN transistor and an external PNP transistor controlled by the signal at U140-17. The PHASE DET OUTPUT signal at U140-15 is coupled, via the adaptive loop filter, to the VCO, where it controls the generation of injection frequencies.

4.4.1.6.5 In addition, the phase detector generates the control signals for the adaptive filter and PROM enable circuits. When changing operating channels while in the receive mode or changing from the transmit mode to the receive mode, the FC pulse (at U140-5) causes the ADAPT line to go high and the $\overline{\text{ADAPT}}$ line to go low for approximately 3.0 milliseconds.

4.4.1.6.6 To achieve maximum switching speed, the $\overline{\text{SO}}$, $\overline{\text{VCO1}}$, and $\overline{\text{VCO2}}$ signals must shift the VCO subrange coincident with the rising edge of the loop (divided VCO) pulse at U140-23. $\overline{\text{VCO1}}$ and $\overline{\text{VCO2}}$ are synchronized to the loop pulse internally within divider U115. The $\overline{\text{SO}}$ output of divider U115-17 is fed to the input of a D flip-flop within phase detector U104-11. This flip-flop is clocked by the loop pulse, allowing its output to respond to an $\overline{\text{SO}}$ change only at the rising edge of the loop pulse. The synchronized $\overline{\text{SO}}$ flip-flop output U140-6 is fed to frequency shift driver U155-10.

4.4.1.7 Adaptive Loop Filter

4.4.1.7.1 The adaptive loop filter is a low-pass filter in the steering line between the phase detector and the VCO. This filter removes noise and variations in the steering line level to prevent unwanted modulation of the VCO.

4.4.1.7.2 The adaptive filter, which is connected to the PHASE DET OUTPUT line (U140-15) is controlled by the phase detector to operate in either of two modes. Each mode requires different filter characteristics, and these characteristics are changed by transmission gates which switch filter components into and out of the steering line signal path, as determined by the phase detector.

4.4.1.7.3 When the synthesizer is in the normal transmit or receive mode, the phase detector drives $\overline{\text{ADAPT}}$ high, turning off Q143. All four transmission gates (U141A, B, C, D) are off. The natural loop frequency of the synthesizer in this mode is approximately 35 Hz. The adaptive loop filter stays in this mode as long as the radio is transmitting or receiving. In this mode the steering line is filtered by R147, a shunt path consisting of R148, C145 and C146, and by R149 and C147. The signal passes to the VCO via RF filter L143 an C147.

4.4.1.7.4 When the synthesizer is in the Adapt mode, the phase detector drives $\overline{\text{ADAPT}}$ low, turning on Q143. This causes the collector of Q143 to go high, turning on all four transmission gates U141A, B, C, D. The synthesizer has a high natural loop frequency in this mode allowing it to change frequencies rapidly. The adaptive filter switches into this mode for approximately 3.0 milliseconds as the radio changes from the transmit mode to the receive mode or from one receive frequency to another (for example, when changing the operating channel of the radio). In the adapt mode, the greater part of the adaptive loop filter is shorted by transmission gate U141A, and the phase detector output is connected to C147. When the filter is in the Adapt mode, C146 and C147 are being charged. The accumulated charge on C147 prevents the VCO from changing frequencies while the mode is changed from adapt to normal receive/transmit operation. C147 always remains connected to the steering line. The signal passes to the VCO via the RF filter comprised of L143 and C159.

4.5 *DVP* CIRCUITS

(Refer to *DVP* schematic diagram)

The electrical circuits of the *DVP* control boards are subdivided into the following: power supply and regulator, clock, receive audio, squelch, push-to-talk (PTT), transmit audio, key insertion, and mode control circuits.

4.5.1 Power Supplies and Regulators

Three different voltage suplies are used on the *DVP* boards. Regulated 9.6 volts powers most of the *DVP* circuitry and comes from the radio 9.6 V regulator circuitry, via P352-6. SW A+ powers the front panel indicator LEDs and comes from P364A-5. PA A+ powers the 5 volt regulator (U101) and comes from P352-8.

4.5.2 Clock

The clock generating circuitry is contained within U102, the *DVP* Control and Interface I.C. This I.C. contains a high frequency oscillator, a prescaler, and a phase-locked loop for frequency generation and division. Crystal Y101 at pins 17 and 19 maintains the oscillator frequency at 3,072 kHz. This frequency is divided by 256 in the prescaler and phase-locked loop to produce the system 12 kHz clock. The prescaler divides by 4, and the phase-locked loop divides by either 63, 64 or 65 depending on whether incoming data transitions are late, absent, or early with respect to the system 12 kHz clock. The 12 kHz clock output of the phase-locked loop keeps the CVSD (U103) and the encryption hybrid (HY101) synchronized for *DVP* functions.

4.5.3 Receive Audio

4.5.3.1 The buffered discriminator output is routed to the *DVP* board via P352-7 and J101-5. If the discriminator output is not a *DVP* signal, it is gated through U105C to buffer U107D and back to the radio audio path via J101-7. The discriminator data also goes to the *DVP* equalizer filter which is formed by U107B and an amplifier contained in U102 (between pins 3 and 5). The filter shapes the eye pattern to create a greater eye opening at U102-5. In general, the eye opening at U102-5 should be about 10% more than the eye opening of the incoming discriminator data.

4.5.3.2 Pin 5 of U102 is internally connected to a limiter whose output is on U102-6. This output swings between supply voltage and ground. Feedback from the limiter to the amplifier input through R120 gives a small amount of hysteresis that causes small crossover distortions on the amplifier output on U102-5. This positive feedback prevents any clock synchronous noise from causing false code detects on very quiet standard mode signals. In addition, switched bias output on U102-8 turns off when code is detected and turns on when no code is detected. This allows the amplifier and limiter to quickly adapt to off channel signals and lowers the initial error rate. This output goes through R121 to modify the voltage on C106. All the dc voltages on U102-3, 4, 5, and 6 are within 0.1 volt of each other, and they are biased internally to half the supply voltage.

4.5.3.3 The limiter output of U102 is internally used to synchronize the clock and operate the code detector. The clock is synchronized with a digital phase-locked loop which effectively divides an internal 64 X clock signal by 63, 64, or 65 depending on whether the limiter transitions are late, absent, or early respectively. This produces a 12 kHz clock on U102-23 which clocks the encryption hybrid (U8) and the CVSD (U7). The clock maintains board synchronization. If the clock should fail for any reason, much of the rest of the *DVP* circuitry becomes inoperable.

4.5.3.4 The clock is used inside U102 to reclock the limiter output at the center of the bits. This signal is called receive cipher and comes out of U102-10. This cipher text goes into the encryption hybrid on HY101-9. HY101 decrypts the cipher and outputs plain text on HY101-15. The plain text goes to the CVSD, U103-10.

4.5.3.5 The CVSD reconstructs the audio by low pass filtering the plain text with an internal FIR filter and multiplying the result by the step size voltage on U103-6. The step size is determined by an internal detector that increases the step size when 3 zeros in a row are detected or when 3 ones in a row are detected. This condition is referred to as slope overload and indicates that the step size is too small. The reconstructed audio output goes out U103-15 to analog switch U105C.

4.5.3.6 The audio gate (U105C) then switches either buffered discriminator or CVSD receive audio back into the radio audio path via J101-7.

4.5.4 Squelch

4.5.4.1 The squelch circuit consists of the *DVP* Interface and Control IC (U102), the CVSD (U103) detector, U106A and U106B. The majority of the squelch circuit is in U102 and consists of two detectors. These detectors are called phase-lock and correlation. The phase-lock detector measures the synchronization of the limiter output with the 12 kHz clock. There will be a phase-lock indication for most periodic signals, EOM, and cipher. The correlation detector measures the randomness of the limiter output. Most standard mode signals are correlated as are most tones and EOM. With these two detectors, U102 can determine the kind of discriminator signal being received.

4.5.4.2 The proper code detector in U103 is another correlation detector which measures the correlation of the received plain text. For signals which decrypt to produce intelligible plain text, the degree of correlation will be high; and the detector output on U103-14 will go high. For signals that are noisy or decrypted with the wrong key, the degree of correlation is low; and U103-14 is low. This signal goes to U102-28 and is used in the squelch decision. The PL disable input at U102-2 also affects the squelch decision. If this pin is high, U102 will ignore the CVSD proper code detector signal, and will unsquelch for all coded signals. U102-2 will be high if the radio is not configured for proper code, or if the microphone is off-hook, or if the monitor switch (in radios so equipped) is depressed. Two other signals also affect the squelch output (pin 14) of U102. These are: 1) the squelch input from the carrier squelch or PL circuitry, and 2) an input from the *DVP* drop out timer on pins 12 and 13 of U102. The input from the carrier squelch or PL circuitry goes to U107A via P352-12 and J101-9. U107A is configured as a comparator so that the squelch input at U102-22 will be a digital signal. This input tells U102 what state the standard radio squelch is in.

4.5.4.3 Once U6 has determined the type of signal at the discriminator, it can set its squelch output, U102-14. If the signal is not coded, U102 will squelch or unsquelch the radio according to its input from the standard radio squelch (U102-22). If the signal is *DVP* code then the outputs from U102 will be affected by the drop out timer, PL disable, and the proper code input from U103. When a private mode message is received, (U102-15) will go high. U102-16 and U102-14 outputs will go high if either the PL disable input is high, or if proper code is detected by U103. In addition, the drop out timer is activated by charging up C124 on U102-12. If EOM id detected, the drop timer is cancelled by discharging C124, U102-15 output stays high, U102-16 and U102-14 will go low. If noise is detected, the drop out timer is delayed by allowing C124 to discharge through R126. During the delay, U102-15 remains high. U102-14 and U102-16 will stay high if either the PL disable is high or proper code is detected. This drop out delay provides fade protection for private mode signals. When the drop out timer times out, U102-14, U102-15 and U102-16 will go low. When a standard mode message is detected, both U102-15 and U102-16 will go low, and the drop out timer is cancelled by discharging C124.

4.5.4.4 U106A and U106B form the last stage of the *DVP* squelch circuitry. These two gates perform the following functions: 1) remove squelch tails after a *DVP* signal has been received, 2) provide a

means for option accessories to control the radio squelch while the radio is receiving a *DVP* transmission, and 3) allow verification tone to be heard during key insertion. U106-6 is the *DVP* squelch output and this is routed back to the radio squelch circuit via P101-16 and J1003.

4.5.5 Push-To-Talk (PTT) Circuitry

4.5.5.1 The PTT circuitry on the *DVP* board consists mainly of U108, Q103, Q104 and part of the interface and control IC (U102). When an active PTT occurs, the PTT flow on the *DVP* board will depend on whether the radio is set to standard or private transmit mode.

4.5.5.2 In standard transmit mode the following actions occur. U108-4 will go low, causing U108-3 and U108-6 to go high. When U108-6 goes high, U108-5 will go low and turn Q112 on. The emitter of Q112 is connected to the radio PTT circuitry, via P352-3, and causes the transmitter to key. When the PTT is released, Q112 turns off, causing the transmitter to turn off.

4.5.5.3 When the radio is in the private transmit mode, the following actions will occur. U108-4 will go low, causing U108-3 to go high, and U108-1 to go low. This supplies an active low PTT to U102-11, causing U102 to be set to transmit mode. U102-18 will then go high, causing the following actions: 1) analog switches U105A and U105B will be set so that *DVP* cipher is sent back into the transmit path, 2) Q111 turns on and its emitter goes high, 3) the collector of Q113 goes low and puts the encryption hybrid (HY101) into transmit mode, 4) U108-7 goes high. The emitter of Q111 is connected via P101 and J1004 to the PL encode filter (if radio is PL equipped). When this signal goes high, it prevents the PL filter from sending PL tones into the transmit path. This is prevented because the PL tones would interfere with the *DVP* cipher being transmitted. When U108-7 goes high, U108-5 will go low and turn on Q112. This causes the transmitter to key. When the active PTT is released, U102-11 will go high. This causes U102 to stop sending cipher and to start sending EOM. U102-18 is sustained high for an additional 180 milliseconds while EOM is being transmitted. After EOM, U102-18 will go low, causing the transmitter to turn off.

4.5.6 Transmit Audio

4.5.6.1 When the radio is set to standard mode, IDC audio comes in via J1001 and J101-15. It then goes through transmission gate U105B and right back into the transmit path via J101-18 and J1002.

4.5.6.2 When the radio is set to private mode, the IDC audio goes to an amplifier on U103 (the CVSD). The CVSD transmit circuit consists of an amplifier from U103-1 to U103-18 followed by a limiter output on U103-16. The limiter output is reclocked through a 3-bit decision rule register to control the compand output on U7-7. The compand output is integrated by R144 and C114 to make the step size voltage which goes in on U103-6. The step size is modulated by the limiter output to create the pulse amplitude modulated (PAM) output on U103-5. The PAM output is compared to the mic amplifier output by the feedback through R153 and C116. The result of the loop is that the PAM output is a digital reconstructed version of the mic amplifier output. The CVSD amplifier output on U103-18 is therefore the amplified difference between mic audio and reconstructed mic audio. The TX DATA on U103-8 is a reclocked limited version of the error and the compand output on U103-7 which is just TX DATA after passing through the register for the 3-bit rule. TX DATA on U103-8 is the transmit plain text.

4.5.6.3 The transmit plain text goes into the encryption hybrid on HY101-17 where it is encrypted. The resulting cipher text comes out HY101-14. This goes through a splatter filter on U102-25 and comes out on U102-27. The splatter filter is carefully constructed to produce an eye pattern with no overshoot, 80% eye opening, and zero crossover jitter. The splatter filter runs on the splatter filter supply connected to U102-26. It is worth noting that EOM always comes out of the splatter filter except when transmitting cipher in the private mode.

4.5.6.4 The splatter filter output (U102-27) goes to two deviation control pots, R158 and R161. R158 controls the amplitude of signal sent back into the VCO modulation path and R161 controls the amplitude of signal sent back into the reference oscillator path. The wiper of R158 is coupled through C119 to buffer U107C. The output is U107C goes through transmission gate U105B and the VCO via P101-17 and J1002. The wiper of R161 goes to transmission gate U105A, then to the reference oscillator via P101-11 and P352-16. Note that with this circuit arrangement the private mode deviation is controlled by the *DVP* potentiometers and by the standard radio deviation adjustment potentiometers, R341 and R344. The deviation adjustment should therefore be carried out in two steps. First the standard mode deviation should be adjusted as it is done in a standard radio. The private mode reference oscillator adjustment should then be set by R161 so that the modulation is 4 Vp-p at the reference oscillator input (P355-7). Then the private mode deviation should be adjusted by turning R158 for 4 kHz of deviation.

4.5.7 Key Insertion

4.5.7.1 The key insertion circuit consists of the 5-pin key insert connector and the encryption hybrid (HY101). Three signal lines, one control and one ground line go into the 5-pin connector. The three signals are key insert data (KID), write enable bar ($\overline{WE}$), and key (KEY). The control line is key insert ground (KIG). KIG is connected to the ground wire in the key

insert cable that connects to the 5-pin connector. When the cable is connected the KIG line is pulled to ground and M1 on HY101 is grounded. For dual code radios, M1 is high for code 2 and low for code 1. For single code radios with a TRN6777B Encryption Hybrid, M1 must be pulled low. Since key insertion works on code 1, the KIG signal ensures reliable key insertion even for dual code radios.

4.5.7.2 The key insertion process is straight forward. The $\overline{WE}$ and KEY signals go directly into the encryption hybrid on HY101-4 and 8 respectively. When key bits are being transferred over the KEY line to the encryption hybrid, the $\overline{WE}$ line must go low to enable the write process in the encryption hybrid. For that interval, the clock must be synchronized with the key bits. The clock synchronization is done by sending KID to U102-3. KID swamps out the discriminator signal and goes through the phase-lock loop for clock synchronization. After the key has been inserted into the encryption hybrid, the code inserter sends an encrypted tone via the KID line to the hybrid. If the key insertion was successful, the hybrid will decrypt the tone and it will be heard in the speaker. The message "BEEP?" will then appear in the code inserter display to remind you to listen for the tone.

4.5.8 Mode Control Circuitry

4.5.8.1 The *DVP* mode controlling circuitry consists mainly of the *DVP* Control Board, the 6-pin connector J104, U109 and U110. The *DVP* Control Board sits just behind the radio front panel, beside the radio channel selector switch. It holds the switches and LED's necessary to control and indicate the mode of the *DVP* circuitry. U110A and U110B are used to buffer and "square-up" the signal coming from the switches on the *DVP* Control Board before it is applied to the clock inputs of U109. U109A and U109B are configured as toggle flip-flops, whose outputs will toggle from one state to the other whenever they are clocked. U109A controls the transmit mode of U102, and in radios equipped with the Dual Code option, U109B controls whether the encryption hybrid is in Code 1 or Code 2.

4.5.8.2 When the output of U109A is high, U102 will be set to private transmit mode, and when its output is low, U102 will be set to standard transmit mode. The output of U109A is changed by pressing and releasing S102 on the radio front panel. This sends a single clock pulse to U109A (via J104-6 and U110A) and causes the output of U109A to change state. This changes the transmit mode of U102. When the output of U109A is high, buffer U110B will apply a high to the base of Q106. Q106 then turns on DS123 (on the *DVP* Control Board) via J104-4, indicating that the radio is in private transmit mode.

4.5.8.3 In radios equipped with the Dual Code option, U109B controls whether the radio is in Code 1 or Code 2. When S101 is depressed, a single clock pulse is applied to the clock input of U109B (via J104-3 and U110D). This causes its output to change state, changing the encryption hybrid from Code 1 or Code 2 or vice-versa. When HY101-5 is high, the encryption hybrid will be set to Code 2, and the output of U110E will be high. This causes Q107 to turn on DS121 on the *DVP* Control Board (via J104-2), indicating that the encryption hybrid is in Code 2.

4.5.8.4 When the radio is receiving a private message, U102-15 will be high. This causes Q109 to turn on DS122 on the *DVP* Control Board (via J104-5), to indicate that a private message is being received.

4.6 PL/DPL CIRCUITS (Refer to PL/DPL Encoder/Decoder Schematic Diagram)

The operation of *Private-Line* or *Digital Private-Line* circuits is controlled by a single-chip, 8-bit, 40-pin microcomputer, U1705.The system uses a personality ROM preprogrammed in accordance with user-specified parameters. Software programming within the microcomputer controls the operation of the decoding, encoding, and microcomputer self-test circuits. The microcomputer is clocked by a 4 MHz oscillator, using externally-connected crystal Y1.

4.6.1 Decoding

The decoding process uses high and low-pass filters to separate the coded tones from the composite audio signal that is received. The coded tones are shaped into square waves and processed by the microcomputer and memory. If the received code corresponds to the preprogrammed code in the memory, the receiver audio circuit is unmuted. If the received code does not match the preprogrammed code in memory, the receiver audio circuit remains muted.

4.6.1.1 PTT Circuit

4.6.1.1.1 Decoding is in process at any time an active microphone PTT signal is absent at the base of inverter Q1703. When the PTT signal is absent (high), Q1703 turns on, developing a low at the collector. The low output is applied through diode CR1708 to inverter Q1710, turning it off. The output from Q1710 is the sidetone enable signal applied to the muting circuits in the receiver. When Q1710 is off, the sidetone enable signal is not grounded, allowing the primary and secondary mute gates on the main board to operate simultaneously.

4.6.1.1.2 The low output from Q1703 is also applied to pin 17 of the microcomputer, setting it to the receive mode. In the receive mode, the microcomputer outputs a low signal at pin 37 that turns off inverter Q1704. The output from Q1704 is the delayed PTT signal that is supplied to the *DVP* PTT circuits to key and unkey the transmitter. When Q1704 is off, the delayed PTT signal is high, unkeying the transmitter. Diode CR1709 prevents the high output from Q1704 from turning on inverter Q1710.

4.6.1.2 High-Pass Voice Filter

The option receive audio from the *DVP* circuits is applied along two paths. One path is through a two stage, high pass decode filter, hybrid HY1702, to remove the PL or DPL signaling tones from the option receive audio. The output from HY1702 is PL filtered audio containing voice only that is inserted into the receiver audio. The low output impedance of HY1702 allows direct connection to the receiver low-level audio path without requiring the use of jumpers.

4.6.1.3 Low-Pass Decode Filter

4.6.1.3.1 The second option receive audio path is through dual operational amplifiers U1701D and U1701A, which are configured as low pass filters. The filters attenuate frequencies above 200 Hz (noise and voice) allowing only the low frequency PL or DPL signals to pass. The filter provide a different cutoff frequency for PL tones or DPL signals: 220 Hz for PL tones and 140 Hz for DPL signals. The cutoff frequencies are determined by transistors Q1701 and Q1709, which are controlled in turn, by the signal level output at pin 36 of the microcomputer. When the microcomputer is set to the receive mode, pin 31 outputs one of two voltage levels: 0.05 V dc for PL tones or 3.9 V dc for DPL signals. Transistors Q1701 and Q1709 therefore respond accordingly to control the cutoff frequencies at the two filters.

4.6.1.3.2 The filtered output from second-stage filter U1701A is applied to operational amplifier/limiter U1701B to produce a square wave output signal. The square wave signal is inverted by an inverter stage in D/A (digital-to-analog) hybrid HY1701 and is applied to pin 16 of the microcomputer.

4.6.1.4 Receive Mute Control

4.6.1.4.1 The microcomputer, having encoded a valid code programmed by the code plug (or personality ROM), and having been set to the receive mode, produces a high output at pin 35. This turns on PL/DPL mute switch Q1702, causing a low signal to be applied to the input (pin 12) of non-inverting three-state buffer U1704. This IC can provide three output conditions, active high, active low, or an open circuit. The output from U1704 (pin 11) is the receive audio mute signal that is applied to the receiver audio to mute or unmute the audio. When the receive audio mute signal is high (a valid PL or DPL signal not received) the receiver audio is muted. When the signal is in the high impedance state, receiver audio muting is controlled by the carrier squelch circuit, allowing all signals on a channel to be heard. When the input to U1704 is low (indicating a valid code) the receive audio output from U1704 is also low, thereby unmuting the receiver audio and allowing only the valid PL or DPL message to be heard. The active-low output of U1704 overrides control of the audio mute line by the carrier squelch circuits, allowing signals to be heard even if below the carrier squelch opening threshold.

4.6.1.4.2 The receive audio mute signal can be set to the high impedence state (disabled) if either the front panel Monitor pushbutton is pushed on or if the microphone is off-hook. Normally with the Monitor pushbutton in the PL/DPL squelch model (out position), or the microphone on-hook, ground is applied to the disabling input (pin 15) of U1704. From the Monitor pushbutton, the ground is the monitor switch signal applied to pin 15 via diode CR1703. From the microphone, the ground is the hang-up switch signal applied through diode CR1704. The ground keeps U1704 enabled allowing only valid PL or DPL squelch signals to be monitored. Pushing in the Monitor pushbutton, or leaving the microphone off-hook effectively disables U1704. This sets its output to the high impedance state allowing all signals on a channel to be monitored.

4.6.2 Encoding

The encoding process uses preprogrammed codes stored in personality ROM. Coded digital bits are converted to low frequency analog code signals. The analog code signals modulate the VCO in the frequency synthesizer. Time-out timer and sidetone alert functions are also provided in conjunction with encoding.

4.6.2.1 PTT Circuit

Encoding is activated by the transmitter circuits when the push-to-talk button on the microphone is pressed. This supplies a low PTT signal to switch Q1703, turning it off. The high output developed by Q1703 is applied to pin 17 of the microcomputer, setting it to the transmit mode. The high output from Q1703 has no effect on the state of switch Q1710 (which is off at this time) due to the reverse bias of blocking diode CR1708.

4.6.2.2 Delayed PTT

When the microcomputer is set to the transmit mode, it responds by outputting a high signal at pin 37. This turns inverter Q1704 on, driving its delayed PTT output signal to ground, and keying the transmitter via the option del PTT signal to the *DVP* PTT circuitry. The ground output from Q1704 is also applied through diode CR1709 to inverter Q1710. Since Q1710 is already off at this time, the ground keeps Q1710 off. After a microcomputer-controlled delay time, which is coded by the personality ROM, the high output from pin 37 goes low. The delay time is either 150 milliseconds for PL signaling tones or 180 milliseconds for DPL signaling codes. After the programmed delay, the low output from pin 37 turns off Q1704, driving the delayed PTT output signal high and unkeying the transmitter. With the ground output from Q1704 removed from the base of Q1710, Q1710 turns on, driving its output low. This produces an active sidetone enable signal that is applied

to the volume control circuits in the receiver to unmute the audio.

4.6.2.3 Time-Out Timer

4.6.2.3.1 During encoding, software programming directs the microcomputer to enable the three data outputs that control the time-out time function. These outputs appear at pins 18, 19, and 26 of the microcomputer. The time-out time is determined by jumpers JU1, JU2, and JU3, and depending on whether they are in or out of the circuit. Up to seven time-out intervals can be preprogrammed, as shown in Table 2.

Table 2. Time-Out Selection

Jumpers			
JU1	JU2	JU3	Time-Out Timer
In	Out	Out	15 Seconds
Out	Out	Out	30 Seconds
Out	In	Out	60 Seconds
In	In	Out	90 Seconds
Out	Out	In	2-1/2 Minutes
In	Out	In	5 Minutes
Out	In	In	None

4.6.2.3.2 When the three data outputs are enabled, square wave pulses appear at the base of Q1705, producing a square wave output at its collector. A low pass encode filter network, composed of resistors R1715 and R1716, and capacitor C1711 converts the square wave pulses to an 800 Hz triangular waveshape that is the time-out timer alert tone. The alert tone is inserted into the receiver audio, via the volume control. Because the receiver audio path between the volume control and the speaker is unmuted by the low sidetone enable signal, the time-out timer alert tone is heard in the speaker.

4.6.2.3.3 The time-out timer circuits can be reset by momentarily releasing the push-to-talk button on the microphone. This action turns on switch Q1703, grounding pin 17 of the microcomputer. This sets the microcomputer to the receive mode disabling the three time-out timer data outputs at pins 18, 19, and 26 of the microcomputer.

4.6.2.4 Digital/Analog Converter

During encoding, the microcomputer outputs the PL or DPL signaling codes as four data bits at pins 3 through 6 of the microcomputer. The four data bits are applied to a D/A (digital-to-analog) converter in hybrid filter HY1701. The D/A converter is a resistive ladder network that converts the PL or DPL digital data to an ac analog signal. The ac analog signal is filtered by two low pass filter stages, also part of hybrid HY1701, that have a cutoff frequency of 360 Hz. The filtered output is then divided into two signals that are used to modulate the VCO in the frequency synthesizer circuits. One signal, coupled through capacitor C1718, is the reference signal that carries signaling information below 50 Hz. The other signal, coupled through capacitor C1712, is the PL and DPL VCO modulation signal that carries information above 50 Hz. The VCO modulation signal is routed via the transmit audio/IDC circuits in the transmitter, to the synthesizer. When PL signaling tones are being encoded, only the PL/DPL VCO output is required by the VCO. When DPL signaling tones are being encoded, both the VCO modulation and reference modulation outputs are necessary. Resistor R1705, connected to pin 13 of HY1701, is factory-selected to produce a frequency deviation of 550 ± 50 Hz.

4.6.3 Activity Checker

4.6.3.1 The microcomputer activity checker circuit consists of the circuitry of Q1706, Q1707, and U1702. The activity checker is controlled by the strobe output pulse appearing at pin 7 of the microcomputer. Normally, strobe pulses are generated every 4 milliseconds. The pulses are sensed by Q1707, which drives U1702. This causes the output of U1702 (pin 8) to be at ground and the reset pulse supplied to pin 39 of the microcomputer to be disabled (high). If a microcomputer fault occurs, software programming within the microcomputer prevents strobe pulses from being generated for 15 milliseconds. This causes 31 Hz square wave pulses to be generated at the output of U1702. The pulses are inverted by Q1706 and are applied to the reset line to reset the microcomputer causing it to restart its operation. The microcomputer resets until the fault is remedied and 4 millisecond strobe pulses are again generated.

4.6.3.2 The square wave output from the activity checker is also used during transmit to unkey the transmitter when a microcomputer fault occurs. The square wave pulses are integrated by capacitor C1715 and resistor R1734, which turns on inverter Q1708. This turns off Q1704, driving its delayed PTT output signal high. This disables the delayed PTT signal and unkeys the transmitter.

4.6.3.3 The actvity checker also incorporates a built-in power-up function that automatically causes a reset at power turn-on, to ensure that the microcomputer starts properly when radio set power is turned on.

4.6.4 Microcomputer Test Program

4.6.4.1 A built-in test program may be used to verify the operation of the microcomputer, and provide a test signal for troubleshooting the PL/DPL board circuitry. To activate the test mode, turn on the radio set power, ground TP6 (U1705-6), and ground TP5 (U1705-38) in order. In test mode, the microcomputer outputs square waves at all I/O ports. The period of the square wave signal at each bit (pin) of the microcomputer is twice the period of the preceding bit, with the shortest period at the lowest numerical bit (such as P0-0) being 88 microseconds. The test waveform series at all ports (P0, P1, P4, and P5) is the same, and all are synchronized.

4.6.4.2 Because external circuitry normally grounds certain microcomputer ports, the test pattern may appear to be missing at the PTT port (P1-0 at U1705-17) or at some of the channel select ports, depending on the position of the channel select switch. To observe the test program waveform at the PTT port, press the microphone push-to-talk button. To observe the waveforms at the channel select ports, it is necessary to unground the channel select lines in question by selecting channels that cause a high on the line being tested, or by lifting the desired microcomputer pin from the socket.

4.6.4.3 To stop the test program, remove both ground connections at the test points.

4.7 TIME-OUT TIMER
(Refer to Time-Out Timer schematic diagram)

4.7.1 The time-out timer is an option used in carrier squelch models only. The time-out timer circuit board is located in the option area of the chassis. The purpose of the time-out timer is to unkey the transmitter and alert the operator after a predetermined period of transmit time. The time-out timer is reset ever time the microphone PTT button is pressed and released.

4.7.2 The time-out timer circuits are controlled by the PTT logic in the transmitter circuits. The PTT signal is applied to counter U1802. When the PTT signal goes low, it takes the counter out of reset. The counter then starts counting the 33 Hz clock signal generated by U1801C and U1801D. JU1 through JU5 determine the allowable duration of the transmission, and only one of them should be in. Refer to the schematic diagram for a table giving jumper status and time-out times.

4.7.3 When the selected output of U1802 goes high, it does four things: 1) it enables the 775 Hz tone oscillator formed by U1801A and U1801B, 2) it disables the 33 Hz clock generator formed by U1801B and U1801C, 3) it turns on Q1803, and 4) it turns on Q1802.

4.7.4 The collector of Q1802 then goes low, applying a low to the TOT PTT control signal, P1801-8. This signal goes to the *DVP* PTT circuitry via J101-24, and causes the *DVP* circuitry to dekey the transmitter. The collector of Q1803 applies a low to the sidetone enable signal via P1801-7 and P352-10, allowing the 775 Hz tone being inserted into the receiver sidetone (via P1801-10 and J352-18) path to be heard.

4.7.5 The time-out timer circuitry remains in this state until the PTT signal goes high (microphone PTT button is released). This puts the counter into the reset mode again, and all of its output go low. This disables the 775 Hz tone oscillator, re-enables the 33 Hz clock generator, and turns off Q1802 and Q1803. When Q1802 turns off, it no longer disables the *DVP* PTT circuitry and the transmitter may then be keyed again.

4.8 POWER DISTRIBUTION CIRCUITS
(Refer to Main Board and Power Interconnect Board Schematic Diagram)

4.8.1 The +9.6 V regulator is the source for distribution of regulated 9.6 volts. The regulator consists of operational amplifier U300A (which functions as a differential amplifier), series pass transistor Q300, and driver transistor Q301. The differential amplifier samples a percentage of the +9.6 V dc output from the series pass transistor, as determined by divider R307 and R308. The sample is compared to a fixed dc reference voltage, and controls the conduction of transistors Q301 and Q300 to keep the sample and reference voltages equal. A constant +9.6 volt output is thereby maintained. Operating voltages for the regulator are the PA A+ voltage and the SW A+ voltage. The PA A+ voltage is supplied to the series pass device, Q300. The SW A+ voltage turns on U300A when the front panel Off-on/Volume control is set to the on position, thus turning on the regulator.

4.8.2 Transistors Q300 and Q301 produce the +9.6 V dc output voltage from the PA A+ input. A portion of the +9.6 V dc output (approximately 52%, determined by 1% resistors R307 and R308) is fed back to the negative (-) input, pin 2, of the differential amplifier. The voltage at pin 2 is the sample voltage. The fixed reference voltage of +5.03 V dc appears at the positive (+) input, pin 3. The reference voltage is established by Zener diode VR301. The Zener diode is biased by resistor R303 for best temperature compensation.

4.8.3 When the output from Q300 and Q301 is +9.6 V dc, the sample voltage is the same as the reference voltage (+5.03 V dc). If the +9.6 V dc output increases, the sample voltage at the negative input rises above the reference voltage at the positive input, causing the output from U300A to decrease. This decreases the current through Q301, causing the current through Q300 to decrease and the output voltage to decrease, until +9.6 volts is obtained. As the output voltage decreases below +9.6 V dc, the sample voltage at the negative input of U300A decreases; the output of U300A increases, and Q301 and Q300 conduct harder, raising output voltage back to +9.6 volts.

4.8.4 Diode CR300 provides short-circuit protection for Q300 and Q301 by turning them off if the regulated output is shorted to ground. The regulator can withstand an indefinite short in this condition; the output of U300A is internally short-circuit protected. Resistors R301 and R302 reduce the voltage gain of Q300 and Q301 for increased stability. Resistor R306 and capacitor C304 filter high frequency Zener noise.