Frequency Synthesizer

1. General

The *SYNTOR X* frequency synthesizer generates directly the first receive injection frequency and transmitter carrier. In the receive mode, the synthesizer locks on a frequency in Range 1 that is 53.9 MHz higher or a frequency in Ranges 2–5 that is 53.9 MHz lower than the receive frequency.

In the transmit mode, the synthesizer locks on the transmit output frequency. The synthesizer has a phase–locked loop (PLL) that operates at the output frequency and consists of a 14.4–MHz reference oscillator, low–noise voltage–controlled oscillators (VCO), a high–speed programmable divide–by–3–or–4 variable–modulus prescaler, a low–speed programmable divider, a sample–and–hold phase detector, and an adaptive loop filter. The 14.4–MHz reference oscillator output is applied, via an injection tripler, to the second mixer of the receiver, where it serves as the low–side second injection frequency. The synthesizer circuits are on the common circuits board and RF board, and in the RF internal casting.

2. Theory of Operation

2. 1 INTRODUCTION

The PLL synthesizer is a single negative–feedback loop that uses the relationship between the phase of the input signals as the controlling variable. The output of a high–accuracy, temperature–compensated crystal reference oscillator (U608) is divided down in frequency by the reference divider (part of U602). The reference divider puts out a high–stability 6.25–kHz (5.00–kHz for some customer frequencies) squarewave signal that is routed from the reference divider to the phase detector (U603–2) to serve as the reference frequency input.

The loop frequency input of the phase detector (U603–23) receives the negative feedback for the PLL. This comes from the VCO, at a frequency proportional to the voltage on the VCO's steering line (P650–2).

The VCO, an FET RF oscillator (Q1401), multiplies the frequency up to the transmit frequency or the receive injection frequency (53.9 MHz below the designated frequency). A programmable N divider divides the VCO frequency down to the loop frequency as follows:

$$f_{(loop)} = F_{(VCO)} / N$$

where: $f_{(loop)}$ = N divider loop frequency output

$f_{(VCO)}$ = VCO output frequency

N = integer

The loop frequency and the reference frequency are applied to the phase detector (U603–23 and U603–2, respectively), whose function is to generate a DC output voltage proportional to the phase difference between these two frequencies. Phase is the controlling variable, since there may be small phase errors in the locked loop, but frequency errors cannot occur. The AC output voltage of the phase detector (PHASE DET OUT at U603–15) goes via the loop adaptive filter to the VCO steering line, thus completing the feedback loop. The loop filter controls the PLL closed loop response and removes noise from the phase detector output.

If the VCO output frequency goes high, the N divider loop frequency output also goes high, thus causing a leading phase displacement at the phase detector loop input. Since the reference signal phase does not change, the internal circuits of the phase detector detect this condition and lower the DC voltage output U603–15. This signal goes to the VCO steering line via the loop adaptive filter, causing a reduction in frequency. This compensates for the original frequency difference.

2. 2 LOOP PROGRAMMING AND CONTROL

For frequency generation and control, the microcomputer reads the programming information from the personality board memory module, combines it with the synthesizer control information, and multiplexes this information to the programmable divider (U602). The programming information, contained in six four–bit words, goes to the multiplex programmed divider via four data lines (D0, D1, D2, and D3) and via three data word address lines (A0, A1, and A2).

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Address lines A0, A1, and A2 in the multiplexing sequence tell the divider which of the six four–bit words the microcomputer is sending on the data lines.

Of the bits sent to the divider, one selects either the transmit or the receive VCO operation. This bit is transferred from the divider (U602–19) to the transmit–receive VCO band switching network, which supplies TX +9.4V to the VCO transmit switching circuitry via P650–3. Another bit determines the frequency range of the VCO. This bit is transferred from the divider (U602–20) to the range shift network, which gives the proper range shift information to the VCO's via P650–5 and P650–6. Sixteen bits program the A and B counters, which are inside the programmable divider. Two bits program a reference divider. Two latched bits ($\overline{C0}$ and $\overline{C1}$) go from the multiplex programmed divider to the programmable variable–modulus prescaler (U602–15 and U602–16, respectively) to control its operation during the divide cycle. Two other latched outputs from the divider, $\overline{S0}$ and $\overline{S1}$, are used by the sample–and–hole phase detector to control the loop adaptive filter. When set high, $\overline{S1}$ indicates a change in frequency. In this case, a seventh word clears the frequency change indication by setting $\overline{S1}$ low, thus generating a control pulse. $\overline{S0}$ switches between the transmit and receive loop filters (high for transmit filter).

The six four–bit words on the data lines remain the same once the condition of synthesizer operation and the frequency have been selected. Any change in radio mode makes the microcomputer address different memory locations in the memory module. Consequently, the six four–bit words may send different information to the divider via the data lines. The microcomputer notifies the divider, via the STROBE line, when the binary information on the data and address lines can be read into the divider and latched in without any chance of error.

2. 3 DIVIDER

The programmable N divider works by "dual–modulus prescaling." It uses two dual–modulus prescalers, a divide–by–3–or–4 prescaler (with its own internal programmable C counter) and a divide–by–63–or–64 prescaler. The divide–by–63–or–64 prescaler, with programmable counters A and B, is inside divider U602. The output frequency of each prescaler is first divided by one divisor to obtain a fixed number of counts, then divided by a second divisor to obtain a different number of counts. The total division performed by this system may be set to an integral value N by the programming of counters A, B, and C. This system of division allows the basic division function of programmable divider U602 to be expanded to a higher operating frequency with no loss of resolution.

Each output frequency requires that a different value of N be programmed into the programmable counters. On the positive–going loop pulse edge, the divide–by–3–or–4 prescaler starts dividing by four and continues to do so until the C counter reaches zero. At this time, the prescaler enters into the divide–by–3 mode. Once the loop pulse goes low, the C counter is preset to the value determined by the $\overline{C0}$ and $\overline{C1}$ bits. This causes a new cycle to begin on the positive–going edge of the next loop pulse.

The divide–by–63–or–64 variable–modulus prescaler works in a similar fashion. When a loop count begins, it initially divides by 64 for the number of times programmed into the A counter. When the A counter counts to zero, the loop pulse goes low and the prescaler changes to the divide–by–63 mode. It stays in this mode until the B counter reaches zero. At this time the loop pulse goes high and the cycle repeats.

Another programmable divider acts on the 14.4–MHz reference oscillator input frequency at U602–2 to produce one of two reference frequencies: 5 kHz or 6.25 kHz. One word of the frequency select data contains two bits (D0 and D1) that select one reference frequency, as shown in Table 1.

Table 1. Reference Frequency Selection

D0	D1	REFERENCE FREQUENCY
0	0	unused
1	0	6.25 kHz
1	1	5.00 kHz

The frequency select data also contains bits TX and $\overline{\text{RANGE}}$. Bit $\overline{\text{RANGE}}$ selects the VCO range shift window for the selected operating frequency. (Refer to the VCO paragraph for details on the range shift windows.) When the VCO bit is latched into the divider, $\overline{\text{RANGE}}$ is forwarded from U602–20 as a RANGE SHIFT signal to the range shift switching network. It is then routed via the feedthrough plate to the VCO. An NPN transistor on U600 compensates for the differing modulation characteristics of the VCO windows. When the RANGE SHIFT signal is low (at U602–20), the transistor turns on, sending a lower–amplitude audio signal to the VCO. (The VCO requires less audio input to fully modulate the RF signal when U602–20 is low than when it is high.)

2. 4 PHASE DETECTOR

Phase detector U603 compares the reference and loop frequency outputs of the divider circuit and uses this information to generate a DC output signal that controls the VCO frequency. The phase detector also monitors the FREQUENCY CHANGE line ($\overline{S1}$) and the LOW BANDWIDTH SELECT line ($\overline{S0}$) and uses this information to generate control signals for the adaptive filter.

The phase detector output signal level is controlled by the length of time between the positive transition of the reference signal and the positive transition of the loop signal. When the reference signal goes high (at U603–2), ramp generator Q603 turns on, maintaining a constant current through C630. This constant current generates a linear rise (ramp) in the voltage at U603–24. The rise of the ramp voltage halts when the LOOP signal (at U603–23) switches to a high level, causing Q603 to turn off.

The positive transition of the loop signal, in addition to halting the ramp generator, resets an internal sample timing circuit. The ramp voltage is held constant for a time determined by sample timing capacitor C631. During this time, the two hold capacitors (C632 and C633) are charged to a level

determined by the ramp voltage. At the end of the sample time, the ramp capacitor is discharged in preparation for the next cycle.

The accumulated charge on the hold capacitors controls the conduction of a push–pull output driver. The output driver consists of an internal NPN transistor and an external PNP transistor controlled by the signal at U603–17. The PHASE DETECTOR OUTPUT signal at U603–15 is coupled, via the adaptive filter, to the VCO, where it controls the generation of injection frequencies.

The phase detector also generates control signals for the adaptive filter. It decodes the FREQUENCY CHANGE signal at U603–5 and the LOW BAND WIDTH SELECT signal at U603–3 to generate four control signals that are coupled to the adaptive filter. These four control signals are: ADAPT, $\overline{\text{ADAPT}}$, RSW, and TSW (appearing at U603–10, –7, –9, and –8, respectively).

When operating channels are being changed in the receive mode or the mode is being changed from transmit to receive, the FREQUENCY CHANGE pulse at U603–5 causes the ADAPT line to go high and the $\overline{\text{ADAPT}}$ line to go low. Since the LOW BAND WIDTH SELECT line is low, the RSW line is driven high, the TSW is driven low, and the adaptive filter is forced into the receive–adapt mode. The $\overline{\text{ADAPT}}$ line returns to a high level and the ADAPT line returns to a low level after approximately 2.4 milliseconds under phase detector control, forcing the adaptive filter to enter into the normal receive mode.

When the PTT pushbutton is pressed, the FREQUENCY CHANGE pulse causes the ADAPT line to go high and the $\overline{\text{ADAPT}}$ line to go low. Since the LOW BANDWIDTH SELECT line is high, the TSW line is driven high, the RSW is driven low, and the adaptive filter is forced into the transmit–adapt mode. The ADAPT and $\overline{\text{ADAPT}}$ lines switch states after approximately 12 milliseconds under control of the phase detector, and the adaptive filter is forced to enter into the normal transmit mode.

While the ADAPT line is high during the transmit–adapt mode, the power amplifier is disabled. (This line connects to the personality board via J602–11.) Moreover, the ADAPT line is forced to switch to a high state when the synthesizer cannot achieve lock, thus preventing the radio from transmitting unstable or off–frequency signals.

For maximum switching speed, the microcomputer sends new data to the synthesizer at the appropriate time of the divide cycle. The phase detector forwards a SYNTHESIZER SYNC signal, from U603–4 via J602–9, notifying the microcomputer of the appropriate time to send new frequency programming information.

2. 5 ADAPTIVE FILTER

2. 5 .1 General

The adaptive filter is a low–pass filter in the steering line between the phase detector and the VCO. It removes noise and variations in the steering line level to prevent unwanted modulation of the VCO.

The phase detector controls the adaptive filter through PHASE DETECTOR OUTPUT line U603–15 to operate in one of the four selectable modes, depending upon the state of the synthesizer at a given time. The modes are transmit adapt, receive adapt, transmit, and receive. The transmit adapt mode and the receive adapt mode differ only in the amount of time spent in the adapt condition, whereas the transmit mode and receive mode each require different filter characteristics. These characteristics are selected by transmission gates that switch the filter components into and out of the steering line signal path, as required.

2. 5 .2 Filter Mode Selection

Each of the four selectable modes, transmit, receive, transmit–adapt, and receive–adapt, is selected by a unique combination of states on two complementary pairs of lines. The TSW and RSW lines make up one such pair, and the ADAPT and ADAPT lines make up the other. These lines are coupled from the phase detector to the adaptive filter and are connected to the input pins of the mode–select gates (U604 A and B). The ADAPT line is also connected to transmission gates U605 and U606.

The low–input AND gates (U604 A and B) have two output lines, TRANSMIT MODE–SELECT and RECEIVE MODE–SELECT. For each filter operation mode selected, one of these output lines is switched into a high state (between +8.6 and +9.6V). Since these gates use low–level inputs, the output of a gate goes high whenever both of its inputs go low. Or, expressed as a Boolean expression, the input/output signals of, say U604A, are:

$$\text{TRANSMIT MODE–SELECT} = \overline{\text{ADAPT}} \bullet \overline{\text{RSW}}$$

In conjunction with the ADAPT line, the out–put lines of the mode–select gates (U604 A and B) control transmission gates U605 and U606. When a selector output is forced high, the associated transmission gates turn on, passing the signals like a closed switch. Transmission gates U605A–D have ON impedances of less than 200 ohms, and gates U606A–D have ON impedances of less than 500 ohms.

2. 5 .3 Transmit Mode

When the synthesizer is in the normal transmit mode, the phase detector drives the TSW and ADAPT lines high and their complements, RSW and $\overline{\text{ADAPT}}$, low. The output of gate U604A goes high, turning on transmission gates U605A, U606A, and U606D. The natural loop frequency of the synthesizer in this mode is approximately 15 Hz. The adaptive filter stays in this mode as long as the radio is transmitting.

In this mode, the steering line is filtered by R652 and a shunt path to ground consisting of C649, C641, C634, and R653. (The ON impedance of the transmission gates is neglected.) This signal passes to the VCO via a test jumper (JU600) and J650–2.

2. 5 .4 Receive Mode

When the synthesizer is in the receive mode, the phase detector drives the RSW and $\overline{\text{ADAPT}}$ lines high and their complements, TSW and ADAPT, low. The output of gate U604B goes high, turning on transmission gates U605C and U606C. The natural loop frequency of the synthesizer in this mode is approximately 75 Hz. The adaptive filter remains in this mode while the radio is in the receive mode.

In this mode, the steering line is filtered by R635, a shunt path consisting of R636, C640, and C641, and R637 and C654. (The ON impedance of the transmission gates is neglected.) The signal passes through the test jumper to the VCO via J650–2.

2. 5 .5 Transmit–Adapt Mode

When the synthesizer is in the transmit–adapt mode, the TSW and ADAPT lines are driven high by the phase detector, and their respective complements, RSW and $\overline{\text{ADAPT}}$, are driven low. Transmission gates U605B, U605D, and U606D are directly turned on by the ADAPT line. The synthesizer has a high natural loop frequency in this mode, allowing it to change frequencies rapidly. The adaptive filter is switched into this mode for approximately 15 milliseconds while the radio changes from the receive mode to the transmit mode. The transmitter is inhibited in this mode by the SYNTHESIZER ADAPT line.

In this mode, transmission gate U606B by–passes the greater part of the adaptive filter. A grounded capacitor, C641, is connected to the steering line. (The ON impedance of the transmission gates is neglected.) While the filter is in this mode, C641 and C654 are being charged. The charge on C654 prevents the VCO from changing frequency during the transition from the transmit–adapt mode to the transmit mode. C654 always remains connected to the steering line. The steering line passes to the VCO through the test jumper via J650–2.

2. 5 .6 Receive–Adapt Mode

When the synthesizer is in the receive–adapt mode, the RSW and ADAPT lines are driven high by the phase detector, and their respective complements, TSW and $\overline{\text{ADAPT}}$, are driven low. Transmission gates U605B, U605D, and U606B are directly turned on by the ADAPT line. The synthesizer has a high natural loop frequency in this mode, allowing it to change injection frequencies rapidly. The adaptive filter switches into this mode for approximately three milliseconds while the radio changes from the transmit mode to the receive mode or from one receive frequency to another (such as when changing the operating channel of the radio).

In this mode, the greater part of the adaptive filter is shorted by transmission gate U606B, and the steering line is connected to C641. (The ON impedance of the transmission gates is neglected.) When the filter is in the receive–adapt mode, C641 and C654 are being charged. The accumulated charge on C654 prevents the VCO from changing frequencies during the transition from the receive–adapt mode to the receive mode. C654 always remains connected to the steering line. The steering line passes to the VCO through the test jumper and J650–2.

When the frequency is changed (or if, for any reason, the loop falls out of lock), the phase detector makes the adaptive filter switch to the ADAPT mode. Consequently, the $\overline{\text{ADAPT}}$ line switches to a low state, causing the OUT–OF–LOCK indicator LED to turn on. Therefore, in normal operation of the frequency synthesizer, the OUT–OF–LOCK indicator LED turns on for a brief period whenever the frequency is being changed. During Channel Scan operation, the radio can be continuously changing frequencies at a fast rate, causing the OUT–OF–LOCK indicator LED to give a dim indication. A brightly lighted indicator LED points to the presence of an out–of–lock fault in the frequency synthesizer. Thus this indicator LED is useful for troubleshooting.

Various radio functions are deactivated each time the frequency synthesizer goes into the ADAPT mode. First the high ADAPT output disables the radio audio stages via the squelch-circuits on the common circuits board. In addition, the transmitter and IDC circuits are disabled via the personality board. This fail–safe feature prevents transmitter key–up (if a loss–of–lock malfunction occurs), thus preventing the generation and transmission of uncontrolled RF signals.

2. 5 .7 Super Filter

Because the VCO requires a very pure DC sup–ply voltage, an ultra–low–pass filter (U600) supplies the VCO with a very–low–noise +8.6 output voltage. The filter removes any ripple or noise present on the +9.6V supply line, thus preventing unwanted modulation of the VCO. A one–volt drop across the filter lowers the output voltage from +9.6 to +8.6V.

The super filter consists of a low–pass filter, an error amplifier, and an external series–pass transistor (Q601). The +9.6V supply is connected to U600–1 as well as to the emitter of Q601. Internally, the input from U600–1 passes through a low–pass filter to the non–inverting input of the error amplifier. C603, connected to U600–2, forms part of the low–pass filter. The output line (also connected to the collector of Q601) is fed back to the inverting input of the error amplifier through U600–4.

The error amplifier output, connected to the base of Q601 via U600–3, controls the conduction of the transistor. These connections enable the super filter to compare the output line voltage with the filtered input line voltage and to increase or decrease the conduction of Q601 to remove any ripple or noise from the VCO supply line.

The VCO supply is further filtered by C604, which is connected to ground. This filtered supply is then forwarded to the transmit–receive VCO switching network. Depending on the state of U602–19, transmit 8.4V or receive 8.4V is sent to the appropriate VCO through the VCO interconnect plate via J650–3 and J650–1. The filtered 8.6V supply is also forwarded to the bandshift switching network, which selects the proper state of the Bandshift 1 and Bandshift 2 lines, depending on the state of U602–20.

2. 5 .8 Feedback Buffer

A signal at the transmit or receive injection frequency is fed back from the VCO buffer to the main board. The divider/ phase detector circuits use this frequency to monitor the oscillator frequency.

The feedback buffer, Q602, accepts an input from a tap network between the two VCO buffer stages. This input signal is forwarded via a coaxial cable and connector P/J600. The feedback amplifier output is coupled to the divide–by–3–or–4 prescaler (U601) via C607.

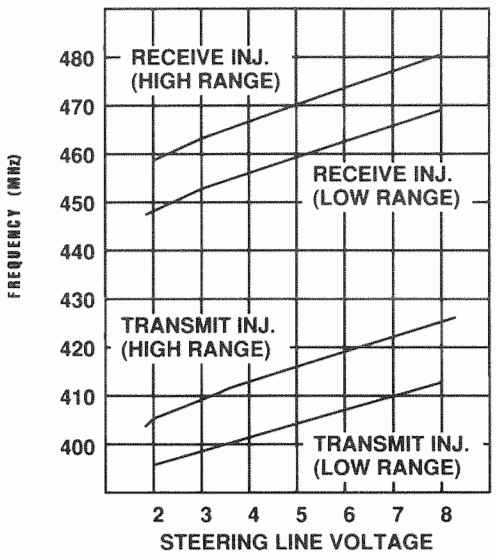


Figure 1. Injection Frequency vs. DC Voltage for Range 1

2. 6 VOLTAGE–CONTROLLED OSCILLATOR (VCO) AND BUFFER

2. 6 .1 General

The VCO and buffer amplifier, which supply the receive injection frequencies and frequency–modulated transmit injection frequencies, are mounted in separate compartments in the internal casting. The VCO output goes to the buffer input via a short coaxial cable. Both VCO and buffer are constructed on alumina thick–film substrates.

The VCO output frequency range for transmit and receive are listed in Table 2. A PIN diode switches the oscillator between the transmit and receive bands within a particular range. An additional PIN diode switch allows each range to be covered in two sub–ranges, the transmit and the receive frequency ranges.

Table 2. VCO Output Frequency Ranges

RANGE	TRANSMIT (MHz)	RECEIVE (MHz)
1	406–420	459.9–473.9
2	450–470	396.1–416.1
3	470–488	416.1–434.1
4	482–500	428.1–446.1
5	494–512	440.1–458.1

2. 6 .2 Oscillator Circuit

The VCO has a grounded–gate Colpitts oscillator that uses a JFET Q1401 as the amplifying element. The oscillator operates at half the desired transmit or receive injection frequency. The transmit or receive band is selected by U602 Pin 19 (BAND SHIFT) on the RF board. When Pin 19 is high, Q608 and Q609 in the RF board's TX/RX bandshifting circuit are both on. The TX/RX bandshifting circuit produces RX +8.4V for Range 1, or TX +9.4V for Ranges 2–5. The bandshifting circuit output switches on the RF PIN diode switch (CR1408 and CR1409) on the VCO via P/J650–3 and connects the TX/RX band shift resonator in parallel with the main resonator. This changes the oscillator frequency by 26.95 MHz to half the desired TX/RX frequency.

Each of these two bands is further split up into two contiguous ranges. When U602 Pin 20 ($\overline{\text{RANGE}}$) on the RF board is high, Q600 pulls the W/ W/ $\overline{\text{RANGE}}$ line (P/J650–6) low. This makes Q606 pull the $\overline{\text{RANGE}}$ line (P/J650–5) high, and RF PIN diode CR1407 on the VCO then switches C1412 across the oscillator resonator. This lowers the oscillator frequency for low–range operation. For high range, the situation is reversed. Within either range, the oscillator is tuned via the steering line as described in Section 2.6.4 below.

The VCO's transmission line resonator has microstrip capacitors plated on the substrate and interconnected with wires. These are trimming capacitors for the oscillator tank circuit. They are adjusted at the factory, and do not depend on the customer's frequencies.

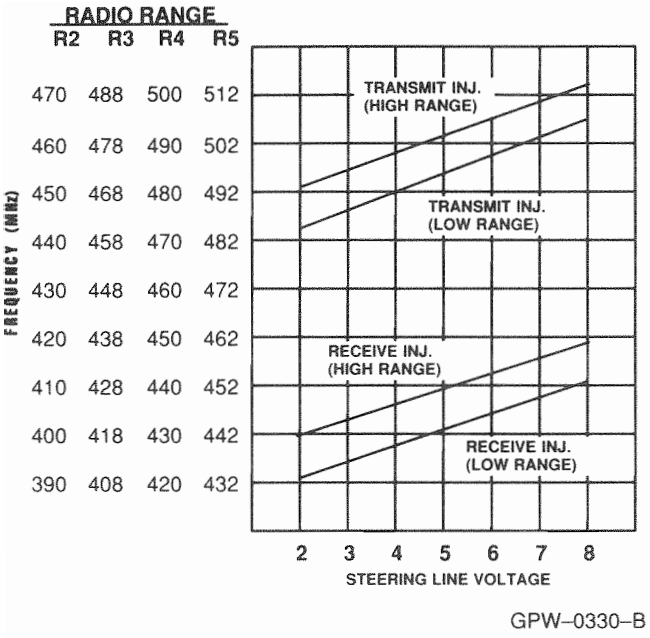


Figure 2. Injection Frequency vs. DC Voltage for Ranges 2, 3, 4, and 5

The oscillator signal is coupled to frequency doubler Q1404, which processes the desired transmit or receive injection frequency. After being filtered to reduce the half–carrier–frequency component, the doubler output goes to the buffer.

2.6.3 Buffer

The buffer is a two–stage amplifier (Q1450 and Q1451) that sends a signal either to the LLA (Low–Level Amplifier) interface board via P700 during transmit, or to the receive injection filter via P101 during receive. Keyed +9.4V, coming by wire from the RF board, turns on RF PIN diode switch CR1450 and turns off PIN diode CR1451 (by turning off Q1452). This switches the buffer output to P700 for the transmitter. In receive, keyed +9.4V is low and the two PIN diodes switch roles to deliver receive injection power to P1450.

The buffer also sends a signal via P600 to the RF board in both the transmit and receive modes to drive the prescaler to send feedback to the synthesizer. Note that the +9.6V to turn the buffer's second stage comes from the RF board via the center conductor of P600. The buffer's first stage is powered by +8.6V coming via a wire from the RF board.

2.6.4 Steering Line Circuit

The steering line, in conjunction with the rangeshift and TX/RX bandshift lines, determines the operating frequency of the VCO. The steering line is driven by the phase detector (U603) and is coupled to the VCO via the adaptive filter. The phase detector supplies a DC output voltage to maintain the VCO output at the desired frequency. When the frequency is changed, the phase detector DC output volt age shifts to change the oscillator frequency and then maintain this new frequency. Figure 1 shows the transmit and receive oscillator frequencies as functions of the steering line DC voltage.

The steering line is coupled from the RF board via J650–2 and the VCO interconnect plate. The plate contains the RF filters that shield the VCO. The steering line DC voltage level determines the capacitance of diodes CR1402, CR1403, CR1404, and CR1405. An increase in the steering line voltage causes the capacitance of these diodes to decrease and the corresponding oscillator frequency to increase. On the other hand, a decrease in the steering line voltage causes an increase in the capacitance of the diodes and a reduction in the oscillator frequency.

2.6.5 Modulation Line

During transmit, the transmit audio signals modulate the VCO directly, using varactor diode CR1408. The transmit audio signal is coupled, via Pin 4 of the VCO interconnect plate, to CR1408, which modulates the oscillator frequency.

2.7 TRANSMIT AUDIO CIRCUITS

Note

While reading the following, refer to the IDC portion of the Common Circuits Board Schematic Diagram attached to the Common Circuits Board section of this manual.

The transmit audio circuits consist of four stages that condition the microphone audio signal for direct frequency modulation of the transmit injection signal. The greater part of the audio path is controlled by the IDC ENABLE signal that is coupled to the IDC (instantaneous deviation control) circuitry via J401–6. This signal controls transmission gate U510A, which enables the transmit audio circuits only when the radio is in the transmit mode. (Transmit +9.5V is applied to the IDC ENABLE line.)

The MIC HI signal is coupled into pre–emphasis amplifier U502D via J401–5. This amplifier has a frequency response that enhances the audio frequencies toward the high end of the transmit audio frequency range (approximately 300–3000 Hz). The amplifier output (at U502–12) is coupled to U501–1. When PTT is activated, the transmission gate control line (at U501–13) switches to a high level and the signal passes through the gate to limiter/amplifier U502A.

The limiter/amplifier clips the audio signals at seven volts peak–to–peak, thus preventing excessive audio modulation of the transmitted signal. (With lower audio input levels, this amplifier acts as a linear gain stage.) The limited transmit audio signal is coupled from U502–3 to splatter filter stage U502C.

The splatter filter is a 3–kHz low–pass filter that removes higher–order harmonics from the audio signal. With unity gain, this filter attenuates high–frequency harmonics on the clipped audio signal from the limiter stage. The splatter filter

output passes from U502–10 to the deviation adjust potentiometer (R517).

External modulation, such as PL or DPL, passes through gates U501B and U501C. These gates are connected in series with the external modulation inputs, and can therefore disable these modulation inputs to circuits that may require such a function. Normally, these enable lines are pulled high by the HY501 resistors. The output of each gate passes to U502B via the resistors that form part of HY502.

An output of combiner U502B is coupled to the compensation adjust potentiometer R543 and the reference oscillator. PL and DPL signals frequency–modulate the reference oscillator, thus preventing the phase detector output from defeating the direct low–frequency modulation of the VCO generated by the PL/DPL signal. (The reference oscillator and phase detector form part of the synthesizer schematic diagram.)

The audio signal at the wiper of R517 is combined with the PL/DPL signals at the compensation adjust potentiometer (R543). This combined signal then passes to the transmit VCO. The compensation adjust potentiometer, R543, is adjusted at the factory and should be readjusted only if the common circuits board, reference oscillator, or VCO is changed. R543 can be readjusted by the procedure presented in the Radio Alignment and Adjustments part of the Maintenance and Troubleshooting Section of this manual.

Reference Modulation Inhibit Switch Q502 is allowed to conduct while the radio is in the receive mode, effectively shorting the reference modulation signal line to ground. This prevents any noise induced on the line in receive mode from affecting the reference oscillator and, consequently, the receive injection frequency. During initial turn–on, C508 is charged through Q502. This action allows a stable receive frequency to be attained almost immediately. Q502 is turned off by TX +9.5V during transmit, enabling the reference modulation signal line.

3. Synthesizer Troubleshooting Procedure

3. 1 GENERAL

The troubleshooting chart at the end of this section gives a comprehensive procedure for troubleshooting the frequency synthesizer.

Major problems that may occur in the frequency synthesizer are:

- Synthesizer does not lock.
- Synthesizer locks on wrong frequency.
- Excessive reference frequency feeds through (spurs).
- Frequency lock is noisy.
- Switching response is slow.

Table 5 summarizes these problems and their possible causes. Tables 6, 7, 8, and 9 show pin connections and voltages for the phase detector, divider, prescaler, and super filter.

The frequency synthesizer troubleshooting chart mentions an open–loop test and the checking of the divider programming. The following paragraphs describe these procedures without using a flowchart.

3. 2 OPEN–LOOP TEST

3. 2 .1 Introduction

This test requires a variable power supply, a frequency counter, a dual–trace oscilloscope, a DC voltmeter, and an RF voltmeter. The Maintenance and Troubleshooting Section of this manual recommends specific models of some of these.

The open–loop test consists of four procedures:

- VCO frequency test
- loop and reference waveforms check
- phase detector check
- adaptive filter check

3. 2 .2 VCO Frequency Test

(1) Remove jumper JU600 to open the STEERING LINE loop. Connect a one–kilohm resistor to the plus terminal of a 0–10V adjustable power supply and connect the free end of the resistor to the VCO side from which JU600 was removed (the side not connected to C637). Connect the negative terminal to B–. This power supply serves as a steering line in this test.

(2) Connect a frequency counter to the divider port P600 of the internal casting. To check the VCO on transmit, press the PTT switch and monitor the frequency while slowly changing the steering voltage from 2.0V to 9.0V. Verify that changing the steering voltage results in the transmit frequencies listed in Table 3 for the appropriate RANGE/$\overline{\text{RANGE}}$ condition. The rangeshift lines to the VCO are at J650–6 (RANGE) and J650–5 ($\overline{\text{RANGE}}$).

Table 3. VCO Output Frequencies During Transmit (MHz)

Range	$\overline{\text{RANGE}}$ = high (8.3V) RANGE = low (0.2V)	$\overline{\text{RANGE}}$ = low (0.2V) RANGE = high (8.3V)
1	406.0–412.8	412.805–420.0
2	450.0–459.6	459.605–470.0
3	470.0–478.7	478.705–488.0
4	482.0–490.7	490.705–500.0
5	494.0–502.7	502.705–512.0

If the rangeshift lines are normal, but the VCO fails to operate, the VCO is faulty and should be replaced. Also check the output level at the VCO divider port (P/J600) and verify that it is greater than –15 dBm for the specified steering line voltage range (2.0 to 9.0V).

(3) For receive, check the VCO as in Step 2. The VCO output frequency should be 53.9 MHz higher in Range 1 and 53.9 MHz lower in Ranges 2–5 than the receive frequency. Verify that changing the steering voltage results in the receive frequencies listed in Table 4 for the appropriate RANGE/$\overline{\text{RANGE}}$ condition.

Table 4. VCO Output Frequencies During Receive (MHz)

Range	$\overline{\text{RANGE}}$ = high (8.3V) RANGE = low (0.2V)	$\overline{\text{RANGE}}$ = low (0.2V) RANGE = high (8.3V)
1	459.9–466.7	466.705–473.9
2	396.1–406.1	406.105–416.1
3	416.1–424.7	424.705–434.1
4	428.1–436.8	436.805–446.1
5	440.1–448.8	448.805–458.1

Also check the output level at the VCO divider port P/J600 and verify that it is greater than –15 dBm for the specified steering line voltage range (2.0 to 9.6V). If the rangeshift lines are normal and the output level to the divider port is adequate, but the desired receive injection frequency cannot be tuned with the steering line voltage, the VCO is faulty and should be replaced.

3. 2 .3 Loop and Reference Waveforms Check

(1) Connect one channel of a dual–trace oscilloscope to U602–5 (REF OUT) and the other to U602–9 (LOOP OUT). Adjust the oscilloscope so that it triggers on the REFERENCE waveform. The oscilloscope trace should be in the chopped mode.

(2) Observe the LOOP waveform and verify that it is moving smoothly across the screen without any jitter when the steering line is varied from 1.0V to 9.6V.

Table 5. Frequency Synthesizer Problems and Possible Causes

PROBLEM	POSSIBLE SOURCE OF TROUBLE
Synthesizer does not lock.	See the Synthesizer Troubleshooting Chart.
Synthesizer locks on wrong frequency. **Note** Frequency errors of 12.5 or 18.75 kHz can be caused by a defective prescaler or by shorted or open programming from lines the divider to the prescaler (U601–7,U601–6).	Reference oscillator (U608) frequency off (should be 14.4 MHz +29 Hz).
	Divider programming from microcomputer erroneous (possible defective memory module, or code plug, or microcomputer).
	Divider U602 is defective.
	Prescaler U601 is defective.
Reference frequency feedthrough (spurs) excessive.	Hold capacitors C632, C633 defective (open is or leaky).
	Ramp capacitor C630 defective.
	Phase detector U603 defective.
	Adaptive filter in ADAPTIVE mode or shorted input to output; guard band shorted to VCO steering line or other adaptive filter mode.
Frequency lock is noisy.	Input level to prescaler (U601–1), loop divider (U602–25), or reference divider (U602–2) is marginal.
	Loose connection, cold solder joint, or faulty component.
	Noisy Q603.
	Defective phase detector U603.
	Defective divider U602 or prescaler U601 (jittery).
	Noisy 5V or 9.6V supplies.
	Defective adaptive filter (open capacitors).
Switching response is slow.	Improper synchronization from microcomputer: check divider programming.
	Malfunctioning adaptive filter: check U604, U605, U606.
	Phase detector U603 gain too low (overdamped response) or too high (underdamped response): check R625, R626, RT600, C630, Q603.
	Leaky adaptive filter capacitors or transmission gates (U605, U606, C641).
	Leaky VCO varactor diodes.

(3) Observe the REFERENCE signal and verify that its period is correct, that it has no jitter, and that one steering line voltage from 2.5 to 9.0V does not exactly yield this period on the loop divider output. (The period depends on the customer's programming requirements. In most cases, it is 160 microseconds for a 6.25–kHz reference.)

(4) If the conditions specified in Steps 2 and 3 are met, then check the divider buffer (Q602 and associated components), the prescaler (U601), the divider (U602), the reference oscillator (U608), and the divider programming. The prescaler can be checked by capacitively coupling a 200–MHz frequency counter to its output and verifying that the output is approximately one–third of the input frequency (or one–sixth the desired loop output frequency). A frequency counter does not give an exact indication of one–third of the input frequency, since the prescaler is dividing by four part of the time. The difference should not exceed 50 ppm.

3. 2 .4 Phase Detector Check

Check the phase detector (U603) by adjusting the steering line voltage for a loop period slightly longer than the reference period and then for a slightly shorter period. With a longer loop period, the phase detector output (U603–15) should switch to a high state (greater than 9V); with a shorter loop period, the phase detector output should switch to a low state (1.2V). If this does not happen, then check the phase detector and associated circuitry.

3. 2 .5 Adaptive Filter Check

Check the adaptive filter for short or open circuits by removing jumper JU600 and then checking for a high voltage on the adaptive filter side when the base detector output is high. The absence of a high voltage is an indication of a faulty condition.

3. 2 .6 VCO Steering Line Leakage

Note

Be sure to use a shielded cable with the voltmeter when making these measurements.

Check the VCO steering line leakage by removing jumper JU600 and connecting a one–megohm resistor to the VCO side. Connect the free end of the resistor to an adjustable power supply set to 9.5V. Use a high–impedance voltmeter (impedance greater than 10 megohms) to verify that the voltage drop across the resistor is less than 18 mV. A higher voltage drop (greater than 18 mV) is an indication of either a leaky VCO interconnection plate or defective VCO steering line varactors (CR1401–1404, CR1409, and CR1411–1414). To determine which is defective, remove the VCO from the RF internal casting and perform the test again. If the voltage drop is greater than two millivolts, replace the interconnection plate.

3. 3 DIVIDER PROGRAMMING TEST

The synthesizer troubleshooting chart refers to the divider programming test. For this test, use a dual–trace oscilloscope. The Maintenance and Troubleshooting Section of this manual recommends specific models. Table 8 gives the pin numbers and functions of the divider (U602). The timing diagram on the synthesizer troubleshooting chart shows the waveforms generated.

(1) Connect Channel 1 of a dual–trace oscilloscope to the STROBE line (U602–27) of the divider. Trigger the oscilloscope on the rising edge of the strobe signal.

(2) Connect Channel 2 of the oscilloscope to the A0 line (U602–23) of the divider.

(3) The waveforms on the oscilloscope should be similar to the example timing diagram. The pulse lengths depend on the frequency programmed into the memory module.

(4) Connect Channel 2 of the oscilloscope to the A1 line (U602–24) and compare the pattern on the oscilloscope with the one in the timing diagram.

(5) Repeat the procedure until A2 (U602–26), D0 (U602–11), D1 (U602–12), D2 (U602–13), and D3 (U602–14) have been checked and verified.

(6) Verify that the prescaler C inputs are as shown in Table 8. If these indications are incorrect, look for a short circuit, repair the circuit board runner, or replace the prescaler (U601).

Note

To check the programming in another way, use a single–trace oscilloscope with an external trigger input. Connect the external trigger to the strobe line and display the strobe signal on the oscilloscope to verify proper triggering. (See the timing diagram on the troubleshooting chart.) Each of the address and data lines can then be checked as in Steps 1 through 5, above.

Table 6. Super Filter Pin Connections and Voltages

PIN	FUNCTION	TO/FROM	NOMINAL VOLTAGE
1	VCC	From 9.6V regulator.	9.6V.
2	FILTER CAP.	C603.	7.1V.
3	EXT. DRIVER CONTROL	Q601 base.	8.9V.
4	8.6V OUT	To VCO.	8.6V.
5	Ground (internal NPN emitter)	From regulator.	0V.
6	Internal NPN collector	To VCO compensation potentiometer R602.	—
7	Internal NPN base	From VCO bandshift, R604, R605.	0.2V, transmit high, 0.7V, transmit low.
8	No connection	—	—

Table 7. Phase Detector (U603) Pin Connections and Voltages

PIN	FUNCTION	TO/FROM	NOMINAL VOLTAGE
1	High current ground.	---	0V.
2	REFERENCE IN	From U602–5.	0V to 4.3V square wave (200 us period).
3	LOW BANDWIDTH	From U602–17.	0V receive; 5V transmit.
4	SYNTHESIZER SYNC.	To microcomputer.	60 us positive pulse 0 – 5V at loop pulse rate; equal to pin 2 if pin 11 is low.
5	FREQUENCY CHANGE	From U602–18.	0.5 VS 11.1 us when frequency changes.
6	not connected.		
7	$\overline{\text{ADAPT}}$	To adaptive filter.	9.6 to 0.6V single pulse, 3.0 ms (Rx) dekey; 15 ms (Tx) key.
8	TSW	To adaptive filter.	0V receive, 9.6V transmit.
9	RSW	To adaptive filter.	9.6V receive, 0V transmit.
10	ADAPT	To adaptive filter.	0 – 9.0V single pulse, 3.0 ms (Rx) dekey; 15 ms (Tx) key
11	LOCK		0V when out of lock; 8V when in lock.
12	HOLD 1	CS11	1.4 to 8V (use high input impedance voltmeter).
13	HOLD 2	CS12	1.4 to 8V (use high input impedance voltmeter).
14	A+	—	9.6V.
15	PHASE DET OUTPUT	To adaptive filter.	1.2 to 9.5V (depending on loop output freq.).
16	Low Current Ground	—	0V.
17	EXT PNP BASE	To PNP Q604 base.	8.9V.
18	VCC	From regulator.	9.6V.
19	RAMP BASE	To PNP Q603 base (ramp generator).	9.1V.
20	FILTERED 9.1V	To R624, R625, RT600, C629.	9.1V.
21	RAMP RES.	To R626, PNP Q603 emitter.	8.0 to 8.7V. Rectangular wave @ reference rate.
22	SAMPLE TIMING CAP.	To C631.	0 to 2V sawtooth wave at loop pulse rate.
23	LOOP IN PULSE	From U602–9 via C628.	1.4V pulse riding on 1.6V (160 us, typical period).
24	RAMP CAP.	From C630 and ramp PNP Q603 collector.	Flat top ramp waveform at reference rate, top voltage 1.4 to 7V (depending on loop output frequency).

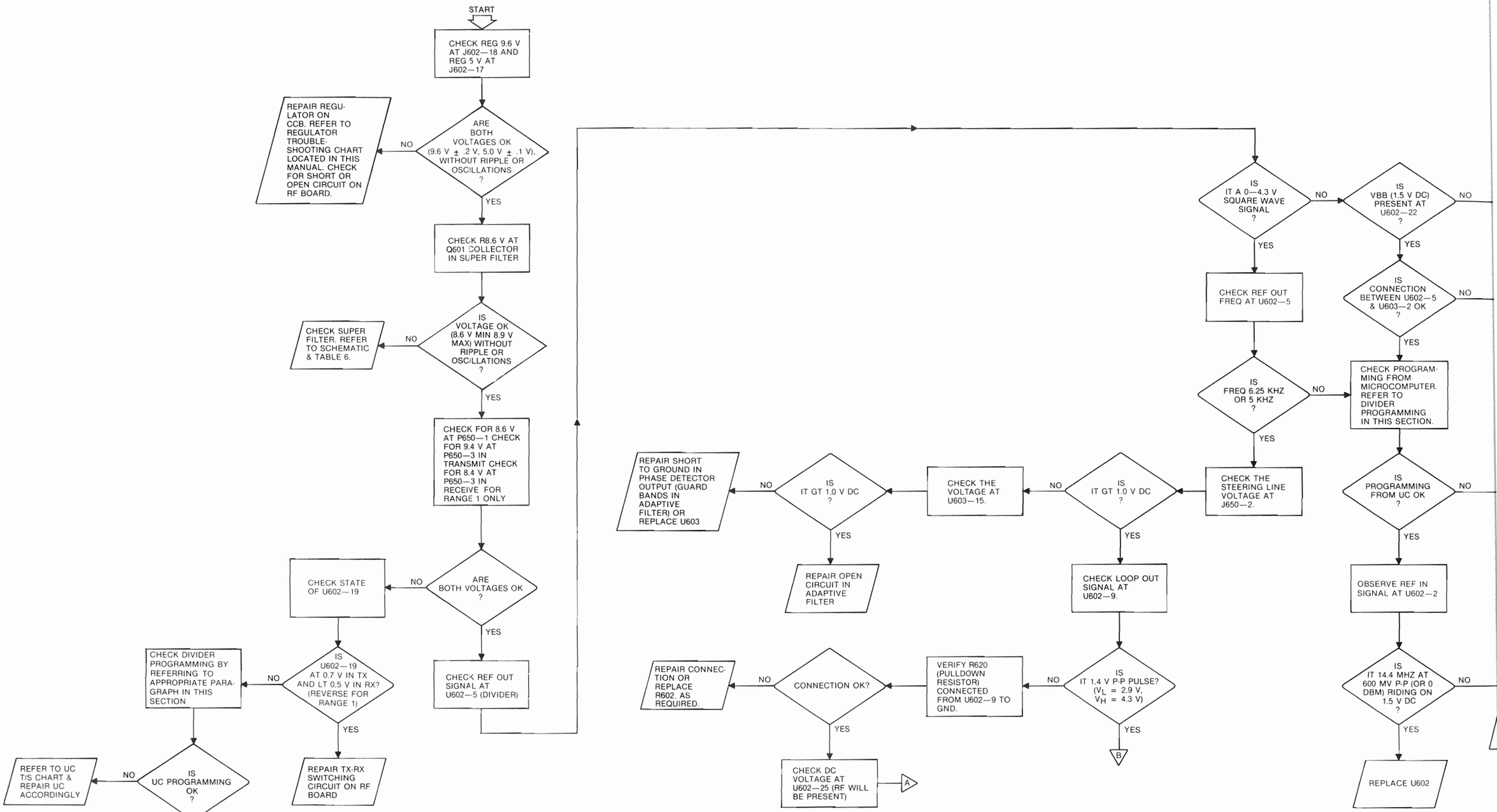
Table 8. Divider (U602) Pin Connections and Voltages

PIN	FUNCTION	TO/FROM	NOMINAL VOLTAGE
1*	GND		0V.
2	REFERENCE IN	From U608 (reference oscillator).	1.5V + 0.6V pp ac (14.4 MHz).
3*	3.6 MHz OUT	To microcomputer.	1V pp (3.6 MHz).
4	GND		0V.
5*	REFERENCE OUT	To U603–2 (phase detector).	0 to 4.3V square wave (4.16, 5, or 6.25 kHz).
6	not connected	—	—
7	not connected	—	—
8	not connected	—	—
9*	LOOP OUT	To phase detector & prescaler.	2.9V to 4.3V narrow pulse (1.4V pp) (200 us nominal period).
10*	VCC	From regulator.	5V.
11	D0	From microcomputer.	0 to 5V pulse train.
12	D1	From microcomputer.	0 to 5V pulse train.
13	D2	From microcomputer.	0 to 5V pulse train.
14	D3	From microcomputer.	0 to 5V pulse train.
15	C0	To prescaler.	0 to 5V.
16	C1	To prescaler.	0 to 5V.
17	LOW BANDWIDTH	To phase detector.	0 to 5V.
18	FREQ CHANGE	To phase detector.	0 to 5V.
19	VCO1 (TX)	To TX–RX switching.	0 to 0.7V.
20	VCO2 ($\overline{\text{RANGE}}$)	To bandshift driver.	0 to 0.7V.
21	not connected	—	—
22	VBB	To divider.	1.5V.
23	A0	From microcomputer.	0 to 5V pulse train.
24	A1	From microcomputer.	0 to 5V pulse train.
25	PRESCALE IN	From prescaler.	1.5V + 0.7V pp ac (approx. 50–80 MHz).
26	A2	From microcomputer.	0 to 5V pulse train.
27*	STROBE	From microcomputer.	0 to 5V pulse train (7 pulses/train).

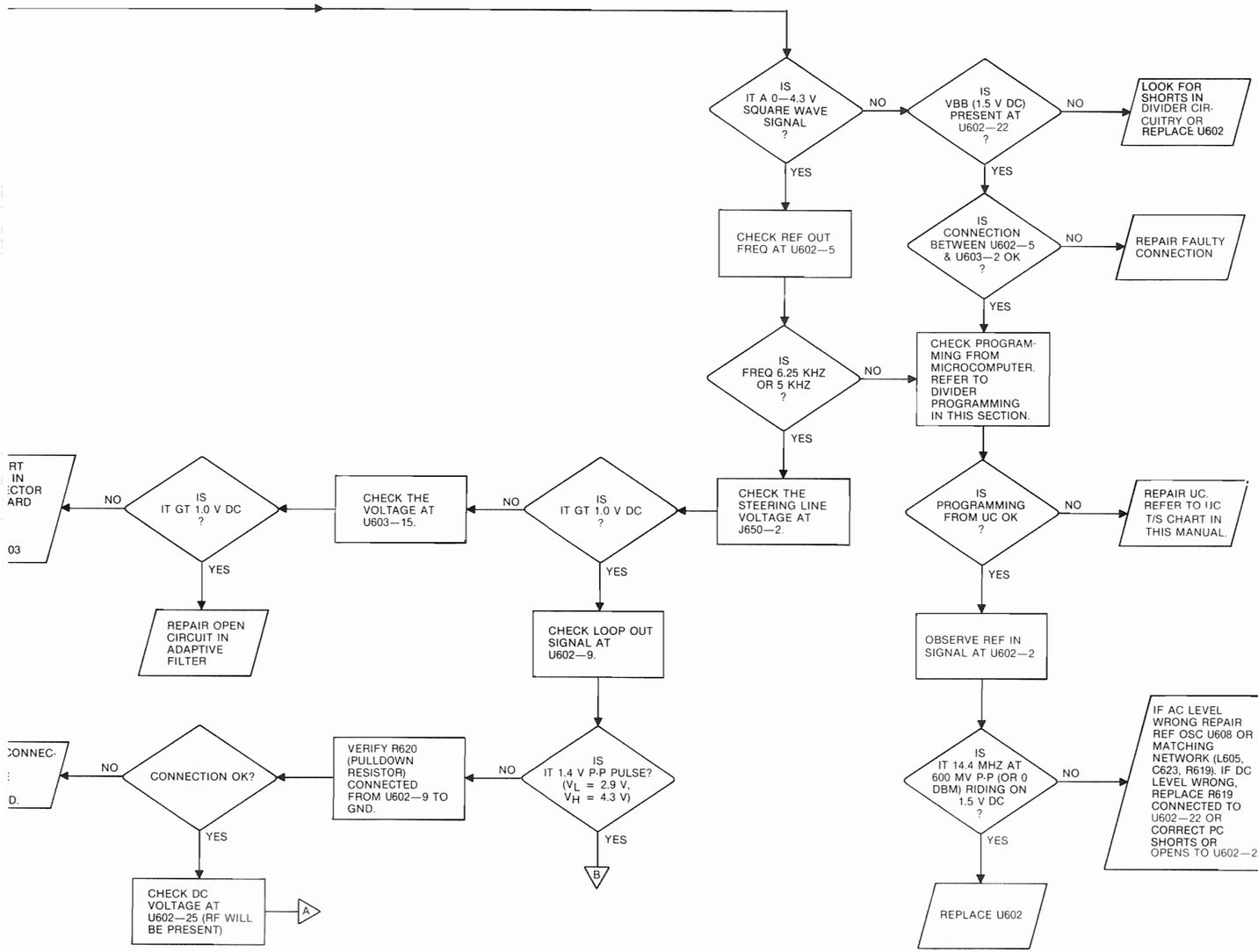
*Should be checked first

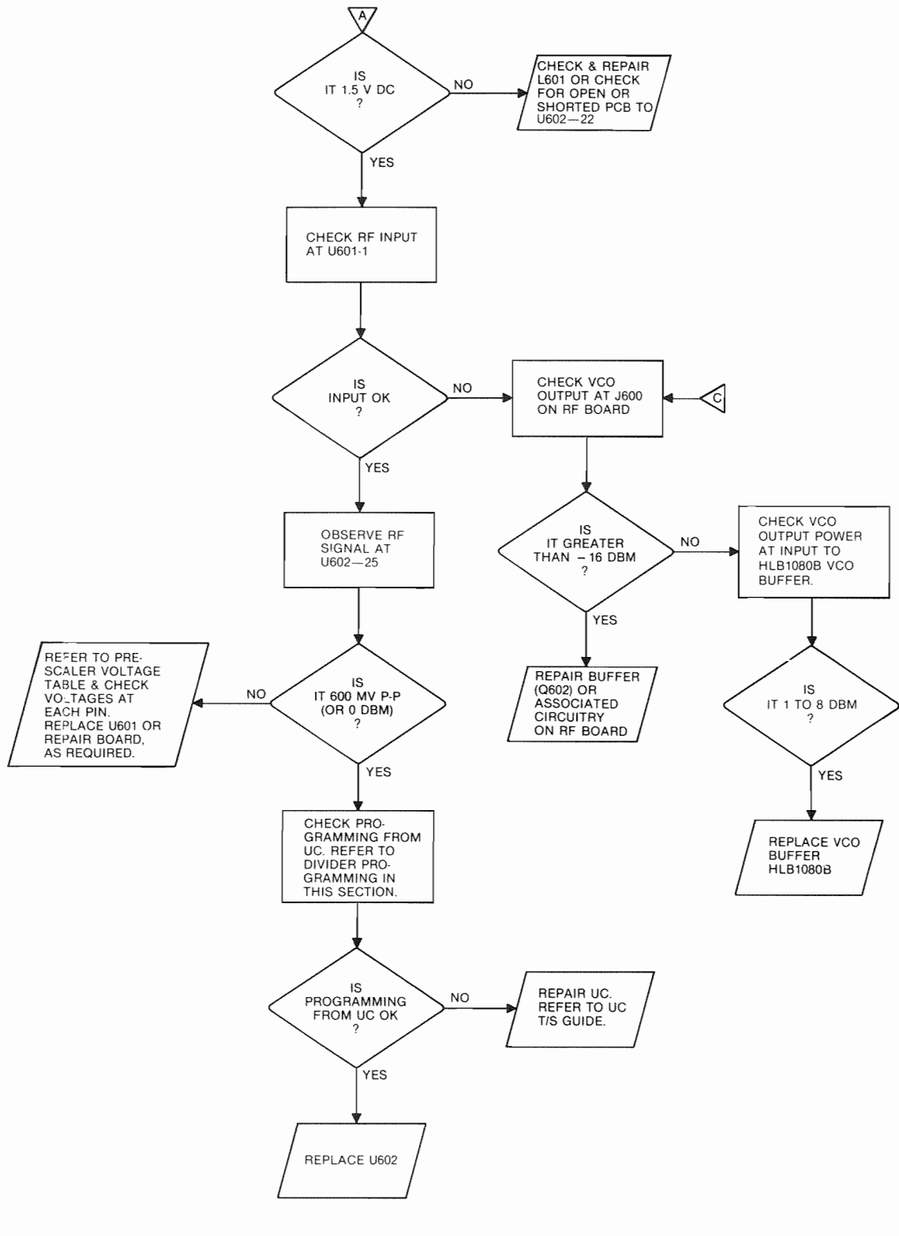
Table 9. Prescaler (U601) Pin Connections and Voltages

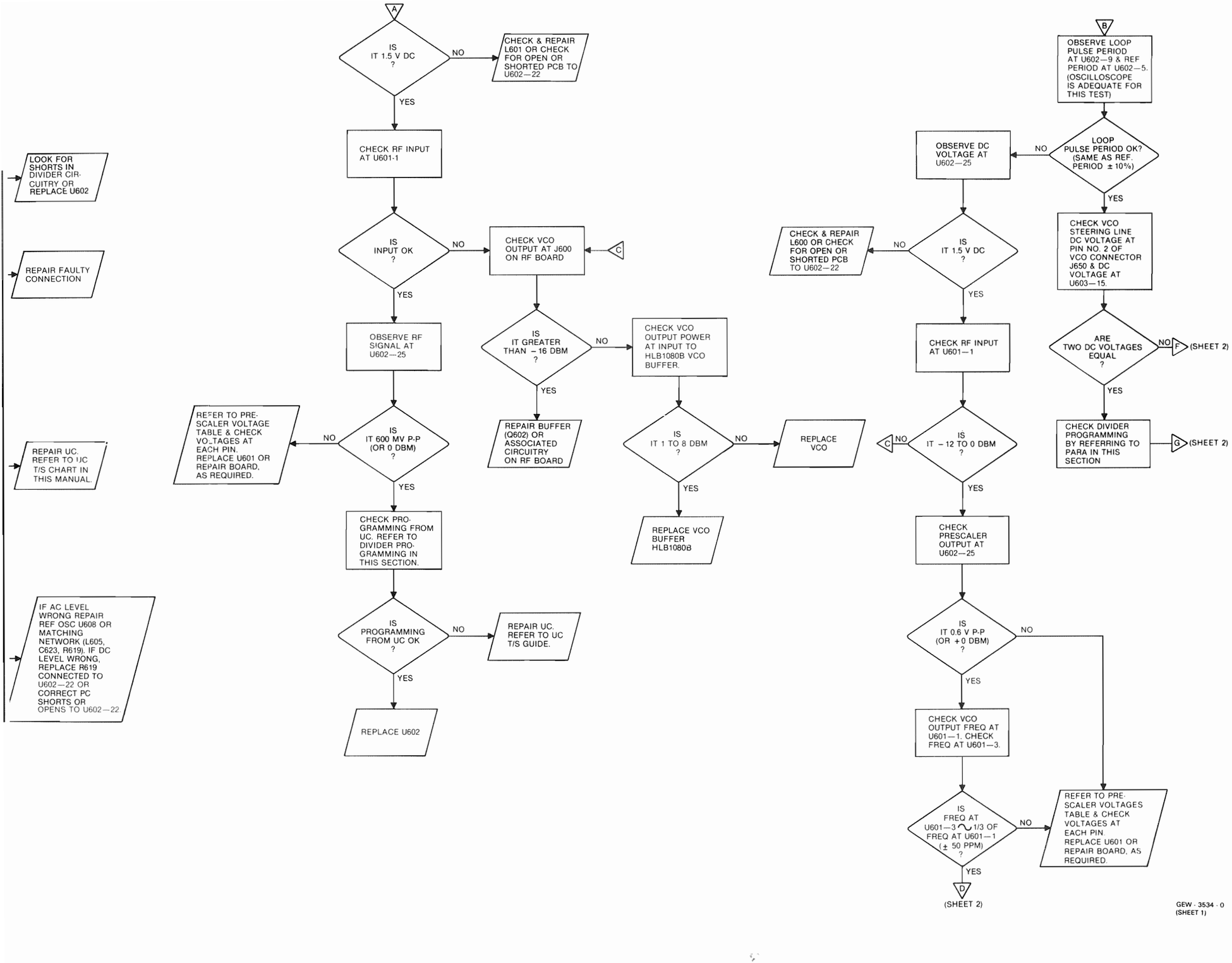
PIN	FUNCTION	TO/FROM	NOMINAL VOLTAGE
1	FIN	from VCO buffer.	–12 to 0 dBm (at half carrier or half first injection frequency) riding on 3.8V.
2	VBB		3.8V, bypassed for RF.
3	PRESCALE OUT	to divider (U602).	0 dBm (0.6V pp) riding on level of 3.6V at approximately one–third VCO frequency (+/–50 ppm).
4	GND		0V.
5	FV	from divider (U602).	1.4V p narrow pulse at reference frequency riding on 3.4V.
6	$\overline{\text{C1}}$	from divider level (programming bit).	0 or 5V; test memory module mode 4– 0V, mode 5– 5V.
7	$\overline{\text{C0}}$	from divider level (programming bit).	0 or 5V; test memory module mode 4– 5V; mode 5– 0V.
8	VCC	from regulator.	+5.0V +/–0.1V.



Troubleshooting Chart for
Syntor X UHF Synthesizer
PW-3533-0
(Sheet 1 of 2)
9/9/86


IS IT A 0—4.3 V SQUARE WAVE SIGNAL ?
NO
IS VBB (1.5 V DC) PRESENT AT U602—22 ?
NO
LOOK FOR SHORTS IN DIVIDER CIR-CUITRY OR REPLACE U602
YES
YES
CHECK REF OUT FREQ AT U602—5
IS CONNECTION BETWEEN U602—5 & U603—2 OK ?
NO
REPAIR FAULTY CONNECTION
YES
IS FREQ 6.25 KHZ OR 5 KHZ ?
NO
CHECK PROGRAM-MING FROM MICROCOMPUTER. REFER TO DIVIDER PROGRAMMING IN THIS SECTION.
YES
CHECK THE STEERING LINE VOLTAGE AT J650—2.
IS PROGRAMMING FROM UC OK ?
NO
REPAIR UC. REFER TO UC T/S CHART IN THIS MANUAL.
YES
OBSERVE REF IN SIGNAL AT U602—2
IS IT 14.4 MHZ AT 600 MV P-P (OR 0 DBM) RIDING ON 1.5 V DC ?
NO
IF AC LEVEL WRONG REPAIR REF OSC U608 OR MATCHING NETWORK (L605, C623, R619). IF DC LEVEL WRONG, REPLACE R619 CONNECTED TO U602—22 OR CORRECT PC SHORTS OR OPENS TO U602—22.
YES
REPLACE U602
IS IT GT 1.0 V DC ?
NO
CHECK THE VOLTAGE AT U603—15.
YES
REPAIR OPEN CIRCUIT IN ADAPTIVE FILTER
IS IT GT 1.0 V DC ?
NO
YES
CHECK LOOP OUT SIGNAL AT U602—9.
IS IT 1.4 V P-P PULSE? (V_L = 2.9 V, V_H = 4.3 V)
NO
VERIFY R620 (PULLDOWN RESISTOR) CONNECTED FROM U602—9 TO GND.
YES
B
CONNECTION OK?
NO
YES
CHECK DC VOLTAGE AT U602—25 (RF WILL BE PRESENT)
A
RT IN CTOR ARD
03
CONNEC-
D.


A
IS IT 1.5 V DC ?
NO
CHECK & REPAIR L601 OR CHECK FOR OPEN OR SHORTED PCB TO U602—22
YES
CHECK RF INPUT AT U601-1
IS INPUT OK ?
NO
CHECK VCO OUTPUT AT J600 ON RF BOARD
C
YES
OBSERVE RF SIGNAL AT U602—25
IS IT GREATER THAN — 16 DBM ?
NO
CHECK VCO OUTPUT POWER AT INPUT TO HLB1080B VCO BUFFER.
YES
REPAIR BUFFER (Q602) OR ASSOCIATED CIRCUITRY ON RF BOARD
REFER TO PRE-SCALER VOLTAGE TABLE & CHECK VOLTAGES AT EACH PIN. REPLACE U601 OR REPAIR BOARD, AS REQUIRED.
IS IT 600 MV P-P (OR 0 DBM) ?
NO
IS IT 1 TO 8 DBM ?
NO
YES
YES
CHECK PRO-GRAMMING FROM UC. REFER TO DIVIDER PRO-GRAMMING IN THIS SECTION.
REPLACE VCO BUFFER HLB1080B
IS PROGRAMMING FROM UC OK ?
NO
REPAIR UC. REFER TO UC T/S GUIDE.
YES
REPLACE U602



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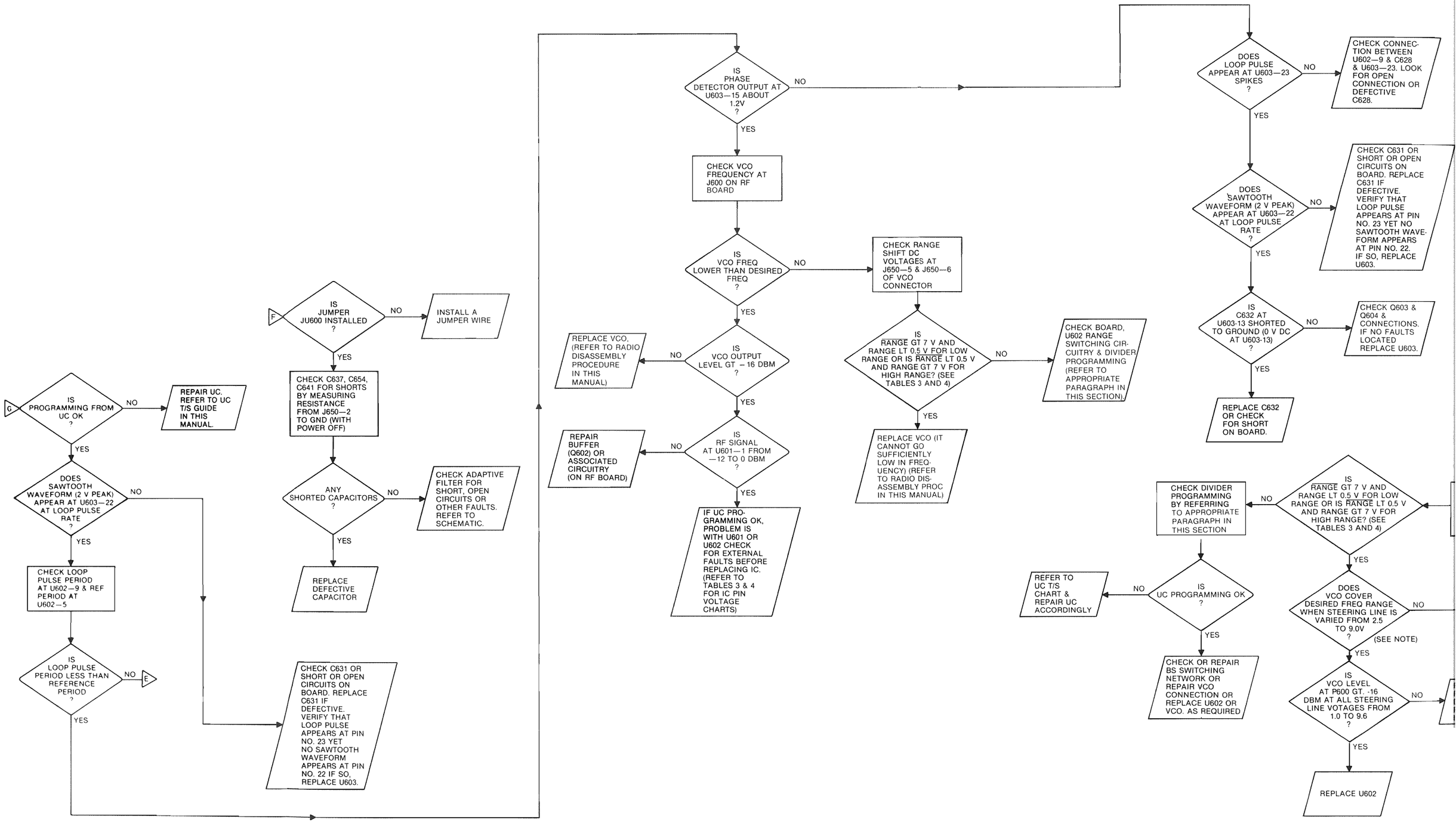

G
IS PROGRAMMING FROM UC OK ?
NO
REPAIR UC. REFER TO UC T/S GUIDE IN THIS MANUAL.
YES
DOES SAWTOOTH WAVEFORM (2 V PEAK) APPEAR AT U603—22 AT LOOP PULSE RATE ?
NO
YES
CHECK LOOP PULSE PERIOD AT U602—9 & REF PERIOD AT U602—5
IS LOOP PULSE PERIOD LESS THAN REFERENCE PERIOD ?
NO
E
YES
F
IS JUMPER JU600 INSTALLED ?
NO
INSTALL A JUMPER WIRE
YES
CHECK C637, C654, C641 FOR SHORTS BY MEASURING RESISTANCE FROM J650—2 TO GND (WITH POWER OFF)
ANY SHORTED CAPACITORS ?
NO
CHECK ADAPTIVE FILTER FOR SHORT, OPEN CIRCUITS OR OTHER FAULTS. REFER TO SCHEMATIC.
YES
REPLACE DEFECTIVE CAPACITOR
CHECK C631 OR SHORT OR OPEN CIRCUITS ON BOARD. REPLACE C631 IF DEFECTIVE. VERIFY THAT LOOP PULSE APPEARS AT PIN NO. 23 YET NO SAWTOOTH WAVEFORM APPEARS AT PIN NO. 22 IF SO, REPLACE U603.
IS PHASE DETECTOR OUTPUT AT U603—15 ABOUT 1.2V ?
NO
YES
CHECK VCO FREQUENCY AT J600 ON RF BOARD
IS VCO FREQ LOWER THAN DESIRED FREQ ?
NO
YES
CHECK RANGE SHIFT DC VOLTAGES AT J650—5 & J650—6 OF VCO CONNECTOR
IS VCO OUTPUT LEVEL GT — 16 DBM ?
NO
REPLACE VCO, (REFER TO RADIO DISASSEMBLY PROCEDURE IN THIS MANUAL)
YES
IS RF SIGNAL AT U601—1 FROM —12 TO 0 DBM ?
NO
REPAIR BUFFER (Q602) OR ASSOCIATED CIRCUITRY (ON RF BOARD)
YES
IF UC PROGRAMMING OK, PROBLEM IS WITH U601 OR U602 CHECK FOR EXTERNAL FAULTS BEFORE REPLACING IC. (REFER TO TABLES 3 & 4 FOR IC PIN VOLTAGE CHARTS)
IS RANGE GT 7 V AND RANGE LT 0.5 V FOR LOW RANGE OR IS RANGE LT 0.5 V AND RANGE GT 7 V FOR HIGH RANGE? (SEE TABLES 3 AND 4)
NO
CHECK BOARD, U602 RANGE SWITCHING CIRCUITRY & DIVIDER PROGRAMMING (REFER TO APPROPRIATE PARAGRAPH IN THIS SECTION)
YES
REPLACE VCO (IT CANNOT GO SUFFICIENTLY LOW IN FREQUENCY) (REFER TO RADIO DISASSEMBLY PROC IN THIS MANUAL)
DOES LOOP PULSE APPEAR AT U603—23 SPIKES ?
NO
CHECK CONNECTION BETWEEN U602—9 & C628 & U603—23. LOOK FOR OPEN CONNECTION OR DEFECTIVE C628.
YES
DOES SAWTOOTH WAVEFORM (2 V PEAK) APPEAR AT U603—22 AT LOOP PULSE RATE ?
NO
CHECK C631 OR SHORT OR OPEN CIRCUITS ON BOARD. REPLACE C631 IF DEFECTIVE. VERIFY THAT LOOP PULSE APPEARS AT PIN NO. 23 YET NO SAWTOOTH WAVEFORM APPEARS AT PIN NO. 22. IF SO, REPLACE U603.
YES
IS C632 AT U603-13 SHORTED TO GROUND (0 V DC AT U603-13) ?
NO
CHECK Q603 & Q604 & CONNECTIONS. IF NO FAULTS LOCATED REPLACE U603.
YES
REPLACE C632 OR CHECK FOR SHORT ON BOARD.
IS RANGE GT 7 V AND RANGE LT 0.5 V FOR LOW RANGE OR IS RANGE LT 0.5 V AND RANGE GT 7 V FOR HIGH RANGE? (SEE TABLES 3 AND 4)
NO
CHECK DIVIDER PROGRAMMING BY REFERRING TO APPROPRIATE PARAGRAPH IN THIS SECTION
YES
IS UC PROGRAMMING OK ?
NO
REFER TO UC T/S CHART & REPAIR UC ACCORDINGLY
YES
CHECK OR REPAIR BS SWITCHING NETWORK OR REPAIR VCO CONNECTION OR REPLACE U602 OR VCO. AS REQUIRED
DOES VCO COVER DESIRED FREQ RANGE WHEN STEERING LINE IS VARIED FROM 2.5 TO 9.0V ?
NO
(SEE NOTE)
YES
IS VCO LEVEL AT P600 GT. -16 DBM AT ALL STEERING LINE VOTAGES FROM 1.0 TO 9.6 ?
NO
YES
REPLACE U602

DOES LOOP PULSE APPEAR AT U603—23 SPIKES ?

NO → CHECK CONNECTION BETWEEN U602—9 & C628 & U603—23. LOOK FOR OPEN CONNECTION OR DEFECTIVE C628.

YES

DOES SAWTOOTH WAVEFORM (2 V PEAK) APPEAR AT U603—22 AT LOOP PULSE RATE ?

NO → CHECK C631 OR SHORT OR OPEN CIRCUITS ON BOARD. REPLACE C631 IF DEFECTIVE. VERIFY THAT LOOP PULSE APPEARS AT PIN NO. 23 YET NO SAWTOOTH WAVEFORM APPEARS AT PIN NO. 22. IF SO, REPLACE U603.

YES

IS C632 AT U603-13 SHORTED TO GROUND (0 V DC AT U603-13) ?

NO → CHECK Q603 & Q604 & CONNECTIONS. IF NO FAULTS LOCATED REPLACE U603.

YES

REPLACE C632 OR CHECK FOR SHORT ON BOARD.

CHECK BOARD, U602 RANGE SWITCHING CIRCUITRY & DIVIDER PROGRAMMING (REFER TO APPROPRIATE PARAGRAPH IN THIS SECTION).

D

CHECK RANGE-SHIFT DC VOLTAGES AT J650—5 & J650—6 OF VCO CONNECTOR

IS RANGE GT 7 V AND RANGE LT 0.5 V FOR LOW RANGE OR IS RANGE LT 0.5 V AND RANGE GT 7 V FOR HIGH RANGE? (SEE TABLES 3 AND 4)

NO → CHECK DIVIDER PROGRAMMING BY REFERRING TO APPROPRIATE PARAGRAPH IN THIS SECTION

YES

DOES VCO COVER DESIRED FREQ RANGE WHEN STEERING LINE IS VARIED FROM 2.5 TO 9.0V ?

NO → REPLACE VCO, REFER TO DISASSEMBLY PROCEDURE IN MANUAL.

(SEE NOTE)

YES

IS VCO LEVEL AT P600 GT. -16 DBM AT ALL STEERING LINE VOTAGES FROM 1.0 TO 9.6 ?

NO → REPLACE VCO, REFER TO DISASSEMBLY PROCEDURE IN MANUAL.

YES

REPLACE U602

IS UC PROGRAMMING OK ?

NO → R TO T & R UC RDINGLY

YES

CHECK OR REPAIR BS SWITCHING NETWORK OR REPAIR VCO CONNECTION OR REPLACE U602 OR VCO. AS REQUIRED

E

IS VOLTAGE AT U603—15 APPROX. 9.5 V ?

NO → IS REF SQUARE WAVE PRESENT AT U603—2 ?

NO → REPAIR PC BOARD CONNECTION

YES

IS RAMP CAPACITOR (C630) SHORTED ?

NO → CHECK Q603, R624, R625, RT600, R626, C629 & THEIR CONNECTIONS. IF NO EXTERNAL FAULTS FOUND, REPLACE U603

YES

REPLACE C630 OR LOOK FOR SHORTS ON THE PCB

YES

CHECK VCO FREQUENCY AT J600 ON RF BOARD

IS VCO FREQ HIGHER THAN DESIRED FREQ ?

SEE NOTE

NO → CHECK RANGE-SHIFT DC VOLTAGES AT J650—5 & 6 (VCO CONNECTOR)

IS RANGE GT 7 V AND RANGE LT 0.5 V FOR LOW RANGE OR IS RANGE LT 0.5 V AND RANGE GT 7 V FOR HIGH RANGE? (SEE TABLES 3 AND 4)

NO → CHECK PC BOARD DIVIDER IC (U602—20) & BS SWITCHING NETWORK

YES

REPLACE VCO (IT CANNOT GO SUFFICIENTLY HIGH IN FREQUENCY) (REFER TO RADIO DISASSEMBLY PROC IN MANUAL.

YES

CHECK VCO OUTPUT LEVEL AT J600 (RF BOARD CONNECTOR)

IS VCO OUTPUT LEVEL GT – 16 DBM ?

NO → REPLACE VCO (REFER TO RADIO DISASSEMBLY PROC IN MANUAL)

YES

IS PRESCALER INPUT AT U601—1 FROM —12 DBM TO 0 DBM ?

NO → REPAIR BUFFER (Q602) OR ASSOCIATED CIRCUITRY (ON RF BOARD)

YES

IF UC PROGRAMMING OK, THEN PROBLEM WITH U602 OR U601. CHECK ALL EXTERNAL CONNECTIONS BEFORE REPLACING AN IC. (REFER TO TABLES 3 & 4 FOR IC PIN VOLTAGE CHARTS.)

SYMBOLS AND ABBREVIATIONS USED IN THE CHART

= TEST TO BE DONE

= DECISION

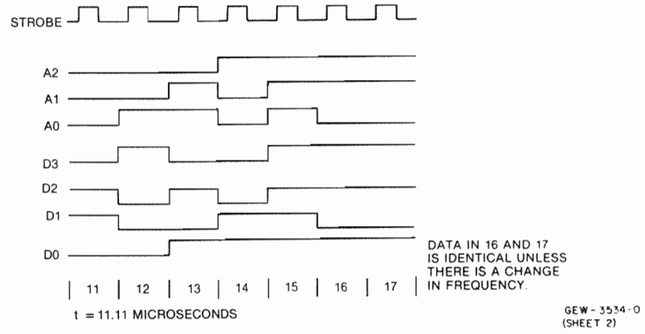
= SOURCE OF FAULT

BS = BANDSHIFT
U601-1 = PIN NO. 1 OF U601
PCB = PRINTED CIRCUIT BOARD
LT = LESS THAN
GT = GREATER THAN
T/S = TROUBLESHOOTING
UC = MICROCOMPUTER
CCB = COMMON CIRCUIT BOARD

NOTE:

1. TEST MUST BE PERFORMED WITH TOP COVER ON.

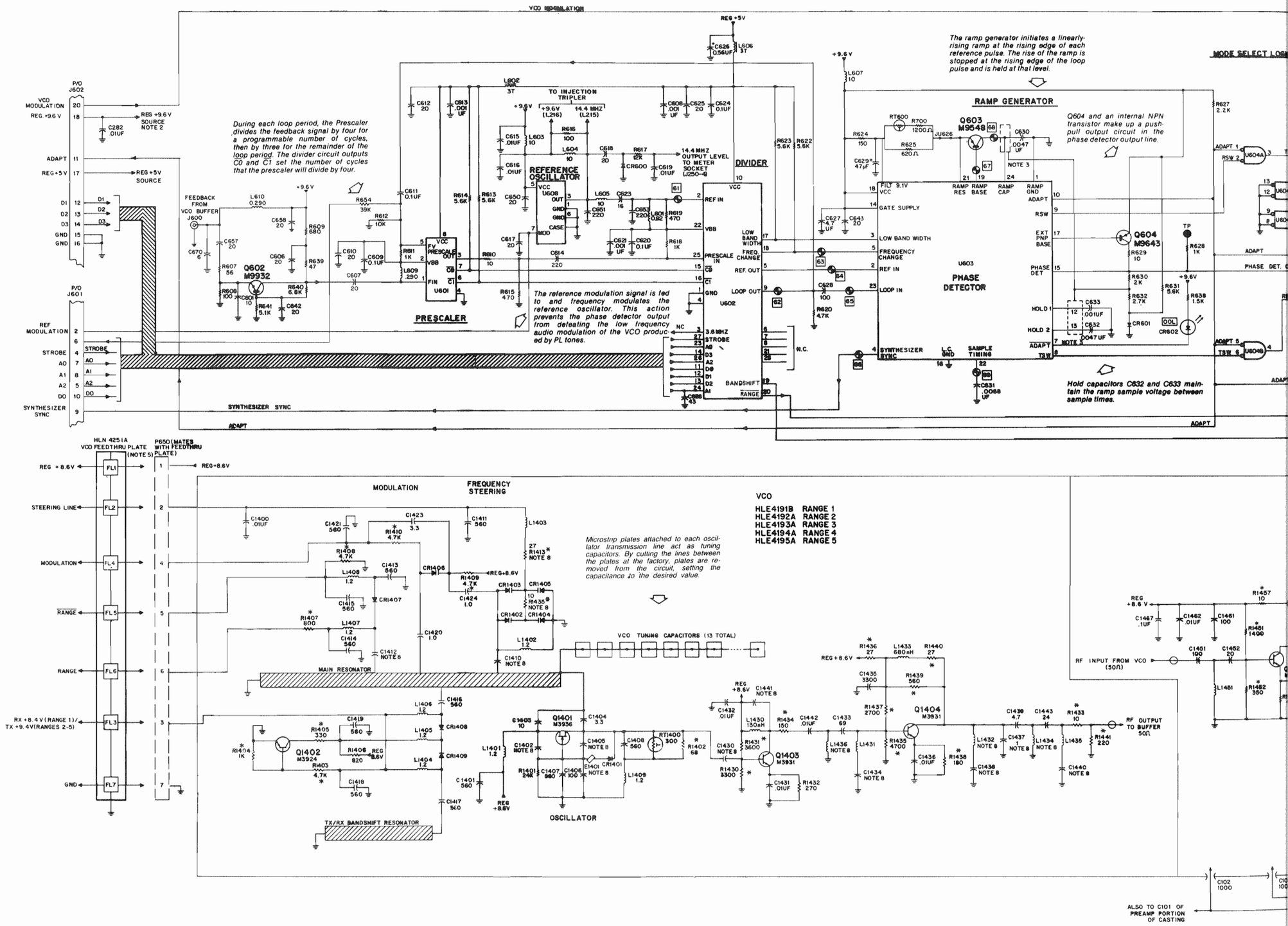
EXAMPLE TIMING DIAGRAM



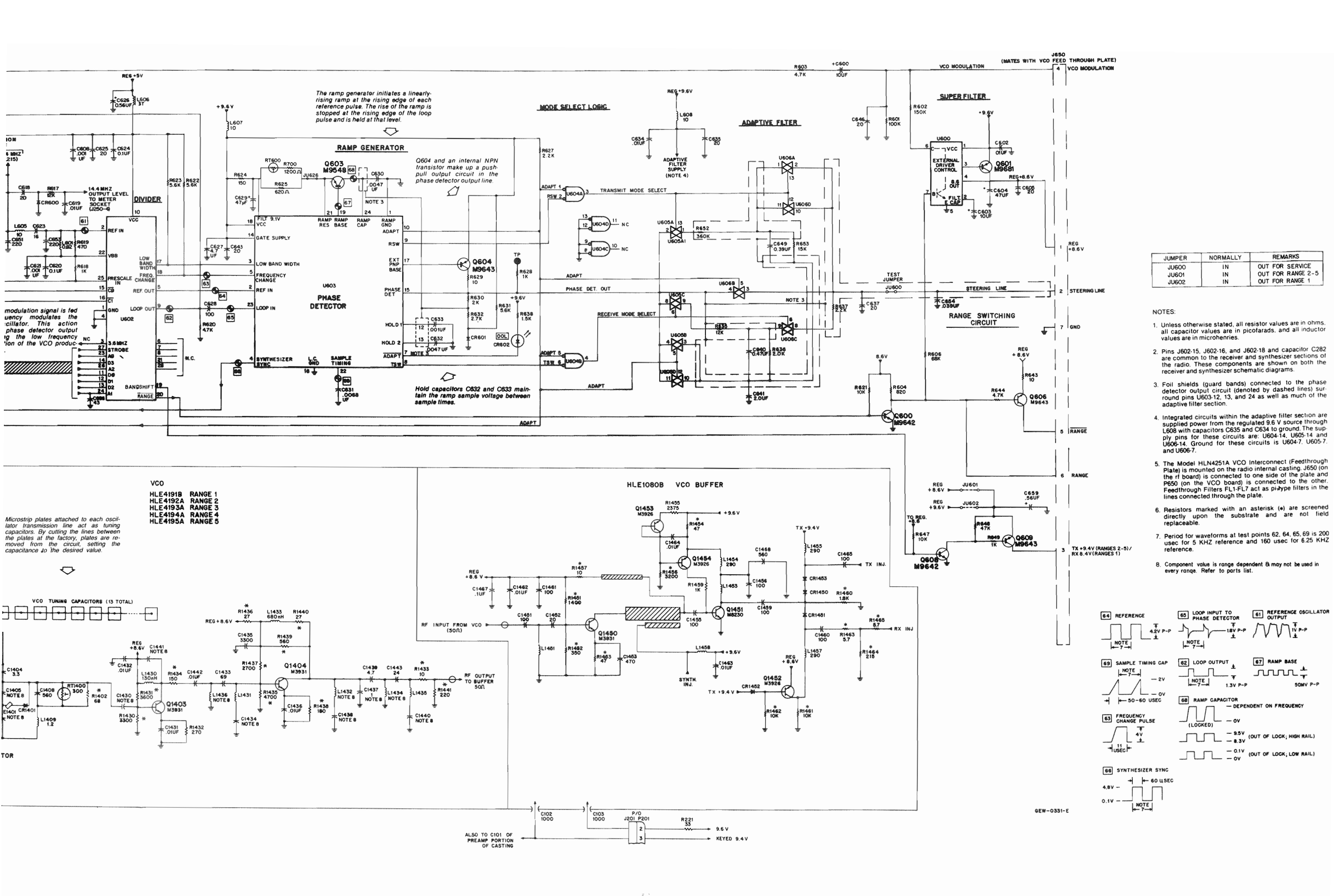
GEW-3534-0 (SHEET 2)

Troubleshooting Chart for *Syntor X* UHF Synthesizer
PW-3533-0
(Sheet 2 of 2)
9/9/86

Frequency Synthesizer
Schematic



Schematic, Circuit Board Diagram, and Parts Lists for Frequency Synthesizer
PW–0332–H
(Sheet 1 of 3)
9/30/88



JUMPER	NORMALLY	REMARKS
JU600	IN	OUT FOR SERVICE
JU601	IN	OUT FOR RANGE 2-5
JU602	IN	OUT FOR RANGE 1

NOTES:

1. Unless otherwise stated, all resistor values are in ohms, all capacitor values are in picofarads, and all inductor values are in microhenries.
2. Pins J602-15, J602-16, and J602-18 and capacitor C282 are common to the receiver and synthesizer sections of the radio. These components are shown on both the receiver and synthesizer schematic diagrams.
3. Foil shields (guard bands) connected to the phase detector output circuit (denoted by dashed lines) surround pins U603-12, 13, and 24 as well as much of the adaptive filter section.
4. Integrated circuits within the adaptive filter section are supplied power from the regulated 9.6 V source through L608 with capacitors C635 and C634 to ground. The supply pins for these circuits are: U604-14, U605-14 and U606-14. Ground for these circuits is U604-7, U605-7, and U606-7.
5. The Model HLN4251A VCO Interconnect (Feedthrough Plate) is mounted on the radio internal casting. J650 (on the rf board) is connected to one side of the plate and P650 (on the VCO board) is connected to the other. Feedthrough Filters FL1-FL7 act as pi-type filters in the lines connected through the plate.
6. Resistors marked with an asterisk (*) are screened directly upon the substrate and are not field replaceable.
7. Period for waveforms at test points 62, 64, 65, 69 is 200 usec for 5 KHZ reference and 160 usec for 6.25 KHZ reference.
8. Component value is range dependent & may not be used in every range. Refer to parts list.

parts list

HLN4462B RF Board Ranges 1, 3, 4, & 5 (Synthesizer section)
HLN5215A RF Board Range 2 (Synthesizer section)
HLN5424A RF Board Ranges 1, 3, 4, & 5 (Synthesizer section)
HLN5423A RF Board Range 2 (Synthesizer section) MXW–1114–D

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
capacitor, fixed, pF, ±5%, 100V (unless otherwise stated)		
C600	23–11013E57	10 uF, ±20%, 25V, tantalum
C601	21–11014H25	10, ±.5pF
C602	08–11051A07	.01 uF, 63V
C603	23–11013E57	10 uF, ±20%, 25V, tantalum
C604	23–82783B31	47 uF, 20V
C605–607	21–11014H32	20
C608	08–11051A01	.001 uF, 63V
C609	08–11051A13	.1 uF, 63V
C610	21–11014H32	20
C611	08–11051A13	.1 uF, 63V
C612	21–11014H32	20
C613	08–11051A01	.001 uF, 63V
C614	21–11015B05	220, ±10%
C615,616	08–11051A07	.01 uF, 63V
C617,618	21–11014H32	20
C619	08–11051A07	.01 uF, 63V
C620	08–11051A13	.1 uF, 63V
C621	08–11051A01	.001 uF, 63V
C623	21–11014H30	16
C624	08–11051A13	.1 uF, 63V
C625	21–11014H32	20
C626	23–11013F10	.56 uF, ±10%, 35V, tantalum
C627	23–11013D55	4.7 uF, ±20%, 20V, tantalum
C628	21–11015B01	100, ±10%, 100V
C629	23–11019A39	47 uF, ±20%, 16V, electrolytic
C630	08–80027B02	.0047 uF
C631	08–11017B07	.0068, ±10%, 50V
C632	08–11051A05	.0047 uF, 63V
C633	08–11017B01	.001 uF, ±10%, 50V
C634	08–11051A07	.01 uF, 63V
C635,637	21–11014H32	20
C640	08–84637L42	.47, ±10%
C641	08–83862M02	2 uF, ±10%
C642–643	21–11014H32	20
C646	21–11014H32	20
C649	08–84637L39	.39 uF, ±10%
C650	21–11014H32	20
C651,653	21–11015B05	220, ±10%
C654	08–80027B04	.039 uF
C655,656	21–83406D87	43, 500V
C657,658	21–11014H32	20
C659	23–84538G24	.56 uF, ±10%, 35V, tantalum
C670	21–82204B03	6, ±.5 pF, 500V (HLN5251A Only)
diode (see note)		
CR600	48–82139G01	germanium
CR601	48–83329G02	silicon
CR602	48–84404E01	LED
connector receptacle		
J600	09–80001F01	phono jack, female (board mounting)
J601–602	09–83445L09	10 contact, female
J650	09–83730M01	7 contact, female
jumper		
JU600	06–11009D23	0 ohm
JU601	06–11009F23	0 ohm (HLN4462B Only)
JU602	06–11009D23	0 ohm
JU626	06–11009B23	0 ohm
coil, rf		
L601	24–83397L13	.82 uH, choke
L602	24–83961B01	3 turns, coded brown
L603–604	24–82723H45	10 uH, choke
L605	24–83397L07	10 uH, choke
L606	24–83961B01	3 turns, coded brown
L607–608	24–82723H45	10 uH, choke
L609–610	24–82723H28	.29 uH
transistor (see note)		
Q600	48–11043C05	NPN, type M9642
Q601	48–11043C10	PNP, type M9681
Q602	48–11043C16	NPN, type M9932
Q603	48–00869548	PNP, type M9548
Q604, 606	48–11043C06	PNP, type M9643
Q608	48–11043C05	NPN, type M9642
Q609	48–11043C06	PNP, type M9643
thermistor		
RT600	06–80275N01	1k
resistor, fixed, ohm, ± 5%, 1/4 watt (unless otherwise stated)		
R601	06–11009A97	100k
R602	06–11009B02	150k
R603	06–11009A73	10k
R604	06–11009A47	820
R606	06–11009A93	68k
R607	06–11009A19	56
R608	06–11009C25	100
R609	06–11009A45	680
R610	06–11009A01	10
R611	06–11009A49	1k
R612	06–11009A73	10k
R613–614	06–11009A67	5.6k
R615	06–11009A41	470
R616	06–11009A25	100
R617	06–11009A75	12k

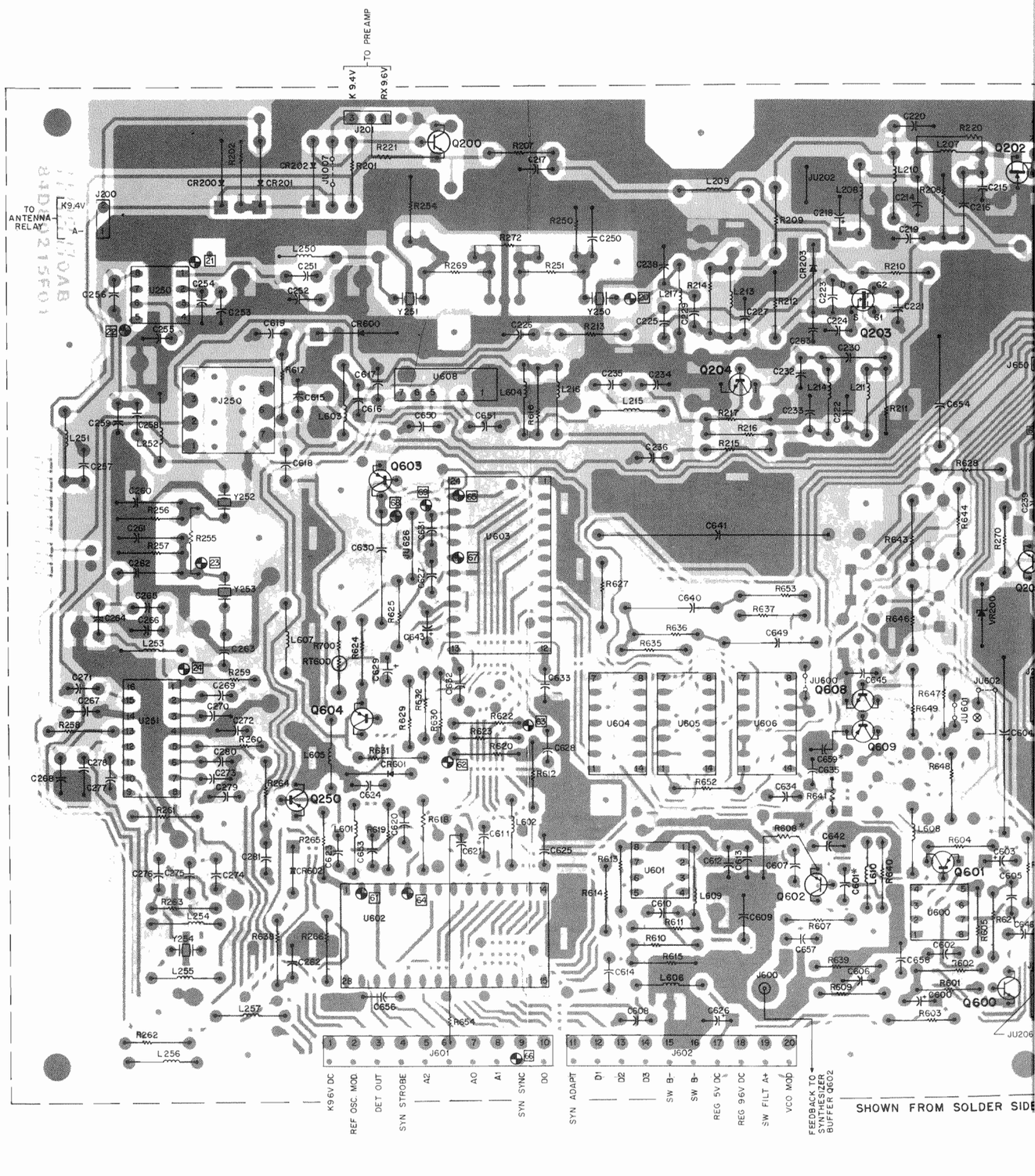
MXW–1114–D (2)

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R618	06–11009A49	1k
R619	06–11009A41	470
R620	06–11009A65	4.7k
R621	06–11009A73	10k
R622–623	06–11009A67	5.6k
R624	06–11009A29	150
R625	06–11009A44	620
R627	06–11009A57	2.2k
R628	06–11009A49	1k
R629	06–11009A01	10
R630	06–11009A56	2k
R631	06–11009C67	5.6k
R632	06–11009A59	2.7k
R635	06–11009A75	12k
R636	06–11009A56	2k
R637	06–11009A57	2.2k
R638	06–11009A53	1.5k
R639	06–11009A17	47
R640	06–11009C69	6.8k
R641	06–11009C66	5.1k
R643	06–11009A01	10
R644	06–11009A65	4.7k
R647	06–11009A73	10k
R648	06–11009A89	47k
R649	06–11009A49	1k
R652	06–11009B11	360k
R654	06–11009C87	39k (HLN5423A, HLN5424A only)
R653	06–11009A77	15k
R700	06–11009C51	1.2k
integrated circuit (see note)		
U600	51–84768F65	super filter, type M6865
U601	51–80235C10	prescaler, type M3510
U602	51–84768F63	divider, type M6863
U603	51–83977M36	phase detector, type M7736
	or	
	51–84768F59	type M6859
U604	51–80072C01	two–input quad NOR gate, type M7201
U605	51–80073C02	quad analog switch, type M7302
U606	51–80073C03	quad analog switch, type M7303
U608	51–80291B02	reference oscillator, type M9102
mechanical parts		
E600	26–80284G01	component side shield
E601	05–84220B01	snap in rivet
E601	26–83597M01	component side prescaler shield
E602	26–83814M01	fence shield
E603	26–84978M01	shield
E604	26–83593M01	synthesizer, component side shield
E605	26–80207D02	synthesizer shield
E606	26–84862M02	solder side shield
MP600	46–83948M01	board stud

8/10/88

note: For best performance, order diodes, transistors, and integrated circuit devices by Motorola part number.

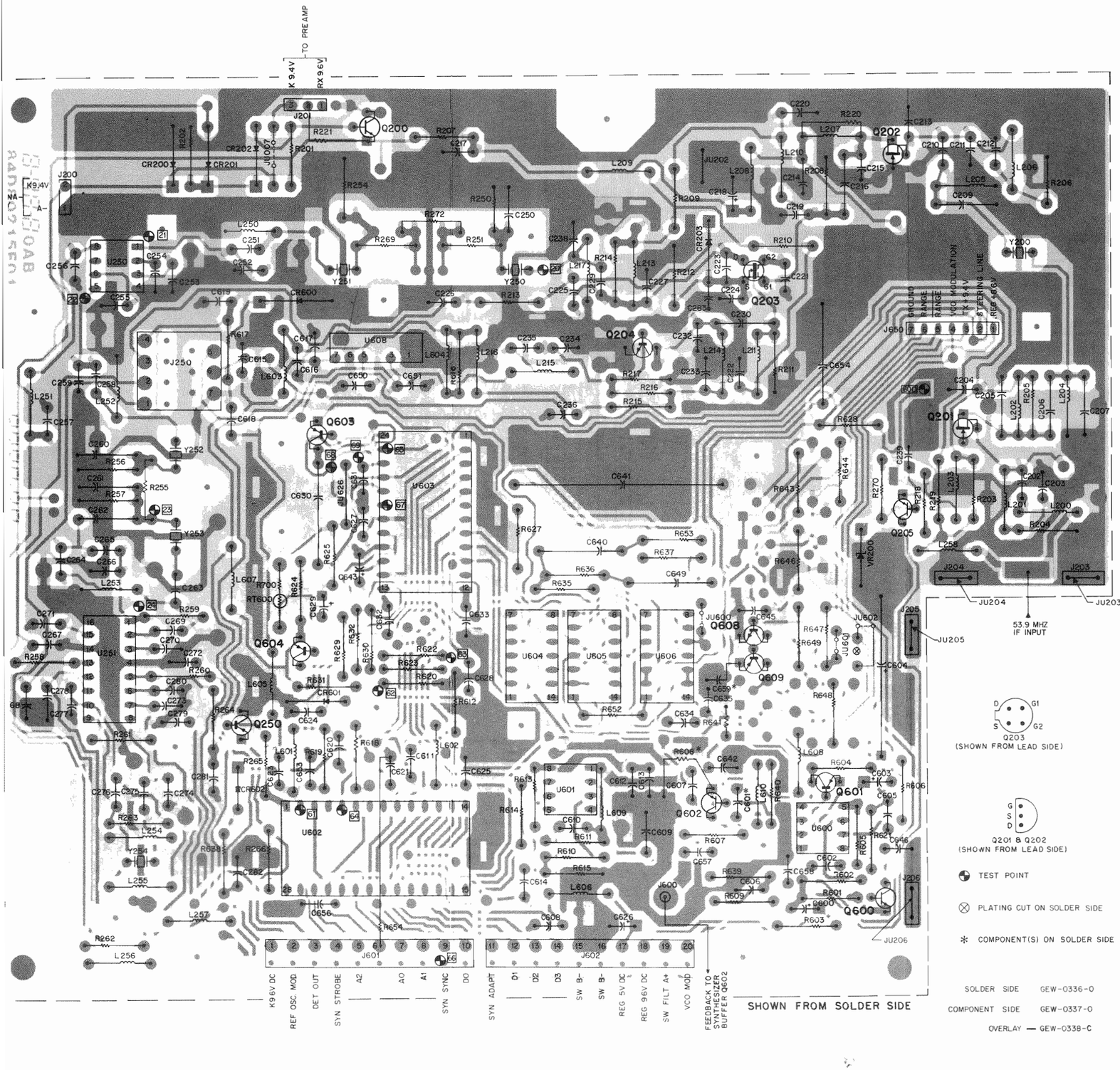
HLN5215A/HLN4462B RF BOARD



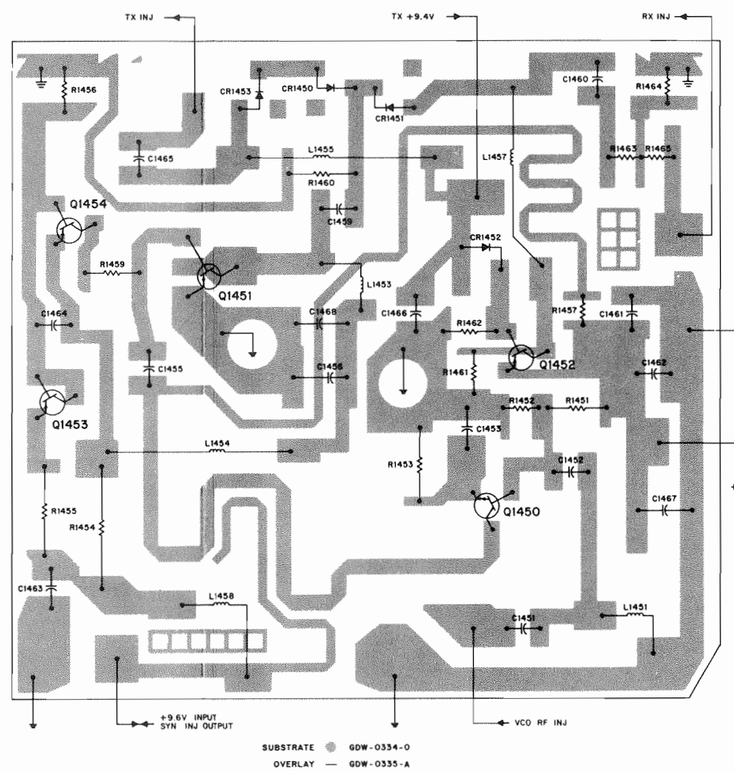
RF BOARD, VCO, AND VCO BUFFER

Circuit Board Diagram and Parts Lists

HLN5215A/HLN4462B RF BOARD



HLE1080B VCO BUFFER



HKN4157A VCO Buffer Cable MXW–2758–A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	05–00136977	eyelet (2 used)
	28–82365D02	coax plug
	37–00132251	heat shrink tubing
	76–83466K01	ferrite bead core (2 used)

5/01/88

SYNTHESIZER

Schematic, Circuit Board Diagram, and Parts Lists for Frequency Synthesizer
PW–0332–H
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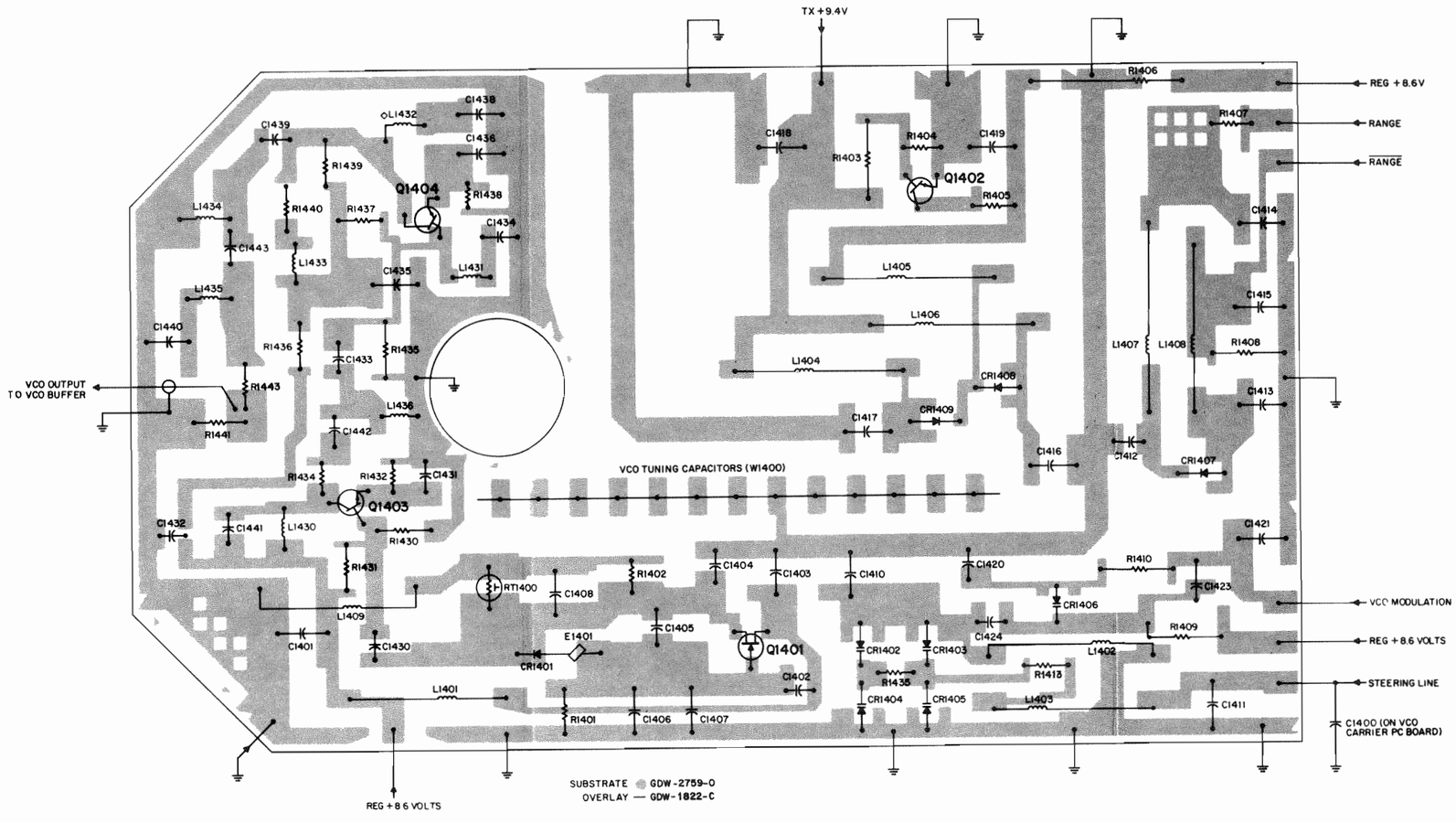
VCO
HLE4191C RANGE 1
HLE4192B RANGE 2
HLE4193A RANGE 3
HLE4194A RANGE 4
HLE4195A RANGE 5



Schematic, Circuit Board Diagram, and
Parts Lists for Frequency Synthesizer
PW–0332–H
(Sheet 3 of 3)
9/30/88

parts list

HLE4191C VCO (Range 1)
HLE4192B VCO (Range 2)
HLE4193A VCO (Range 3)
HLE4194A VCO (Range 4)
HLE4195A VCO (Range 5)

MXW–0342–G

RANGE 1	2	3	4	5	REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
					capacitor, fixed, pF, ±5%, 100V (unless otherwise stated)		
●	●	●	●	●	C1400	21–83162H36	.01 uF, 50V
●	●	●	●	●	C1401	21–13740C11	560, 50V
●	●				C1402	21–11078A17	3.3, ±.25 pF
		●	●	●	C1402	21–11078A21	4.7, ±.25 pF
●	●	●	●	●	C1403	21–11078B13	10, ±.5 pF
●	●	●	●	●	C1404	21–11078A17	3.3, ±.25 pF
●					C1405	21–11078A21	4.7, ±.25 pF
	●	●	●	●	C1405	21–11078A13	2.2, ±.25 pF
●	●	●	●	●	C1406	21–11078B42	100
●	●	●	●	●	C1407,1408	21–13740C11	560, 50V
●		●	●		C1410	21–11078B15	12
				●	C1410	21–11078B13	12
	●				C1410	21–11078B16	13
●	●	●	●	●	C1411	21–13740C11	560, 50V
●			●	●	C1412	21–11078A17	3.3; ±.25 pF
	●	●			C1412	21–11078A21	4.7, ±.25 pF
●	●	●	●	●	C1413–1419	21–13740C11	560, 50V
●	●	●	●	●	C1420	21–11078A01	1.0, ±.25 pF
●	●	●	●	●	C1421	21–13740C11	560, 50V
●	●	●	●	●	C1423	21–11078A17	3.3, ±.25 pF
●	●	●	●	●	C1424	21–11078A01	1.0, ±.25 pF
●	●	●	●		C1430	21–11078A15	2.7, ±.25 pF
				●	C1430	21–11078A13	2.2, ±.25 pF
●	●	●	●	●	C1431,1432	21–13741M45	.01 uF, ±10%, 50V
●	●	●	●	●	C1433	21–05157A88	69, 50V
●	●				C1434	21–13740A33	15, 50V
		●			C1434	21–13740B28	16, 50V
			●	●	C1434	21–13740A31	12, 50V
●	●	●	●	●	C1435	21–84547A17	3300, ±20%, 25V
●	●	●	●	●	C1436	21–13741M45	.01 uF, ±10%, 50V
●					C1438	21–13740A39	27, 50V
		●	●		C1438	21–13740B33	22, 50V
				●	C1438	21–13740B32	20, 50V
	●				C1438	21–05157A83	22, ±2%, 50V
●	●	●	●	●	C1439	21–11078A21	4.7, ±.25 pF
●	●	●	●	●	C1440	21–11078B09	6.8, ±.25 pF
				●	C1440	21–11078B07	5.6, ±.25 pF
●	●				C1441	21–11078A21	4.7 pF, ±.25 pF
		●	●	●	C1441	21–11078A17	3.3, ±.25 pF
●	●	●	●	●	C1442	21–13741M45	.01 uF, ±10%, 50V
●	●	●	●	●	C1443	21–13740A38	24, 50V
					diode (see note)		
●	●	●	●	●	CR1401	48–84616A11	hot carrier
●	●				CR1402–1406	48–80006E10	silicon
		●	●	●	CR1402–1406	48–80006E11	silicon
●	●	●	●	●	CR1407–1409	48–84622E02	PIN, silicon
					ferrite bead		
●		●	●	●	E1401	76–80178D02	core
					connector receptacle		
●	●	●	●	●	J1400	09–83729M01	7–contact
●	●	●	●	●	P1400	07–80162D01	lead frame
					RF coil		
●	●	●	●	●	L1401–1409	24–82723H27	1.2 uH, green
●	●	●	●	●	L1430	24–80140E06	130 nH
●	●	●	●	●	L1431	24–80091G09	airwound
●					L1432	24–80091G05	airwound
	●	●	●	●	L1432	24–80091G24	airwound
●	●	●	●	●	L1433	24–80140E07	680 nH
●	●				L1434	24–80091G05	airwound
		●	●	●	L1434	24–80091G21	airwound
●	●	●	●	●	L1435	24–80091G06	airwound
●	●	●			L1436	24–80091G05	airwound
			●	●	L1436	24–80091G21	airwound
					transistor (see note)		
●	●	●	●	●	Q1401	48–84939C36	FET
●	●	●	●	●	Q1402	48–84939C24	NPN
●	●	●	●	●	Q1403,1404	48–84939C31	NPN
					resistor, fixed, ohm, ±5%, 1/4 watt (unless otherwise stated)		
●	●	●	●	●	R1401	06–11077B08	24k, 1/8W
●	●	●	●	●	R1406	06–11009C47	820
					thermistor		
●	●	●	●	●	RT1400	06–00865641	300

note: For best performance, order diodes, transistors, and integrated circuits by Motorola part number. 9/30/88