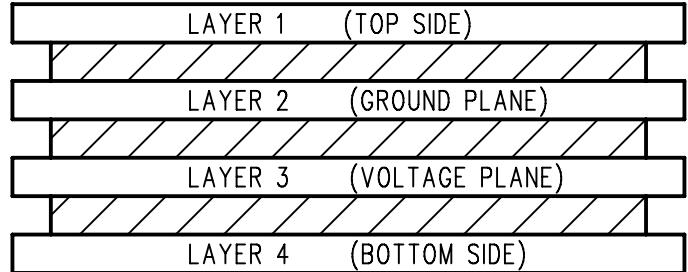


LAYUP DETAIL

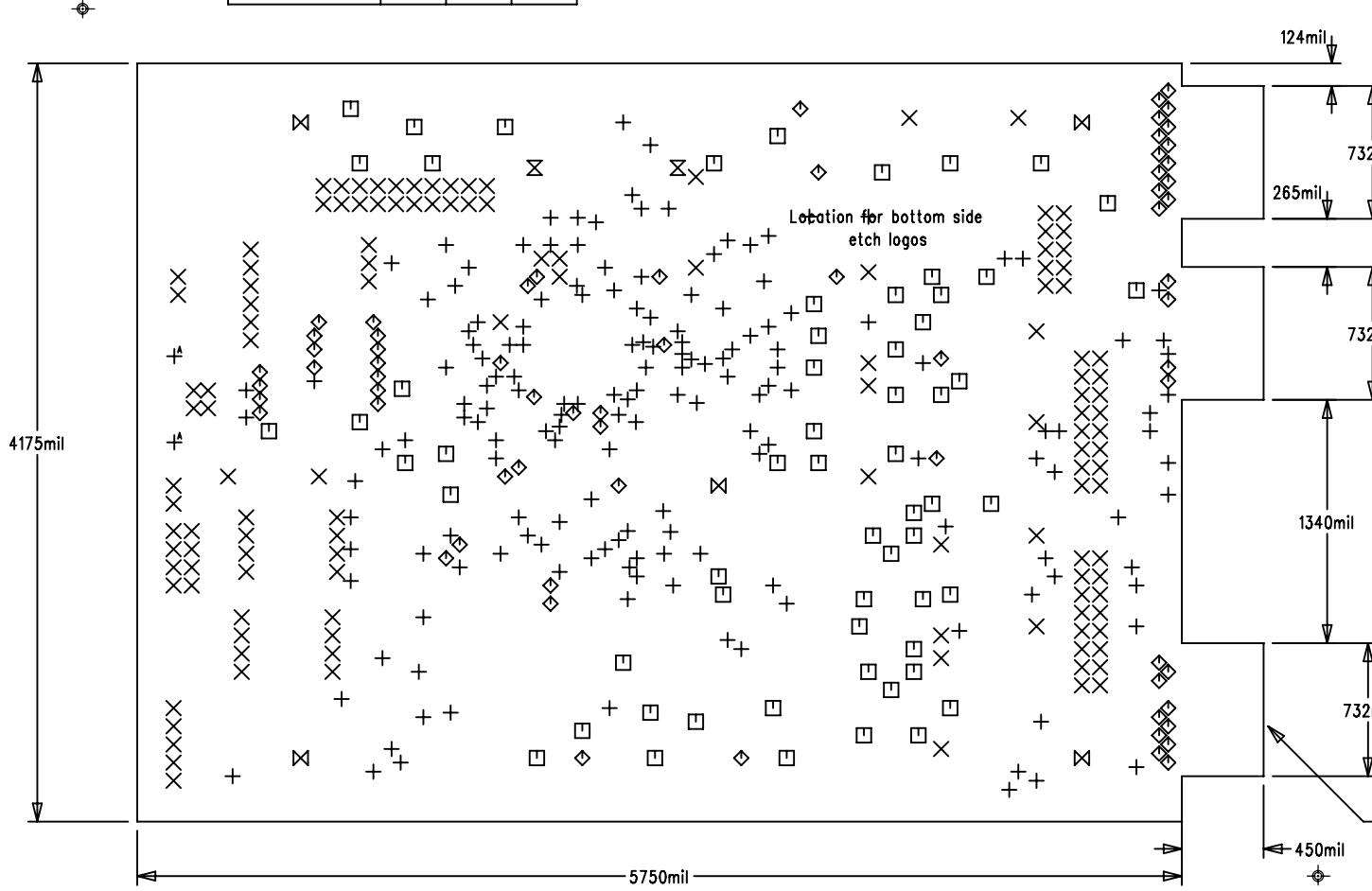
4 LAYER

SILK
SOL

SIZE	QTY	SYM	PLTD
20	168	+	PLTD
37	130	X	PLTD
35	61	□	PLTD
22	66	◊	PLTD
40	2	☒	PLTD
156	5	☒	PLTD
91	2	A	PLTD



SOL



DRILL/FAB

NOTES: Unless otherwise specified

SCREEN (TOP SIDE)
DERMASK (TOP SIDE)

.062 +/- .007
↓
DERMASK (BOTTOM SIDE)

2 mil
1 mil
1 mil

Bevel edge connector (3 pl.)

1. Fabricate PCB in accordance with IPC-6012, Class 2; per IPC-6011.
2. Materials:
 1. Laminate and Prepreg (B-stage) to be in accordance with IPC-4101/21.
 2. Copper foil to be in accordance with IPC-MF-150. Unless otherwise specified copper weight for all layers to be 1 oz. Copper weight is to be considered "finished".
 3. All holes shall be located within 0.008" Diameter of True Position. Layer to layer registration shall be within 0.005".
4. Finish:
 1. All exposed conductive pattern areas not covered with solder mask or other plating shall be Hot Air Solder Leveled using eutectic Tin Lead Solder (Sn63/Pb37) per ANSI/J-STD-006 (HASL).
 2. Apply liquid photo imageable solder mask (color green) per IPC-SM-840, class 2 to both sides of the board over bare copper. Via holes covered with solder mask do not need to be plugged.
 3. Silkscreen shall be white, permanent, organic, non-conductive ink. There shall be no silkscreen on any solderable component pad.
5. Marking:
 1. Board part number and revision is rendered in etch on the bottom side of the board. Revision should be identical to this drawing.
 2. UL logo, manufacturer's identification and date code letter shall be rendered in etch on the bottom side of the board approximately where shown.
6. Plate Edge Connector 0.00003" minimum gold thickness over 0.0001" minimum low stress nickel on tabs

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