MOTOROLA INC.
Communications
Sector

ANALOG INTERFACE BOARD (A07)

MODEL RTL4092A

1. DESCRIPTION

1.1 The analog interface board (AIB) processes analog voltages to obtain an absolute value and sign voltage for the counter board. The AIB is a microprocessor controlled signal buffer, filter, and ranging device. The external vertical input voltages are multiplexed to obtain the absolute value and sign of the voltage that is sent to the counter.

1.2 The AIB consists of the four range attenuator, rms-dc converter, 1 kHz notch filter, ×.1 attenuator, absolute value amplifier, peak detector, and attenuator driver stage. All ac, dc, AGC, and other input and output signal connections are made through the main interconnect board.

2. THEORY OF OPERATION

2.1 RANGE ATTENUATOR

External DVM inputs to the VERT/SINAD/DIST/DVM IN input jack are ranged by the microprocessor over a four-decode range before being routed to the rms-dc converter. A relay ladder driven by inputs from the attenuator driver stage selects the ranging values prior to being sent to the ac/dc coupler. An ac filter consisting of C77, C78, R124, and R125 allows an accurate dc voltage measurement to be taken when an ac voltage is also present at the input by attenuating the ac signal.

2.2 RMS-DC CONVERTER

AC voltages are applied to multiplexer U4 which selects signals either before the notch filter or after the filter for both ac voltage and SINAD measurements. Battery voltage and AGC levels are also applied to U4. When measuring SINAD, the microprocessor switches the notched and unnotched signals input to U4 at 60 millisecond intervals.

2.3 TWO-STATE 1 kHZ NOTCH FILTER

The two-stage notch filter consists of five distinct filters with two of the notch filters cascaded to obtain increased attenuation. The output of amplifier U2 is coupled across a high-pass filter made up of C79 and R80. Two low-pass filters attenuate frequencies above 19 kHz. The notch filter is designed to attenuate a 1 kHz signal by 50 dB.

2.4 ×.1 ATTENUATOR

The composite voltage output from multiplexer U6 is scaled by the ×.1 attenuator prior to being amplified by U7. Transistors Q2 and Q5 are level shifters. The ×.1 attenuator consists of Q1 and the combined impedance of R51, R38, and R36. The attenuated signal is amplified by voltage follower U7.

2.5 ABSOLUTE VALUE AMPLIFIER

The output of amplifier U7 is inverted by amplifier U8 while U9 determines the input polarity. The output of U8 and U7 is gated by U10 to the analog-to-digital converter on the counter board. Transistors Q7 and Q8 are level shifters and Q9 drives the sign polarity output.

2.6 PEAK DETECTOR CIRCUIT

The peak detector circuit provides dc outputs equal to the negative and positive peak values of the input signal relative to the average dc level of the input signal. The positive and negative signals are selected through the 1-of-8 multiplexer U6.

2.7 ATTENUATOR DRIVER STAGE

The attenuator driver stage provides the voltage to the range attenuator relays. Function data from the microprocessor is applied through buffer U15 to latches U16 and U17. The output of U16 controls the multiplexer, while U17 primarily controls the attenuator relays.

technical writing services
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8/12/83- *PHI*
68P81064E57-O

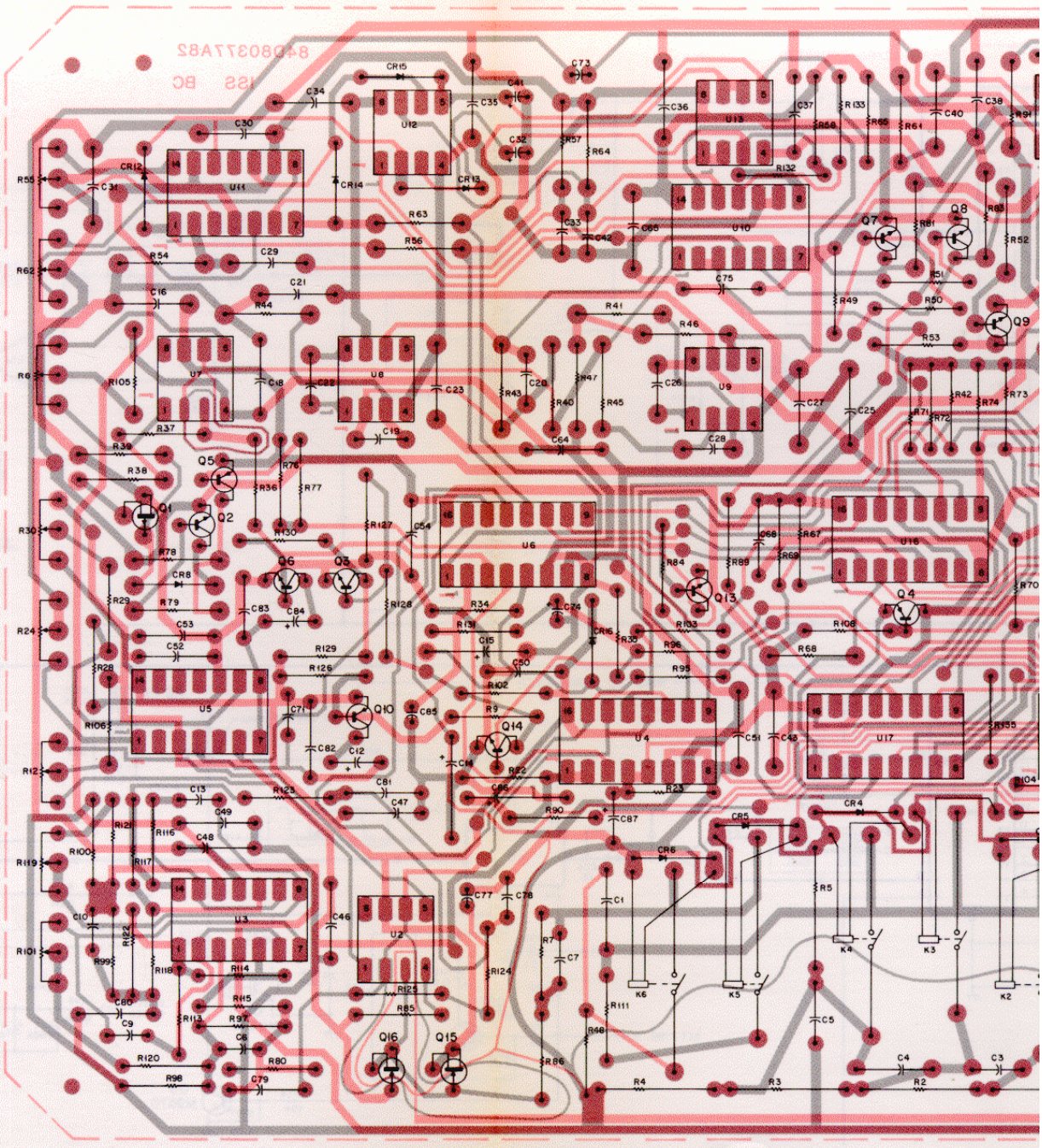
parts list

RTL4092A Analog Interface Board — PL-8499-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed: uF + 80-20%; 25 V: unless otherwise stated
C1	8-84637L06	.0068 ± 5%; 680 V
C2	20-84307A11	var. 5.5-18 pF; NP0; 350 V
C3	21-84494B11	200 pF ± 5%; 500 V
C4	21-863296	2500 pF ± 2%; 500 V
C5	8-84637L47	.022 ± 5%; 250 V
C6	21-80397A11	.022 ± 5%; 50 V; NP0
C7	21-84494B11	200 pF ± 5%; 500 V
C8		NOT USED
C9, 10	21-80397A11	.022 ± 5%; 50 V; NP0
C11		NOT USED
C12	23-84538G24	0.56 ± 10%; 35 V
C13	21-80397A11	.022 ± 5%; 50 V; NP0
C14, 15	23-84762H14	0.47 ± 20%; 50 V
C16	21-82372C03	0.1
C17		NOT USED
C18	21-82372C03	0.1
C19	21-84494B46	180 pF ± 3%; 500 V
C20	21-82428B21	.01 + 10-30%; 100 V
C21	21-82372C03	0.1
C22	21-84494B42	27 pF ± 5%; 500 V
C23	21-82372C03	0.1
C24	23-84908L01	2.2 ± 20%; 50 V non polar
C25	21-82372C03	0.1
C26	21-84494B42	27 pF ± 5%; 500 V
C27	21-82372C03	0.1
C28	21-84494B46	180 pF ± 3%; 500 V
C29, 30	21-82372C03	0.1
C31	21-82372C03	0.1
C32	23-84665F01	10 + 100-10%; 25 V
C33	21-80397A01	0.47 ± 10%; 50 V
C34 thru 40	21-82372C03	0.1
C41	23-84665F01	10 + 100-10%; 25 V
C42	21-80397A10	0.47 ± 10%; 50 V
C43	21-82372C03	0.1
C44, 45		NOT USED
C46 thru 54	21-82372C03	0.1
C55	21-83406D93	16 pF ± 5%; 500 V; NP0
C56 thru 59	21-82372C03	0.1
C60 thru 63	23-84665F01	10 + 100-10%; 25 V
C64, 65	21-82372C03	0.1
C66		NOT USED
C67, 68, 69	21-82372C03	0.1
C70		NOT USED
C71	21-80370A04	.022 ± 10%; 100 V
C72		NOT USED
C73	23-84708L01	2.2 ± 20%; 50 V non polar
C74	21-84665F01	10 + 100-10%; 25 V
C75	21-82372C03	0.1
C76	21-84494B33	30 pF ± 5%; 500 V
C77	23-84908L01	2.2 ± 20%; 50 V non polar
C78	21-84008H23	0.22 ± 10%; 100 V
C79, 80, 81	21-82372C03	0.1
C82	21-82428B15	.005 ± 10%; 100 V
C83	8-84637L24	.068 ± 10%; 100 V
C84	23-84538G02	4.7 ± 20%; 50 V
C85	23-84908L01	2.2 ± 20%; 50 V non polar
C86	23-84762H14	0.47 ± 20%; 50 V
C87	23-84535G28	0.33 ± 10%; 35 V
		diode: (see note)
CR1 thru 6	48-83654H01	silicon
CR8	48-83654H01	silicon
CR12 thru 15	48-83654H01	silicon
CR16	48-84616A09	hot carrier
		relay, reed:
K1 thru 6	80-80346A01	12 V
		transistor: (see note)
Q1	48-84308A43	FET, N-channel; type M0843
Q2, 3	48-869570	NPN; type M9570
Q4, 5	48-869571	PNP; type M9571
Q6 thru 9	48-869570	PNP; type M9570
Q10, 11	48-869571	PNP; type M9571
Q12, 13, 14	48-869570	NPN; type M9570
Q15, 16	48-869831	FET, N-channel; type M9831
Q17	48-869571	PNP; type M9571
		resistor, fixed: ± 5%; 1/4 W: unless otherwise stated
R1	6-80390A85	1.82 meg ± 0.25%
R2	6-80390A86	182k ± 0.25%
R3	6-80390A87	18.2k ± 0.25%
R4	6-80390A88	2.1k ± 0.25%
R5	6-80390A89	54.9k ± 0.25%
R6		NOT USED
R7	6-10621E85	1.0 meg ± 1%; 1/8 W
R8	18-83452F11	var. 5k
R9	6-124A73	10k
R10, 11		NOT USED
R12	18-83452F11	var. 5k
R22, 23	6-10621C60	4.75k ± 1%; 1/8 W
R24	18-83452F09	var. 1k
R25, 26, 27		NOT USED
R28	6-10621B98	1.1k ± 1%; 1/8 W
R29	6-10621E85	1.0 meg ± 1%; 1/8 W
R30	18-83452F23	var.; 500k
R31, 32, 33		NOT USED
R34	6-84640C97	6.98k ± 0.5%; 1/8 W
R35	6-84640C27	2.87k ± 0.5%; 1/8 W
R36	6-84640C61	499k ± 0.5%; 1/8 W
R37	6-80390A84	54.9 ± 0.5%
R38	6-84640C20	511 ± 0.5%; 1/8 W
R39	6-124A97	100k
R40	6-84640C70	73.2k ± 0.5%; 1/8 W
R41	6-124A94	75k
R42	6-124A61	3.3k
R43	6-84640C70	73.2 ± 0.5%; 1/8 W
R44	6-84640C67	35.7k ± 0.5%; 1/8 W
R45	6-83175C72	75k ± 1%; 1/8 W
R46	6-10621E85	1.0 meg ± 1%; 1/8 W
R47	6-124A10	24
R48	6-124B50	15 meg
R49	6-124A53	1.5k
R50	6-124A72	9.1k
R51, 52	6-124A97	100k
R53	6-124A73	10k
R54	6-124B22	1.0 meg
R55	18-83452F13	var. 10k
R56	6-124A80	20k
R57	6-124B22	1.0 meg
R58	6-124B40	5.6 meg
R59, 60	6-84640C70	73.2k ± 0.5%; 1/8 W
R61	6-124B22	1.0 meg
R62	18-83452F13	var. 10k
R63	6-124A80	20k
R64	6-124B22	1.0 meg
R65	6-124B40	5.6 meg
R66	6-124A49	1k
R67	6-124A73	10k
R68 thru 74	6-124A61	3.3k
R75		NOT USED
R76 thru 79	6-124A73	10k
R80	6-124A67	5.6k
R81	6-124A73	10k
R82		NOT USED
R83	6-124A73	10k
R84	6-124A61	3.3k
R85	6-124A01	10
R86	6-124A66	5.1k
R87	6-124A58	2.4k
R88	6-124A97	100k
R89	6-124A61	3.3k
R90	6-10621D42	33.3k ± 1%; 1/8 W
R91	6-83175C72	75k ± 1%; 1/8 W
R92, 93		NOT USED
R94	6-10621D07	14.3k ± 1%; 1/8 W
R95	6-84640C97	6.98k ± 0.5; 1/8 W
R96	6-84640C27	2.87k ± 0.5%; 1/8 W
R97 thru 100	6-80390A91	158k ± 0.25%; 1/8 W
R101	18-83452F09	var. 1k
R102	6-124A76	13k
R103	6-124A61	3.3k
R104	6-124A49	1k
R105, 106	6-10621C63	5.11k ± 1%; 1/8 W
R107	6-124A61	3.3k
R108	6-124A94	75k
R109		NOT USED
R110	6-10621D88	100k ± 1%; 1/8 W
R111	6-124C25	100 ± 10%
R112		NOT USED
R113	6-84640C97	6.98k ± 0.5%; 1/8 W
R114, 115	6-80390A90	6.98k ± 0.25%; 1/8 W
R116	6-84640C97	6.98k ± 0.5%; 1/8 W
R117, 118	6-80390A90	6.98k ± 0.25%; 1/8 W
R119	18-83452F09	var. 1k
R120, 121	6-84640C97	6.98k ± 0.5%; 1/8 W
R122, 123	6-124A20	62
R124	6-124A91	56k
R125	6-124A67	5.6k
R126	6-124A61	3.3k
R127	6-124A64	4.3k
R128 thru 130	6-124A73	10k
R131	6-124A72	9.1k
R132, 133	6-124A39	390
R134, 135	6-124A97	100k
		integrated circuit: (see note)
U2	51-80365A09	operational amplifier
U3	51-84561L75	quad operational amplifier
U4	51-82884L54	4-channel analog multiplexer
U5	51-80365A13	rms ac/dc converter
U6	51-82884L46	8-channel analog multiplexer
U7	51-80365A09	operational amplifier
U8, 9	51-80365A27	operational amplifier
U10	51-82884L48	quad analog switch
U11	51-80365A12	dual operational amplifier

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
U12	51-80365A26	dual comparator
U13, 14	51-80365A07	dual op amp
U15	51-84561L03	hex inverter
U16, 17	51-82884L70	hex 'D' type flip-flop
U18	51-84561L42	dual 1-4 decoder/demultiplexer
U19		NOT USED
U20	51-83629M08	quad op amp
	mechanical part	
M1, 2	45-80395A38	EJECTOR

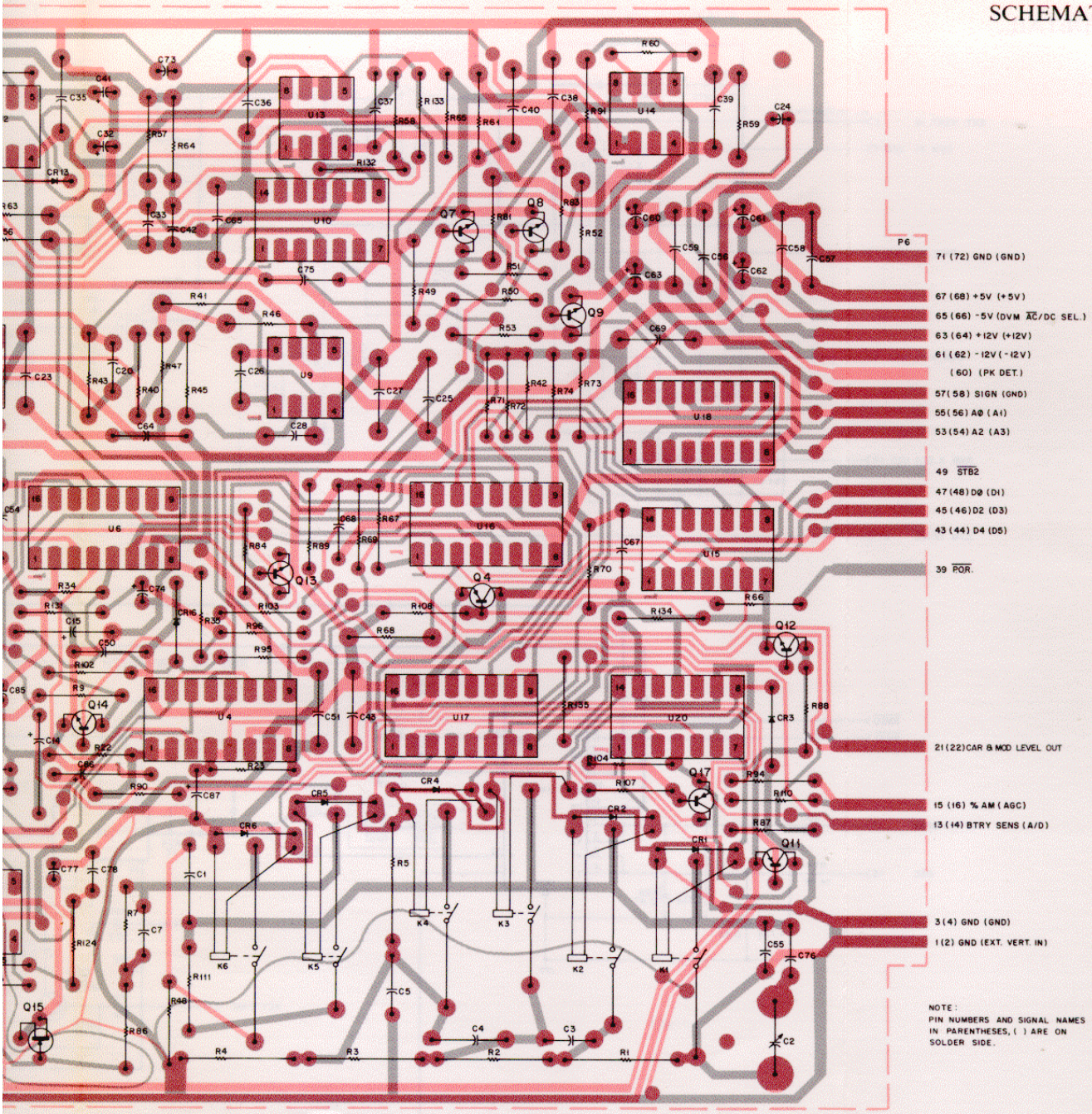
note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.



SHOWN FROM COMPONENT SIDE

ANALOG

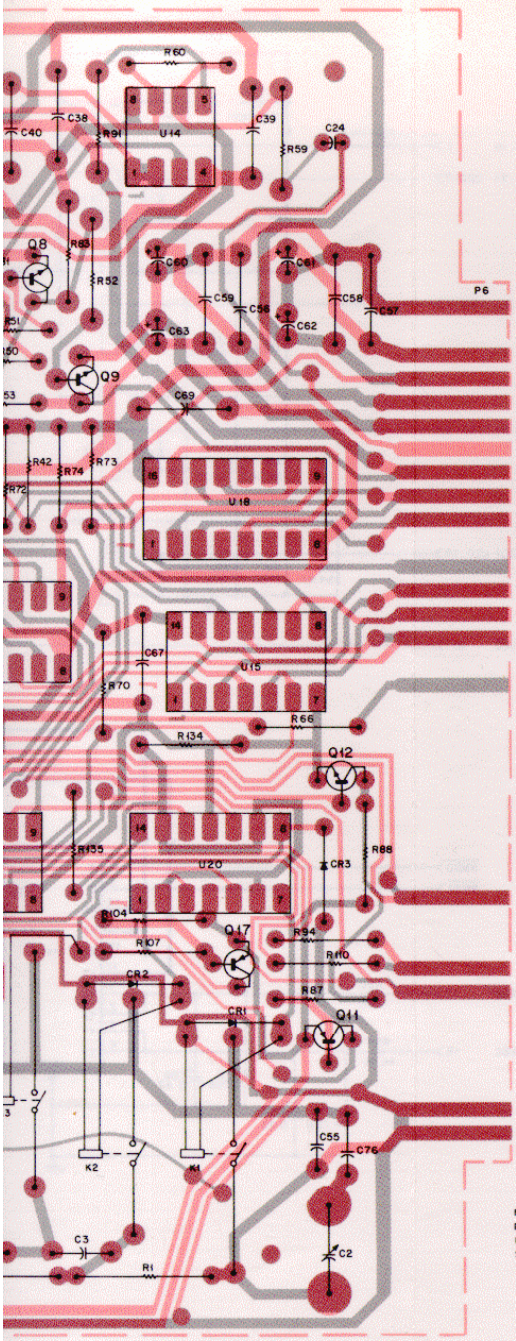
SCHEMATIC



SHOWN FROM COMPONENT SIDE

ANALOG INTERFACE BOARD (A07)

MODEL RTL4092A
SCHEMATIC DIAGRAM, CIRCUIT BOARD DETAIL,
AND PARTS LIST



P6

71 (72) GND (GND)

67 (68) +5V (+5V)

65 (66) -5V (DVM AC/DC SEL.)

63 (64) +12V (+12V)

61 (62) -12V (-12V)

(60) (PK DET.)

57 (58) SIGN (GND)

55 (56) A0 (A1)

53 (54) A2 (A3)

49 $\overline{STB2}$

47 (48) D0 (D1)

45 (46) D2 (D3)

43 (44) D4 (D5)

39 $\overline{POR}$.

21 (22) CAR & MOD LEVEL OUT

15 (16) % AM (AGC)

13 (14) BTRY SENS (A/D)

3 (4) GND (GND)

1 (2) GND (EXT. VERT. IN)

NOTE:
PIN NUMBERS AND SIGNAL NAMES IN PARENTHESES, ( ) ARE ON SOLDER SIDE.

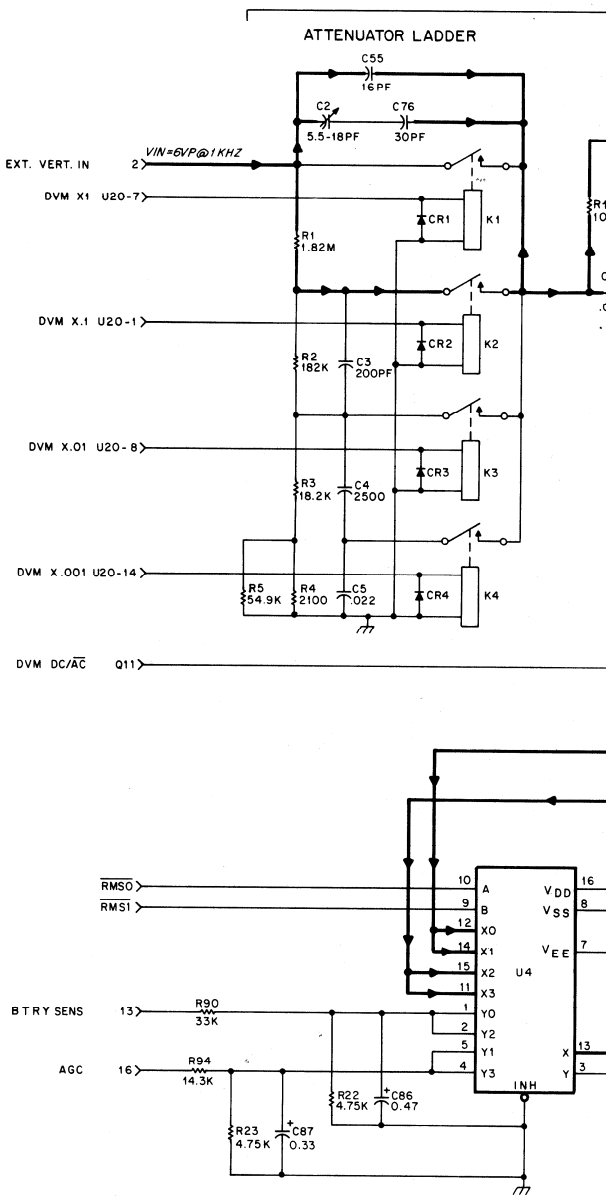
SOLDER SIDE ● BD-EEPS-36197-O
COMPONENT SIDE ● BD-EEPS-36198-O
OL-EEPS-36190-B

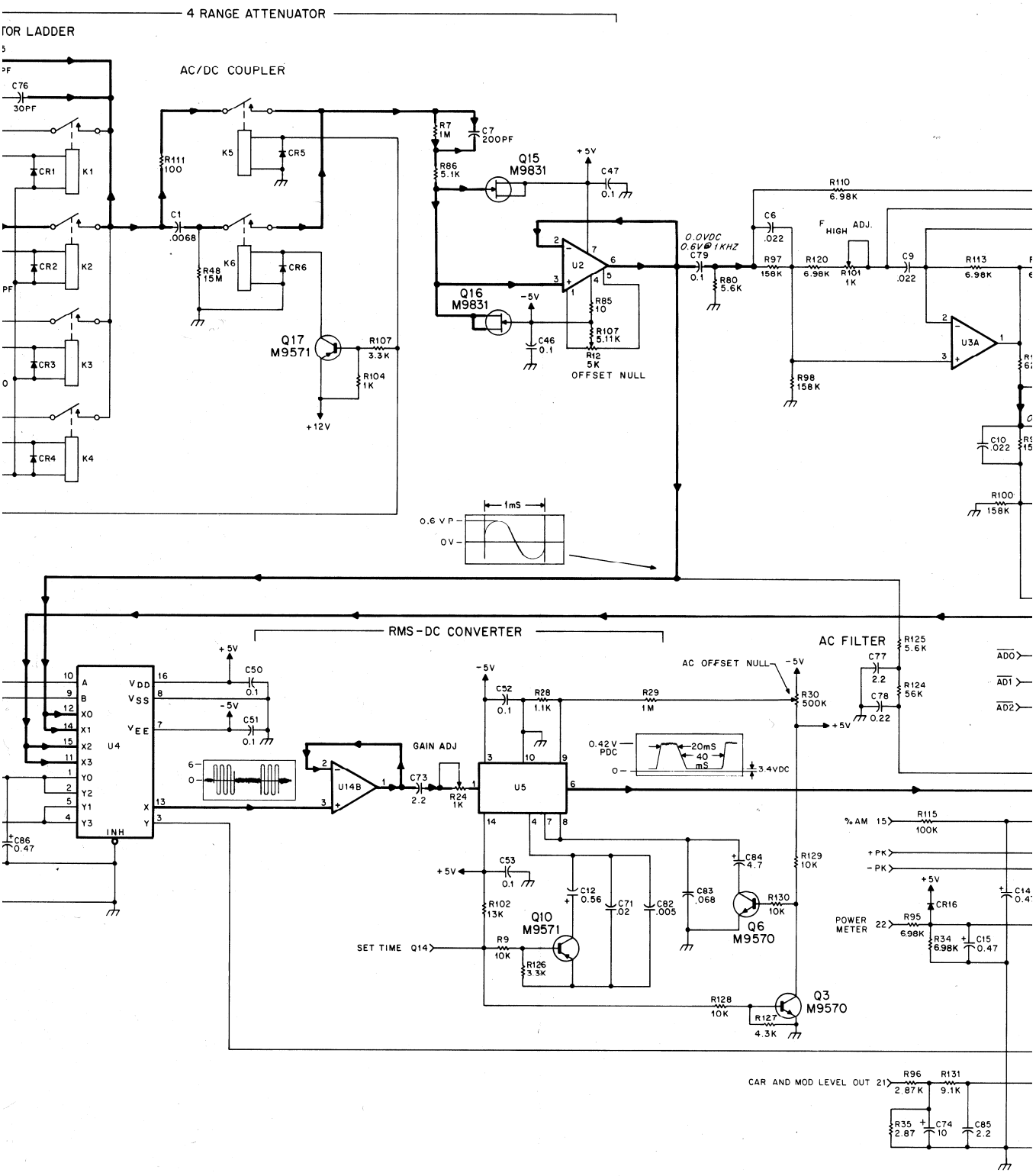
ANALOG INTERFACE BOARD

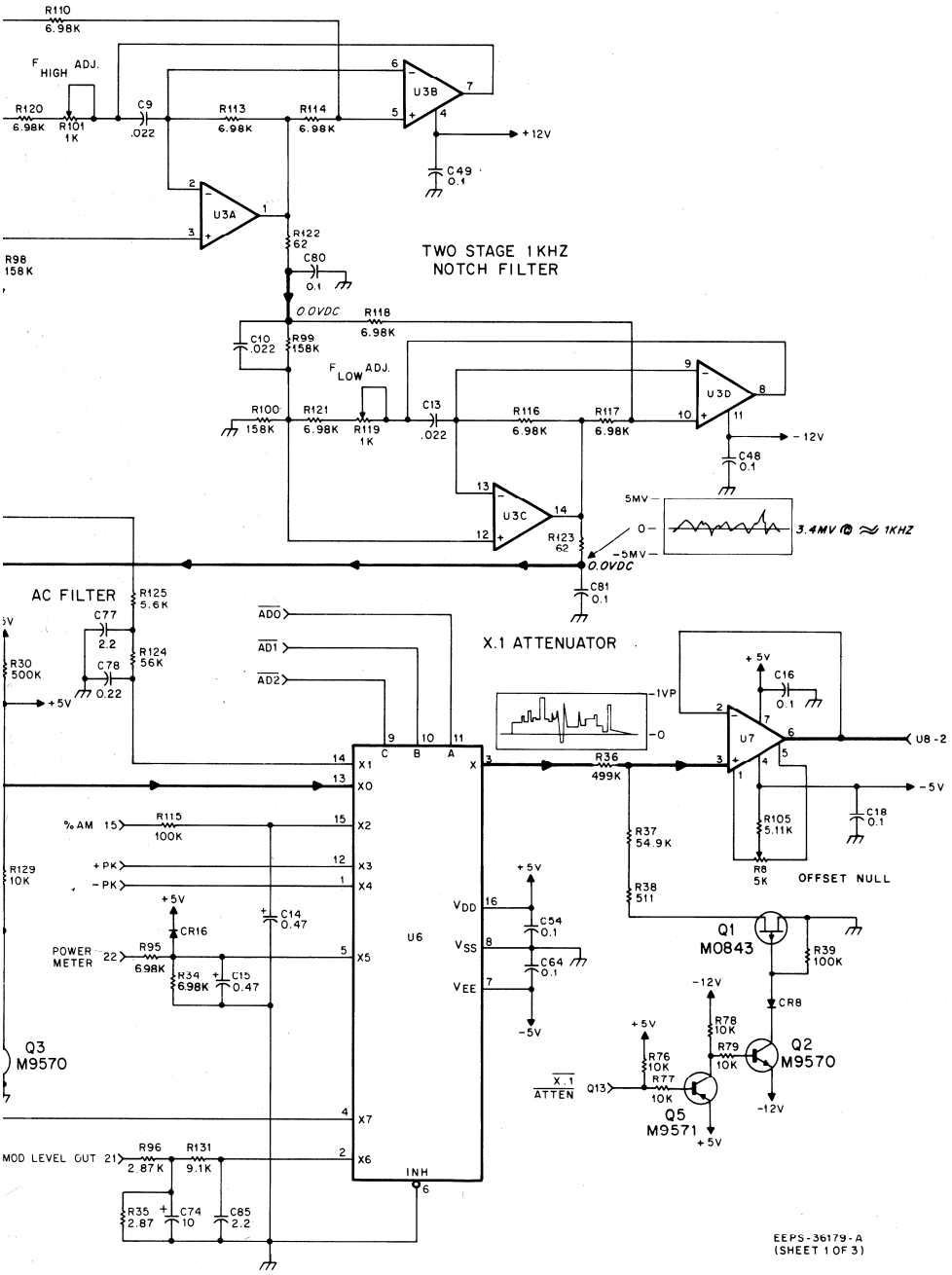
Motorola No. PEPS-36849-O
(Sheet 1 of 4)
8/12/83-PHI

ANALOG INTERFACE BOARD (A07)

MODEL RTL4092A
SCHEMATIC DIAGRAM, CIRCUIT BOARD DETAIL,
AND PARTS LIST




4 RANGE ATTENUATOR
TOR LADDER
AC/DC COUPLER
C76
30PF
CR1
K1
CR2
K2
CR3
K3
CR4
K4
R111
100
K5
CR5
C1
.0068
K6
CR6
R48
15M
Q17
M9571
R107
3.3K
R104
1K
+12V
R7
1M
C7
200PF
R86
5.1K
Q15
M9831
+5V
C47
0.1
Q16
M9831
-5V
C46
0.1
U2
R85
10
R107
5.11K
R12
5K
OFFSET NULL
0.0VDC
0.6V@1KHZ
C79
0.1
R80
5.6K
R110
6.98K
C6
.022
R97
158K
R120
6.98K
F HIGH ADJ.
R101
1K
C9
.022
R113
6.98K
U3A
R98
158K
C10
.022
R100
158K
1mS
0.6 V P-P
0V
RMS-DC CONVERTER
U4
VDD
VSS
VEE
INH
C86
0.47
C50
0.1
C51
0.1
GAIN ADJ
U14B
C73
2.2
R24
1K
U5
C52
0.1
R28
1.1K
R29
1M
AC OFFSET NULL
R30
500K
AC FILTER
C77
2.2
C78
0.22
R125
5.6K
R124
56K
ADO
AD1
AD2
0.42V PDC
20mS
40 mS
3.4VDC
C53
0.1
R102
13K
C12
0.56
C71
.02
C82
.005
C83
.068
C84
4.7
R129
10K
R130
10K
Q10
M9571
Q6
M9570
SET TIME Q14
R9
10K
R126
3.3K
R128
10K
R127
4.3K
Q3
M9570
% AM
R115
100K
+PK
-PK
CR16
POWER METER
R95
6.98K
R34
6.98K
C15
0.47
C14
0.47
CAR AND MOD LEVEL OUT
R96
2.87K
R131
9.1K
R35
2.87
C74
10
C85
2.2



Notes:

1. Unless otherwise indicated: resistor microfarads; and inductor values ar
2. Integrated circuits on this board are
3. IC types and connections for this bo

Reference Designation	Mfgr's Description
U2, 7	Op Amp
U3	Quad Diff. Op Amp
U4	4-Channel Analog M
U5	AC/DC Converter
U6	8 CH Analog Mux
U8	Op Amp
U9	Op Amp
U10	Quad Analog Switc
U11	Dual Op Amp
U12	Comparator
U13, 14	Dual Op Amp
U15	Hex Inverter
U16, 17	Hex D Flip/Flp
U18	Dual 1-4 Decoder/D
U20	Quad Op Amp

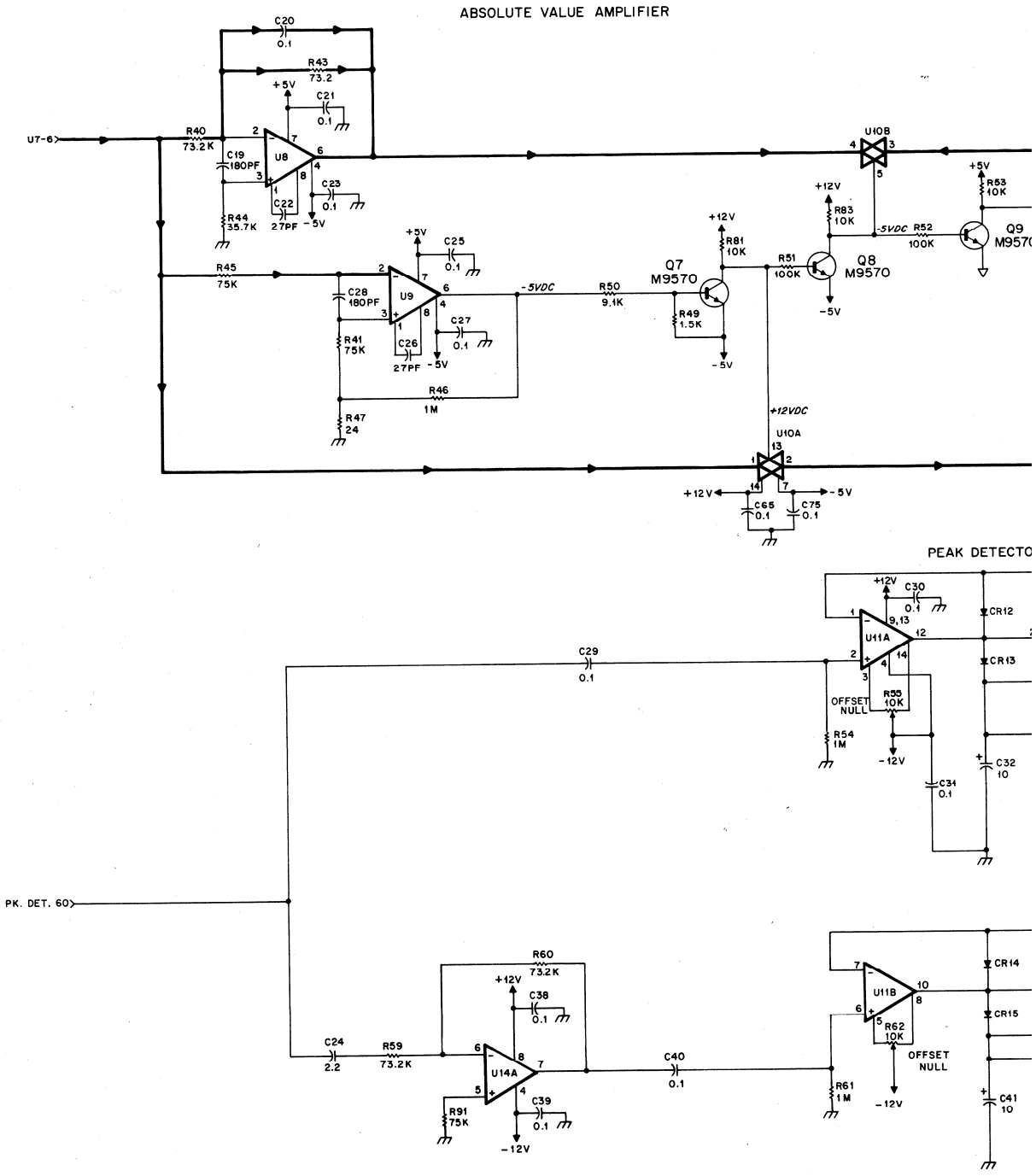
Notes:

1. Unless otherwise indicated: resistor values are in ohms; capacitor values are in microfarads; and inductor values are in millihenries.

2. Integrated circuits on this board are TTL and CMOS devices.

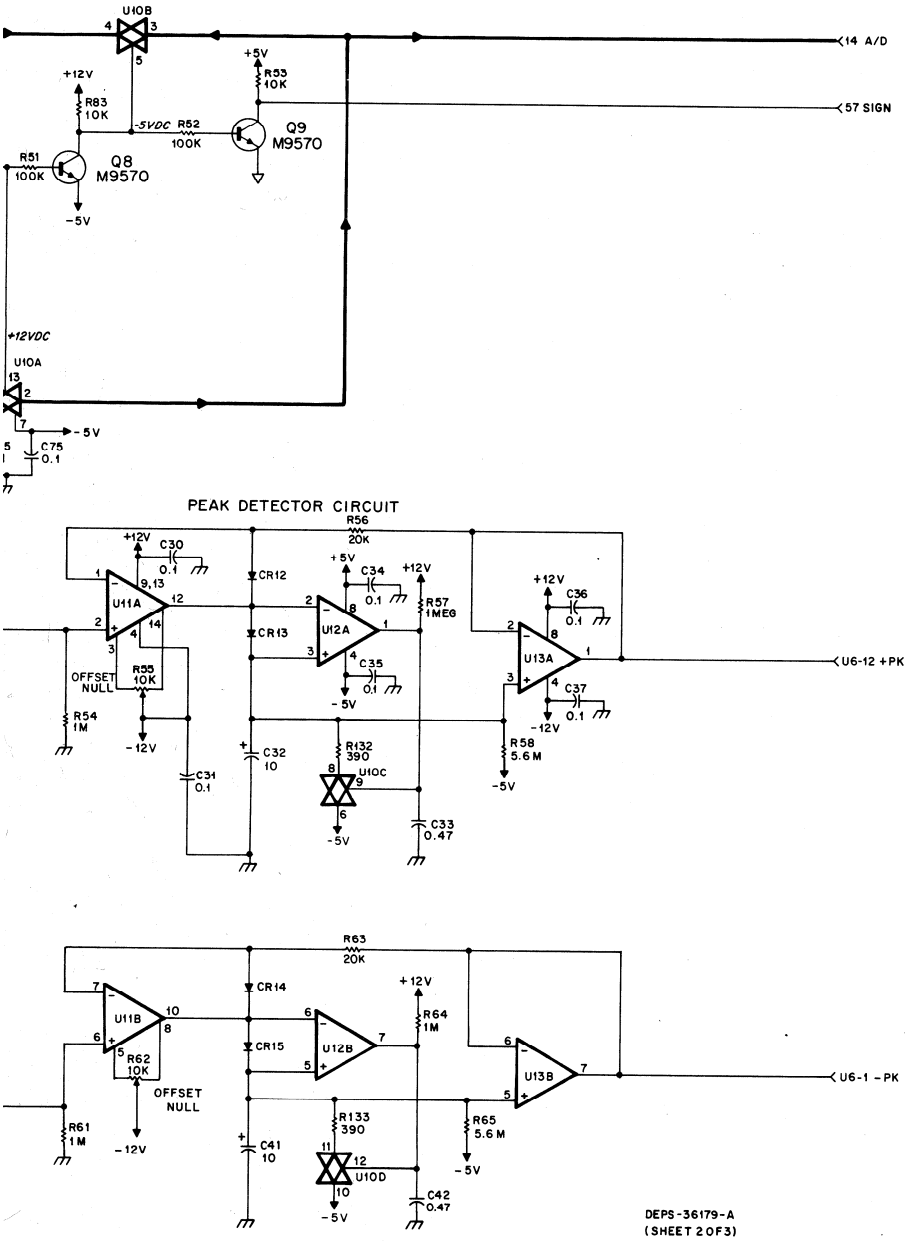
3. IC types and connections for this board are as follows:

Reference Designation	Mfgr's Description	+5 V	−5 V	+12 V	−12 V	GND
U2, 7	Op Amp	7	4	—	—	
U3	Quad Diff. Op Amp	—	—	4	11	
U4	4-Channel Analog Mux	16	7	—	—	8, 6
U5	AC/DC Converter	14	3	—	—	10
U6	8 CH Analog Mux	16	7	—	—	8, 6
U8	Op Amp	7	4	—	—	
U9	Op Amp	7	4	—	—	
U10	Quad Analog Switch	—	7, 9, 10	14	—	—
U11	Dual Op Amp	—	—	9, 13	4	
U12	Comparator	8	4	—	—	
U13, 14	Dual Op Amp	—	—	8	4	
U15	Hex Inverter	14	—	—	—	7
U16, 17	Hex D Flip/Flp	16	—	—	—	8
U18	Dual 1-4 Decoder/Demux	16	—	—	—	8
U20	Quad Op Amp	—	—	4	—	11


ABSOLUTE VALUE AMPLIFIER
PEAK DETECTO
U7-6
PK. DET. 60
C20
0.1
R43
73.2
+5V
C21
0.1
R40
73.2K
C19
180PF
U8
C22
27PF
C23
0.1
-5V
R44
35.7K
R45
75K
C28
180PF
U9
C25
0.1
C26
27PF
C27
0.1
R41
75K
R46
1M
R47
24
-5VDC
R50
9.1K
Q7
M9570
+12V
R81
10K
R49
1.5K
R51
100K
Q8
M9570
R83
10K
R52
100K
Q9
M957(
R53
10K
U10B
U10A
+12VDC
C65
0.1
C75
0.1
C29
0.1
U11A
C30
0.1
OFFSET
NULL
R55
10K
R54
1M
-12V
C31
0.1
C32
10
CR12
CR13
R60
73.2K
C38
0.1
C24
2.2
R59
73.2K
U14A
R91
75K
C39
0.1
C40
0.1
U11B
R62
10K
R61
1M
CR14
CR15
C41
10

ANALOG INTERFACE BOARD (A07)

MODEL RTL4092A
SCHEMATIC DIAGRAM, CIRCUIT BOARD DETAIL,
AND PARTS LIST



ANALOG INTERFACE BOARD

*Motorola No. **PEPS-36849-O***
(Sheet 3 of 4)
8/12/83-PHI

ANALOG INTERFACE BOARD (A07)

MODEL RTL4092A
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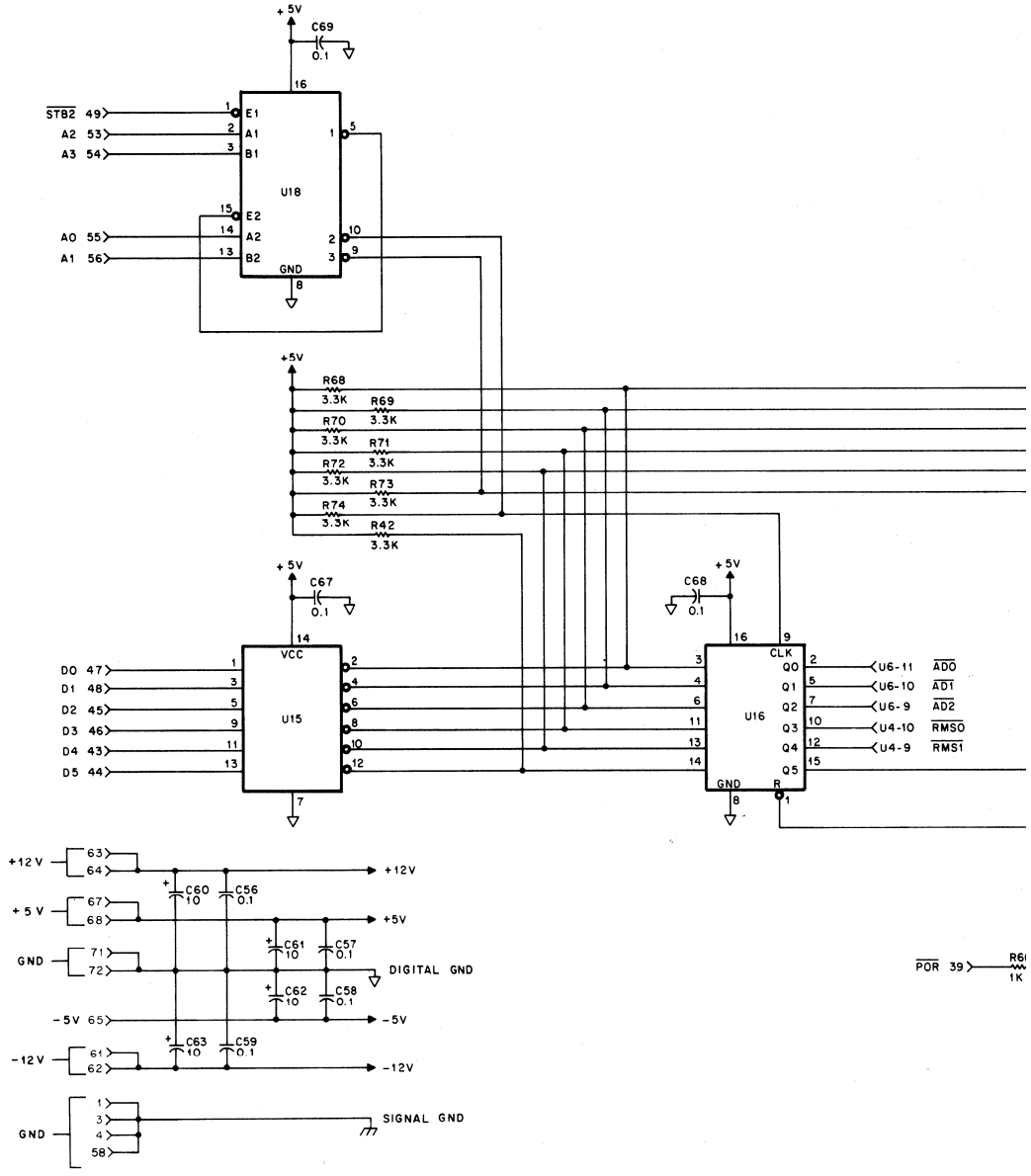
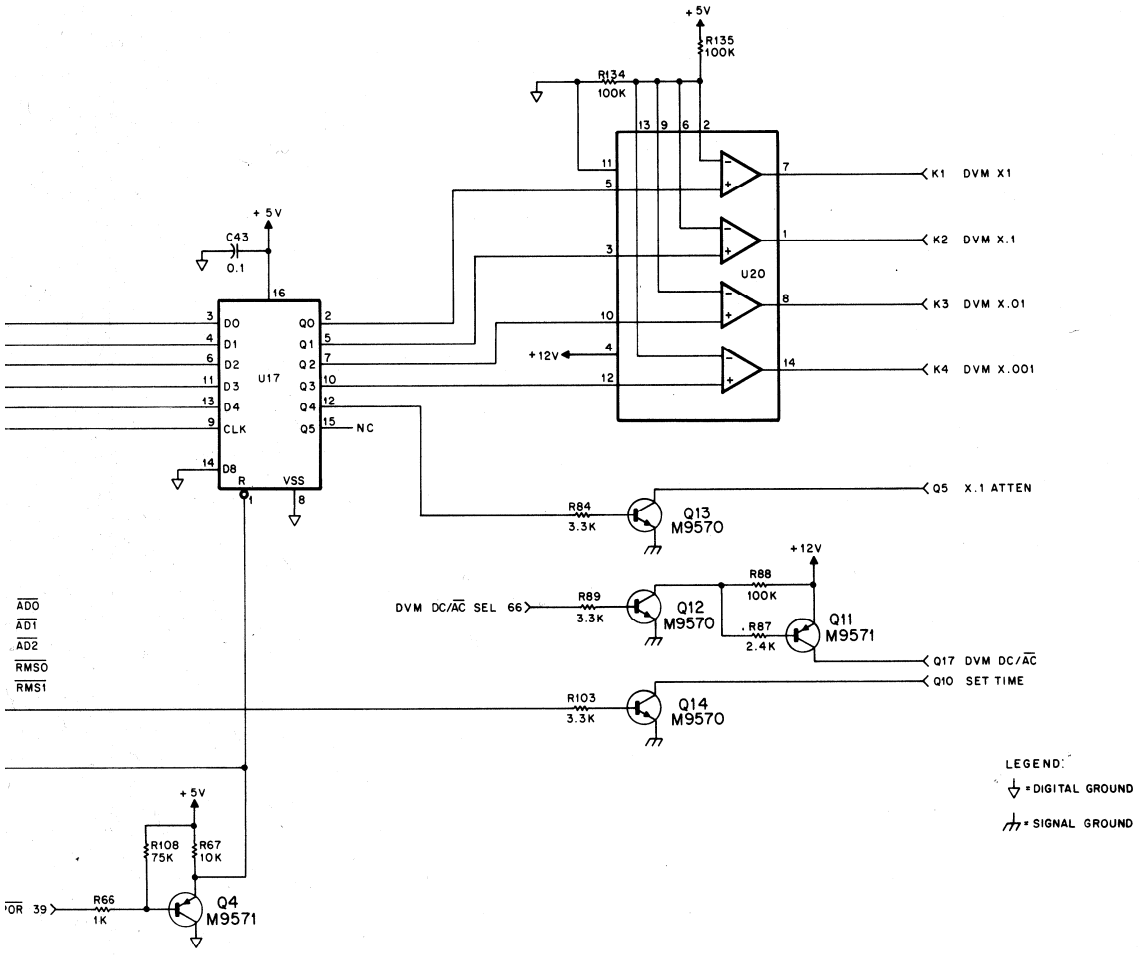


Motorola No. ***PEPS-36849-O***
(Sheet 4 of 4)
8/12/83- PHI

ATTENUATOR DRIVER STAGE



DEPS - 36179 - A
(SHEET 3 OF 3)

CENTRAL PROCESSING UNIT (CPU) BOARD (A08)

MODEL RTC4023A

1. DESCRIPTION

The central processing unit (CPU) board contains the microprocessor, program memory, read/write memory, and input/output buffers. The card uses a Motorola M6800 series microprocessor, a 16k × 8 ROM, and a 384 × 8 RAM.

2. THEORY OF OPERATION

2.1 INPUT/OUTPUT BUS

The CPU communicates with all the modules in the service monitor through the I/O bus. The bus consists of eight bidirectional data lines, four address lines, and four strobe lines. A second bus consisting of eight bidirectional data lines, two handshake lines, and two status lines is available for the optional tone signaling card. In addition to the two buses, there are six dedicated I/O lines: DPL, LC. BUSY, AD. INT., COUNT INT., $\overline{SQ\ OPN}$, and $\overline{IRQ}$.

2.2 MICROPROCESSOR

2.2.1 An M6805 microprocessor is used to control the service monitor operating modes. The device contains 16 I/O lines in two ports, 112 bytes of internal RAM, and a total addressable complement of 8192 bytes. An external RAM of 384 bytes is provided, along with two 8k × 8 programmed memories. The low order lines are BØ-B7 and the high order address and data lines are A8-A12. The low order lines are multiplexed whereas the high order lines are not. The AS and DS signals are derived from the 3.40 MHz crystal oscillator. The 680 kHz DS signal is further divided to obtain a 340 kHz signal used by the front panel interface module.

2.2.2 Memory Access

The lower address bits are latched by U5 during the high-to-low transition of AS. The selected address is routed to ROM, RAM, and the I/O decoding logic. High order address bits are routed directly to ROM and the chip select decoding logic. Addresses below $0200 are selected by PB7 (MEM SEL); and PB5 (ROM SEL) is used to select the main ROM (U4), or the auxiliary ROM (U22). Shift register U21 delays ROM SEL for four address strobe cycles to simplify ROM paging for the operating program. Data selector U9 is used to divide locations before $0200 into four 128-byte segments. U9 applies ROM, RAM, and I/O select signals. Chip selects for U4 and U22 are decoded by U7 and U8.

2.2.3 Input/Output

2.2.3.1 The two communication buses are interfaced to the CPU through several input and output ports. All input devices drive the address/data lines directly. Output ports receive data from the microprocessor PAØ-PA7 lines. Lines PBØ-PB4 and PB6 are buffered directly from the microprocessor. When PB7 is high and the selected address is between $0080 and $00FF, U9 generates an I/O select ($\overline{IOSEL}$). An $\overline{IOSEL}$ and $\overline{A3}$ enables U12 to select one of seven ports.

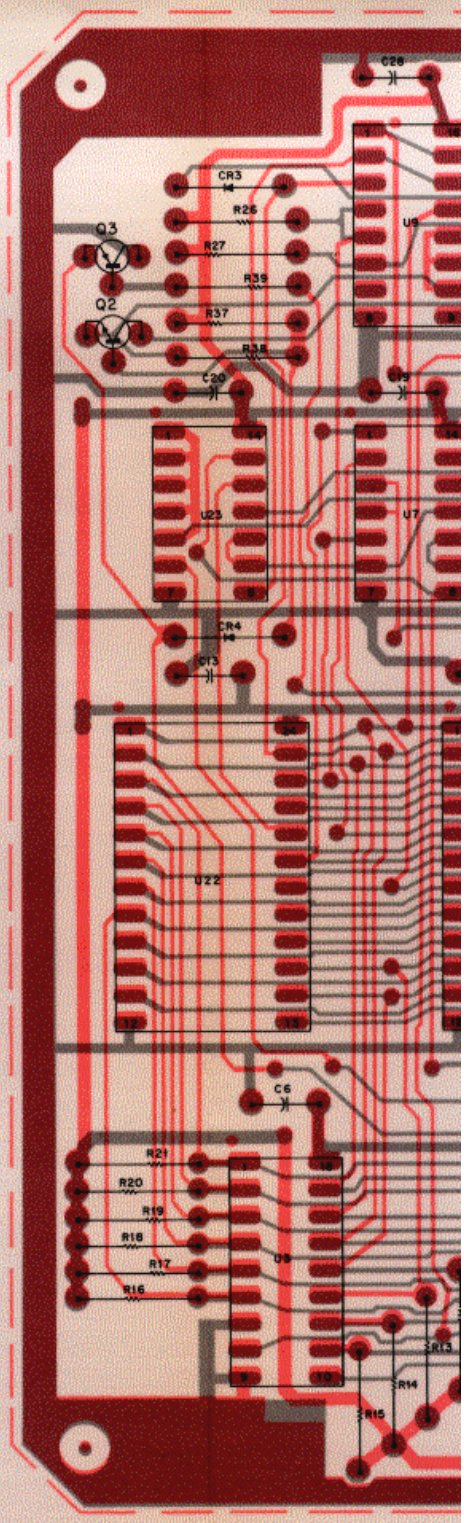
2.2.3.2 The selects enable U13, U15, and U17 to drive the multiplexed bus. The ports are read by the microprocessor with normal memory access. To alter the contents of an output latch, the microprocessor first places new data on the PA lines, and then, by referencing the memory address of the latch, clocks the information into the latch. PB4 and I/O bus drive disable signals for U16 to a high impedance during I/O bus read. U18 is in the high impedance state when the microprocessor reads the option bus.

2.2.4 CMOS RAM

Data held in RAM's U2 and U3 is preserved by voltage from the lithium battery on the front panel interface board. Diodes CR1 and CR2 switch RAM power between the +5 V supply and the battery. The $\overline{P.O.R.}$ (power-on-reset) generated by the front panel interface senses the loss of power and resets the microprocessor and U5. Line A8 is held low through U11 and CR3. Q1 and Q2 disconnect R/$\overline{W}$ and chip select from the RAM's to inhibit access during power transitions.

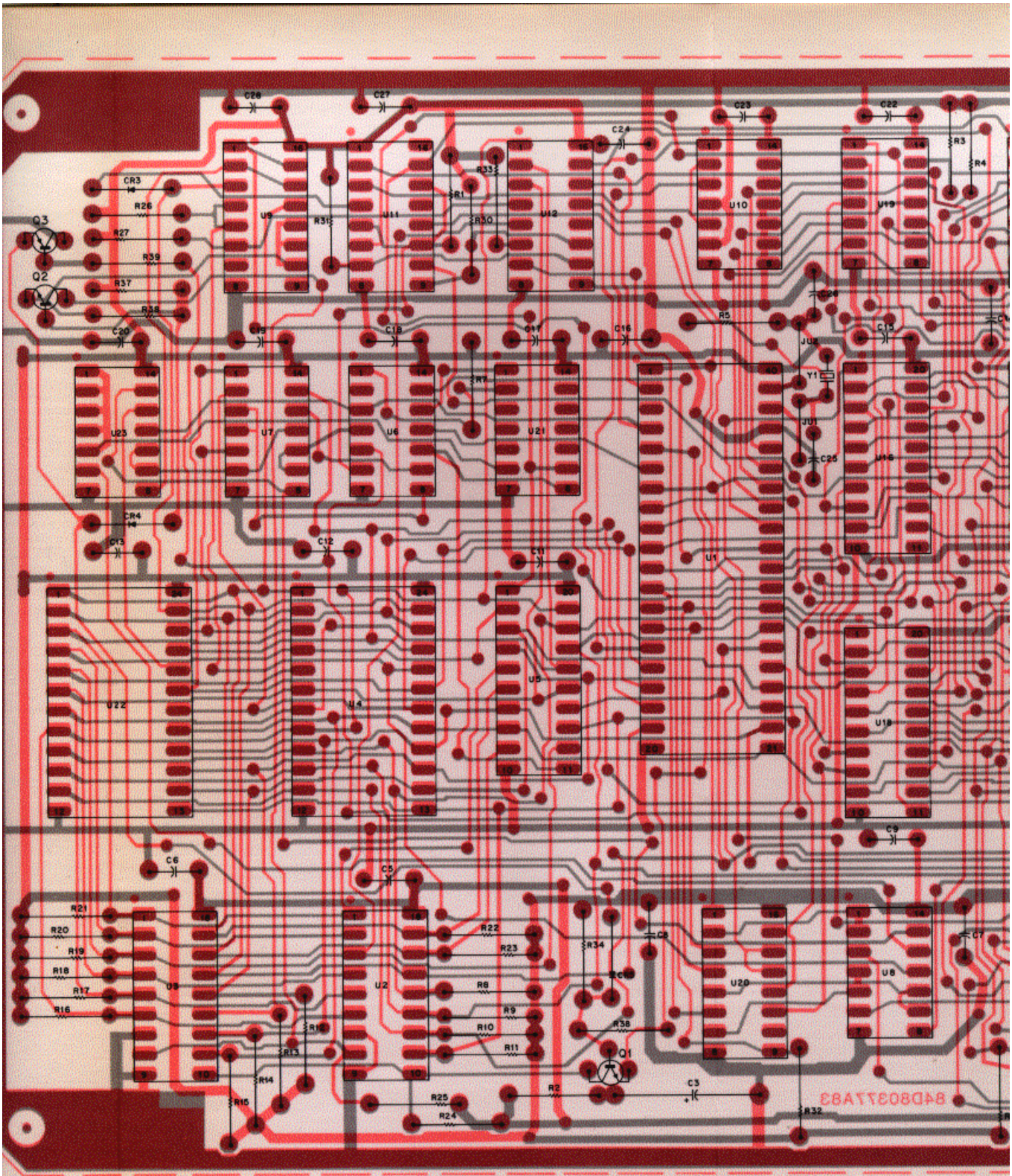
CPU BOARD (A08)

MODEL RTC4023A
SCHEMATIC DIAGRAM, CIRCUIT BOARD DETAIL,
AND PARTS LIST

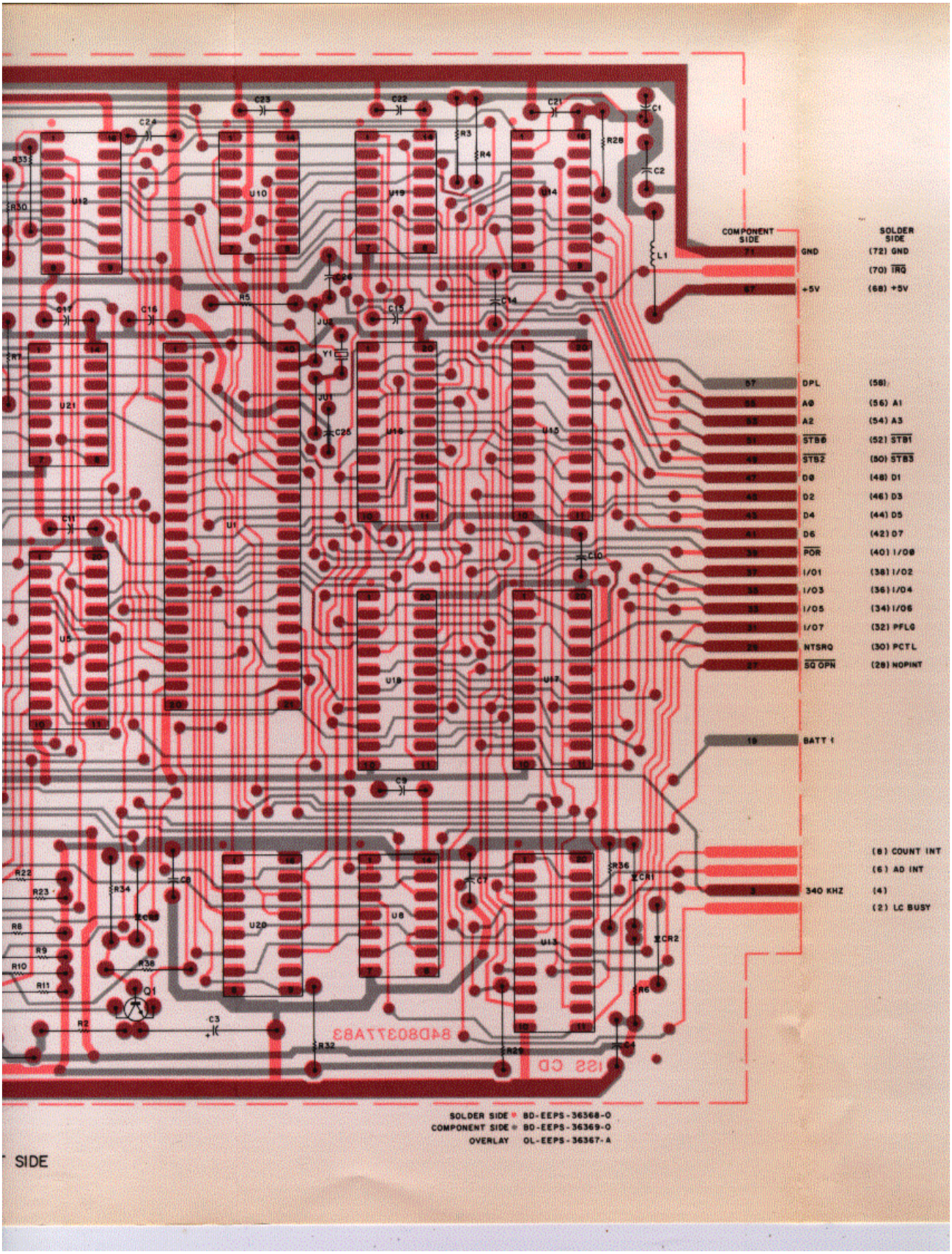


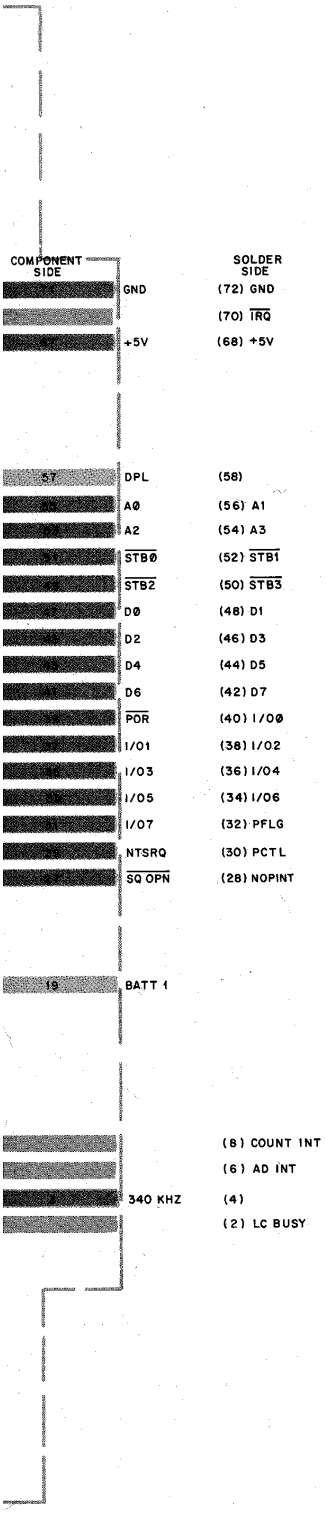
Motorola No. PEPS-36850-O
(Sheet 1 of 2)
8/12/83- PHI

SHOWI



SHOWN FROM COMPONENT SIDE


COMPONENT SIDE
SOLDER SIDE
71 GND (72) GND
(70) IRQ
67 +5V (68) +5V
57 DPL (58)
56 A0 (56) A1
55 A2 (54) A3
51 STB0 (52) STB1
49 STB2 (50) STB3
47 D0 (48) D1
45 D2 (46) D3
43 D4 (44) D5
41 D6 (42) D7
39 POR (40) I/O0
37 I/O1 (38) I/O2
35 I/O3 (36) I/O4
33 I/O5 (34) I/O6
31 I/O7 (32) PFLG
29 NTSRQ (30) PCTL
27 SQ OPN (28) NOPINT
19 BATT +
(8) COUNT INT
(6) AD INT
3 340 KHZ (4)
(2) LC BUSY
SOLDER SIDE = BD-EEPS-36368-0
COMPONENT SIDE = BD-EEPS-36369-0
OVERLAY OL-EEPS-36367-A
SIDE

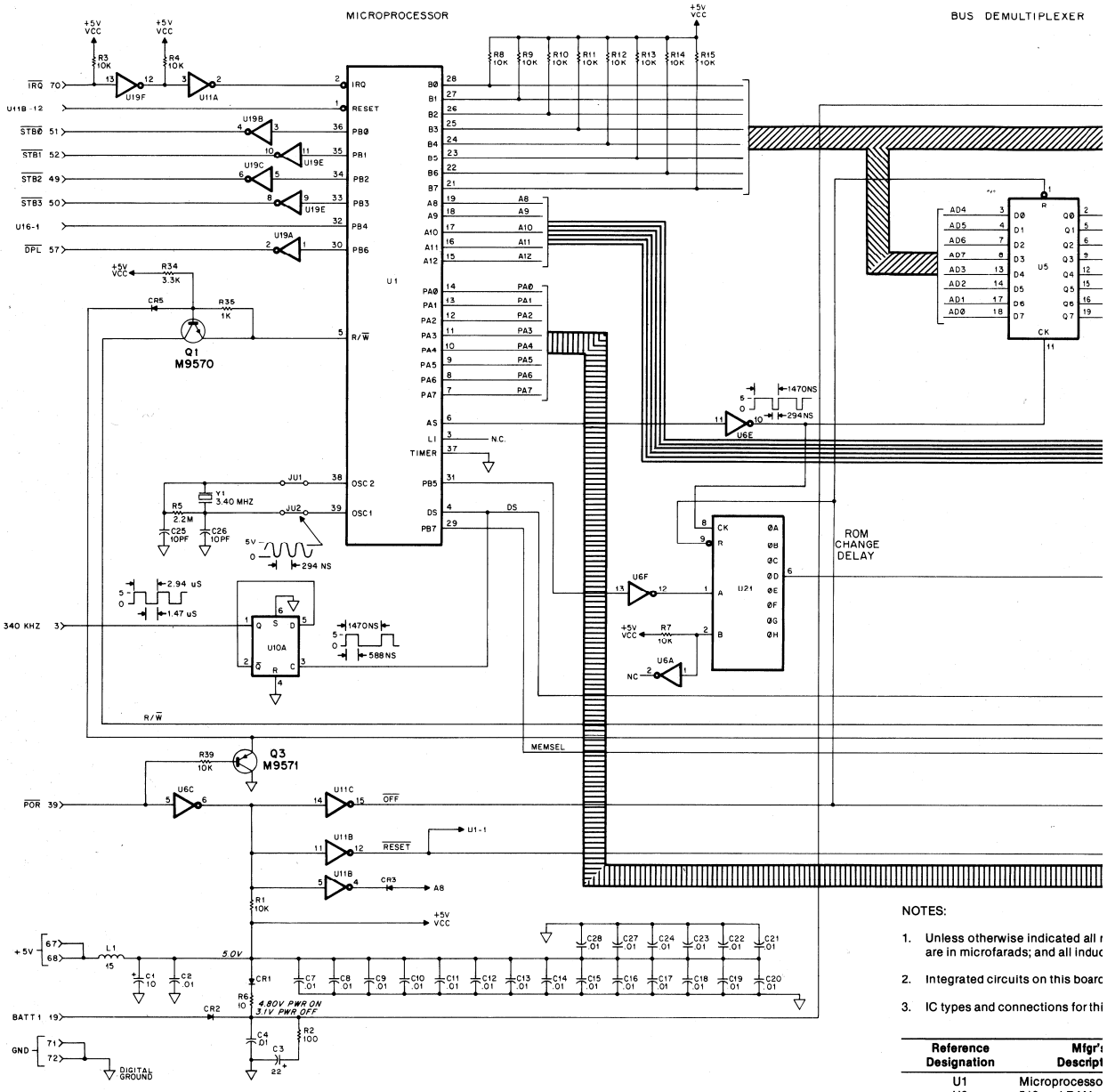


parts list

RTC4023A CPU Board — PL-8454-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		capacitor, fixed uF; + 70-30%; 100 V: unless otherwise stated
C1	23-84665F01	10 uF + 100-10%; 25 V
C2	21-82428B21	.01
C3	23-84762H10	22 uF ± 20%; 15 V
C4 thru 24	21-82428B21	.01
C25, 26	21-82355B11	30 pF ± 5%; 500 V
C27, 28	21-82428B21	.01
		diode: (see note)
CR1, 2	48-84616A01	hot carrier
CR3	48-83654H01	silicon
CR4, 5	48-84616A01	hot carrier
		coil, rf:
L1	24-83451F01	choke; 15 uH
		transistor: (see note)
Q1, 2	48-869570	NPN; type M9570
Q3	48-869571	PNP; type M9571
		resistor, fixed; ± 5%; 1/4 W: unless otherwise stated
R1	6-11009C73	10k
R2	6-11009C25	100
R3, 4	6-11009C73	10k
R5	6-124B30	2.2 meg
R6	6-11009C01	10
R7 thru 24	6-11009C73	10k
R25, 26, 27	6-11009C49	1k
R28 thru 33	6-11009C73	10k
R34	6-11009C61	3.3k
R35	6-11009C49	1k
R36	6-11009C73	10k
R37	6-11009C61	3.3k
R38	6-11009C49	1k
R39	6-11009C73	10k
		integrated circuit: (see note)
U1	51-83625M44	microprocessor
U2, 3	51-83625M55	512 × 4 RAM
U4	51-80397A23	8k × 8 ROM
U5	51-82609M17	octal D flip-flop
U6	51-84561L03	hex inverter
U7	51-84561L38	triple NOR gate
U8	51-83627M04	quad open collector NAND gate
U9	51-84561L47	dual 2 to 4 decoder
U10	51-82884L13	dual D flip-flop
U11	51-82884L02	hex inverter
U12	51-84561L41	1 of 8 decoder
U13	51-82609M56	octal buffer
U14	51-84561L51	hex D flip-flop
U15	51-82609M56	octal buffer
U16	51-82627M03	octal D latch
U17	51-82609M56	octal buffer
U18	51-83627M03	octal D latch
U19	51-84561L03	hex inverter
U20	51-82884L70	hex D flip-flop
U21	51-82609M52	8-bit serial input/parallel output shift register
U22	51-80397A24	8k × 8 ROM
U23	51-84561L08	triple NAND gate
		crystal: (see note)
Y1	48-80378A44	3.4 MHz
		mechanical parts
	45-80395A37	EJECTOR, (YEL); 2 used
	9-84881F01	SOCKET, 24 contact; 2 used
	9-83893M01	SOCKET, 40 contact
	42-10217A24	TIE, wrap
	14-84602K01	INSULATOR, crystal
	84-80377A83	PC BOARD

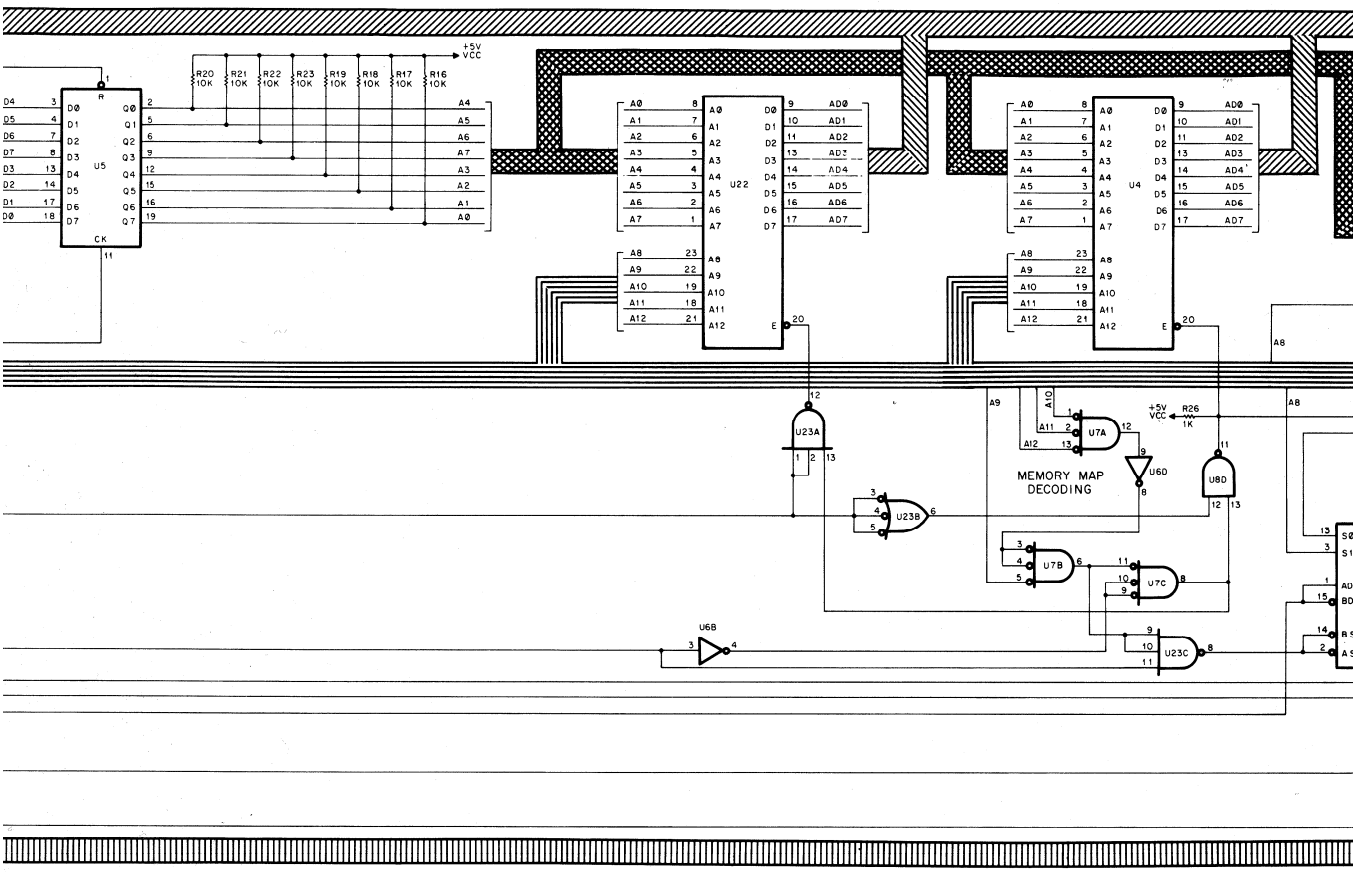
note: For optimum performance, diodes, transistors, crystals, and integrated circuits must be ordered by Motorola part numbers.



NOTES:

1. Unless otherwise indicated all r are in microfarads; and all induc
2. Integrated circuits on this boarc
3. IC types and connections for thi

Reference Designation	Mfgr's Descript
U1	Microprocesso
U2	512 × 4 RAM
U3	512 × 4 RAM
U4	8k × 8 ROM
U5	Octal D Flip-Flc
U6	Hex Inverter
U7	Triple NOR
U8	Quad Open Col
U9	Dual 2 to 4 Dec
U10	Dual D Flip-Flo
U11	Hex Inverter
U12	1 of 8 Decoder
U13	Octal Buffer
U14	Hex D Flip-Flop
U15	Octal Buffer
U16	Octal D-Latch
U17	Octal Buffer
U18	Octal D-Latch
U19	Hex Inverter
U20	Hex D Flip-Flop
U21	8 Bit Serial/Par
U22	8k × 8 ROM
U23	Triple NAND

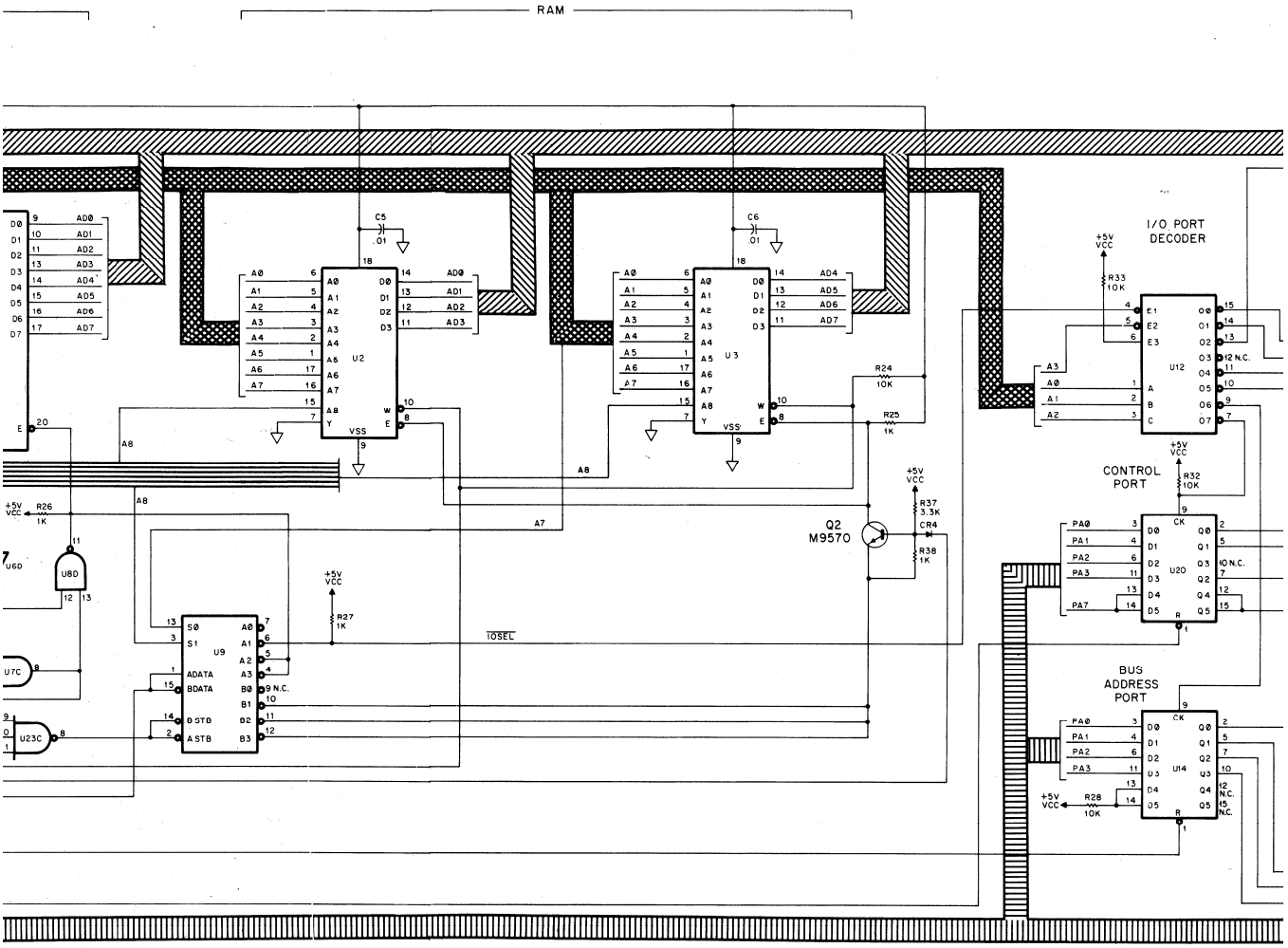


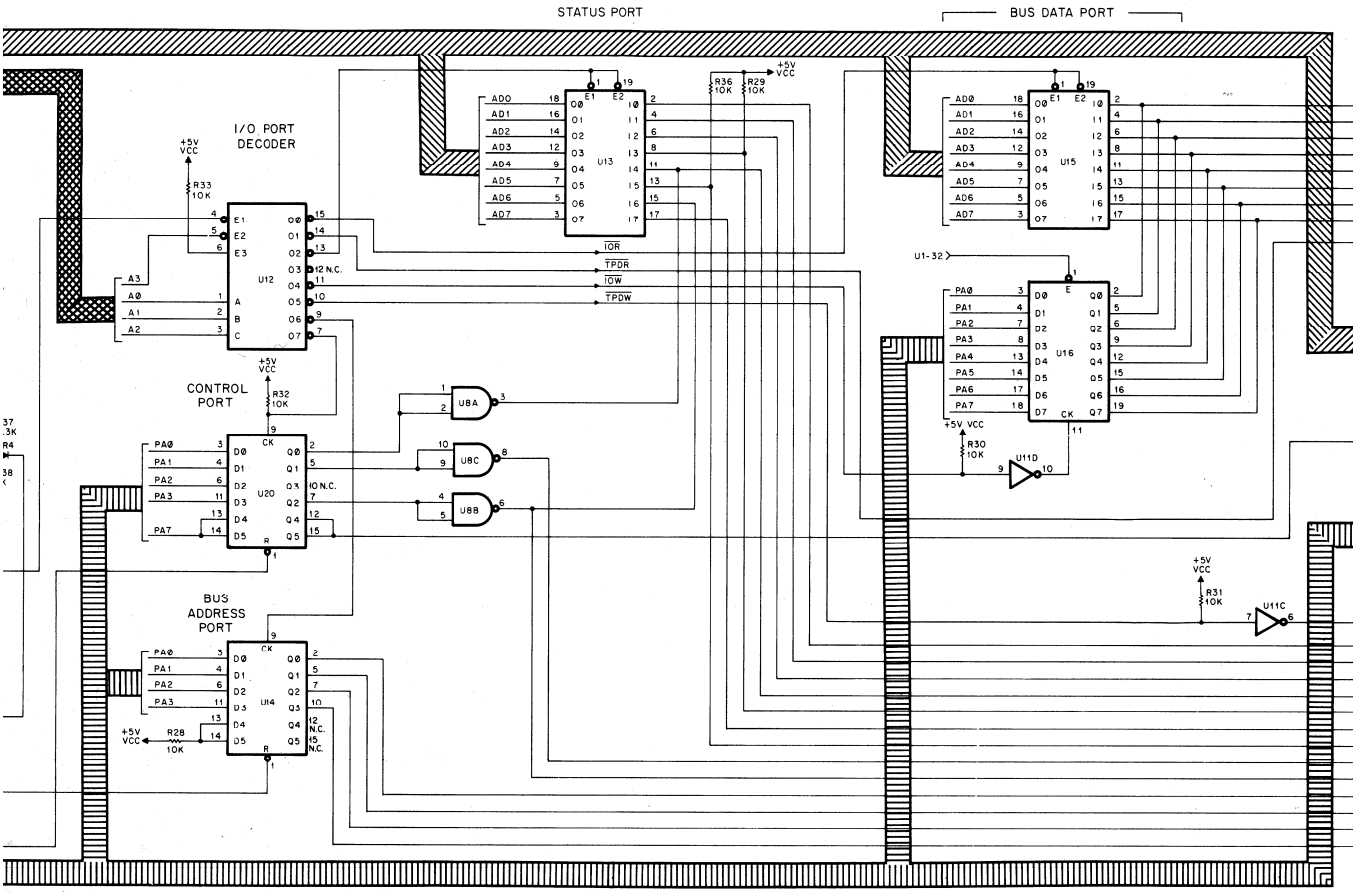
is otherwise indicated all resistor values are in ohms; all capacitor values microfarads; and all inductor values are in microhenries.

rated circuits on this board are TTL and CMOS devices.

es and connections for this board are as follows:

rence gnation	Mfgr's Description	VCC	GND	Ram Pwr
J1	Microprocessor	40	20	
J2	512 × 4 RAM		9	18
J3	512 × 4 RAM		9	18
J4	8k × 8 ROM	24	12	
J5	Octal D Flip-Flop	20	10	
J6	Hex Inverter	14	7	
J7	Triple NOR	14	7	
J8	Quad Open Coll NAND	14	7	
J9	Dual 2 to 4 Decoder	16	8	
10	Dual D Flip-Flop	14	7	
11	Hex Inverter	1	8	
12	1 of 8 Decoder	16	8	
13	Octal Buffer	20	10	
14	Hex D Flip-Flop	16	8	
15	Octal Buffer	20	10	
16	Octal D-Latch	20	10	
17	Octal Buffer	20	10	
18	Octal D-Latch	20	10	
19	Hex Inverter	14	7	
20	Hex D Flip-Flop	16	8	
21	8 Bit Serial/Parallel Shift	14	7	
22	8k × 8 ROM	24	12	
23	Triple NAND	14	7	

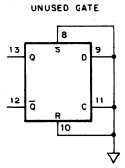

RAM
I/O PORT DECODER
CONTROL PORT
BUS ADDRESS PORT
U2
U3
U9
U12
U20
U14
U6D
U8D
U7C
U23C
C5 .01
C6 .01
R24 10K
R25 1K
R26 1K
R27 1K
R28 10K
R32 10K
R33 10K
R37 3.3K
R38 1K
CR4
Q2 M9570
+5V VCC
A8
A7
IOSEL
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
PA0
PA1
PA2
PA3
PA7
ADATA
BDATA
B STB
A STB
N.C.



LEGEND

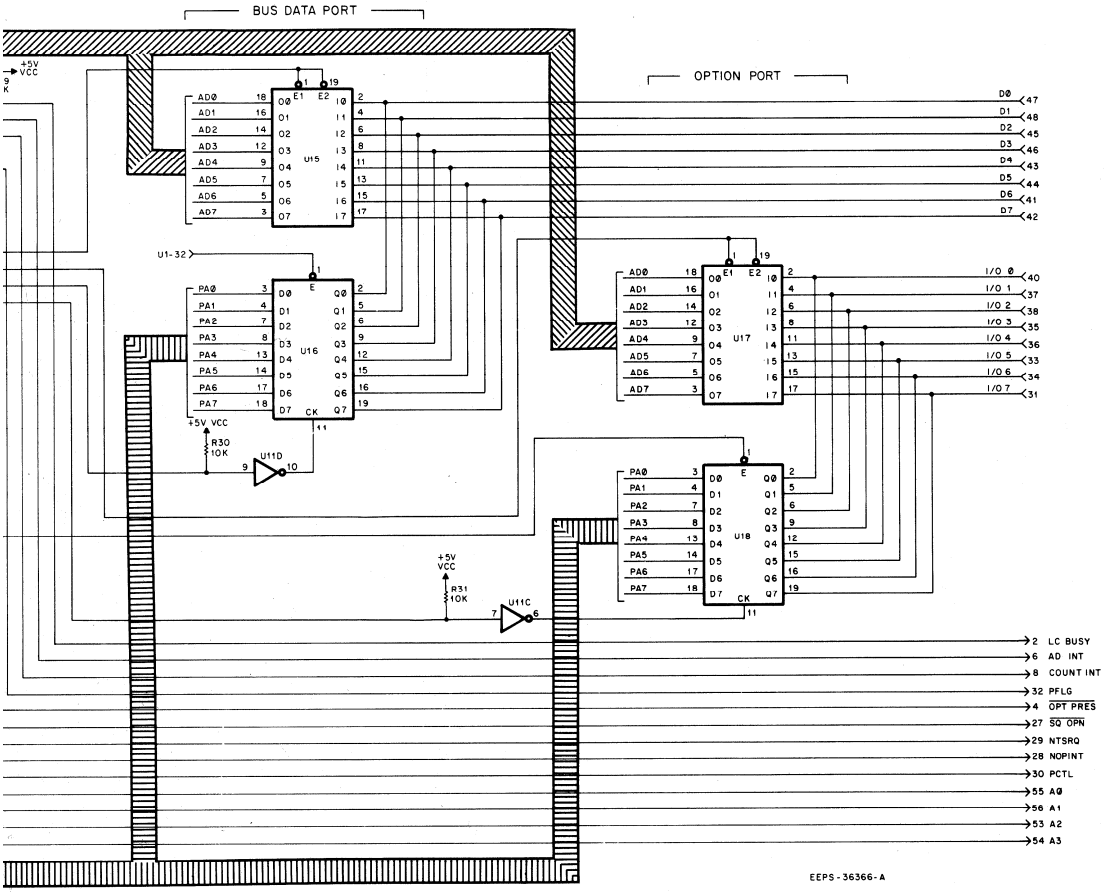
⏚ = DIGITAL GROUND

UNUSED GATE



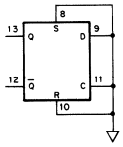
CPU BOARD (A08)

MODEL RTC4023A
SCHEMATIC DIAGRAM, CIRCUIT BOARD DETAIL,
AND PARTS LIST



LEGEND
= DIGITAL GROUND

UNUSED GATE



CPU BOARD

Motorola No. PEPS-36850-O
(Sheet 2 of 2)
8/12/83- PHI

COUNTER BOARD (A10)

MODEL RTL4106A

1. DESCRIPTION

The counter board consists of the microprocessor bus interface frequency error and PL (Private-Line™) counter, analog-to-digital converter, and audio circuitry.

2. THEORY OF OPERATION

2.1 MICROPROCESSOR INTERFACE

The counter communicates with the microprocessor via the system data and address bus. The address and strobe are decoded by address decoder U1 to obtain load commands and control pulses. The data bus, DØ-D7, is connected to control latch U14 and output drivers U10 and U11. The drivers gate data onto the data bus when enabled by the A/D and counter read commands. U14 latches the bits that control the audio routing. The AC/DC SEL command output of U14 is sent to the analog interface board (AIB) where it controls the coupling of the external input to the AIB. U24 is the counter mode latch that generates the FREQ ERROR/PL and .1/.01 SEC GATE signals that are used to control the mode of operation.

2.2 COUNTER OPERATION, FREQUENCY ERROR MODE

2.2.1 Counter mode latch U24 enables the counter to measure the receiver i-f frequency. The microprocessor reads the i-f, subtracts 10.7 MHz, and displays the result on the front panel LCD. The 10.7 MHz signal from the receiver is applied to the phase comparator input of phase-locked loop U26. The i-f is compared with that of the PLL VCO to produce an error voltage that locks the VCO frequency to that of the input i-f. Thus, the VCO output of U26 is a low noise reproduction of the i-f, and is further amplified by transistors Q5 and Q6. With U24-2 high, the B inputs to multiplexer U2 are gated to the U2 outputs. U23A divides the SYNTH 1 kHz frequency by 10. U25A and U25B select either 1 kHz or 100 Hz for the clock input of U3 providing a .01 second or 0.1 second gate time for the frequency counter. The count input to counter U8 is connected to the squared VCO signal and the enable command is sent to U6-4 via U2.

2.2.2 Counter operation begins when the counter start pulse (START COUNT) is decoded at U1. The pulse causes U5 to toggle causing preset to be removed from U3, and U8 counts the i-f frequency. $\overline{\text{COUNT ENABLE}}$ stays low until U3 rolls over from the F state to Ø. Thus, U8 is enabled for 10 cycles of the gate clock. State F is decoded internally by U3 and appears at the carry output, U3-7. The low-to-high transition of the carry toggles U5 Q output high. U3 returns to preset and the count cycle ends. The low-to-high transition of $\overline{\text{COUNT ENABLE}}$ latches an interrupt into U13B to end the microprocessor cycle. The counter interrupt latch is cleared by the $\overline{\text{CTR READ}}$ pulse. The microprocessor reads three bytes from U8 sequentially and then resets U8 by addressing U1-9.

2.3 COUNTER OPERATION, PL MODE

2.3.1 Before the sub-audible PL tone can be counted, it must be separated from the recovered audio. The PL filter comprised of U20A, U21, and U22 has a cutoff frequency of 270 Hz and this signal is squared for counting by U20B and Q4.

2.3.2 With U24-2 low, the counter is in the PL mode and the A inputs of U2 are gated to the U2 output. The count input of U8 is connected to the 10 MHz timebase and the PL tone drives the clock input of U3. The count enable of U8 is driven from the carry output of U3. PL frequency is measured by gating 10 MHz into U8 for one period of the audio tone. The microprocessor reads the number of 10 MHz pulses counted, multiplies by 100 nanoseconds per pulse and calculates the reciprocal of the time to obtain the PL frequency.

2.3.3 Counter operation is similar to that for frequency error except that U3 is preset to a different value and U23B is enabled. For normal operation in which a tone is present, reset is removed from U23B; preset is removed from U3 when U5 toggles after a counter start pulse is decoded. The carry output of U3