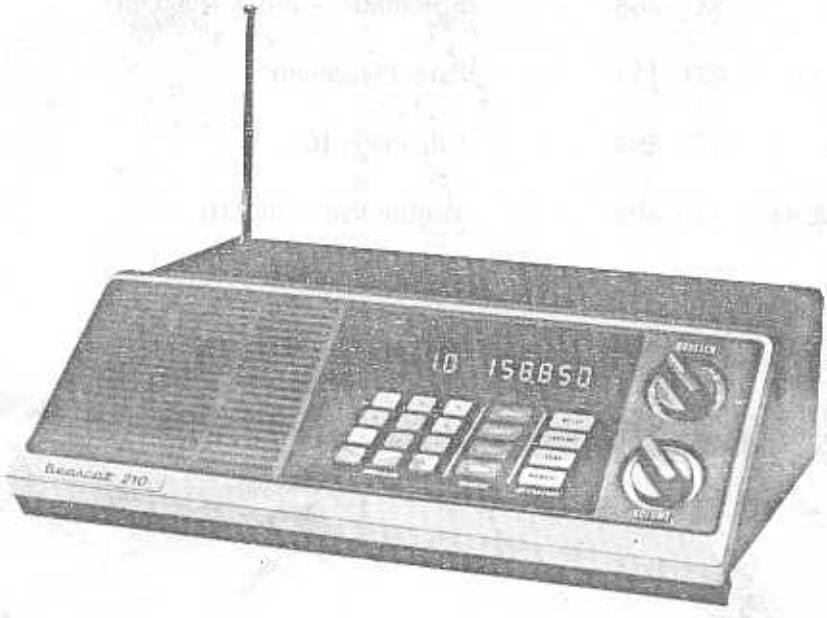
Bearcat®

SERVICE MANUAL

BC – 210



MFG. BY – Electra COMPANY

DIVISION OF MASCO CORPORATION OF INDIANA
CUMBERLAND, INDIANA 46229

Reference Document List

(Fig. 1)	XC 668	Schematic – Block Diagram
(Fig. 1-A)	XD 151	Parts Placement
(Fig. 2)	XB 894	Schematic IC – 1
(Fig. 3 & 4)	XB 898	Tuning Vol – BC210
(Fig. 5)	XB 895	Schematic IC – 2
(Fig. 6)	XC 667	Schematic – Sq. Sys.
(Fig. 7)	XD 248	Synthesizer – BC210

BC-210 SERVICE MANUAL

CIRCUIT DESCRIPTION

SPECIFICATIONS*

Size:	7 x 3½ x 9
Weight:	4½ lbs.
Cabinet:	Vinyl-clad steel
Power Requirements:	117Vac 50-60 Hz 11W; or 13.8Vdc 6W
Antenna:	Telescoping antenna electronically tuned for all bands (supplied) Connector provided for outside antenna.
Input Impedance:	50-70 ohms
Sensitivity:	H and L bands ±5KHz deviation - .6uv/12db SINAD.U and T bands slightly less.
Channels:	10 with synthesized circuitry - no crystals required
Frequency Ranges:	Low Band 32-50MHz Ham Band 146-148MHz High Band 148-174MHz UHF Band 450-470MHz UHF "T" Band 470-512MHz Plus: Gov't UHF 416-450MHz
Scan Rate:	Approximately 20 channels per second
Audio Output:	2W Peak 8 ohm Load

I

GENERAL

Figure 1 is a block diagram illustrating the main elements of the Bearcat 210 receiver. From a single antenna input, Low/High VHF (32-50MHz, 146-174MHz) and UHF frequencies (416MHz-512MHz) are coupled through separate track-tuned R-F amplifier and mixer stages to a common I.F. (10.8MHz). A second oscillator (10.4MHz) is used for mixing down to a 400KHz second I.F. before the signal is limited and demodulated. The recovered audio is then coupled to the audio amplifier and also filtered for proper squelch activation.

The local oscillator signal is derived from a phase-locked-loop synthesizer. The VCO (Voltage-controlled oscillator) frequency is divided down by a programmable counter which is preset from memory and compared to a reference frequency. Any frequency or phase difference produces a correction signal to change the VCO tuning voltage. This tuning voltage then forces the VCO to oscillate at the frequency required for the counter to produce an output that is in phase with the reference frequency. Thus, changing the modulus of the counter will change the frequency of the VCO. In order to increase the range of the counter, it is prescaled by 15 to 16 on all bands and the VCO is mixed with a 133MHz oscillator on High Band and VHF to achieve the higher frequencies required. For UHF, the VCO is then tripled to obtain its proper local oscillator frequency.

The frequency program is entered from a decimal keyboard into a microprocessor where it is multiplexed to drive the display and decoded to enter the proper binary code in memory to control the synthesizer.

II

R-F SECTION

UHF:

Referring to the Bearcat 210 schematic diagram, the UHF signal is coupled from the antenna through D1, a pin diode forward biased through R2, and then through C1 and C2 to the first R-F tuned circuit of C11, VVC3 and L3. The proper DC tuning voltage is applied through R14 to VVC-3 so that it's capacitance in series with C11 resonates with L3 at the programmed frequency. The UHF signal is then coupled through C13 to the R-F input (pin 5) of IC-1 (NB57-801). Referring to figure 2, the UHF frequencies are amplified and brought out through pin 15 with an output load of L8 and R8. Note that the tripled oscillator frequency is also present at this output. The amplified signal is again track-tuned by C67, VVC-5 and C16 with the tuning voltage through R3. The lead length on C16 is acting as the inductor for this tuned circuit. The UHF and tripled oscillator signal is then coupled through R15 and C68 to pin 14 where they are mixed down to an I.F. frequency of 10.8MHz at pin 12 with the tuned I.F. circuit (T3) as the load.

VHF:

The High Band frequencies are coupled from the antenna through D1, forward biased by R1, and then C1, L11-C5, and C69 to the first R-F tuned circuit. C5, L11, and C50 form a trap to keep UHF frequencies out of the VHF circuits. The High Band is track-tuned with L4 and the series capacity of C3 and VVC-4 via the tuning voltage through R9. Note that D15 is forward biased through R4 which grounds L4 through C6 to provide the proper inductance for tracking on High Band.

The Low Band frequencies are coupled through L1, C5-L11, and C69 to the first tuned circuit. Note that D1 is not forward biased, the antenna loading coil L1 matches the antenna to the radio in Low Band. D15 is also turned OFF in Low Band removing the AC ground from L4. The tuned circuit therefore consists of the series inductance of L4 and L5 and the series capacity of C3 and VVC-4.

The Low and High Band frequencies are then coupled through C71 to the RF input (pin 8) of IC-1. These signals are amplified and brought out on pin 9 along with the oscillator signal. At this output, the second track-tuned circuit is composed of L9, L10, C17 and VVC-6. On High Band, D11 is forward biased to ground L9 through C15.

The amplified signal and oscillator signal are then coupled through C20 to the VHF mixer input (pin 10) of IC-1 where they are mixed down to the 10.8MHz I.F. output frequency.

VCO:

The Voltage Controlled Oscillator consists of dual MOS transistors within IC-1. The oscillator frequency is determined by the external tuned circuit at the input pin 3 (C7, L7, L6, VVC1, VVC2).

On High Band or UHF band, D14 is forward biased by R5 or R6 respectively, grounding L6 through C9. On these bands, the inductance of L6 resonates with the series capacity of C7 and VVC's 1 and 2 to provide the oscillator frequency range from 135 to 167MHz. The high inductance of L7 is almost negligible at these frequencies since it is in parallel with L6 through C7.

On Low Band, D14 is not forward biased and L6 becomes negligible due to the high series inductance of L17. The VCO frequency is now determined by L7 and VVC's 1 and 2 to provide the VCO range from 21 to 40MHz. The DC current source for all bands is through L6, R11 and L17.

TRACK-TUNING:

The tuning voltage versus frequency curves, produced by both VCO ranges, are used as the reference for track-tuning all R-F circuits.

The Low Band VCO curve (figure 3) is applied directly to VVC's 4 and 6 through R50, R9 and R18 for tracking the Low Band R-F circuits.

The High Band tuned circuits require a different slope for tracking than is produced by the VCO (See figure 4). This is accomplished by Q2 which conducts only in High Band operation to offset the tuning voltage. When the VCO voltage is below 9 volts, Q2 is sourcing current through R50 and R51 to increase the tracking voltage to VVC's 4 and 6 through R9 and R18. When the VCO voltage exceeds 9 volts, Q2 sinks current through R50 and R51 to reduce the R-F tracking voltage.

For tracking the UHF circuits, the tuning voltage level required is less than the VCO voltage. This is provided by D5 and voltage divider R56 producing the offset is shown in figure 4.

I.F.:

From the mixer output at pin 12 of IC-1, the 10.8MHz I.F. frequency is passed through two quartz crystal filters (FL 1 & 2) to provide selectivity. These filters establish I.F. bandwith (15KHz).

The I.F. then goes to pin 16 of IC-2 (NB53101) for mixing down to the second I.F. (Refer to figure 5). The second oscillator is within IC-2 and controlled by the external crystal Y1. This 10.4MHz oscillator is internally mixed with the 10.8MHz I.F. input to produce the 400KHz second I.F. at pin 3. The 400KHz I.F. is coupled through the double-tuned I.F. transformer T4 to the I.F. amplifier input at pin 5. The I.F. is then limited and demodulated with the recovered audio output at pin 9. T1, R23 and C23 provides the phase shift to balance the demodulator.

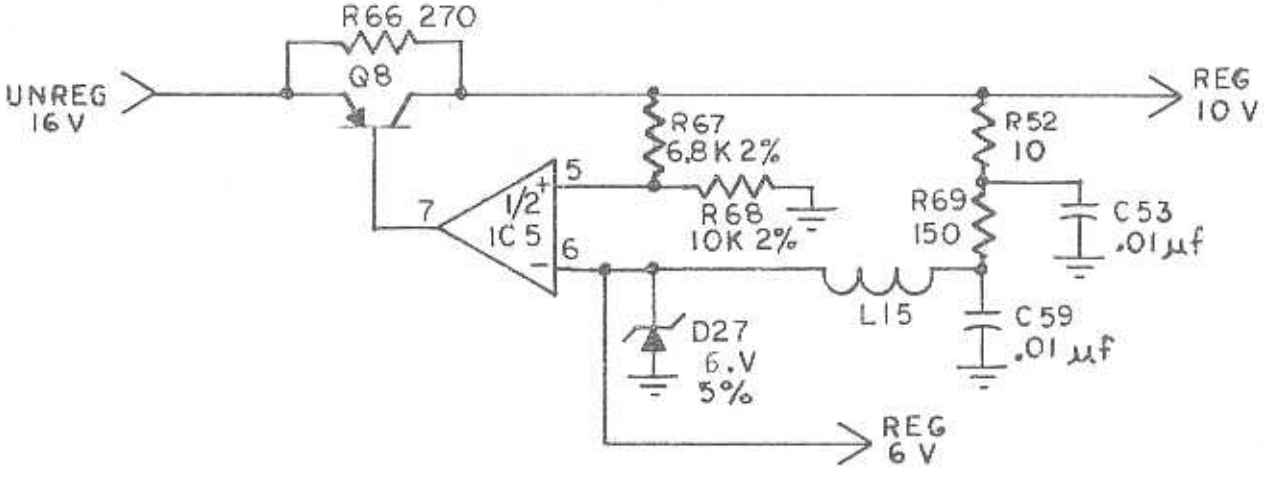
AUDIO:

The recovered audio at pin 9 of IC-2 goes through the low-pass filter R26 and C29 before being coupled through C28 to the volume control R31. R84 and C47 then form a second low-pass filter at the input of IC-3 which provides amplification to drive the speaker.

POWER SUPPLY:

The voltage supply for the Bearcat 210 is developed by the full-wave rectifier circuit of T2, D8, and D9. This develops 16 volts, filtered by C48 for supply to the audio (IC-3) and display drivers.

The 10v/6v Reg. supply is shown in Fig. 6A.



POWER SUPPLY (continued)

The un-regulated 16v is regulated by Q8 to 10v. The input to the base of Q8 determines how much Q8 is turned on or off. The op-Amp in IC-5 compares the two inputs at pin 5 and pin 6. Pin 6 is the Zener (D27) regulated 6v reference and pin 5 is the 10v regulated output divided to 6v by R67 and R68. If the output of Q8 at the collector is low the OP-Amp turns on Q8 harder thus raising the output until it reaches 10v. R66 assures proper starting of this circuit.

The 6 volts regulated by D27 is used as supply voltage for IC-2, 7, 8, 9, 10 and 11. The 10 volts regulated by Q8 and IC-5 is used as the voltage supply for Q3, IC-6, IC-12 and IC-13. A 9 volt source is derived from +10 through R80 for IC-1, Q1, Q2, Q5, Q6, Q9 and Q29.

IV

SQUELCH

The Bearcat 210 utilizes 3 squelch systems. The first is the conventional noise squelch system which is used to unsquelch the radio when a carrier is received causing noise quieting through the system. The second system will squelch the receiver if a transmission is received containing a continuous 2KHz tone such as that used for marking the mobile telephone frequencies. The third is a system to permit the receiver to unsquelch only when a receiver signal is at the proper frequency thereby preventing the receiver from responding to adjacent channel frequencies of sufficient strength to produce noise quieting in the I.F. system. This last system, in the SEARCH mode, prevents signals of sufficient strength from stopping the receiver at an adjacent frequency prior to the time it reaches the active channel.

NOISE SQUELCH:

The noise squelch system uses an operational amplifier within IC-2 as a bandpass amplifier (refer to figure 6). The resonant frequency (8.5KHz), Q, and gain are determined by external components R24, R25, R27, C26 and C27. It is necessary to use this high frequency noise so normal audio frequencies do not activate the squelch system.

When no transmission is being received, the high frequency noise (8.5KHz) is amplified by IC-2. The noise is then coupled through C30 and detected by D2 to produce a negative voltage which is filtered by R28 and C31. This negative voltage is then applied through R86 to pin 12 of IC-2 which overcomes the positive bias provided by the squelch control R30 through R87 and R88 to pins 1 and 7 respectively of IC-13 which are both normally high (+9 volts). With the voltage at pin 12 below the turn on level (due to the negative voltage from the detected noise) pin 13 voltage will go high to permit the receiver to scan and pin 14 will be low shutting off the audio at the volume control R31. When a signal is received, the resultant I.F. produces noise quieting through the system which reduces the 8.5KHz noise amplified by IC-2 thereby reducing the negative voltage level from the detected noise. This reduced negative level permits the positive bias of R30, R87, and R88 to reach the turn-on level at pin 12 of IC-2 which forces pin 13 to go low to stop scanning and shuts off the pin 14 output to enable the audio to reach IC-3 for amplification.

2KHz TONE SQUELCH:

The 2KHz squelch system uses one of the two op-amps within IC-5 in an active filter arrangement. Referring to figure 6, the gain, bandwidth and frequency are determined by C56, C57, R39, R71, and R73. R73 is adjusted to make the circuit resonant at exactly 2KHz. The narrow bandwidth provided by IC-5 is required to prevent audio frequencies near 2KHz from triggering the squelch system.

When a signal is received having a modulation frequency of 2KHz, the amplified signal at pin 1 of IC-5 is coupled through C55 and R70 to C51. Note that the cathode of D4 is biased at a +1.9 volt reference. If the output of IC-5 is less than 5.2 volts peak-to-peak (1.8 volts r.m.s.), the positive peaks will be less than 2.6 volts so D4 does not conduct and the average DC at C51 is 0 volts. If the 2KHz output of IC-5 exceeds 5.2 volts, peak-to-peak, the positive peak (+2.6 volts) will be limited by turning on D4. Since the negative peaks are not limited, a negative DC voltage is developed across C51. When the negative voltage on C51 becomes less than .7 volts below the bias on pin 12 of IC-2, D13 will conduct causing the voltage at pin 12 to go low forcing pin 13 to go high to resume scanning and pin 14 goes low to shut off the audio.

FREQUENCY DETECTOR SQUELCH:

The purpose of this circuit is to keep adjacent channel activity from unsquelching the radio. This would happen in conventional scanner radios in the presence of strong or interfering signals. This circuit will not let the radio unsquelch if the signal is more than 7KHz from received frequency.

The voltage comparator window is set up in IC-13. The upper voltage limit is on pin 5, the lower voltage limit is on pin 3. These voltages are established by R58, R57, R79, and R81. If a voltage above the upper limit or below the lower limit appears on common pins 3 and 6, the output of pin 1 or 7 will go low. This reduces the voltage at pin 12 of IC-2 forcing the receiver to continue scanning. The voltage is within the limits or "within the window" both outputs will be high. With both outputs high in normal operation, the squelch control R30 is used to set the bias for pin 12 of IC-2. If these outputs are high and other squelch conditions acceptable the radio will be unsquelched.

The discriminator output (IC2 pin 9) develops a d.c. voltage which is inversely proportional to frequency. The slope of the discriminator is approximately .18 volts/KHz (from the center frequency) and has a dc offset of 2.75v. dc. This voltage is filtered by R54 and C72 and serves as the window detector input.

V

SYNTHESIZER

The Bearcat 210 synthesizer consists of a Voltage Controlled Oscillator (VCO) which is mixed down by 133MHz (H-U/T) and prescaled before division by a presettable counter controlled from memory. The output of this divider is compared to a reference frequency producing an error signal for a loop filter to compensate the VCO voltage to correct the frequency.

MIXER:

Referring to figure 7, the VCO signal is taken from pin 1 of IC-1 and buffered by an emitter follower stage Q29. It is then coupled through C41 to Q1 which serves as a 133MHz oscillator controlled by Y2 and as a mixer. Q1 is biased for operation as an oscillator and mixer only in the H or U/T Bands by R61 or R60. Since the lower frequency range of the Low Band VCO requires no mixing down before the prescaler, Q1 serves only as a buffer stage. In H or U/T Bands, L14 permits only the different frequency (VCO-133MHz) to pass through to IC-6.

PRESCALER:

The input at pin 2 of IC-6 (NC57902) is divided by 15 or 16 with the output at pin 11. The division is by 15 when the control input pin 6 is HIGH and by 16 when LOW.

÷ N:

The prescaler output is connected to pin 7 of IC-7 (NB25702) to clock the ÷ N and 12+A counters. Nine memory bits are used for presetting the ÷ N counter and four for the 12 + A counter to provide the proper division at the programmed frequency.

Initially the 12 + A counter output is HIGH and the ÷ N and 12 + A counter is clocked once for each 15 clocks at the prescaler. When 12 + A is reached, the output goes low to allow the prescaler to divide by 16 until the divide by N has reached its full count of 512 = (2^9).

The ÷ N advances 12 + A times when the prescaler is dividing by 15 and the remainder (512 - M - 12 + A) when the prescaler is dividing by 16. When the ÷ N has reached full count, it's output goes high to reset itself and the 12 + A counter to start over again. The total division by prescaler and ÷ N is therefore:

$$15\ (12 + A) + 16\ (512 - M - 12 + A) \qquad \text{Equation 1}$$

$$\text{Simplifying, } = 8180 - 16\ M + 31A \qquad \text{Equation 2}$$

PHASE COMPARATOR:

The reference frequency for comparison with the ÷N output is derived from the 10.4MHz oscillator in IC-2 controlled by Y1. the 10.4MHz signal is coupled to pin 16 of IC-6 where it is divided by 4 for an output of 2.6MHz at pin 11 for an input at pin 5 of IC-7. The 2.6MHz signal is then divided by 520 for LOW or HIGH VHF and by 624 for UHF controlled within IC-7 by the U bandswitch information in memory. This provides a frequency of 5.0KHz on LOW and HIGH bands and 4.16667KHz (4.16667 x 3 =12.5KHz channel spacing on U/T band) on UHF as a reference for comparing the ÷ N output in the frequency phase comparator.

The phase comparator provides a tri-state output at pin 3 of IC-7. This output will go low when the VCO and the ÷ N output is low in frequency. When the VCO is high in frequency the output will go high. When both are in phase, the phase-comparator has a high impedance output.

LOOP FILTER:

The phase comparator output is filtered and amplified by IC-4, R46, and R47 establish a 3 volt bias on pin 2 of IC-4 to match the bias on pin 3 provided by R36 and R37. The correction pulses are applied through R34 and R35 and filtered by C-54 to the inverting input of IC-4.

If the VCO is running too low in frequency, negative correction pulses will go to the inverting input forcing the output DC voltage to go higher. Meanwhile, C36 in the feedback loop charges to oppose the input change and hold the output at this new level. In the same manner, if the VCO runs to high in frequency, positive correction pulses from the comparator will cause a decrease in the control voltage from IC-4 forcing the VCO back down until the ÷N output is in phase with the reference to stop the correction pulses. When the VCO is on frequency and the comparator output is a high impedance, the charge on C36 will hold the control voltage keeping the VCO at that frequency. Since the width of the correction pulse is dependent on the degree of phase difference, the further the VCO is off frequency, the longer will be the pulse to correct it. D23 and D24 block noise less than 1.4 volts peak to peak coming from the phase comparator when its output is in the high impedance state.

VOLTAGE TRIPLER:

In order to achieve the voltage range required from the loop filter for tracking the VCO and R-F circuits, a supply voltage of 25 volts is required. This supply is derived from the Q3 voltage tripler circuit.

The 12 + A Counter output at pin 6 of IC-7 drives the base of Q3 through R75. This output, used for prescaler division control, has a variable pulsewidth and a frequency of the synthesizer reference (5.0KHz L/H, 4.16667KHz U/T).

Q3 is a MPS A13 Darlington transistor having a minimum beta of 5000 which amplifies the prescaler signal with R76 as the collector load. A high B transistor reduces PLL noise in receiver.

Initially, C63 is charged to 9.3 volts through D19 and C66 is charged to 8.6 volts through D18 and D19. With a 10 volt peak-to-peak output at the collector of Q3, the charge on C63 changes from its 9.3 volt reference to 19.3 volts peak. This voltage is then detected by D18 to charge C66 to the peak voltage (18.6 volts). This voltage then charges C64 through D17 to 17.9 volts referenced to the collector of Q3. With the voltage swing at the collector of Q3, C64 changes from the 17.9 volt reference to 27.9 volts which is detected by D16 and filtered by C65 to charge to peak voltage of 27.2 volts at the output. This voltage is loaded down to about 25 volts by the current drain of IC-4.

FREQUENCY PROGRAM CODES:

As discussed in the synthesizer description, the microprocessor derives a 15 bit binary code for each frequency program. Thirteen (13) are used for presetting the ÷ N and 12 + A counters and the remaining two for U and H bandswitch control.

Referring to equation 2 on page 9, we found the total division by prescaler and ÷ N to be:

$$8180 - 16\,M + 31\,A$$

In Low Band, with the VCO frequency equal to the reference frequency (5KHz) times the prescaler and ÷ division.

$$F\ (VCO) = (8180 - 16\ M = 31A)\ 5KHz \qquad \text{Equation 3}$$

Since the VCO is 10.8MHz below programmed frequency,

$$F - 10.8MHz = (8180 - 16\ M + 31\ A)\ 5KHz \qquad \text{Equation 4}$$

FREQUENCY PROGRAM CODES: (continued)

Simplifying:

$$10{,}340 - 200\ F\ (MHz) = 16M + 31\ A \qquad \text{Equation 5}$$

Where F is the Low Band receive frequency in MHz, and 16 M + 31 A is the memory binary code.

Since the High Band VCO is mixed down by 133MHz:

$$F - 10.8MHz - 133MHz = (8180 - 16M + 31\ A)\ 5KHz \qquad \text{Equation 6}$$

Simplifying:

$$36940 - 200\ F\ (MHz) = 16\ M + 31\ A \qquad \text{Equation 7}$$

Where F is the High Band receive frequency in MHz and 16 M + 31 A is the memory binary code.

The UHF VCO is tripled and uses a 4.16667KHz synthesizer reference frequency, therefore:

$$\frac{F - 10.8MHz}{3} - 133MHz = (8180 - 16M + 31\ A)\ \ 4.16667KHz \qquad \text{Equation 8}$$

Simplifying:

$$40964 - 80\ F\ (MHz) = 16M + 31A \qquad \text{Equation 9}$$

The formulas derived; equations 5, 7, and 9; permit calculation of the memory program code (16M + 31 A) for any Low, High, or UHF frequency. The result must be converted from base 10 to binary. These formulas represent the decoding done by the microprocessor to derive the snythesizer codes. Example:

To find the binary code for a programmed frequency of 162.55MHz, we use equation 7:

$$36940 - 200\ (162.55) = 16M + 31A$$

$$4430 = 16M + 31A$$

$$4430 = \overline{100010100}^{M}\ \ \overline{1110_2}^{A}\ \ \overline{0}^{\overline{H}}\ \overline{1}^{\overline{U}}$$

BANDSWITCHING:

The bandswitch data from memory is brought out on pins 2 ($\overline{H}$) and 20 ($\overline{U}$) of IC-7. When $\overline{H}$ is Low for High Band operation, base current for Q6 is supplied through D21 (7.5V Zener) to turn it on for 9 volts at the collector. Similarly, when $\overline{U}$ is low, Q5 is turned on through D22 giving 9 volts at the collector for UHF operation. When $\overline{H}$ is HIGH (6 volts) for Low Band or UHF, D21 does not reach its Zener voltage prohibiting current through it, thereby shutting off Q6. Q5 is shut off in the same manner when U is HIGH for Low and High Band operation.

VI

MICROPROCESSOR

KEYBOARD ENTRY AND DISPLAY:

IC-12 is a custom microprocessor I.C. (NB73303) programmed to accept a decimal keyboard input and convert it to the appropriate binary code for synthesizer control and to decode and multiplexthe information for segment scanning of a 10-digit seven segment display.

The decimal keyboard is used to control data inputs K2, K4, and K8 of the microprocessor by decoding the time sequence of pulses from the segment scan outputs when each key is depressed. The information in the calculator is multiplexed to ground segment cathodes of each required 7-segment digit during the sequential strobing of the anodes to display the proper frequency. The cathodes are grounded through their associated driver transistors (Q19-Q28) and 180 ohm resistors (R45 array). The anodes are driven by Q11 - Q18 through R49. The R44 array consists of 22K resistors at the base of each anode driver to insure the shut-off of that device when its controlling segment scan output is low.

PROGRAMMING:

The segment scanning outputs are used in multiplexing control data for the synthesizer. The microprocessor converts the input data to the proper binary code to control the synthesizer. Referring to figure 7, when a frequency is entered through the microprocessor by depressing the "E" key, the D11 output at pin 6 will go LOW. The output of Nand gate 1 ($\overline{D11}$) is therefore HIGH controlling one input of gates 4, 6, 7, 10, 12, 13, and 15. With a HIGH level at one input of gates 6 and 7, the output from the segment E and F lines are used to set and reset the quad latch of gates 6, 7, 8, and 9 to produce the code required for the programmed frequency.

At the same time segment D goes LOW and segment C has a high pulse for one Msec. to set the READ/WRITE latch of gates 13, 14, 15, and 16 LOW. This low READ/WRITE level at pin 19 of IC-7 permits the internal shift register to accept the input data and enter it into memory.

Meanwhile 15 clock pulses are applied from segment G through gate 4 to pin 17 of IC-7 to clock the data into the shift register. This write operation requires about 60 msec.

After data has been entered into memory (60 msec.), D11 will go HIGH again for about 1 msec. and $\overline{D11}$ LOW to reset the

PROGRAMMING: (continued)

READ/WRITE latch of gates 13, 14, 15, and 16 HIGH for READ operation. After this pulse has occurred, $\overline{D11}$ will go HIGH again to permit an additonal 15 clock pulses from segment G to pass through gate 4 to clock data from the memory shift register. With segment P LOW to produce a HIGH at one gate 3 input, the data is clocked through gate 5 on positive clock pulses from segment G to the other input of gate 3 which passes the data into the microprocessor shift register through control input K1 (pin 5). This data is then decoded and multiplexed to drive the display and verify the proper memory program for the frequency entered. This read back operation requires about 40 msec. after which D11 returns HIGH and the microprocessor resumes its segment scanning operation.

The memory supply voltage at pin 22 of IC-7 is a 2-volt level from pin 9 of IC-6. Since VSS of IC-7 (pin 1) is 6 volts, D11 is reverse biased and the 1.6 volt battery is not used. When power is off and VSS is at 0 volts, the battery supplies -1.6 volts to the memory through D10 to retain the programmed data.

If a frequency or search limit is programmed which is not within the band limits of the synthesizer, the microprocessor will not accept the data and displays an E to indicate an error in programming.

The microprocessor requires a fast VCC rise time in order to RESET properly and avoid gliches which could create invalid control data during the transition resulting in memory loss. This rapid power-on time is accomplished by D28, R101, and Q30.

When the 10 volt supply is rising, Q30 is turned off since there is no base current through D28. When the 10 volt supply reaches 8.9 volts, D28 regulates its cathode voltage to 7.5 volts providing base current for Q30 to switch it on supplying VCC to the microprocessor through D25.

SCAN:

With D11 HIGH, K1 serves as a scan control input for the microprocessor. When the receiver is squelched and a HIGH squelch level is present from pin 13 of IC-2 at the input of gate 2, the segment P strobe is passed to an input of gate 3 with the other input HIGH due to a LOW at the DATA input of gate 5. This strobe from gate 3 then controls the K1 input to instruct the microprocessor to scan if the scan key has been depressed.

SCAN: (continued)

The scan operation consists of grounding the digit cathodes for segments A,B,C,D,E, and F sequentially for each complete segment scan sequency (approximately 50 msec.) thereby producing a display of "rolling zeros" from left to right. Meanwhile D11 goes LOW at the end of each segment scan sequence (after segment P) with segment A output inhibited, to permit D11 to set gate 10 HIGH when the next segment B strobe occurs. After inverting by gate 11, this scan signal is differentiated by R74 and C76 to trigger the clock input (pin 15) of IC-7. This clock advances a decade counter controlling a 1 of 10 decoder to address the next memory line. When segment B goes HIGH (4 msec.) D11 returns HIGH to begin the segment scan sequence for the next digit.

After the segment scan sequence is completed for the last digit (D10) and D11 goes LOW, the segment A output goes HIGH to produce a LOW pulse from gate 12 to reset the decade channel address counter to channel 1 through R42 at pin 9 of IC-7. This provides synchronization with the active memory channel and the corresponding digit activated in the scan sequence.

When a signal is received,setting the squelch output of IC-2 (pin 13) HIGH, gate 2 permits the next segment P pulse to pass through to gate 3 which has one input HIGH to produce a LOW at the K1 input. This stops the "rolling zero" scan and sets D11 LOW to permit gate 4 to transfer 15 clock pulses to the memory shift register. This transfers the data through gates 5 and 3 into K1 where it is entered into a shift register for decoding and multiplexing to display the active frequency and channel. This data transfer operation from memory requires about 40 msec.

In the manual mode of operation, the frequency and channel information is continually displayed with each successive activation of the MANUAL key setting Q11 LOW permitting a segment B scan pulse through gates 10 and 11 to advance the memory address along with clock pulses from segment G through gate 4 to clock the new data through gates 5 and 3 for display.

DELAY AND LOCKOUT:

The Bearcat 210 microprocessor (IC12) utilizes an internal memory to store 2 bits per channel in additon to the 15 bits stored by the memory in IC-7. These additional bits controlling scan DELAY and channel LOCKOUT are entered into the microprocessor memory with activation of their corresponding keys.

The DELAY function instructs the microprocessor to wait about two seconds after the scan control at gate 2 goes HIGH,allowing the segment P strobe to pass through gates 2 and 3 to the K1 input before resuming the scan operation. On "simplex" communication systems, using a common frequency for base and mobile, this feature allows time for a reply before scan is resumed.

DELAY AND LOCKOUT: (continued)

The LOCKOUT function instructs the microprocessor to bypass undesired channels in its scan sequence.

Both LOCKOUT and DELAY are recalled and entered into the microprocessor shift register along with channel and frequency information for display. The delay function is symbolized on the display by a small square in the first digit location and LOCKOUT by a dash in the fourth digit location from the left.

Successive activation of DELAY or LOCKOUT keys alters the program state for that function. Since DELAY and LOCKOUT data are not stored in the memory in IC-7, this information is lost when power is turned off.

SEARCH:

The 210 microprocessor includes the capability of searching frequencies between any programmed limits of each band. When a frequency is entered into the microprocessor register through the keyboard and the LOWER limit key is depressed, the data is stored in the microprocessory memory and used to reset a 13 bit binary counter. When a frequency is entered for the UPPER limit, it too is stored in memory and used for presetting the counter.

When the START key is depressed, D11 goes LOW to set $\overline{\text{D11}}$ HIGH permitting 15 clock pulses from the segment G output to pass through gate 4 to the memory shift register. Meanwhile the memory READ/WRITE control (pin 19) was set low when $\overline{\text{D11}}$ went HIGH by the segment D line going LOW at the same time and segment C supplying a positive pulse for 1 msec. to set the latch of gates 13, 14, 15, and 16.

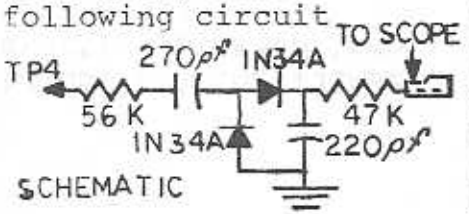
With the READ/WRITE control LOW, the low search limit frequency code is transferred through segment E and F outputs and decoded by the quad latch of gates 6, 7, 8, and 9 to be clocked into memory by the 15 clock pulses from gate 4. These clock pulses are also used before inversion by gate 4 to permit the data to pass through gates 5 and 3 to the K1 input where it is entered into the microprocessor shift register.

When D11 goes HIGH at the end of the WRITE time, the date in the microprocessor shift register is decoded for frequency display and the READ/WRITE control goes HIGH to allow the new memory data to control the synthesizer.

SEARCH: (continued)

This sequence is repeated with the microprocessor binary counter counting down one bit at a line from the low frequency search limit code to the high limit code.

The 50 msec. WRITE time and 50 msec. READ time for each frequency permits a search rate of 10 frequencies per second. After the microprocessor counter has reached its high frequency limit (lowest code), it is reset to the low frequency code to repeat the search. The sequential count of the binary counter in search can be stopped at any time to display the frequency by depressing the HOLD key. The search operation with the programmed limits may also be moved for use in another synthesizer memory channel by advancing to that channel with the MANUAL key and depressing START to continue the search sequence. The last search frequency present before changing channels will remain in memory on the original search channel. Since the search limits are stored only in the microprocessor, these instructions are lost when power is turned off.

NO.	DESCRIPTION	INPUT SIGNAL	ADJUSTMENT	NOTES
1	L-Band - Tuning Voltage calib.	None Radio programmed to 33.76MHz	Adjust L7 (violet) For 3.3± .2 volts at TP3	
2.	H-Band - Tuning Voltage calib.	None Radio programmed to 146.05	Adjust L6 (red) For 2.8v ± .2v at TP3	
3.	I.F. Adjustment	Method 1 Apply a swept 10.8MHz signal to ant.input. It is desirable to sweep ±25KHz at a 60Hz rate. (or less). See notes for level. (Radio may be programmed to any L or H frequency).	Monitor output of TP4 with Det.,Probe or the following circuit  SCHEMATIC	It is important that the Sig. input level be adjusted to keep I.F. from limiting.
			Scope should be set to .01 to .05v/Div range. Adjust scope pattern T4-Bottom slug-Max.Amp. T4-Top Slug - Symetry T3-For min. ripple	If sweep is at 60Hz rate, scope may be on line sync. otherwise, Horizontal input must be attached to sweep signal
		Method 2 Apply an L or H signal swept by a sawtooth waveform ±25KHz. Program radio to L or H signal generator frequency.	Adjustment same as Method 1.	
4.	Discriminator Adjustment	No input signal and radio programmed 146.05.	Adjust T1 to give 2.75v ± .1v at pin 9 of IC2	Conventional disc. should not be used on this radio. The window det.circuit relies on proper adj. of this coil.

NO.	DESCRIPTION	INPUT SIGNAL	ADJUSTMENT	NOTES
5.	L-Band frequency alignment	Preferred method 1--none	Measure freq.*at pin 14 of IC6 - adjust C25 for 2.6MHz exactly. *Counter accuracy .003% or better (±80Hz)	
		Method 2 Apply a 33-35MHz L-Band signal @ 1mv. The accuracy of the signal generator or counter on the signal generator must be .0003% (3ppm) or ±150Hz.	Measure IF with counter at TP6. Adjust C25 for 400KHz ±50Hz	Couple TP6 thru a .005uf cap. to counter
6.	H & U/T frequency alignment	Method 1 Apply any U/T-Band signal (450-512). Accuracy of generator or counter on generator must be .0004% (4ppm) or ±2000Hz. Program radio to U/T signal frequency	Measure I.F.with counter at TP6 - adjust L12 for 400KHz ±500Hz.	Adjust of L12 aligns H & U/T-Band
		Method 2 No input signal. Radio on H or U/T channel using a pick-up loop (9-10 turns 18-22ga, wire on 3/4" dia. attached to coax) monitor on a frequency counter 133MHz. Accuracy of counter must be .0002% (2ppm) or ±330Hz	Adjust L12 for 133MHz exactly--pick-up loop placed near Y2.	Some detuning of 133 osc. may occur if loop is too tightly coupled. Use minimum coupling to get an accurate counter reading.

NO.	DESCRIPTION	INPUT SIGNAL	ADJUSTMENT	NOTES
7.	U/T Sensitivity alignment	453.25MHz @ 2uv to antenna input. Program radio to 453.25MHz.	Adjust R56 for best quieting at audio output (tuning voltage at TP5 will be approx.6.7v.)	It may be necessary to reduce sig.level below 2uv to the point where the effect of adjusting R56 can be measured.
8.	H-Band Sensitivity Alignment	Apply a 146.05 signal @ 1uv to antenna input. Program radio to 146.05	Adjust L4 & L9 for best quieting at audio output	It may be necessary to reduce signal level and re-adjust L4 & L9.
9.	L-Band Sensitivity Alignment	Apply 40-42MHz signal @ 1uv to antenna input. Program radio to test frequency	Adjust L5 & L10 for best quieting at audio output	It may be necessary to reduce signal level and re-adjust L5 & L10.
10.	2KHz squelch adjustment	Apply 2KHz ±40Hz to junction of R39 and R54 through a .1uf capacitor. Program radio to a channel with no activity. 4v p-p input (1.4 VRMS)	Adjust R73 for maximum AC voltage (approx. 4.2mv) at C55 & R70 Junction.	Adjust input signal level to produce

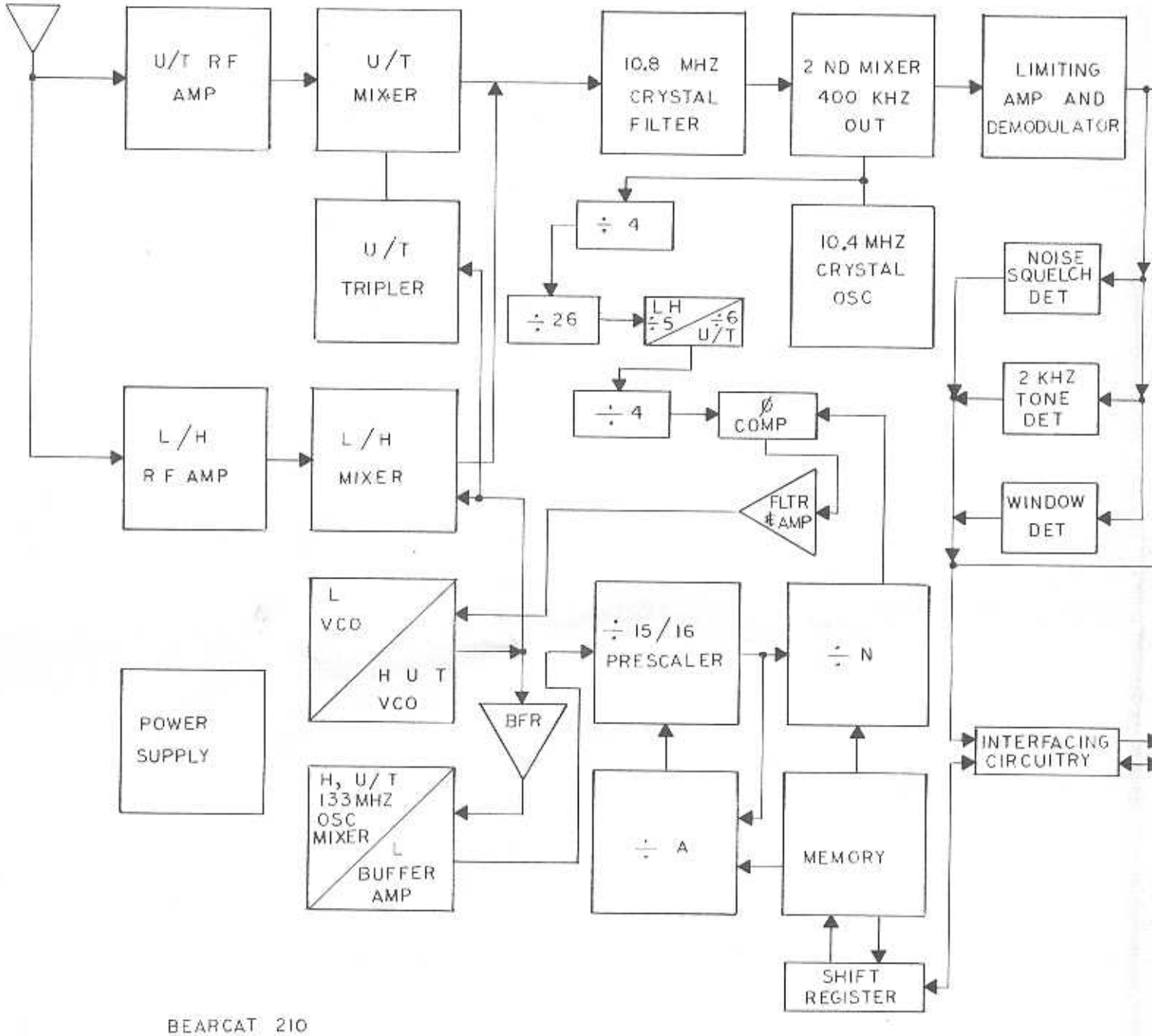
SYMPTOMS & CURES FOR BC 210

SYMPTOMS	CURES
R. F. Difficulties	
No L Band	Q5, Q6, D11, D15, D21, D22
No H Band	Q6, D11, D15, D21
No U/T Band	Q5, D22, IC-1
No L & H Band	Q5, Q9
L Band weak	IC-1
H Band weak	Q2, IC-1
U/T Band	IC-1
L & H Band weak	IC-1
Low end of L Band won't oscillate	L17 should be a 33uh (replace if not)
High end of L Band won't oscillate	IC-6 (heat sensitivity)
Low end of H Band & high end of U/T Band won't lock in	Add a 3.3PF to C15
Low end of H Band won't lock in	Change C8 to a 15PF, Y1
H & U/T VCO won't adjust	Q1, Y2
Won't receive strong signals	Check IF alignment, IC2
2kc trap doesn't work	Adjust T1, R73, replace IC-5
Unit Dead - No display or audio	T2, IC-3, IC-5, D27, Q8
Squelch Difficulties	
No I.F.	IC-2, FL1, FL2, T3, T4
Will not squelch	IC-2, D2
Will not un-squelch	IC-2
Audio Difficulties	
When scanning unit has audio	IC-2
No Audio	IC-3
Distorted Audio	IC-3
Power Supply Difficulties	
6 Volt High or Low	IC-5, IC-6, D27
10 Volt High or Low	IC-5, IC-6, D27
16 Volt High or Low	IC-3, IC-5, D8, D9
25 Volt Low	Y1, IC-1, IC-6, IC-7, Q3, D16, D17 D18, D19
Display Difficulties	
In search mode the readout reads High or Low	IC-13, alignment not correct Y1, Y2
No Display	Flex strip from display to circuit board, power supply voltage not correct. IC-12.
Missing one segment in all digits	Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18, flex strip
Missing one segment in one digit	Display
Missing one digit	Q19, Q20, Q21,Q22, Q23, Q24, Q25, Q26, Q27, Q28, flex strip, IC-12

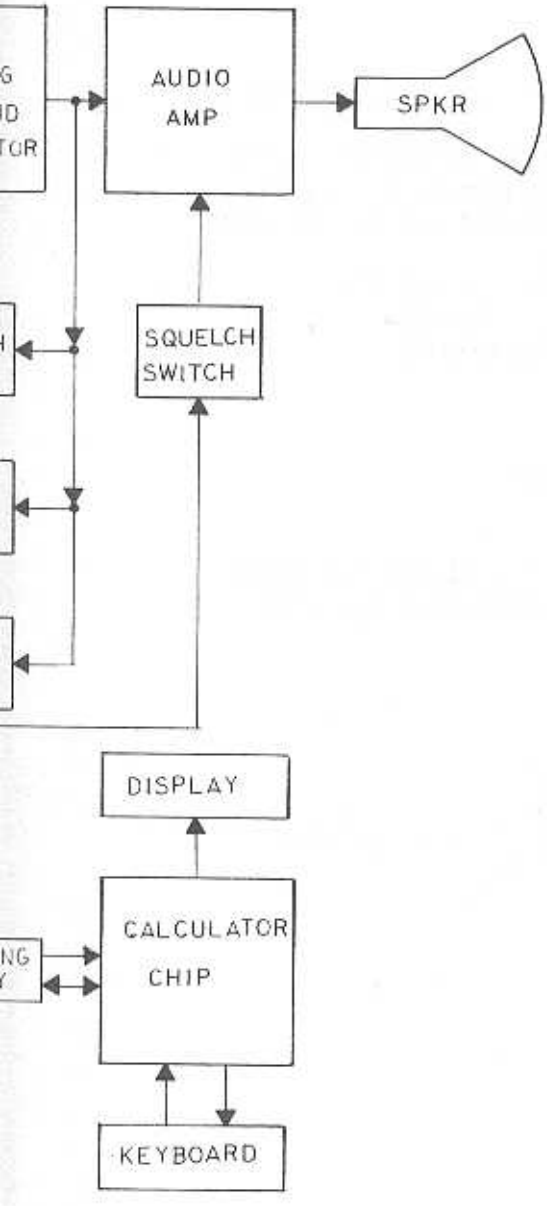
Program Difficulties

Won't program	IC-6, IC-7, IC-8, IC-9, IC-10, IC-II, IC-12 *
Won't hold program on all channels	Battery, Battery contact, IC-7
Program advances one channel each time channel one is passed	Check for difference in pulse height from pin 10 of IC-11 and pin 9 of IC-7. Same height change IC-7, No pulse change IC-11.
Won't scan	IC-8, IC-12, Keyboard
No Man Scan	Q11, Keyboard
No Lock-out	Keyboard
No Delay	Keyboard, IC-12
No Search	Keyboard

(*) Note: When entering a valid program check pins 17 and19 of IC-7 for a downward pulses, check pin #18 of IC-7 for upward pulses.



BEARCAT 210
BLOCK DIAGRAHM
FIGURE 1



Rev	EN	Description & Location	Int.	date

Part No. XC668

Rev.

Ref. Models

Approx. Scale NONE		DO NOT SCALE DWG.	
Originator KAY	date 2-2-78	Mech. Eng.	date
Dev. Eng.	date	Prod. Eng.	date

Tolerances unless otherwise specified
2 Place dec. ± .010 3 Place dec. ± .005
Fractions ± 1/64 Angles ± 1/2°

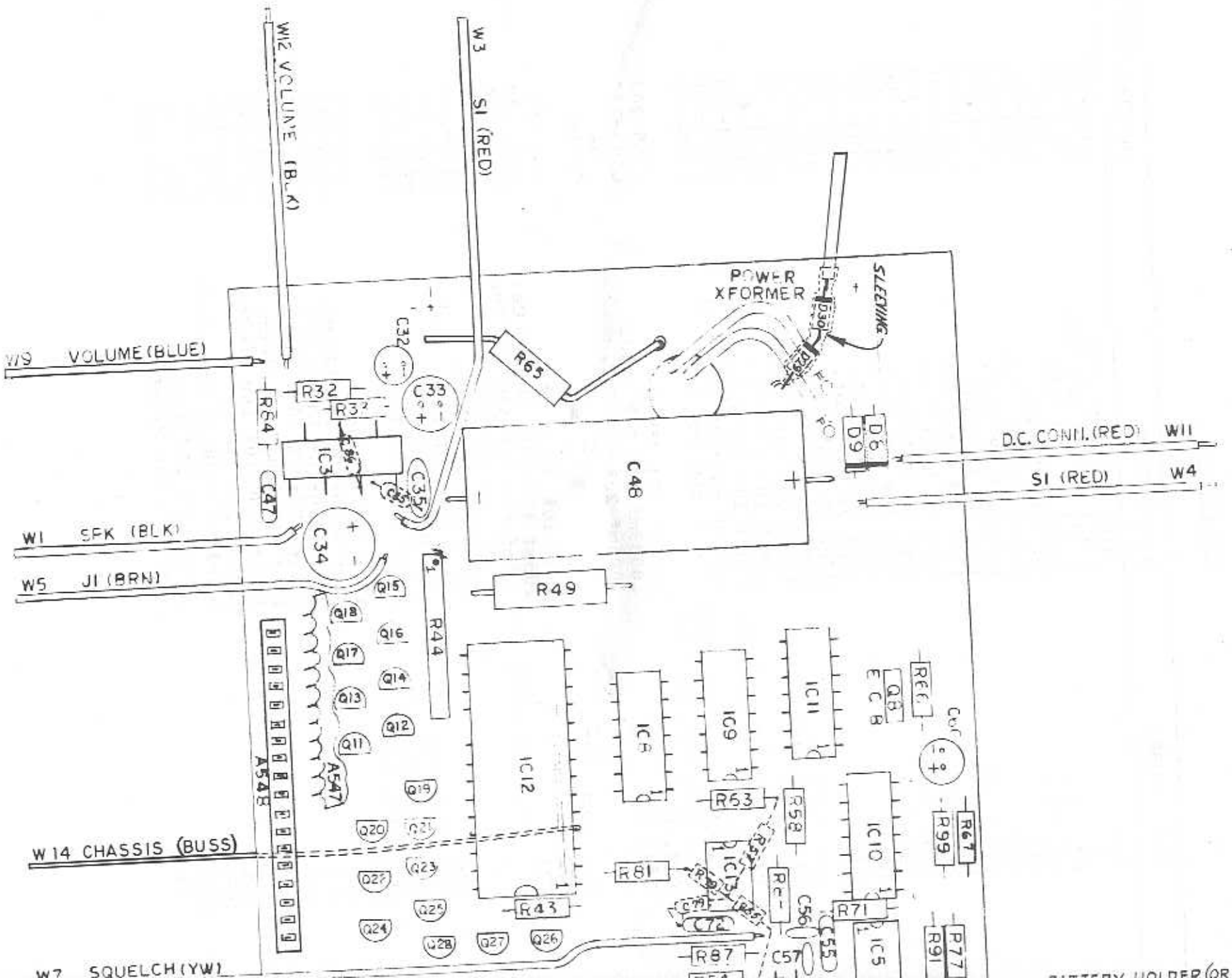
Electra COMPANY
DIV OF MASCO CORP OF IND
CUMBERLAND IND 46229

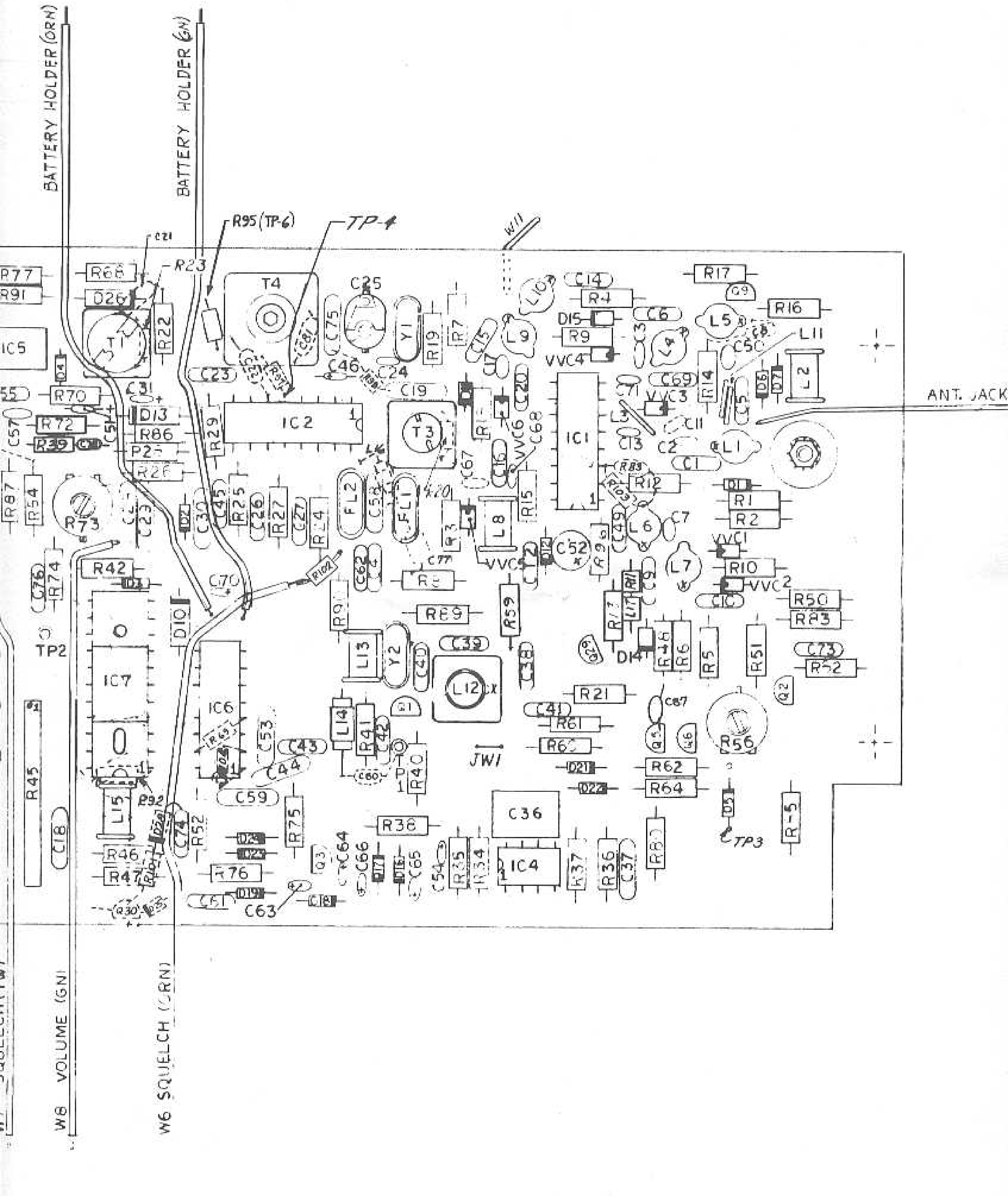
Title SCHEMATIC-BLOCK DIAGRAM

Part No. XC668 Rev.

CAPACITORS

PART NUMBER	DESCRIPTION	ELECTRA NUMBER
C58	.82pf 10% Cer. NPO	C905-000
C5	2.2pf ±.25pf NPO Cer.	C103-022
C2, C50	3.3pf 5% NPO Mini	CJ01-033
C4, C42	5pf 5% NPO Cer.	C101-050
C69	6.8pf 10% NPO Cer.	C102-068
C67	8.2pf 5% NPO Cer.	C101-082
C11, C49	10pf 5% NPO Cer.	C101-100
C23	10pf 10% NPO Cer.	C102-100
C7, C71	15pf 5% N150 Mini	CJ03-150
C39, C40	15pf 5% NPO Cer.	C101-150
C80, C83	22pf 10% NPO Cer.	C102-220
C8	33pf 20% NPO Cer.	C104-330
C75	39pf 5% N150 Cer.	C110-390
C24	47pf 5% N150 Cer.	C110-470
C13, C68	47pf 5% N750 Mini	CJ07-470
C41, C73, C12	100pf 20% Y5F Cer.	C133-101
C26, C27	470pf 10% Y5F Cer.	C132-471
C6, C9, C15, C74, C87	470pf 20% Y5F Cer.	C133-471
C3, C17	.001mf +80-20% Z5U Mini	CJ13-102
C1, C10, C14, C16, C20	.001mf Z5U GMV Cer.	C345-102
C38, C43, C45, C62,C86,C78		
C29, C47	.002mf 20% Z5U Cer.	C305-202
C56, C57	.0033mf 10% Z5P Mylar	C503-332
C76	.005mf 20% Z5U Cer.	C304-502
C19, C28, C30, C44, C53, C59, C77	.01mf 20% Z5U Cer.	C304-103
C72	.047 10% Mylar	C503-473
C21	.05mf +80-20% Z5U 12v Cer.	C320-503
C22, C61, C81, C85	.1mf +80-20% X5U 12v Cer.	C331-104
C35	.1mf 20% 16v Z5U Cer.	C302-104
C31	.22mf 20% 10v Tant.	C602-224
C36	.47mf 10% Z5P Poly	C503-474
C37, C54, C82	.47 20% 35v Tant.	C606-474
C46, C51, C63, C64, C65, C66, C79	2.2mf 20% 25v Tant.	C605-225
C70	10mf 20% 6v Tant.	C601-106
C60	22mf +100-10% 16v Elect.	C733-226
C32	22mf +100-10% 10v Elect.	C732-226
C52	100mf +80-20% 16v. Elect.	C753-107
C33	47mf +100-10% 16v Elect.	C733-476
C34	220mf +100-10% 16v Elect.	C733-227
C48	2200mf 25v Elect.	C707-228
C25	1.7-16pf Plastic Var. Cap.	CB74-301
C78	.001mf 20% Z5U 50v.	C303-102
C55	.01mf 10% 35v Mylar	C501-103


W12 VOLUME (BLK)
W3 S1 (RED)
W9 VOLUME (BLUE)
POWER XFORMER
SLEEVING
C32
C33
R65
R32
R32
R64
IC3
C47
C35
C48
D6
D9
D.C. CONN. (RED) W11
S1 (RED) W4
W1 SPK (BLK)
C34
W5 J1 (BRN)
R49
Q15
Q18
Q16
Q17
Q14
Q13
Q12
Q11
R44
A547
A548
IC12
IC8
IC9
IC11
R63
R58
IC10
R67
R99
W14 CHASSIS (BUSS)
R81
R43
R71
C56
C55
IC5
R91
R77
W7 SQUELCH (YW)
R87
C57
BATTERY HOLDER (ORN)


BATTERY HOLDER (ORN)
BATTERY HOLDER (GN)
R95 (TP-6)
TP-4
W11
ANT. JACK
TP2
TP3
JW1
IC1
IC2
IC4
IC5
IC6
IC7
T1
T3
T4
C36
W8 VOLUME (GN)
W6 SQUELCH (ORN)

RESISTORS

PART NUMBER	DESCRIPTION	ELECTRA NUMBER
	CARBON FILM	
	All Resistors 1/4w, 10% unless otherwise noted	
R44	Res. Network 8-22K	RA54-201
R45	Res. Network 10-180	RA54-901
R56	100k Trimpot (Piher PT10v)	RB71-502
R73	500 ohm Trimpot (Piher PT10v)	RB71-503
R30	Pot 100K (Squelch)	RC53-601
R31	Pot-switch 100K	RC53-602
R65	2.2M 1/2w 10% Carbon Comp.	R214-225
R49	18 ohm 1w 10%	R305-180
R68	10K 2% ½w	R303-103
	INDUCTORS	
L1	Loading Coil	LB53-402
L2, L15	Choke	LA21-801
L3	Coil	LA50-802
L4, L9	H-Band (Orange)	LB53-503
L5, L10	L-Band (Blue)	LB53-403
L11	Choke 1 1/2 turn #22Awg	LA50-901
L12	Osc. Coil (Green)	LB53-502
L13	Coil (Red)	LA21-806
L14	Choke 2.5 uh. 10%	LA54-501
L16	Choke	LA20-501
L17	33uh.10%	LB46-303
T1	Quad Coil 400KHz	LB53-301
T2	Power Transformer	TB29-702
T3	IF Trans. (10.8MHz)	TB52-003
T4	IF Trans. (400KHz)	TB57-801
	SEMI-CONDUCTORS	
Q1, Q29	2N3563	QB75-901
Q2	Mot.SPF792	QB76-101
Q3	MPS-A13	QB82-001
Q5, Q6, Q9, Q19, Q20 Q21, Q22, Q23, Q24, Q25, Q26, Q27, Q28	2N4126	QC59-602
Q8	92PE 77A	QB76-402
Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18	MPS-3393	QC58-102
Q30	MPS-3640	QC59-201

SEMI-CONDUCTORS

PART NUMBER	DESCRIPTION	ELECTRA NUMBER
D1, D2, D3, D4, D5, D6, D7, D12, D13, D16, D17, D18, D19, D23,D24,D25,D26	IN-4148	DB73-602
D8, D9, D29, D30	IN-4002	DB70-301
D10	IN34A	DB68-401
D11, D14, D15	MPN-3401	DB73-101
D21, D22, D28	IN755A (7.5v. 5% 400mw)	DB70-801
D27	IN5233B 6v 5% Zener	DB72-302
VVC1, VVC2, VVC3, VVC4, VVC5, VVC6	Siemens BB209 Tuning Diode (matched)	DB70-601
IC1	NC57801 (custom)	NC57-801
IC2	SC8780P or Motorola MC3357	NB53-101
IC3	SGS/ATES #TBA820	NB66-201
IC4	SC74012P (custom)	NB61-301
IC5, IC13	LM358N	NB73-402
IC6	NC57902 (custom)	NC57-902
IC7	B257-2 (custom)	NB25-702
IC8, IC9, IC10, IC11	MC14011CP	NB67-901
IC12	TMC 0983C (custom)	NB73-303

MISC. ELECT. & MECH.

	Keyboard	BC51-801
	P.C. Board	BD22-102
	Plug Button (Auto Mount Holes)	HA27-101
	Antenna Insulator	HA21-501
	Mobile Mtg.Bracket	HB23-402
	Squelch or Volume Knob	HB46-402
	Battery Holder Cap	HB61-401
	Key Tops (indicate # or word)	HC493XX
	Front Panel	HD11-301
	Wrap Around	HD11-401
	Antenna Plug	JA12-701
	Antenna Jack	JA36-201
	Speaker Jack	JB47-401
	Antenna	MA13-802
	AC Power Cord	MC64-703
	DC Power Assembly	MB66401
	2 amp 3AG Fuse	MA37-602
	Battery 1.5v (Mallory 10L123)	MA61-201
SPK1	Speaker	MB33-202
	Display (BC-210)	MC52-001
Y1	10.4MHz Crystal	YA53-801
FL1	10.8MHz Crystal Filter	YA55-901
FL2	10.8MHz Crystal Filter	YA60-101
Y2	133MHz Crystal	YA61-001

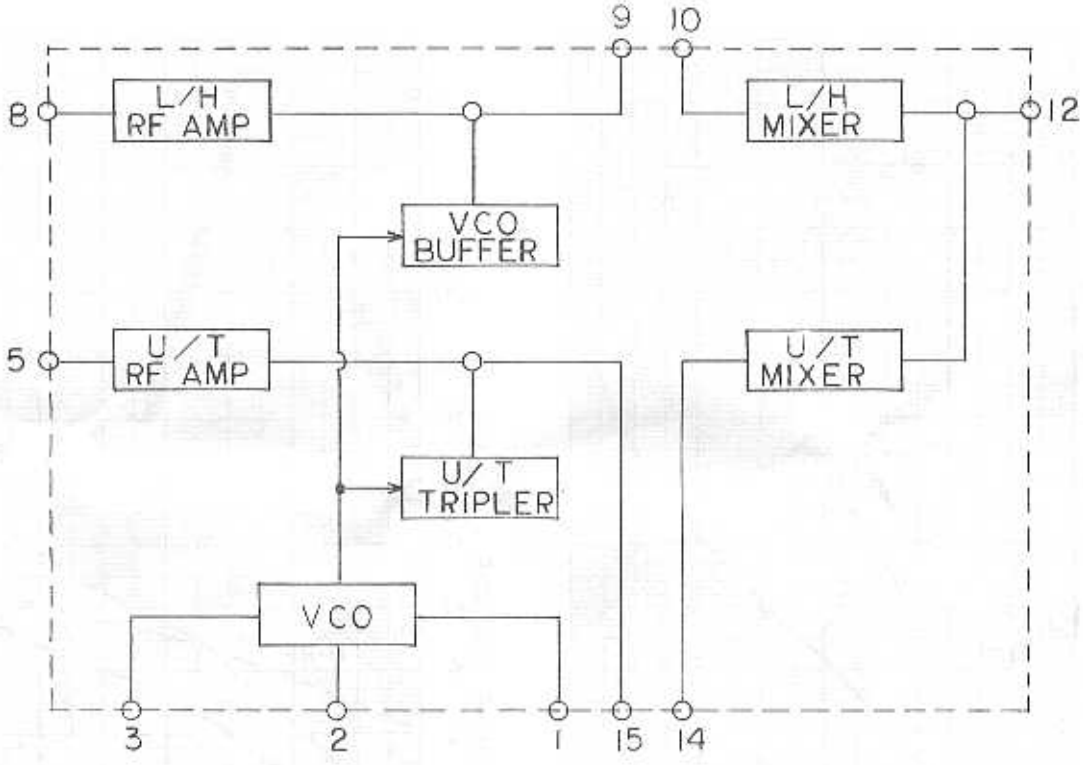


FIGURE 2
IC-1 NC5780I

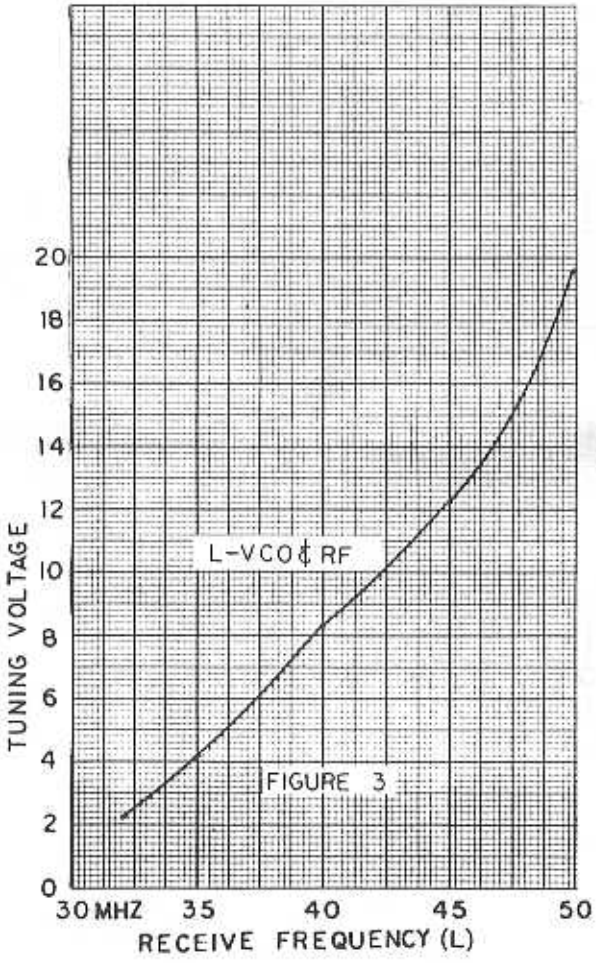


FIGURE 3

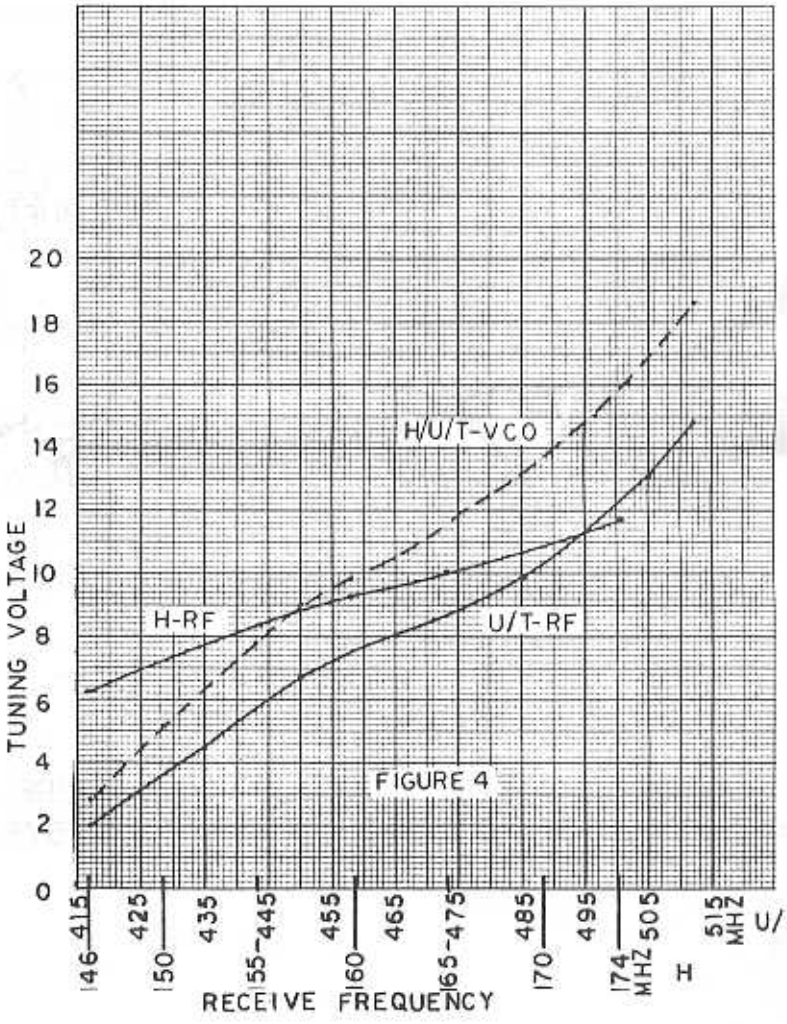


FIGURE 4

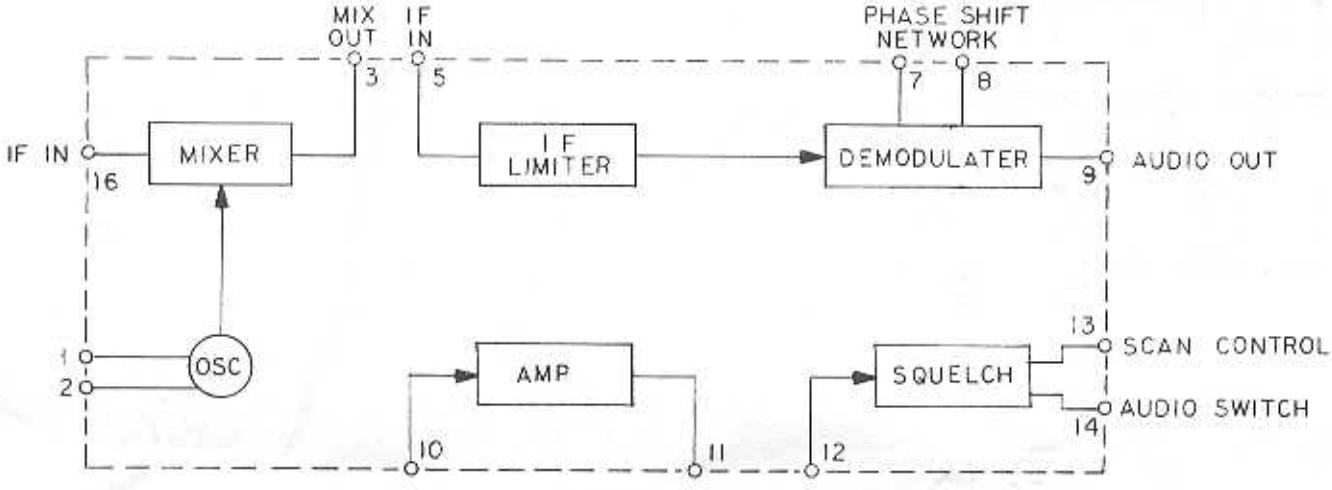
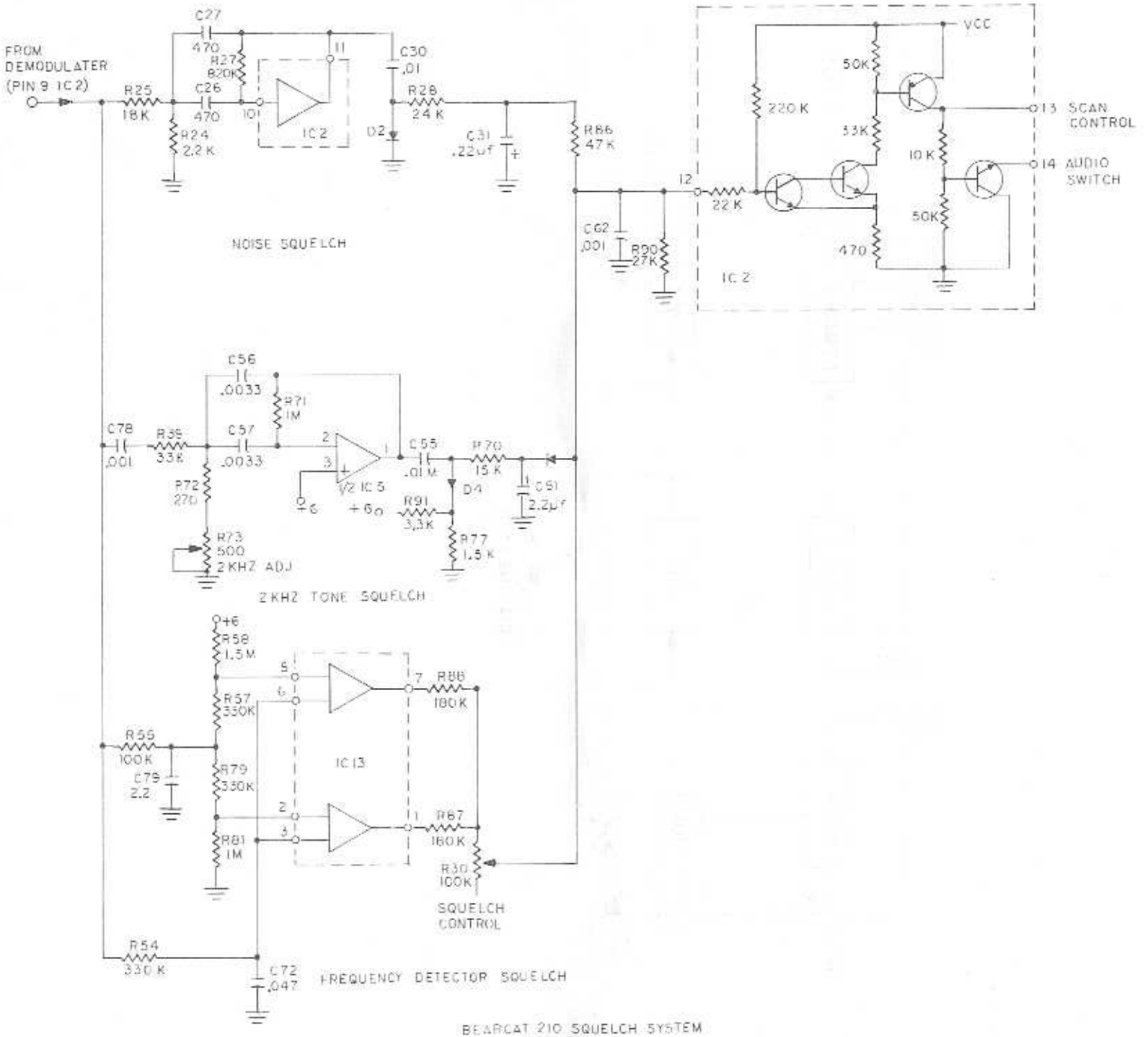
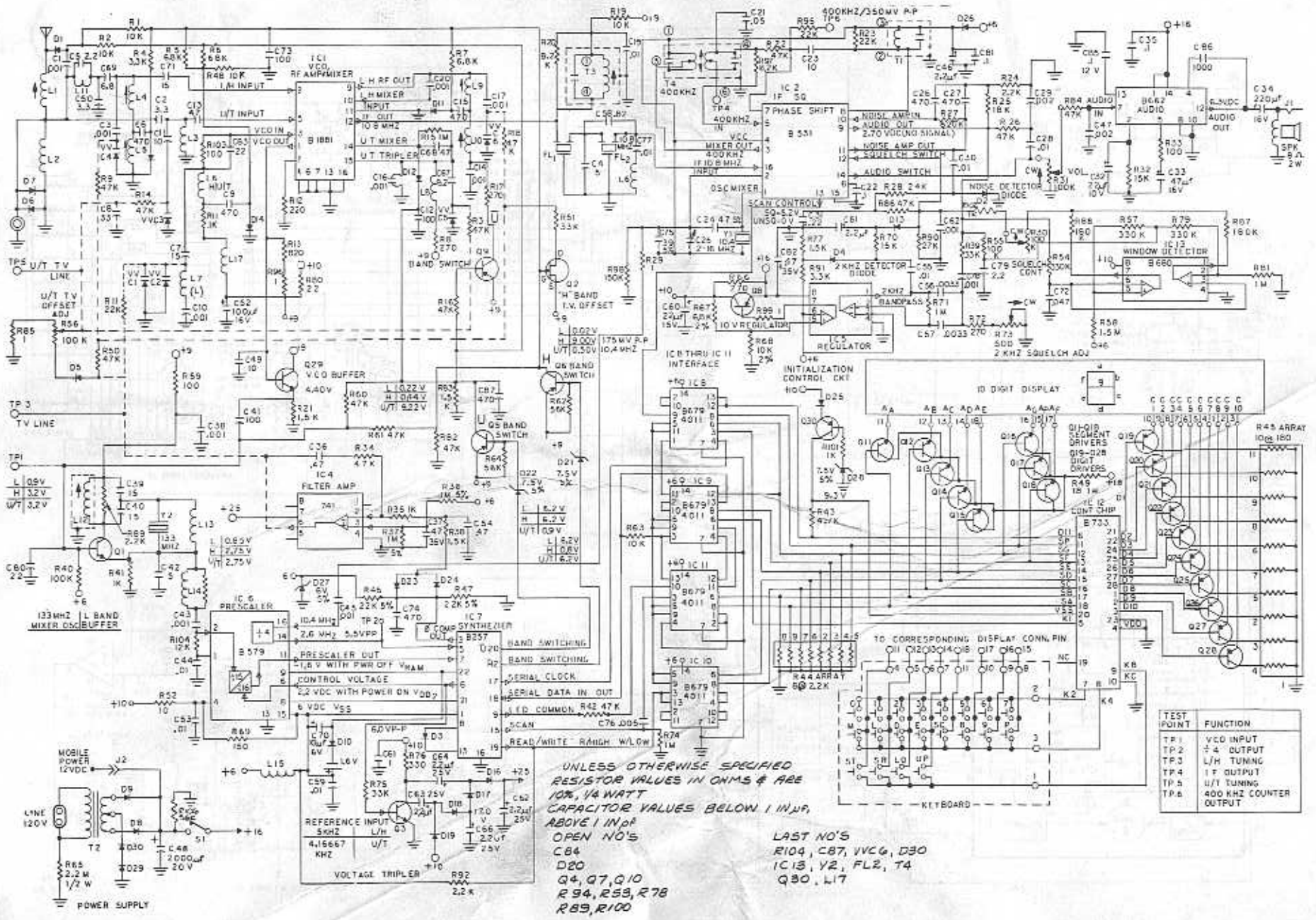


FIGURE 5
IC-2 NB53101



BEARCAT 210 SQUELCH SYSTEM
FIGURE 6



TEST POINT	FUNCTION
TP1	VCO INPUT
TP2	÷4 OUTPUT
TP3	L/H TUNING
TP4	I F OUTPUT
TP5	U/T TUNING
TP6	400 KHZ COUNTER OUTPUT

UNLESS OTHERWISE SPECIFIED
RESISTOR VALUES IN OHMS & ARE
10%, 1/4 WATT
CAPACITOR VALUES BELOW 1 IN μF,
ABOVE 1 IN pF
OPEN NO'S
C84
D20
Q4, Q7, Q10
R94, R53, R78
R89, R100

LAST NO'S
R104, C87, VVC6, D30
IC13, Y2, FL2, T4
Q30, L17

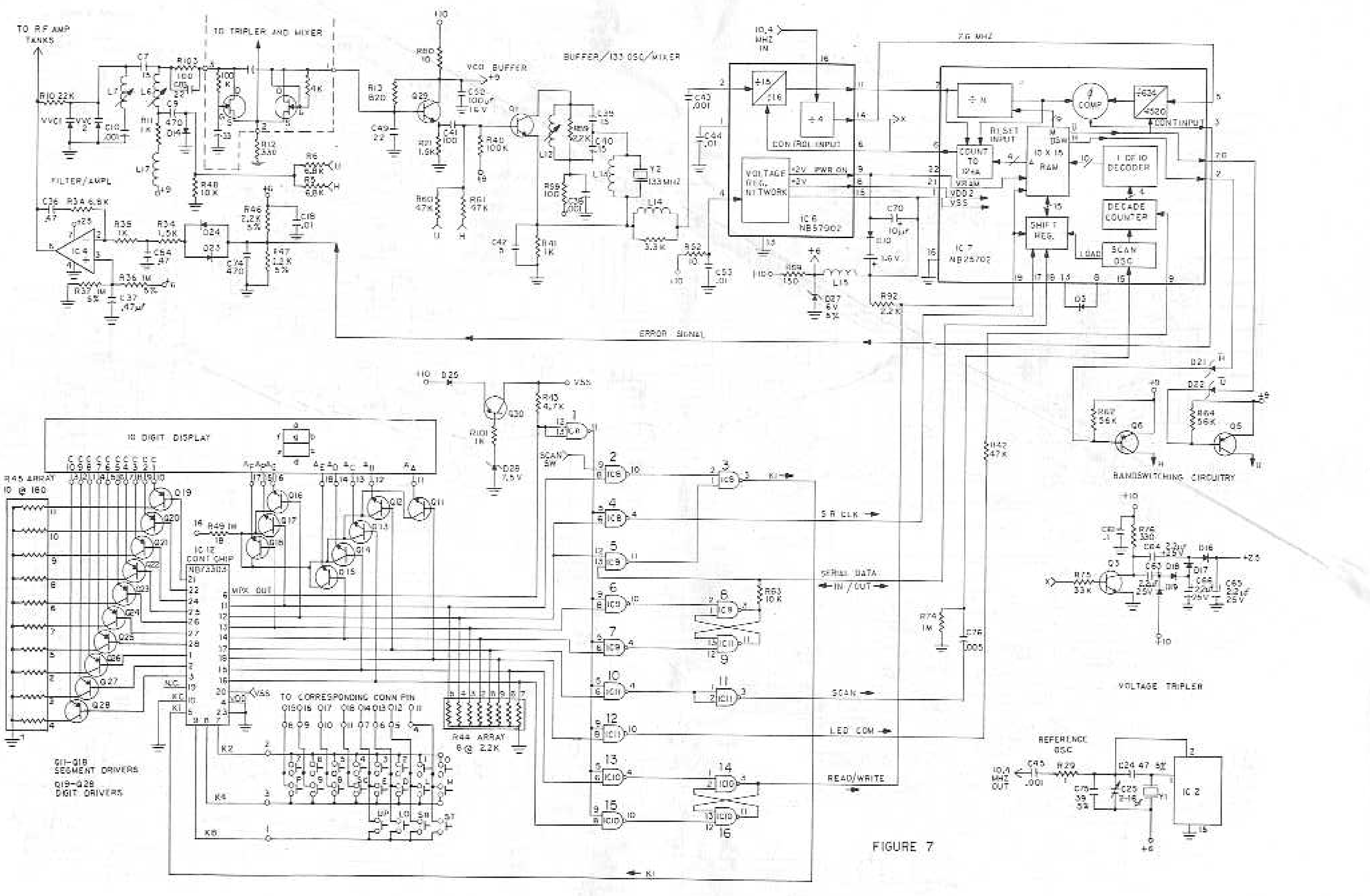

TO R.F. AMP TANKS
TO TRIPLER AND MIXER
BUFFER/133 OSC/MIXER
VCO BUFFER
FILTER/AMPL
10.4 MHZ IN
7.6 MHZ
IC 6 NB57002
VOLTAGE REG. NETWORK
CONTROL INPUT
IC 7 NB25702
COUNT TO 124A
RESET INPUT
10 X 15 RAM
1 OF 10 DECODER
DECADE COUNTER
SHIFT REG.
SCAN OSC
LOAD
COMP
CONT INPUT
ERROR SIGNAL
BANDSWITCHING CIRCUITRY
VOLTAGE TRIPLER
REFERENCE OSC
10.4 MHZ OUT
IC 2
10 DIGIT DISPLAY
R45 ARRAY 10 @ 180
IC 12 CONT CHIP NB72303
MPX OUT
TO CORRESPONDING CONN PIN
R44 ARRAY 8 @ 2.2K
S R CLK
SERIAL DATA IN/OUT
SCAN
LED COM
READ/WRITE
SCAN SW
Q11-Q18 SEGMENT DRIVERS
Q19-Q28 DIGIT DRIVERS

FIGURE 7