Circuit Description (UHF version)

Receive Signal Path

Incoming RF from the RX antenna jack is delivered to the RX Unit and passes through the bandpass filter consisting of coils L4025, L4024 and L4002, capacitors C4105, C4106, C4107, C4007 & CV4001. Signals within the frequency range of the receiver are then amplified by Q4010 (SGM2016). The amplified RF is then bandpass filtered again by CV4002 to ensure pure in-band input to first double-balanced mixer D4003 (DBM0127).

Buffered output from the VCO Unit is amplified by Q4012 (2SC3357) and low-pass filtered by L4012, L4013, C4043, C4045 and C4047, to provide a pure first local signal between 352.1 and 464.1 MHz to the first double-balanced mixer. The 47.9 MHz first mixer product is amplified by Q4017 (2SC3356), then passed through dual monolithic crystal filter (± 7.5 kHz BW) XF-4001 (48L15B1-1), to strip away all but the desired signal, which is then amplified by Q4025 (2SC3356).

The amplified 1st IF signal is then applied to FM IF subsystem IC Q4018 (MC3372D), which contains the 2nd mixer, 2nd local oscillator, limiter amplifier, noise amplifier, and squelch gates. A 2nd L.O. signal generated from 47.445-MHz crystal X4003 produces the 455 kHz 2nd IF when mixed with the 1st IF within Q4018. The 2nd IF passes through ceramic filter CF4001 (CFW455E) to strip away any unwanted mixer products, and is applied to the limiter amp in Q4018. This removes amplitude variations in the 455 kHz IF before detection of modulation by ceramic discriminator CD4001 (CDB455C16). The detected audio is amplified by Q4016-1 (NJM2902M) and delivered to J4002 pin 1 (DISC OUT).

Squelch Control

When no carrier is received, noise at the output of the detector stage from Q4018, pin 9, is sampled and fed to squelch gate Q4022 (2SA1179), VR4001 adjusts the squelch threshold before delivery to the 3-pole active bandpass filter formed by Q4026 and Q4027 (both 2SC2812), where the audio is high-pass filtered and audio frequencies above 5 kHz are rejected. The noise signal is next amplified by Q4023 and Q4021 (both 2SC2812), then rectified by diode D4004 (1SS226) to produce a DC control voltage for the squelch switch section in Q4024. This resulting DC voltage is amplified by Q4016-4 (NJM2902M). The output of Q4016 is then compared with a 9-V reference voltage at Q4016-3. The open-collector output voltage from analog switch Q4024 (DTC144EK) is delivered to J4001 pin 7 (NSQ DET) and on to microprocessor Q1008 pin 26 (NSQ DET).

Then Q1009 pin 14 (LINE OUT) goes high, turning on analog mute gate Q2004-4 (NJU4066DM) on Control Unit 2, allowing audio to pass from J2007 (DISC IN) through audio stages discussed earlier (Q2011 and Q2006) to analog switch Q2007 (MC14053).

S-Meter

S-meter signal output from pin 13 of Q4018 (MC3372D) is applied to C4081, where the 455 kHz signal is rejected (filtered), and to buffer amplifier Q4016-2 (NJM2902M) through J4001 pin 1 to CNTL-1 Unit.

CTCSS Operation

A CTCSS (Continuous Tone-Coded Squelch System) is provided by programming via CE-8 Software. The CTCSS IC Q2008 (MX165CLH) contains a CTCSS tone encoder for any one of 39 subaudible tones. The CTCSS audio level output from pin 16 of Q2008 is amplified by Q2005-1(NJM2902M), and adjusted by VR2003 before injection into the audio chain at Q2003-2 (NJM2902M).

RX PLL Circuit

PLL circuitry on the RX unit consists of PLL subsystem IC Q4014 (MC1415190F), which contains a reference oscillator/divider, serial-to-parallel data latch, programmable divider, and a phase comparator. Stability is obtained by a regulated 5-V DC supply via Q4001 (TA78L05) to Q4011 (DTA143EK) and temperature-compensating capacitors associated with the 12.8-MHz frequency reference crystal X4002 (GFS-720).

RX Unit VCO Q5501(2SK508) oscillates between 352.1 and 464.1 MHz according to the programmed receiving frequency and repeater version type (see chart on page 1-2). A sample of the VCO output is amplified by Q4015 (2SC3356) and returned to the prescaler/swallow counter in Q4014. There the VCO signal is divided by 64 or 65, according to a control signal from the data latch section of Q1008 on CNTL-1 Unit, before being applied to the programmable divider section of the PLL chip.

The data latch section of Q4014 also receives serial dividing data from microprocessor Q1008 on CNTL-1 Unit, which causes the pre-divided VCO signal to be further divided by 28,168 ~ 46,410 in the programmable divider section, depending upon the desired receive frequency, so as to produce a 10-kHz or 12.5-kHz derivative of the current VCO frequency. Meanwhile, the reference divider section of Q4014 divides the 12.8-MHz crystal reference by 1280 (or 1024) to produce the 10-kHz (or 12.5-kHz) loop reference (respectively).

The 10-kHz or 12.5-kHz signal from the programmable divider (derived from the VCO), and that derived from the crystal are applied to the phase detector section of Q4014, which produces a dual 5-V pulsed output with pulse duration depending on the phase difference between the input signals. This pulse train is then converted to DC, low-pass filtered, then fed back to varactor diodes D5501, D5502, on the RX Unit.

Changes in the level of the DC voltage applied to the varactor diodes affect the reactance in tank circuit VCO Q5502, changing the oscillating frequency according to the phase difference between the signals derived from the VCO and the crystal reference oscillator. The output of receiver VCO Q5501, after buffering by Q5502, is delivered for amplification by Q4013 (2SC3356) before application to the first mixer, as described previously.

Transmitter

Transmitter VCO Q5001 (2SC508) oscillates between 400 and 512 MHz according to the programmed TX frequency. The theory of operation of the remainder of the PLL circuitry is similar to that of the RX VCO unit. However, dividing data from the microprocessor is such that the VCO frequency is the actual transmit frequency (rather than offset for IFs as in the receiving case).

IDC-processed speech audio from CNTL-2 Unit is pre-emphasized by C2013, R2018 and Q2002-4 (NJM2902), before application to the TX VCO. Speech audio is delivered to diode D5003 (1SV229) from Control Unit 2, frequency modulating the PLL carrier up to ± 5 kHz from the unmodulated carrier at the transmitting frequency.

DCS modulation from CNTL-2 Unit is low-pass filtered by Q3001 (NJM2904M), then applied to both the VCO and to the PLL frequency reference, via crystal oscillator unit X3001 (GFS-720). The modulated signal from the TX VCO unit is buffered by Q5002 (2SC3356) and Q3005 (2SC3356), then passes through buffer-amp Q3007 (2SC3356). The signal then enters RF diode switch D3004 (HSU277) and amplifier Q3011(2SC3357). The signal level is then attenuated before delivery to the PA Unit. The low-level transmit signal passes through buffer amp Q6001 (2SC23357) before being applied to pre-driver amplifier Q6002 (MRF559).

The transmit signal is finally amplified by PA module Q6003 (M57729) up to 25 watts. Harmonic and spurious radiation in the final output is suppressed by a 5-pole low-pass filter formed by inductors L6008, L6009 and L6010 and capacitors C6016, C6017, C6018, C6019 and C6020 on the PA unit, before delivery to the TX antenna jack. If a CTCSS tone is enabled for transmission, the subaudible tone from the CTCSS IC Q2008 (MX165CLH) is low-pass filtered, then mixed with the IDC-processed speech audio.

APC (Automatic Power Control)

RF power output from final amplifier Q6003 (M57729) is sampled by C6023 and delivered to detector diode D6003 (1SS319) where it is rectified. The resulting DC voltage (DET) is delivered to the REG Unit. There the APC voltage is fed through buffer amplifier Q7003-1 to comparator Q7003-4 (both NJM2902M) where the voltage is compared with a reference voltage from the CPU (POWER REF) to produce a control voltage to the Automatic Power Controller Q6005 (2SB1134R), which regulates supply voltage to RF power module Q6003, to maintain stable high or low output power under varying antenna loading conditions.

CNTL-1 Unit

CNTL-1 Unit consists of 8-bit microprocessor Q1008 (M38063EGP), 256-kByte EPROM Q1015 (TMS27C256), EEPROM Q1002 (BR93C56), and various analog switches. Microprocessor operational code is stored in Q1015, while channel and optional data, and repeater configuration information, is programmed from an external computer at 4800 bits/sec. connected to J2008 on CNTL-2 Unit, and stored in Q1002 via programming cable connection to J2008 on CNTL Unit 2.

The output from microprocessor Q1008 contains three-line serial control data (DATA, CLOCK & ENABLE) used for repeater/base mode control, TX and RX PLL data, and to control analog switch Q2004 (NJU4066-BM) on CNTL-2 Unit.

Crystal X1001 oscillates at 4.9152 MHz, and provides stable clock timing for the microprocessor. When the repeater is powered on, the voltage at pin 71 becomes stable, and the output of voltage detector IC Q1017 (Q1008 pin 25- RST) becomes high, resetting the CPU and initializing it for operation.

First, the CPU performs an initialization routine which loads the operating program from RAM, and frequency and other system data from Q1002. The CPU then sends PLL and analog switch control data (J1001 pins 2, 3, & 4; and J1002 pins 2, 3 & 4), to prepare the repeater for operation. If an abnormal signal (such as PLL unlock or HI TEMP) is detected at pin 2 or pin 6 of the CPU, CPU pin 12 becomes low, inhibiting transmission by disabling the TX voltage rail.

Watch-Dog Timer

Watch-Dog Timer Q1018 (MC74HC4060F) monitors the CPU for thrashing. When abnormal CPU operation occurs, Q1008, pin 70 goes low, pulling diode OR gate D1018 (DAN202K), which in turn enables the pulse train generated by Q1018 to be input to pin 12.

Q1018, pin 1 then outputs a control pulse to transistor driver Q1020 (FMG2), which in turn switches the output of 5-V DC regulator Q1017 low, resetting microprocessor Q1009 at pin 25.

Three LEDs are used on CNTL-1 Unit for TX, ALARM and AC indications. The TX LED indicates the repeater is transmitting, the ALARM LED warns of four possible conditions: PLL unlock (TX & RX), high final amplifier temperature, EEPROM programming data loss and microprocessor thrashing.

CNTL-2 Unit

CNTL-2 Unit contains most of the analog switching gates used to control the various repeater interconnections. RX & TX speech audio is processed here.

Base Operation (TX, line-input audio)

Line input from J2001 pins 3 & 4 is impedance matched by transformer T2001, then delivered to audio selector Q2001 (MC14053BF). Line level can be attenuated by switch S2001 and line sensitivity can be adjusted to –10 dB ±10 dBm by potentiometer VR2001 to compensate for audio line level variations. Part of this audio is amplified by Q2015 (TDA7233D) for local speaker output.

Line audio then passes through analog switch Q2004-3 (NJU4066BM) where the audio is pre-emphasized (+6dB/octave) by C2013 & R2018 and Q2002-4 (NJM2902). The audio then passes through IDC (instantaneous deviation control) amplifier Q2003-1 (NJM2902M). Potentiometer VR2002 sets maximum deviation. The signal is then amplified by Q2003-2 before passing through the 5-section active low-pass filter formed by Q2003-4 and Q2003-3, where frequencies

above 3 kHz are attenuated and bandwidth is limited to prevent over-deviation. The CTCSS Tone audio level output is adjusted by VR2006 then delivered to Q2002-3 and the transmitter line input.

Modulated audio from the Rx unit is delivered to J2008-1 where it is fed through int/ext audio select switch S2002 to Chebyshev Filter Q2008-3 (NJM2902M) and then high-pass filtered by R2118 and R2146. The output is then delivered to five-section, active HPF Q2008-1 which rejects audio frequencies below 300 Hz. 3-pole active LPF Q2006-3 rejects audio frequencies above 3000 Hz.

Audio is de-emphasized by Q2006-2 (uPC4741G2), R2043 & C2036, providing flat response from 300 Hz ~ 3 kHz. The filtered audio then passes through attenuator S2004 and LINE output level potentiometer VR2003 to buffer amplifier Q2006-4 (uPC4741G2) and impedance matching transformer T2002 to **LINE** jack J2001 pins 1 & 2.

Repeater Operation

Duplex Operation

The demodulated audio is delivered from the RX unit to Q2008 and is high-pass filtered and de-emphasized as described above. Repeater "sensitivity" is adjusted using VR2005 before delivery to Q2005 (uPC4741G2) via repeater switch S2001-3. When the repeater mute switch Q2001-4 is closed, the gain of Q2005 is reduced to 0, effectively muting repeater audio. Repeater audio deviation is controlled by potentiometer VR2004 before the signal is delivered to audio amplifier Q2003-4, where the signal is processed in the same manner as previously described.

Intercom Function

Inserting a standard speaker/mic headset into the **INTERCOM** jack (J2010) provides closed-loop audio for test/communications with an installed remote base, for use by service technicians. Inserting the headset into the jack disables speaker audio via J2002, pins 1 & 2. Headset microphone audio is delivered to buffer amplifiers Q2007-3 and Q2007-4 (both NJM2902) before application to line audio selector Q2004.

Note!

If using the optional YH-2 headset, you can connect into either the line or Tx/Rx circuits for maintenance or testing.

Insert the **MIC/EAR** plug of the YH-2 into J2009 on the CNTL-2 unit, then slide the **INTERCOM** switch (S2003) to the desired position:

NOR - normal operation, the line is connected to the Tx/Rx circuits.

TRCV - the YH-2 is connected to the radio Tx/Rx circuits, and the base station can be keyed by pressing the blue PTT button on the CNTL-1 Unit.

LINE - the YH-2 is connected to the line; keying is not required.

Headset level is adjusted by **MON-LVL** (VR2007) on the CNTL-2 Unit. The default setting is minimum (fully counter-clockwise). *Note!* - remember to set the switch at **NOR** for normal operation *when the YH-2 is removed.*

Power Supply

The power supply includes the power transformer and bridge rectifier D0002 (S25VB20) on the chassis, a filter capacitor bank on the CAPA Unit, and various regulation and switching circuitry on the REG Unit. AC power is applied to the primary of T0001 through fuse FH0001 and relay RL0001. The 16.5-V AC at the secondary is the dual-fused by FH0002 and FH0003 before delivery to full-wave bridge rectifier D0002 and the CAPA Unit.

The output of D0002 is filtered by capacitor bank C8501 and C8502 and the resulting DC is applied to the collectors of Q7002 and Q7004 (both 2SD1842Q) on the REG Unit, and regulator IC Q7013 (FMW1). The control output of Q7103 is applied to the base of Q7007 (2SB1134R), the emitter of which then controls the bases of Q7002 and Q7004, thus highly regulating the voltages at the emitters.

This output voltage is delivered through relay RL7001 (FBR631D012) and fuse FH7001 to supply the 13.8-V DC bus for the rest of the repeater. A sample of the 13.8-V DC

from the pass transistors is also delivered to 9-volt regulator IC Q7001 (AN6541) to provide a regulated 9-volt output for repeater circuitry that requires it.

While operating from the AC power, regulated 13.8-V DC is fed through R7004 and D7002 (1SS226), providing a trickle charge for a battery that might be connected. If the AC power source is interrupted, the DC current from the battery then flows back through Q7016 (2SC2812), RL7001 and the DC fuse, which is now switched (when AC fails) to bypass R7004 and D7002, and apply full battery voltage directly to the DC bus.